aTCA-6150

Dual Intel® Xeon® 5600 Series Processor
10GbE ATCA Processor Blade

User's Manual



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Revision History

Revision	Release Date	Description of Change(s)
2.00	2011/04/12	Intial Release

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Preface

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Using this Manual

Audience and Scope

The aTCA-6150 User's Manual is intended for hardware technicians and systems operators with knowledge of installing, configuring and operating ATCA systems.

Manual Organization

This manual is organized as follows:

Chapter 1, Introduction: Introduces the aTCA-6150, its features, block diagrams, and package contents.

Chapter 2, Specifications: Presents detailed specification information, power consumption, and board layout drawings.

Chapter 3, Functional Description: Describes the aTCA-6150's functional components and board interfaces.

Chapter 4, Hardware Platform Management: Describes the hardware platform management system, including IPMI sensors, commands, and firmware upgrade procedure.

Chapter 5, Getting Started: Describes the installation of components to the aTCA-6150.

Chapter 6, Driver Installation: Provides information on how to install the aTCA-6150 device drivers.

Chapter 7, Watchdog Timer: Describes the watchdog functionality of the aTCA-6150.

Chapter 8, BIOS Setup: Describes basic navigation for the AMIBIOS®8 BIOS setup utility.

Important Safety Instructions: Presents safety instructions all users must follow for the proper setup, installation and usage of equipment and/or software.

Getting Service: Contact information for ADLINK's worldwide offices.

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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.



NOTE: Additional information, aids, and tips that help users perform tasks.



CAUTION: Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.



WARNING: Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

1.1 Overview

The aTCA-6150 is a highly integrated multi-core dual-processor AdvancedTCA processor blade supporting six sockets for DDR3-1066 VLP RDIMM up to 48GB maximum system memory capacity. IO features include two 10Gigabit Ethernet ports (XAUI, 1000BASE-KX4) compliant with PICMG 3.1 option 1/9, four Gigabit Ethernet 10/100/1000BASE-T ports to the face plate and AdvancedTCA Base Interface channels. More detailed features are outlined below and a functional block diagram is shown in the next section.

- Two Six-Core Intel® Xeon® Processor L5638 or Quad-Core Intel® Xeon® Processor L5618
- Server-class Intel® 5520/ICH10R chipset
- DDR3-1066 JEDEC standard VLP RDIMM (REG/ECC), up to 48GB
- Onboard 4GB bootable USB interface NAND flash
- Three Intel® 82576EB PCI-Express Gigabit Ethernet controllers
- Intel® 82599EB PCI-Express 10Gigabit Ethernet (XAUI) controller
- Dual PICMG 3.1 option 1/9 Fabric Interface channels
- Modular Fabric riser card for other PICMG Fabric Interface protocols
- Failover system BIOS
- Analog UXGA high color graphics

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1.2 Block Diagram

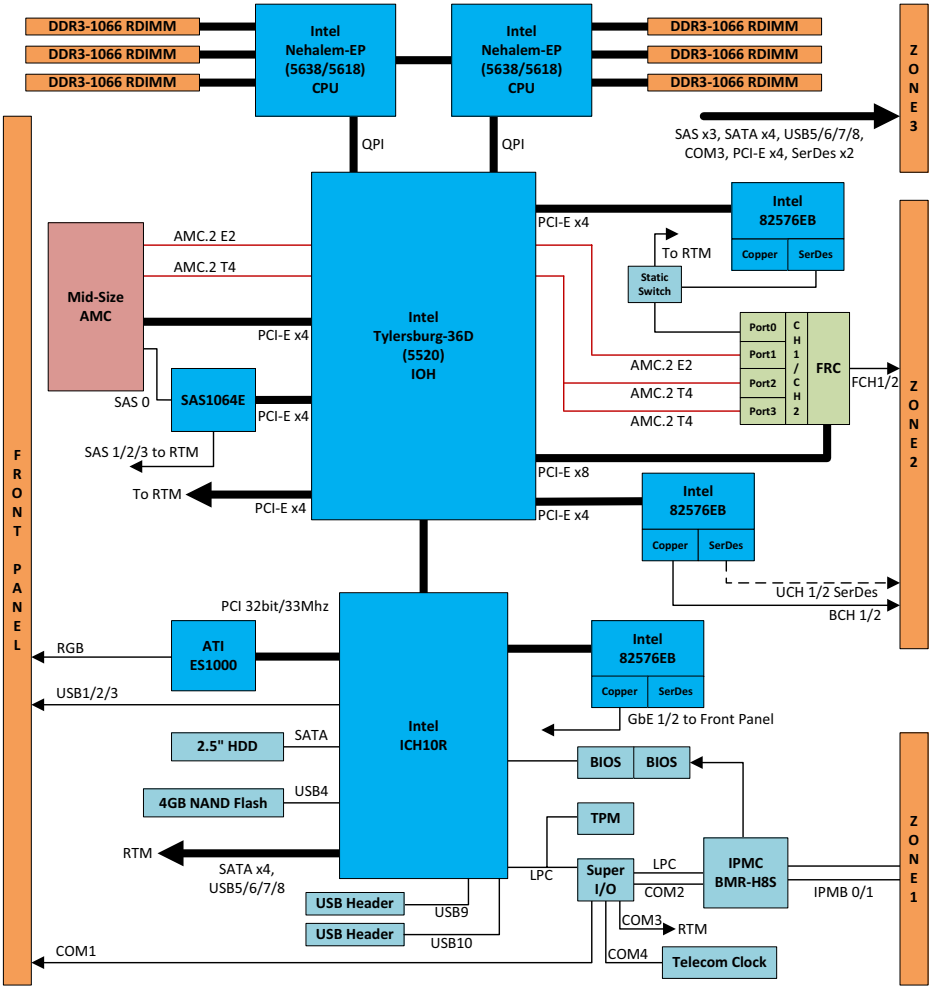


Figure 1-1: aTCA-6150 Functional Block Diagram

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1.3 Package Contents

Before opening the product box, please check the shipping carton for any damage. If the shipping carton and contents are damaged, notify the dealer for a replacement. Retain the shipping carton and packing material for inspection by the dealer. Obtain authorization before returning any product to ADLINK.

Check that the following items are included in the package. If there are any missing items, contact your dealer:

- aTCA-6150 AdvancedTCA processor blade (CPU, RAM specifications will differ depending on options selected)
- RJ-45 to DB9 cable



This product must be protected from static discharge and physical shock. Never remove any of the components except at a static-free workstation. Use the anti-static bag shipped with the product when putting the board on a surface. Wear an anti-static wrist strap properly grounded on one of the system's ESD ground jacks when installing or servicing system components.

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2 Specifications

2.1 CPU, Chipset, Memory

CPU	• SIx-core Intel® Xeon® Processor L5638 (2.00GHz QPI 5.86GT/s, 12MB L2 cache, LGA1366 package) • Quad-core Intel® Xeon® Processor L5618 (1.87GHz QPI 5.86GT/s, 12MB L2 cache, LGA1366 package)
Chipset	• Intel® 5520/ICH10R chipset
Memory	• Registered ECC DDR3-1066 SDRAM • Six RDIMM sockets • Up to 48GB

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2.2 Standards and Interface

Standards	• PICMG 3.0 R2.0 AdvancedTCA • PICMG 3.1 AdvancedTCA Ethernet option 1/9
Networking	• Three dual-port Intel® 82576EB Gigabit Ethernet controllers • Four 10/100/1000BASE-T ports (2 on face plate and 2 on Base Interface channels 1-2) • Two SerDes ports on Zone 3 to RTM • Dual 10GBASE-KX4 Fabric Interface Channels via Intel® 82599EB on aDB-6150-A riser card
Serial ATA	• Five Serial ATA II ports from ICH10R, one onboard, four to RTM
Serial Attached SCSI	• Four SAS ports from LSISAS1064E, one to AMC, three to RTM
Display	• ATI ES1000 graphics controller with 2D accelerator • DDR2-533 64MB memory • Analog RGB up to 1600x1200@75Hz refresh rate
USB	• Three USB 2.0 ports on front panel, four ports to RTM
Serial	• One RJ-45 RS-232 port
Storage	• On-board 4GB USB NAND Flash • AMC.3 SAS • Four SATA and three SAS ports on RTM
Front Panel I/O	• 1x VGA port (DB-15) • 3x USB 2.0 port (Type-A) • 1x RS-232 port (RJ45) • 2x GbE ports (RJ45) • 1x AMC bay (aTCA-6150A only) • LEDs: OOS, Media, User and Hotswap • Recessed reset button
Rear I/O	• PCI-E x4 from Intel 5520 • 1x COM port • 4x USB 2.0 ports • 4x SATA ports from ICH10R • 3x SAS/SATA ports from LSISAS1064E • 2x SerDes ports

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2.3 Software

BIOS	• AMI® BIOS with 8Mbit flash memory
Supported OS	• Microsoft® Windows® Server 2003 • Microsoft® Windows® Server 2008 • Microsoft® Windows® Server 2008 R2 • RedHat Enterprise Linux Release 5.4 • MontaVista Linux Carrier Grade Edition 4.0 • Contact ADLINK for other OS availability

2.4 Mechanical & Environmental

Dimensions	• 322.25mm x 280mm x 30.48mm (H x D x W) - 6HP slot
Operating Temperature	• Standard: 0°C to 50°C • NEBS short-term: 0°C to 55°C
Storage Temperature	• -40°C to 85°C
Humidity	• 5% to 90% non-condensing
Shock	• 15G peak-to-peak, 11ms duration, non-operation
Vibration	• Non-operating: 1.88G rms, 5 to 500 Hz, each axis • Operating: 0.5G rms. 5 to 500Hz, each axis
Compliance	• CE, FCC Class A, CUL, NEBS Level 3 (design)

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2.5 Power Consumption

This section provides information on the power consumption of aTCA-6150.

System Configuration

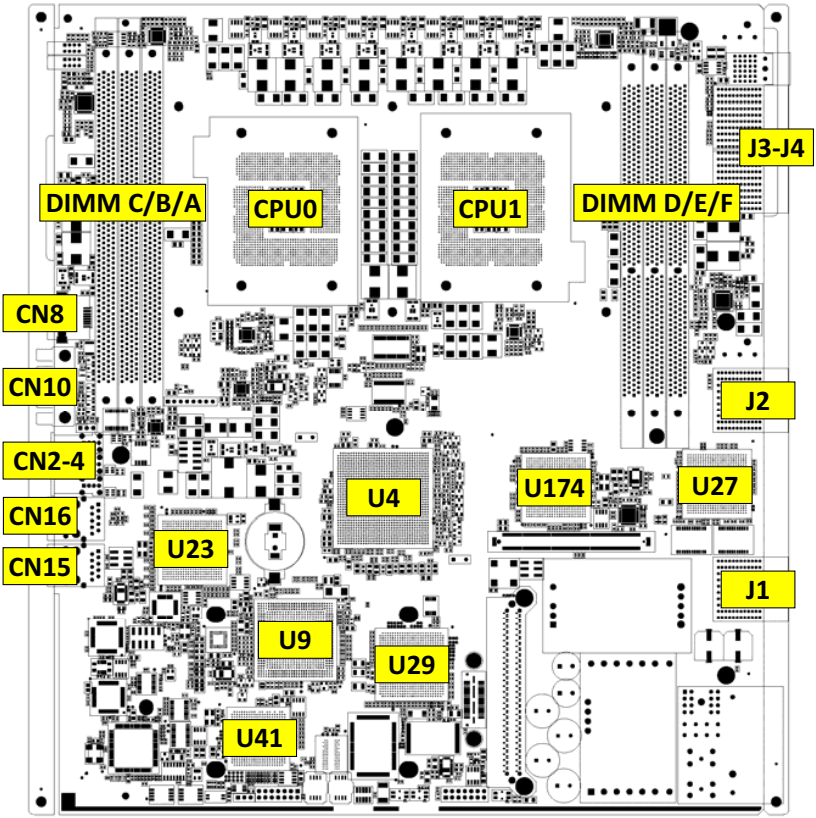
- **Memory:** 2G DDR3-1066 ECC REG x6
- **Graphics:** ATI ES1000
- **Power Supply:** Sunpower SPS-600P-48
- **CPU:**
  - Six-core Intel® Xeon® processor L5638
  - Quad-core Intel® Xeon® processor L5618

The following table describes power consumption of the aTCA-6150 using real applications with a 48V power rail under various operating systems.

OS vs. CPU	L5638 CPU x1	L5638 CPU x2	L5618 CPU x1	L5618 CPU x2
DOS	89.7 W	138.6 W	80.8 W	121.1 W
Linux, Idle	65.9 W	108.1 W	64.3 W	101.7 W
Windows Server 2003, Idle	76.1 W	109.2 W	72. 2 W	104.1 W
Windows Server 2003, CPU 100% Usage	105.6 W	174. 4 W	88.4 W	136.3 W
Windows Server 2008, Idle	53.6 W	106.5 W	55.0 W	99.4 W
Windows Server 2008, CPU 100% Usage	104.2 W	171.2 W	89.6 W	134.4 W

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2.6 aTCA-6150 Board Layout



CPU1, CPU2	CPU1/2 processors	**CN16**	1GbE Ethernet port
DIMM A/B/C	DDR3-1066MHz (CPU0)	**CN15**	1GbE Ethernet port
DIMM D/E/F	DDR3-1066MHz (CPU1)	**U23**	Intel 82576EB
J1	Base Interface	**U4**	Intel 5520
J2	Fabric Interface	**U174**	Intel 82576EB
J3-J4	Zone 3 to RTM	**U27**	Intel 82576EB
CN8	COM port	**U9**	Intel ICH10R
CN10	DB-15 VGA connector	**U29**	LSISAS1064E controller
CN2-4	USB ports	**U41**	ATI ES1000 graphics

Figure 2-1: aTCA-6150 Board Layout

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2.7 aTCA-6150 Front Panel

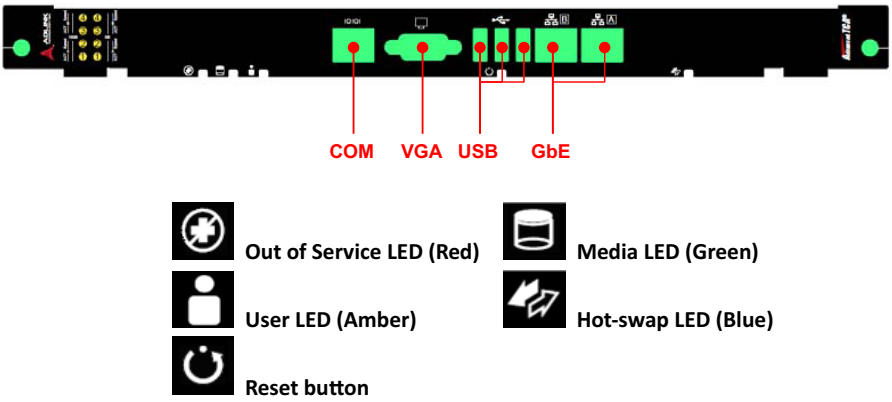


Figure 2-2: aTCA-6150 Front Panel

LED Definitions

The following shows the LED in the front panel which included the Hot-swap LED, User LED, Media LED, and OOS LED.

Hot-swap LED

Hot-swap LED (Blue)	FRU State number	FRU State Name
Off	M0	FRU not installed
On	M1	FRU inactive
Long blink	M2	FRU activation request
Off	M3	FRU activation in process
Off	M4	FRU active
Short blink	M5	FRU deactivation request
Short blink	M6	FRU deactivation in process

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Out of Service LED

OOS LED (Red)	State	Remark
Blink	During BIOS POST	FRU State M4
Off	BIOS POST OK	FRU State M4
On	After OS shutdown	FRU State M1

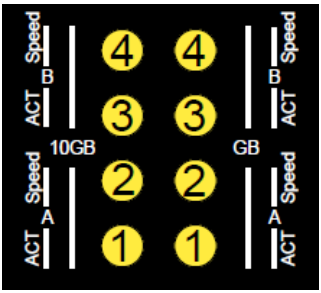
Media LED

Media LED (Green)	State	Remark
Blink	Accessing Disk I/O	
Off	Disk I/O idle	

User LED

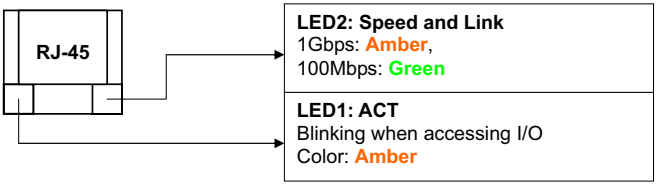
User LED (Amber)	State	Remark
On	Default On	This LED is reserved for customer applications and can be controlled via GPIO.

Base Fabric Channel LED

BASE Channel and Fabric Channel LED		
Fabric 2 Speed/Link 1Gbps – OFF 10Gbps – ON (Amber)		**BCH2 Speed/Link** 100 Mbps: Green 1Gbps: Amber
Fabric 2 ACT (Amber) Blink when accessing Ethernet I/O		**BCH2 ACT** (Amber) Blink when accessing Ethernet I/O
Fabric 1 Speed/Link 1Gbps - OFF 10Gbps – ON (Amber)		**BCH1 Speed/Link** 100 Mbps: Green 1Gbps: Amber
Fabric 1 ACT (Amber) Blink when accessing Ethernet I/O		**BCH1 ACT** (Amber) Blink when accessing Ethernet I/O

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GbE LED



2.8 Compliance

The aTCA-6150 conforms to the following specifications:

- PICMG 3.0 R2.0 ECN0002 AdvancedTCA
- PICMG 3.1 Ethernet over AdvancedTCA option 1 and 9
- AMC.0 Advanced Mezzanine Card R2.0 Midsize
- AMC.1 PCI Express R1.0
- AMC.2 E2 / Type 4
- AMC.3 Storage R1.0

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3 Functional Description

3.1 CPU, Memory and Chipset

Supported Processors

Six-core Intel® Xeon Processor L5638
Quad-core Intel® Xeon Processor L5618

The Intel Xeon® processor 5600 series is the first generation dual-processor server/workstation solution to implement key new technologies:

- Integrated Memory controller
- Point-to-point link interface based on Intel® QuickPath Interconnect (Intel® QPI)

The processor is optimized for performance with the power efficiencies of a low-power micro-architecture to enable smaller, quieter systems.

The Intel® Xeon processors L5638 and L5618 are multi-core processors based on 32 nm process technology. Processor features include two Intel® QPI point-to-point links with 5.86GT/s, 12MB of shared cache, and an integrated memory controller. The processors support all the existing Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3) and Streaming SIMD Extensions 4 (SEE4). Also supported are: Execute Disable Bit, Intel® 64 Technology, Enhanced Intel® SpeedStep Technology, Intel® Virtualization Technology (Intel® VT), and Intel® Hyper-Threading Technology.

The Intel® Xeon® Processor L5638 has a max. TDP of 60 W and the Intel® Xeon® Processor L5618 has a max. TDP of 40 W. Both processors have an elevated case temperature specification. The elevated case temperatures are intended to meet the short-term thermal profile requirements of NEBS Level 3. These 2-socket processors are ideal for thermally constrained form factors in embedded servers, communications and storage markets.

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Supported Processors, Maximum Power Dissipation

The following tables describe the processors supported on the aTCA-6150 and their maximum power dissipation.

	Intel® L5638	Intel® L5618
L2 cache	12 MB	12 MB
Clock	2.00 GHz	1.87 GHz
QPI	5.86 GT/s	5.86 GT/s
Max. Power	60 W	40 W

Memory

The aTCA-6150 supports DDR3-1066 RDIMM in six sockets (3 per processor) up to 48GBytes. The available COTS DDR3-1066 RDIMM densities are 1 GB, 2GB, 4GB and 8GB.



NOTE:

Memory configuration changes can only be performed at the factory. Failure to comply with the above may result in damage to your board or improper operation.

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Chipset

Intel® 5520/ICH10R Chipset Overview

The Intel® 5520 Chipset I/O Hub (IOH) provides a connection point between various I/O components and Intel® QuickPath Interconnect (Intel® QPI) based processors. The Intel® 5520 Chipset is combined with Intel® Xeon® Processor 5500 in their respective two socket platforms. The Intel® Xeon® 5500 Platform consists of the Intel Xeon Processor 5500 Series, the Intel 5520 Chipset I/O Hub (IOH), the I/O Controller Hub (Intel® ICH10), and the I/O subsystem. The processor includes an integrated Memory Controller (IMC) that resides within the processor package. This platform is the first single processing platform that introduces the Intel QuickPath Interconnect. Intel QuickPath Interconnect is Intel's next generation point-to-point system interconnect interface and replaces the Front Side Bus.



The term *IOH* refers to the Intel 5520 Chipset I/O Hub (IOH) and *ICH10R* refers to the Intel® 82801JIR ICH10R I/O Controller Hub 10 components.

The IOH provides the interface between the processor Intel QuickPath Interconnect and industry-standard PCI Express components. The two Intel QuickPath Interconnect interfaces are full-width links (20 lanes in each direction). The two x16 PCI Express Gen2 ports are also configurable as x8 and x4 links compliant to the PCI Express Base Specification, Revision 2.0. The single x4 PCI Express Gen2 port can bifurcate into two independent x2 interfaces.In addition, the legacy IOH supports a x4 ESI link interface for the legacy bridge. The IOH supports the following features and technologies:

- Intel® QuickPath Interconnect profile
- Interface to CPU or other IOH (limited configurations) PCI Express Gen2
- Intel® I/O Accelerated Technology (Intel® I/OAT) and Intel® Quick Data Technology (updated DMA engine with virtualization enhancements)
- Integrated Intel® Management Engine (Intel® ME)

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ATI ES1000 Graphics Controller

The aTCA-6150 provides an analog VGA port on the front panel powered by an AMD ES1000 2D graphics controller with the following features:

- 32-bit PCI bus (Rev 2.2), 3.3 V with bus mastering support
- Support for SPI Serial and Flash Memory video BIOS
- One CRT controller capable of supporting two identical simultaneous display paths
- Dual integrated DACs for CRT display support
- Support for external TMDS transmitter via 24-bit digital output to drive most popular TMDS transmitters up to 165MHz frequency
- Independent DDC lines for both DACs and TMDS connections; also full AppleSense support on DAC connection
- Static and dynamic Power Management support (APM as well as ACPI) with full VESA DPMS and Energy Star compliance
- Comprehensive testability including full internal scan, memory BIST, I/O xor tree and Iddq
- Full ACPI 1.0b, OnNow, and IAPC (Instantly Available PC) power management, including PCI power management registers
- Bi-endian support for compliance on a variety of processor platforms
- Bus mastering of 2D display lists
- Triple 10-bit palette DAC supports pixel rates to 350MHz
- DDC1 and DDC2 for plug and play monitors
- Flexible memory support:
  - DDR1 and DDR2 SDRAM and SGRAM
  - 16-bit interface
  - 8MB to 256MB
- Up to 1GB/s bandwidth.
- Single chip solution in 0.13 micron process, 1.2V CMOS technology in a BGA package

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3.2 Peripherals

The following standard peripherals are available on the aTCA-6150 blade:

Timer

The aTCA-6150 is equipped with the following timers:

- **Real-Time Clock:** The ICH10R contains a real-time clock that performs timekeeping functions and includes 256 bytes of general purpose battery-backed CMOS RAM. Features include an alarm function, programmable periodic interrupt and a 100-year calendar. All battery-backed CMOS RAM data remains stored in an additional EEPROM. This prevents data loss in case the aTCA-6150 is operated without battery.
- **Counter/Timer:** Three 8254-style counter/timers are included on the aTCA-6150 as defined for the PC/AT (System Timer, Refresh Request, Speaker Tone Output).
- **High Precision Event Timers (HPET):** In addition to the three 8254-style counters, the ICH10R includes three High Precision Event Timers (HPET) that may be used by the operating system. They can be used in one-shot and periodic modes to generate an interrupt when the counter reaches a pre-programmed value.

Watchdog Timer

The aTCA-6150 provides a Watchdog Timer that is programmable for a timeout period ranging from 1 to 255 minutes, or 1 to 255 seconds. Please refer to “Watchdog Timer” on page 59 for a detailed programming guide.

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Battery

The aTCA-6150 is equipped with a 3.0 V “coin cell” lithium battery for the RTC. To replace the battery, proceed as follows:

- Turn off power
- Remove the battery
- Place the new battery in the socket

Make sure that you insert the battery with the correct orientation. The positive pole must be on the top

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. A suitable battery is the Panasonic CR2032.



NOTE:

The user must be aware that the battery’s operational temperature range is less than that of the aTCA-6150’s storage temperature range. For exact temperature range information, refer to the battery manufacturer’s specifications.



NOTE:

Care must be taken to ensure that the battery is correctly replaced. The battery should be replaced only with an identical or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer’s instructions. The typical life expectancy of a 225mAh battery is 4-5 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and standby (shutdown) time of the system in which it operates. To ensure that the lifetime of the battery has not been exceeded, it is recommended to change the battery after 3-4 years.

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Reset

The aTCA-6150 is automatically reset by a precision voltage monitoring circuit that detects a drop in voltage below the acceptable operating limit of 4.85V for the 5V line and below 3.2V for the 3.3V line. Other reset sources include the Watchdog Timer, the face plate push-button switch and also the RESET signal from the IPMC. The aTCA-6150 responds to any of these sources by initializing local peripherals.

A reset will be generated by the following conditions:

- Power failure, +5 V supply falls below 4.1 V (typ.) or +3.3 V supply falls below 2.93 V (typ.)
- Pushbutton ´RESET" pressed
- Watchdog time-out
- IPM controller reset

SMBus and I2C Devices

The aTCA-6150 provides a System Management Bus (SMBus) hosted by the ICH10R and an I2C bus hosted by the IPM controller, H8S/2168. The following table describes the function and address of the devices.

SMBus Device	Address (HEX)	I2C Device	Address (HEX)
DIMM A	0xA0	PECI-to-I2C	0x92
DIMM B	0xA4	LM75	0x9E
DIMM C	0xA8	PCA9555PW	0x40
DIMM D	0xA0	Fabric Riser Card	0xAE
DIMM E	0xA4		
DIMM F	0xA8		
Clock Gen	0xD2		
Clock Buffer	0xDC		

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GPIO List

The following table summarizes GPIO usage on ICH10R:

ICH10R	I/O	Signal	Description
GPI[2]	Input	IOH_ERR-L	IOH Error output signals
GPI[8]	Input	QPI_TTL_CATERR-L	CPU Indicates that the system has experienced a catastrophic error and cannot continue to operate
GPI[23]	Output	USR_LED	User defined LED
GPI[27]	Output	QPI_FREQSEL0	QuickPath Interconnect Frequency Strapping Options
GPI[28]	Output	QPI_FREQSEL1	QuickPath Interconnect Frequency Strapping Options
GPI[29]	Output	FM_CPU0_LVDDR3_EN	DDR3L DIMM voltage control (DIMM A/B/C)
GPI[30]	Output	FM_CPU1_LVDDR3_EN	DDR3L DIMM voltage control (DIMM D/E/F)
GPI[32]	Output	POSTOK-L	POST OK to IPMC
GPI[52]	Output	ICH_SMBUS_MUX0	DDR SMBUS Multiplier control
GPI[53]	Output	ICH_SMBUS_MUX1	DDR SMBUS Multiplier control
GPI[56]	Output	QPI_FSEL_PWRGD-L	IOH Hard Reset Triggers a Power-Up Reset control

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3.3 I/O Interfaces

USB

The aTCA-6150 supports eight USB 2.0 ports:

- three Type-A ports on front panel
- four ports routed to RTM
- one channel for 4GB on-board NAND flash

On the USB 2.0 front panel port, a USB cable with up to 5 meters in length can be used.

On the USB 2.0 Rear I/O ports, it is strongly recommended to use a cable below 3 meters in length for USB 2.0 devices.

The USB 2.0 ports are high-speed, full-speed, and low-speed capable. Hi-speed USB 2.0 allows data transfers of up to 480 Mb/s, 40 times faster than a full-speed USB (USB 1.1). One USB peripheral may be connected to each port.

Front Panel USB Connector (CN9-11)

Pin #	Signal Name
1	Vcc
2	Data-
3	Data+
4	GND



Table 3-1: Front Panel USB Connector Pin Definition

NOTE:

The aTCA-6150 host interfaces can be used with maximum 500mA continuous load current as specified in the Universal Serial Bus Specification, Revision 2.0. Short circuit protection is provided. All the signal lines are EMI filtered.

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VGA Analog Interface

The DB-15 female connector CN10 is for analog display output.

DB-15 VGA Connector (CN10)

Signal Name	Pin #	Pin #	Signal Name
Red	1	9	+5 V
Green	2	10	Ground
Blue	3	11	NC
NC	4	12	DDC_DATA
Ground	5	13	HSYNC
Ground	6	14	VSYNC
Ground	7	15	DDC CLK
Ground	8		

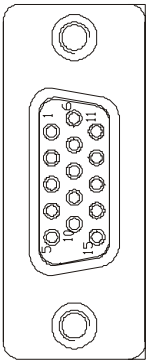


Table 3-2: VGA Connector Pin Definition

Gigabit Ethernet

The aTCA-6150 is equipped with three dual-port Intel® 82571EB Gigabit Ethernet controllers, which provide a total of six GbE ports onboard. In default configuration, two ports are connected to the front panel and two ports are connected to the Base Interface channels. The third controller provides two 1GB Fiber Channels (routed to SERDES links to the RTM if no riser card installed).

The aDB-6150-A Fabric riser card provides the capability to support different configurations for Fabric Channels 1 and 2. An aDB-6150-A will be installed on the aTCA-6150 by default. An Intel 82599EB Ethernet controller on the riser card connects to the IOH via a PCI-E x8 interface and provides 10GbE links to Fabric Channels 1 and 2 (FCH1/FCH2).

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Serial Port

One PC-compatible serial RS-232, RJ45 port is provided on the front panel with DIP switches SWX1 and SWX2 on the board that are used to set the COM port function to *RS-232 mode* or *IPMC debug mode*. A complete set of handshaking and modem control signals are supported, with data transfer rates up to 115.2 kB/sec.

The Front Panel RJ45 COM connector CN8 pin-assignment is listed below.

COM Serial Port Connector (RJ45)

Pin #	Signal	Function
1	DCD#	Data Carrier Detect
2	RTS#	Request to Send
3	DSR#	Data Set Ready
4	TXD	Transmit Data
5	RXD	Receive Data
6	GND	Ground
7	CTS#	Clear to Send
8	DTR#	Data Terminal Ready

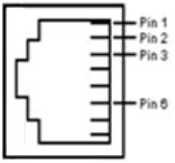


Table 3-3: COM1 Serial Port Connector Pin Definition

When the Front Panel RJ45 COM connector is set to *IPMC debug mode*, the pin assignment of the RJ45 connector is as below.

Pin #	Signal	Function
1	NC	Not connected
2	NC	Not connected
3	NC	Not connected
4	DBG_TX	IPMC Transmit Data
5	DBG_RX	IPMC Receive Data
6	GND	Ground
7	NC	Not connected
8	NC	Not connected

Table 3-4: IPMC Debug Port Connector Pin Definition

See “COM Mode Switch Settings (SWX1 and SWX2)” on page 26 for DIP switch settings.

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3.4 Switches

Switch SW1 is for Blade Operation Mode Control (Pins 1 & 2) and PICMG 3.1 Option Control (Pins 3 & 4). Switch SW2 is for debugging purposes. Switches SWX1 and SWX2 are used to set the COM port function to *RS-232 mode* or *IPMC debug mode*. SW7 is provided to clear CMOS.

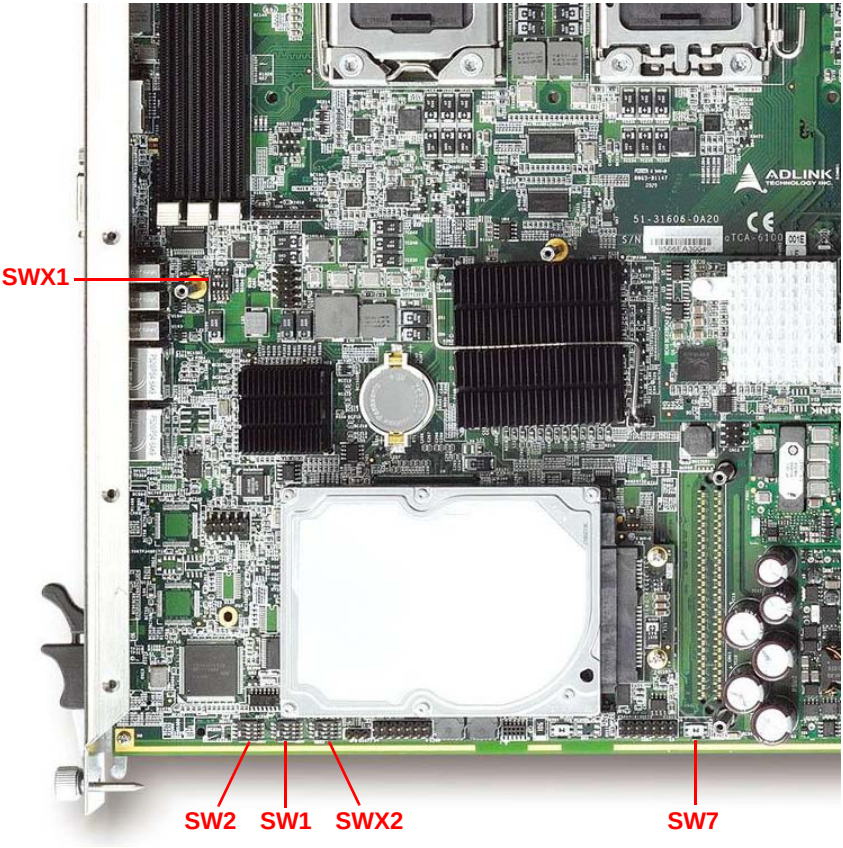


Figure 3-1: aTCA-6150 Switch Locations

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SW1 - Blade Operation Mode Control

Normal operation requires a shelf manager for the blade to boot. Standalone mode allows the blade to boot without a shelf manager. There are different switch settings for PCB Revisions A2 and A3 onwards.

Options	Pin 1	Pin 2
Normal mode*	OFF	OFF
Standalone mode	OFF	ON

Table 3-5: Blade Operation Mode Switch Settings (Rev. A2)

Options	Pin 1	Pin 2
Normal mode*	ON	OFF
Standalone mode	ON	ON

Table 3-6: Blade Operation Mode Switch Settings (Rev. A3 and higher)

* Default



Pin 1 on SW1 is used to identify the PCB version to the IPMC. On PCB Rev. A2, the IPMC can only detect the processor nearest the front panel for temperature and voltage monitoring. From PCB Rev. A3 onwards, the IPMC can detect both processors automatically.

SW1 - PICMG 3.1 Option Control

Options	Pin 3	Pin 4
PICMG 3.1 Opt. 1	OFF	OFF
PICMG 3.1 Opt. 9*	ON	OFF

* Default

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SW2 - Debug use only

Switch SW2 is for debugging purposes. For normal operation, leave the switch in the default settings.

SW2	Pin 1	Pin 2	Pin 3	Pin 4
Default Setting	OFF	OFF	OFF	OFF

- Pin 1: ON for FWE pin protection; OFF for Normal operation
- Pin 2: ON for Slave SPI; OFF for Master SPI

IPMC Mode Select:

  - Pin 3: ON for Program mode; OFF for Normal mode
  - Pin 4: ON for Program mode; OFF for Normal mode

COM Mode Switch Settings (SWX1 and SWX2)

Switches SWX1 and SWX2 are used to set the COM port function to *RS-232 mode* or *IPMC debug mode*. There are different switch settings for PCB Revisions A2 and A3 onwards.

Mode	Switch	Pin 1	Pin 2	Pin 3	Pin 4
RS-232 port (default)	SWX1	ON	ON	OFF	OFF
	SWX2	OFF	ON	N/A	
IPMC debug port	SWX1	OFF	OFF	ON	ON
	SWX2	ON	OFF	N/A	

Table 3-7: COM Mode Switch Settings (Rev. A2)

Mode	Switch	Pin 1	Pin 2	Pin 3	Pin 4
RS-232 port (default)	SWX1	ON	ON	OFF	OFF
	SWX2	ON	OFF	N/A	
IPMC debug port	SWX1	OFF	OFF	ON	ON
	SWX2	OFF	ON	N/A	

Table 3-8: COM Mode Switch Settings (Rev. A3 and higher)

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SW7 - Clear CMOS

SW7 is provided to clear CMOS. Press the switch to clear the CMOS and reset the BIOS values to default.



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4 Hardware Platform Management

4.1 Platform Management Overview

The purpose of the hardware platform management system is to monitor, control, and assure proper operation of AdvancedTCA® Boards and other Shelf components. The hardware platform management system watches over the basic health of the system, reports anomalies, and takes corrective action when needed. The hardware platform management system can retrieve inventory information and sensor readings as well as receive event reports and failure notifications from Boards and other Intelligent FRUs. The hardware platform management system can also perform basic recovery operations such as power cycle or reset of managed entities.

The IPMC controller on the aTCA-6150 supports an “intelligent” hardware management system, based on the Intelligent Platform Management Interface Specification. The hardware management system provides the ability to manage the power, cooling, and interconnect needs of intelligent devices; to monitor events; and to log events to a central repository.

4.2 IPMI Sensors

Following table lists all the sensors supported by the aTCA-6150.

Item	Sensor Name	Sensor Address	Description
(1)	Hotswap	(0x0)	FRU Hotswap Sensor. Please refer to section 4.2.1
(2)	Shelf FRU Hotswap	(0x1)	FRU Hotswap Sensor. Please refer to section 4.2.1
(3)	Hotswap AMC 1	(0x2)	AMC#1 Hotswap Sensor. Please refer to section 4.2.1
(4)	RTM Hotswap	(0x3)	RTM Hotswap Sensor. Please refer to section 4.2.1
(5)	IPMB Physical	(0x5)	Physical IPMB Sensor. Please refer to section 4.2.2
(6)	BMC Watchdog	(0x6)	Watchdog Timer Sensor. Please refer to section 4.2.3

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Item	Sensor Name	Sensor Address	Description
(7)	Version change	(0x4)	Version Change Sensor. Please refer to section 4.2.4
(8)	+1..5V DDR-CPU	(0x7)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 1.65 Volts Upper Critical Threshold = 1.62 Volts Upper Non-Critical Threshold = 1.59 Volts Lower Non-Critical Threshold = 1.41 Volts Lower Critical Threshold = 1.38 Volts Lower Non-Recoverable Threshold = 1.35 Volts
(9)	+1.8V CPU	(0x8)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 1.98 Volts Upper Critical Threshold = 1.944 Volts Upper Non-Critical Threshold = 1.908 Volts Lower Non-Critical Threshold = 1.692 Volts Lower Critical Threshold = 1.656 Volts Lower Non-Recoverable Threshold = 1.62 Volts
(10)	+5.0V	(0x9)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 5.5 Volts Upper Critical Threshold = 5.4 Volts Upper Non-Critical Threshold = 5.3 Volts Lower Non-Critical Threshold = 4.7 Volts Lower Critical Threshold = 4.6 Volts Lower Non-Recoverable Threshold = 4.5 Volts
(11)	+3.3V	(0xA)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 3.63 Volts Upper Critical Threshold = 3.564 Volts Upper Non-Critical Threshold = 3.498 Volts Lower Non-Critical Threshold = 3.102 Volts Lower Critical Threshold = 3.036 Volts Lower Non-Recoverable Threshold = 2.97 Volts
(12)	+12V	(0xB)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 13.2 Volts Upper Critical Threshold = 12.96 Volts Upper Non-Critical Threshold = 12.72 Volts Lower Non-Critical Threshold = 11.28 Volts Lower Critical Threshold = 11.04 Volts Lower Non-Recoverable Threshold = 10.8 Volts

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Item	Sensor Name	Sensor Address	Description
(13)	LM75 SYS Temp	(0x13)	System Temperature. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 95 °C Upper Critical Threshold = 75 °C Upper Non-Critical Threshold = 60 °C
(14)	CPU0 Temp	(0x11)	CPU Temperature. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 100 °C Upper Critical Threshold = 80 °C Upper Non-Critical Threshold = 65 °C
(15)	CPU1 Temp	(0x12)	CPU Temperature. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 100 °C Upper Critical Threshold = 80 °C Upper Non-Critical Threshold = 65 °C
(16)	W83627_OVT	(0xC)	Discrete Sensor(Normal:0x0001, Abnormal:0x0002) OVT#/SMI#: Can create interrupts that depend on the temperatures measured by SYSTIN and CPUTIN. This mode is enabled by setting THYST (Temperature Hysteresis) to 127 °C.
(17)	SIO_THERM	(0xD)	Discrete Sensor(Normal:0x0001, Abnormal:0x0002) Same as W83627 OVT.
(18)	SIO_WDT	(0xE)	Discrete Sensor(Normal:0x0001, Abnormal:0x0002) Watchdog timer output signal. The time-out counter ranges from 1 to 255 minutes in the minute mode, or 1 to 255 seconds in the second mode.
(19)	ICH_THEM	(0xF)	Discrete Sensor(Normal:0x0001, Abnormal:0x0002) Thermal Alarm: Active low signal generated by external hardware to generate an SMI# or SCI.
(20)	FSB_GPIO_FERR	(0x10)	Discrete Sensor(Normal:0x0001, Abnormal:0x0002) FERR# (floating-point error) is qualified by STPCLK#. When STPCLK# is not asserted, FERR# indicates a floating-point error and will be asserted when the processor detects an unmasked floating-point error. When STPCLK# is not asserted, FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR# indicates that the processor has a pending break event waiting for service. The assertion of FERR# indicates that the processor should be returned to the Normal state.

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Item	Sensor Name	Sensor Address	Description
(21)	BIOS CHANGE	(0x15)	Discrete Sensor Dual Bios function.
(22)	BIOS POST ERROR	(0x16)	Discrete Sensor Dual Bios function.

Table 4-1: aTCA-6150 IPMI Sensors

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4.2.1 Get Sensor Reading (FRU Hotswap Sensor)

	Byte	Data field
Request data	1	Sensor Number (FFh = reserved)
Response data	1	Completion Code
	2	Sensor Reading. [7:0] - Not used. Write as 00h.
	3	Standard IPMI byte (See “Get Sensor Reading” in IPMI specification): [7] - 0b = All Event Messages disabled from this sensor [6] - 0b = sensor scanning disabled [5] - 1b = initial update in progress. This bit is set to indicate that a “Re-arm Sensor Events” or “Set Event Receiver” command has been used to request an update of the sensor status, and that update has not occurred yet. Software should use this bit to avoid getting an incorrect status while the first sensor update is in progress. This bit is only required if it is possible for the IPM Controller to receive and process a “Get Sensor Reading or Get Sensor Event Status” command for the sensor before the update has completed. This is most likely to be the case for sensors, such as fan RPM sensors, that may require seconds to accumulate the first reading after a re-arm. [4:0] – reserved. Ignore on read.
	4	Current State Mask [7] – 1b = FRU Operational State M7 - Communication Lost [6] – 1b = FRU Operational State M6 - FRU Deactivation In Progress [5] – 1b = FRU Operational State M5 - FRU Deactivation Request [4] – 1b = FRU Operational State M4 - FRU Active [3] – 1b = FRU Operational State M3 - FRU Activation in Progress [2] – 1b = FRU Operational State M2 - FRU Activation Request [1] – 1b = FRU Operational State M1 - FRU Inactive [0] – 1b = FRU Operational State M0 - FRU Not Installed
	5	[7:0] – Optional/Reserved. If provided, write as 80h (IPMI restriction). Ignore on read.

Table 4-2: Get Sensor Reading (FRU Hotswap Sensor)

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4.2.2 Get Sensor Reading (Physical IPMB-0 Sensor)

	Byte	Data field
Request data	1	Sensor Number (FFh = reserved)
Response data	1	Completion Code
	2	Sensor Reading. [7:0] - Not used. Write as 00h.
	3	Standard IPMI byte (See “Get Sensor Reading” in IPMI specification): [7] - 0b = All Event Messages disabled from this sensor [6] - 0b = sensor scanning disabled [5] - 1b = initial update in progress. This bit is set to indicate that a “Re-arm Sensor Events” or “Set Event Receiver” command has been used to request an update of the sensor status, and that update has not occurred yet. Software should use this bit to avoid getting an incorrect status while the first sensor update is in progress. This bit is only required if it is possible for the IPM Controller to receive and process a “Get Sensor Reading or Get Sensor Event Status” command for the sensor before the update has completed. This is most likely to be the case for sensors, such as fan RPM sensors, that may require seconds to accumulate the first reading after a re-arm. [4:0] – reserved. Ignore on read.
	4	Current State Mask [7] – 1b = FRU Operational State M7 - Communication Lost [6] – 1b = FRU Operational State M6 - FRU Deactivation In Progress [5] – 1b = FRU Operational State M5 - FRU Deactivation Request [4] – 1b = FRU Operational State M4 - FRU Active [3] – 1b = FRU Operational State M3 - FRU Activation in Progress [2] – 1b = FRU Operational State M2 - FRU Activation Request [1] – 1b = FRU Operational State M1 - FRU Inactive [0] – 1b = FRU Operational State M0 - FRU Not Installed
	5	[7:0] – Optional/Reserved. If provided, write as 80h (IPMI restriction). Ignore on read.

Table 4-3: Get Sensor Reading (Physical IPMB-0 Sensor)

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4.2.3 Watchdog Timer Sensor

Sensor Type	Sensor Type Code	Sensor Specific Offset	Event
Watchdog 2	23h		This sensor is recommended for new IPMI v1.0 and later implementations.
		00h	Timer expired, status only (no action, no interrupt)
		01h	Hard Reset
		02h	Power Down
		03h	Power Cycle
		04h-07h	reserved
		08h	Timer interrupt
			The Event Data 2 field for this command can be used to provide an event extension code, with the following definition: 7:4 interrupt type 0h = none 1h = SMI 2h = NMI 3h = Messaging Interrupt Fh = unspecified all other = reserved 3:0 timer use at expiration: 0h = reserved 1h = BIOS FRB2 2h = BIOS/POST 3h = OS Load 4h = SMS/OS 5h = OEM Fh = unspecified all other = reserved

Table 4-4: Watchdog Timer Sensor

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4.2.4 Version Change Sensor

Sensor Type	Sensor Type Code	Sensor Specific Offset	Event
Version Change	2Bh	00h	00h Hardware change detected with associated Entity. Informational. This offset does not imply whether the hardware change was successful or not. Only that a change occurred.
		01h	01h Firmware or software change detected with associated Entity.Informational. Success or failure not implied.
		02h	02h Hardware incompatibility detected with associated Entity.
		03h	03h Firmware or software incompatibility detected with associated Entity.
		04h	04h Entity is of an invalid or unsupported hardware version.
		05h	05h Entity contains an invalid or unsupported firmware or software version.
		06h	06h Hardware Change detected with associated Entity was successful. (deassertion event means unsuccessful').
		07h	07h Software or F/W Change detected with associated Entity was successful. (deassertion event means 'unsuccessful')
			Event data 2 can be used for additional event information on the type of version change - see definition below

Table 4-5: Version Change Sensor

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Event Data 2

7:0 Version change type

- 00h unspecified
- 01h management controller device ID (change in one or more fields from ‘Get Device ID’)
- 02h management controller firmware revision
- 03h management controller device revision
- 04h management controller manufacturer ID
- 05h management controller IPMI version
- 06h management controller auxiliary firmware ID
- 07h management controller firmware boot block
- 08h other management controller firmware
- 09h system firmware (EFI / BIOS) change
- 0Ah SMBIOS change
- 0Bh operating system change
- 0Ch operating system loader change
- 0Dh service or diagnostic partition change
- 0Eh management software agent change
- 0Fh management software application change
- 10h management software middleware change
- 11h programmable hardware change (e.g. FPGA)
- 12h board/FRU module change (change of a module plugged into associated entity)
- 13h board/FRU component change (addition or removal of a replaceable component on the board/FRU that is not tracked as a FRU)
- 14h board/FRU replaced with equivalent version
- 15h board/FRU replaced with newer version
- 16h board/FRU replaced with older version
- 17h board/FRU hardware configuration change (e.g. strap, jumper, cable change, etc.)

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4.2.5 Get Sensor Reading Command

	Byte	Data field
Request data	1	Sensor Number (FFh = reserved)
Response data	1	Completion Code
	2	Sensor reading Byte 1: byte of reading. Ignore on read if sensor does not return an numeric (analog) reading.
	3	[7] - 0b = All Event Messages disabled from this sensor [6] - 0b = sensor scanning disabled [5] - 1b = reading/state unavailable (formerly “initial update in progress”). This bit is set to indicate that a ‘re-arm’ or ‘Set Event Receiver’ command has been used to request an update of the sensor status, and that update has not occurred yet. Software should use this bit to avoid getting an incorrect status while the first sensor update is in progress. This bit is only required if it is possible for the controller to receive and process a ‘Get Sensor Reading’ or ‘Get Sensor Event Status’ command for the sensor before the update has completed. This is most likely to be the case for sensors, such as fan RPM sensors, that may require seconds to accumulate the first reading after a re-arm. The bit is also used to indicate when a reading/state is unavailable because the management controller cannot obtain a valid reading or state for the monitored entity, typically because the entity is not present. See *PICMG Specification 3.0, Section 16.4, Event Status, Event Conditions, and Present State* and *Section 16.6, Re-arming* for more information. [4:0] - reserved. Ignore on read.

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	Byte	Data field
Response data (cont'd)	4	For threshold-based sensors Present threshold comparison status [7:6] - reserved. Returned as 1b. Ignore on read. [5] - 1b = at or above () upper non-recoverable threshold [4] - 1b = at or above () upper critical threshold [3] - 1b = at or above () upper non-critical threshold [2] - 1b = at or below () lower non-recoverable threshold [1] - 1b = at or below () lower critical threshold [0] - 1b = at or below () lower non-critical threshold For discrete reading sensors [7] - 1b = state 7 asserted [6] - 1b = state 6 asserted [5] - 1b = state 5 asserted [4] - 1b = state 4 asserted [3] - 1b = state 3 asserted [2] - 1b = state 2 asserted [1] - 1b = state 1 asserted [0] - 1b = state 0 asserted
	(5)	For discrete reading sensors only. (Optional) (00h Otherwise) [7] - reserved. Returned as 1b. Ignore on read. [6] - 1b = state 14 asserted [5] - 1b = state 13 asserted [4] - 1b = state 12 asserted [3] - 1b = state 11 asserted [2] - 1b = state 10 asserted [1] - 1b = state 9 asserted [0] - 1b = state 8 asserted

Table 4-6: Get Sensor Reading Command

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4.3 IPMI Commands

Following table presents all the commands which are supported by the aTCA-6150 in different interfaces and compatible with IPMI v1.5 and PICMG 3.0 R2.0 ECN001. There are two interfaces implemented with IPMI command support.

(1) KCS: OpenIPMI
(2) IPMB0: IPMBa & IPMBb

	KCS	IPMB0
IPMI Commands		
IPM Device "Global" Commands		
Get Device ID	x	x
Cold Reset	x	x
Warm Reset	x	x
Get Self Test Results	x	x
Get Device GUID	x	x
IPMI Messaging Support Commands		
Set BMC Global Enables	x	x
Get BMC Global Enables	x	x
Clear Message Flags	x	x
Get Message Flags	x	x
Get Message	x	x
Send Message	x	x
Master Write-Read	x	x
BMC Watchdog Timer		
Reset Watchdog Timer	x	x
Set Watchdog Timer	x	x
Get Watchdog Timer	x	x
Event Commands		
Set Event Receiver	x	x
Get Event Receiver	x	x
Platform Event	x	x

Table 4-7: Supported IPMI Commands

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	KCS	IPMB0
Sensor Device Commands		
Get Device SDR Info	x	x
Get Device SDR	x	x
Reserve Device SDR Repository	x	x
Get Sensor Reading Factors	x	x
Set Sensor Hysteresis	x	x
Get Sensor Hysteresis	x	x
Set Sensor Threshold	x	x
Get Sensor Threshold	x	x
Set Sensor Event Enable	x	x
Get Sensor Event Enable	x	x
Rearm Sensor Events	x	x
Get Sensor Event Status	x	x
Get Sensor Reading	x	x
FRU Device Commands		
Get FRU Inventory Area Info	x	x
Read FRU Data	x	x
Write FRU Data	x	x
PICMG Commands		
HPM.1 Upgrade Commands (HPM.1)		
Get target upgrade capabilities	x	x
Get component properties	x	x
Abort Firmware Upgrade	x	x
Initiate upgrade action	x	x
Upload firmware block	x	x
Finish firmware upload	x	x
Get upgrade status	x	x
Activate firmware	x	x
Query Self-test Results	x	x
Query Rollback status	x	x
Initiate Manual Rollback	x	x

Table 4-7 (cont'd): Supported IPMI Commands

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	KCS	IPMB0
AdvancedTCA		
Get PICMG Properties	x	x
Get Address Info	x	x
FRU Control	x	x
FRU Control Capabilities	x	x
Get FRU LED Properties	x	x
Get LED Color Capabilities	x	x
Set FRU LED State	x	x
Get FRU LED State	x	x
Set IPMB State		x
Set FRU Activation Policy	x	x
Get FRU Activation Policy	x	x
Set FRU Activation	x	x
Get Device Locator Record ID	x	x
Get Port State	x	x
Set Port State		x
Compute Power Properties		x
Set Power Level		x
Get Power Level	x	x
Bused Resource Control		x
Get IPMB Link Info	x	x
SET_CLOCK_STATE	x	x
GET_CLOCK_STATE	x	x
Get AMC-Port State		x
Set AMC-Port State		x

Table 4-7 (cont'd): Supported IPMI Commands

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4.4 IPMI Firmware Upgrade Procedure

The processor can communicate with the IPMC by Keyboard Controller Style (KCS), and an upgrade tool for DOS environment to upgrade the IPMC firmware is provided on the ADLINK All-in-One CD or can be downloaded from the ADLINK website. Please follow the procedures below to upgrade the IPMC firmware.

1. Copy the upgrade tool for DOS onto a bootable USB flash drive, and change the boot order setting in BIOS so that the USB flash drive is the first boot device.

```
C:\IPMC\AT6150>dir/w

 Volume in drive C has no label
 Volume Serial Number is 0065-1CB9
 Directory of C:\IPMC\AT6150

[.]      [..]        README.DOC    [TESTTOOL]    [UPGRADE]
         1 file(s)      2,185,216 bytes
         4 dir(s)     863,748,096 bytes free

C:\IPMC\AT6150>cd upgrade

C:\IPMC\AT6150\UPGRADE>dir/w

 Volume in drive C has no label
 Volume Serial Number is 0065-1CB9
 Directory of C:\IPMC\AT6150\UPGRADE

[.]      [..]     A203.IMG     CWSDPMI.EXE    CWSDPR0.EXE
CWSPARAM.EXE    HPMDOS.EXE      UPGRADE.BAT
         7 file(s)        884,350 bytes
         2 dir(s)     863,748,096 bytes free

C:\IPMC\AT6150\UPGRADE>
```

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2. Execute **upgrade.bat**. This tool will upgrade the IPMC firmware automatically. After the firmware has been upgraded successfully, please do a power cycle or remove the blade from the chassis and reinsert.

```
C:\IPMC\AT6150\UPGRADE>upgrade.bat

C:\IPMC\AT6150\UPGRADE>CWSDPMI.EXE -s-
CWSDPMI V0.90+ (r4) Copyright (C) 1997 CW Sandmann
     ABSOLUTELY NO WARRANTY

C:\IPMC\AT6150\UPGRADE>hpmdos.exe -I KCS -F A203.img
     upgrade
Adlink HPH.1 DOS Upgrade Agent
Update HPM.1 components using PICMG HPM.1 file
Validating firmware image integrity...OK
Performing preparation stage...OK
    Services may be affected during upgrade. Do you wish
     to continue? y/n
    Target Product ID     : 6150
    Target Manufacturer ID: 005f13
Performing upgrade stage:    Upgrading H8S-AMCc F/W
    with Version: Major: 1
                  Minor: 51
                  Aux  : a2 00 00 03
    Writing firmware: 100 % completed

Firmware upgrade procedure successful
Upgrade successful, please shutdown and boot system
HPM.1 upgrade succeed!!
```

3. Go to the \TESTTOOL directory and execute TEST.BAT. This tool will list all the sensors on the aTCA-6150, and “Auxiliary Firmware Revision Information: a2000003” indicates the firmware version is a2000003.

```
C:\IPMC\AT6150\TESTTOOL>dir/w

 Volume in drive C has no label
 Volume Serial Number is 0065-1CB9
 Directory of C:\IPMC\AT6150\TESTTOOL

[.]      [..]       INFO.INI      IPMITEST.EXE   TEST.BAT
```

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```
IPMITOOL v 2.0.1 03/17/2008 - IPMI toolkit for Terminal
     mode.
Copyright(c) 2006. All Rights Reserved
FOR PRODUCTS WITH PICMG 2.9(CPCI) CAPABILITY ONLY.
DO NOT RUN THIS PROGRAM UNDER WINDOWS NT, 2000, OR XP.
Please Press any key to continue.
############################################################

[#]Check IPMC status .....[OK]
        Product Name: aTCA-6150
        Firmware Version: V1.51
[#]Check Development status .....OK
       Auxiliary Firmware Revision Information : a2000003
[#]Check KCS status .....OK
[#] Check IPMB addr .....        (IPMB addr: 0x80)
[#] FRU Information .....
        Board product Name: aTCA6150
        Board FRU ID: FRU-OP1 V1.1
###### Press any key to continue ######
01.Hot Swap [00] .....Status OK
02.ShelfFRU HotSwap [01] .....Status OK
03.Hot Swap AMC 1 [02] .....Status OK
04.IPMB Physical [0A] .....Status OK
05.BMC Watchdog [14] .....Status OK
06.Version change [15] .....Status OK
07.+5.0V [05] .....RAW Data(D1) 5.104 V ....Status OK
08.+3.3V [06] .....RAW Data(D1) 3.367 V ....Status OK
09.+1.8V [07] .....RAW Data(B7) 1.789 V ....Status OK
10.+1.5V [08] .....RAW Data(98) 1.485 V ....Status OK
10.+1.5V [08] .....RAW Data(98) 1.485 V ....Status OK
12.LM75 SYS Temp [16] .....RAW Data(A0) 32.000 C
     ....Status OK
13.W83627 OVT [0B] .....Status OK
14.SIO THERM [0C] .....Status OK
15.SIO WDT [0D] .....Status OK
16.ICH THRM [0E] .....Status OK
17.CPU THERMTRIP [0F] .....Status OK
18.FSB FERR [10] .....Status OK
19.FSB IERR [11] .....Status OK
20.SYS PWROK [12] .....Status OK
21.CPU0 Temp [17] .....RAW Data(21) 33.000 C ...Status OK
22.CPU1 Temp [18] .....RAW Data(1C) 28.000 C ...Status OK
23.Hot Swap [00] .....Status OK
```

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5 Getting Started

The aTCA-6150 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

5.1 Safety Requirements

The following safety precautions must be observed when installing or operating the aTCA-6150. ADLINK assumes no responsibility for any damage resulting from failure to comply with these requirements.

Exercised due care when handling the board as the heat sink can get very hot. Do not touch the heat sink when installing or removing the board. The board should not be placed on any surface or in any form of storage container until the board and heat sink have cooled down to room temperature.

If your board type is not specifically qualified as being hot swap capable, switch off the system power before installing the board in a free slot. Failure to do so could endanger your life or health and may damage your board or system.

Certain blades require bus master and/or Rear I/O capability. If you are in doubt whether such features are required for the board you intend to install, please check your specific board and/or system documentation to make sure that your system is provided with an appropriate free slot in which to insert the board.

This ATCA blade contains electrostatic sensitive devices. Please observe the necessary precautions to avoid damage to your board:

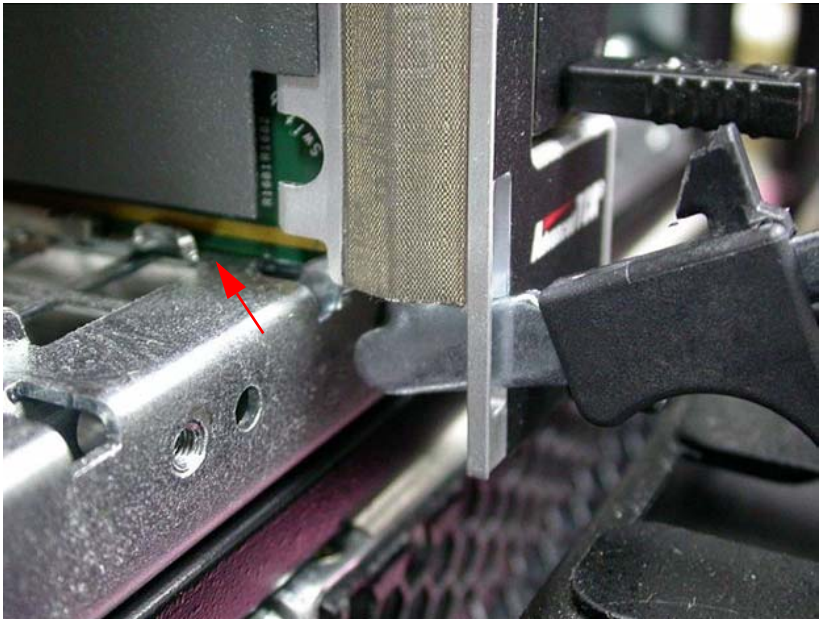
- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

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5.2 Installing the aTCA-6150

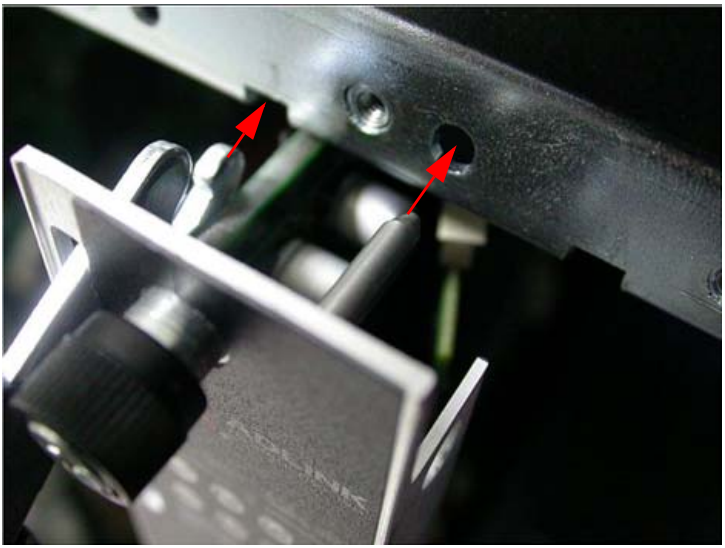
Follow these steps to install the aTCA-6150 to the chassis.

1. Carefully align the board edges with the chassis guide rails and insert the blade into the chassis guide rail.



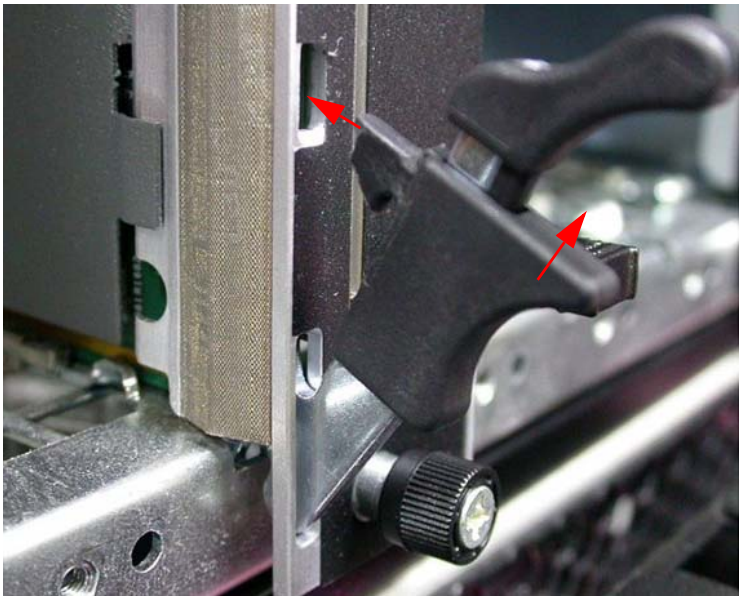
2. Check that the catch hooks and alignment pins at either end of the blade are correctly inserted into the proper openings. Push inwards on the handles until the blade is firmly seated in the chassis. (Do not force the handles if there is resistance as this may damage the connectors and/or backplane.)

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3. Pinch the ejector to unlock the handle and insert the catch into the faceplate.





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4. Secure the blade by tightening the captive screws.



5.3 Removing the aTCA-6150

To remove the aTCA-6150 blade, undo the captive screws, pinch the ejector handle release mechanisms and pull outwards on the ejector handles to eject the blade from the backplane. Pull the blade towards you until it is free of the chassis.

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6 Driver Installation

The drivers for the aTCA-6150 are available on the ADLINK website. Please visit the product website for details: http://www.adlinktech.com.

The following describes the driver installation procedures for Windows® Server 2003

1. Install the Windows operating system before installing any driver. Most standard I/O device drivers are installed during Windows installation.
2. Download the drivers from the website:
   - ▷ Chipset - Intel® Chipset Installation Utility Version
   - ▷ LAN Controller - Intel® PRO/1000 PT Dual Port Server Adapter
   - ▷ SAS Controller - LSI Adapter, SAS 3000 series, 4-port with 1064E
   - ▷ VGA Controller - ATI ES1000, 6.14.10.6553

We recommend using all the drivers provided on the ADLINK All-in-One CD or downloaded from the ADLINK website to ensure driver compatibility. Contact ADLINK to get support for other operating systems.

6.1 Chipset Driver Installation

To install the chipset driver for Windows® Server 2003:

1. Run the InstallShield installation program:
   - ▷ Self-extracting .EXE distribution: INFINST_AUTOL.EXE
   - ▷ Compressed .ZIP distribution: SETUP.EXE
2. You will be prompted to agree to the license agreement. If you do not agree, the installation program will exit before extracting any files.
3. Once the operating system reboots, follow the on-screen instructions and accept default settings to complete the setup.

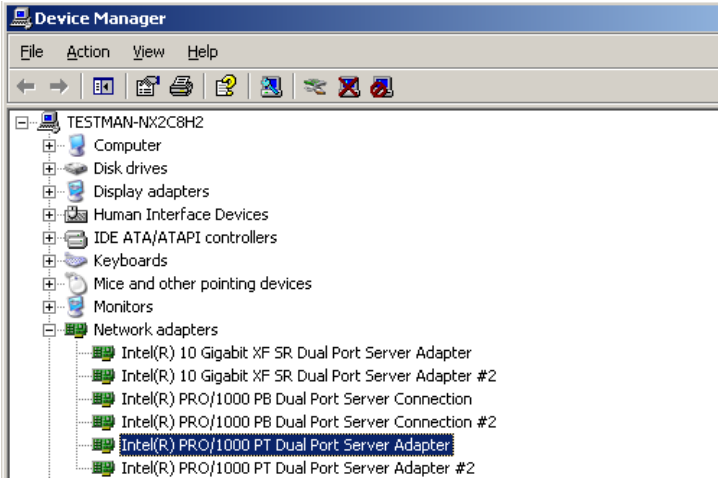
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6.2 LAN Driver Installation

Download the archive Intel_Network_Adapter_Win2003_v14.3.zip, then extract and run the installation wizard. All language files are embedded in this archive. You do not need to download an extra language pack.

After installing the Intel LAN driver, you will see the following Network Adapters in the Device Manager:

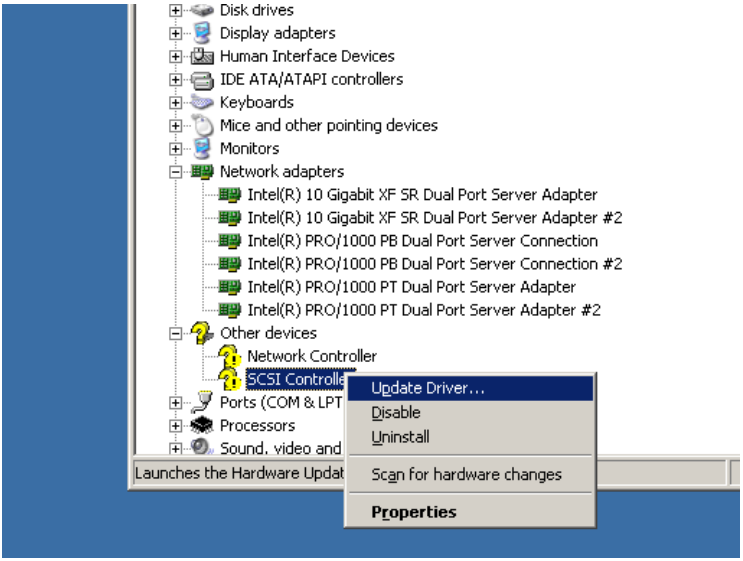
- Intel 10 Gigabit KX4 Dual Port Server Adapter x2
- 82576EB Intel PRO/1000 PB Dual Port Server Connection x6.



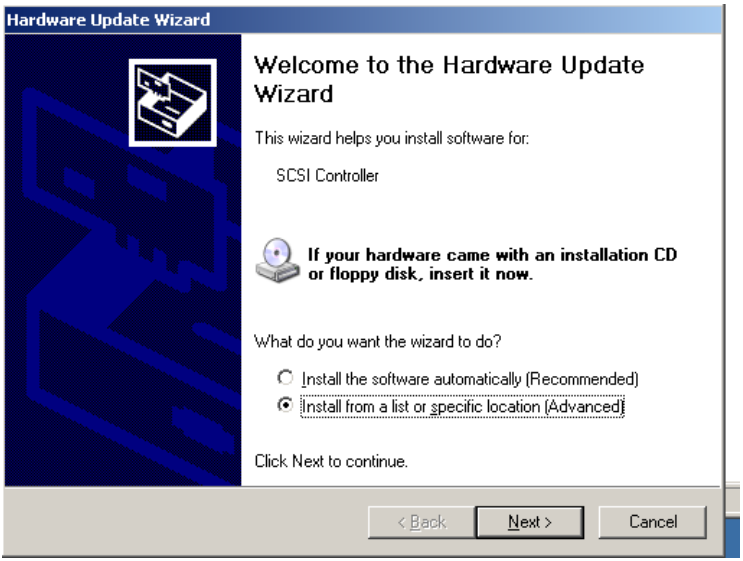
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6.3 LAN Driver Installation

Right-click the mouse on the SCSI Controller in the Device Manager and select *Update Driver*.

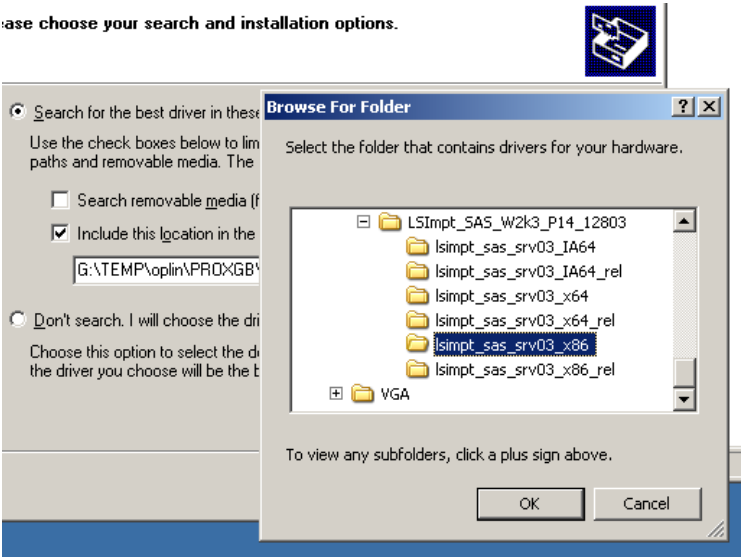


Select *Install from a list or specific location (Advanced)*.

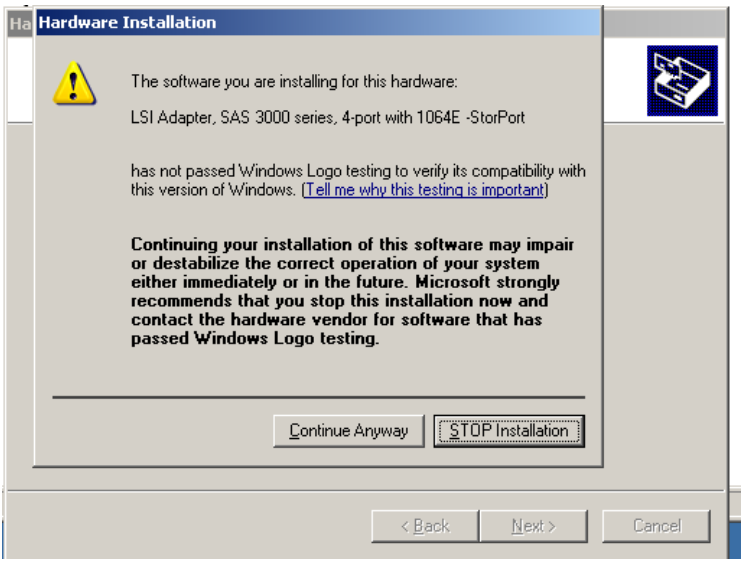


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Navigate to the location *lsimpt_sas_srv03_x86*.

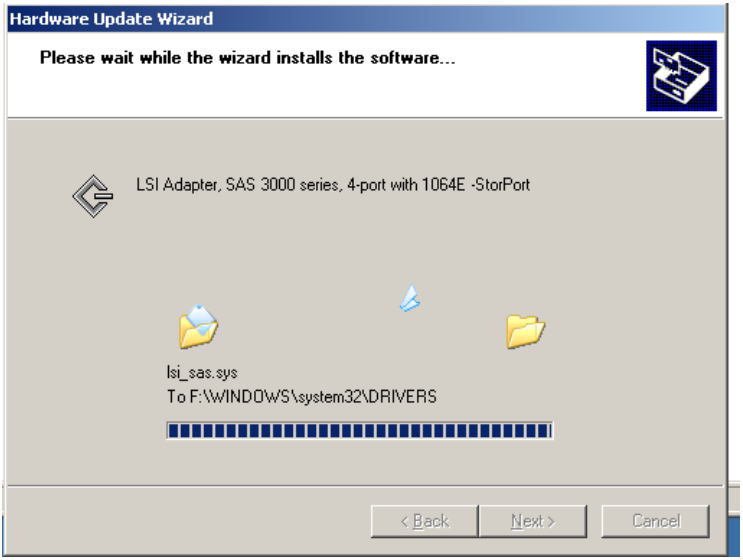


Select *Continue Anyway* when this message pops up.

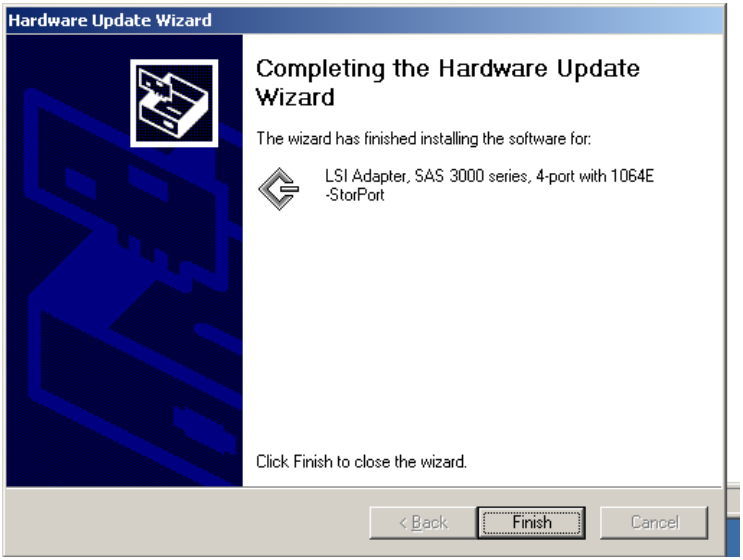


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The *LSI adapter, SAS 3000 series, 4-port with 1064E–StorPort* driver will be installed.



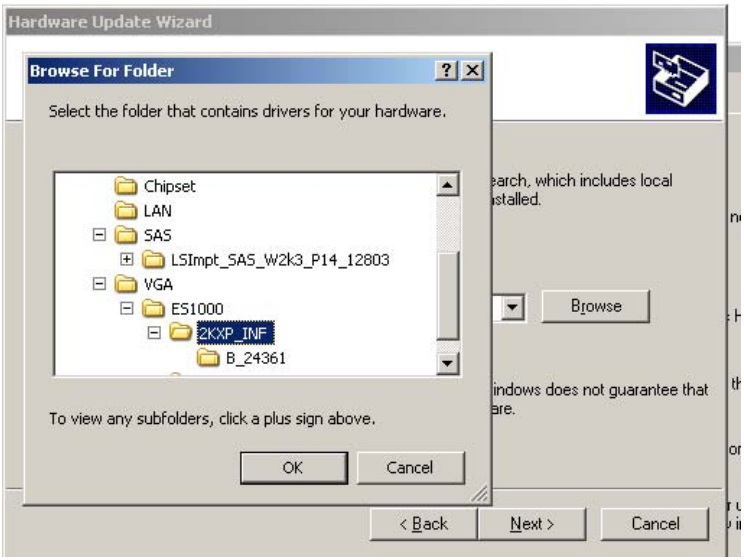
Click *Finish* to complete the installation.



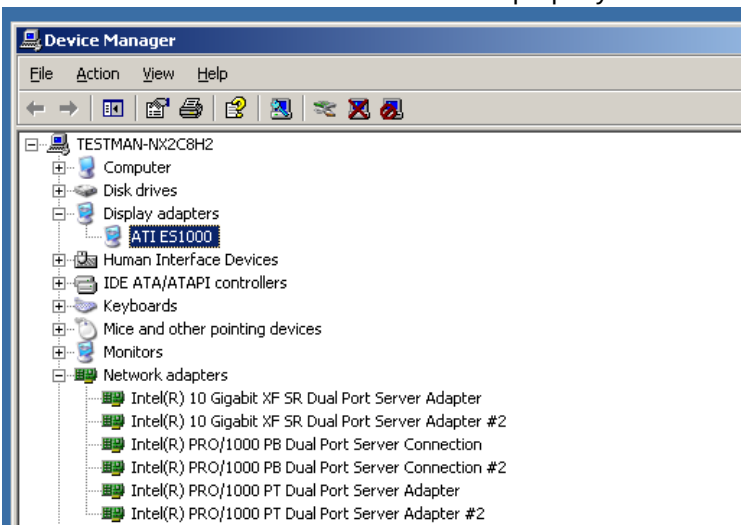
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6.4 VGA Driver Installation

Right-click the mouse on the VGA Controller in the Device Manager and select Update Driver. Navigate to the directory *2KXP_INF* for the VGA driver.



Check if the ATI ES1000 driver was installed properly.



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7 Watchdog Timer

7.1 Overview

The aTCA-6150 supports a Watchdog Timer function which is built into the Winbond W83627UHG to protect the system from specific software or hardware failures that may cause the system stop responding. The application is first registered with the watchdog device. Once the watchdog device is enabled, the application must periodically send a signal to the watchdog device. If the watchdog device doesn't receive this signal within the set period of time, it will reboot the system or restart the application.

The Watchdog Timer of the W83627UHG consists of an 8-bit programmable time-out counter and a control and status register. The time-out counter ranges from 1 to 255 minutes in the minutes mode, or 1 to 255 seconds in the seconds mode. The mode of the Watchdog Timer counter are selected at Logical Device 8, CR[F5h], bit[3]. The time-out value is set at Logical Device 8, CR[F6]. Writing zero disables the Watchdog Timer function. Writing any non-zero value to this register causes the counter to load this value into the Watchdog Timer counter and start counting down.

The W83627UHG outputs a low signal to the WDTO# (pin 77) when a time-out event occurs. In other words, when the value is counted down to zero, the timer stops, and the W83627UHG sets the WDTO# status bit in Logic Device 8, CR[F7h], bit[4], outputting a low signal to the WDTO# pin (pin 77). Writing a zero will clear the status bit and the WDTO# pin returns to high. This bit will also be cleared if LRESET# or PWROK# signal is asserted.

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7.2 Sample Code

This sample code is provided for testing the Watchdog Timer function of the W83627UHG on the aTCA-6150.

```
#include<stdlib.h>
#include<stdio.h>
#include<string.h>
#include<dos.h>

void WDTRUN(int config_port,int count_value);
void Enter_W627UHG_Config(int config_port);
void Exit_W627UHG_Config(int config_port);

void main(int argc,char *argv[])
{
   int number,DevID1,DevID2,chipflag=0;
   int ioport = 0x4E;//Default config_port = 0x4E

      if((argc==1) || ((argc == 3)&& (*argv[2] != 'i')) ||
      (argc>3))
        {
           printf("ADLINK Watchdog Timer Utility of aTCA-
      6150.\n\n");
           printf("  Usage: WDT6150 value [i]\n");
          printf("        value is from 1 to 15300, the unit is
      second.\n");
           printf("         Write 0 will disable watchdog
      timer.\n\n");
           printf("         i - change IO port to 0x2E. Default
      is 0x4E.\n");
           exit(1);
        }
      else
        {
            if(argc==3) ioport=0x2E;
           //Detect W83627UHG.
             Enter_W627UHG_Config(ioport);

           //Get Chip ID Hi Byte = 0xA2, Chip ID LO Byte = 0x3x
             outportb(ioport, 0x20);
             DevID1 = inportb(ioport+1);
             outportb(ioport, 0x21);
             DevID2 = inportb(ioport+1);

               if((DevID1 == 0xA2) && ((DevID2 & 0xF0) == 0x30))
                  chipflag = 1;
```

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```
            if(chipflag == 0)
              {
               printf("ADLINK Watchdog Timer Utility of aTCA-
      6150.\n\n");
               printf("Can't find any Winbond W83627UHG on
      system!\n");
               Exit_W627UHG_Config(ioport);
               exit(1);
              }
            else
              {
               printf("ADLINK Watchdog Timer Utility of aTCA-
      6150.\n\n");
                 number=atoi(argv[1]);

                 WDTRUN(ioport,number);
                 Exit_W627UHG_Config(ioport);
              }
       }
}

void Enter_W627UHG_Config(int config_port)
{
      outportb(config_port, 0x87);
      outportb(config_port, 0x87);
}
void Exit_W627UHG_Config(int config_port)
{
      outportb(config_port, 0xAA);
}
void WDTRUN(int config_port,int count_value)
{
   int temp;
   int counter;

      //Select WDT device
        outportb(config_port, 0x07);
        outportb(config_port+1, 0x08);//device 8

      //Activate WDT device
        outportb(config_port, 0x30);
        temp = inportb(config_port+1);
        temp = temp | 0x01;
        outportb(config_port+1, temp);

      //Set second/minute mode
        outportb(config_port, 0xF5);
```

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```
        temp = inportb(config_port+1);
        temp = temp & 0xFD;//disable WDTO to KBRST#.
        if(count_value <= 60)
          temp = temp & 0xF7;//second.

      //Count the timeout value
      if(((count_value>60) && (count_value<=15300)) ||
      (count_value > 15300))
        {
          if(count_value > 15300)
            count_value = 15300;
          counter = count_value/60;
          if((count_value%60)>30)
            counter=counter+1;
          printf("WDT timeout in %d minutes.",counter);
          temp = temp | 0x08;//Count in minute mode.
          outportb(config_port+1, temp);
        }
      else
        {
          if(count_value == 0)
            {
            counter = count_value;
            printf("WDT is Disabled.");
            }
          else
            {
            counter = count_value;
            printf("WDT timeout in %d seconds.",counter);
            outportb(config_port+1, temp);
              }
            }

      //reset WDT by KB, MS interrupt
        outportb(config_port, 0xF7);
        temp = inportb(config_port + 1);
        temp = temp | 0xC0;//Bit 6 = KB interrupt, Bit 7 = MS
      interrupt
        outportb(config_port+1, temp);
      //Write count value
        outportb(config_port, 0xF6);
        outportb(config_port+1, counter);
}
```

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8 BIOS Setup

The following chapter describes basic navigation for the AMIBIOS®8 BIOS setup utility.

8.1 Starting the BIOS

To enter the setup screen, follow these steps:

1. Power on the motherboard
2. Press the < Delete > key on your keyboard when you see the following text prompt:
   < Press DEL to run Setup >
3. After you press the < Delete > key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu, such as Chipset and Power menus.



Note: In most cases, the < Delete > key is used to invoke the setup screen. There are several cases that use other keys, such as < F1 >, < F2 >, and so on.

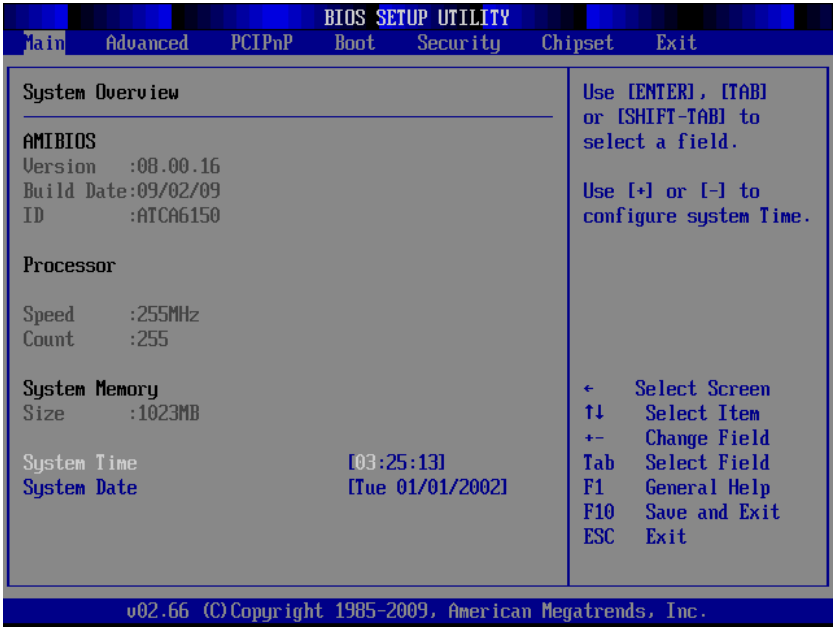
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Setup Menu

The main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in this user's guide.

The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed" options cannot be configured, "Blue" options can be.

The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

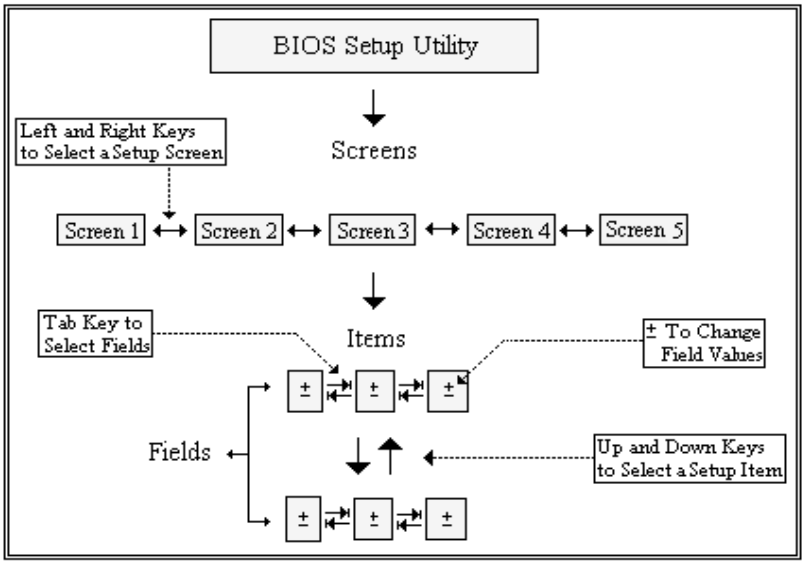


Navigation

The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process.

These keys include < F1 >, < F10 >, < Enter >, < ESC >, < Arrow > keys, and so on. .

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Note: There is a hot key legend located in the right frame on most setup screens.

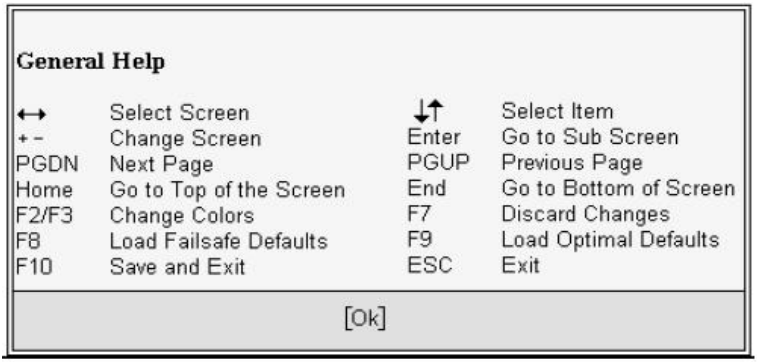
The < F8 > key on your keyboard is the Fail-Safe key. It is not displayed on the key legend by default. To set the Fail-Safe settings of the BIOS, press the < F8 > key on your keyboard. It is located on the upper row of a standard 101 keyboard. The Fail-Safe settings allow the motherboard to boot up with the least amount of options set. This can lessen the probability of conflicting settings.

Hotkey Descriptions

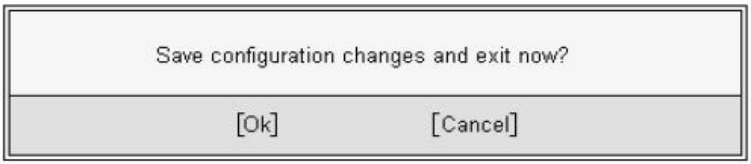
F1 The < F1 > key allows you to display the General Help screen.

Press the < F1 > key to open the General Help screen.

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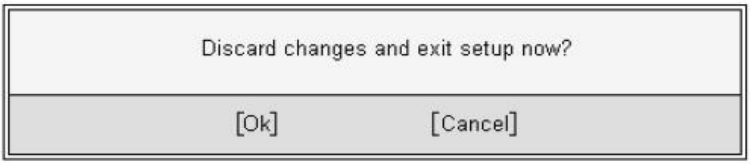


F10 The < F10 > key allows you to save any changes you have made and exit Setup. Press the < F10 > key to save your changes. The following screen will appear:



Press the < Enter > key to save the configuration and exit. You can also use the < Arrow > key to select Cancel and then press the < Enter > key to abort this function and return to the previous screen.

ESC The < Esc > key allows you to discard any changes you have made and exit the Setup. Press the < Esc > key to exit the setup without saving your changes. The following screen will appear:



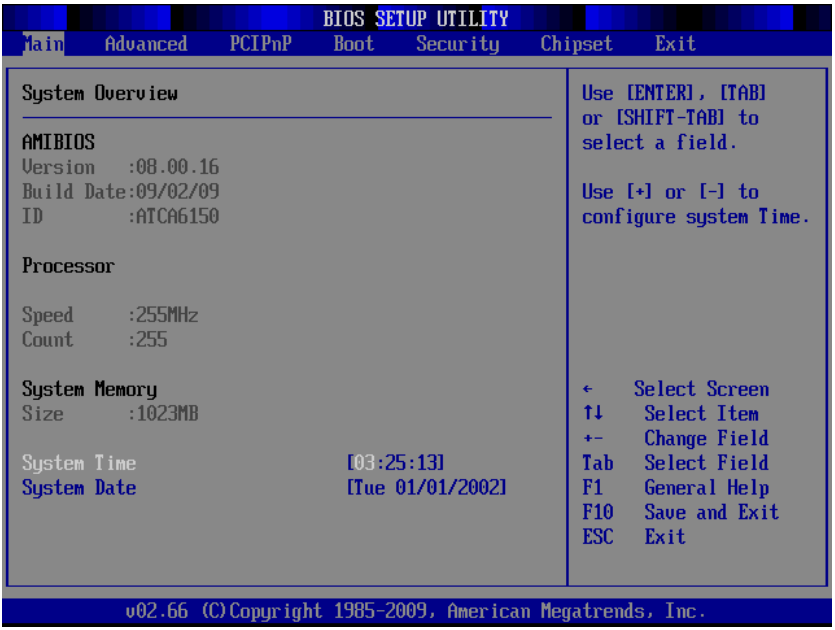
Press the < Enter > key to discard changes and exit. You can also use the < Arrow > key to select Cancel and then press the < Enter > key to abort this function and return to the previous screen.

Enter The < Enter > key allows you to display or change the setup option listed for a particular setup item. The < Enter > key can also allow you to display the setup sub-screens.

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8.2 Main Setup

When you first enter the Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



System Time/System Date

Use this option to change the system time and date. Highlight System Time or System Date using the < Arrow > keys. Enter new values using the keyboard. Press the < Tab > key or the < Arrow > keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

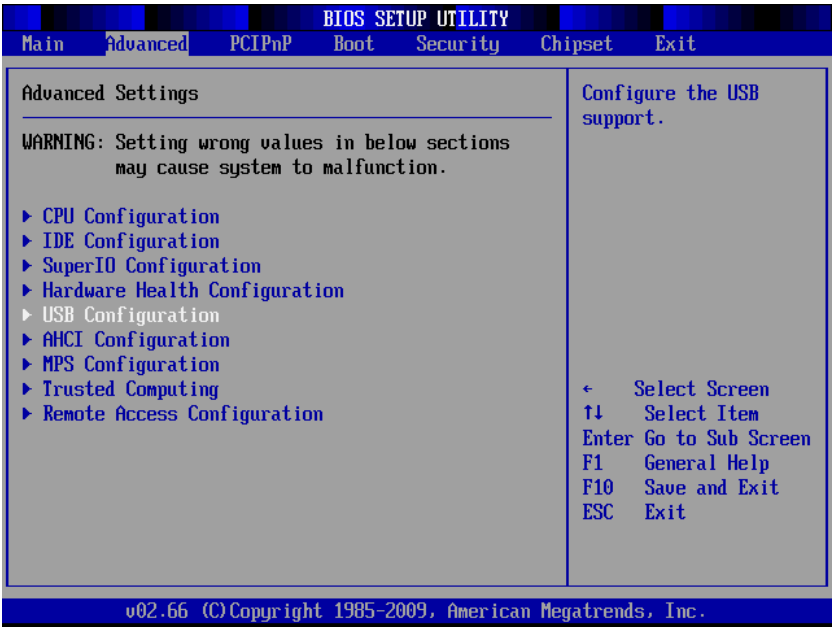
Note: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

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8.3 Advanced BIOS Setup

Select the Advanced tab from the setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as SuperIO Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the < Arrow > keys. The Advanced BIOS Setup screen is shown below.

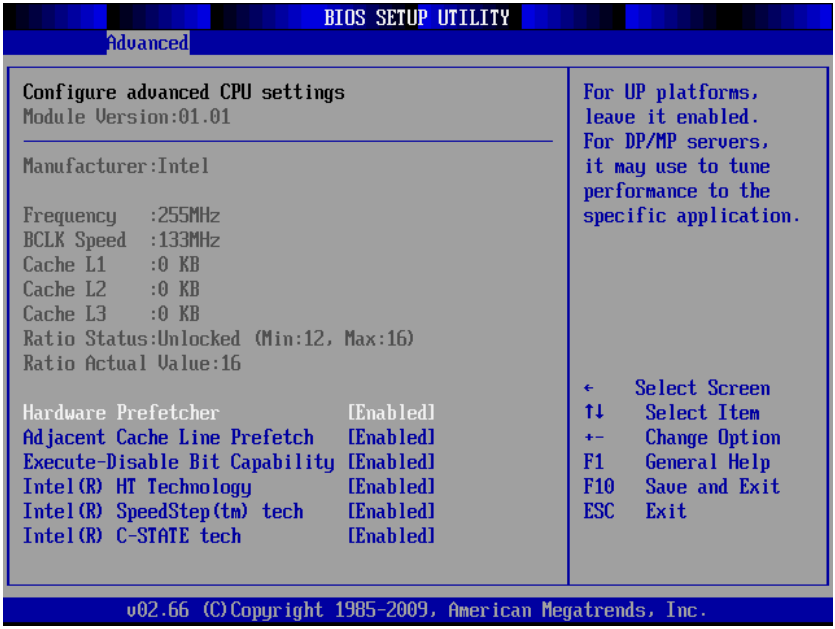
The sub menus are described on the following pages.



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8.3.1 CPU Configuration

You can use this screen to select options for the CPU Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the CPU Configuration screen is shown below.



Hardware Prefetcher

This is used for reducing the waiting time of DRAM. The hardware prefetcher looks for streams of data and tries to predict what data will be needed next by the processor and proactively tries to fetch these data.

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Adjacent Cache Line Prefetch

This is used to choose the optimal use of sequential memory access for performance purpose. Disable this setting for applications that require high use of random memory access.

Execute-Disable Bit Capability

Intel's Execute Disable Bit is an hardware-based security feature that can help reduce system exposure to viruses and malicious code. It allows the processor to classify areas in memory where application code can or cannot execute. When a malicious worm attempts to insert code in the buffer, the processor disables code execution, preventing damage and worm propagation. To use Execute Disable bit you must have a PC or server with a processor with Execute Disable Bit capability and a supporting operating system.

Intel® HT Technology

Hyper-Threading Technology is used to improve parallelization of computations performed on PC microprocessors. A processor with hyper-threading enabled is treated by the operating system as two processors instead of one.

Intel® Speedstep™ Technology

Intel® SpeedStep™ technology allows the system to dynamically adjust processor voltage and core frequency, which can result in decreased average power consumption and decreased average heat production.

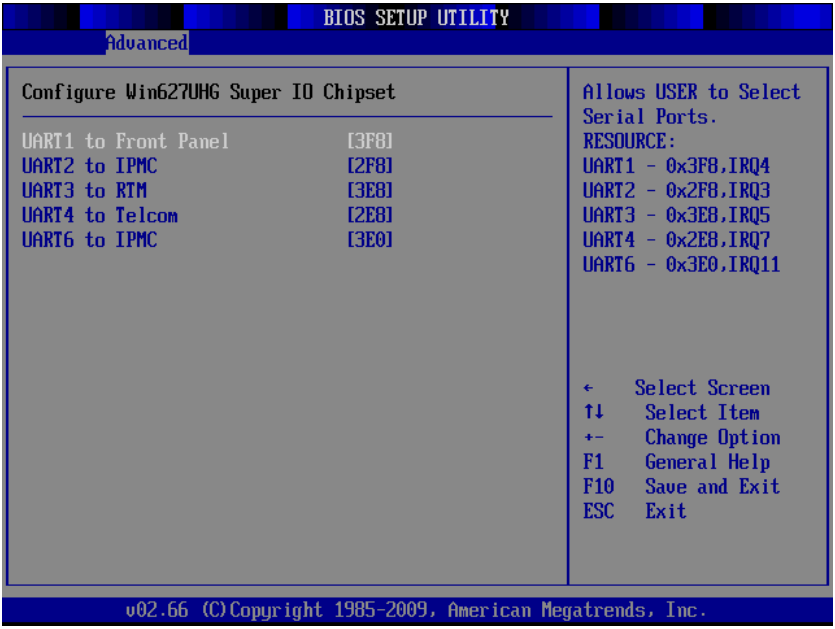
Intel® C-State Technology

This function controls the availability of the CPU C-state power saving technology.

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8.3.2 Super IO Configuration

You can use this screen to select options for the Super IO settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



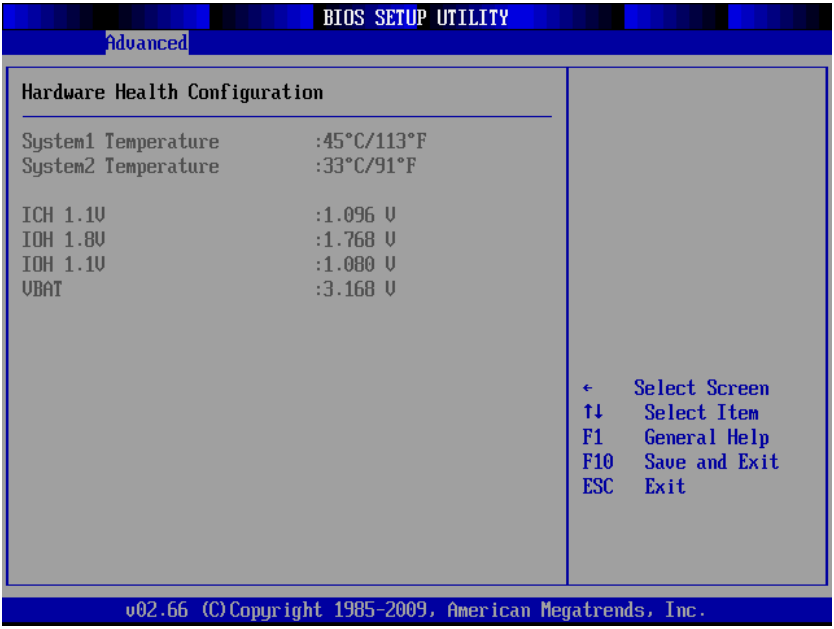
UART1 to Front Panel, UART2 to IPMC, UART3 to ZONE2, UART4 to Telecom, UART6 to IPMC

These items are for enabling/disabling the serial port to the Front Panel, IPMC, RTM, and Telecom. Detailed resources for these serial ports are listed in the help field of the setup screen.

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8.3.3 Hardware Health Configuration

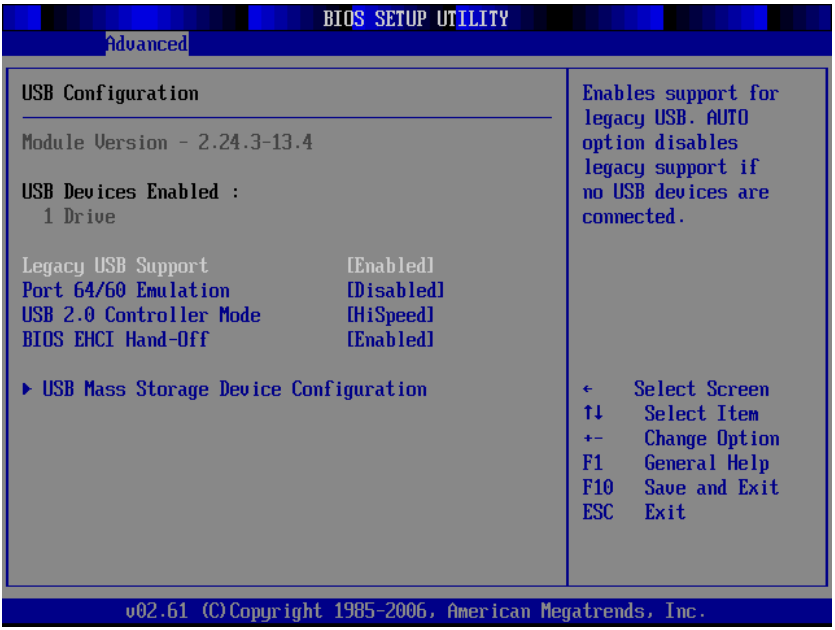
This option displays the current status of all of the monitored hardware devices/components such as voltages and temperatures.



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8.3.4 USB Configuration

You can use this screen to select options for the USB Configuration. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



Legacy USB Support

Legacy USB Support refers to USB mouse and keyboard support. Normally if this option is not enabled, any attached USB mouse or USB keyboard will not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or USB keyboard can control the system even when there are no USB drivers loaded on the system. Set this value to enable or disable the Legacy USB Support.

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- **Disabled:** Set this value to prevent the use of any USB device in DOS or during system boot.
- **Enabled:** Set this value to allow the use of USB devices during boot and while using DOS.
- **Auto:** This option auto detects USB Keyboards or Mice and if found, allows them to be utilized during boot and while using DOS.

Port 64/60 Emulation

This option uses USB to receive the IO port 64/60 trap to emulate the legacy keyboard controller.

USB 2.0 Controller Mode

The USB 2.0 Controller Mode configures the data rate of the USB port. The options are **FullSpeed** (12 Mbps) and **HiSpeed** (480 Mbps).

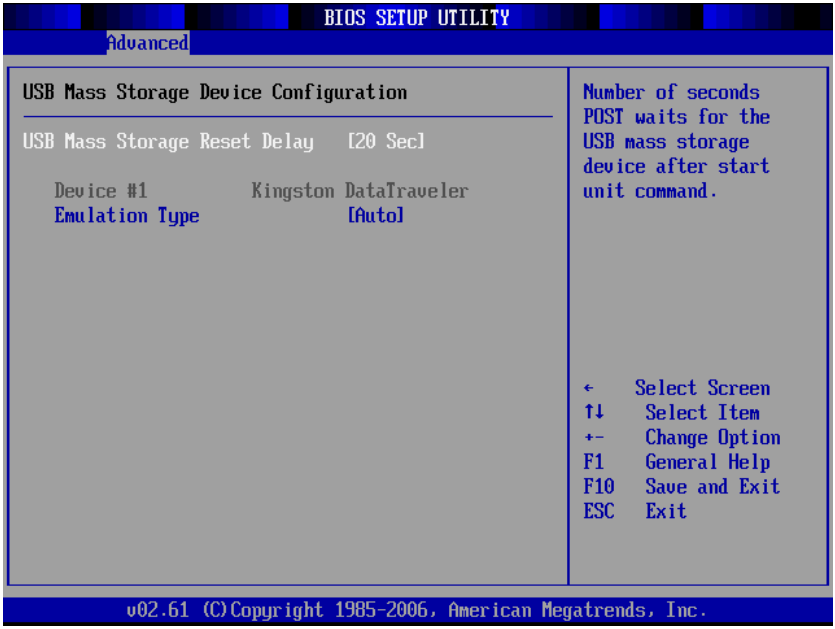
BIOS EHCI hand-off

This option provides a workaround for operating systems without ECHI hand-off support. The EHCI ownership change should be claimed by the EHCI driver.

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USB Mass Storage Device Configuration

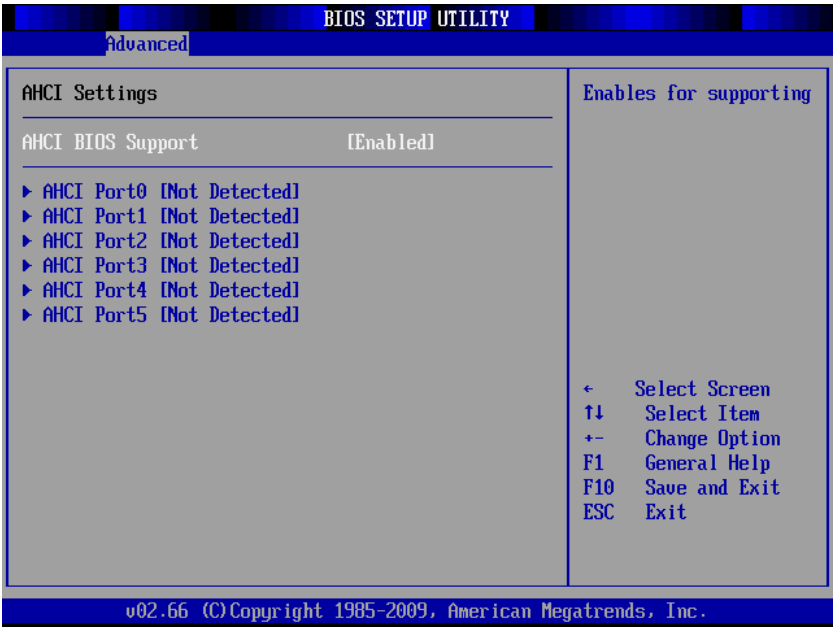
This is a submenu for configuring the USB Mass Storage Class Devices when BIOS finds they are in use on USB ports. Emulation Type can be set according to the type of attached USB mass storage device(s). If set to Auto, USB devices less than 530MB will be emulated as Floppy and those greater than 530MB will remain as hard drive. The Forced FDD option can be used to force a hard disk type drive (such as a Zip drive) to boot as FDD.



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8.3.5 AHCI Configuration

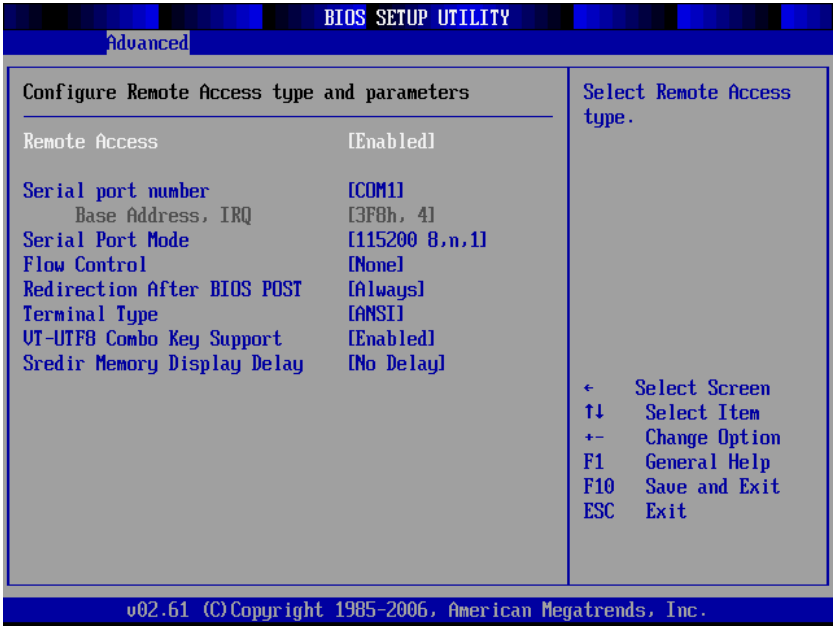
This screen allows you to enable/disable AHCI BIOS support. When enabled, BIOS will detect the presence of AHCI disks and show which port they are on.



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8.3.6 Remote Access Configuration

Remote access configuration provides the settings to allow remote access by another computer to get POST messages and send commands through serial port access.



Remote Access

Select this option to Enable or Disable the BIOS remote access feature.

Note: Enabling Remote Access requires a dedicated serial port connection. Once both serial ports are configured to disabled, you should set this value to Disabled or it may cause abnormal boot.

Serial Port Number

Select the serial port you want to use for the remote access interface. You can set the value for this option to COM1 or COM3.

Note: If you have changed the resource assignment of the serial ports in Advanced> SuperIO Configuration, you must Save Changes and Exit, reboot the system, and enter the setup menu again in order to see those changes reflected in the available Remote Access options.

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Serial Port Mode

Select the baud rate you want the serial port to use for console redirection. The options are **115200 8,n,1**; **57600 8,n,1**; **19200 8,n,1**; and **09600 8,n,1**.

Flow Control

Set this option to select Flow Control for console redirection. The settings for this value are **None**, **Hardware**, or **Software**.

Redirection After BIOS POST

This option allows you to set Redirection configuration after BIOS POST. The settings for this value are **Disabled**, **Boot Loader**, or **Always**.

- **Disabled:** Set this value to turn off the redirection after POST
- **Boot Loader:** Set this value to allow the redirection to be active during POST and Boot Loader.
- **Always:** Set this value to allow the redirection to be always active.

Terminal Type

This option is used to select either VT100/VT-UTF8 or ANSI terminal type. The settings for this value are **ANSI**, **VT100**, or **VT-UTF8**.

VT-UTF8 Combo Key Support

This option enables VT-UTF8 Combination Key Support for ANSI/VT100 terminals. The settings for this value are **Enabled** or **Disabled**.

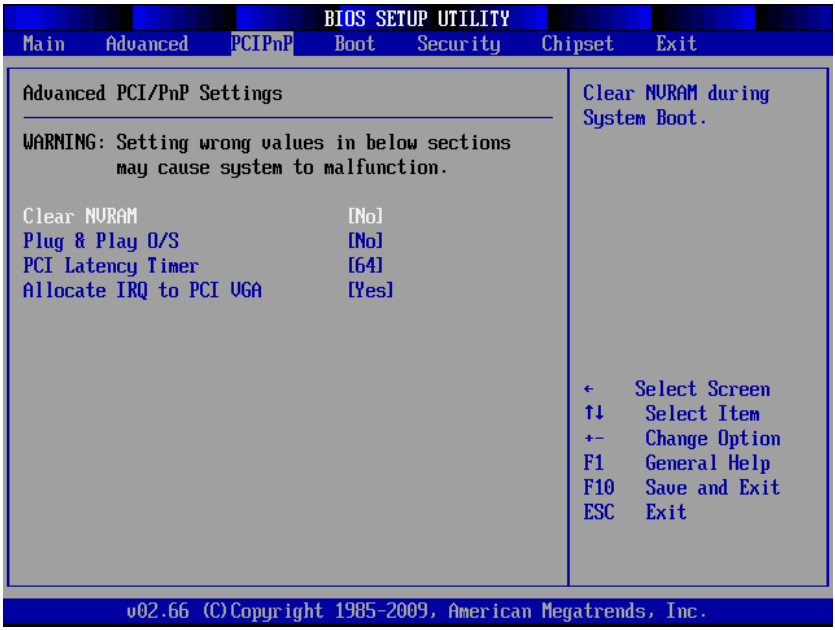
Sredir Memory Display Delay

This option gives the delay in seconds to display memory information. The options for this value are **No Delay**, **Delay 1 Sec**, **Delay 2 Sec**, or **Delay 4 Sec**.

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8.4 Advanced PCI/PnP Settings

Select the PCI/PnP tab from the setup screen to enter the Plug and Play BIOS Setup screen. You can display a Plug and Play BIOS Setup option by highlighting it using the < Arrow > keys. The Plug and Play BIOS Setup screen is shown below.



Clear NVRAM

Set this to enable/disable Clear NVRAM during system boot. NVRAM content like ESCD will be cleared and updated at next boot.

Plug & Play O/S

- **No:** Let the BIOS configure all the devices in the system.
- **Yes:** Let the operating system configure Plug and Play (PnP) devices not required for boot if your system has a Plug and Play operating system.

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PCI Latency Timer

Set this value to allow the PCI Latency Timer to be adjusted. This option sets the latency of all PCI devices on the PCI bus.

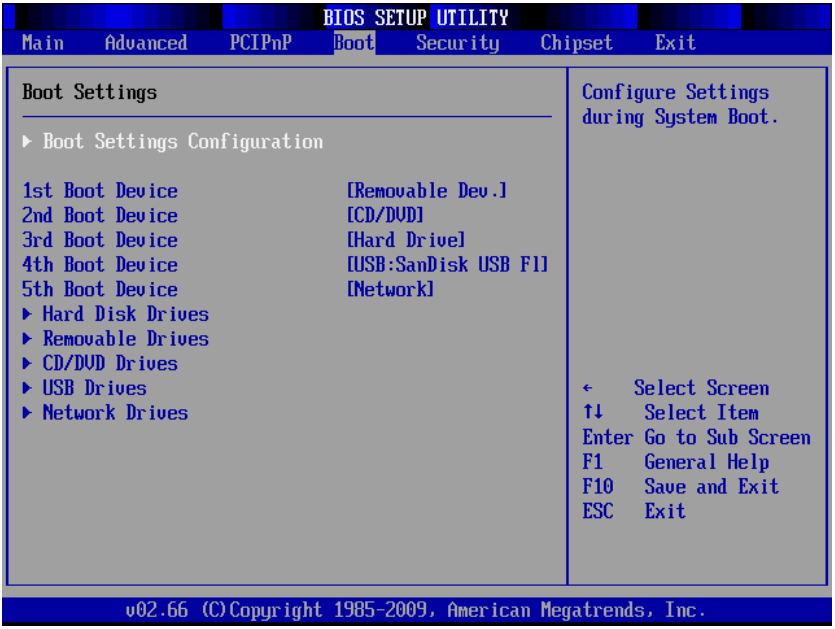
Allocate IRQ to PCI VGA

This options assigns IRQs to the PCI VGA card.

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8.5 Boot Settings

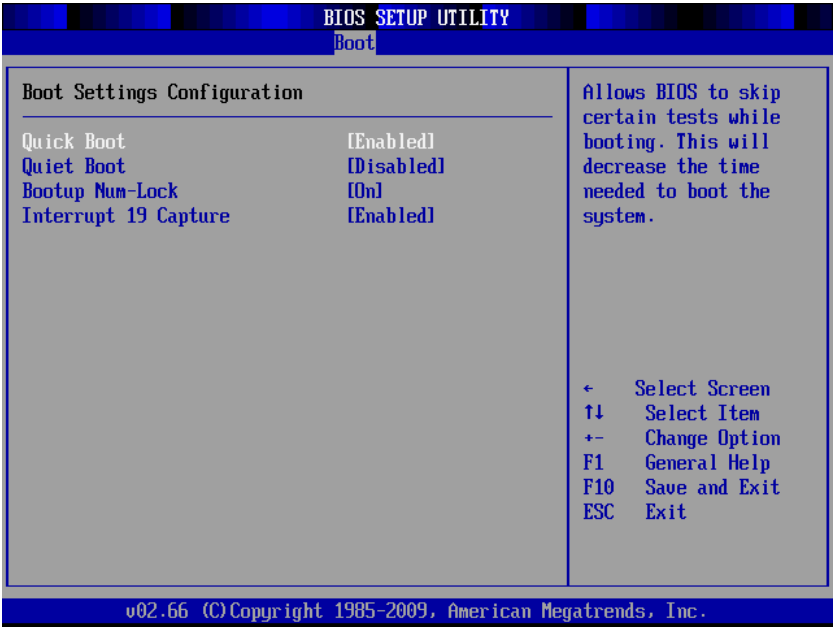
Select the Boot tab from the setup screen to enter the Boot BIOS Setup screen. You can select any of the items in the left frame of the screen, such as Boot Device Priority, to go to the sub menu for that item. You can display a Boot BIOS Setup option by highlighting it using the < Arrow > keys. The Boot Settings screen is shown below:



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8.5.1 Boot Settings Configuration

Use this screen to select options for the Boot Settings Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



Quick Boot

Disabled – Set this value to allow the BIOS to perform all POST tests.

Enabled – Set this value to allow the BIOS to skip certain POST tests to boot faster.

Quiet Boot

Disabled – Set this value to allow the computer system to display the POST messages.

Enabled – Set this value to allow the computer system to display the OEM logo.

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Bootup Num-Lock

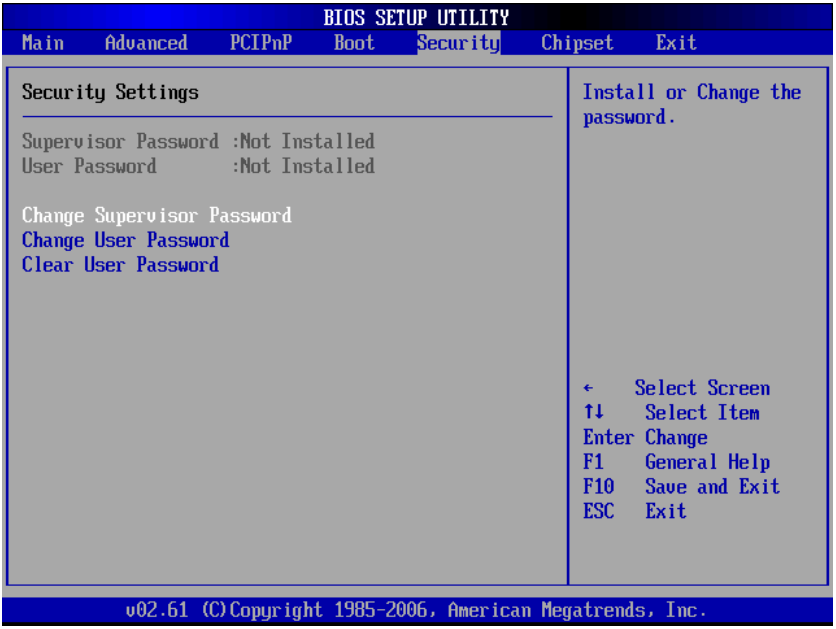
Set this value to allow the Number Lock setting to be modified during boot up. **Off** – This option does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard will light up when the Number Lock is engaged. **On** – Set this value to allow the Number Lock on the keyboard to be enabled automatically when the computer system is boot up. This allows the immediate use of 10-keys numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard will be lit.

Interrupt 19 Capture

When enabled, allows option ROMs to trap interrupt 19.

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8.6 Security Setup



Password Support

Two Levels of Password Protection

Provides both a Supervisor and a User password. If you use both passwords, the Supervisor password must be set first.

The system can be configured so that all users must enter a password every time the system boots or when Setup is executed, using either or either the Supervisor password or User password.

The Supervisor and User passwords activate two different levels of password security. If you select password support, you are prompted for a one to six character password. Type the password on the keyboard. The password does not appear on the screen when typed. Make sure you write it down. If you forget it, you must drain NVRAM and re-configure.

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Remember the Password

Keep a record of the new password when the password is changed. If you forget the password, you must erase the system configuration information in NVRAM.

To access the sub menu for the following items, select the item and press < Enter >:

- Change Supervisor Password
- Change User Password
- Clear User Password

Supervisor Password

Indicates whether a supervisor password has been set.

User Password

Indicates whether a user password has been set.

Change Supervisor Password

Select this option and press < Enter > to access the sub menu. You can use the sub menu to change the supervisor password.

Change User Password

Select this option and press < Enter > to access the sub menu. You can use the sub menu to change the user password.

Clear User Password

Select this option and press < Enter > to access the sub menu. You can use the sub menu to clear the user password.

Change Supervisor Password

Select Change Supervisor Password from the Security Setup menu and press < Enter >.

Enter New Password:

Type the password and press < Enter >. The screen does not display the characters entered. Retype the password as prompted and press < Enter >. If the password confirmation is incorrect, an

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error message appears. The password is stored in NVRAM after completes.

Change User Password

Select Change User Password from the Security Setup menu and press < Enter >.

Enter New Password:

Type the password and press < Enter >. The screen does not display the characters entered. Retype the password as prompted and press < Enter >. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after completes.

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8.7 Chipset Setup

Select the Chipset tab from the setup screen to enter the Chipset BIOS Setup screen. You can select any of the items in the left frame of the screen to go to the sub menu for that item. The Chipset BIOS Setup screen is shown below.



Onboard SAS Controller

Set this value to Enable/Disable SAS controller.

Boots Graphic Adapter Priority

Set this value to decide which BUS, PCI or PCIE, get first VGA boot priority.

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CPU Bridge Configuration

The CPU Bridge configuration displays the information and setting of QPI (Quick Path Interface) and memory.



QPI Links Speed

Set to Full-speed for normal operation. Slow-mode is used for debugging.

QPI Frequency

Auto: Let BIOS decide the frequency that CPUs can support (strongly recommend).

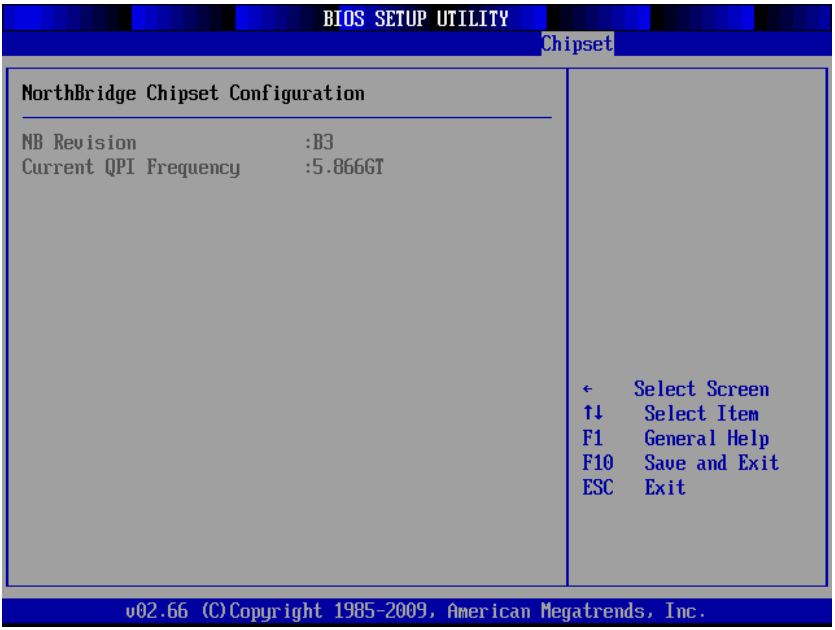
Memory Frequency

Auto: Let BIOS decide the frequency that all memory DIMMs can support (strongly recommend).

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North Bridge Configuration

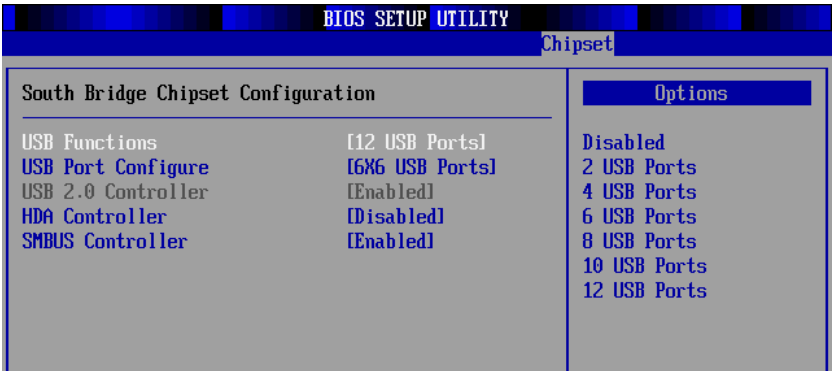
The North Bridge Chipset Configuration screen displays information about the IOH.



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South Bridge Configuration

The South Bridge Chipset Configuration screen displays information and settings for the ICH10R.



USB Functions

Set this value to allow the system to disable, enable, and select a set number of onboard USB ports.

USB Port Configure

The ICH10R contains 2 EHCI controllers which support a total of 12 USB ports. Each EHCI connects 6 ports by default (6x6 USB Ports). Set this option to “8x4 USB Ports” to move ports 11 and 12 from EHCI2 to ECHI1.

USB 2.0 Controller

This option takes effect only when USB Functions are enabled. Enabling will allow USB 2.0 functionality to all USB ports.

HDA Controller

Set this value to Enable/Disable the High Definition Audio Controller.

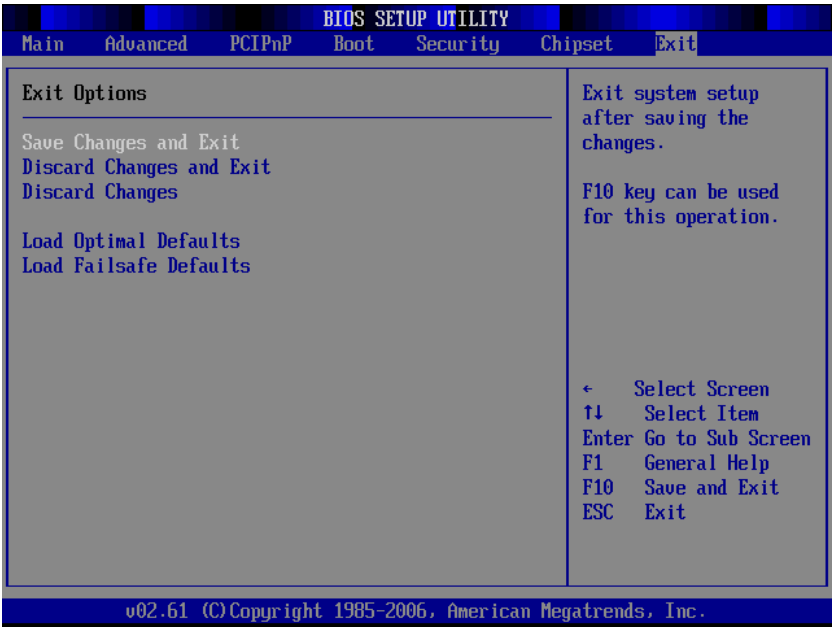
SMBUS Controller

Set this value to enable/disable the SMBUS Controller

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8.8 Exit Menu

Select the Exit tab from the setup screen to enter the Exit BIOS Setup screen. You can display an Exit BIOS Setup option by highlighting it using the < Arrow > keys. The Exit BIOS Setup screen is shown below.



Save Changes and Exit

When you have completed the system configuration changes, select this option to leave Setup and reboot the computer so the new system configuration parameters can take effect.

Save Configuration Changes and Exit Now?

[Ok] [Cancel]

appears in the window. Select Ok to save changes and exit.

Discard Changes and Exit

Select this option to quit Setup without making any permanent changes to the system configuration.

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Discard Changes and Exit Setup Now?

[Ok] [Cancel]

appears in the window. Select Ok to discard changes and exit.

Discard Changes

Select Discard Changes from the Exit menu and press < Enter >.

Select Ok to discard changes.

Load Optimal Defaults

Automatically sets all Setup options to a complete set of default settings when you select this option. The Optimal settings are designed for maximum system performance, but may not work best for all computer applications. In particular, do not use the Optimal Setup options if your computer is experiencing system configuration problems.

Select Load Optimal Defaults from the Exit menu and press < Enter >.

Select Ok to load optimal defaults.

Load Failsafe Defaults

Automatically sets all Setup options to a complete set of default settings when you select this option. The Failsafe settings are designed for maximum system stability, but not maximum performance. Select the FailSafe Setup options if your computer is experiencing system configuration problems.

Select Load Fail-Safe Defaults from the Exit menu and press < Enter >.

Load FailSafe Defaults?

[Ok] [Cancel]

appears in the window. Select Ok to load FailSafe defaults.

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8.9 BIOS Update Procedure

Download the BIOS binary file from ADLINK web site or Technical Service department. Extract the compressed file and execute P.BAT to update the BIOS. Please note that the name of the BIOS file will reflect the BIOS revision. The example below will update the BIOS using the file A6150T12. ROM.

```
*******************************************************
C:\BIOS\AT6150>dir/w

 Volume in drive C has no label
 Volume Serial Number is 0065-1CB9
 Directory of C:\BIOS\AT6150

[.]   [..]   A6150T12.ROM    AFUDOS.EXE     AFUWIN.EXE
HISTORY.TXT   P.BAT    UCORESYS.SYS    UCOREW64.SYS
         7 file(s)      2,623,464 bytes
         2 dir(s)     867,123,200 bytes free

C:\BIOS\AT6150>p.bat

C:\BIOS\AT6150>afudos a6150t12.rom /p /b /reboot


*******************************************************
*       AMI Firmware Update Utility  Ver.4.12         *
  Copyright (C)2006 American Megatrends Inc. All Rights
                        Reserved
*******************************************************

- Bootblock checksum .... ok
- Bootblock checksum .... ok
- Module checksums ...... ok
- Erasing flash ......... done
- Writing flash ......... done
- Verifying flash ....... done
- Writing Bootblock ..... done
- Verifying Bootblock ... 0x000D3800 (100%)
*******************************************************
```

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Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.
- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

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A Lithium-type battery may be provided for uninterrupted, backup or emergency power.



Risk of explosion if battery is replaced with one of an incorrect type. Dispose of used batteries appropriately.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

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Getting Service

Contact us should you require any service or assistance.

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