ADLINK TECHNOLOGY INC.

aTCA-6250

Dual Intel Xeon E5-2658/2648L AdvancedTCA Processor Blade

User's Manual



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Revision History

Revision	Release Date	Description of Change(s)
2.00	July 10, 2012	Initial release
2.01	September 6, 2012	Add switch SW12 description
2.02	January 9, 2013	Add Safety and Getting Service sections

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1 Overview

1.1 Introduction

The ADLINK aTCA-6250 is a high performance AdvancedTCA® (ATCA) processor blade featuring dual 8-core Intel® Xeon® processor E5-2658/E5-2648L, Intel® C604 PCH, eight-channel memory up to 128GB of DDR3 memory and 400W power supply subsystem. Versatile connectivity includes dual 10GbE Fabric Interfaces, dual GbE Base Interfaces, quad front panel GbE egress ports, front panel dual COM and USB 2.0 ports and front panel VGA connector. An onboard SATA connector supports a disk on module (DOM) up to 32GB and the optional RTM (aTCA-R6270) supports dual 10GbE SFP+ ports, dual USB ports and dual hot-swappable SAS bays providing additional network throughput and storage capacities.

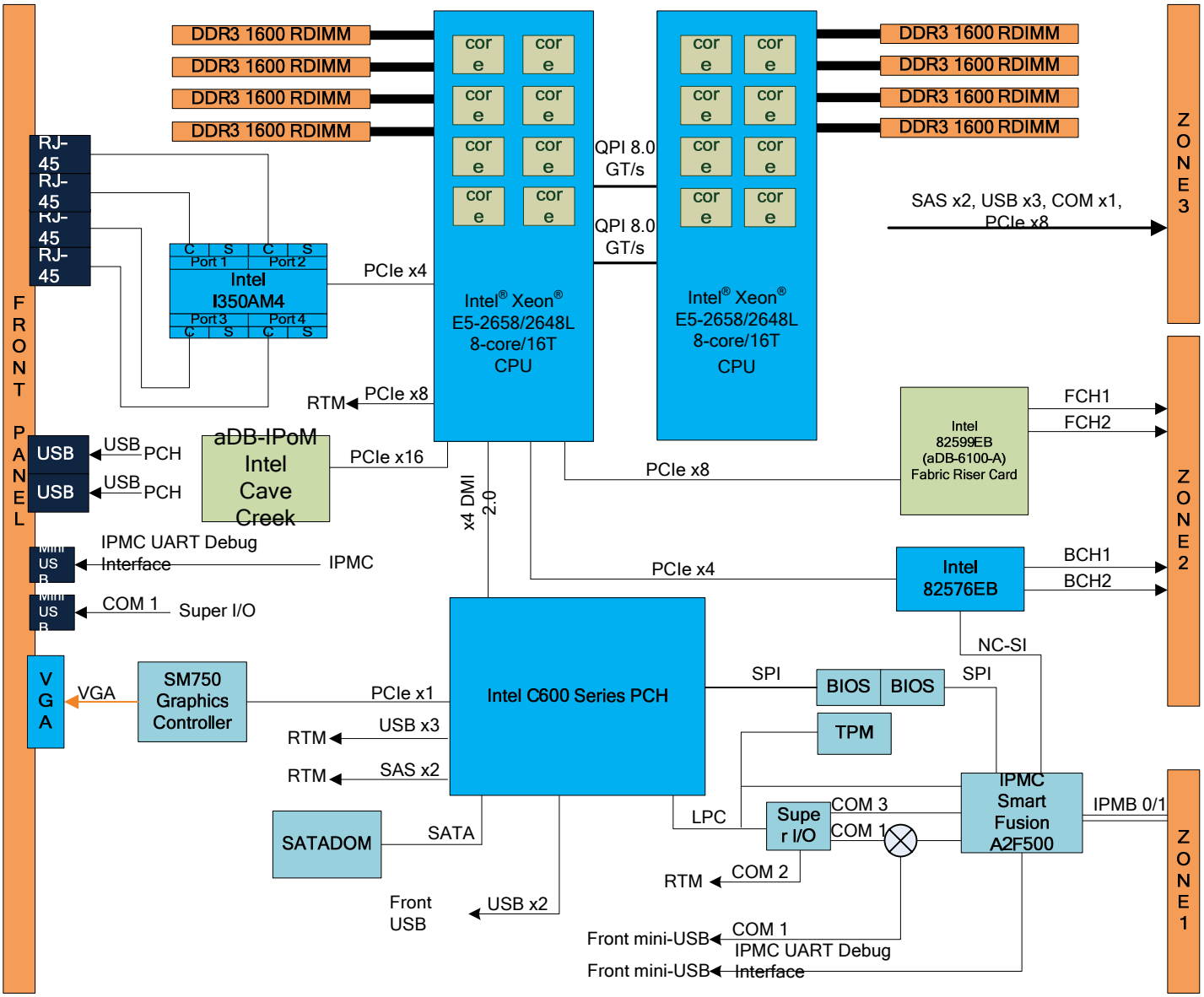
The aTCA-6250's thermal solution (including VRM heat sink) ensures stable operation under extreme operating environments and allows for compliance to the NEBS Level 3 standard (design only). The robust computing power and reliability of the aTCA-6250 meets the requirements of telecom equipment manufacturers (TEMs) and network equipment providers (NEPs), allowing them to build the next-generation telecom networks and communication infrastructures.

Detailed features are outlined below and a functional block diagram is shown in the next section.

- Two eight-core Intel® Xeon® processor E5-2658/E5-2648L
- Server-class Intel® C604 PCH
- DDR3-1600 JEDEC standard VLP RDIMM (REG/ECC), up to 128 GB
- Onboard bootable 16GB SATA Interface disk on module (max. 32GB)
- One Intel® I350 AM4 quad-port PCI Express Gigabit Ethernet controller
- One Intel® 82576EB dual-port PCI Express Gigabit Ethernet controller
- One Intel® 82599EB 10Gigabit Ethernet (XAUI) controller
- Optional Intel® 82599ES 10Gigabit Ethernet (SFP+) controller on RTM (aTCA-R6270)
- Optional dual SAS 3G interface drive bays on RTM (aTCA-R6270)
- Dual PICMG 3.1 Option 9 Fabric Interface channels
- Failover system BIOS
- Analog VGA output up to 1920x1440 resolution

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1.2 Block Diagram



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1.3 Package Contents

Before opening, please check the shipping carton for any damage. If the shipping carton and contents are damaged, notify the dealer for a replacement. Retain the shipping carton and packing material for inspection by the dealer. Obtain authorization before returning any product to ADLINK.

Check that the following items are included in the package. If there are any missing items, contact your dealer:

- aTCA-6250 AdvancedTCA processor blade (CPU, RAM specifications may differ depending on options selected)
- USB Mini-B to DB-9 cable (for front panel serial port)

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2 Specifications

2.1 aTCA-6250 Specifications

2.1.1 CPU/ Chipset/ Memory

CPU	Dual eight-core Intel® Xeon® processor E5-2658/E5-2648L, (2.1/1.8GHz QPI 8.0GT/s, 20MB L2 cache, LGA2011 Socket)
Chipset	Intel® C604 PCH
Memory	Registered ECC DDR3-1333/1600 VLP RDIMM Eight RDIMM sockets Up to 128GB

2.1.2 Standard and Interface

Standards	PICMG 3.0 R2.0 AdvancedTCA PICMG 3.1 AdvancedTCA Ethernet, Option 9
Networking	One quad-port Intel® I350 AM4 Gigabit Ethernet Controller One dual-port Intel® 82576EB Gigabit Ethernet Controller Four 10/100/1000BASE-T RJ45 ports on face plate Two 10/100/1000BASE-T Base Interface channels Two 10GBASE-BX4 Fabric Interface channels via Intel® 82599EB 10G Ethernet Controller on aDB-6100-A riser card (Option 9) Two 10GBASE SFP+ ports on RTM (aTCA-R6270)
Display	Silicon Motion SM750 graphics controller Front panel analog VGA connector supports up to 1920x1440 resolution
USB	Two USB 2.0 ports on front panel, Two USB 2.0 ports to RTM
Serial	One IPMC serial debug port (USB Mini-B) One RS-232 ports on front panel (USB Mini-B) One RS-232 port to RTM
Storage	Onboard SATA connector supports DOM up to 32GB Four SAS channels to RTM
Front Panel I/O	1x VGA port (DB-15) 2x USB 2.0 port (Type-A) 1x IPMC serial debug port (USB Mini-B connector) 1x RS-232 port (USB Mini-B connector) 4x GbE ports (RJ45) LEDs: OOS, Media, User and Hotswap Recessed reset button
Rear I/O (aTCA-R6270)	2x SFP+ ports (Intel® 82599ES 10G Ethernet Controller from PCIe x8 on CPU1) 1x RS-232 port (RJ-45) 2x USB 2.0 ports 2x SAS ports from Intel® C604 PCH

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2.1.3 Software

BIOS	AMI BIOS with 8Mbit flash memory
Supported OS	Microsoft Windows Server 2008 Microsoft Windows Server 2008 R2 Red Hat Enterprise Linux 6.2 Contact ADLINK for other OS availability

2.1.4 Mechanical & Environmental

Dimensions	322.25mm x 280mm x 30.48mm (H x D x W) - 6HP slot
Operating Temperature	Standard: 0°C to 55°C NEBS short-term: 0°C to 61°C (sea level)
Storage Temperature	-40°C to 85°C
Humidity	5% to 90% non-condensing
Shock	15G peak-to-peak, 11ms duration, non-operation
Vibration	Non-operating: 1.88 Grms, 5 to 500 Hz, each axis Operating: 0.5 Grms, 5 to 500Hz, each axis
Compliance	CE, FCC Class A, CUL, NEBS Level 3 (design)

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2.2 Power Consumption

This section provides information on the power consumption of the aTCA-6250.

System configuration
(1) Memory: 8x TS1GKR72V3HL 8GB DDR3-1600 ECC REG
(2) Graphics: Silicon Motion SM750
(3) Power Supply: Chroma DC Power supply 62012P-80-60
(4) CPU: 2x eight-core Intel® Xeon® processor E5-2658

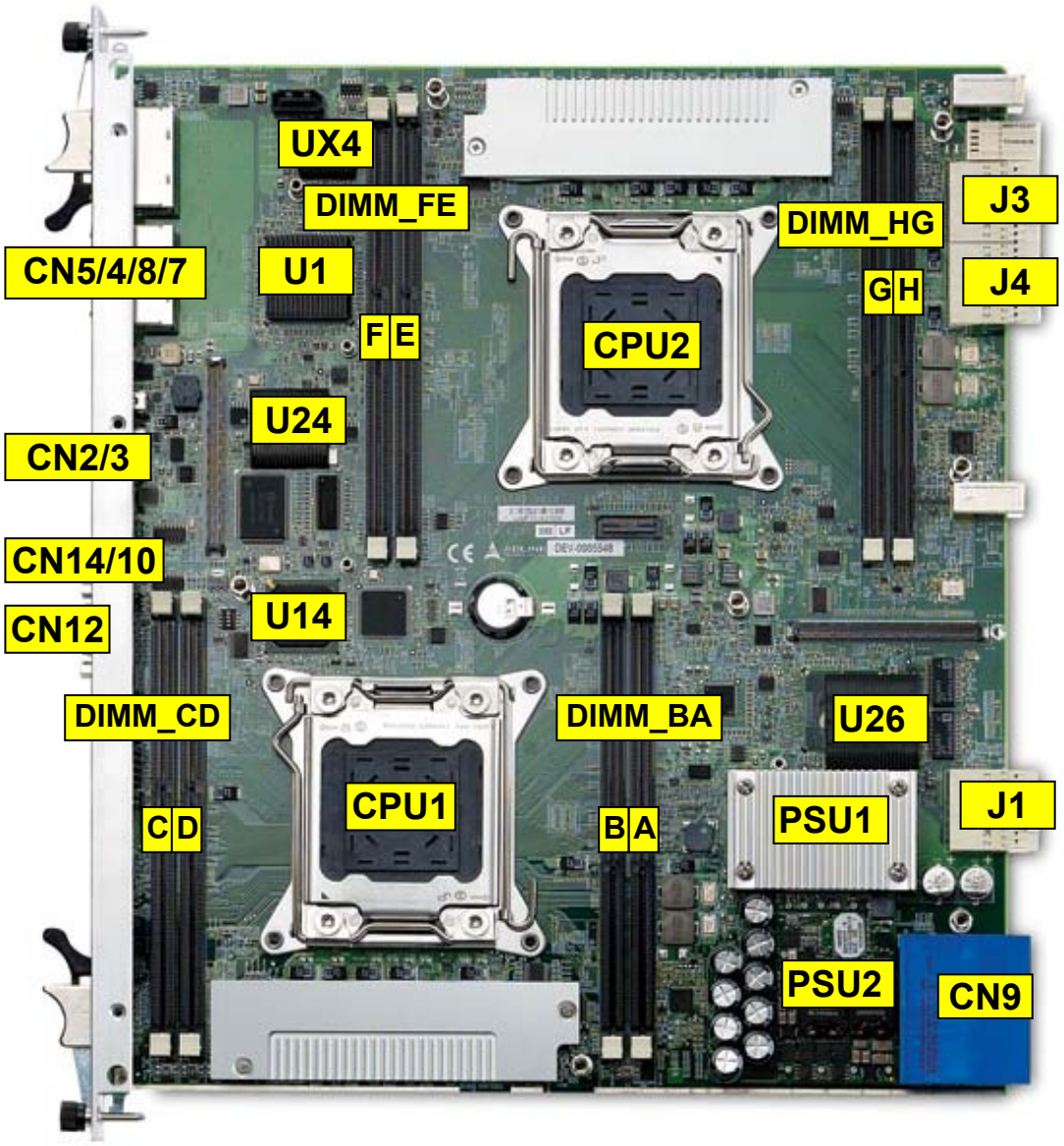
The following table lists power consumption under different operating systems and applications with a 48V power rail.

OS and Application	Power Consumption
DOS	**119.52 W**
Linux, Idle	**123.36 W**
Windows Server 2008 R2, idle	**75.84 W**
Windows Server 2008 R2, BurnIn Test, CPU 100% usage	**209.76 W**
Windows Server 2008 R2, Power Thermal Utility, CPU 100% Usage	**280.32 W**

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2.3 Board Layout

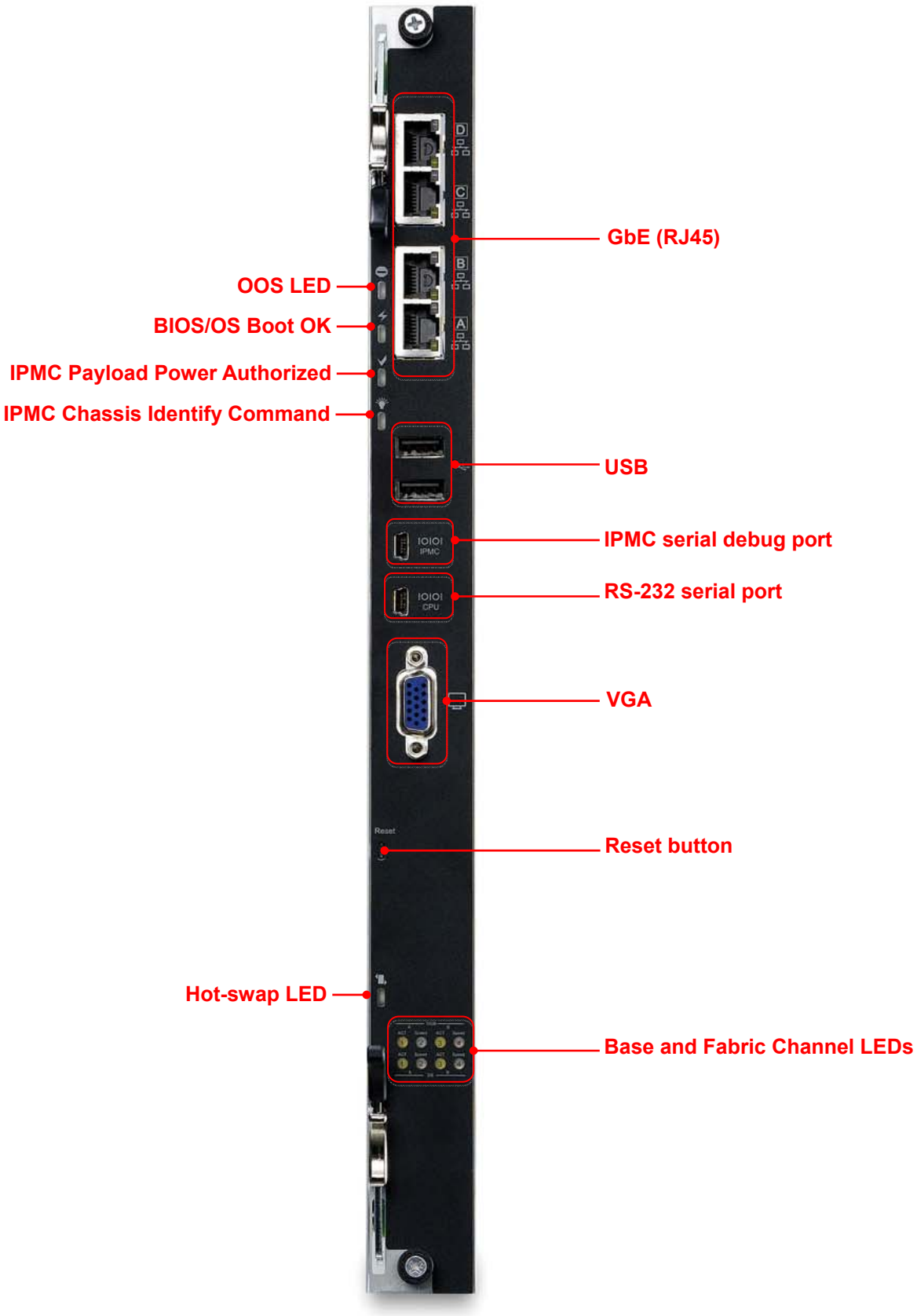
2.3.1 aTCA-6250 Board Layout



Location	Description	Location	Description
CN2/3	USB ports	J1	Base/Fabric Interface
CN4/5/7/8	GbE ports	J3/4	Zone 3 to RTM
CN9	Zone 1 Connector	U1	Intel C604 PCH
CN10/,14	Serial ports (USB Mini-B)	U24	Intel I350 AM4 NIC
CN12	VGA connector (DB-15)	U26	Intel 82576EB
CPU1	CPU1 Socket	UX4	Silicon Motion SM750
CPU2	CPU2 Socket	PSU1	400W -48V DC/DC module
DIMM_BA/CD	DDR3-1600 DIMM A-D	PSU2	400W Hotswap Power Module
DIMM_FE/HG	DDR3-1600 DIMM E-H		

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2.3.2 aTCA-6250 Front Panel



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2.3.3 Status LED Definitions

The following sections describe the front panel Status LEDs: Hot-swap LED, OOS LED, BIOS/OS Boot OK LED, IPMC Payload Power Authorized LED and IPMC Chassis Identify Command LED.

2.3.3.1 Out of Service (OOS) LED



Out of Service LED (Red)	State	Remark
Blinking	During BIOS POST	M4
Off	BIOS POST OK	M4
On	After OS shutdown	M1

2.3.3.2 BIOS/OS Boot OK



BIOS/OS Boot OK (Green)	State	Remark
Blinking	During OS Boot	
Off	During BIOS POST	
On	OS Boot OK	

2.3.3.3 IPMC Payload Power Authorized



IPMC Payload Power Authorized (Amber)	State	Remark
On	Payload Power Authorized	
Off	Payload Power Not Authorized	

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2.3.3.4 IPMC Chassis Identify Command LED



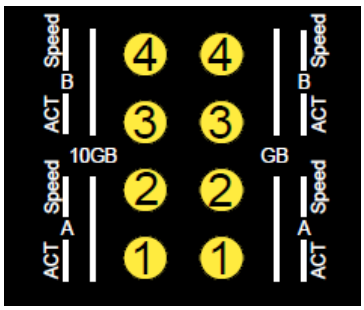
IPMC Chassis Identify Command (Amber)	State	Remark
Off	Default Off	
Blinking	Chassis Identify Command Active	

2.3.3.5 Hot-swap LED



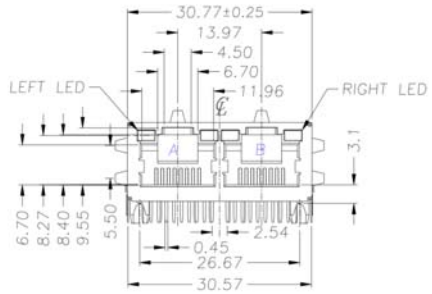
Hot-swap LED (Blue)	FRU State number	FRU State Name
Off	M0	FRU not installed
On	M1	FRU inactive
Long blink	M2	FRU activation request
Off	M3	FRU activation in process
Off	M4	FRU active
Short blink	M5	FRU deactivation request
Short blink	M6	FRU deactivation in process

2.3.3.6 Base and Fabric Channel LED

BASE Channel and Fabric Channel LED		
Fabric 2 Speed and Link 1Gbps – OFF 10Gbps – ON **(Amber)**		**BCH2** Speed and Link 100 Mbps: **Green** 1Gbps: **Amber**
Fabric 2 ACT **(Amber)** Blink when accessing Ethernet I/O		**BCH2** ACT **(Amber)** Blink when accessing Ethernet I/O
Fabric 1 Speed and Link 1Gbps - OFF 10Gbps – ON **(Amber)**		**BCH1** Speed and Link 100 Mbps: **Green** 1Gbps: **Amber**
Fabric 1 ACT **(Amber)** Blink when accessing Ethernet I/O		**BCH1** ACT **(Amber)** Blink when accessing Ethernet I/O

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2.3.3.7 GbE LED



LEFT LED: Speed and Link 1Gbps: **Amber**, 100Mbps: **Green**
RIGHT LED: ACT Blinking while data exchanging Color: **Amber**

2.4 Compliance

The aTCA-6250 conforms to the following specifications:

- PICMG 3.0 R2.0 ECN0002 AdvancedTCA
- PICMG 3.1 Ethernet over AdvancedTCA Option 9
- NEBS Level 3 (design)

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3 Functional Description

3.1 CPU, Memory and Chipset

3.1.1 CPU

The Intel® Xeon® processor E5-2658/E5-2648L implements several key technologies:

- Four channel Integrated Memory Controller supporting DDR3
- Integrated I/O with up to 40 lanes for PCI Express Generation 3.0
- Two point-to-point link interface based on Intel® QuickPath Interconnect (Intel® QPI) up to 8.0GT/s
- 20 MB of shared cache
- Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3) and Streaming SIMD Extensions 4 (SSE4)

The Intel® Xeon® processor E5-2658/E5-2648L supports several advanced technologies:

- Execute Disable Bit
- Intel® 64 Technology
- Enhanced Intel® SpeedStep® Technology
- Intel® Virtualization Technology (Intel® VT)
- Intel® Hyper-Threading Technology (Intel® HT Technology)

The Intel® Xeon® processor E5-2658/E5-2648L has a maximum TDP of 95W/70W and has an elevated case temperature specification. The elevated case temperatures are intended to meet the short-term thermal profile requirements of NEBS Level 3. The Intel® Xeon® processor E5-2658/E5-2648L is ideal for thermally constrained form factors in embedded servers, communications and storage markets.

Supported Processors, Maximum Power Dissipation

The following table describes the Intel® Xeon® processor E5 family CPUs supported by the aTCA-6250:

Name	E5-2648L	E5-2658
L2 cache	20MB	20MB
Clock	1.8GHz	2.1GHz
QPI	8.0 GT/s	8.0 GT/s
TDP	70W	95W

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3.1.2 Memory

The aTCA-6250 is a dual processor system with each Intel® Xeon® processor E5 providing four memory channels supporting DDR3 800, 1066, 1333, and 1600 MT/s DIMMs. The maximum memory capacity is 128GB with memory interleaving support. The 400/533/667/800 MHz differential memory clocks are driven by the Intel® Xeon® processor E5 CPU with length-matching and impedance controlled through all the DIMM slots.

The next generation of Xeon® family CPU is code named Ivy Bridge-EP. Each Ivy Bridge-EP provides four memory channels supporting DDR3 800, 1066, 1333, 1600 and 1866MT/s DIMMs. The maximum memory capacity is 128GB with memory interleaving support. The 400/533/667/800/933 MHz differential memory clocks are driven by the Ivy Bridge-EP CPU with length-matching and impedance controlled through all the DIMM slots.

The DDR3 DIMMs support the I^2C interface. They are connected together and routed to the PCH for the management.



Memory configuration changes are only permitted to be performed at the factory. Failure to comply with the above may result in damage to your board or improper operation.

3.1.3 Intel® C604 PCH Overview

The Intel® C604 Chipset PCH provides a connection point between various I/O components and DMI based processors. Functions and capabilities include:

- PCI Express Base Specification, Revision 2.0 support for up to eight ports with transfers up to 5 GT/s.
- PCI Local Bus Specification, Revision 2.3 support for 33 MHz PCI operations (supports up to four Req/Gnt pairs).
- ACPI Power Management Logic Support, Revision 4.0a Enhanced DMA controller, interrupt controller, and timer functions
- Integrated Serial Attached SCSI host controllers at transfer rate up to 3Gb/s on up to four ports.
- Integrated Serial ATA host controller switch independent DMA operation on up to six ports.
- USB host interface with two EHCI high-speed USB 2.0 Host controllers and 2 rate matching hubs provide support for support for up to fourteen USB 2.0 ports
- Integrated 10/100/1000 Gigabit Ethernet MAC with System Defense
- System Management Bus (SMBus) Specification, version 2.0 with additional support for I^2C devices
- Intel® High Definition Audio Supports
- Intel® Rapid Storage Technology enterprise (Intel® RSTe)
- Intel® Active Management Technology (Intel® AMT)
- Intel® Virtualization Technology for Directed I/O (Intel® VT-d)
- Intel® Trusted Execution Technology (Intel® TXT)
- Low Pin Count (LPC) interface Firmware Hub (FWH) interface
- Serial Peripheral Interface (SPI)
- Intel® Anti-Theft Technology (Intel® AT)
- JTAG Boundary Scan support

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3.1.4 Silicon Motion SM750 Graphics Controller

The aTCA-6250 provides an analog VGA port on the front panel powered by a Silicon Motion SM750 2D graphics controller with the following features:

- PCI-Express x1 architecture
- 16MB integrated video DDR memory
- Low power consumption < 1.5W
- 300 MHz DAC supports up to 1920x1440 resolution
- 128-bit 2D graphic engine
- ROPs, BitBLT, transparent BLT, pattern BLT, Color expansion, and Line drawing
- YUV-16/32-bit RGB conversion
- Support 7 layers of display frames (2 hardware cursors, primary graphic, video, video alpha, alpha, and secondary graphic)
- Two 8-bit portsorone16-bitvideocaptureportsupportsITU601
- and ITU 656 specifications UV-16/32-bit RGB conversion
- ReduceOn Power Management Technology
- Quick-Rotation features allow for 90°, 180°, and 270° rotation of on-screen images

3.2 Peripherals

The following peripherals are available on the aTCA-6250 blade

3.2.1 Reset

The aTCA-6250 is automatically reset by a precision voltage monitoring circuit that detects a drop in voltage below the acceptable operating limit of 4.85V for the 5V line and below 3.2V for the 3.3V line. Other reset sources include the Watchdog Timer, the face plate push-button switch and also the RESET signal from the IPMC. The aTCA-6250 responds to any of these sources by initializing local peripherals.

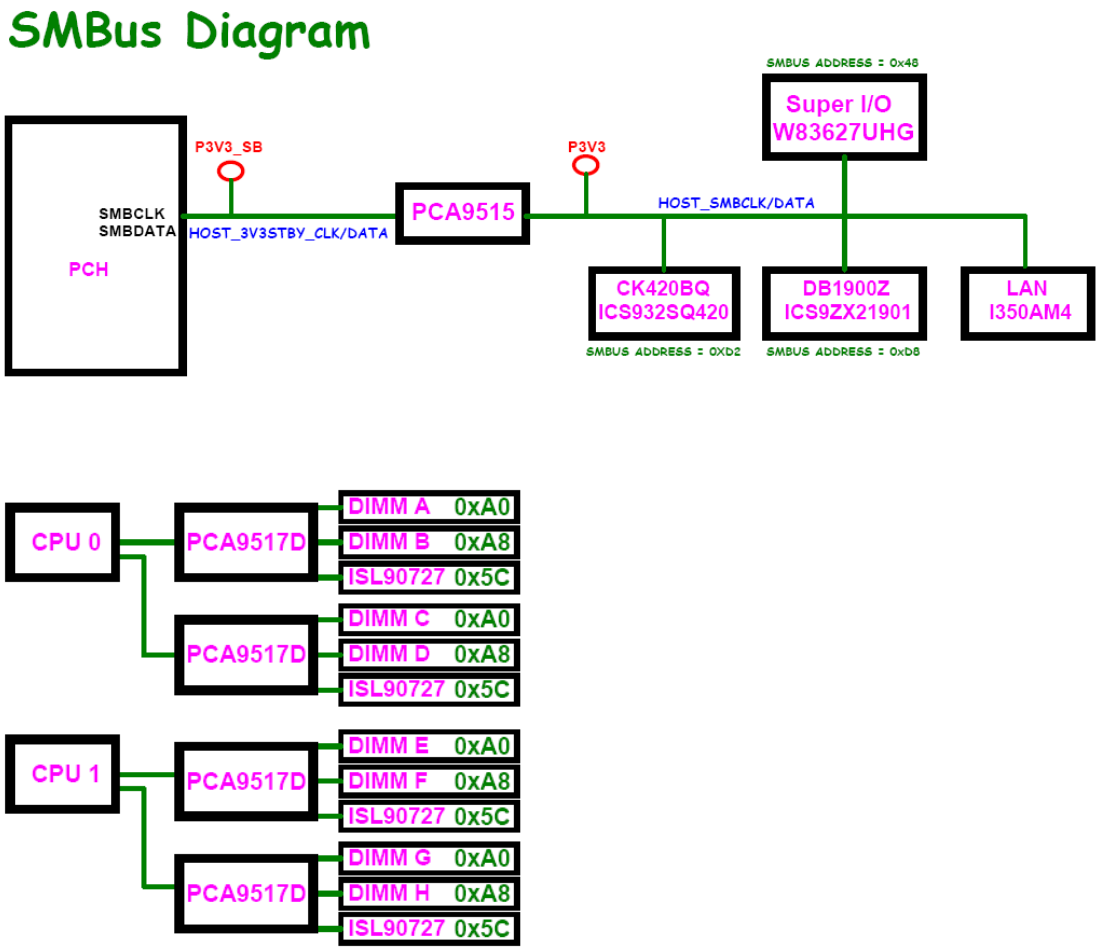
A reset will be generated by the following conditions:

- Power failure, +5 V supply falls below 4.1 V (typ.) or +3.3 V supply falls below 2.93 V (typ.)
- Pushbutton "RESET" pressed
- Watchdog time-out
- IPM controller reset

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3.2.2 SMBus Devices

The aTCA-6250 provides a System Management Bus (SMBus) hosted by the Intel® C604 PCH. The topology is shown in the diagram below.



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3.2.3 GPIO List

The following table summarizes GPIO usage on the Intel® C604 PCH

Control / Status Signal	GPIO	DIR	Description
HOT SWAP LED	J22	Output	Blue Hot Swap LED Control
OOS_LED	C9	Output	LED1
BOOT _STATUS_LED	C16	Output	LED2
IPMC_PAYLOAD_PWR	H17	Output	LED3
RMII_TXDO0	AA5	Output	RMII transmit data 0
RMII_TXDO1	W5	Output	RMII transmit data 1
RMII_TX_ENO	Y4	Output	RMII transmit enable
SPI0_nSS	Y20	Output	SPI slave select
SPI0_DO	U17	Output	SPI data output
SPI0_SCK	W19	Output	SPI clock
IPMB BUS A ENABLE	C21	Output	IPMB Bus A Enable control
IPMB BUS B ENABLE	J20	Output	IPMB Bus B Enable control
HA7	F1	Input	Hardware Address Input 7
HA6	G3	Input	Hardware Address Input 6
HA5	F3	Input	Hardware Address Input 5
HA4	B9	Input	Hardware Address Input 4
HA3	B12	Input	Hardware Address Input 3
HA2	A5	Input	Hardware Address Input 2
HA1	D3	Input	Hardware Address Input 1
HA0	B17	Input	Hardware Address Input 0
HSWITCH	A8	Input	Handle Switch
SPI0_DI	V18	Input	SPI data input
ADC_PP_3V3	V9	Input	Payload voltage (3.3V)
ADC_PP_1V5	AA8	Input	Payload voltage (1.5V)
ADC_PP_5V	AB8	Input	Payload voltage (5V)
RMII_REF_CLK	T6	Input	RMII reference clock
RMII_CRS_DV	W4	Input	RMII carrier sense / receive data valid
RMII_RXD0	V5	Input	RMII receive data 0
RMII_RXD1	U5	Input	RMII receive data 1
SOL_SMB_nALERT	D12	Input	SOL SMBus ALERT
IPMB BUS A READY	A9	Input	IPMB Bus A Ready signal.
IPMB BUS B READY	B14	Input	IPMB Bus B Ready signal.
IPMB BUS A SCL	U21	InOut	IPMB Bus A Serial Data Line signal
IPMB BUS A SDA	V21	InOut	IPMB Bus A Serial Clock signal
IPMB BUS B SCL	U20	InOut	IPMB Bus B Serial Data Line signal
IPMB BUS B SDA	V22	InOut	IPMB Bus B Serial Clock signal
MO_SCL	V1	InOut	Master-onlyI2C Serial Clock signal
MO_SDA	R3	InOut	Master-onlyI2C Serial Clock signal
SOL_SMB_SCL	W1	InOut	SOL SMBus clock
SOL_SMB_SDA	Y1	InOut	SOL SMBus data

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3.3 I/O Interfaces

3.3.1 USB

The aTCA-6250 supports four USB 2.0 ports:

- Two Type-A ports on front panel
- Two ports routed to RTM

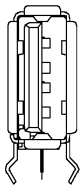
On the USB 2.0 front panel port, a USB cable up to 5 meters in length can be used.

On the USB 2.0 Rear I/O ports, it is strongly recommended to use a cable less than 3 meters in length for USB 2.0 devices.

The USB 2.0 ports are high-speed, full-speed, and low-speed capable. Hi-speed USB 2.0 allows data transfers of up to 480 Mb/s, 40 times faster than a full-speed USB (USB 1.1). One USB peripheral may be connected to each port.

With the aTCA-R6270 (RTM), the aTCA-6250 supports two additional USB ports on the I/O panel of the RTM.

USB Connector Pin Definition (Type A)



Pin	Signal
1	5V USB VCC
2	USB-
3	USB+
4	GND USB

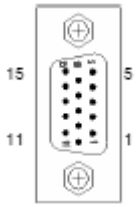
Note: The aTCA-6250 host interfaces can be used with a maximum 500mA continuous load current as specified in the Universal Serial Bus Specification, Revision 2.0. Short circuit protection is provided. All the signal lines are EMI filtered.

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3.3.2 VGA Interface

A DB-15 female connector on the front panel provides analog display output.

Front Panel VGA Pin Definition (DB-15)



Pin	Name	Pin	Name
1	RED	9	+5v
2	GREEN	10	GND
3	BLUE	11	NC
4	NC	12	DDC_DATA
5	GND	13	HSYNC
6	GND	14	VSYNC
7	GND	15	DDC_CLK
8	GND		

3.3.3 Ethernet Connection

The aTCA-6250 is equipped with one quad-port Intel® I350 AM4 Gigabit Ethernet Controller and one dual-port Intel® 82576EB Gigabit Ethernet Controller which provide six GbE ports in total. In default configuration, four ports from the Intel® I350 AM4 Gigabit Ethernet Controller are connected to the front panel RJ-45 ports. Two GbE ports from the Intel® 82576EB Gigabit Ethernet Controller are connected to Zone 2 Base Channels 1 and 2 (BCH1/BCH2).

The aDB-6100-A Fabric riser card is installed on the aTCA-6250 by default and provides support for different configurations of Fabric Channels 1 and 2. Equipped with an Intel® 82599EB Ethernet controller, the riser card provides two 10GbE links to Fabric Channels 1 and 2 (FCH1/FCH2).

With the aTCA-R6270 RTM installed, the aTCA-6250 supports dual 10GbE SFP+ ports from the Intel 82599ES Network Interface Controller connected to the PCIe x8 bus of CPU1.

Front Panel GbE Pin Definition (RJ-45)

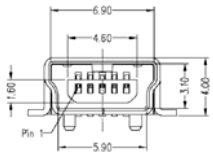
Pin	GbE Signal Names
1	Transmit Data1 +
2	Transmit Data1 -
3	Receive Data2 +
4	Receive Data3 +
5	Receive Data3 -
6	Receive Data2 +
7	Transmit Data4 +
8	Transmit Data4 -

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3.3.4 Serial Port

Two serial ports are output to USB Mini-B connectors on the front panel for use as service terminals . The port labeled IPMI is an "IPMC" debug port and the port labeled CPU" is connected to COM 1 of the Super IO chip.

Serial Port Pin Definition (USB Mini-B)

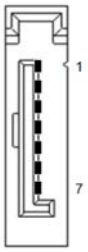


PIN	Signal Name	In/Out
1	Signal Ground	
2	Transmitted Data (TxD)	Out
3	Received Data (RxD)	In
4	Signal Ground	
5	Signal Ground	

3.3.5 Onboard SATA Interface

The aTCA-6250 has one 7-pin SATA connector reserved for onboard mounting of a Serial ATA disk on module (DOM). The SATA connector pin list is shown as below.

SATA Pin Definition (7-pin)



Pin	Signal Names
1	GND
2	SATA0_TX-P
3	SATA0_TX-N
4	GND
5	SATA0_RX-N
6	SATA0_RX-P
7	P5V

The aTCA-6250 is equipped wit han InnoDisk Serial ATA Disk on Module (16GB, available up to 32GB) which supports SATA 3.0Gb/s interface with sustained read to 130MB per second and sustained write reach up to 125MB per second.

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3.3.6 Switch And Jumper Settings

3.3.6.1 Set Blade Operation Mode

Use switch SW4 to set the Blade Operation Mode. Normal operation requires a shelf manager for the blade to boot. Standalone mode allows the blade to boot without a shelf manager.

SW4 Blade Operation	Pin 1	Pin 2	Pin 3	Pin 4
Normal Mode (default)	OFF	OFF	OFF	OFF
Standalone Mode	OFF	OFF	ON	OFF

3.3.6.2 IPMC JTAG Signal

The switch SW12 is designed for hardware debug purposes. Do not change the default settings. Doing may result in an abnormal boot, failure to boot, and or damage to the board.

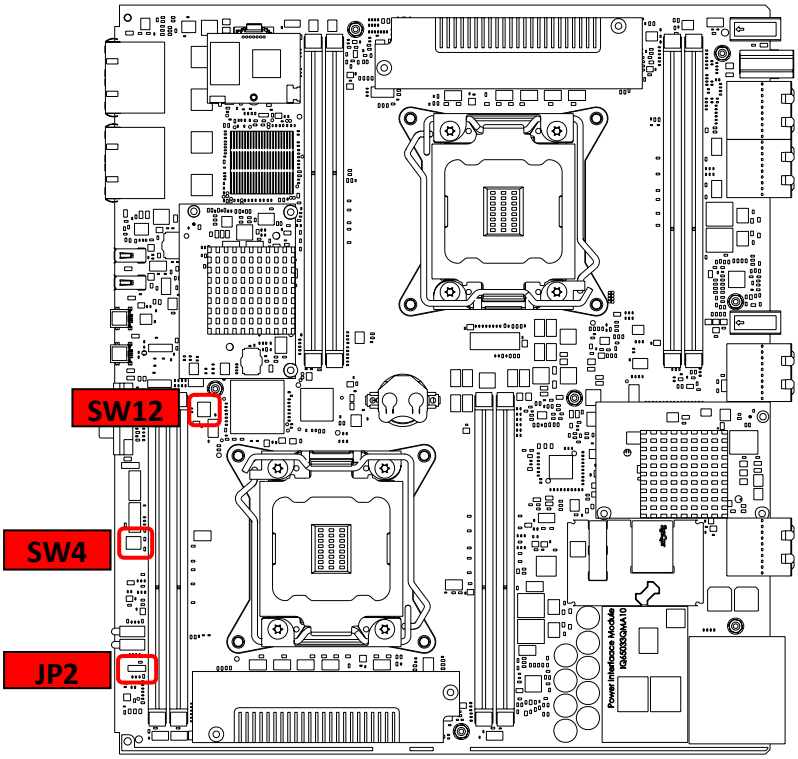
SW12 IPMC JTAG	Pin 1	Pin 2	Pin 3	Pin 4
Default Setting	OFF	ON	ON	ON

3.3.6.3 Shelf/Logic Ground Jumper

Use JP2 to short Shelf Ground to Logic Ground.

Shelf/Logic GND	JP2 Setting
Shorted	1-2
Open (default)	2-3

The locations of SW4, SW12 and JP2 are shown below:



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4 Intelligent Platform Management System

The purpose of the intelligent platform management system is to monitor, control, and assure proper operation of AdvancedTCA® Boards and other Shelf components. The intelligent platform management system watches over the basic health of the system, reports anomalies, and takes corrective action when needed. The intelligent platform management system can retrieve inventory information and sensor readings as well as receive event reports and failure notifications from Boards and other Intelligent FRUs. The intelligent platform management system can also perform basic recovery operations such as reset of managed entities.

The IPMC controller on aTCA-6250 supports an “intelligent” hardware management system, based on the Intelligent Platform Management Interface Specification. The intelligent management system provides the ability to manage the power, cooling, and interconnect needs of intelligent devices; to monitor events; and to log events to a central repository.

4.1 IPMI Sensors

The following table lists all the sensors supported by the aTCA-6250.

Item	Sensor Name	Sensor Address	Description
(1)	Hot Swap	(0x0)	FRU Hotswap Sensor.
(2)	RTM Hot Swap	(0x1)	RTM Hotswap Sensor.
(3)	Version change	(0x2)	Version Change Sensor.
(4)	IPMB Physical	(0x3)	Physical IPMB Sensor.
(5)	BMC Watchdog	(0x4)	Watchdog Timer Sensor.
(6)	LM73 Temp PCH	(0x5)	Temperature Sensor. Upper Non-Recoverable Threshold = 95 degrees C Upper Critical Threshold = 75 degrees C Upper Non-Critical Threshold = 60 degrees C Lower Non-Critical Threshold = 0 degrees C Lower Critical Threshold = -5 degrees C Lower Non-Recoverable Threshold = -10 degrees C
(7)	LM73 Temp PSU1	(0x6)	Temperature Sensor. Upper Non-Recoverable Threshold = 95 degrees C Upper Critical Threshold = 75 degrees C Upper Non-Critical Threshold = 60 degrees C Lower Non-Critical Threshold = 0 degrees C Lower Critical Threshold = -5 degrees C Lower Non-Recoverable Threshold = -10 degrees C
(8)	LM73 Temp I350 AM4	(0x7)	Temperature Sensor. Upper Non-Recoverable Threshold = 95 degrees C Upper Critical Threshold = 75 degrees C Upper Non-Critical Threshold = 60 degrees C Lower Non-Critical Threshold = 0 degrees C

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			Lower Critical Threshold = -5 degrees C Lower Non-Recoverable Threshold = -10 degrees C
(9)	LM73 TEMP CPU1_1	(0x8)	Temperature Sensor. Upper Non-Recoverable Threshold = 95 degrees C Upper Critical Threshold = 75 degrees C Upper Non-Critical Threshold = 60 degrees C Lower Non-Critical Threshold = 0 degrees C Lower Critical Threshold = -5 degrees C Lower Non-Recoverable Threshold = -10 degrees C
(10)	LM73 TEMP CPU1_2	(0x9)	Temperature Sensor. Upper Non-Recoverable Threshold = 95 degrees C Upper Critical Threshold = 75 degrees C Upper Non-Critical Threshold = 60 degrees C Lower Non-Critical Threshold = 0 degrees C Lower Critical Threshold = -5 degrees C Lower Non-Recoverable Threshold = -10 degrees C
(11)	LM73 TEMP CPU1_3	(0xA)	Temperature Sensor. Upper Non-Recoverable Threshold = 95 degrees C Upper Critical Threshold = 75 degrees C Upper Non-Critical Threshold = 60 degrees C Lower Non-Critical Threshold = 0 degrees C Lower Critical Threshold = -5 degrees C Lower Non-Recoverable Threshold = -10 degrees C
(12)	LM73 TEMP CPU2_1	(0xB)	Temperature Sensor. Upper Non-Recoverable Threshold = 95 degrees C Upper Critical Threshold = 75 degrees C Upper Non-Critical Threshold = 60 degrees C Lower Non-Critical Threshold = 0 degrees C Lower Critical Threshold = -5 degrees C Lower Non-Recoverable Threshold = -10 degrees C
(13)	LM73 TEMP CPU2_2	(0xC)	Temperature Sensor. Upper Non-Recoverable Threshold = 95 degrees C Upper Critical Threshold = 75 degrees C Upper Non-Critical Threshold = 60 degrees C Lower Non-Critical Threshold = 0 degrees C BIOS Lower Critical Threshold = -5 degrees C Lower Non-Recoverable Threshold = -10 degrees C
(14)	LM73 TEMP CPU2_3	(0xD)	Temperature Sensor. Upper Non-Recoverable Threshold = 95 degrees C Upper Critical Threshold = 75 degrees C Upper Non-Critical Threshold = 60 degrees C Lower Non-Critical Threshold = 0 degrees C Lower Critical Threshold = -5 degrees C Lower Non-Recoverable Threshold = -10 degrees C
(15)	PVTT_CPU1	(0xE)	Voltage Sensor. Upper Non-Recoverable Threshold = 1.137 Volts Upper Critical Threshold = 1.117 Volts Upper Non-Critical Threshold = 1.095 Volts Lower Non-Critical Threshold = 1.005 Volts Lower Critical Threshold = 0.984 Volts Lower Non-Recoverable Threshold = 0.871 Volts
(16)	P0V75_DDR_VTT1	(0xF)	Voltage Sensor. Upper Non-Recoverable Threshold = 0.825 Volts Upper Critical Threshold = 0.81 Volts Upper Non-Critical Threshold = 0.795 Volts Lower Non-Critical Threshold = 0.705 Volts

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			Lower Critical Threshold = 0.69 Volts Lower Non-Recoverable Threshold = 0.675 Volts
(17)	P_VCCP1	(0x10)	Voltage Sensor. Upper Non-Recoverable Threshold = 1.385 Volts Upper Critical Threshold = 1.365 Volts Upper Non-Critical Threshold = 1.35 Volts Lower Non-Critical Threshold = 0.6 Volts Lower Critical Threshold = 0.58 Volts Lower Non-Recoverable Threshold = 0.56 Volts
(18)	PVSA_CPU1	(0x11)	Voltage Sensor. Upper Non-Recoverable Threshold = 1.232 Volts Upper Critical Threshold = 1.215 Volts Upper Non-Critical Threshold = 1.2 Volts Lower Non-Critical Threshold = 0.6 Volts Lower Critical Threshold = 0.582 Volts Lower Non-Recoverable Threshold = 0.565 Volts
(19)	PVTT_CPU2	(0x12)	Voltage Sensor. Upper Non-Recoverable Threshold = 1.137 Volts Upper Critical Threshold = 1.117 Volts Upper Non-Critical Threshold = 1.095 Volts Lower Non-Critical Threshold = 1.005 Volts Lower Critical Threshold = 0.984 Volts Lower Non-Recoverable Threshold = 0.871 Volts
(20)	P0V75_DDR_VTT2	(0x13)	Voltage Sensor. Upper Non-Recoverable Threshold = 0.825 Volts Upper Critical Threshold = 0.81 Volts Upper Non-Critical Threshold = 0.795 Volts Lower Non-Critical Threshold = 0.705 Volts Lower Critical Threshold = 0.69 Volts Lower Non-Recoverable Threshold = 0.675 Volts
(21)	P_VCCP2	(0x14)	Voltage Sensor. Upper Non-Recoverable Threshold = 1.385 Volts Upper Critical Threshold = 1.365 Volts Upper Non-Critical Threshold = 1.35 Volts Lower Non-Critical Threshold = 0.6 Volts Lower Critical Threshold = 0.58 Volts Lower Non-Recoverable Threshold = 0.56 Volts
(22)	PVSA_CPU2	(0x15)	Voltage Sensor. Upper Non-Recoverable Threshold = 1.232 Volts Upper Critical Threshold = 1.215 Volts Upper Non-Critical Threshold = 1.2 Volts Lower Non-Critical Threshold = 0.6 Volts Lower Critical Threshold = 0.582 Volts Lower Non-Recoverable Threshold = 0.565 Volts
(23)	P1V1_SSB	(0x16)	Voltage Sensor. Upper Non-Recoverable Threshold = 1.21 Volts Upper Critical Threshold = 1.188 Volts Upper Non-Critical Threshold = 1.166 Volts Lower Non-Critical Threshold = 1.034 Volts Lower Critical Threshold = 1.012 Volts Lower Non-Recoverable Threshold = 0.99 Volts
(24)	P1V5_SSB	(0x17)	Voltage Sensor. Upper Non-Recoverable Threshold = 1.65 Volts Upper Critical Threshold = 1.62 Volts Upper Non-Critical Threshold = 1.59 Volts Lower Non-Critical Threshold = 1.296 Volts Lower Critical Threshold = 1.242 Volts

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			Lower Non-Recoverable Threshold = 1.215 Volts
(25)	P1V8_LAN_82576	(0x18)	Voltage Sensor. Upper Non-Recoverable Threshold = 1.98 Volts Upper Critical Threshold = 1.944 Volts Upper Non-Critical Threshold = 1.908 Volts Lower Non-Critical Threshold = 1.692 Volts Lower Critical Threshold = 1.656 Volts Lower Non-Recoverable Threshold = 1.62 Volts
(26)	P1V8_LAN_I350 AM4	(0x19)	Voltage Sensor. Upper Non-Recoverable Threshold = 1.98 Volts Upper Critical Threshold = 1.944 Volts Upper Non-Critical Threshold = 1.908 Volts Lower Non-Critical Threshold = 1.692 Volts Lower Critical Threshold = 1.656 Volts Lower Non-Recoverable Threshold = 1.62 Volts
(27)	P1V_LAN_82576	(0x1A)	Voltage Sensor. Upper Non-Recoverable Threshold = 1.1 Volts Upper Critical Threshold = 1.08 Volts Upper Non-Critical Threshold = 1.06 Volts Lower Non-Critical Threshold = 0.94 Volts Lower Critical Threshold = 0.92 Volts Lower Non-Recoverable Threshold = 0.9 Volts
(28)	P1V_LAN_I350 AM4	(0x1B)	Voltage Sensor. Upper Non-Recoverable Threshold = 1.1 Volts Upper Critical Threshold = 1.08 Volts Upper Non-Critical Threshold = 1.06 Volts Lower Non-Critical Threshold = 0.94 Volts Lower Critical Threshold = 0.92 Volts Lower Non-Recoverable Threshold = 0.9 Volts
(29)	CPU1 Temp(PECI)	(0x1C)	CPU Temperature. Upper Non-Recoverable Threshold = 95 degrees C Upper Critical Threshold = 75 degrees C Upper Non-Critical Threshold = 60 degrees C Lower Non-Critical Threshold = 0 degrees C Lower Critical Threshold = -5 degrees C Lower Non-Recoverable Threshold = -10 degrees C
(30)	CPU2 Temp(PECI)	(0x1D)	CPU Temperature. Upper Non-Recoverable Threshold = 95 degrees C Upper Critical Threshold = 75 degrees C Upper Non-Critical Threshold = 60 degrees C Lower Non-Critical Threshold = 0 degrees C Lower Critical Threshold = -5 degrees C Lower Non-Recoverable Threshold = -10 degrees C
(31)	System FW PROG	(0x1E)	System Firmware Progress Sensor.
(32)	48V_A Power(V)	(0x1F)	48V Voltage Sensor. Upper Non-Recoverable Threshold = 55 Volts Upper Critical Threshold = 50 Volts Upper Non-Critical Threshold = 49 Volts Lower Non-Critical Threshold = 36 Volts Lower Critical Threshold = 35 Volts Lower Non-Recoverable Threshold = 33 Volts
(33)	48V_B Power(V)	(0X20)	48V Voltage Sensor. Upper Non-Recoverable Threshold = 55 Volts Upper Critical Threshold = 50 Volts Upper Non-Critical Threshold = 49 Volts Lower Non-Critical Threshold = 36 Volts

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			Lower Critical Threshold = 35 Volts Lower Non-Recoverable Threshold = 33 Volts
(34)	+1.5V DDR-CPU1	(0x21)	Voltage Sensor. Upper Non-Recoverable Threshold = 1.65 Volts Upper Critical Threshold = 1.62 Volts Upper Non-Critical Threshold = 1.59 Volts Lower Non-Critical Threshold = 1.296 Volts Lower Critical Threshold = 1.242 Volts Lower Non-Recoverable Threshold = 1.215 Volts
(35)	+1.8V CPU1	(0x22)	Voltage Sensor. Upper Non-Recoverable Threshold = 1.98 Volts Upper Critical Threshold = 1.944 Volts Upper Non-Critical Threshold = 1.908 Volts Lower Non-Critical Threshold = 1.692 Volts Lower Critical Threshold = 1.656 Volts Lower Non-Recoverable Threshold = 1.62 Volts
(36)	+1.5V DDR-CPU2	(0x23)	Voltage Sensor. Upper Non-Recoverable Threshold = 1.65 Volts Upper Critical Threshold = 1.62 Volts Upper Non-Critical Threshold = 1.59 Volts Lower Non-Critical Threshold = 1.296 Volts Lower Critical Threshold = 1.242 Volts Lower Non-Recoverable Threshold = 1.215 Volts
(37)	+1.8V CPU2	(0x24)	Voltage Sensor. Upper Non-Recoverable Threshold = 1.98 Volts Upper Critical Threshold = 1.944 Volts Upper Non-Critical Threshold = 1.908 Volts Lower Non-Critical Threshold = 1.692 Volts Lower Critical Threshold = 1.656 Volts Lower Non-Recoverable Threshold = 1.62 Volts
(38)	+5.0V	(0x25)	Voltage Sensor. Upper Non-Recoverable Threshold = 5.5 Volts Upper Critical Threshold = 5.4 Volts Upper Non-Critical Threshold = 5.3 Volts Lower Non-Critical Threshold = 4.7 Volts Lower Critical Threshold = 4.6 Volts Lower Non-Recoverable Threshold = 4.5 Volts
(39)	+3.3V	(0x26)	Voltage Sensor. Upper Non-Recoverable Threshold = 3.63 Volts Upper Critical Threshold = 3.564 Volts Upper Non-Critical Threshold = 3.498 Volts Lower Non-Critical Threshold = 3.102 Volts Lower Critical Threshold = 3.036 Volts Lower Non-Recoverable Threshold = 2.97 Volts
(40)	+12V	(0x27)	Voltage Sensor. Upper Non-Recoverable Threshold = 13.2 Volts Upper Critical Threshold = 12.96 Volts Upper Non-Critical Threshold = 12.72 Volts Lower Non-Critical Threshold = 11.28 Volts Lower Critical Threshold = 11.04 Volts Lower Non-Recoverable Threshold = 10.8 Volts

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4.1.1 Sensor Reading (FRU Hotswap Sensor)

	Byte	Data field
Request data	1	Sensor Number (FFh = reserved)
Response data	1	Completion Code
	2	Sensor Reading. [7:0] - Not used. Write as 00h.
	3	Standard IPMI byte (See “Get Sensor Reading” in IPMI specification): [7] - 0b = All Event Messages disabled from this sensor [6] - 0b = sensor scanning disabled [5] - 1b = initial update in progress. This bit is set to indicate that a “Re-arm Sensor Events” or “Set Event Receiver” command has been used to request an update of the sensor status, and that update has not occurred yet. Software should use this bit to avoid getting an incorrect status while the first sensor update is in progress. This bit is only required if it is possible for the IPM Controller to receive and process a “Get Sensor Reading or Get Sensor Event Status” command for the sensor before the update has completed. This is most likely to be the case for sensors, such as fan RPM sensors, that may require seconds to accumulate the first reading after a re-arm. [4:0] – reserved. Ignore on read.
	4	Current State Mask [7] – 1b = FRU Operational State M7 - Communication Lost [6] – 1b = FRU Operational State M6 - FRU Deactivation In Progress [5] – 1b = FRU Operational State M5 - FRU Deactivation Request [4] – 1b = FRU Operational State M4 - FRU Active [3] – 1b = FRU Operational State M3 - FRU Activation in Progress [2] – 1b = FRU Operational State M2 - FRU Activation Request [1] – 1b = FRU Operational State M1 - FRU Inactive [0] – 1b = FRU Operational State M0 - FRU Not Installed
	(5)	[7:0] – Optional/Reserved. If provided, write as 80h (IPMI restriction). Ignore on read.

4.1.2 Get Sensor Reading (Physical IPMB-0 Sensor)

	Byte	Data field
Request data	1	Sensor Number (FFh = reserved)
Response data	1	Completion Code
	2	[7] – IPMB B Override State 0b = Override state, bus isolated 1b = Local Control state - IPM Controller determines state of bus. [6:4] = IPMB B Local Status 0h = No Failure. Bus enabled if no override in effect. 1h = Unable to drive clock HI 2h = Unable to drive data HI 3h = Unable to drive clock LO 4h = Unable to drive data LO 5h = Clock low timeout 6h = Under test (the IPM Controller is attempting to determine if it is causing a bus hang). 7h = Undiagnosed Communications Failure [3] – IPMB A Override State 0b = Override state, bus isolated 1b = Local Control state - IPM Controller determines state of bus. [2:0] = IPMB A Local Status

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		0h = No failure. Bus enabled if no override in effect. 1h = Unable to drive clock HI 2h = Unable to drive data HI 3h = Unable to drive clock LO 4h = Unable to drive data LO 5h = Clock low timeout 6h = Under test (the IPM Controller is attempting to determine if it is causing a bus hang). 7h = Undiagnosed Communications Failure
	3	Standard IPMI byte (see “Get Sensor Reading” in IPMI specification) [7] – 0b = All Event Messages disabled from this sensor [6] – 0b = Sensor scanning disabled [5] – 1b = Initial update in progress. This bit is set to indicate that a “Re-arm Sensor Events” or “Set Event Receiver” command has been used to request an update of the sensor status, and that update has not occurred yet. Software should use this bit to avoid getting an incorrect status while the first sensor update is in progress. This bit is only required if it is possible for the controller to receive and process a “Get Sensor Reading” or “Get Sensor Event Status” command for the sensor before the update has completed. This is most likely to be the case for sensors, such as fan RPM sensors, that may require seconds to accumulate the first reading after a re-arm. [4:0] – Reserved. Ignore on read.
	4	[7:4] – Reserved. Write as 0h, ignore on read [3] 1b = IPMB A enabled, IPMB-B enabled [2] 1b = IPMB A disabled, IPMB-B enabled [1] 1b = IPMB-A enabled, IPMB-B disabled [0] 1b = IPMB A disabled, IPMB-B disabled
	(5)	[7:0] – Optional/Reserved. If provided, write as 80h (IPMI restriction). Ignore on read.

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4.1.3 Watchdog Timer Sensor

Sensor Type	Sensor Type Code	Sensor Specific Offset	Event
Watchdog 2	23h		This sensor is recommended for new IPMI v1.0 and later implementations.
		00h	Timer expired, status only (no action, no interrupt)
		01h	Hard Reset
		02h	Power Down
		03h	Power Cycle
		04h-07h	reserved
		08h	Timer interrupt
			The Event Data 2 field for this command can be used to provide an event extension code, with the following definition: 7:4 interrupt type 0h = none 1h = SMI 2h = NMI 3h = Messaging Interrupt Fh = unspecified all other = reserved 3:0 timer use at expiration: 0h = reserved 1h = BIOS FRB2 2h = BIOS/POST 3h = OS Load 4h = SMS/OS 5h = OEM Fh = unspecified all other = reserved

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4.1.4 Version Change Sensor

Sensor Type	Sensor Type Code	Sensor Specific Offset	Event
Version Change	2Bh	00h	00h Intelligent change detected with associated Entity. Informational. This offset does not imply whether the intelligent change was successful or not. Only that a change occurred.
		01h	01h Firmware or software change detected with associated Entity.Informational. Success or failure not implied.
		02h	02h Intelligent incompatibility detected with associated Entity.
		03h	03h Firmware or software incompatibility detected with associated Entity.
		04h	04h Entity is of an invalid or unsupported intelligent version.
		05h	05h Entity contains an invalid or unsupported firmware or software version.
		06h	06h Intelligent Change detected with associated Entity was successful. (deassertion event means unsuccessful').
		07h	07h Software or F/W Change detected with associated Entity was successful. (deassertion event means 'unsuccessful') *Event data 2 can be used for additional event information on the type of version change, with the following definition:* Event Data 2 7:0 Version change type 00h unspecified 01h management controller device ID (change in one or more fields from 'Get Device ID') 02h management controller firmware revision 03h management controller device revision 04h management controller manufacturer ID 05h management controller IPMI version 06h management controller auxiliary firmware ID 07h management controller firmware boot block 08h other management controller firmware 09h system firmware (EFI / BIOS) change 0Ah SMBIOS change 0Bh operating system change 0Ch operating system loader change 0Dh service or diagnostic partition change 0Eh management software agent change 0Fh management software application change 10h management software middleware change 11h programmable intelligent change (e.g. FPGA) 12h board/FRU module change (change of a module plugged into associated entity) 13h board/FRU component change (addition or removal of a replaceable component on the board/FRU that is not tracked as a FRU) 14h board/FRU replaced with equivalent version 15h board/FRU replaced with newer version 16h board/FRU replaced with older version 17h board/FRU intelligent configuration change (e.g. strap, jumper, cable change, etc.)

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4.1.5 System Firmware Progress Sensor

Sensor Type	Sensor Type Code	Sensor Specific Offset	Event
System Firmware Progress (formerly POST Error)	0Fh	00h	System Firmware Error (POST Error) The Event Data 2 field can be used to provide an event extension code, with the following definition: Event Data 2 00h Unspecified. 01h No system memory is physically installed in the system. 02h No usable system memory, all installed memory has experienced an unrecoverable failure. 03h Unrecoverable hard-disk/ATAPI/IDE device failure. 04h Unrecoverable system-board failure. 05h Unrecoverable diskette subsystem failure. 06h Unrecoverable hard-disk controller failure. 07h Unrecoverable PS/2 or USB keyboard failure. 08h Removable boot media not found 09h Unrecoverable video controller failure 0Ah No video device detected 0Bh Firmware (BIOS) ROM corruption detected 0Ch CPU voltage mismatch (processors that share same supply have mismatched voltage requirements) 0Dh CPU speed matching failure 0Eh to FFh reserved System Firmware Hang (uses same Event Data 2 definition as following System Firmware Progress offset) System Firmware Progress The Event Data 2 field can be used to provide an event extension code, with the following definition: Event Data 2 00h Unspecified.
		01h	01h Memory initialization. 02h Hard-disk initialization 03h Secondary processor(s) initialization 04h User authentication 05h User-initiated system setup
		02h	06h USB resource configuration 07h PCI resource configuration 08h Option ROM initialization 09h Video initialization 0Ah Cache initialization 0Bh SM Bus initialization 0Ch Keyboard controller initialization 0Dh Embedded controller/management controller initialization 0Eh Docking station attachment 0Fh Enabling docking station 10h Docking station ejection 11h Disabling docking station 12h Calling operating system wake-up vector

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			13h Starting operating system boot process, e.g. calling Int 19h 14h Baseboard or motherboard initialization 15h reserved 16h Floppy initialization 17h Keyboard test 18h Pointing device test 19h Primary processor initialization 1Ah to FFh reserved

4.1.6 Get Sensor Reading Command

	Byte	Data field
Request data	1	Sensor Number (FFh = reserved)
Response data	1	Completion Code
	2	Sensor reading Byte 1: byte of reading. Ignore on read if sensor does not return an numeric (analog) reading.
	3	[7] - 0b = All Event Messages disabled from this sensor [6] - 0b = sensor scanning disabled [5] - 1b = reading/state unavailable (formerly “initial update in progress”). This bit is set to indicate that a ‘re-arm’ or ‘Set Event Receiver’ command has been used to request an update of the sensor status, and that update has not occurred yet. Software should use this bit to avoid getting an incorrect status while the first sensor update is in progress. This bit is only required if it is possible for the controller to receive and process a ‘Get Sensor Reading’ or ‘Get Sensor Event Status’ command for the sensor before the update has completed. This is most likely to be the case for sensors, such as fan RPM sensors, that may require seconds to accumulate the first reading after a re-arm. The bit is also used to indicate when a reading/state is unavailable because the management controller cannot obtain a valid reading or state for the monitored entity, typically because the entity is not present. For more in formation, please see *Section 16.4, Event Status, Even Conditions, and Present State* and *Section 16.6, Re-arming* on the PICMG specification 3.0. [4:0] - reserved. Ignore on read.
	4	For threshold-based sensors Present threshold comparison status [7:6] - reserved. Returned as 1b. Ignore on read. [5] - 1b = at or above (≥) upper non-recoverable threshold [4] - 1b = at or above (≥) upper critical threshold [3] - 1b = at or above (≥) upper non-critical threshold [2] - 1b = at or below (≤) lower non-recoverable threshold [1] - 1b = at or below (≤) lower critical threshold [0] - 1b = at or below (≤) lower non-critical threshold For discrete reading sensors [7] - 1b = state 7 asserted [6] - 1b = state 6 asserted [5] - 1b = state 5 asserted [4] - 1b = state 4 asserted [3] - 1b = state 3 asserted [2] - 1b = state 2 asserted [1] - 1b = state 1 asserted [0] - 1b = state 0 asserted

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	(5)	For discrete reading sensors only. (Optional) (00h Otherwise) [7] - reserved. Returned as 1b. Ignore on read. [6] - 1b = state 14 asserted [5] - 1b = state 13 asserted [4] - 1b = state 12 asserted [3] - 1b = state 11 asserted [2] - 1b = state 10 asserted [1] - 1b = state 9 asserted [0] - 1b = state 8 asserted

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4.2 IPMI Commands

The following table presents all the commands which are supported by the aTCA-6250 in different interfaces and compatible with IPMI v1.5 and PICMG 3.0 R2.0 ECN001.

There are two interfaces implemented with IPMI command support.
(1) KCS: OpenIpmi; (2) IPMB0: IPMBa & IPMBb

	KCS	IPMB0
IPMI Command		
IPM Device "Global" Commands		
Get Device ID	●	●
Cold Reset	●	●
Warm Reset	●	●
Get Self Test Results	●	●
Get Device GUID	●	●
IPMI Messaging Support Commands		
Set BMC Global Enables	●	●
Get BMC Global Enables	●	●
Clear Message Flags	●	●
Get Message Flags	●	●
Get Message	●	●
Send Message	●	●
Master Write-Read	●	●
BMC Watchdog Timer		
Reset Watchdog Timer	●	●
Set Watchdog Timer	●	●
Get Watchdog Timer	●	●
Chassis Device Commands		
Chassis Identify	●	●
Set System Boot Option	●	●
Get System Boot Option	●	●
Event Commands		
Set Event Receiver	●	●
Get Event Receiver	●	●
Platform Event	●	●
Sensor Device Commands		
Get Device SDR Info	●	●
Get Device SDR	●	●
Reserve Device SDR Repository	●	●
Get Sensor Reading Factors	●	●
Set Sensor Hysteresis	●	●
Get Sensor Hysteresis	●	●
Set Sensor Threshold	●	●
Get Sensor Threshold	●	●
Set Sensor Event Enable	●	●
Get Sensor Event Enable	●	●
Rearm Sensor Events	●	●
Get Sensor Event Status	●	●
Get Sensor Reading	●	●
FRU Device Commands		
Get FRU Inventory Area Info	●	●
Read FRU Data	●	●
Write FRU Data	●	●

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PICMG Command		
HPM.1 Upgrade Commands (HPM.1)		
Get target upgrade capabilities	●	●
Get component properties	●	●
Abort Firmware Upgrade	●	●
Initiate upgrade action	●	●
Upload firmware block	●	●
Finish firmware upload	●	●
Get upgrade status	●	●
Activate firmware	●	●
Query Self-test Results	●	●
Query Rollback status	●	●
Initiate Manual Rollback	●	●
AdvancedTCA		
Get PICMG Properties	●	●
Get Address Info	●	●
FRU Control	●	●
FRU Control Capabilities	●	●
Get FRU LED Properties	●	●
Get LED Color Capabilities	●	●
Set FRU LED State	●	●
Get FRU LED State	●	●
Set IPMB State		●
Set FRU Activation Policy	●	●
Get FRU Activation Policy	●	●
Set FRU Activation	●	●
Get Device Locator Record ID	●	●
Get Port State	●	●
Set Port State		●
Compute Power Properties		●
Set Power Level		●
Get Power Level	●	●
Bused Resource Control		●
Get IPMB Link Info	●	●
SET_CLOCK_STATE	●	●
GET_CLOCK_STATE	●	●
Get AMC-Port State		●
Set AMC-Port State		●

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5 Getting Started

The aTCA-6250 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

5.1 Safety Requirements

The following safety precautions must be observed when installing or operating the aTCA-6250. ADLINK assumes no responsibility for any damage resulting from failure to comply with these requirements.

Exercised due care when handling the board as the heat sink can get very hot. Do not touch the heat sink when installing or removing the board. The board should not be placed on any surface or in any form of storage container until the board and heat sink have cooled down to room temperature.

This ATCA blade contains electrostatic sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

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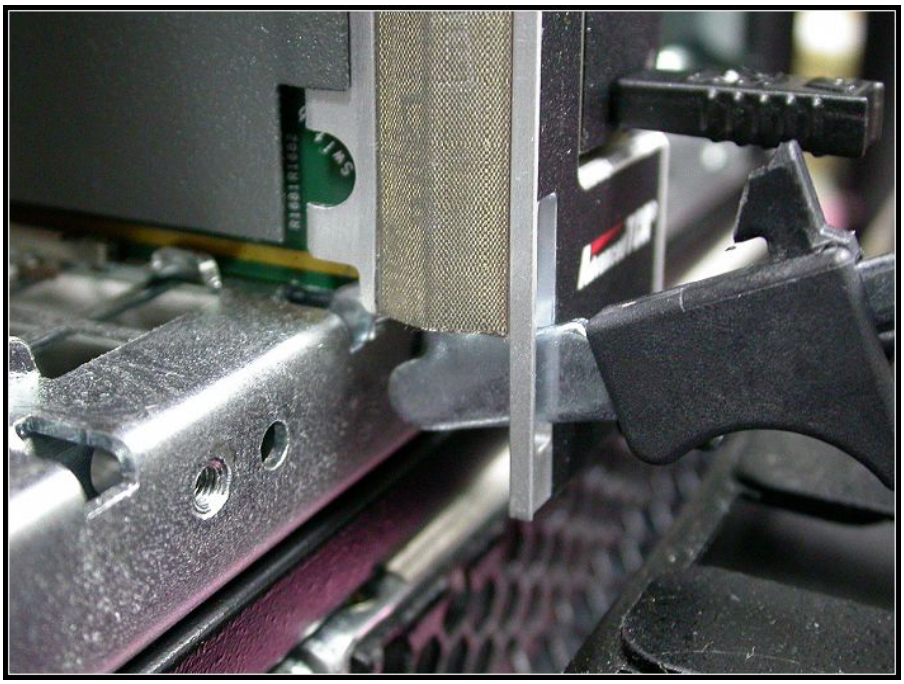
5.2 Installing and Removing the aTCA-6250

5.2.1 Installing the Blade

Follow these steps to install the aTCA-6250 blade to the chassis.

Step 1

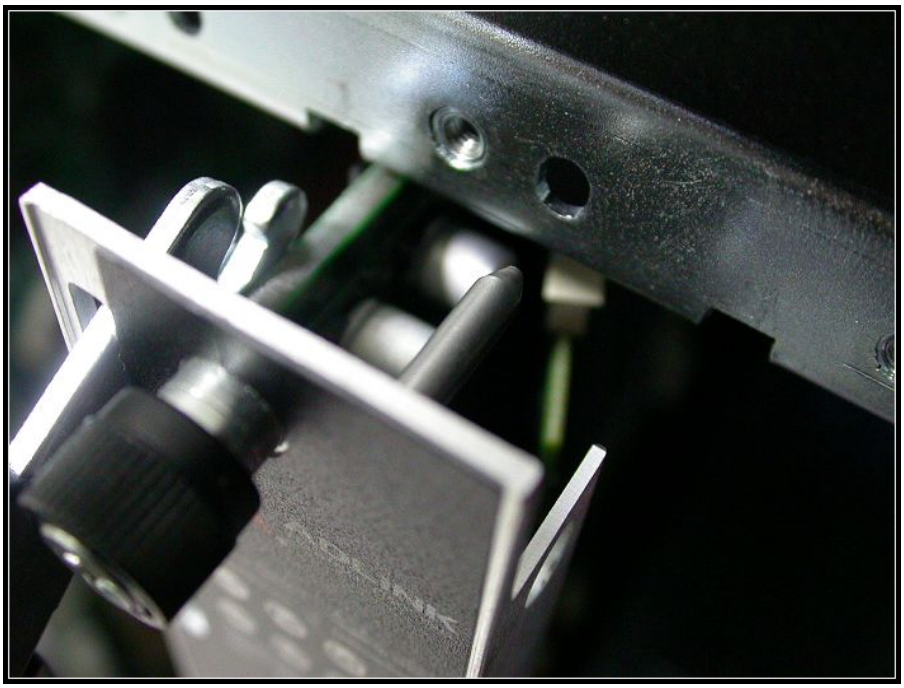
Carefully align the board edges with the chassis guide rails and push the blade inwards.



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Step 2

Check if the catch hooks and alignment pins at both ends of the module are correctly inserted into the proper openings. Push inwards on the handles until the blade is firmly seated in the chassis. (Do not force the handles if there is any abnormal resistance or it could damage the connectors and/or backplane.)





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Step 3

Push the ejector handles inwards until it is locked.





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Step 4

Lock both ends of the captive screws.



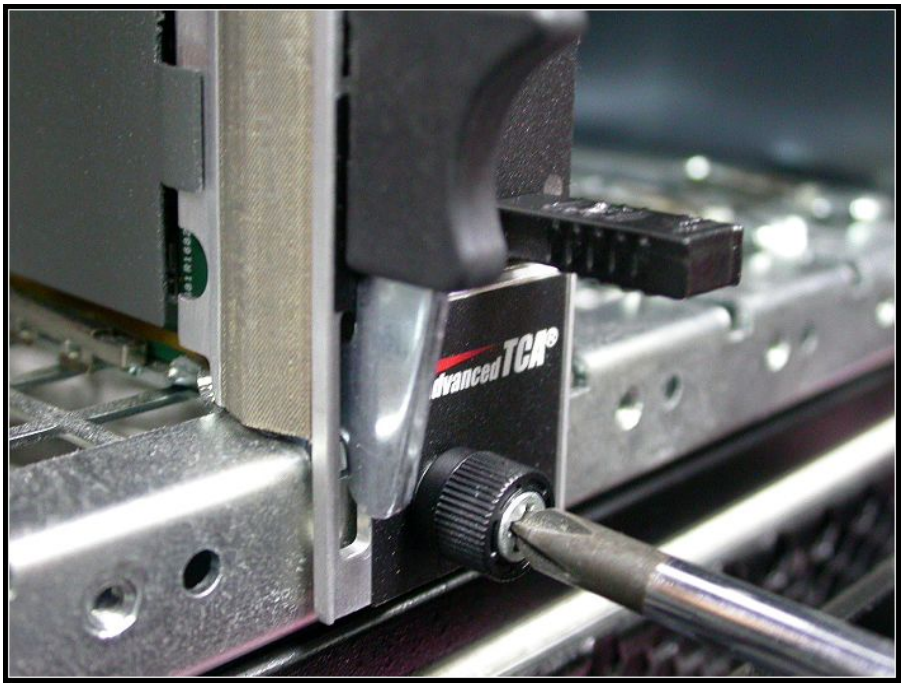
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5.2.2 Removing the Blade

Follow these steps to remove the aTCA-6250 blade from the chassis.

Step 1

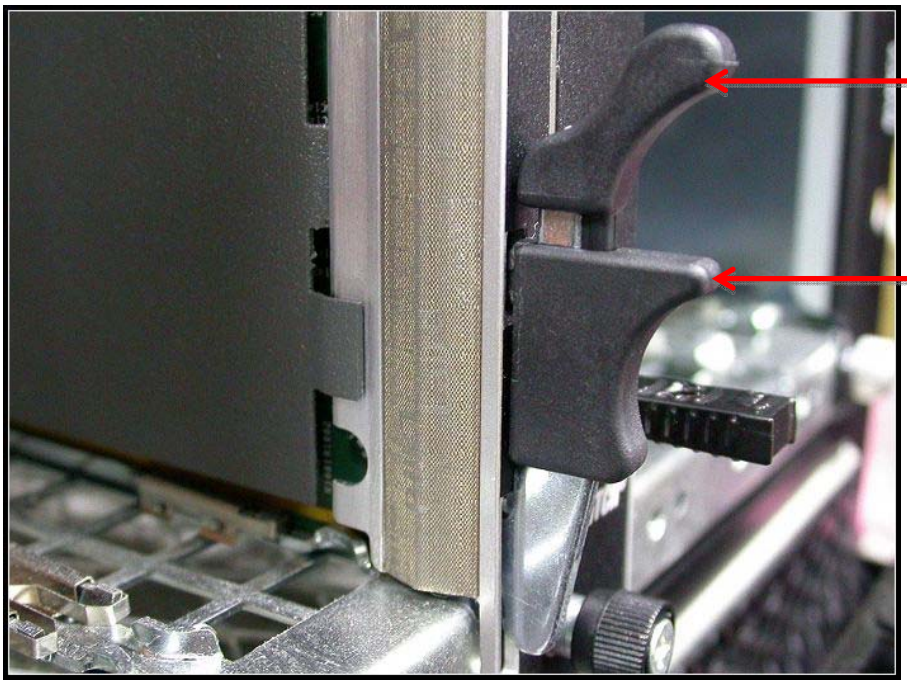
Unlock both ends of the captive screws.



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Step 2

Pinch the lever and latch together then pull outwards to release the ejector handles at both ends.

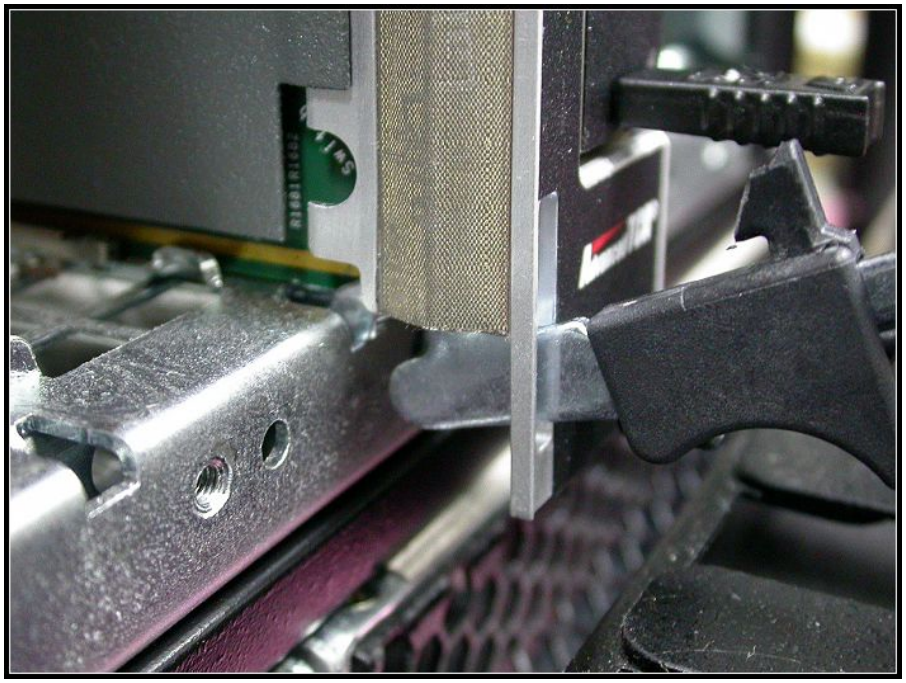




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Step 3

Pull the blade outwards from the chassis until it is removed.



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5.3 Firmware Update Procedure

The aTCA-6250 supports firmware update (IPMC FW, BIOS, FRU) over various interfaces (LAN, KCS, serial interface or IPMB). Please follow the procedures listed below to update the IPMC firmware.

Note: IPMB-0 will be disabled during the process of upgrading IPMC firmware. This is a limitation of the IPMC controller (SmartFusion A2F500)

5.3.1 Update Over Serial Interface

The following IPMItool command line parameters are used for communicating with the carrier IPMC via a serial interface:

- **-I serial-terminal**

This parameter instructs the IPMItool utility to use the serial interface for communications with the carrier IPMC.

- **-D <dev[:baudrate]>**

This parameter specifies the serial device and baud rate settings to use. For Linux hosts, the serial device is the system path to the device node (e.g. /dev/ttyS0).

Perform the following steps to update the IPMC firmware**:**

Step 1: Prepare an external host PC with Linux OS and connect it to the serial port on the aTCA-6250 via the COM port (USB Mini-B on the front panel). Put the IPMItool utility and new firmware image on the host PC. Enter the following command:

```
[root@localhost 6250_A2]# ./ipmitool -I serial-terminal -D /dev/
ttyS0:115200  hpm upgrade hpm1fw.img activate
```

Step 2: Enter “y” when prompted and wait until the string “firmware update procedure successful” is displayed.

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```
[root@localhost 6250_A2]# ./ipmitool -I serial-terminal -D /dev/
ttyS0:115200  hpm upgrade hpm1fw.img activate

PICMG HPM.1 Upgrade Agent 1.0:

Validating firmware image integrity...OK
Performing preparation stage...
    Services may be affected during upgrade. Do you wish to cont
inue? y/n y
OK
    Target Product ID     : 25168
    Target Manufacturer ID: 24339
Performing upgrade stage:
    Upgrading A2F-AMCc F/W
    with Version: Major: 1
                  Minor: 0
                  Aux  : 162 000 000 000
    Writing firmware: 100 % completed
Performing activation stage:

Firmware upgrade procedure successful
```

To update other images (BIOS, FRU, etc), just replace the target image and the file name while typing command.

Item	File name
IPMC firmware	hpm1fw.img
BIOS	hpm1bios.img

Note:
1. The hpm1bios.img always updates the backup BIOS image.
2. Make sure the payload power is off (M1 state) before updating the IPMC firmware

5.3.2 Update over KCS

Step1: Prepare an aTCA-6250 with Linux system. Enter the following command to make sure the ipmi_si and ipmi_devintf modules are loaded before the IPMItool utility can be used.

```
[root@localhost 6250_A2]# modprobe ipmi_si
[root@localhost 6250_A2]# modprobe ipmi_devintf
```

Step2: Put IPMItool and “target image” in the Linux system then enter the following command:

```
[root@localhost 6250_A2]# ./ipmitool hpm upgrade hpm1fw.img acti
vate
```


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Step3: Select “y” and wait until the string of “firmware update procedure successful” is displayed.

```
[root@localhost 6250_A2]# ./ipmitool hpm upgrade hpm1fw.img acti
vate

PICMG HPM.1 Upgrade Agent 1.0:

Validating firmware image integrity...OK
Performing preparation stage...
    Services may be affected during upgrade. Do you wish to cont
inue? y/n y
OK
    Target Product ID     : 25168
    Target Manufacturer ID: 24339
Performing upgrade stage:
    Upgrading A2F-AMCc F/W
    with Version: Major: 1
                  Minor: 0
                  Aux  : 162 000 000 000
    Writing firmware: 100 % completed
Performing activation stage:

Firmware upgrade procedure successful
```

To update other images (BIOS, FRU, etc), just replace the target image and the file name while typing command.

Item	File name
IPMC firmware	hpm1fw.img
BIOS	hpm1bios.img

5.3.3 Update over LAN

The following IPMItool command line parameters are used for communicating with the carrier IPMC via LAN:

- **-I lan**

The parameter instructs the IPMItool utility to use the RMCP protocol for communicating with the IPMC.

- **-H <IP address >**

The parameter specifies the IP address of the IPMC.

Please follow the step to update firmware**:**
Step1: Prepare an external x86 PC and connect the target aTCA-6250 via BASE Interface. Put IPMItool and “target image” on the x86 PC with Linux system. Enter the following command:

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```
[root@localhost 6250_A2]# ./ipmitool -I lan -H 172.17.172.134 -U
 "adlinkuser" -P "adlinkuser"  hpm upgrade hpm1fw.img activate
```

Step2: Select “y” and wait until the string of “firmware update procedure successful” is displayed.

```
[root@localhost 6250_A2]# ./ipmitool -I lan -H 172.17.172.134 -U
 "adlinkuser" -P "adlinkuser"  hpm upgrade hpm1fw.img activate

PICMG HPM.1 Upgrade Agent 1.0:

Validating firmware image integrity...OK
Performing preparation stage...
    Services may be affected during upgrade. Do you wish to cont
inue? y/n y
OK
    Target Product ID     : 25168
    Target Manufacturer ID: 24339
Performing upgrade stage:
    Upgrading A2F-AMCc F/W
    with Version: Major: 1
                  Minor: 0
                  Aux  : 162 000 000 000
    Writing firmware: 100 % completed
Performing activation stage:

Firmware upgrade procedure successful
```

To update other images (BIOS, FRU, etc), just replace the target image and the file name while typing command.

Item	File name
IPMC firmware	hpm1fw.img
BIOS	hpm1bios.img

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6 BIOS

This chapter will guide you how to configure BIOS setup items. There will be detailed description for each BIOS setup item in the following sections.

6.1 Entering the BIOS Setup Screen

To enter the setup screen, follow these steps:

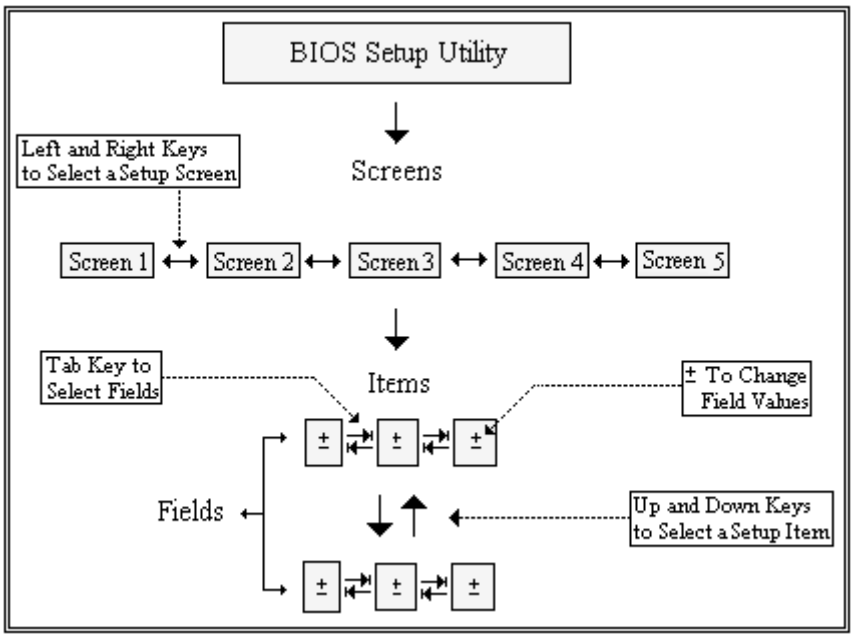
Step 1: Power on the aTCA-6250.
Step 2: Press the <S> key on a USB keyboard when you see the following text prompt on boot up screen.



Step 3: After you press the <S> key, the Main BIOS setup menu will be displayed. You can access the other setup screen from the BIOS setup utility, such as CPU configuration, USB configuration and so on.

6.1.1 Navigation

The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process. These keys include <F1>, <F2>, <F3>, <F4>, <ESC>, <Enter>, <Arrow> keys, and so on.



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NOTE:	There is a hot key legend located in the right frame on most setup screens..
→←	Left/Right. The *Left and Right* < Arrow > keys allow you to select a setup screen.
↑↓	Up/Down The *Up and Down* < Arrow > keys allow you to select a setup item or sub-screen.
+-	Plus/Minus the *Plus and Minus* < Arrow > keys allow you to change the field value of a particular setup item. For example: Date and Time.
ESC	The < Esc > key allows you to discard any changes you have made and exit the Setup. Press the < Esc > key to exit the setup without saving your changes. Press the < Enter > key to discard changes and exit. You can also use the < Arrow > key to select *Cancel* and then press the < Enter > key to abort this function and return to the previous screen.
Enter	The < Enter > key allows you to display or change the setup option listed for a particular setup item. The < Enter > key can also allow you to display the setup sub-screens.

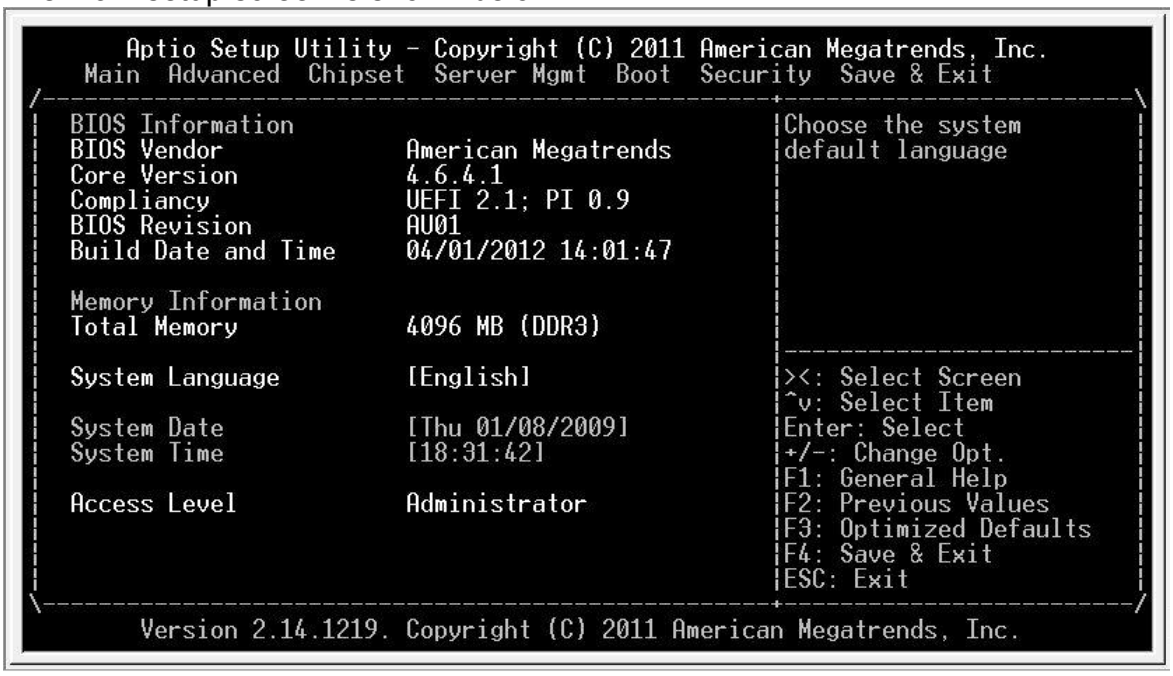
6.2 Main BIOS Setup Screen

The Main BIOS setup menu is the screen where you start navigation of the BIOS setting menus. You can always return to the Main setup screen by selecting the Main tab. Each BIOS setup menu option is described in the following sections.

There are two parts of the Main BIOS setup menu screen. The left part of the screen displays the available options. The user can configure the options in blue text. The selected option will appear highlighted in white text. Options in gray text are for information only

The upper right part of the screen displays the description of the selected option. The lower right part of the screen shows the navigation keys that user can use.

The Main setup screen is shown below.



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System Language

Choose the language of BIOS setup utility. So far, there is only “English” is supported on aTCA-6250.

System Time/System Date

Use these two options to change system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values using the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.



The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

System & Board Information

The Main BIOS setup screen reports memory and board information.

BIOS Vendor

It reports the BIOS vendor of aTCA-6250’s BIOS. American Megatrend, Inc. is the BIOS vendor that aTCA-6250 is using.

Core Version

It shows what core version is used from AMI to develop aTCA-6250’s BIOS.

Compliancy

It shows what version of EFI specification is compliant with aTCA-6250’s BIOS.

BIOS Revision

It shows revision of aTCA-6250’s BIOS.

Build Date and Time

It shows date and time that aTCA-6250 BIOS is released.

Total Memory

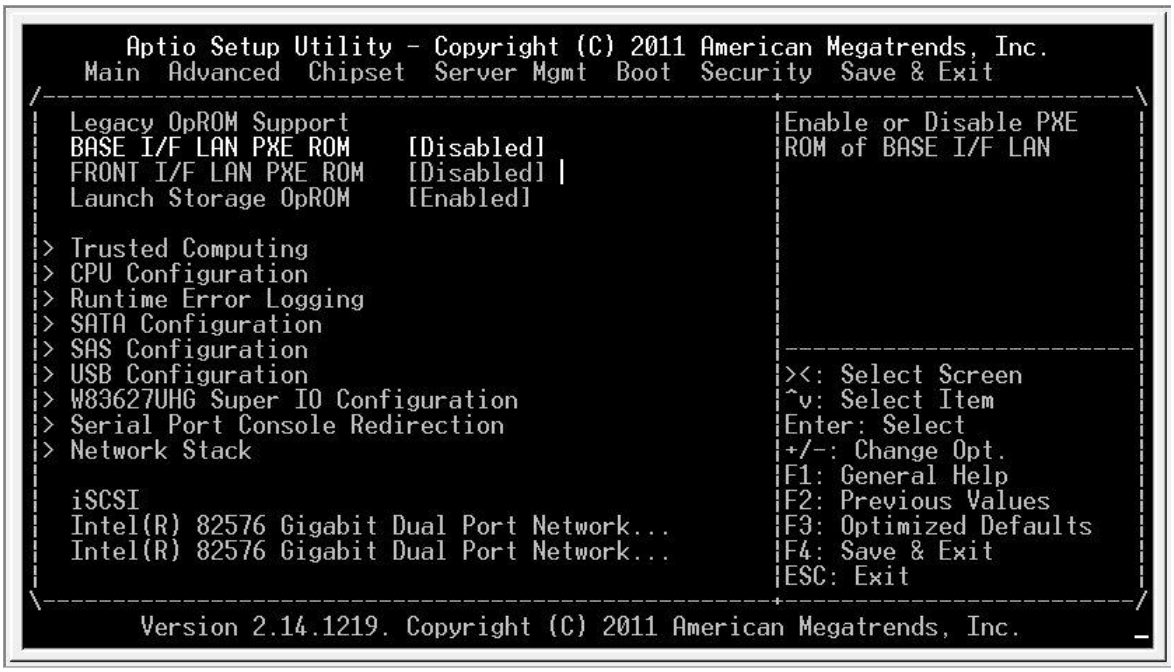
It shows the memory size on aTCA-6250.

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6.3 Advanced Setup Screen

Select the ***Advanced*** tab from the setup screen to enter ***Advanced*** BIOS setup screen. You can select any of items in the left frame of the screen, such as CPU configuration, to go to the sub menu for that item. You can select an ***Advanced*** BIOS sub menu or option by highlighting it using the <Arrow> keys. The Advanced BIOS setup screen is shown below.

The sub menus are described in the following sections.



BASE I/F LAN PXE ROM
FRONT I/F LAN PXE ROM

These two options can be configured to invoke Ethernet's PXE ROM on BASE/FRONT interface. When it is set to Disabled, system will boot without PXE ROM. Options: **Enabled/Disabled**.

Launch Storage OpROM

Boot option for legacy mass storage devices with option ROM. Options: **Enabled/Disabled**.

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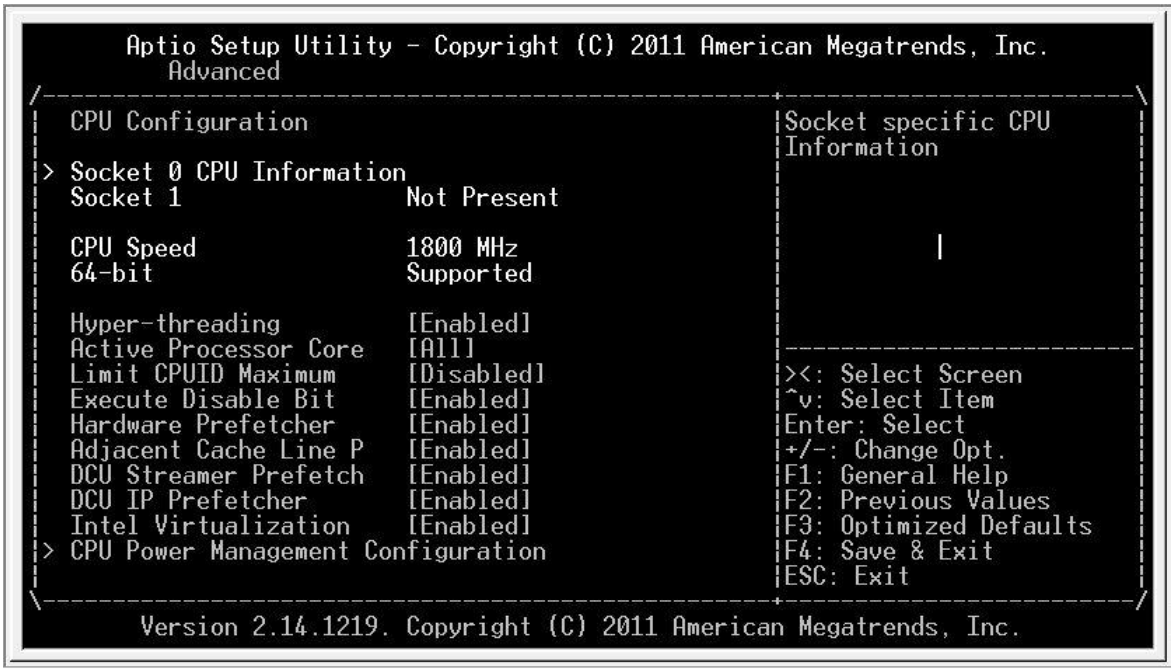
6.3.1 Trusted Computing

Trusted computing is an industry standard to make personal computers more secure through a dedicated hardware chip, called a Trusted Platform Module (TPM). This option allows enabling or disabling the TPM support.



6.3.2 CPU Configuration

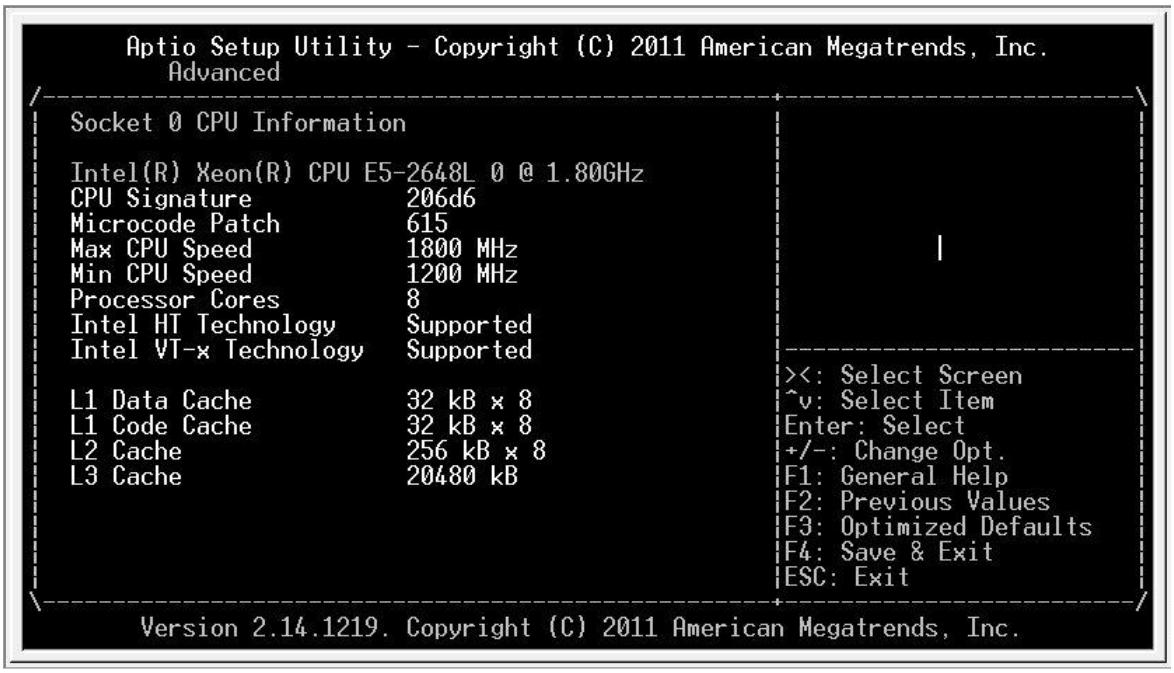
You can use this screen to select options for the CPU configuration settings. Use the up and down <Arrow> keys to select an item. Use the <+> and <-> keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the CPU configuration screen is shown below.



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Socket 0/1 CPU Information

BIOS will show the information of detected CPU, like CPU speed and its supported feature. Detailed information will also be listed in each socket CPU information sub menu like below. User can select “Socket 0” or “Socket 1” information for more detailed understanding of what CPU is using on system.



Hyper-threading

This item allows you to enable or disable the Hyper-Threading technology. Options: **Enabled/Disabled**.

Active Processor Core

This item allows you to select the number of cores to enable in each processor package. This BIOS setting is present only when a multi-core processor is installed.

Limit CPUID Maximum

When the computer is booted up, the operating system executes CPUID instruction to identify the processor and its capabilities. Before it can do so, it must first query the processor to find out the highest input value CPUID recognizes. This determines the kind of basic information CPUID can provide the operating system. This option allows you to circumvent problems with older operating systems that do not support Intel Pentium 4 processor with Hyper-Threading Technology.

When **Enabled**, the processor will limit the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When **Disabled**, the processor will return the actual maximum CPUID input value of the processor when queried. Options: **Enabled/Disabled**.

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Execute Disable Bit

Intel's Execute Disable Bit functionality can help prevent certain classes of malicious buffer overflow attacks when combined with a supporting operating system. Execute Disable Bit allows the processor to classify areas in memory by where application code can execute and where it cannot. When a malicious worm attempts to insert code in the buffer, the processor disables code execution and prevents damage and worm propagation.

Hardware Prefetcher

This is used for reducing the waiting time of DRAM. The hardware prefetcher looks for streams of data and tries to predict what data will be needed next by the processor and proactively tries to fetch these data. Options: **Enabled/Disabled**.

Adjacent Cache Line Prefetch

It is opened for choose the optimal use of sequential memory access for performance purpose. Disable this setting for the application that requires high use of random memory access. Options: **Enabled/Disabled**.

DCU Streamer Prefetch

There are two distinct hardware prefetchers on aTCA-6250. Data Cache Unit (DCU) streamer prefetcher and Data Cache Unit (DCU) IP-prefetcher. DCU streamer prefetchers detect multiple reads to a single cache line in a certain period of time and choose to load the following cache line to the L1 data caches.

This option allows user to enable or disable DCU streamer Prefetcher.

DCU IP Prefetcher

DCU IP Prefetcher looks for sequential load history to determine whether to prefetch the data to the L1 caches.

This option allows user to enable or disable DCU IP Prefetcher.

Intel Virtualization

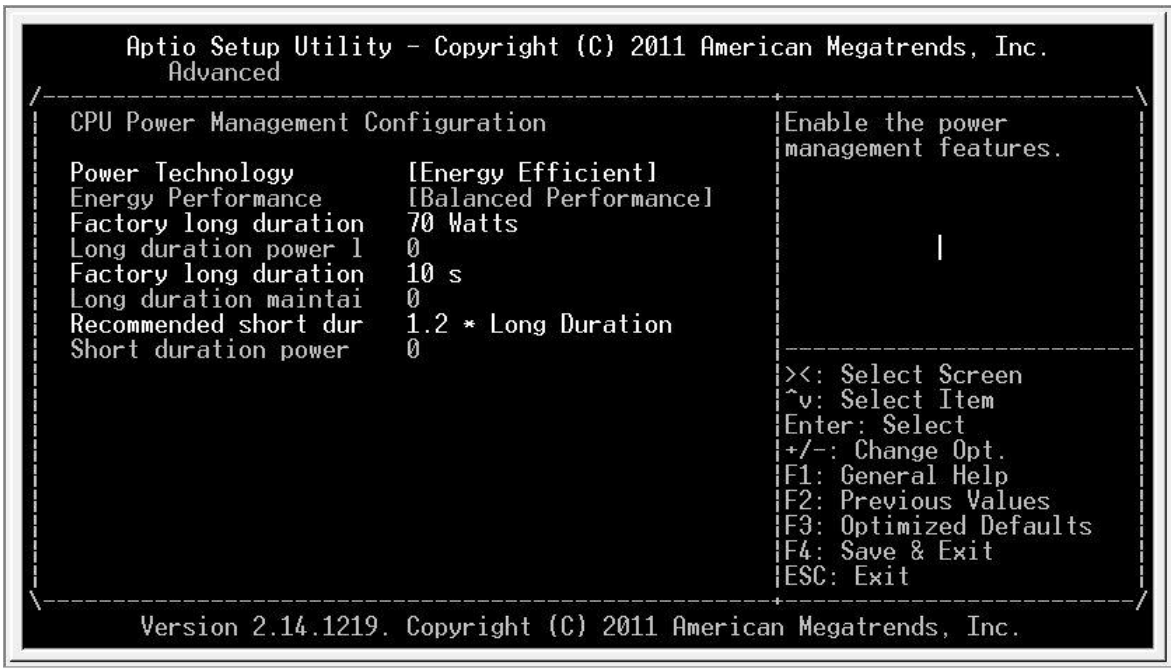
Intel Virtualization Technology consists of components that support virtualization of platforms based on Intel processors, thereby enabling the running of multiple operating systems and applications in independent partitions. Each partition behaves like a virtual machine (VM) and provides isolation and protection across partitions.

Intel VT requires the use of a processor with Intel VT support. Additionally, a third-party VMM may also be required. Options: **Enabled/Disabled**.

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CPU Power Management Configuration

CPU Power Management configuration opens some item for adjusting the load or timing to reduce the power consumption. User can go to this setup page to configure the best setting for the whole system.



Power Technology

This item enables the power management features.

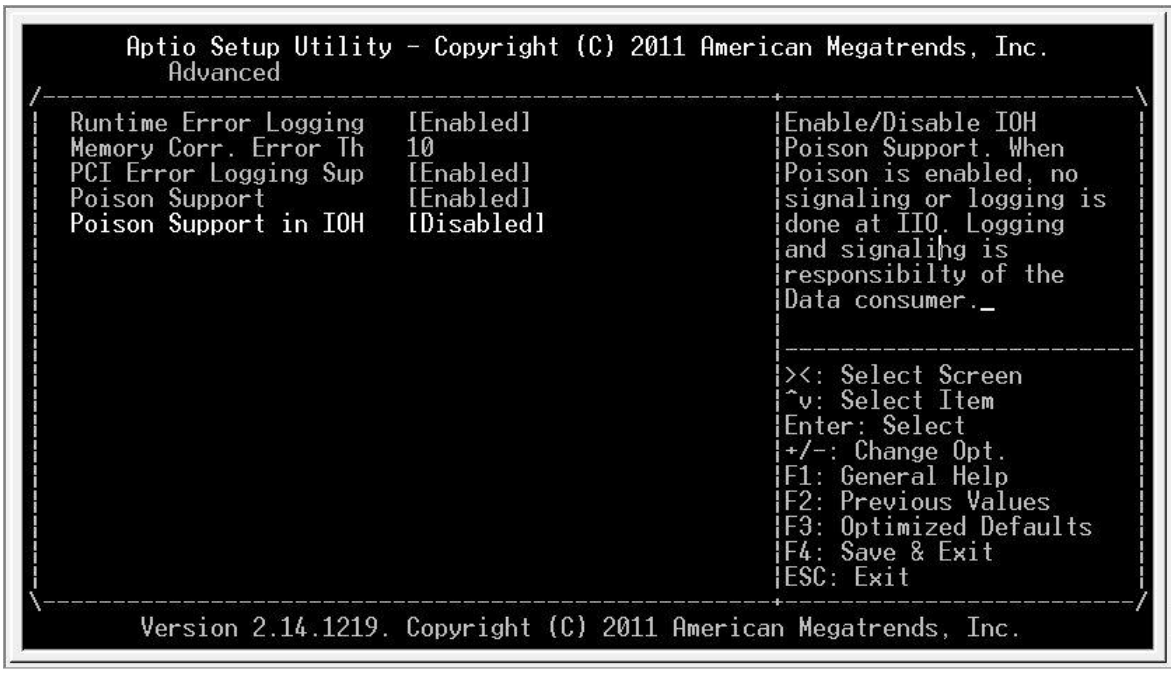
Energy Performance

This item is designed for configuring the energy performance.

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6.3.3 Runtime Error Logging

You can use this screen to specify options for the runtime error logging settings. Use the up and down <Arrow> keys to select an item. Use <+> and <-> keys to change the value of the selected option. The settings are described in the following pages. The screen is shown as below.



Runtime Error Logging

This option allows user to enable or disable runtime error logging.

Memory Corr. Error Threshold

This option is for setting memory correctable error threshold value.

PCI Error Logging Support

This option is for enabling or disabling PCI error logging.

Poison Support

This option is for enabling or disabling Poison Support. When poisoning is enabled, CPU doesn't signal the uncorrectable error via MCERR but may signal CMCI if CMCI is enabled.

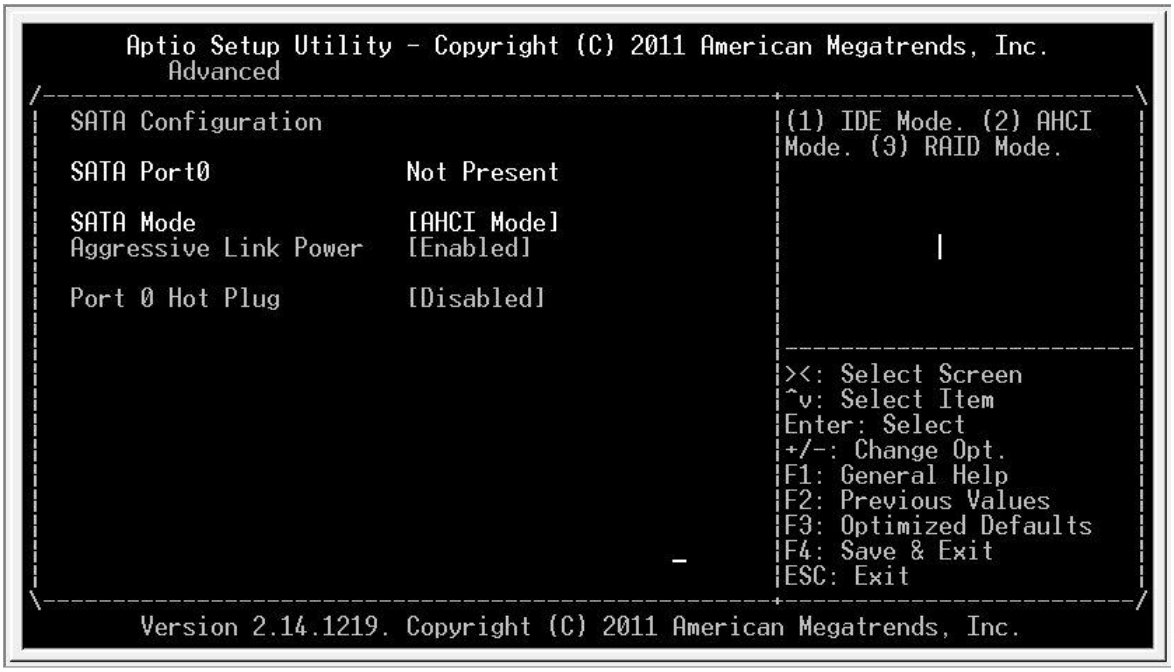
Poison Support in IOH

This option is for enabling or disabling IOH Poison Support. When poison is enabled, no signaling or logging is done at IIO. Logging and signaling is responsibility of the Data consumer.

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6.3.4 SATA Configuration

You can use this screen to specify options for the SATA configuration settings. Use the up and down <Arrow> keys to select an item. Use <+> and <-> keys to change the value of the selected option. The settings are described in the following pages. The screen is shown as below.



SATA Mode

This option is designed for configuring SATA mode. It can be Disabled, IDE Mode and AHCI Mode.

Aggressive Link Power

It allows enabling or disabling Aggressive Link Power for SATA.

Port 0 Hot Plug

When SATA Mode is configured to AHCI Mode, SATA drive is able to be hot plugged. This option allows setting the hot plug function of SATA drive.

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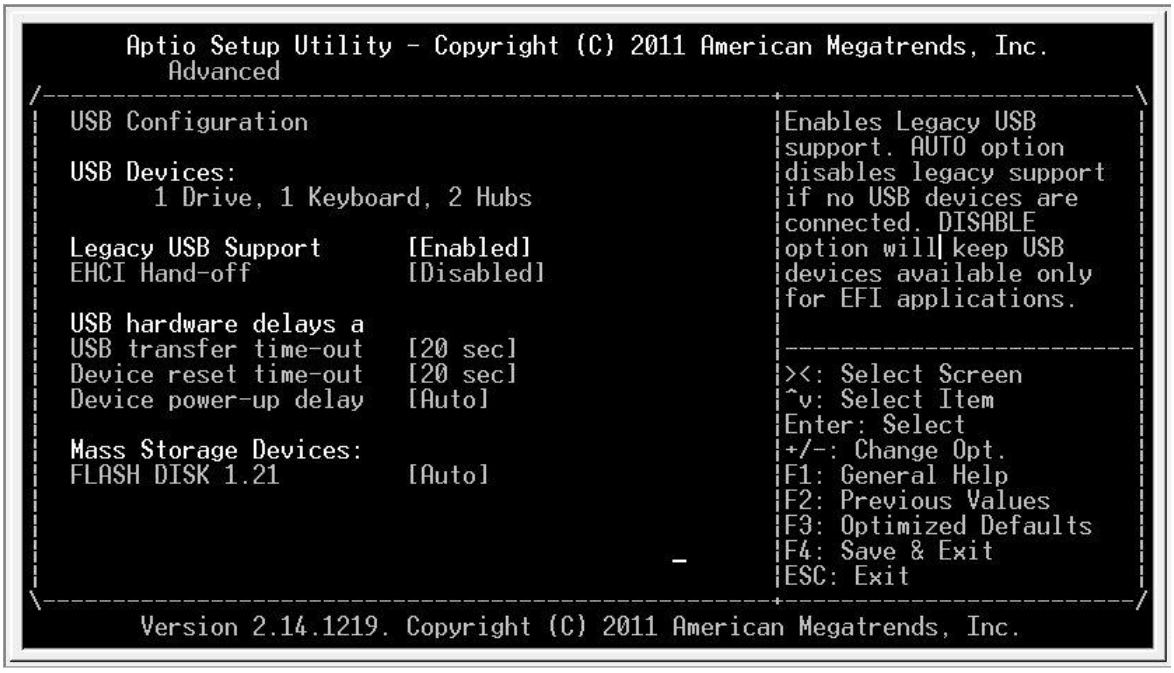
6.3.5 SAS Configuration

You can use this screen to view the current SAS configuration. The SAS device is shown dynamically when system boot. The SAS option will detect the existed drive and then show them on this setup screen. User can check the result of detection from this screen. The screen is shown as below.



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6.3.6 USB Configuration



Legacy USB Support

Legacy USB support refers to USB mouse and keyboard support. If this option is not enabled, any attached USB mouse or keyboard will not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or keyboard can control the system even there is no USB driver loaded on the system.

EHCI Hand-off

This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

USB transfer time-out

This item specifies the timeout in seconds for USB control, bulk, and interrupt transfers.

Device reset time-out

This item specifies the number of seconds that system boot will wait for a USB mass storage device to start.

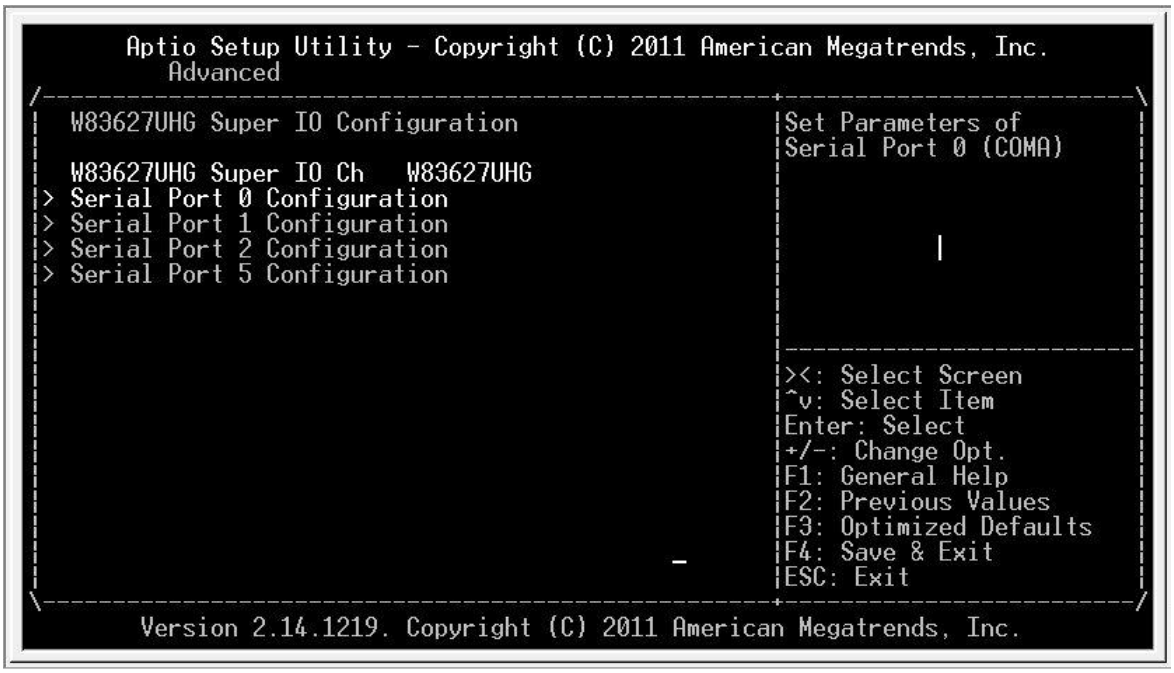
Device power-up delay

This item specifies the maximum time that USB device will take before it reports itself properly to the USB host controller. “Auto” uses the default value: for a root port, it is 100ms, for a Hub port, the delay is taken from Hub descriptor.

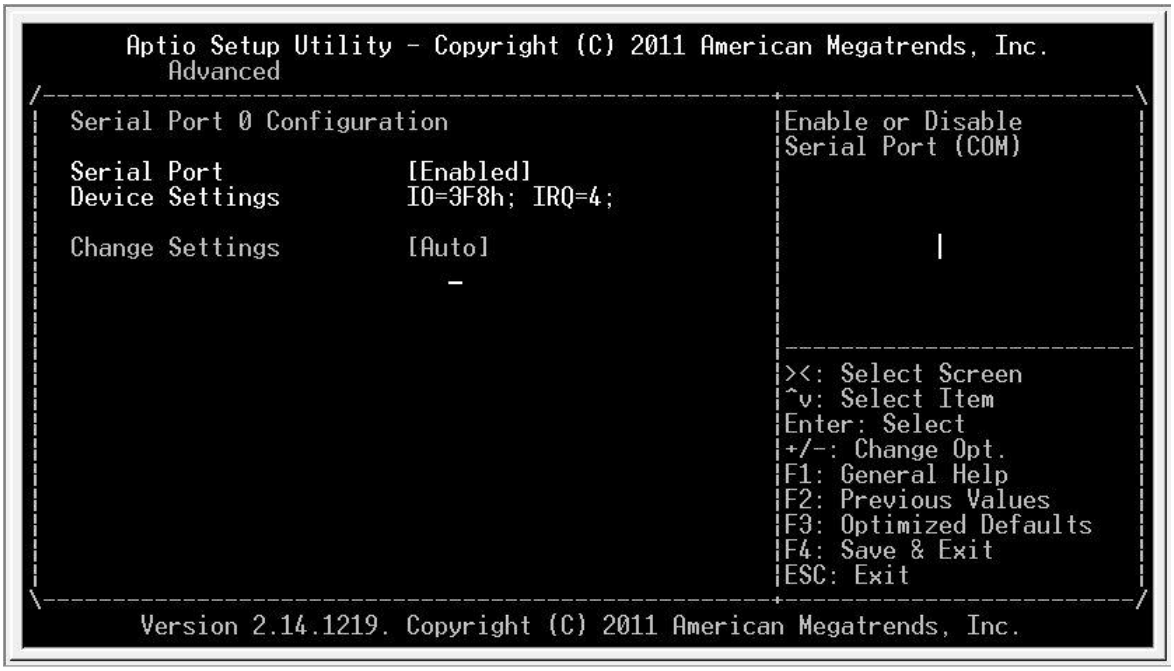
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6.3.7 W83627UHG SIO Configuration

You can use this screen to specify options for the Super IO configuration settings. Use the up and down <Arrow> keys to select an item. Use <+> and <-> keys to change the value of the selected option. The settings are described in the following pages. The screen is shown as below.



Winbond W83627UHG is designed on aTCA-6250. When system boot, BIOS will detect superIO and show the name on this screen.



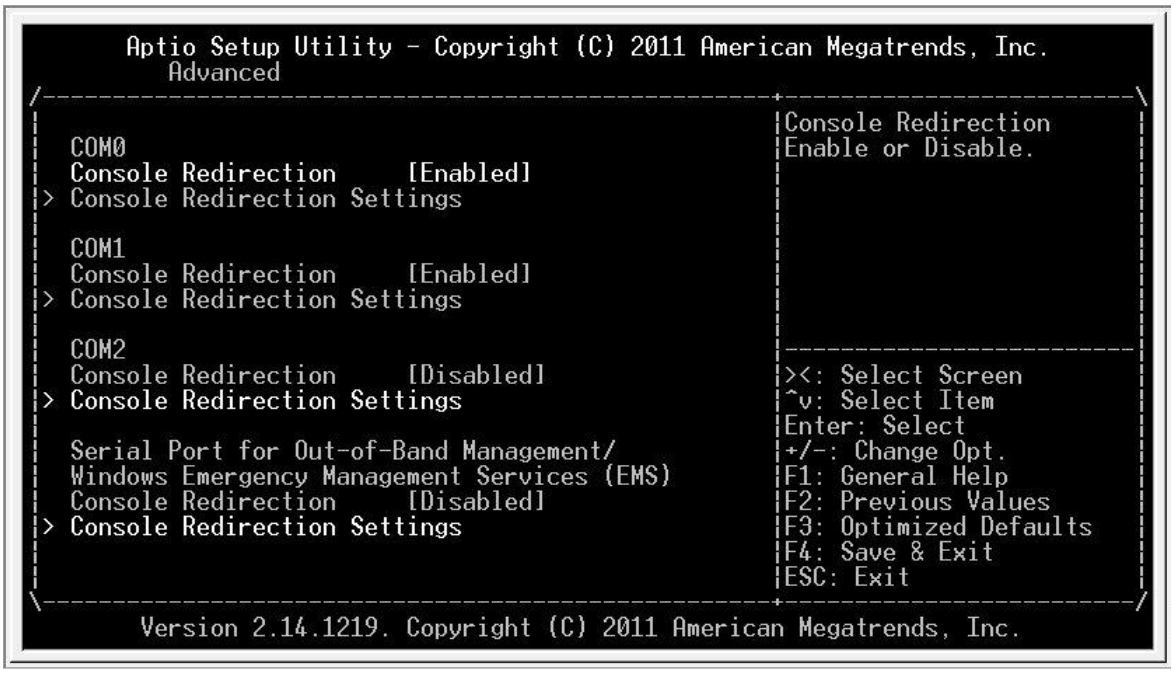
Serial Port

This item is designed for enabling/disabling the serial ports.

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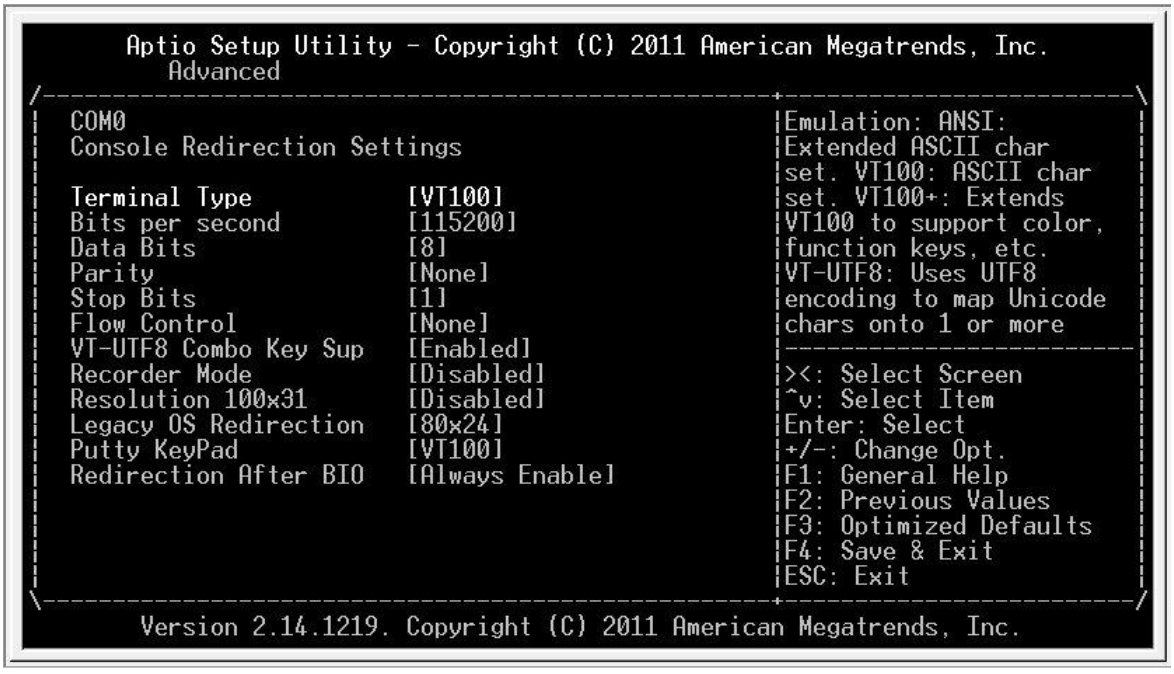
6.3.8 Serial Port Console Redirection

The settings on this setup screen specify how the host computer and the remote computer (which the user is using) exchange data. Both computers should have the same or compatible settings, like baud rate, terminal type, and so on.



6.3.9 COM0/COM1/COM2 Console Redirection

This item is used to configure the enabling/disabling of console redirection to each COM port. For example, COM0 is set to enable console redirection. The below screen will be needed to set properly for communicating with other computer that is using terminal software to receive the message from aTCA-6250.



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Terminal Type

VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100.

Bits per second

Select the bits per second that you want serial port to use for console redirection.

Data Bits

This option allows to select the data bits you want the serial port to use for console redirection.

Parity

Set this option to select Parity for console redirection.

Stop Bits

Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may requires more than 1 stop bit.

Flow Control

Set this option to select Flow control for console redirection.

VT-UTF8 Combo Key Sup

This option is used for enabling or disabling VT-UTF8 Combo key.

Recorder Mode

This option is used for enabling or disabling Recorder Mode.

Resolution 100x31

This option is used for enabling or disabling resolution 100x31 support.

Legacy OS Redirection

This option is used for configuring the legacy OS text format for proper display if system boots to legacy OS with console redirection enabled.

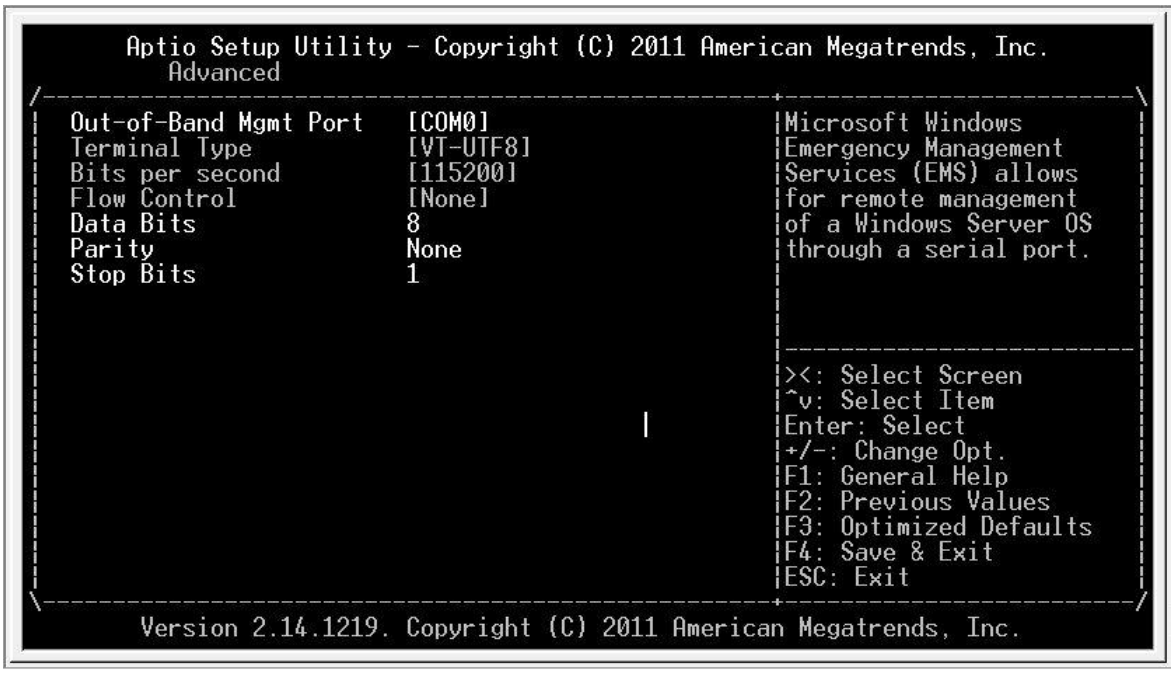
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Putty KeyPad

This option allows configuring the format of keypad when console redirection is enabled.

Redirection After BIOS

This option allows user to configure the console redirection mode via serial port after BIOS POST OK.



Terminal Type

VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100.

Bits per second

Select the bits per second that you want serial port to use for console redirection.

Flow Control

Set this option to select Flow control for console redirection.

Data Bits

This option allows to select the data bits you want the serial port to use for console redirection.

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Parity

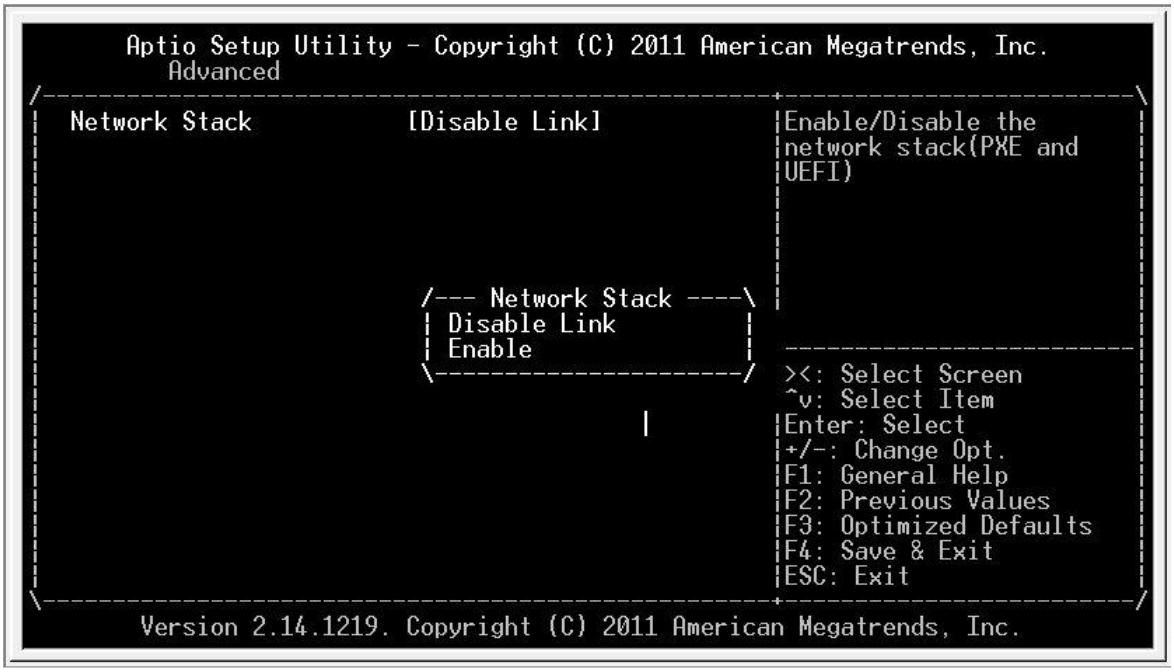
Set this option to select Parity for console redirection.

Stop Bits

Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may requires more than 1 stop bit.

6.3.10 Network Stack

You can use this screen to specify options for the Network Stack settings.
The screen is shown as below.



Network Stack

This option is used for enabling or disabling the network stack for onboard Ethernet.

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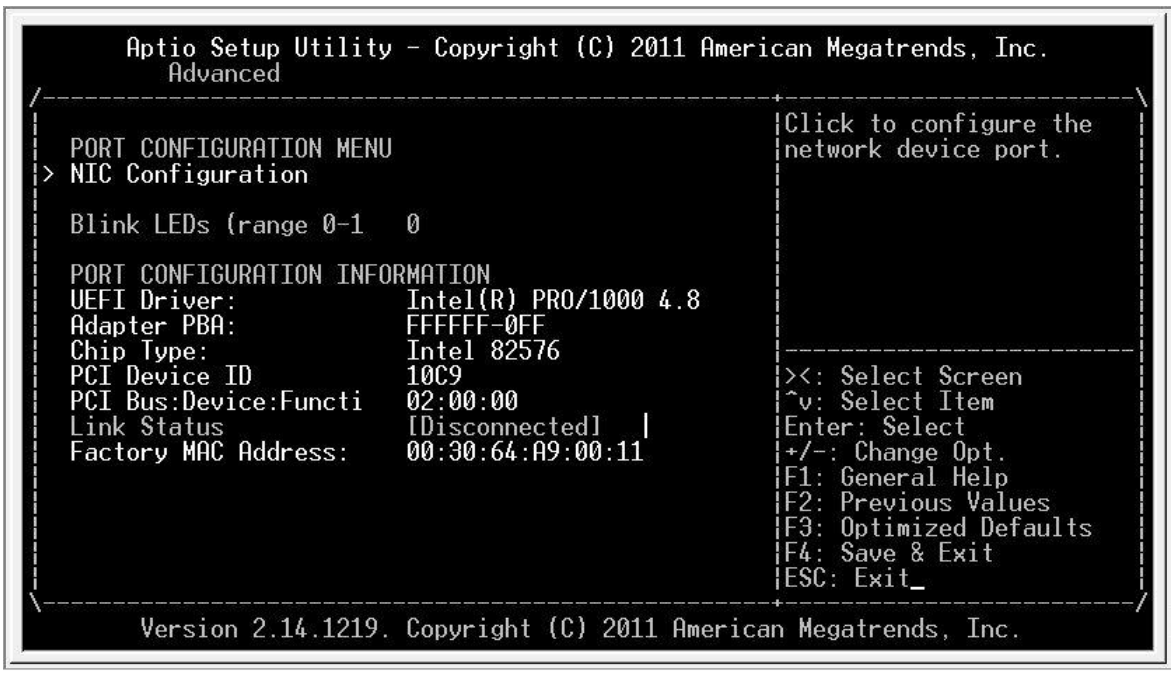
6.3.11 iSCSI

You can use this screen to specify options for the iSCSI settings.
The screen is shown as below.



6.3.12 Ethernet Port Configuration

You can use this screen to specify options for the Ethernet port configuration settings.
The screen is shown as below.



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Ethernet Port Information

The port configuration information will be shown on screen, like chip type, device ID, MA address, and so on.



Link Speed

This option allows user to change link speed and duplex for the current Ethernet port that user is configuring.

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6.4 Chipset Setup Screen

Select Chipset tab from the setup screen to enter Chipset BIOS setup screen. You can select any of the items in the left frame of the screen to go to sub menu for that item. An example of Chipset BIOS setup screen is shown below.

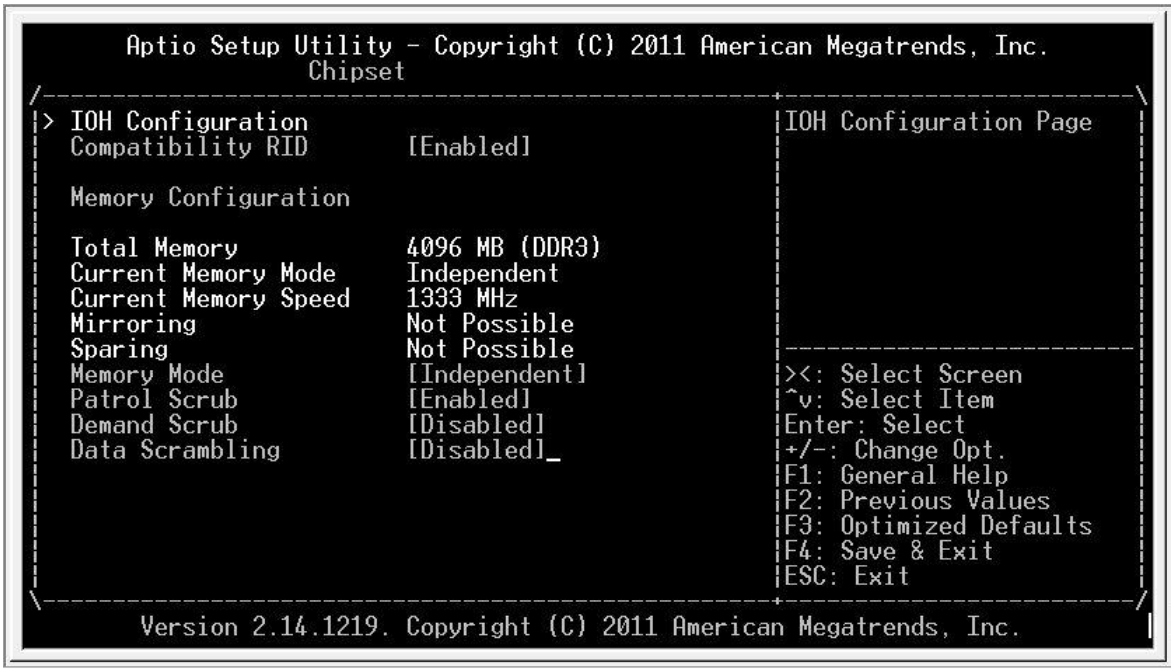
There are two sub bios setup menus for chipset configuration. They are for north bridge and south bridge.



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6.4.1 IOH Configuration

You can use this screen to specify options for the North Bridge settings. Use the up and down <Arrow> keys to select an item. Use <+> and <-> keys to change the value of the selected option. The settings are described in the following pages. The screen is shown as below.



Memory Information

In this setup screen, some memory information will be shown.

Memory Mode

This option is used for configuring the memory mode.

Patrol Scrub

This item is used for enabling or disabling patrol scrub.

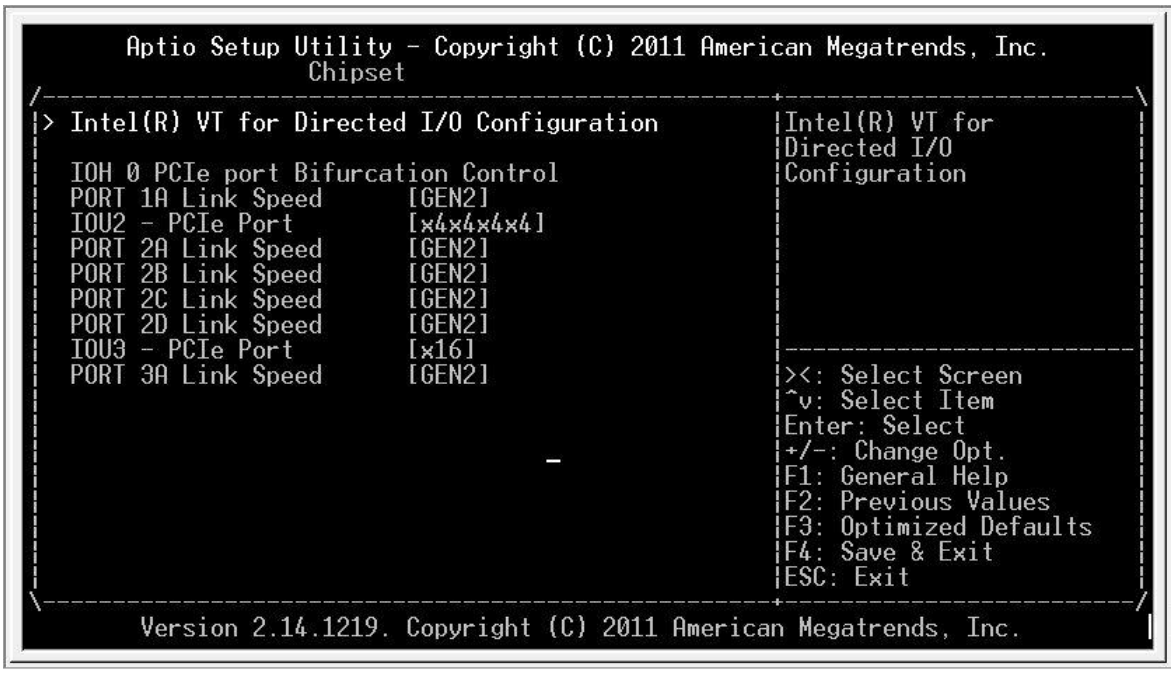
Demand Scrub

This item is used for enabling or disabling Demand Scrubbing feature.

Data Scrambling

This item is used for enabling or disabling Data Scrambling.

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PORT 1A Link Speed

Port 1A is designed to link onboard PCIe x8 Ethernet. This item is for configuring the link speed to x8 device.

IOU2 – PCIe Port

IOU2 can be configured to x4x4x4x4 (if RTM has two x4 PCIe devices) or x4x4x8 (if RTM has one x8 PCIe device)

PORT 2A Link Speed

Port 2A is designed to link onboard PCIe x4 Ethernet. It provides the link to RTM base channel. This item is for configuring the link speed to x4 device.

PORT 2B Link Speed

Port 2B is designed to link onboard PCIe x4 Ethernet. It provides the link to front GbE ports. This item is for configuring the link speed to x4 device.

PORT 2C Link Speed

Port 2C is designed to link onboard PCIe x4/x8 Ethernet. It provides the link to RTM. This item is for configuring the link speed to x4/x8 device.

PORT 2D Link Speed

Port 2D is designed to link onboard PCIe x4 Ethernet. It will not show in setup screen if IOU2 port is configured to x4x4x8. It provides the link to RTM base channel. This item is for configuring the link speed to x4 device.

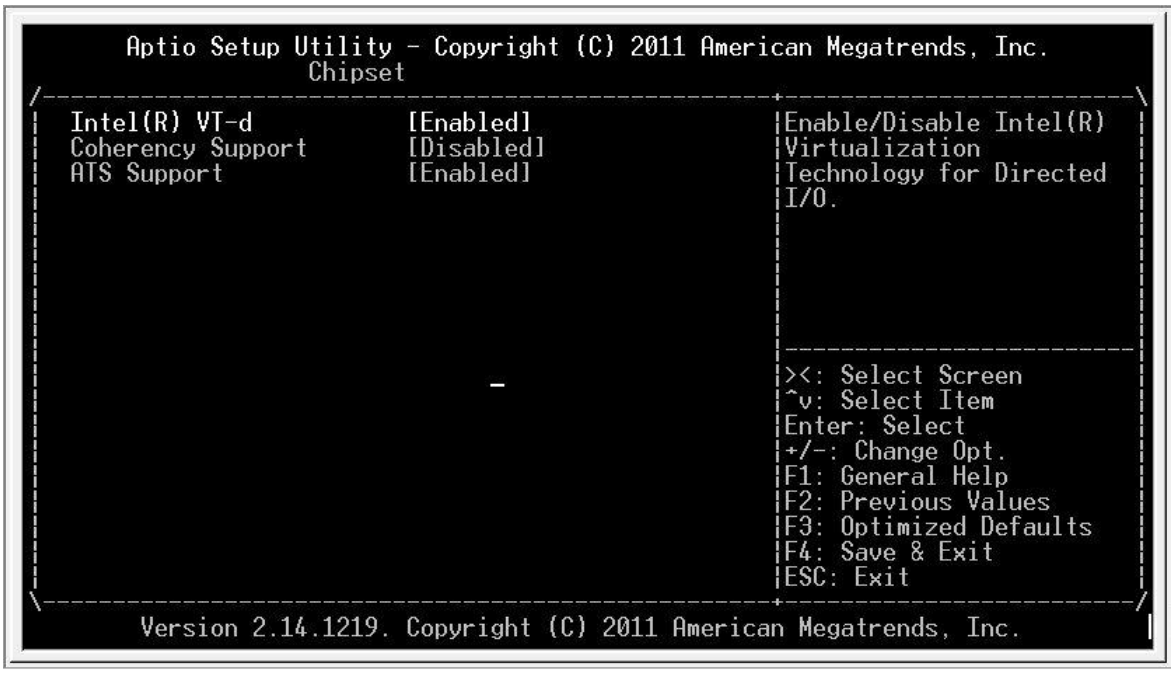
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IOU3 – PCIe Port

IOU3 provides a x16 link to PCIe device.

PORT 3A Link Speed

Port 3A is designed to link onboard PCIe x16 device. This item is for configuring the link speed to x16 device.



Intel(R) VT-d

This item allows user to enable or disable Intel ® VT for directed I/O (VT-d) which provides additional hardware support for managing I/O virtualization.

Coherency Support

It allows user to enable or disable Non-Isoch VT-d Engine Coherency support.

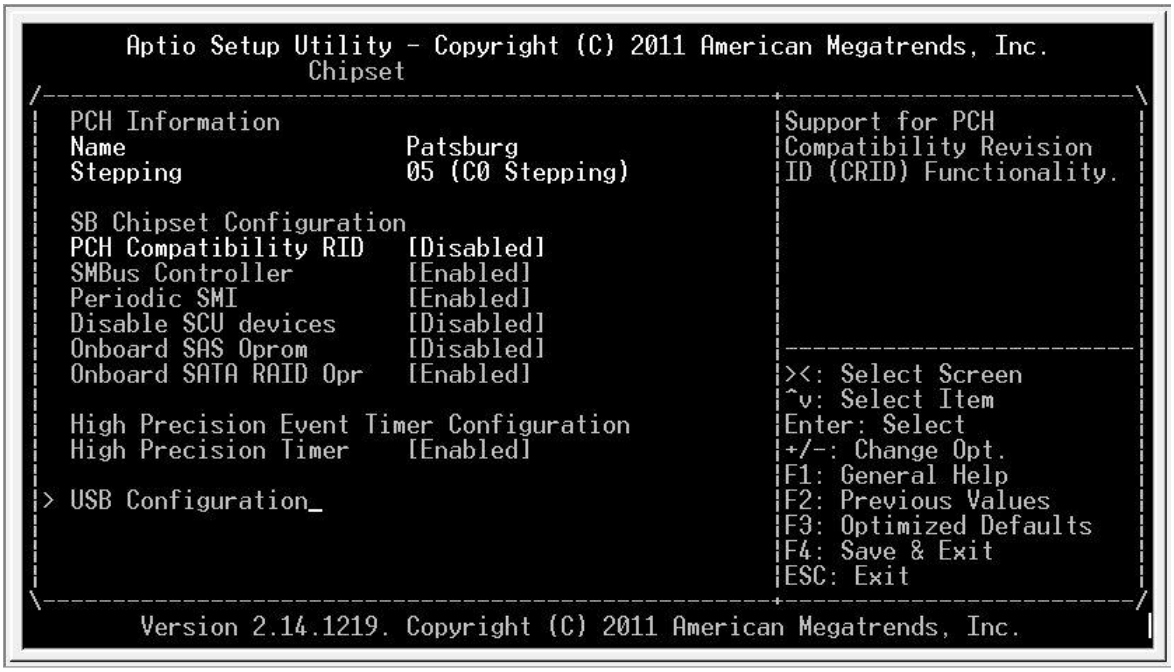
ATS Support

It allows user to enable or disable Non-Isoch VT-d Engine Address Translation Services (ATS) support.

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6.4.2 PCH Configuration

You can use this screen to specify options for the PCH configuration settings. Use the up and down <Arrow> keys to select an item. Use <+> and <-> keys to change the value of the selected option. The settings are described in the following pages. The screen is shown as below.



PCH Information

The PCH information will include the name and stepping of PCH that is designed on aTCA-6250.

PCH Compatibility RID

It is for setting the support for PCH compatibility revision ID (CRID) functionality.

SMBus Controller

This option allows enabling or disabling system's SMBus controller.

Periodic SMI

It allows user to enable or disable the periodic generation of a System management Interrupt (SMI).

Disable SCU devices

It is for enabling or disabling Patsburg SCU devices.

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Onboard SAS Oprom

This item allows user to enable or disable SAS option ROM.

Onboard SATA RAID Oprom

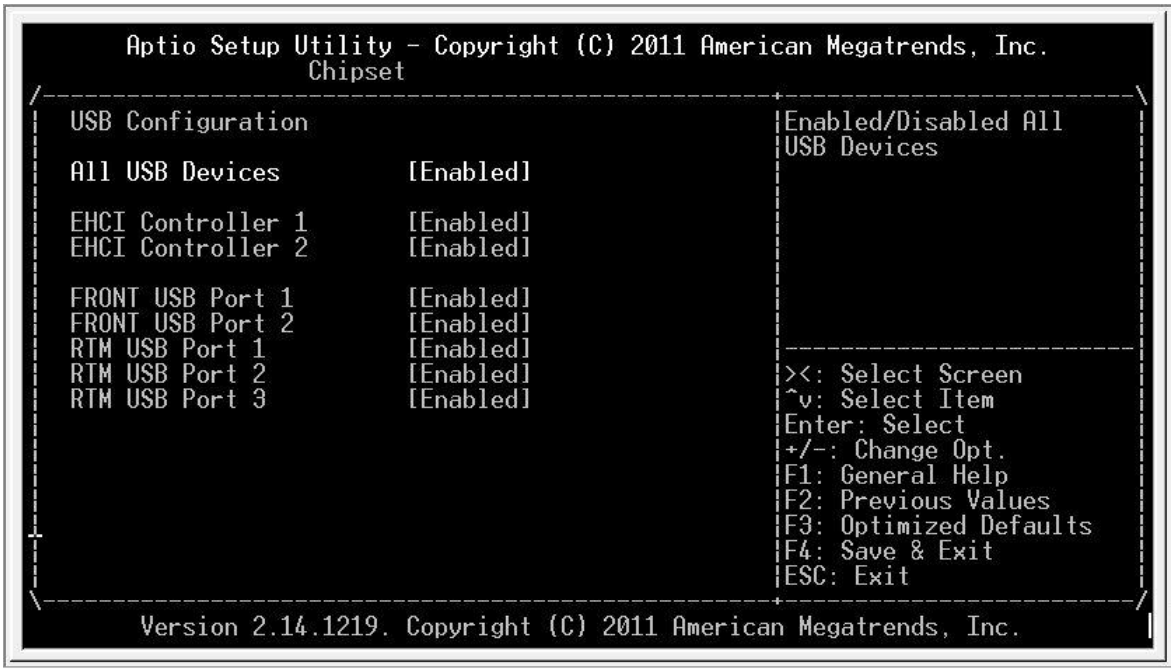
This item allows user to enable or disable SATA RAID option ROM.

High Precision Timer

The High Precision Event Timer is a hardware timer used in personal computers. A High Precision Event Timer chip consists of a 64-bit main counter counting at least at 10MHz and a set of up to 256 comparators. HPET is programmed via a memory mapped I/O window that is discoverable via ACPI. The HPET circuit in modern PCs is integrated into the southbridge. The HPET can produce periodic interrupts at a much higher resolution than the RTC. This option allows user to enable or disable High Precision Event Timer.

USB Configuration

You can use this screen to specify options for the USB configuration settings. Use the up and down <Arrow> keys to select an item. Use <+> and <-> keys to change the value of the selected option. The settings are described in the following pages. The screen is shown as below.



All USB Devices

This item enables or disables all USB devices.

EHCI Controller 1

This item enables or disables USB 2.0 (EHCI) controller 1.

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EHCI Controller 2

This item enables or disables USB 2.0 (EHCI) controller 2.

FRONT USB Port 1

This item is for enabling or disabling front USB port. When it is disabled, all USB device plugged in this front USB port will not work properly.

FRONT USB Port 2

This item is for enabling or disabling front USB port. When it is disabled, all USB device plugged in this front USB port will not work properly.

RTM USB Port 1

This item is for enabling or disabling RTM USB port. When it is disabled, all USB device plugged in this RTM USB port will not work properly.

RTM USB Port 2

This item is for enabling or disabling RTM USB port. When it is disabled, all USB device plugged in this RTM USB port will not work properly.

RTM USB Port 3

This item is for enabling or disabling RTM USB port. When it is disabled, all USB device plugged in this RTM USB port will not work properly.

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6.5 Server Mgmt Setup Screen

You can use this screen to specify options for the Server Management settings. Use the up and down <Arrow> keys to select an item. Use <+> and <-> keys to change the value of the selected option. The settings are described in the following pages. The screen is shown as below.



BMC Support

It is for enabling or disabling the interface to communicate with BMC.

FRB-2 Timer

It is for enabling or disabling FRB-2 timer (POST timer).

FRB-2 Timer timeout

It can select the value between 3 to 6 min for FRB-2 timer expiration value.

OS Watchdog Timer

If enabled, starts a BIOS timer which can only be shut off by Intel Management software after the OS loads.

OS WD Timer Timeout

If is for configuring the length of the OS boot watchdog timer. Not available if OS boot watchdog timer is disabled.

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6.5.1 System Event Log

You can use this screen to specify options for the System Event Log settings. Use the up and down <Arrow> keys to select an item. Use <+> and <-> keys to change the value of the selected option. The settings are described in the following pages. The screen is shown as below.



SEL Components

It is designed for enabling or disabling all features of system event logging during boot.

Erase SEL

It is used for enabling or disabling SEL erasing.

When SEL is Full

It is used for configuring the action if SEL reaches full condition.

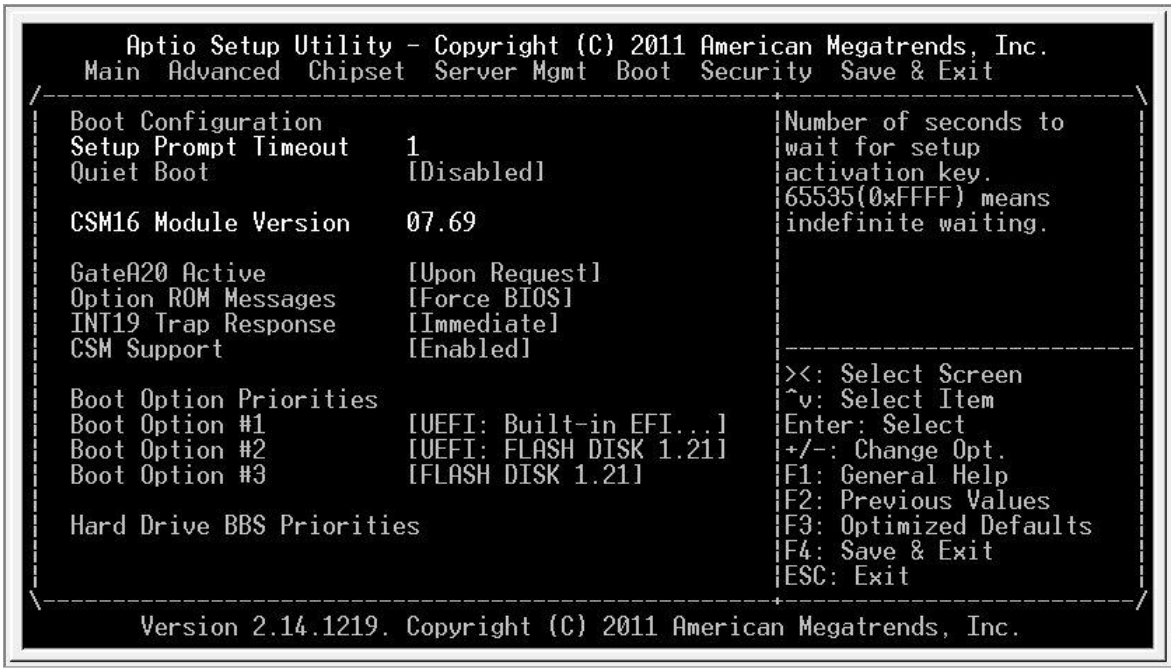
Log EFI Status Codes

It is used for disable the logging of EFI status codes or log only error code or only progress code or both.

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6.6 Boot Setup Screen

You can use this screen to specify options for the Boot configuration settings. Use the up and down <Arrow> keys to select an item. Use the <+> and <-> keys to change the value of the selected option. The settings are described in the following pages. The screen is shown as the below.



Setup Prompt Timeout

It's the number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting. Use the <+> and <-> keys to change the value of this item.

Quiet Boot

This item allows system BIOS to show the boot up splash logo. When it is set to "Enabled", the logo that in system BIOS will be shown during display outputs.

GateA20 Active

Upon Request – GA20 can be disabled by using BIOS services. Always – do not allow disabling GA20. This option is useful when any RT code is executed above 1MB.

Option ROM Messages

Set this option to enable for allowing system to display PCI devices' option ROMs during system boot up.

INT19 Trap Response

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Interrupt 19 is the software interrupt that handles the boot disk function. When set to Enabled, this item allows the option ROMs to trap interrupt 19.

CSM Support

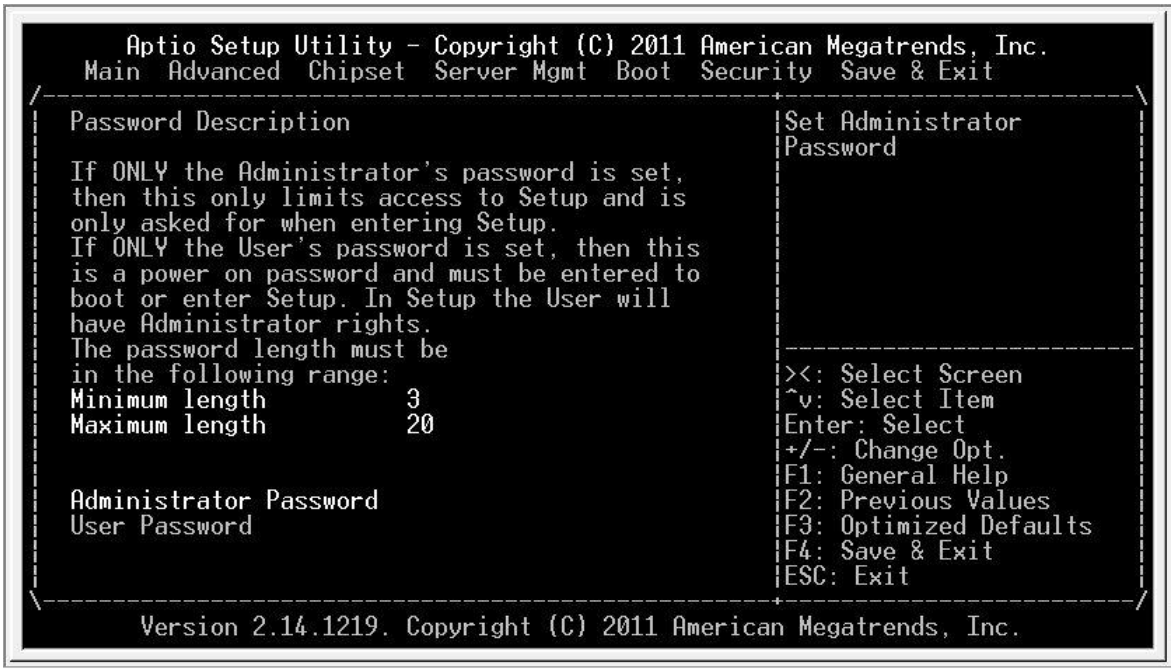
Use this item to enable or disable CSM support. For legacy OS application, CSM is non-EFI environment for proper operation.

Boot Option Priorities

It shows the boot priority of boot devices. User can adjust the order to make customized boot priority of found bootable devices.

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6.7 Security Setup Screen



System BIOS provides two levels of password protection. They are Administrator password and User password. The system can be configured that all users must enter password every time the system boots or when setup utility is executed, using either Administrator password or User password.

The Administrator and User passwords activate two different levels of password security. If you select password support, you are prompted for 3 to 20 characters password. Type the password on the keyboard. The password doesn't appear on the screen when typed. Make sure you write it down. If you forget it, you must drain NVRAM and re-configure it.

Administrator Password

Use this option to set a password for administrator with full control of the BIOS setup utility.

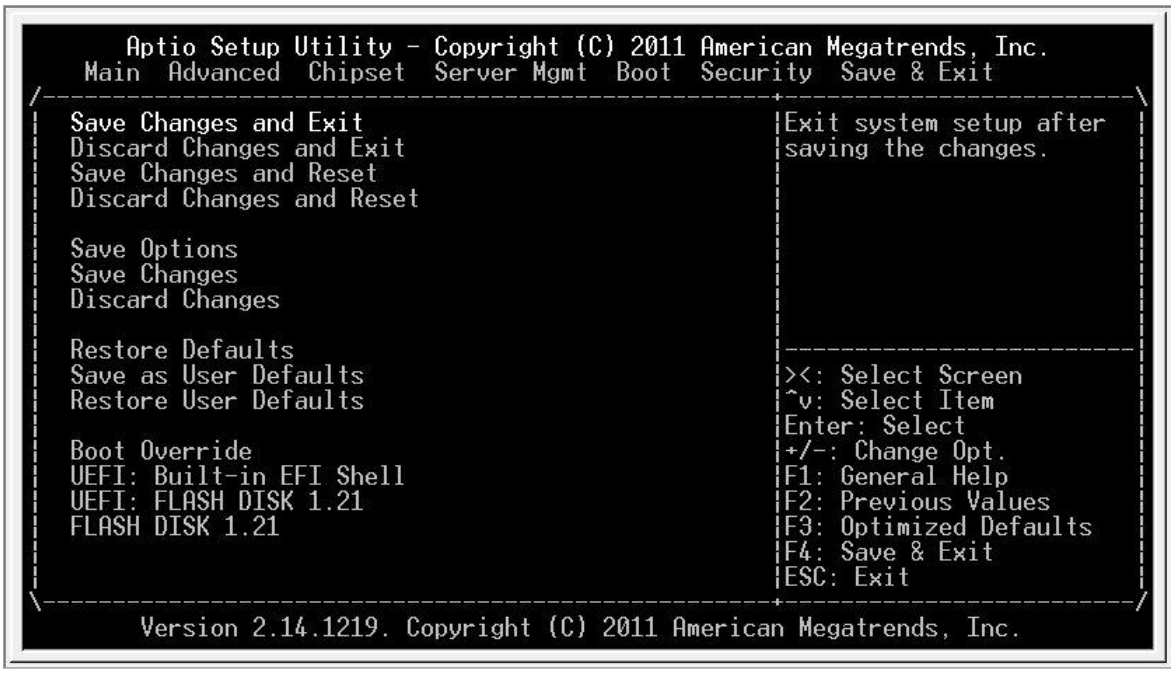
User Password

Use this option to set a password for user with limited access to the BIOS setup utility.

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6.8 Save & Exit Setup Screen

Select ***Save & Exit*** tab from setup utility to enter ***Save & Exit*** BIOS setup screen. You can select an item by highlighting it using the <Arrow> keys. The ***Save & Exit*** BIOS setup screen is shown below.



Save Changes and Exit

When you have completed the system configuration changes, select this option to leave setup utility and reboot the computer to let new system configuration parameters can take effect. When selecting this item and then press <Enter>. The below message will be shown up and wait for the confirmation.

Save Changes and Exit?
[OK] [Cancel]

Select OK and press <Enter> to save changes and exit. It will keep booting the system to OS if no changes need to reset system.

Discard Changes and Exit

Select this option to quit setup without making any permanent changes to the system configuration. When selecting this item and then press <Enter>. The below message will be shown up and wait for the confirmation.

Discard Changes and Exit?
[OK] [Cancel]

Select OK and press <Enter> to discard changes and exit. It will keep booting the system to OS.

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Save Changes and Reset

It has the same function as Save Changes and Exit except resetting system. System will always be reset after selecting this item no matter what change is made,

Discard Changes and Reset

It has the same function as Discard Changes and Exit except resetting system. System will always be reset after selecting this item and will not save any configuration.

Save Changes

Save the changes done so far to any of setup options.

Discard Options

Discard the changes done so far to any of setup options.

Restore Defaults

Load BIOS built-in default value for all setup options.

Save as User Defaults

Save the changes done so far as user defaults.

Restore User Defaults

Restore the saved user default to all the setup options.

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7 Serial Over LAN

Serial Over LAN (SOL) is a remote management feature that allows the IPMC (Smart Fusion A2F500) to redirect the serial console from the blade via an IPMI session over the network with RMCP+ protocol.

The aTCA-6250 supports SOL on the Base Interface which is powered by the Intel 82576 Gigabit Ethernet Controller. The Intel 82576 Gigabit Ethernet Controller is connected to the IPMC (Smart Fusion A2F500) via the NC-SI interface, which provides remote management capability before the payload power is authorized. Users can use the SOL feature to transmit/receive serial console message from a remote site with full console management functionaility.

The aTCA-6250 supports 2 channels (channel 1/2) and 2 user IDs for SOL. You can refer to the following sections for more detailed information.

Note: SOL does not support simultaneous login of more than one user.

7.1 Preparation For SOL Connection

First of all, you need to prepare a remote client with Linux OS and connect to the network.

7.2 Configure The Remote Client

7.2.1 Install IPMItool For The Remote Client

You can download the latest IPMItool and document from the following website http://IPMItool.sourceforge.net

Click on either the *bz or *gz version of IPMItool to download the bzipped or gzipped IPMItool source code tarball respectively.

To build IPMItool, unzip and untar the downloaded IPMItool package, configure IPMItool for your system, and change to the created IPMItool directory to build IPMItool.

Example using the gzipped tarball:

```
tar xvzf IPMItool*.tar.gz□cd IPMItool*
```

Run the following to configure IPMItool for your system:

```
./configure
```


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Build the source code and install IPMItool:

```
make
make install
```

Now your remote client is ready to connect to the target the aTCA-6250.

Note: The install must be run with root permissions to overlay the existing IPMItool utility in /usr/local/bin.

7.3 Configure The Target aTCA-6250

7.3.1 BIOS Configuration

You can refer to section 6.3.8/6.3.9 to enable Serial Port Console Redirection on COM0

Note: The aTCA-6250 supports SOL on COM0 only

7.3.2 Linux grub Setting

GRUB supports sending its messages to the serial console. The following lines should be added to the top of the /boot/grub/grub.conf file.

```
default=1
timeout=5
serial --unit=1 --speed=115200 --word=8 --parity=no --stop=1
terminal --timeout=15 serial console
```

The following parameters need to be passed to each instance of the Linux kernel. They should be added to the kernel line.

```
console=tty0 console=ttyS1,115200n8
```

An example is shown below:

```
title SOL (2.6.18-128.el5)
root (hd0,0)
kernel /boot/vmlinuz-2.6.18-128.el5 ro root=LABEL=/ console=tty0
console=ttyS1,115200n8
initrd /boot/initrd-2.6.18-128.el5.img
```


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7.3.3 Linux System Setting

Linux needs to be told to listen for logins on the serial port. This is done by adding the following line to /etc/inittab.

Add the following line to the init configuration file /etc/inittab.

s1:12345:respawn:/sbin/agetty –L ttyS1 115200 vt100

Now the target aTCA-6250 is ready for SOL connection.

7.4 Establish SOL Connection

Execute the following command from your remote client to establish the SOL Connection Command:

> ipmitool -I lanplus -H <Target IPMC IP > -C < Cipher Suite Id > -U <User Name> -P <Password> sol activate

Note: Please refer to the following table for the Cipher Suite Id

ID	characteristics	Cipher Suite	Authentication Algorithm	Integrity Algorithm(s)	Confidentiality Algorithm(s)
0	“straight password"	00h, 00h, 00h	RAKP-none	None	None
1	S	01h, 00h, 00h	RAKP-HMAC-SHA1	None	None
2	S, A	01h, 01h, 00h		HMAC-SHA1-96	None
3	S, A, E	01h, 01h, 01h			AES-CBC-128
4	S, A, E	01h, 01h, 02h			xRC4-128
5	S, A, E	01h, 01h, 03h			xRC4-40
6	S	02h, 00h, 00h	RAKP-HMAC-MD5	None	None
7	S, A	02h, 02h, 00h		HMAC-MD5-128	None
8	S, A, E	02h, 02h, 01h			AES-CBC-128
9	S, A, E	02h, 02h, 02h			xRC4-128
10	S, A, E	02h, 02h, 03h			xRC4-40
11	S, A	02h, 03h, 00h		MD5-128	None
12	S, A, E	02h, 03h, 01h			AES-CBC-128
13	S, A, E	02h, 03h, 02h			xRC4-128
14	S, A, E	02h, 03h, 03h			xRC4-40
80h-BFh	OEM specified	OEM specified	OEM specified	OEM specified	OEM specified
C0h-FFh	reserved	-	-	-	-

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The default values of the aTCA-6250 SOL parameters are listed in the table below

Parameter	Default Value
Channel 1 IP Address	172.17.172.134
Channel 2 IP Address	172.17.172.135
User ID	2
User Name	adlinkuser
Password	adlinkuser

Below are 2 samples to establish the SOL session via channel 1 with default user name and password:

Sample:

Establish a non-nncrypted RMCP+ SOL session

```
./ipmitool -I lanplus -H 172.17.172.134 -C 0 -U "adlinkuser" -P "adlinkuser" sol activate
```

Establish an encrypted RMCP+ SOL session

```
./ipmitool -I lanplus -H 172.17.172.134 -C 3 -k gkey -U "adlinkuser" -P "adlinkuser" sol activate
```

For more details on IPMI commands, please visit the following site: http://ipmitool.sourceforge.net.

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8 Drivers

The drivers for aTCA-6250 are available on the ADLINK website. Please visit the aTCA-6250 product web site for more details:
http://www.adlinktech.com/PD/web/PD_detail.php?cKind=&pid=1111

We recommend using all the drivers provided on the ADLINK website to ensure driver compatibility. Contact ADLINK to get support for other operating system..

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Safety Instructions

1. Read these safety instructions carefully.
2. Keep this user's manual for future reference.
3. Read the specifications section of this manual for detailed information on the operating environment of this equipment.
4. When installing/mounting or uninstalling/removing equipment, turn off power and unplug any power cords/cables.
5. To avoid electrical shock and/or damage to equipment:
    a. Keep equipment away from water or liquid sources;
    b. Keep equipment away from high heat or high humidity;
    c. Keep equipment properly ventilated (do not block or cover ventilation openings);
    d. Make sure to use recommended voltage and power source settings;
    e. Always install and operate equipment near an easily accessible electrical socket-outlet;
    f. Secure the power cord (do not place any object on/over the power cord);
    g. Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
    h. If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.
6. Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.
7. Equipment must be serviced by authorized technicians when:
    a. The power cord or plug is damaged;
    b. Liquid has penetrated the equipment;
    c. It has been exposed to high humidity/moisture;
    d. It is not functioning or does not function according to the user's manual;
    e. It has been dropped and/or damaged; and/or,
    f. It has an obvious sign of breakage.
8. The equipment can be operated at an ambient temperature of 55°C.

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Getting Service

Contact us should you require any service or assistance.

ADLINK Technology, Inc.
Address: 9F, No.166 Jian Yi Road, Zhonghe District
New Taipei City 235, Taiwan
新北市中和區建一路 166 號 9 樓
Tel: +886-2-8226-5877
Fax: +886-2-8226-5717
Email: service@adlinktech.com

Ampro ADLINK Technology, Inc.
Address: 5215 Hellyer Avenue, #110, San Jose, CA 95138, USA
Tel: +1-408-360-0200
Toll Free: +1-800-966-5200 (USA only)
Fax: +1-408-360-0222
Email: info@adlinktech.com

ADLINK Technology (China) Co., Ltd.
Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203)
300 Fang Chun Rd., Zhangjiang Hi-Tech Park,
Pudong New Area, Shanghai, 201203 China
Tel: +86-21-5132-8988
Fax: +86-21-5132-3588
Email: market@adlinktech.com

ADLINK Technology Beijing
Address: 北京市海淀区上地东路 1 号盈创动力大厦 E 座 801 室(100085)
Rm. 801, Power Creative E, No. 1, B/D
Shang Di East Rd., Beijing, 100085 China
Tel: +86-10-5885-8666
Fax: +86-10-5885-8625
Email: market@adlinktech.com

ADLINK Technology Shenzhen
Address: 深圳市南山区科技园南区高新南七道 数字技术园 A1 栋 2 楼 C 区 (518057)
2F, C Block, Bldg. A1, Cyber-Tech Zone, Gao Xin Ave. Sec. 7,
High-Tech Industrial Park S., Shenzhen, 518054 China
Tel: +86-755-2643-4858
Fax: +86-755-2664-6353
Email: market@adlinktech.com

LiPPERT ADLINK Technology GmbH
Address: Hans-Thoma-Strasse 11, D-68163, Mannheim, Germany
Tel: +49-621-43214-0
Fax: +49-621 43214-30
Email: emea@adlinktech.com

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ADLINK Technology, Inc. (French Liaison Office)
Address: 15 rue Emile Baudot, 91300 Massy CEDEX, France
Tel: +33 (0) 1 60 12 35 66
Fax: +33 (0) 1 60 12 35 66
Email: france@adlinktech.com

ADLINK Technology Japan Corporation
Address: 〒101-0045 東京都千代田区神田鍛冶町 3-7-4
神田 374 ビル 4F
KANDA374 Bldg. 4F, 3-7-4 Kanda Kajicho,
Chiyoda-ku, Tokyo 101-0045, Japan
Tel: +81-3-4455-3722
Fax: +81-3-5209-6013
Email: japan@adlinktech.com

ADLINK Technology, Inc. (Korean Liaison Office)
Address: 서울시 서초구 서초동 1675-12 모인터빌딩 8 층
8F Mointer B/D,1675-12, Seocho-Dong, Seocho-Gu,
Seoul 137-070, Korea
Tel: +82-2-2057-0565
Fax: +82-2-2057-0563
Email: korea@adlinktech.com

ADLINK Technology Singapore Pte. Ltd.
Address: 84 Genting Lane #07-02A, Cityneon Design Centre,
Singapore 349584
Tel: +65-6844-2261
Fax: +65-6844-2263
Email: singapore@adlinktech.com

ADLINK Technology Singapore Pte. Ltd. (Indian Liaison Office)
Address: 1st Floor, #50-56 (Between 16th/17th Cross) Margosa Plaza,
Margosa Main Road, Malleswaram, Bangalore-560055, India
Tel: +91-80-65605817, +91-80-42246107
Fax: +91-80-23464606
Email: india@adlinktech.com

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