aTCA-6900 Series

Dual Quad/Dual-Core LV-Xeon AdvancedTCA
Processor Blade with AMC Bays

User's Manual



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Revision History

Revision	Release Date	Description of Change(s)
2.00	2009/6/2	Initial Release
2.01	2009/7/8	Correct release date
2.02	2011/2/16	Correct Media and User LED colors, add power rating to AMC Bay #2 specification, remove “dual-channel” from memory specification, update addresses
2.03	2011/5/3	Correct Media and User LED colors in tables

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Preface

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Using this Manual

Audience and Scope

The aTCA-6900 User's Manual is intended for hardware technicians and systems operators with knowledge of installing, configuring and operating industrial grade single board computers.

Manual Organization

This manual is organized as follows:

Chapter 1, Introduction: Introduces the aTCA-6900, its features, block diagrams, and package contents.

Chapter 2, Specifications: Presents detailed specification information, power consumption, and board layout drawings.

Chapter 3, Functional Description: Describes the aTCA-6900's functional components and board interfaces.

Chapter 4, Hardware Platform Management: Describes the hardware platform management system, including IPMI sensors, commands, and firmware upgrade procedure.

Chapter 5, Getting Started: Describes the installation of components to the aTCA-6900.

Chapter 6, Driver Installation: Provides information on how to install the aTCA-6900 device drivers.

Chapter 7, Watchdog Timer: Describes the watchdog functionality of the aTCA-6900 Series.

Chapter 8, BIOS Setup: Describes basic navigation for the AMIBIOS®8 BIOS setup utility.

Important Safety Instructions: Presents safety instructions all users must follow for the proper setup, installation and usage of equipment and/or software.

Getting Service: Contact information for ADLINK's worldwide offices.

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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.


NOTE:

Additional information, aids, and tips that help users perform tasks.


CAUTION:

Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.


WARNING:

Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

1.1 Overview

The aTCA-6900 Series is a highly integrated multi-core dual-processor AdvancedTCA server blade supporting four DDR2-667 JEDEC standard angled-type sockets for full-height RDIMM up to 32GB maximum system memory capacity. It features two PICMG AMC.0 single width, mid-size AMC bays with AMC.1, AMC.2 and AMC.3 support. IO features include two 10Gigabit Ethernet ports (XAUI, 1000BASE-KX4) compliant to PICMG 3.1 option 9, four Gigabit Ethernet 10/100/1000BASE-T ports to the face plate and AdvancedTCA Base Interface channels. Detailed features are as follows:

- Two Dual-Core Intel® Xeon® Processor LV 5138 or Quad-Core Intel® Xeon® Processor L5408
- Server-class Intel® 5100/ICH9R chipset
- DDR2-667 JEDEC standard RDIMM(REG/ECC), up to 32GB
- Dual PICMG AMC.0 single-width, mid-size AMC bays
- AMC#1: AMC.1 PCI-Express Type 4, AMC.2 Gigabit Ethernet E2/T3, AMC.3 Storage SATA/SAS
- AMC#2: AMC.1 PCI-Express Type 1, AMC.2 Gigabit Ethernet E2/T3, AMC.3 Storage SATA/SAS
- Onboard 4GB bootable USB interface NAND flash
- Dual Intel® 82571EB PCI-Express Gigabit Ethernet controllers
- Intel® 82598EB PCI-Express 10Gigabit Ethernet (XAUI) controller
- Dual PICMG 3.1 option 1/9 fabric interface channels
- Modular fabric riser card for other PICMG fabric interface protocols
- Optional onboard 24+2 Gigabit Ethernet managed switch
- SATA RAID 0/1/5 enabled rear transition module
- Failover system BIOS
- Analog UXGA high color graphics

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1.2 Block Diagram

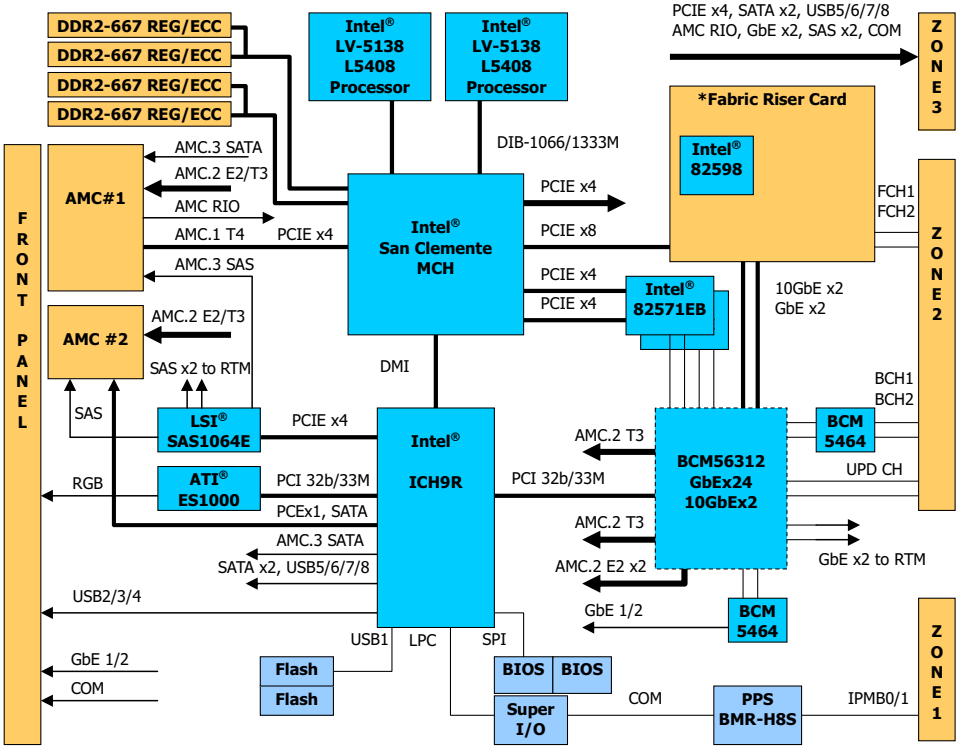


Figure 1-1: aTCA-6900 Series Functional Block Diagram

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1.3 Package Contents

Before opening the product box, please check the shipping carton for any damage. If the shipping carton and contents are damaged, notify the dealer for a replacement. Retain the shipping carton and packing material for inspection by the dealer. Obtain authorization before returning any product to ADLINK.

Check that the following items are included in the package. If there are any missing items, contact your dealer:

- aTCA-6900 Series AdvancedTCA processor blade (CPU, RAM specifications will differ depending on options selected)
- RJ-45 to DB9 cable
- ADLINK All-in-One CD
- This user's manual



This product must be protected from static discharge and physical shock. Never remove any of the components except at a static-free workstation. Use the anti-static bag shipped with the product when putting the board on a surface. Wear an anti-static wrist strap properly grounded on one of the system's ESD ground jacks when installing or servicing system components.

1.4 Product List

Products included in the aTCA-6900 Series:

aTCA-6900 – standard model

aTCA-6900S – with built-in BCM56312 switch

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2 Specifications

2.1 CPU, Chipset, Memory

CPU	• Dual-Core Intel® Xeon® Processor LV 5138 (2.13GHz FSB 1066MHz, 4MB L2 cache, LGA771 package, 65nm) • Quad-Core Intel® Xeon® Processor L5408, (2.13GHz FSB 1066MHz, 12MB L2 cache, LGA771 package, 45nm)
Chipset	• Intel® 5100/ICH9R chipset
Memory	• Registered ECC DDR2-667 SDRAM • Four RDIMM sockets • Up to 32GB

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2.2 Standards and Interface

Standards	• PICMG 3.0 R2.0 AdvancedTCA • PICMG 3.1 option 1/9 Ethernet over AdvancedTCA • AMC.0 Advanced Mezzanine Card R2.0 • AMC.1 PCI Express® R1.0 • AMC.2 Gigabit Ethernet R1.0 • AMC.3 Storage R1.0
Gigabit Ethernet	• Intel® 82571EB PCI-Express Gigabit Ethernet controllers • Four 10/100/1000BASE-T ports on face plate and Base Interface channels 1-2
Serial ATA	• Four Serial ATA II ports from ICH9R, two to AMC, two to RTM • Intel Matrix Storage Driver RAID 0/1/5
Serial Attached SCSI	• Four SAS ports from LSISAS1064E, two to AMC, two to RTM
Display	• ATI ES1000 graphics controller with 2D accelerator • DDR2-533 64MB memory • Analog RGB up to 1600x1200@75Hz refresh rate
USB	• Three USB v2.0 ports
Serial	• One RJ-45 RS-232 port
Storage	• On-board 4GB USB NAND Flash • AMC.3 SATA/SAS • Two SATA and two SAS ports on RTM
Front panel I/O	• 1x VGA port (DB-15) • 3x USB 2.0 port (Type-A) • 1x RS-232 port (RJ45) • 2x GbE ports (RJ45) • LEDs: OOS, Media, Power and Hotswap • Recessed reset button
Rear I/O	• PCI-E x4 from 5100MCH • 2x GbE ports from BCM56312 • 4x USB 2.0 ports • 2x SATA ports from ICH9R • 2x SAS/SATA ports from LSISAS1064E • Rear IO signals from AMC#1

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2.3 Software

BIOS	• AMI® BIOS with 8Mbit flash memory
Supported OS	• Microsoft® Windows® Server 2003 • RedHat Enterprise Linux Release 5.2 • MontaVista Linux Carrier Grade Edition 4.0 • Contact ADLINK for other OS availability

2.4 Mechanical & Environmental

Form factor	• 322.25mm x 280mm x 30.48mm (6HP)
Operating temperature	• Standard: 0°C to 45°C • NEBS short-term: 0°C to 55°C
Storage temperature	• -40°C to 85°C
Humidity	• 5% to 90% non-condensing
Shock	• 15G peak-to-peak, 11ms duration, non-operation
Vibration	• Non-operating: 1.88G rms, 5 to 500 Hz, each axis • Operating: 0.5G rms. 5 to 500Hz, each axis
Compliance	• CE, FCC Class A, CUL, NEBS Level 3 (design)

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2.5 Power Consumption

This section provides information on the power consumption of aTCA-6900.

System Configuration

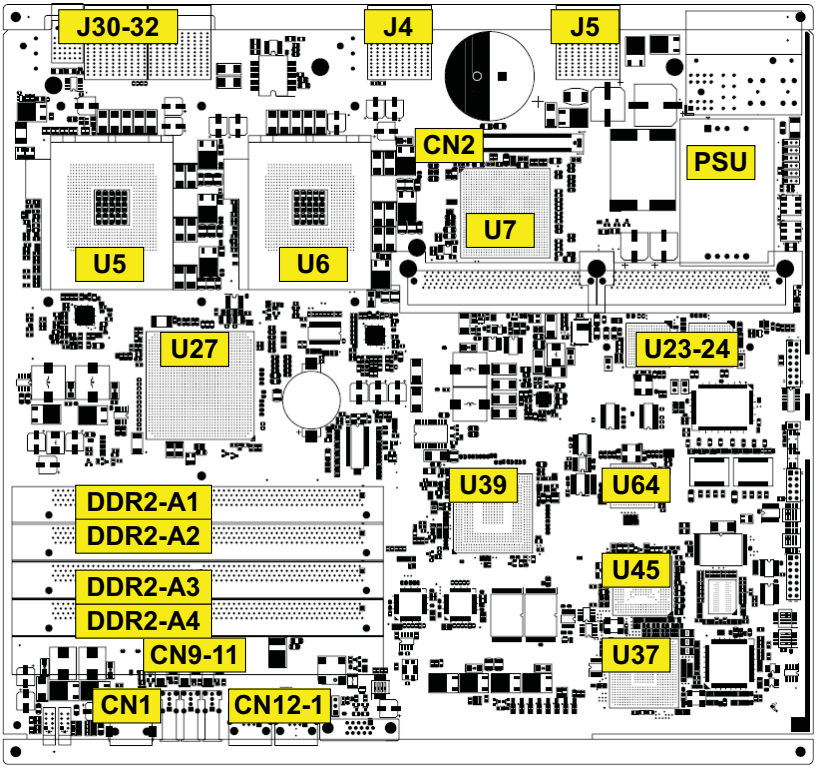
- **Memory:** Transcend 2G DDR2 667 REG-D CL5
- **Graphics:** ATI ES1000
- **AMC Bay:** ADLINKTECH aDB-7000 rev.A1
- **Power Supply:** SUNPOWER SPS-600P-48
- **CPU:**
  - Intel® Quad-Core Xeon® processor L5408
  - Intel® Dual-Core Xeon® processor LV 5138

The following table describes power consumption of the aTCA-6900 using real applications with a 48V power rail under various operating systems.

OS vs. CPU configuration	5138 CPU x1	5138 CPU x2	5408 CPU x1	5408 CPU x2
DOS	72.43 W	88.70 W	76.51 W	82.46 W
Linux, Idle	75.50 W	85.92 W	72.48 W	78.14 W
Windows® XP, Idle	71.32 W	80.49 W	69.93 W	75.16 W
Windows® XP, CPU 100% Usage	99.31 W	139.20 W	112.27 W	168.62 W

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2.6 aTCA-6900 Board Layout



U5, U6	CPU0,1 processors	**CN9-11**	USB ports
U27, U39	5100/ICH9R chipset	**CN12-13**	RJ45 GbE ports
U7, U64	Broadcom SW/PHY	**J4-5**	Zone2
U23, U24	82571EB GbE	**J30-32**	RTM Zone3
U37	LSISAS1064E SAS	**CN2**	Fabric riser card
U45	ATI ES1000 graphics	**CN14**	RJ45 COM
DDR2-A1, A3	DDR2-667 ch-B	**DDR2-A2, A4**	DDR2-667 ch-A

Figure 2-1: aTCA-6900 Board Layout

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2.7 aTCA-6900 Assembly Outline

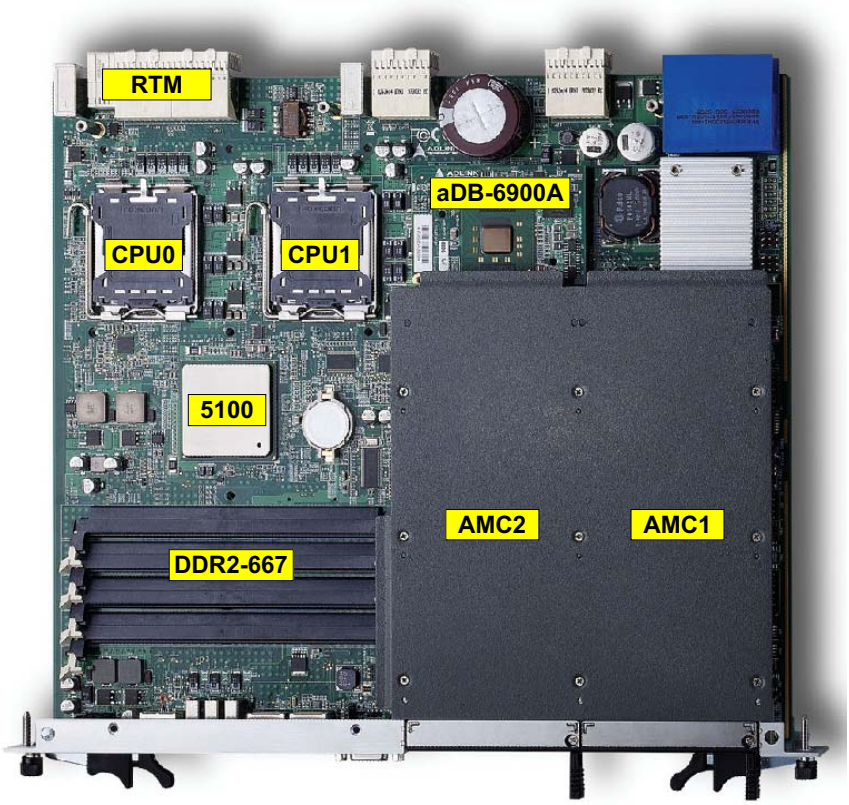


Figure 2-2: aTCA-6900 Assembly Outline

The aDB-6900A is a fabric riser card with dual 10GbE ports for the aTCA-6900.

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2.8 aTCA-6900 Front Panel

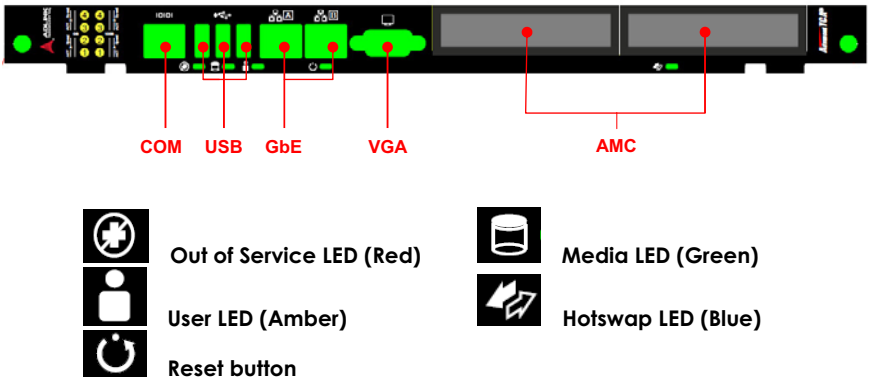


Figure 2-3: aTCA-6900 Front Panel

LED Definitions

The following shows the LED in the front panel which included the Hot-swap LED, User LED, Media LED, and OOS LED.

Hotswap LED

Hot-swap LED (Blue)	FRU State number	FRU State Name
Off	M0	FRU not installed
On	M1	FRU inactive
Long blink	M2	FRU activation request
Off	M3	FRU activation in process
Off	M4	FRU active
Short blink	M5	FRU deactivation request
Short blink	M6	FRU deactivation in process

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OOS LED

Out of Service LED (Red)	State	Remark
Blink	During BIOS POST	FRU State M4
Off	BIOS POST OK	FRU State M4
On	After shutdown the OS	FRU State M1

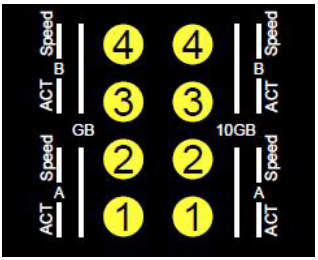
Media LED

Media LED (Green)	State	Remark
Blink	Accessing Disk I/O	
Off	Disk I/O idle	

User LED

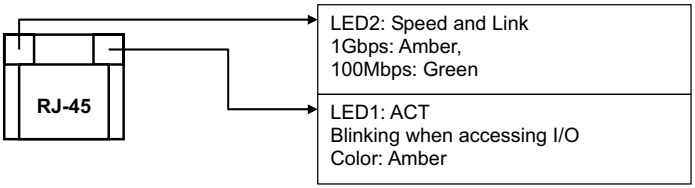
User LED (Amber)	State	Remark
On	Default On	This LED is reserved for customer's application and could be controlled via GPIO.

Base Fabric Channel LED

BASE Channel and Fabric Channel LED		
BCH2 Speed and Link 100 Mbps: Green 1Gbps: Amber		**Fabric 2 Speed and Link** 1Gbps - Green 10Gbps - Amber
BCH2 ACT Blink when accessing Ethernet I/O		**Fabric 2 ACT** Blink when accessing Ethernet I/O
BCH1 Speed and Link 100 Mbps: Green 1Gbps: Amber		**Fabric 1 Speed and Link** 1Gbps - Green 10Gbps - Amber
BCH1 ACT Blink when accessing Ethernet I/O		**Fabric 1 ACT** Blink when accessing Ethernet I/O

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GbE LED



2.9 Compliance

The aTCA-6900 conforms to the following specifications:

- PCIMG 3.0 R2.0 ECN0001 AdvancedTCA
- PICMG 3.1 Ethernet over AdvancedTCA option 1 and 9
- AMC.0 Advanced Mezzanine Card R2.0 Midsize
- AMC.1 PCI Express R1.0
- AMC.2 E2 / Type 3
- AMC.3 Storage R1.0

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3 Functional Description

3.1 CPU, Memory and Chipset

CPU

Two Dual-Core Intel® LV 5138 Processors

The aTCA-6900 supports two Dual-Core Intel® LV-5138 processors at 2.13GHz with 1066MHz FSB and 4MB L2 cache. The Dual-Core Intel® Xeon® Processor 5100 Series are 64-bit server processors utilizing two Intel microarchitecture cores. These processors are based on Intel's 65 nanometer process technology combining high performance with the power efficiencies of a low-power microarchitecture. Some key features include on-die, 32 KB Level 1 instruction and data caches and 4 MB Level 2 cache with Advanced Transfer Cache Architecture. The processors' Data Prefetch Logic speculatively fetches data to the L2 cache before an L1 cache requests occurs, resulting in reduced bus cycle penalties and improved performance. The 1066 MHz Front Side Bus (FSB) is a quad-pumped bus running off a 266 MHz system clock making 8.5 GBytes per second data transfer rates possible.

Enhanced thermal and power management capabilities are implemented including Thermal Monitor (TM1), Thermal Monitor 2 (TM2) and Enhanced Intel SpeedStep® Technology. These technologies are targeted for dual processor in enterprise environments. TM1 and TM2 provide efficient and effective cooling in high temperature situations. Enhanced Intel SpeedStep® Technology provides power management capabilities to servers and workstations.

The Dual-Core Intel® Xeon® Processor LV-5138 features include Advanced Dynamic Execution, enhanced floating point and multi-media units, Streaming SIMD Extensions 2 (SSE2) and Streaming SIMD Extensions 3 (SSE3). Advanced Dynamic Execution improves speculative execution and branch prediction internal to the processor. The floating point and multi-media units include 128-bit wide registers and a separate register for data movement. SSE3 instructions provide highly

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efficient double-precision floating point, SIMD integer, and memory management operations. It also supports Intel® Extended Memory 64 Technology (Intel® EM64T) as an enhancement to Intel's IA-32 architecture. This enhancement allows the processor to execute operating systems and applications written to take advantage of the 64-bit extension technology.

Two Quad-Core Intel® L5408 Processors

In addition to two Dual-Core LV-5138 processors, the aTCA-6900 also supports two Quad-Core Intel L5408 Xeon processors. The Quad-Core Intel® Xeon® Processor L5408 is a server processor utilizing four 45-nm Hi-k next generation Intel® Core™ microarchitecture cores. The processor is manufactured on Intel's 45 nanometer process technology combining high performance with the power efficiencies of a low-power microarchitecture. Some key features include on-die, primary 32-kB instruction cache and32-kB write-back data cache in each core and 12 MB (2 x 6MB) Level 2 cache with Intel® Advanced Smart Cache Architecture. The processors' Data Prefetch Logic speculatively fetches data to the L2 cache before an L1 cache requests occurs, resulting in reduced effective bus latency and improved performance. The 1066 MHz Front Side Bus (FSB) is a quad-pumped bus running off a 266 MHz system clock making 8.5 GBytes per second data transfer rates possible.

Enhanced thermal and power management capabilities are implemented including Intel® Thermal Monitor (TM1), Thermal Monitor 2 (TM2) and Enhanced Intel SpeedStep® Technology. These technologies are targeted for dual processor configurations in enterprise environments. TM1 and TM2 provide efficient and effective cooling in high temperature situations. Enhanced Intel SpeedStep Technology provides power management capabilities to servers and workstations.

Quad-Core Intel® Xeon® Processor L5408 features include Intel® Wide Dynamic Execution, enhanced floating point and multi-media units, Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3), and Streaming SIMD Extensions 4.1 (SSE4.1). Advanced Dynamic Execution

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improves speculative execution and branch prediction internal to the processor. The floating point and multi-media units include 128-bit wide registers and a separate register for data movement. SSE3 instructions provide highly efficient double-precision floating point, SIMD integer, and memory management operations.

It also supports Intel® 64 Architecture as an enhancement to Intel's IA-32 architecture. This enhancement allows the processor to execute operating systems and applications written to take advantage of the 64-bit extension technology.

Supported Processors, Maximum Power Dissipation

The following tables describe the processors supported on the aTCA-6900 and their maximum power dissipation.

	Intel® LV 5138	Intel® L5408
L2 cache	4MB	12MB
Clock	2.13GHz	2.13GHz
FSB	1066MHz	1066MHz

Memory

The aTCA-6900 supports DDR2-667 RDIMM in four sockets up to 32GBytes. The available COTS DDR2-667 RDIMM densities are 1 GB, 2GB, 4GB and 8GB.



Memory configuration changes can only be performed at the factory. Failure to comply with the above may result in damage to your board or improper operation.

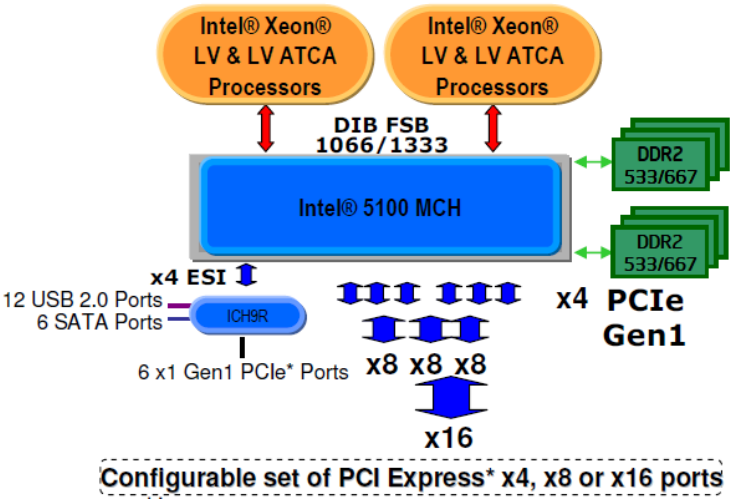
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Chipset

Intel® 5100/ICH9R Chipset Overview

The Intel® 5100 Memory Controller Hub Chipset (code-named San Clemente) is designed for systems based on the Dual-Core Intel® Xeon® processor 5100 series and Quad-Core Intel® Xeon® processor 5400 series, and supports FSB operation of 1066 MT/s. The Intel® 5100 MCH Chipset-based platforms contain two main components: the Memory Controller Hub (MCH) for the host bridge and Intel® 82801IR I/O Controller Hub (ICH9R) for the I/O subsystem.

In an Intel® 5100 MCH Chipset-based platform, the MCH provides two FSB processor interfaces, two DDR2 memory channels, six x4 PCI Express bus interfaces configurable to form x4, x8 or x16 ports, an Enterprise South Bridge Interface (ESI), and three SMBus interfaces for system management, PCI Hot Plug control and DIMM Serial Presence Detect (SPD). The Intel® 5100 Memory Controller Hub Chipset device has DMA Engine (Crystal Beach) capabilities and supports Intel® I/O Acceleration Technology (Intel® I/OAT). The following System Block Diagram shows a block diagram of an Intel® 5100 MCH Chipset based platform.



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The ICH9R is an I/O controller hub supporting various I/O interfaces including six PCI Express x1 ports, Serial ATA host controllers supporting up to six SATA ports at a speed of 3 Gb/s, twelve external USB 2.0 ports with port disable capability, a System Management Bus interface (SMBus), a Serial Peripheral Interface (SPI) and a Low Pincount bus (LPC) for BIOS and firmware storage. Additionally, the ICH9R contains a PCI Controller supporting up to four Bus Masters (PCI Local Bus Specification, Rev. 2.3 compliant), an integrated 10/100/1000 LAN controller and a dedicated ESI port for communication with the MCH.

The ICH9R component provides the data buffering and arbitration required to ensure that system interfaces operate efficiently and provide the bandwidth necessary to enable the system to obtain peak performance. The ICH9R component is ACPI compliant Suspend to RAM, Suspend to Disk, and Soft-Off power management states. Through the use of the integrated LAN functions, the ICH9R also supports Alert Standard Format for remote management.

ATI ES1000 Graphics Controller

The aTCA-6900 provides an analog VGA port on the front panel powered by an AMD ES1000 2D graphics controller with the following features:

- 32-bit PCI bus (Rev 2.2), 3.3 V with bus mastering support
- Support for SPI Serial and Flash Memory video BIOS
- One CRT controller capable of supporting two identical simultaneous display paths
- Dual integrated DACs for CRT display support
- Support for external TMDS transmitter via 24-bit digital output to drive most popular TMDS transmitters up to 165MHz frequency
- Independent DDC lines for both DACs and TMDS connections. Also full AppleSense support on DAC connection
- Static and dynamic Power Management support (APM as well as ACPI) with full VESA DPMS and Energy Star compliance

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- Comprehensive testability including full internal scan, memory BIST, I/O xor tree and Iddq
- Full ACPI 1.0b, OnNow, and IAPC (Instantly Available PC) power management, including PCI power management registers
- Bi-endian support for compliance on a variety of processor platforms
- Bus mastering of 2D display lists
- Triple 10-bit palette DAC supports pixel rates to 350MHz
- DDC1 and DDC2 for plug and play monitors
- Flexible memory support:
  - DDR1 and DDR2 SDRAM and SGRAM
  - 16-bit interface
  - 8MB to 256MB
- Up to 1GB/s bandwidth.
- Single chip solution in 0.13 micron process, 1.2V CMOS technology in a BGA package

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3.2 Peripherals

The following standard peripherals are available on the aTCA-6900 blade:

Timer

The aTCA-6900 is equipped with the following timers:

- Real-Time Clock: The IICH contains a real-time clock that performs timekeeping functions and includes 256 bytes of general purpose battery-backed CMOS RAM. Features include an alarm function, programmable periodic interrupt and a 100-year calendar. All battery-backed CMOS RAM data remains stored in an additional EEPROM. This prevents data loss in case the aTCA-6900 is operated without battery.
- Counter/Timer: Three 8254-style counter/timers are included on the aTCA-6900 as defined for the PC/AT (System Timer, Refresh Request, Speaker Tone Output).
- In addition to the three 8254-style counters, the IICH includes three High Precision Event Timers (HPET) that may be used by the operating system. They are implemented as a single counter each with its own comparator and value register. They support One-shot and periodic interrupts.

Watchdog Timer

The aTCA-6900 provides a Watchdog Timer that is programmable for a timeout period ranging from 1 to 255 minutes in the *minute mode*, or 1 to 255 seconds in the *second mode*. Please refer to “section 6 Watchdog Timer” for detail programming guide.

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Battery

The aTCA-6900 is provided with a 3.0 V “coin cell” lithium battery for the RTC. To replace the battery, proceed as follows:

- Turn off power
- Remove the battery
- Place the new battery in the socket

Make sure that you insert the battery with the correct orientation. The positive pole must be on the top

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. A suitable battery is the PANASONIC CR2032.



NOTE:

The user must be aware that the battery’s operational temperature range is less than that of the aTCA-6900’s storage temperature range. For exact range information, refer to the battery manufacturer’s specifications.



NOTE:

Care must be taken to ensure that the battery is correctly replaced. The battery should be replaced only with an identical or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer’s instructions. The typical life expectancy of a 225mAh battery is 4-5 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and standby (shutdown) time of the system in which it operates. To ensure that the lifetime of the battery has not been exceeded, it is recommended to change the battery after 3-4 years.

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Reset

The aTCA-6900 is automatically reset by a precision voltage monitoring circuit that detects a drop in voltage below the acceptable operating limit of 4.85V for the 5V line and below 3.2V for the 3.3V line. Other reset sources include the Watchdog Timer, the face plate push-button switch and also the RESET signal from the IPMC. The aTCA-6900 responds to any of these sources by initializing local peripherals.

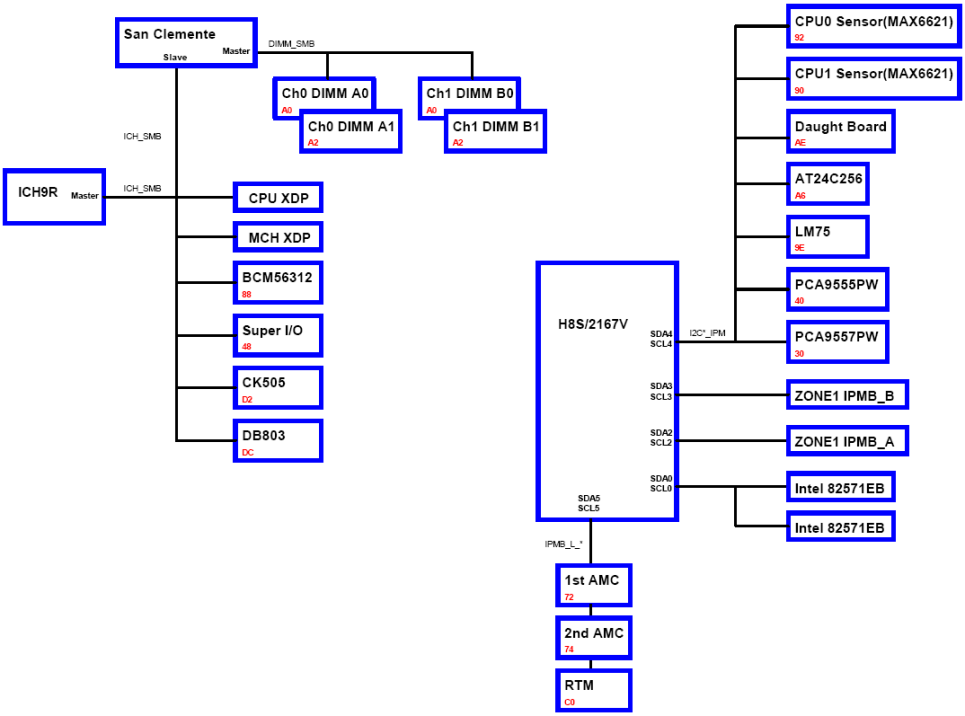
A reset will be generated by the following conditions:

- Power failure, +5 V supply falls below 4.1 V (typ.) or +3.3 V supply falls below 2.93 V (typ.)
- Pushbutton ´RESET" pressed
- Watchdog time-out
- IPM controller reset

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SMBus and I2C Devices

The aTCA-6900 provides a system management bus (SMBus) hosted by the ICH9R and an I2C bus hosted by the IPM controller, H8S/2168, as shown in the following diagram. The following table describes the function and address of the devices.



SMBus Device	Address (HEX)	I2C Device	Address (HEX)
DDR2-A0	10100010(A2)	CPU0 sensor	10010010(92)
DDR2-A1	10100000(A0)	CPU1 sensor	10010000(90)
DDR2-B0	10101010(AA)	External FRU	10100110(A6)
DDR2-B1	10101000(A8)	LM75	10011110(9E)
BCM56312	10001000(88)	PCA9555PW	01000000(40)
Super IO	01001000(48)	PCA9557PW	00110000(30)
Clock Gen	11010010(D2)	Fabric riser card	10101110(AE)
Clock Buffer	11011100(DC)		

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GPIO List

The following table summarizes GPIO usage on ICH9R IO controller hub:

ICH9R	I/O	Signal	Description
GPI[0]	Input	LPC_PME-L	LPC power management event
GPI[8]	Input	ICH_GPIO8	Debug from MCH ERR-L1
GPI[10]	Input	ICH_GPIO10	Debug from MCH ERR-L2
GPO[15]	Output	PCI_STOP-L	PCI stop to clock generator
GPI[19]	Input	3255_INT_REQ1	Interrupt request 1 from IDT82V3255
GPI[21]	Input	3255_INT_REQ2	Interrupt request 2 from IDT82V3255
GPI[22]	Input	LPC_SMI-L	LPC system management interrupt from IPMC
CPO[25]	Output	CLK_CPU_STOP-L	CPU stop to clock generator
GPO[27]	Output	10G-LAN0_DISABLE-L	Disable LAN0 on fabric riser card
GPO[28]	Output	10G_LAN1_DISABLE-L	Disable LAN1 on fabric riser card
GPO[32]	Output	POSTOK-L	POST OK to IPMC
GPO[34]	Output	USERLED	User defined LED, default = Power LED
GPI[38]	Input	ICH_GPIO38	Debug from MCH ERR-L10
GPO[39]	Output	ICH_CPU0_FORCEPR-L	CPU0 forced protection
GPO[48]	Output	ICH_CPU1_FORCEPR-L	CPU1 forced protection
GPI[57]	Input	W83627_OVT-L	W83627 over-temperature event
GPO[58]	Output	3255_CS-L2	Chip select to IDT82V3255

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3.3 I/O Interfaces

USB

The aTCA-6900 supports eight USB 2.0 ports:

- three Type-A ports on front panel
- four ports routed to RTM
- one channel for 4GB on-board NAND flash

On the USB 2.0 front panel port, a USB cable with up to 5 meters in length can be used.

On the USB 2.0 Rear I/O ports, it is strongly recommended to use a cable below 3 meters in length for USB 2.0 devices.

The USB 2.0 ports are high-speed, full-speed, and low-speed capable. Hi-speed USB 2.0 allows data transfers of up to 480 Mb/s, 40 times faster than a full-speed USB (USB 1.1). One USB peripheral may be connected to each port.

Front Panel USB Connector (CN9-11)

Pin #	Signal Name
1	Vcc
2	UV0-
3	UV0+
4	GND

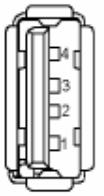


Table 3-1: Front Panel USB Connector Pin Definition

NOTE: The aTCA-6900 host interfaces can be used with maximum 500mA continuous load current as specified in the Universal Serial Bus Specification, Revision 2.0. Short circuit protection is provided. All the signal lines are EMI filtered.

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VGA Analog Interface

The DB-15 female connector CN15 is for analog display output.

DB-15 VGA Connector (CN15)

Signal Name	Pin #	Pin #	Signal Name
Red	1	2	Green
Blue	3	4	N.C.
GND	5	6	GND
GND	7	8	GND
+5V.	9	10	GND
N.C.	11	12	DDC_DATA
HSYNC	13	14	VSYNC
DDC_CLK	15		

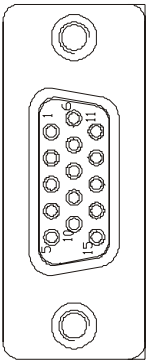


Table 3-2: VGA Connector Pin Definition

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Gigabit Ethernet

aTCA-6900

The standard aTCA-6900 contains two Intel® 82571EB Dual Gigabit Ethernet controllers, which provide a total of four 10/100/1000Base-T ports onboard. In default configuration, two of them are connected to the front panel and the other two are connected to the Base Interface channels.

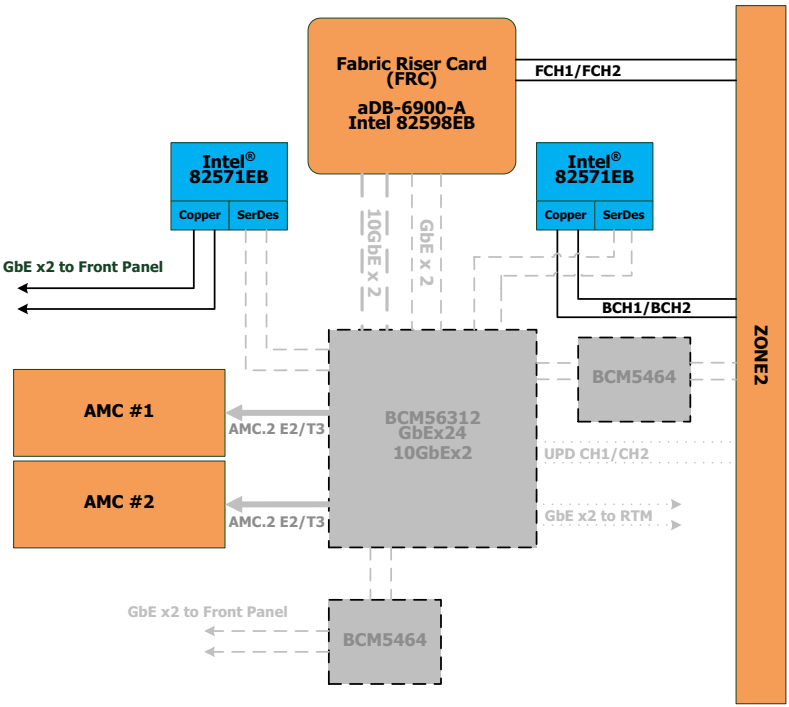


Figure 3-1: Standard aTCA-6900 GbE Configuration

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aTCA-6900S

In the aTCA-6900S with built-in BCM56312 switch, the 82571EB controllers will work in SERDES mode providing the ports to the onboard BCM56312 24-port layer 3 switch. The port mapping in this configuration is shown in the table below.

The Fabric Riser Card (FRC) provides the capability to support different configurations for FCH1 and FCH2. An aDB-6900-A FRC is installed on both the aTCA-6900 and aTCA-6900S by default. The Intel 82598EB Ethernet controller connects to the MCH via a PCI-E x8 interface and provides 10GbE link to FCH1 and FCH2.

Port	Connection	Port	Connection
0	82571EB port 0	10-11	AMC#1 port 0/1
1	82571EB port 1	12-14	AMC#1 port 8-10
2	N/A	15	FRC port 0
3	N/A	16-17	RTM port 0/1
4-5	Egress GbE 1/2	18-19	AMC#2 port 0/1
6-7	N/A	20-22	AMC#2 port 8-10
8-9	Update Ch 1/2	23	FRC port 1

Table 3-3: aTCA-6900S GbE Configuration

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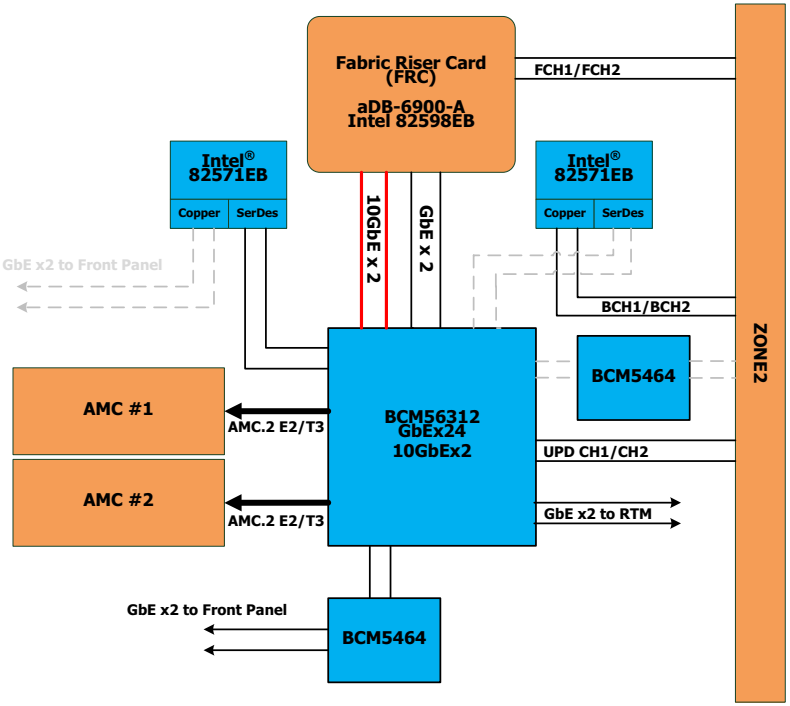


Figure 3-2: aTCA-6900S GbE Custom Configuration

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Serial Port

One PC-compatible serial RS-232, RJ45 port is provided on the front panel with DIP switches SWX1 and SWX2 used to set COM function. A complete set of handshaking and modem control signals are supported, with data transfer rates up to 115.2 kB/sec.

The Front Panel RJ45 COM connector CN14 pin-assignment are DIP switch settings are listed below.

COM1 Serial Port Connector (RJ45)

Pin #	Signal	Function
1	DCD#	Data Carrier Detect
2	RTS#	Request to Send
3	DSR#	Data Set Ready
4	TXD	Transmit Data
5	RXD	Receive Data
6	GND	Ground
7	CTS#	Clear to Send
8	DTR#	Data Terminal Ready

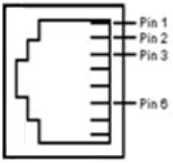


Table 3-4: COM1 Serial Port Connector Pin Definition

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COM Mode Switch Settings (SWX1 and SWX2)

Mode	Switch	Pin 1	Pin 2	Pin 3	Pin 4
RS-232 (default)	SWX1	ON	ON	OFF	OFF
	SWX2	ON	OFF	N/A	
IPMC debug port	SWX1	OFF	OFF	ON	ON
	SWX2	OFF	ON	N/A	

Table 3-5: COM Mode Switch Settings

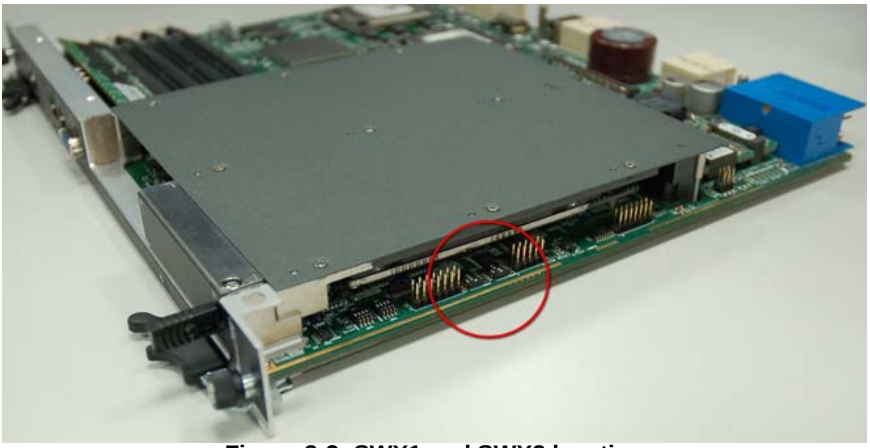


Figure 3-3: SWX1 and SWX2 location

When the switch SWX4 is set to IPMC debug port, the pin assignment of the RJ45 connector is as below.

Pin #	Signal	Function
1	NC	Not connected
2	NC	Not connected
3	NC	No connected
4	DBG_TX	IPMC Transmit Data
5	DBG_RX	IPMC Receive Data
6	GND	Ground
7	NC	No connected
8	NC	No connected

Table 3-6: IPMC Debug Port Connector Pin Definition

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3.4 AMC Bays

The aTCA-6900 provides two PICMG AMC.0 R2.0 single width, mid-size AMC bays, with the following features:

AMC#1:

- AMC.1 PCI Express Type 4 (PCI-E x4 from 5100 MCH)
- AMC.2 Gigabit Ethernet E2/Type 3 (from BCM56312)
- AMC.3 Storage S2 (port2: SATA from ICH9R, port3: SAS from LSISAS1064E)
- TDP: 60W (+12V, 5A, maximum)
- 8 contacts allocated to Payload Power
- 56 contacts to allocated to Logic Ground
- 2 contacts reserved

AMC#2:

- AMC.1 PCI Express Type 1 (port4: PCI-E x1 from ICH9R)
- AMC.2 Gigabit Ethernet E2/Type 3 (from BCM56312)
- AMC.3 Storage S2 (port2: SATA from ICH9R, port3: SAS from LSISAS1064E)
- TDP: 30W (+12V, 2.5A, maximum)

The AMC connector pin assignment is as follows.



NOTE:

For AMC#2, pins 50, 51, 53, 54, 59, 60, 62, 63, 65, 66, 68, 69 are not connected (NC).

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Pin#	Signal	Function	Pin#	Signal	Function
85	GND	Logic Ground	86	GND	Logic Ground
84	P12V_ PWR	12V Payload Power	87	GE12_RX-	Port 8 AMC.2 T3 RX-
83	PS0#	Presence 0	88	GE12_RX+	Port 8 AMC.2 T3 RX+
82	GND	Logic Ground	89	GND	Logic Ground
81	PCIEREF-	Fabric Clock A-	90	GE12_TX-	Port8 AMC.2 T3 TX-
80	PCIEREF+	Fabric Clock A+	91	GE12_TX+	Port8 AMC.2 T3 TX+
79	GND	Logic Ground	92	GND	Logic Ground
78	AMC_CLKB-N	Reserved	93	GE13_RX-	Port 9 AMC.2 T3 RX-
77	AMC_CLKB-P	Reserved	94	GE13_RX+	Port 9 AMC.2 T3 RX+
76	GND	Logic Ground	95	GND	Logic Ground
75	AMC-CLKA-N	Reserved	96	GE13_TX-	Port 9 AMC.2 T3 TX-
74	AMC-CLKA-P	Reserved	97	GE13_TX+	Port 9 AMC.2 T3 TX+
73	GND	Logic Ground	98	GND	Logic Ground
72	P12V_PWR	12V Payload Power	99	GE14_RX-	Port 10 AMC.2 T3 RX-
71	IPMB_SDA_0	IPMB-L Data	100	GE14_RX+	Port 10 AMC.2 T3 RX+
70	GND	Logic Ground	101	GND	Logic Ground
69	PCIE_MCH_RX3-	Port 7 RX- for PCIe	102	GE14_TX-	Port 10 AMC.2 T3 TX-
68	PCIE_MCH_RX3+	Port 7 RX+ for PCIe	103	GE14_TX+	Port 10 AMC.2 T3 TX+
67	GND	Logic Ground	104	GND	Logic Ground
66	PCIE_MCH_TX3-	Port 7 TX- for PCIe	105	NC	Not connected
65	PCIE_MCH_TX3+	Port 7 TX+ for PCIe	106	NC	Not connected
64	GND	Logic Ground	107	GND	Logic Ground
63	PCIE_MCH_RX2-	Port 6 RX- for PCIe	108	NC	Not connected
62	PCIE_MCH_RX2+	Port 6 RX+ for PCIe	109	NC	Not connected
61	GND	Logic Ground	110	GND	Logic Ground
60	PCIE_MCH_TX2-	Port 6 TX- for PCIe	111	NC	Not Connected
59	PCIE_MCH_TX2+	Port 6 TX+ for PCIe	112	NC	Not Connected
58	GND	Logic Ground	113	GND	Logic Ground
57	P12V_PWR	12V Payload Power	114	NC	Not Connected
56	IPMB_SCL_0	IPMB-L Clock	115	NC	Not Connected
55	GND	Logic Ground	116	GND	Logic Ground

Table 3-7: AMC Connector Pin Assignment

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Pin#	Signal	Function	Pin#	Signal	Function
54	PCIE_MCH_RX1-	Port 5 RX- for PCIe	117	RTM_IO13_TX-	RTMIO13 TX-
53	PCIE_MCH_RX1+	Port 5 RX+ for PCIe	118	RTM_IO13_TX+	RTMIO13 TX+
52	GND	Logic Ground	119	GND	Logic Ground
51	PCIE_MCH_TX1-	Port 5 TX- for PCIe	120	RTM_IO13_RX-	RTMIO13 RX-
50	PCIE_MCH_TX1+	Port 5 TX+ for PCIe	121	RTM_IO13_RX+	RTMIO13 RX+
49	GND	Logic Ground	122	GND	Logic Ground
48	PCIE_MCH_RX0-	Port 4 RX- for PCIe	123	RTM_IO14_TX-	RTMIO14 TX-
47	PCIE_MCH_RX0+	Port 4 RX+ for PCIe	124	RTM_IO14_TX+	RTMIO14 TX+
46	GND	Logic Ground	125	GND	Logic Ground
45	PCIE_MCH_TX0-	Port 4 TX- for PCIe	126	RTM_IO14_RX-	RTMIO14 RX-
44	PCIE_MCH_TX0+	Port 4 TX+ for PCIe	127	RTM_IO14_RX+	RTMIO14 RX+
43	GND	Logic Ground	128	GND	Logic Ground
42	P12V_PWR	12V Payload Power	129	RTM_IO15_TX-	RTMIO15 TX-
41	ENABLE-#	AMC Enable	130	RTM_IO15_TX+	RTMIO15 TX+
40	GND	Logic Ground	131	GND	Logic Ground
39	SAS1_RX1-	Port 3 RX- for SAS P1	132	RTM_IO15_RX-	RTMIO15 RX-
38	SAS1_RX1+	Port 3 RX+ for SAS P1	133	RTM_IO15_RX+	RTMIO15 RX+
37	GND	Logic Ground	134	GND	Logic Ground
36	SAS1_TX1-	Port 3 TX- for SAS P1	135	NC	Not Connected
35	SAS1_TX1+	Port 3 TX+ for SAS P1	136	NC	Not Connected
34	GND	Logic Ground	137	GND	Logic Ground
33	SATA1_RX0-	Port 2 RX- for SATA P1	138	NC	Not Connected
32	SATA1_RX0+	Port 2 RX+ for SATA1	139	NC	Not Connected
31	GND	Logic Ground	140	GND	Logic Ground
30	SATA_TX0-	Port 2 TX- for SATA	141	RTM_IO17_TX-	RTMIO17 TX-
29	SATA_TX0+	Port 2 TX+ for SATA	142	RTM_IO17_TX+	RTMIO17 TX+
28	GND	Logic Ground	143	GND	Logic Ground
27	P12V_PWR	12V Payload Power	144	RTM_IO17_RX-	RTMIO17 RX-
26	GA2	Geographic Addr. 2	145	RTM_IO17_RX+	RTMIO17 RX+
25	GND	Logic Ground	146	GND	Logic Ground
24	LAN_A_SRDS_RXB-	Port 1 RX- for GbE	147	RTM_IO18_TX-	RTMIO18 TX-

Table 3-6: AMC Module Connector Pin Assignment (cont'd)

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Pin#	Signal	Function	Pin#	Signal	Function
23	LAN_A_SRDS_RXB+	Port 1 RX+ for GbE	148	RTM_IO18_TX+	RTMIO18 TX+
22	GND	Logic Ground	149	GND	Logic Ground
21	LAN_A_SRDS_TXB-	Port 1 TX- for GbE	150	RTM_IO18_RX-	RTMIO18 RX-
20	LAN_A_SRDS_TXB+	Port 1 TX+ for GbE	151	RTM_IO18_RX+	RTMIO18 RX+
19	GND	Logic Ground	152	GND	Logic Ground
18	P12V_PWR	12V Payload Power	153	RTM_IO19_TX-	RTMIO19 TX-
17	GA1	Geographic Addr.1	154	RTM_IO19_TX+	RTMIO19 TX+
16	GND	Logic Ground	155	GND	Logic Ground
15	LAN_A_SRDS_RXA-	Port 0 RX- for GbE	156	RTM_IO19_RX-	RTMIO19 RX-
14	LAN_A_SRDS_RXA+	Port 0 RX+ for GbE	157	RTM_IO19_RX+	RTMIO19 RX+
13	GND	Logic Ground	158	GND	Logic Ground
12	LAN_A_SRDS_TXA-	Port 0 TX- for GbE	159	RTM_IO20_TX-	RTMIO20 TX-
11	LAN_A_SRDS_TXA+	Port 0 TX+ for GbE	160	RTM_IO20_TX+	RTMIO20 TX+
10	GND	Logic Ground	161	GND	Logic Ground
9	P12V_PWR	12V Payload Power	162	RTM_IO20_RX-	RTMIO20 RX-
8	NC	Not Connected	163	RTM_IO20_RX+	RTMIO20 RX+
7	GND	Logic Ground	164	GND	Logic Ground
6	NC	Not Connected	165	TCK	JTAG Test Clock Input
5	GA0	Geographic Addr. 0	166	TMS	JTAG Test Mode Select In
4	P3V3_MP	+3.3V Mgmt. Power	167	TRST#	JTAG Test Reset Input
3	PS1#	Presence 1	168	TDO	JTAG Test Data Output
2	P12V_PWR	12V Payload Power	169	TDI	JTAG Test Data Input
1	GND	Logic Ground	170	GND	Logic Ground

Table 3-6: AMC Module Connector Pin Assignment (cont'd)

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3.5 Switches

Switches SW4, SW5 and SW6 are for debugging purposes. For normal operation, leave the switches in their default settings.



Figure 3-4: SW4 and SW5 location

SW4

SW4	Pin 1	Pin 2	Pin 3	Pin 4
Default Setting	ON	OFF	ON	ON

- Pin 1: N/C
- Pin 2: ON for Standalone Mode / OFF for Normal Mode
- Pin 3: Reserved
- Pin 4: Reserved

SW5

SW5	Pin 1	Pin 2	Pin 3	Pin 4
Default Setting	OFF	OFF	OFF	OFF

- Pin 1: ON for FWE pin protection / OFF for Normal operation
- Pin 2: ON for Slave SPI / OFF for Master SPI
- Pin 3: IMPC MODE SELECT
- Pin 4: ON for Program IPMC / OFF for Normal operation

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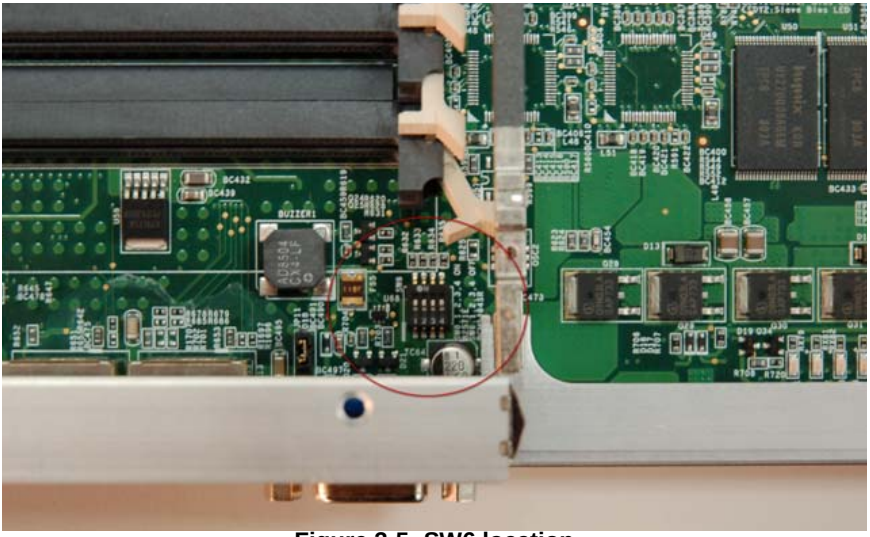


Figure 3-5: SW6 location

SW6

SW6	Pin 1	Pin 2	Pin 3	Pin 4
aTCA-6900	ON	ON	ON	ON
aTCA-6900S	OFF	OFF	ON	ON

- Pin 1: ON 82571EB (AA) to RJ45 / OFF BCM5464 (1) to RJ45
- Pin 2: ON 82571EB (AB) to RJ45 / OFF BCM5464 (2) to RJ45
- Pin 3: ON 82571EB (BA) to BCH1 / OFF BCM5464 (3) to BCH1
- Pin 4: ON 82571EB (BB) to BCH2 / OFF BCM5464 (4) to BCH2

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4 Hardware Platform Management

4.1 Platform Management Overview

The purpose of the hardware platform management system is to monitor, control, and assure proper operation of AdvancedTCA® Boards and other Shelf components. The hardware platform management system watches over the basic health of the system, reports anomalies, and takes corrective action when needed. The hardware platform management system can retrieve inventory information and sensor readings as well as receive event reports and failure notifications from Boards and other Intelligent FRUs. The hardware platform management system can also perform basic recovery operations such as power cycle or reset of managed entities.

The IPMC controller on the aTCA-6900 supports an “intelligent” hardware management system, based on the Intelligent Platform Management Interface Specification. The hardware management system provides the ability to manage the power, cooling, and interconnect needs of intelligent devices; to monitor events; and to log events to a central repository.

4.2 IPMI Sensors

Following table lists all the sensors supported by the aTCA-6900.

Item	Sensor Name	Sensor Address	Description
(1)	Hotswap	(0x0)	FRU Hotswap Sensor. Please refer to section 4.2.1
(2)	Shelf FRU Hotswap	(0x1)	FRU Hotswap Sensor. Please refer to section 4.2.1
(3)	Hot Swap AMC 1	(0x2)	AMC#1 Hotswap Sensor. Please refer to section 4.2.1
(4)	Hot Swap AMC 2	(0x3)	AMC#2 Hotswap Sensor. Please refer to section 4.2.1
(5)	Hot Swap AMC 3	(0x4)	RTM Hotswap Sensor. Please refer to section 4.2.1

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Item	Sensor Name	Sensor Address	Description
(6)	+5.0V	(0x5)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 5.5 Volts Upper Critical Threshold = 5.4 Volts Upper Non-Critical Threshold = 5.3 Volts Lower Non-Critical Threshold = 4.7 Volts Lower Critical Threshold = 4.6 Volts Lower Non-Recoverable Threshold = 4.5 Volts
(7)	+3.3V	(0x6)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 3.63 Volts Upper Critical Threshold = 3.564 Volts Upper Non-Critical Threshold = 3.498 Volts Lower Non-Critical Threshold = 3.102 Volts Lower Critical Threshold = 3.036 Volts Lower Non-Recoverable Threshold = 2.97 Volts
(8)	+1.8V	(0x7)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 1.98 Volts Upper Critical Threshold = 1.944 Volts Upper Non-Critical Threshold = 1.908 Volts Lower Non-Critical Threshold = 1.692 Volts Lower Critical Threshold = 1.656 Volts Lower Non-Recoverable Threshold = 1.62 Volts
(9)	+1.5V	(0x8)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 1.65 Volts Upper Critical Threshold = 1.62 Volts Upper Non-Critical Threshold = 1.59 Volts Lower Non-Critical Threshold = 1.41 Volts Lower Critical Threshold = 1.38 Volts Lower Non-Recoverable Threshold = 1.35 Volts
(10)	+1.2V	(0x9)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 1.32 Volts Upper Critical Threshold = 1.296 Volts Upper Non-Critical Threshold = 1.272 Volts Lower Non-Critical Threshold = 1.034 Volts Lower Critical Threshold = 1.012 Volts Lower Non-Recoverable Threshold = 0.99 Volts
(11)	IPMB Physical	(0xa)	Physical IPMB Sensor. Please refer to section 4.2.2

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Item	Sensor Name	Sensor Address	Description
(12)	W83627 OVT	(0xb)	Discrete Sensor(Normal:0x0001, Abnormal:0x0002) OVT#/SMI#: Can create interrupts that depend on the temperatures measured by SYSTIN and CPUTIN. This mode is enabled by setting THYST (Temperature Hysteresis) to 127°C.
(13)	SIO THERM	(0xc)	Discrete Sensor(Normal:0x0001, Abnormal:0x0002) Same as W83627 OVT.
(14)	SIO WDT	(0xd)	Discrete Sensor(Normal:0x0001, Abnormal:0x0002) Watchdog timer output signal. The time-out counter ranges from 1 to 255 minutes in the minute mode, or 1 to 255 seconds in the second mode.
(15)	ICH THRM	(0xe)	Discrete Sensor(Normal:0x0001, Abnormal:0x0002) Thermal Alarm: Active low signal generated by external hardware to generate an SMI# or SCI.
(16)	CPU THERMTRIP	(0xf)	Discrete Sensor(Normal:0x0001, Abnormal:0x0002) Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a temperature beyond which permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermal sensor.
(17)	FSB FERR	(0x10)	Discrete Sensor(Normal:0x0001, Abnormal:0x0002) FERR# (floating-point error) is qualified by STPCLK#. When STPCLK# is not asserted, FERR# indicates a floating-point error and will be asserted when the processor detects an unmasked floating-point error. When STPCLK# is not asserted, FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR# indicates that the processor has a pending break event waiting for service. The assertion of FERR# indicates that the processor should be returned to the Normal state.

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Item	Sensor Name	Sensor Address	Description
(18)	FSB IERR	(0x11)	Discrete Sensor(Normal:0x0001, Abnormal:0x0002) IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor FSB. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#.
(19)	SYS PWROK	(0x12)	Discrete Sensor(Normal:0x0002, Abnormal:0x0001) PWROK is asserted by a processor as the result of a power fail.
(20)	BMC Watchdog	(0x14)	Watchdog Timer Sensor. Please refer to section 4.2.3
(21)	Version change	(0x15)	Version Change Sensor. Please refer to section 4.2.4
(22)	LM75 SYS Temp	(0x16)	System Temperature. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 95 °C Upper Critical Threshold = 75 °C Upper Non-Critical Threshold = 60 °C
(23)	CPU0 Temp	(0x17)	CPU Temperature. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 100 °C Upper Critical Threshold = 80 °C Upper Non-Critical Threshold = 65 °C
(24)	CPU1 Temp	(0x18)	CPU Temperature. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 100 °C Upper Critical Threshold = 80 °C Upper Non-Critical Threshold = 65 °C

Table 4-1: aTCA-6900 IPMI Sensors

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4.2.1 Get Sensor Reading (FRU Hotswap Sensor)

	Byte	Data field
Request data	1	Sensor Number (FFh = reserved)
Response data	1	Completion Code
	2	Sensor Reading. [7:0] - Not used. Write as 00h.
	3	Standard IPMI byte (See “Get Sensor Reading” in IPMI specification): [7] - 0b = All Event Messages disabled from this sensor [6] - 0b = sensor scanning disabled [5] - 1b = initial update in progress. This bit is set to indicate that a “Re-arm Sensor Events” or “Set Event Receiver” command has been used to request an update of the sensor status, and that update has not occurred yet. Software should use this bit to avoid getting an incorrect status while the first sensor update is in progress. This bit is only required if it is possible for the IPM Controller to receive and process a “Get Sensor Reading or Get Sensor Event Status” command for the sensor before the update has completed. This is most likely to be the case for sensors, such as fan RPM sensors, that may require seconds to accumulate the first reading after a re-arm. [4:0] – reserved. Ignore on read.
	4	Current State Mask [7] – 1b = FRU Operational State M7 - Communication Lost [6] – 1b = FRU Operational State M6 - FRU Deactivation In Progress [5] – 1b = FRU Operational State M5 - FRU Deactivation Request [4] – 1b = FRU Operational State M4 - FRU Active [3] – 1b = FRU Operational State M3 - FRU Activation in Progress [2] – 1b = FRU Operational State M2 - FRU Activation Request [1] – 1b = FRU Operational State M1 - FRU Inactive [0] – 1b = FRU Operational State M0 - FRU Not Installed
	5	[7:0] – Optional/Reserved. If provided, write as 80h (IPMI restriction). Ignore on read.

Table 4-2: Get Sensor Reading (FRU Hotswap Sensor)

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4.2.2 Get Sensor Reading (Physical IPMB-0 Sensor)

	Byte	Data field
Request data	1	Sensor Number (FFh = reserved)
Response data	1	Completion Code
	2	Sensor Reading. [7:0] - Not used. Write as 00h.
	3	Standard IPMI byte (See “Get Sensor Reading” in IPMI specification): [7] - 0b = All Event Messages disabled from this sensor [6] - 0b = sensor scanning disabled [5] - 1b = initial update in progress. This bit is set to indicate that a “Re-arm Sensor Events” or “Set Event Receiver” command has been used to request an update of the sensor status, and that update has not occurred yet. Software should use this bit to avoid getting an incorrect status while the first sensor update is in progress. This bit is only required if it is possible for the IPM Controller to receive and process a “Get Sensor Reading or Get Sensor Event Status” command for the sensor before the update has completed. This is most likely to be the case for sensors, such as fan RPM sensors, that may require seconds to accumulate the first reading after a re-arm. [4:0] – reserved. Ignore on read.
	4	Current State Mask [7] – 1b = FRU Operational State M7 - Communication Lost [6] – 1b = FRU Operational State M6 - FRU Deactivation In Progress [5] – 1b = FRU Operational State M5 - FRU Deactivation Request [4] – 1b = FRU Operational State M4 - FRU Active [3] – 1b = FRU Operational State M3 - FRU Activation in Progress [2] – 1b = FRU Operational State M2 - FRU Activation Request [1] – 1b = FRU Operational State M1 - FRU Inactive [0] – 1b = FRU Operational State M0 - FRU Not Installed
	5	[7:0] – Optional/Reserved. If provided, write as 80h (IPMI restriction). Ignore on read.

Table 4-3: Get Sensor Reading (Physical IPMB-0 Sensor)

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4.2.3 Watchdog Timer Sensor

Sensor Type	Sensor Type Code	Sensor Specific Offset	Event
Watchdog 2	23h		This sensor is recommended for new IPMI v1.0 and later implementations.
		00h	Timer expired, status only (no action, no interrupt)
		01h	Hard Reset
		02h	Power Down
		03h	Power Cycle
		04h-07h	reserved
		08h	Timer interrupt
			The Event Data 2 field for this command can be used to provide an event extension code, with the following definition: 7:4 interrupt type 0h = none 1h = SMI 2h = NMI 3h = Messaging Interrupt Fh = unspecified all other = reserved 3:0 timer use at expiration: 0h = reserved 1h = BIOS FRB2 2h = BIOS/POST 3h = OS Load 4h = SMS/OS 5h = OEM Fh = unspecified all other = reserved

Table 4-4: Watchdog Timer Sensor

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4.2.4 Version Change Sensor

Sensor Type	Sensor Type Code	Sensor Specific Offset	Event
Version Change	2Bh	00h	00h Hardware change detected with associated Entity. Informational. This offset does not imply whether the hardware change was successful or not. Only that a change occurred.
		01h	01h Firmware or software change detected with associated Entity.Informational. Success or failure not implied.
		02h	02h Hardware incompatibility detected with associated Entity.
		03h	03h Firmware or software incompatibility detected with associated Entity.
		04h	04h Entity is of an invalid or unsupported hardware version.
		05h	05h Entity contains an invalid or unsupported firmware or software version.
		06h	06h Hardware Change detected with associated Entity was successful. (deassertion event means unsuccessful').
		07h	07h Software or F/W Change detected with associated Entity was successful. (deassertion event means 'unsuccessful')
			Event data 2 can be used for additional event information on the type of version change - see definition below

Table 4-5: Version Change Sensor

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Event Data 2

7:0 Version change type

- 00h unspecified
- 01h management controller device ID (change in one or more fields from ‘Get Device ID’)
- 02h management controller firmware revision
- 03h management controller device revision
- 04h management controller manufacturer ID
- 05h management controller IPMI version
- 06h management controller auxiliary firmware ID
- 07h management controller firmware boot block
- 08h other management controller firmware
- 09h system firmware (EFI / BIOS) change
- 0Ah SMBIOS change
- 0Bh operating system change
- 0Ch operating system loader change
- 0Dh service or diagnostic partition change
- 0Eh management software agent change
- 0Fh management software application change
- 10h management software middleware change
- 11h programmable hardware change (e.g. FPGA)
- 12h board/FRU module change (change of a module plugged into associated entity)
- 13h board/FRU component change (addition or removal of a replaceable component on the board/FRU that is not tracked as a FRU)
- 14h board/FRU replaced with equivalent version
- 15h board/FRU replaced with newer version
- 16h board/FRU replaced with older version
- 17h board/FRU hardware configuration change (e.g. strap, jumper, cable change, etc.)

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4.2.5 Get Sensor Reading Command

	Byte	Data field
Request data	1	Sensor Number (FFh = reserved)
Response data	1	Completion Code
	2	Sensor reading Byte 1: byte of reading. Ignore on read if sensor does not return an numeric (analog) reading.
	3	[7] - 0b = All Event Messages disabled from this sensor [6] - 0b = sensor scanning disabled [5] - 1b = reading/state unavailable (formerly “initial update in progress”). This bit is set to indicate that a ‘re-arm’ or ‘Set Event Receiver’ command has been used to request an update of the sensor status, and that update has not occurred yet. Software should use this bit to avoid getting an incorrect status while the first sensor update is in progress. This bit is only required if it is possible for the controller to receive and process a ‘Get Sensor Reading’ or ‘Get Sensor Event Status’ command for the sensor before the update has completed. This is most likely to be the case for sensors, such as fan RPM sensors, that may require seconds to accumulate the first reading after a re-arm. The bit is also used to indicate when a reading/state is unavailable because the management controller cannot obtain a valid reading or state for the monitored entity, typically because the entity is not present. See *PICMG Specification 3.0, Section 16.4, Event Status, Event Conditions, and Present State* and *Section 16.6, Re-arming* for more information. [4:0] - reserved. Ignore on read.

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	Byte	Data field
Response data (con't)	4	For threshold-based sensors Present threshold comparison status [7:6] - reserved. Returned as 1b. Ignore on read. [5] - 1b = at or above () upper non-recoverable threshold [4] - 1b = at or above () upper critical threshold [3] - 1b = at or above () upper non-critical threshold [2] - 1b = at or below () lower non-recoverable threshold [1] - 1b = at or below () lower critical threshold [0] - 1b = at or below () lower non-critical threshold For discrete reading sensors [7] - 1b = state 7 asserted [6] - 1b = state 6 asserted [5] - 1b = state 5 asserted [4] - 1b = state 4 asserted [3] - 1b = state 3 asserted [2] - 1b = state 2 asserted [1] - 1b = state 1 asserted [0] - 1b = state 0 asserted
	(5)	For discrete reading sensors only. (Optional) (00h Otherwise) [7] - reserved. Returned as 1b. Ignore on read. [6] - 1b = state 14 asserted [5] - 1b = state 13 asserted [4] - 1b = state 12 asserted [3] - 1b = state 11 asserted [2] - 1b = state 10 asserted [1] - 1b = state 9 asserted [0] - 1b = state 8 asserted

Table 4-6: Get Sensor Reading Command

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4.3 IPMI Commands

Following table present all the commands which are supported by the aTCA-6900 in different interfaces and compatible with IPMI v1.5 and PICMG 3.0 R2.0 ECN001. There are four interfaces are implemented with IPMI command support.

(1) SDI: serial debug interface
(2) SPI: serial payload interface
(3) KCS: OpenIpmi
(4) IPMB0: IPMBa & IPMBb

	SDI	SPI	KCS	IPMB0
IPMI Commands				
IPM Device "Global" Commands				
Get Device ID	x	x	x	x
Cold Reset	x	x	x	x
Warm Reset	x	x	x	x
Get Self Test Results	x	x	x	x
Get Device GUID	x	x	x	x
IPMI Messaging Support Commands				
Set BMC Global Enables	x	x	x	x
Get BMC Global Enables	x	x	x	x
Clear Message Flags	x	x	x	x
Get Message Flags	x	x	x	x
Get Message	x	x	x	x
Send Message	x	x	x	x
Master Write-Read	x	x	x	x
BMC Watchdog Timer				
Reset Watchdog Timer	x	x	x	x
Set Watchdog Timer	x	x	x	x
Get Watchdog Timer	x	x	x	x
Event Commands				
Set Event Receiver	x	x	x	x
Get Event Receiver	x	x	x	x
Platform Event	x	x	x	x

Table 4-7: Supported IPMI Commands

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	SDI	SPI	KCS	IPMB0
Sensor Device Commands				
Get Device SDR Info	x	x	x	x
Get Device SDR	x	x	x	x
Reserve Device SDR Repository	x	x	x	x
Get Sensor Reading Factors	x	x	x	x
Set Sensor Hysteresis	x	x	x	x
Get Sensor Hysteresis	x	x	x	x
Set Sensor Threshold	x	x	x	x
Get Sensor Threshold	x	x	x	x
Set Sensor Event Enable	x	x	x	x
Get Sensor Event Enable	x	x	x	x
Rearm Sensor Events	x	x	x	x
Get Sensor Event Status	x	x	x	x
Get Sensor Reading	x	x	x	x
FRU Device Commands				
Get FRU Inventory Area Info	x	x	x	x
Read FRU Data	x	x	x	x
Write FRU Data	x	x	x	x
PICMG Commands				
HPM.1 Upgrade Commands (HPM.1)				
Get target upgrade capabilities	x	x	x	x
Get component properties	x	x	x	x
Abort Firmware Upgrade	x	x	x	x
Initiate upgrade action	x	x	x	x
Upload firmware block	x	x	x	x
Finish firmware upload	x	x	x	x
Get upgrade status	x	x	x	x
Activate firmware	x	x	x	x
Query Self-test Results	x	x	x	x
Query Rollback status	x	x	x	x
Initiate Manual Rollback	x	x	x	x

Table 4-7 (cont'd): Supported IPMI Commands

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	SDI	SPI	KCS	IPMB0
AdvancedTCA				
Get PICMG Properties	x	x	x	x
Get Address Info	x	x	x	x
FRU Control	x	x	x	x
FRU Control Capabilities	x	x	x	x
Get FRU LED Properties	x	x	x	x
Get LED Color Capabilities	x	x	x	x
Set FRU LED State	x	x	x	x
Get FRU LED State	x	x	x	x
Set IPMB State	x			x
Set FRU Activation Policy	x	x	x	x
Get FRU Activation Policy	x	x	x	x
Set FRU Activation	x	x	x	x
Get Device Locator Record ID	x	x	x	x
Get Port State	x	x	x	x
Set Port State	x			x
Compute Power Properties	x			x
Set Power Level	x			x
Get Power Level	x	x	x	x
Bused Resource Control	x			x
Get IPMB Link Info	x	x	x	x
SET_CLOCK_STATE	x	x	x	x
GET_CLOCK_STATE	x	x	x	x
Get AMC-Port State	x			x
Set AMC-Port State	x			x

Table 4-7 (cont'd): Supported IPMI Commands

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4.4 IPMI Firmware Upgrade Procedure

The processor can communicate with the IPMC by Keyboard Controller Style (KCS), and an upgrade tool for DOS environment to upgrade the IPMC firmware is provided on the ADLINK All-in-One CD or can be downloaded from the ADLINK website. Please follow the procedures below to upgrade the IPMC firmware.

1. Copy the upgrade tool for DOS into a bootable USB flash drive, and change the boot order setting in BIOS so that the USB flash drive is the first boot device.

```
C:\IPMC\AT6900>dir/w

 Volume in drive C has no label
 Volume Serial Number is 0065-1CB9
 Directory of C:\IPMC\AT6900

[.]      [..]        README.DOC    [TESTTOOL]    [UPGRADE]
         1 file(s)      2,185,216 bytes
         4 dir(s)     863,748,096 bytes free

C:\IPMC\AT6900>cd upgrade

C:\IPMC\AT6900\UPGRADE>dir/w

 Volume in drive C has no label
 Volume Serial Number is 0065-1CB9
 Directory of C:\IPMC\AT6900\UPGRADE

[.]      [..]     A314.IMG     CWSDPMI.EXE    CWSDPR0.EXE
CWSPARAM.EXE    HPMDOS.EXE      UPGRADE.BAT
         7 file(s)        884,350 bytes
         2 dir(s)     863,748,096 bytes free

C:\IPMC\AT6900\UPGRADE>
```

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2. Execute **upgrade.bat**. This tool will upgrade the IPMC firmware automatically. After the firmware has been upgraded successfully, please do a power cycle or remove the blade from the chassis and reinsert.

```
C:\IPMC\AT6900\UPGRADE>upgrade.bat

C:\IPMC\AT6900\UPGRADE>CWSDPMI.EXE -s-
CWSDPMI V0.90+ (r4) Copyright (C) 1997 CW Sandmann
     ABSOLUTELY NO WARRANTY

C:\IPMC\AT6900\UPGRADE>hpmdos.exe -I KCS -F A314.img
     upgrade
Adlink HPH.1 DOS Upgrade Agent
Update HPM.1 components using PICMG HPM.1 file
Validating firmware image integrity...OK
Performing preparation stage...OK
    Services may be affected during upgrade. Do you wish
     to continue? y/n
    Target Product ID     : 6900
    Target Manufacturer ID: 005f13
Performing upgrade stage:    Upgrading H8S-AMCc F/W
    with Version: Major: 1
                  Minor: 51
                  Aux  : a3 00 00 14
    Writing firmware: 100 % completed

Firmware upgrade procedure successful
Upgrade successful, please shutdown and boot system
HPM.1 upgrade succeed!!
```

3. Goto the \TESTTOOL directory and execute TEST.BAT. This tool will list all the sensors on the aTCA-6900, and “Auxiliary Firmware Revision Information: a3000005” indicates the firmware version is a3000005.

```
C:\IPMC\AT6900\TESTTOOL>dir/w

 Volume in drive C has no label
 Volume Serial Number is 0065-1CB9
 Directory of C:\IPMC\AT6900\TESTTOOL

[.]      [..]       INFO.INI      IPMITEST.EXE   TEST.BAT
```

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```
IPMITOOL v 2.0.1 03/17/2008 - IPMI toolkit for Terminal
     mode.
Copyright(c) 2006. All Rights Reserved
FOR PRODUCTS WITH PICMG 2.9(CPCI) CAPABILITY ONLY.
DO NOT RUN THIS PROGRAM UNDER WINDOWS NT, 2000, OR XP.
Please Press any key to continue.
############################################################

[#]Check IPMC status .....[OK]
        Product Name: aTCA-6900
        Firmware Version: V1.51
[#]Check Development status .....OK
       Auxiliary Firmware Revision Information : a3000005
[#]Check KCS status .....OK
[#] Check IPMB addr .....        (IPMB addr: 0x80)
[#] FRU Information .....
        Board product Name: aTCA6900
        Board FRU ID: FRU-OP1 V1.1
###### Press any key to continue ######
01.Hot Swap [00] .....Status OK
02.ShelfFRU HotSwap [01] .....Status OK
03.Hot Swap AMC 1 [02] .....Status OK
04.IPMB Physical [0A] .....Status OK
05.BMC Watchdog [14] .....Status OK
06.Version change [15] .....Status OK
07.+5.0V [05] .....RAW Data(D1) 5.104 V ....Status OK
08.+3.3V [06] .....RAW Data(D1) 3.367 V ....Status OK
09.+1.8V [07] .....RAW Data(B7) 1.789 V ....Status OK
10.+1.5V [08] .....RAW Data(98) 1.485 V ....Status OK
10.+1.5V [08] .....RAW Data(98) 1.485 V ....Status OK
12.LM75 SYS Temp [16] .....RAW Data(A0) 32.000 C
     ....Status OK
13.W83627 OVT [0B] .....Status OK
14.SIO THERM [0C] .....Status OK
15.SIO WDT [0D] .....Status OK
16.ICH THRM [0E] .....Status OK
17.CPU THERMTRIP [0F] .....Status OK
18.FSB FERR [10] .....Status OK
19.FSB IERR [11] .....Status OK
20.SYS PWROK [12] .....Status OK
21.CPU0 Temp [17] .....RAW Data(21) 33.000 C ...Status OK
22.CPU1 Temp [18] .....RAW Data(1C) 28.000 C ...Status OK
23.Hot Swap [00] .....Status OK
```

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5 Getting Started

The aTCA-6900 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

5.1 Safety Requirements

The following safety precautions must be observed when installing or operating the aTCA-6900. ADLINK assumes no responsibility for any damage resulting from failure to comply with these requirements.

Exercised due care when handling the board as the heat sink can get very hot. Do not touch the heat sink when installing or removing the board. The board should not be placed on any surface or in any form of storage container until the board and heat sink have cooled down to room temperature.

If your board type is not specifically qualified as being hot swap capable, switch off the system power before installing the board in a free slot. Failure to do so could endanger your life or health and may damage your board or system.

Certain modules require bus master and/or Rear I/O capability. If you are in doubt whether such features are required for the board you intend to install, please check your specific board and/or system documentation to make sure that your system is provided with an appropriate free slot in which to insert the board.

This ATCA blade contains electrostatic sensitive devices. Please observe the necessary precautions to avoid damage to your board:

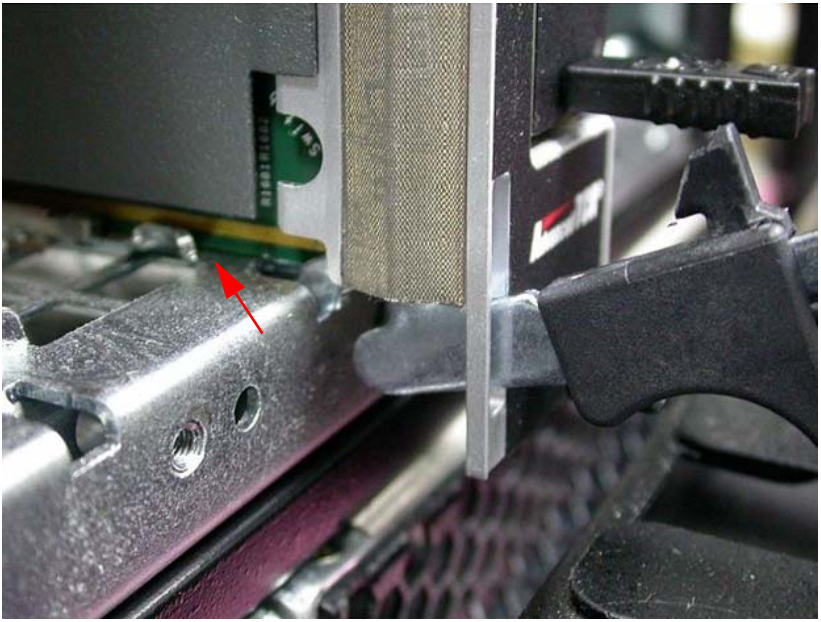
- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

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5.2 Installing the aTCA-6900

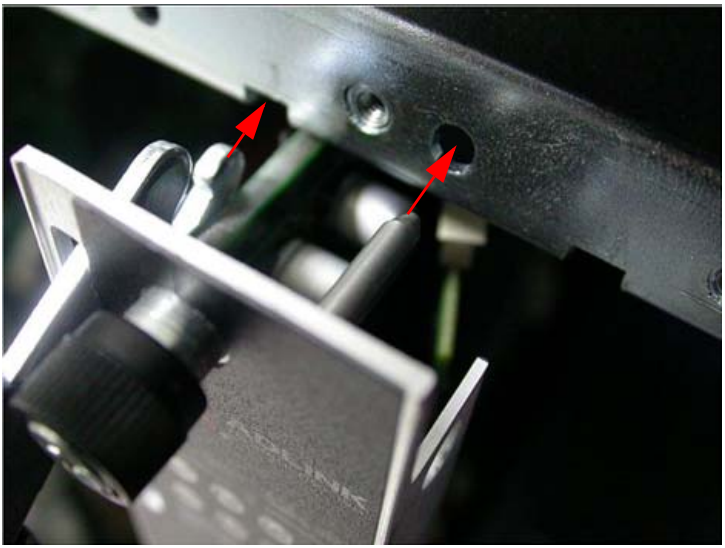
Follow these steps to install the aTCA-6900 to the chassis.

1. Carefully align the board edges with the chassis guide rails and insert the module into the chassis guide rail.



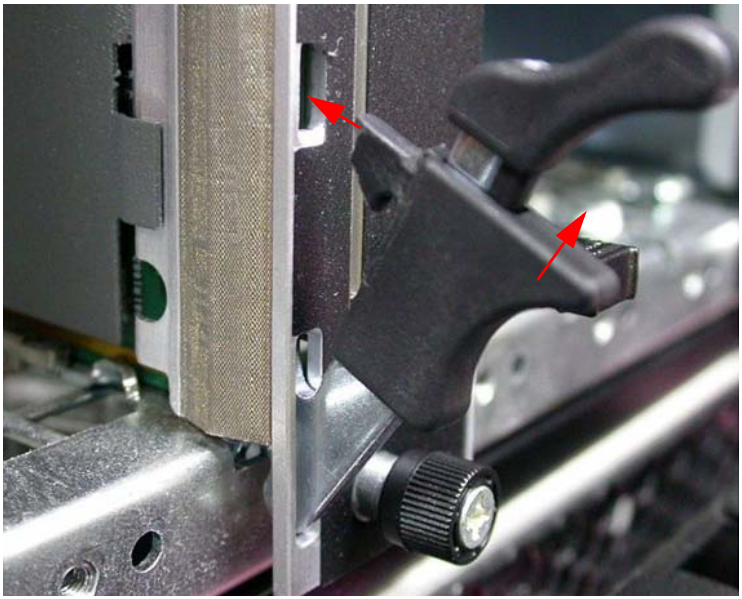
2. Check that the catch hooks and alignment pins at either end of the module are correctly inserted into the proper openings. Push inwards on the handles until the module is firmly seated in the chassis. (Do not force the handles if there is resistance as this may damage the connectors and/or backplane.)

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3. Pinch the ejector to unlock the handle and insert the catch into the faceplate.





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4. Secure the module by tightening the captive screws.



5.3 Removing the aTCA-6900

To remove the aTCA-6890 module, undo the captive screws, pinch the ejector handle release mechanisms and pull outwards on the ejector handles to eject the module from the backplane. Pull the module towards you until it is free of the chassis.

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6 Driver Installation

The drivers for the aTCA-6900 are available on the ADLINK website. Please visit the product website for details: http://www.adlinktech.com.

The following describes the driver installation procedures for Windows® Server 2003

1. Install the Windows operating system before installing any driver. Most standard I/O device drivers are installed during Windows installation.
2. Download the drivers from the website:
   - ▷ Chipset - Intel® Chipset Installation Utility Version
   - ▷ LAN Controller - Intel® PRO/1000 PT Dual Port Server Adapter
   - ▷ SAS Controller - LSI Adapter, SAS 3000 series, 4-port with 1064E
   - ▷ VGA Controller - ATI ES1000, 6.14.10.6553

We recommend using all the drivers provided on the ADLINK All-in-One CD or downloaded from the ADLINK website to ensure driver compatibility. Contact ADLINK to get support for other operating systems.

6.1 Chipset Driver Installation

To install the chipset driver for Windows® Server 2003:

1. Run the InstallShield installation program:
   - ▷ Self-extracting .EXE distribution: INFINST_AUTOL.EXE
   - ▷ Compressed .ZIP distribution: SETUP.EXE
2. You will be prompted to agree to the license agreement. If you do not agree, the installation program will exit before extracting any files.
3. Once the operating system reboots, follow the on-screen instructions and accept default settings to complete the setup.

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6.2 LAN Driver Installation

Download the self-extracting archive, PRO2KXP_v13_3.EXE. When you run it, it will extract the files to a temporary directory, run the installation wizard, and remove the temporary files when the installation is complete. All language files are embedded in this archive. You do not need to download an extra language pack. For the device name shown in the device manager, Please refer to the following.

For the aTCA-6900

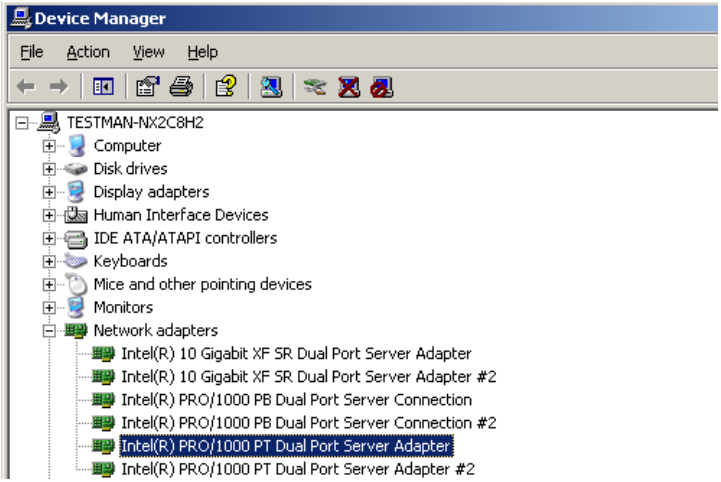
After installing the Intel LAN driver, you will see 6 Network Adapters in the Device Manager:

- Intel 10 Gigabi XF SR Dual Port Server Adapter x2
- 82571EB Intel PRO/1000 PB Dual Port Server Connection x4.

For the aTCA-6900S

After installing the Intel LAN driver you will see 6 6 Network Adapters in the Device Manager:

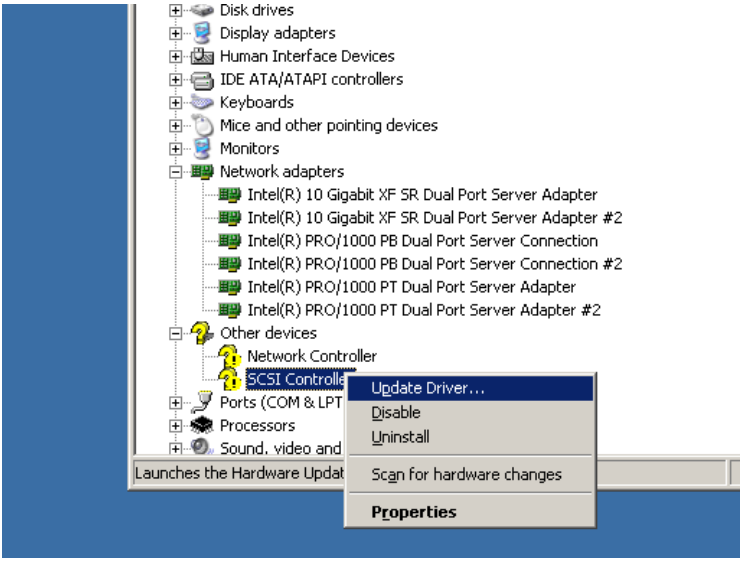
- Intel 10 Gigabi XF SR Dual Port Server Adapter x2
- 82571EB Intel PRO/1000 PT Dual Port Server Connection x4.



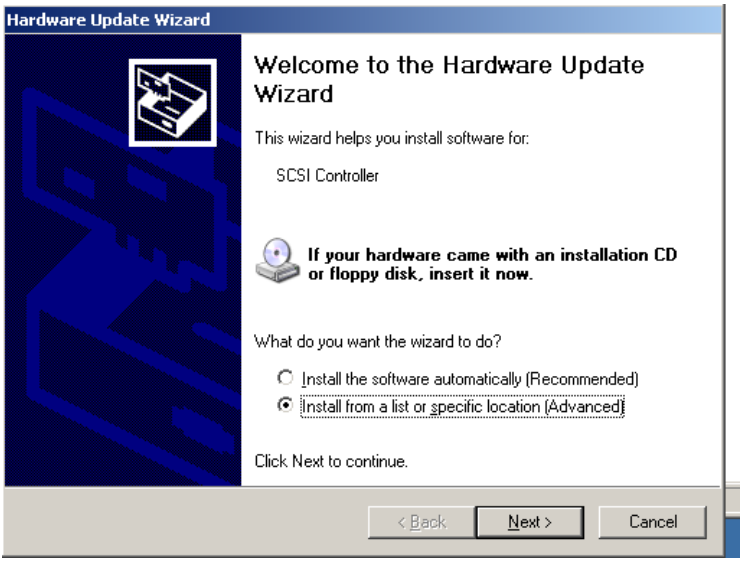
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6.3 LAN Driver Installation

Right-click the mouse on the SCSI Controller in the Device Manager and select *Update Driver*.

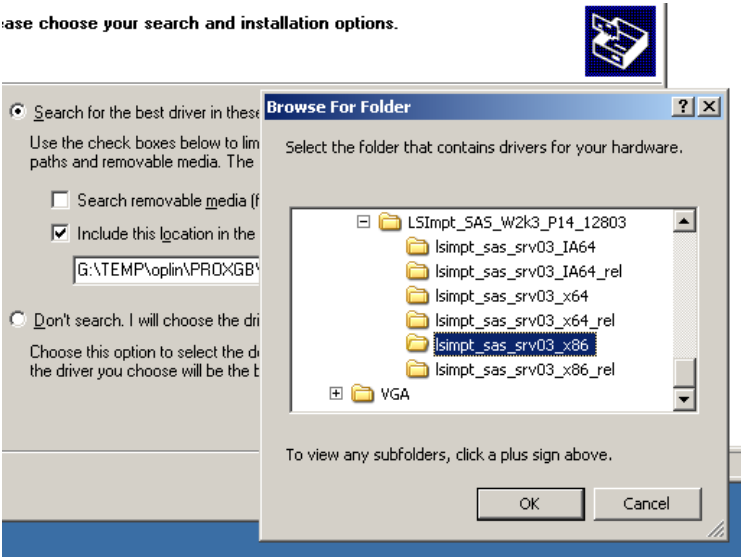


Select *Install from a list or specific location (Advanced)*.

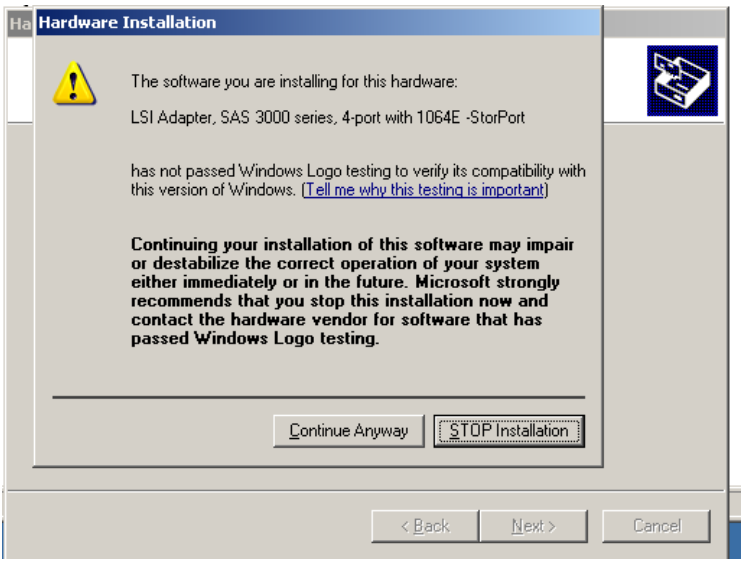


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Navigate to the location *lsimpt_sas_srv03_x86*.

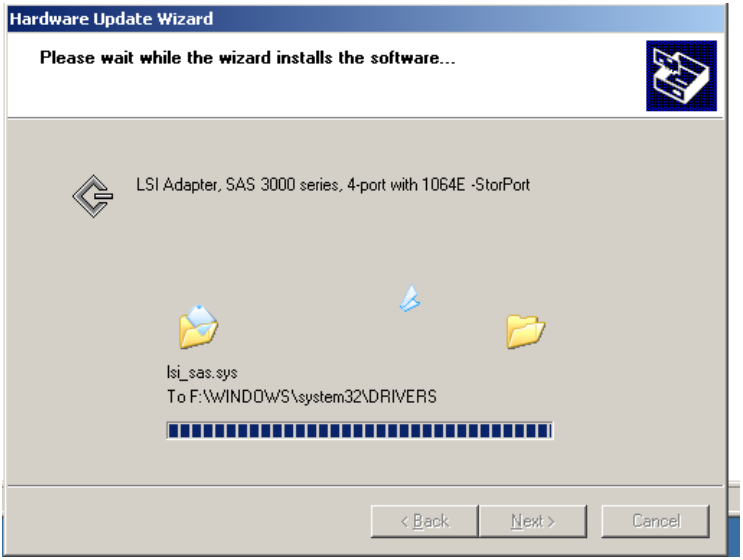


Select *Continue Anyway* when this message pops up.

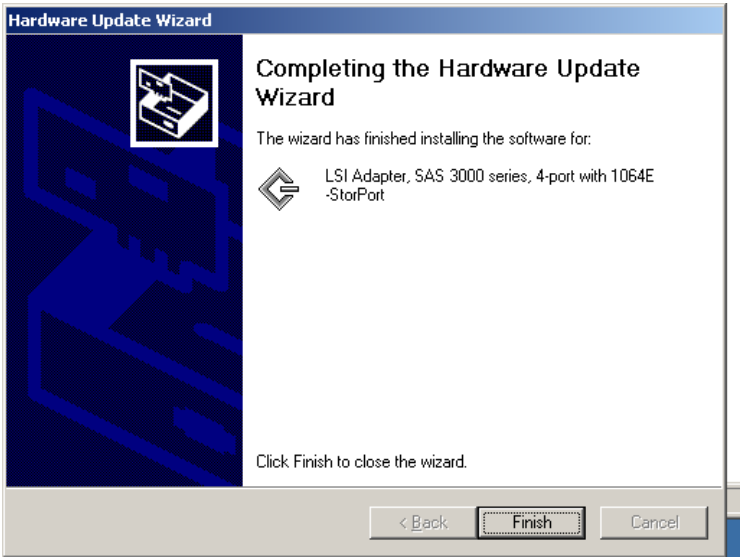


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The *LSI adapter, SAS 3000 series, 4-port with 1064E–StorPort* driver will be installed.

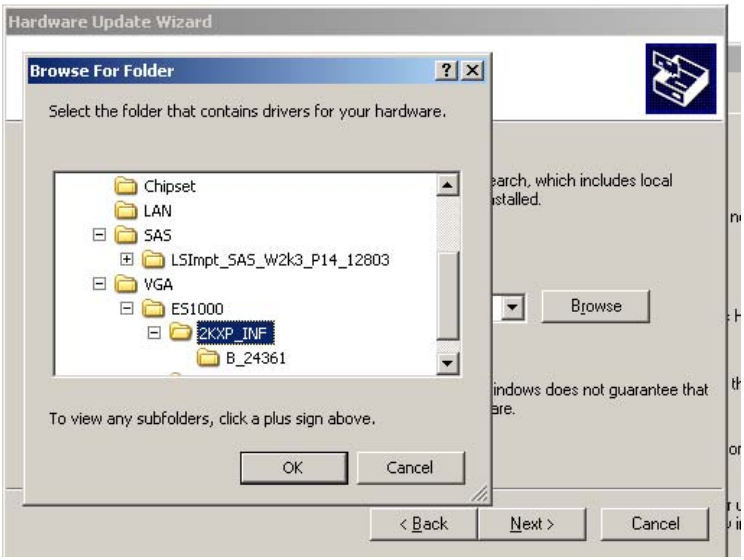


Click *Finish* to complete the installation.

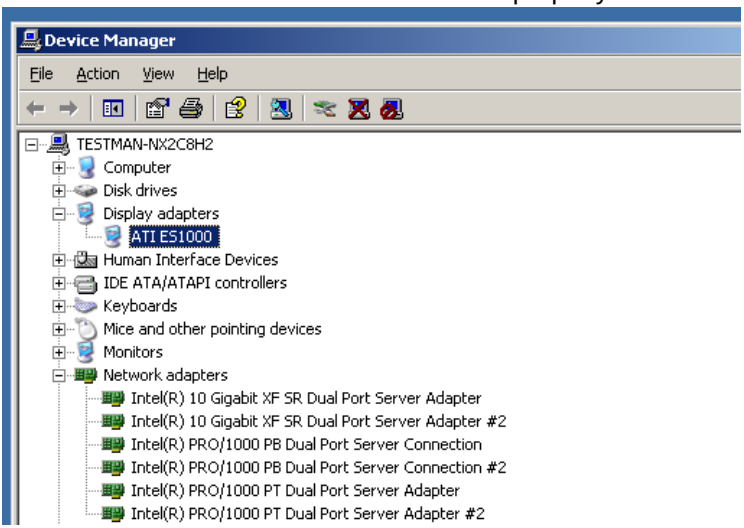


6.4 VGA Driver Installation

Right-click the mouse on the VGA Controller in the Device Manager and select Update Driver. Navigate to the directory *2KXP_INF* for the VGA driver.



Check if the ATI ES1000 driver was installed properly.



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6.5 SDK Installation for Switch (aTCA-6900S)

The Broadcom Software Development Kit (SDK) enables software development for target systems using Broadcom switch devices from the StrataSwitch and StrataXGS families. ADLINK provides the Broadcom SDK Linux Support Package (LSP) to enable switch functions on Linux systems to allow users to quickly utilize the switch device.

The LSP contains three parts: the Linux kernel, building tool-chains and Broadcom SDK compiled binary files. The Broadcom SDK contains kernel modules, user space proxy, RC script files and default VLAN configuration. Please refer to the “Broadcom SDK LSP Installation Guide” downloadable from the aTCA-6900 product page on the ADLINK website for detailed installation procedures. The SDK package is also downloadable from the website.

Please go to **www.adlinktech.com** and search for “aTCA-6900” to find the product page. Click on Associated Software to download the installation guide and SDK package.

Note: The SDK supports Linux OS only. Kernel 2.6.22.19 has been tested with the aTCA-6900S and SDK 5.6.0. The SDK was developed and tested on Red Hat Enterprise Linux (RHEL) 4 update 3, RHEL 5.0, RHEL 5.1, RHEL 5.2.

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7 Watchdog Timer

7.1 Overview

The aTCA-6900 supports a Watchdog Timer function which is built into the Winbond W83627UHG to protect the system from specific software or hardware failures that may cause the system stop responding. The application is first registered with the watchdog device. Once the watchdog device is enabled, the application must periodically send a signal to the watchdog device. If the watchdog device doesn't receive this signal within the set period of time, it will reboot the system or restart the application.

The Watchdog Timer of the W83627UHG consists of an 8-bit programmable time-out counter and a control and status register. The time-out counter ranges from 1 to 255 minutes in the minutes mode, or 1 to 255 seconds in the seconds mode. The mode of the Watchdog Timer counter are selected at Logical Device 8, CR[F5h], bit[3]. The time-out value is set at Logical Device 8, CR[F6]. Writing zero disables the Watchdog Timer function. Writing any non-zero value to this register causes the counter to load this value into the Watchdog Timer counter and start counting down.

The W83627UHG outputs a low signal to the WDTO# (pin 77) when a time-out event occurs. In other words, when the value is counted down to zero, the timer stops, and the W83627UHG sets the WDTO# status bit in Logic Device 8, CR[F7h], bit[4], outputting a low signal to the WDTO# pin (pin 77). Writing a zero will clear the status bit and the WDTO# pin returns to high. This bit will also be cleared if LRESET# or PWROK# signal is asserted.

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7.2 Sample Code

This sample code is provided for testing the Watchdog Timer function of the W83627UHG on the aTCA-6900.

```
#include<stdlib.h>
#include<stdio.h>
#include<string.h>
#include<dos.h>

void WDTRUN(int config_port,int count_value);
void Enter_W627UHG_Config(int config_port);
void Exit_W627UHG_Config(int config_port);

void main(int argc,char *argv[])
{
   int number,DevID1,DevID2,chipflag=0;
   int ioport = 0x4E;//Default config_port = 0x4E

      if((argc==1) || ((argc == 3)&& (*argv[2] != 'i')) ||
      (argc>3))
        {
           printf("ADLINK Watchdog Timer Utility of aTCA-
      6900.\n\n");
           printf("  Usage: WDT6900 value [i]\n");
          printf("        value is from 1 to 15300, the unit is
      second.\n");
           printf("         Write 0 will disable watchdog
      timer.\n\n");
           printf("         i - change IO port to 0x2E. Default
      is 0x4E.\n");
           exit(1);
        }
      else
        {
            if(argc==3) ioport=0x2E;
           //Detect W83627UHG.
             Enter_W627UHG_Config(ioport);

           //Get Chip ID Hi Byte = 0xA2, Chip ID LO Byte = 0x3x
             outportb(ioport, 0x20);
             DevID1 = inportb(ioport+1);
             outportb(ioport, 0x21);
             DevID2 = inportb(ioport+1);

               if((DevID1 == 0xA2) && ((DevID2 & 0xF0) == 0x30))
                  chipflag = 1;
```

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```
            if(chipflag == 0)
              {
               printf("ADLINK Watchdog Timer Utility of aTCA-
      6900.\n\n");
               printf("Can't find any Winbond W83627UHG on
      system!\n");
               Exit_W627UHG_Config(ioport);
               exit(1);
              }
            else
              {
               printf("ADLINK Watchdog Timer Utility of aTCA-
      6900.\n\n");
                 number=atoi(argv[1]);

                 WDTRUN(ioport,number);
                 Exit_W627UHG_Config(ioport);
              }
       }
}

void Enter_W627UHG_Config(int config_port)
{
      outportb(config_port, 0x87);
      outportb(config_port, 0x87);
}
void Exit_W627UHG_Config(int config_port)
{
      outportb(config_port, 0xAA);
}
void WDTRUN(int config_port,int count_value)
{
   int temp;
   int counter;

      //Select WDT device
        outportb(config_port, 0x07);
        outportb(config_port+1, 0x08);//device 8

      //Activate WDT device
        outportb(config_port, 0x30);
        temp = inportb(config_port+1);
        temp = temp | 0x01;
        outportb(config_port+1, temp);

      //Set second/minute mode
        outportb(config_port, 0xF5);
```

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```
        temp = inportb(config_port+1);
        temp = temp & 0xFD;//disable WDTO to KBRST#.
        if(count_value <= 60)
          temp = temp & 0xF7;//second.

      //Count the timeout value
      if(((count_value>60) && (count_value<=15300)) ||
      (count_value > 15300))
        {
          if(count_value > 15300)
            count_value = 15300;
          counter = count_value/60;
          if((count_value%60)>30)
            counter=counter+1;
          printf("WDT timeout in %d minutes.",counter);
          temp = temp | 0x08;//Count in minute mode.
          outportb(config_port+1, temp);
        }
      else
        {
          if(count_value == 0)
            {
            counter = count_value;
            printf("WDT is Disabled.");
            }
          else
            {
            counter = count_value;
            printf("WDT timeout in %d seconds.",counter);
            outportb(config_port+1, temp);
              }
            }

      //reset WDT by KB, MS interrupt
        outportb(config_port, 0xF7);
        temp = inportb(config_port + 1);
        temp = temp | 0xC0;//Bit 6 = KB interrupt, Bit 7 = MS
      interrupt
        outportb(config_port+1, temp);
      //Write count value
        outportb(config_port, 0xF6);
        outportb(config_port+1, counter);
}
```

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8 BIOS Setup

The following chapter describes basic navigation for the AMIBIOS®8 BIOS setup utility.

8.1 Starting the BIOS

To enter the setup screen, follow these steps:

1. Power on the motherboard
2. Press the < Delete > key on your keyboard when you see the following text prompt:
   < Press DEL to run Setup >
3. After you press the < Delete > key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu, such as Chipset and Power menus.



Note: In most cases, the < Delete > key is used to invoke the setup screen. There are several cases that use other keys, such as < F1 >, < F2 >, and so on.

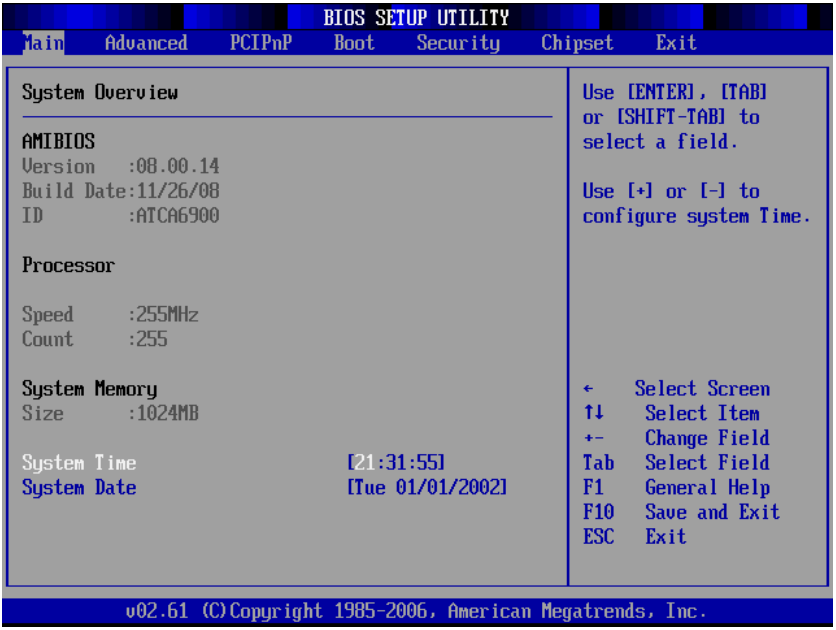
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Setup Menu

The main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in this user's guide.

The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed" options cannot be configured, "Blue" options can be.

The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

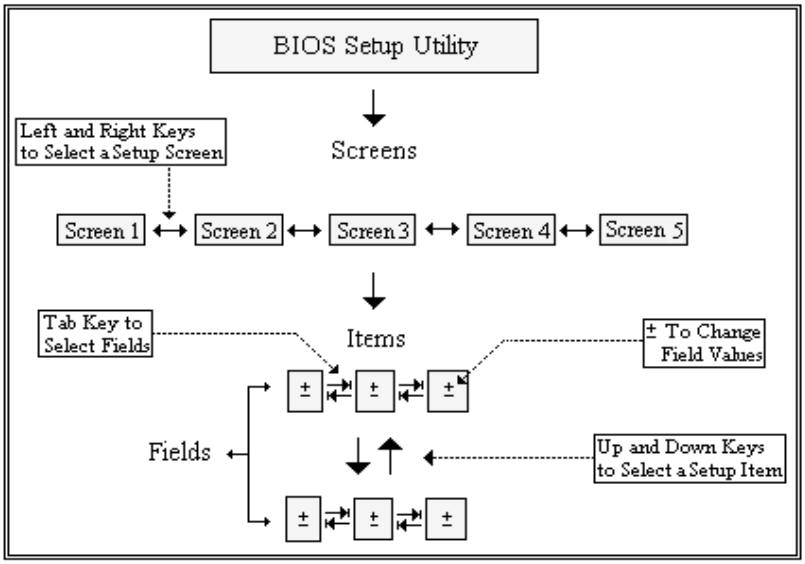


Navigation

The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process.

These keys include < F1 >, < F10 >, < Enter >, < ESC >, < Arrow > keys, and so on. .

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Note: There is a hot key legend located in the right frame on most setup screens.

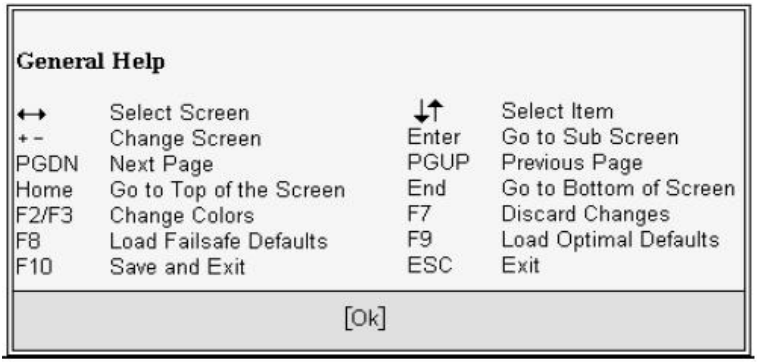
The < F8 > key on your keyboard is the Fail-Safe key. It is not displayed on the key legend by default. To set the Fail-Safe settings of the BIOS, press the < F8 > key on your keyboard. It is located on the upper row of a standard 101 keyboard. The Fail-Safe settings allow the motherboard to boot up with the least amount of options set. This can lessen the probability of conflicting settings.

Hotkey Descriptions

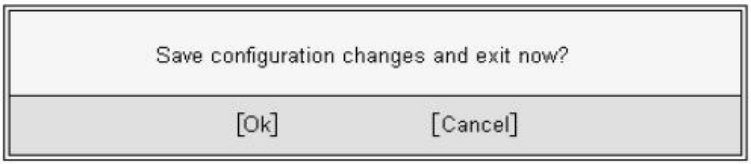
F1 The < F1 > key allows you to display the General Help screen.

Press the < F1 > key to open the General Help screen.

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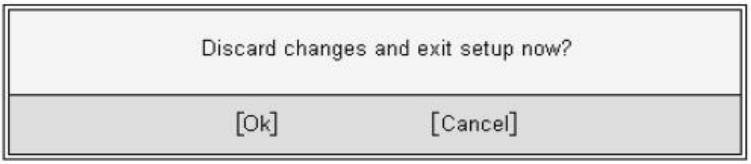


F10 The < F10 > key allows you to save any changes you have made and exit Setup. Press the < F10 > key to save your changes. The following screen will appear:



Press the < Enter > key to save the configuration and exit. You can also use the < Arrow > key to select Cancel and then press the < Enter > key to abort this function and return to the previous screen.

ESC The < Esc > key allows you to discard any changes you have made and exit the Setup. Press the < Esc > key to exit the setup without saving your changes. The following screen will appear:



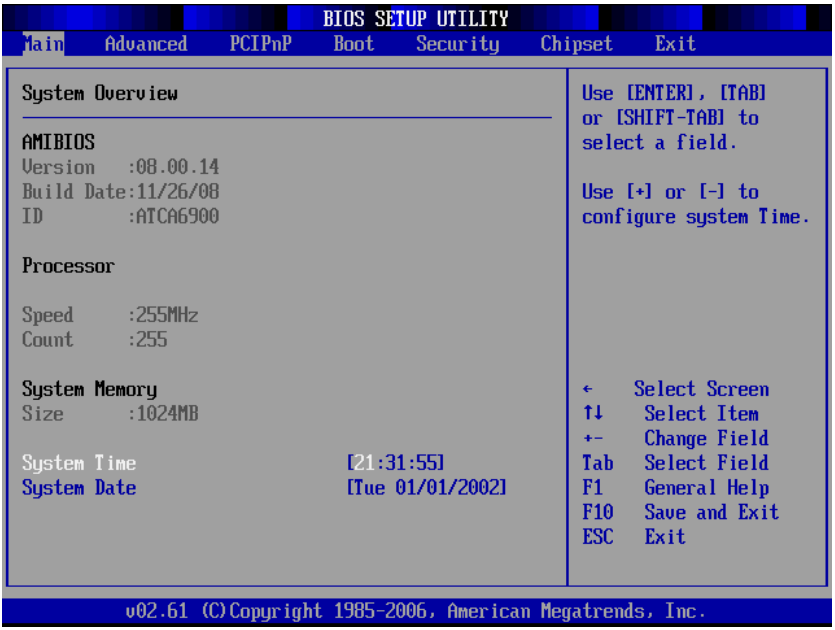
Press the < Enter > key to discard changes and exit. You can also use the < Arrow > key to select Cancel and then press the < Enter > key to abort this function and return to the previous screen.

Enter The < Enter > key allows you to display or change the setup option listed for a particular setup item. The < Enter > key can also allow you to display the setup sub-screens.

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8.2 Main Setup

When you first enter the Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



System Time/System Date

Use this option to change the system time and date. Highlight System Time or System Date using the < Arrow > keys. Enter new values using the keyboard. Press the < Tab > key or the < Arrow > keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

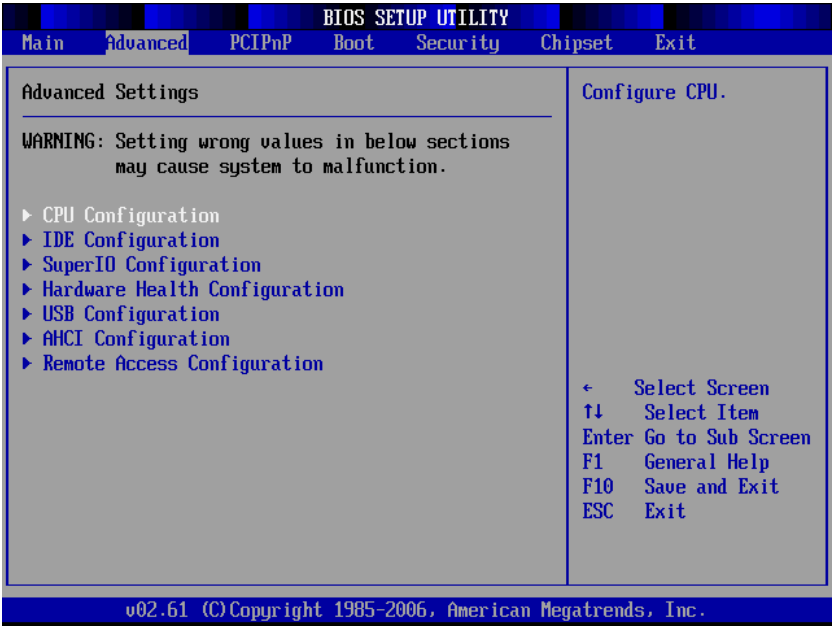
Note: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

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8.3 Advanced BIOS Setup

Select the Advanced tab from the setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as SuperIO Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the < Arrow > keys. The Advanced BIOS Setup screen is shown below.

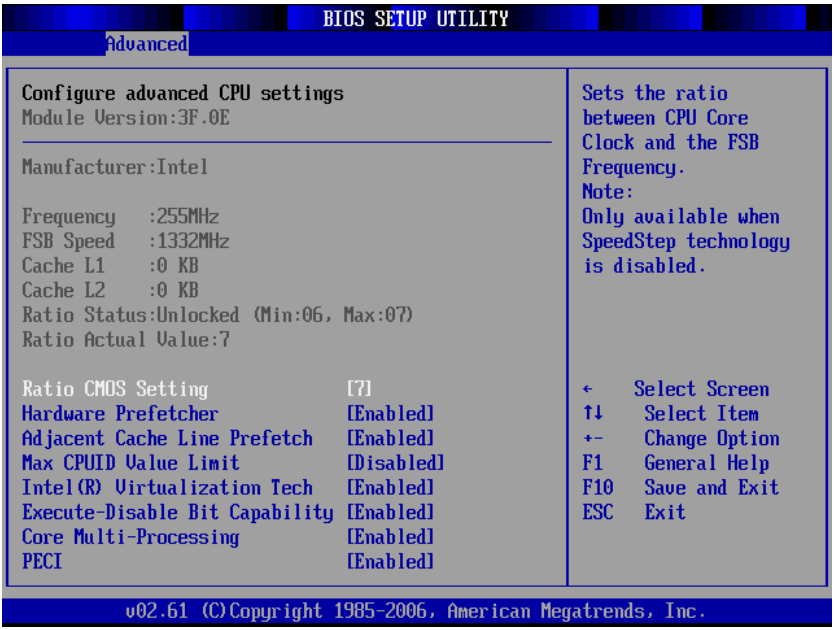
The sub menus are described on the following pages.



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8.3.1 CPU Configuration

You can use this screen to select options for the CPU Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the CPU Configuration screen is shown below.



Ratio CMOS Setting

This allows for setting the CPU's ratio by manually.

Hardware Prefetcher

This is used for reducing the waiting time of DRAM. The hardware prefetcher looks for streams of data and tries to predict what data will be needed next by the processor and proactively tries to fetch these data.

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Adjacent Cache Line Prefetch

This is used to choose the optimal use of sequential memory access for performance purpose. Disable this setting for applications that require high use of random memory access.

Max CPUID Value Limit

When the computer is booted up, the operating system executes the CPUID instruction to identify the processor and its capabilities. Before it can do so, it must first query the processor to find out the highest input value CPUID recognized. This determines the kind of basic information CPUID can provide the operating system. This option allows you to circumvent problems with older operating systems.

When Enabled, the processor will limit the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When Disabled, the processor will return the actual maximum CPUID input value of the processor when queried.

Intel® Virtualization Technology

Intel® Virtualization Technology consists of components that support virtualization of platforms based on Intel processors, thereby enabling the running of multiple operating systems and applications in independent partitions. Each partition behaves like a virtual machine (VM) and provides isolation and protection across partitions. Intel VT requires the use of a processor with Intel VT support. Additionally, a third-party VMM may also be required.

Execute-Disable Bit Capability

Intel's Execute Disable Bit is an hardware-based security feature that can help reduce system exposure to viruses and malicious code. It allows the processor to classify areas in memory where application code can or cannot execute. When a malicious worm attempts to insert code in the buffer, the processor disables code execution, preventing damage and worm propagation. To use Execute Disable bit you must have a PC or server with a processor with Execute Disable Bit capability and a supporting operating system.

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Core Multi-Processing

This item enables/disables multi-core processing functionality for multi-core processors.

PECI

Enables/disables the Platform Environment Control Interface (PECI). PECI is used for monitoring CPU temperature from the CPU's internal diode. It is recommended to enable it for temperature monitoring in IPMC.

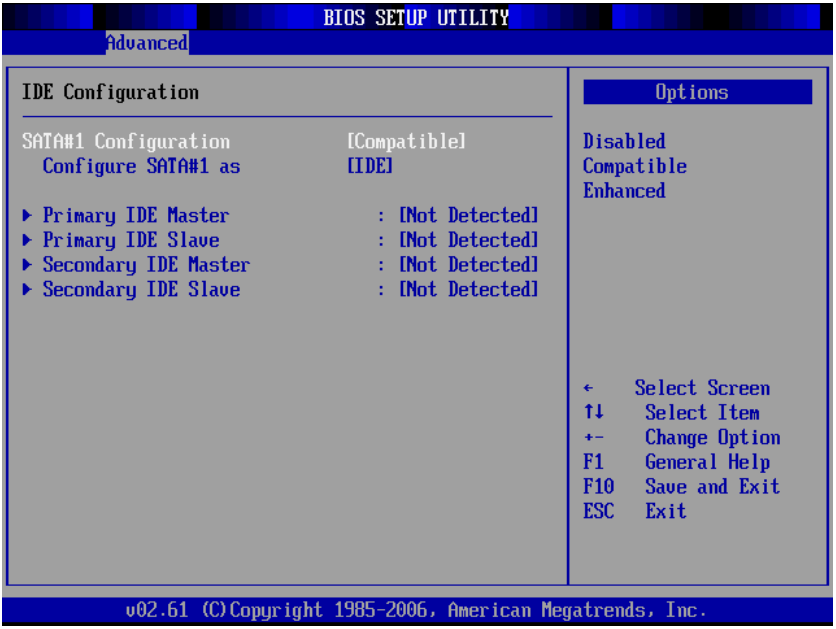
Intel® Speedstep™ Technology

Intel® SpeedStep™ technology allows the system to dynamically adjust processor voltage and core frequency, which can result in decreased average power consumption and decreased average heat production.

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8.3.2 IDE Configuration

You can use this screen to select options for the IDE Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the IDE Configuration screen is shown below.



SATA#1 Configuration

This item specifies which mode the SATA channels should be initialized in. The settings are **Disabled**, **Compatible** and **Enhanced**.

Configure SATA#1 as

When running in Enhanced mode, SATA devices can be configured as IDE, RAID or AHCI devices from this item.

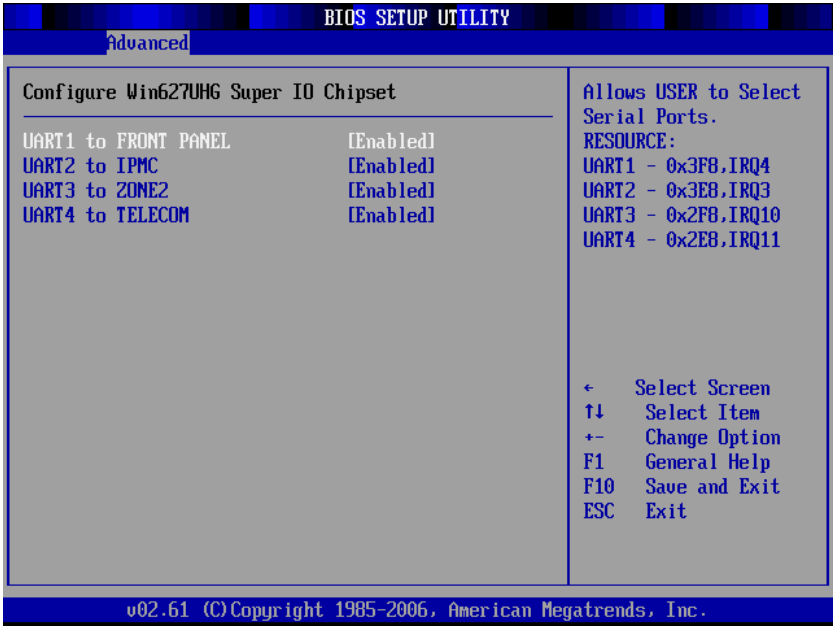
Primary/Secondary IDE Master/Slave

Select one of the hard disk drives to configure it. Press < Enter > to access its sub menu.

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8.3.3 Super IO Configuration

You can use this screen to select options for the Super IO settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



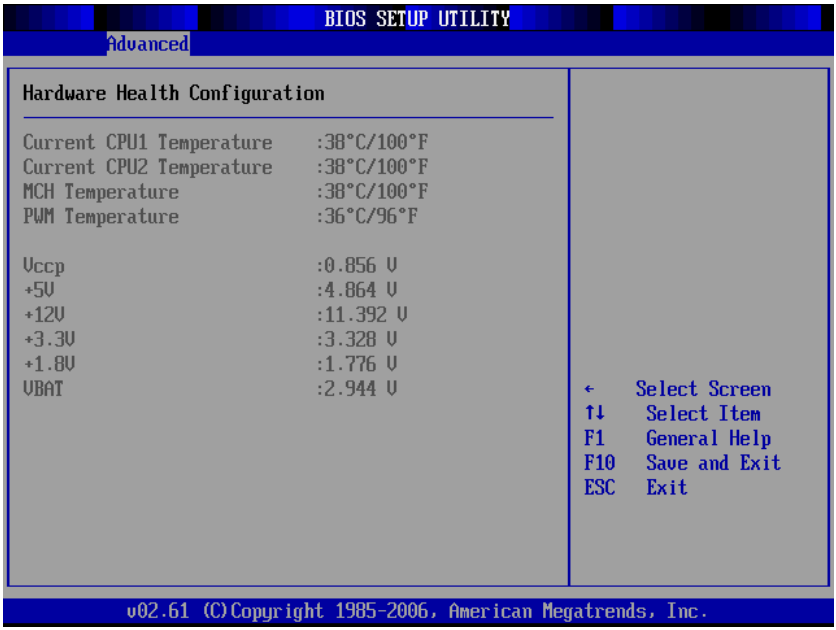
UART1 to FRONT PANEL, UART2 to IPMC, UART3 to ZONE2, UART4 to TELECOM

These items are for enabling/disabling the serial port to front panel, IPMC, ZONE2, and TELECOM. Detailed resources for these serial ports are listed in the help field of the setup screen.

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8.3.4 Hardware Health Configuration

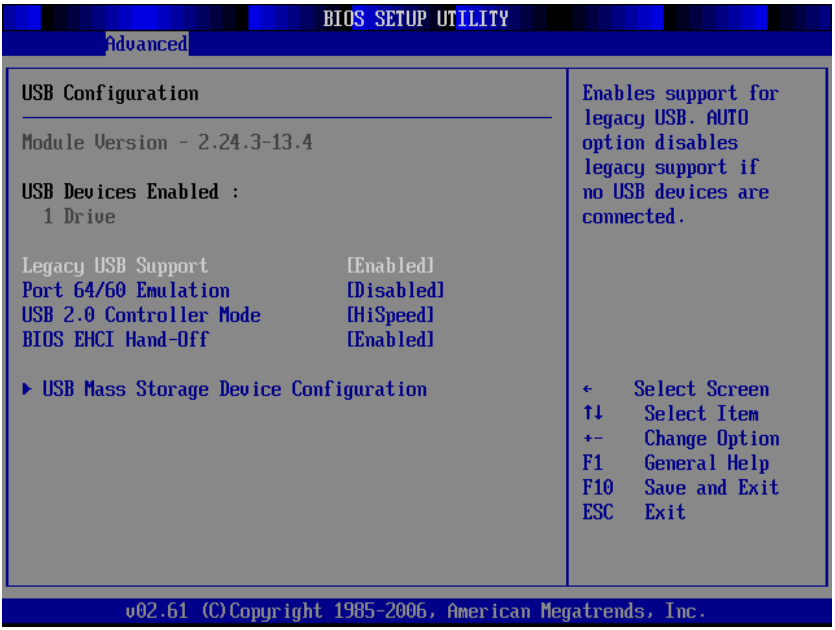
This option displays the current status of all of the monitored hardware devices/components such as voltages and temperatures. The options are Enabled and Disabled.



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8.3.5 USB Configuration

You can use this screen to select options for the USB Configuration. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



Legacy USB Support

Legacy USB Support refers to USB mouse and keyboard support. Normally if this option is not enabled, any attached USB mouse or USB keyboard will not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or USB keyboard can control the system even when there are no USB drivers loaded on the system. Set this value to enable or disable the Legacy USB Support.

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- **Disabled:** Set this value to prevent the use of any USB device in DOS or during system boot.
- **Enabled:** Set this value to allow the use of USB devices during boot and while using DOS.
- **Auto:** This option auto detects USB Keyboards or Mice and if found, allows them to be utilized during boot and while using DOS.

Port 64/60 Emulation

This option uses USB to receive the IO port 64/60 trap to emulate the legacy keyboard controller.

USB 2.0 Controller Mode

The USB 2.0 Controller Mode configures the data rate of the USB port. The options are **FullSpeed** (12 Mbps) and **HiSpeed** (480 Mbps).

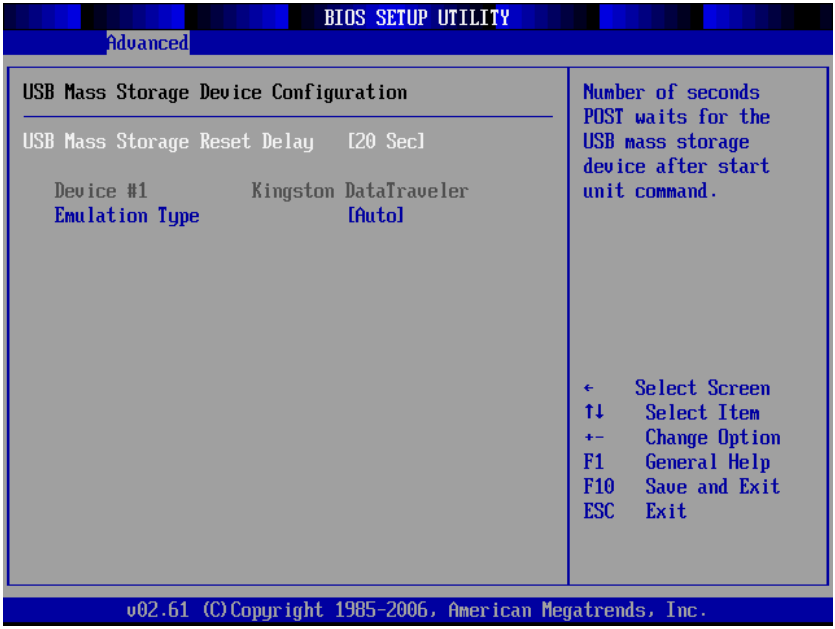
BIOS EHCI hand-off

This option provides a workaround for operating systems without ECHI hand-off support. The EHCI ownership change should be claimed by the EHCI driver.

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USB Mass Storage Device Configuration

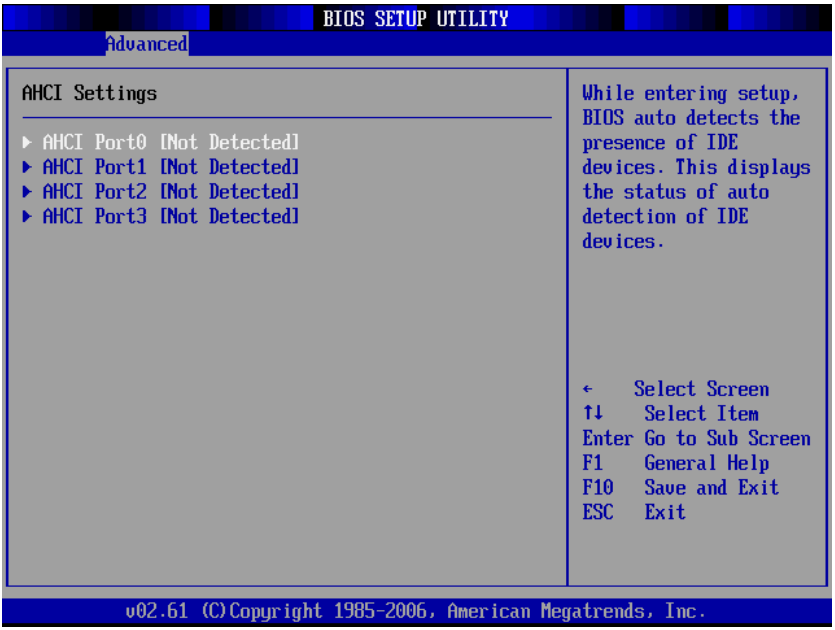
This is a submenu for configuring the USB Mass Storage Class Devices when BIOS finds they are in use on USB ports. Emulation Type can be set according to the type of attached USB mass storage device(s). If set to Auto, USB devices less than 530MB will be emulated as Floppy and those greater than 530MB will remain as hard drive. The Forced FDD option can be used to force a hard disk type drive (such as a Zip drive) to boot as FDD.



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8.3.6 AHCI Configuration

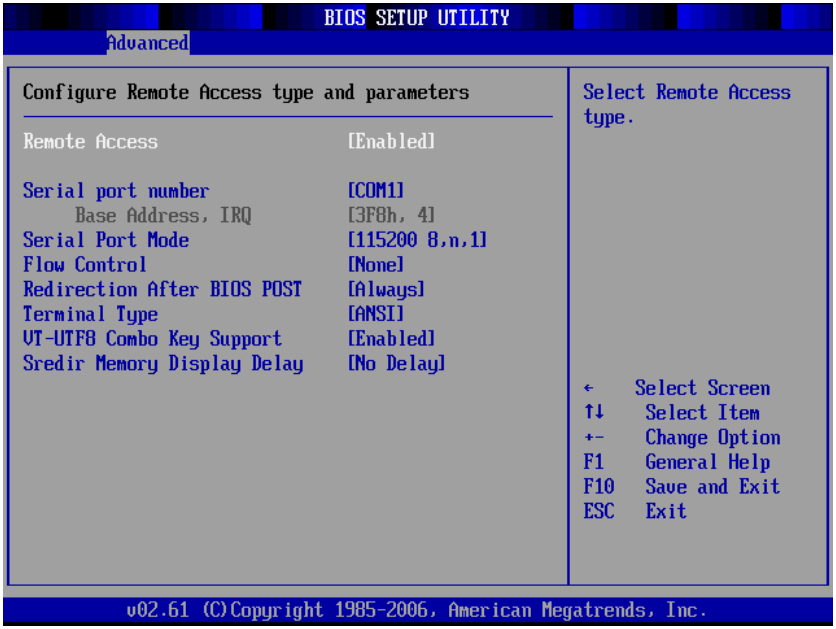
On this screen, BIOS will detect the presence of AHCI disks and show which port they are on, when SATA is configured as AHCI device.



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8.3.7 Remote Access Configuration

Remote access configuration provides the settings to allow remote access by another computer to get POST messages and send commands through serial port access.



Remote Access

Select this option to Enable or Disable the BIOS remote access feature.

Note: Enabling Remote Access requires a dedicated serial port connection. Once both serial ports are configured to disabled, you should set this value to Disabled or it may cause abnormal boot.

Serial Port Number

Select the serial port you want to use for the remote access interface. You can set the value for this option to COM1, COM2 or COM3.

Note: If you have changed the resource assignment of the serial ports in Advanced> SuperIO Configuration, you must Save Changes and Exit, reboot the system, and enter the setup menu again in order to see those changes reflected in the available Remote Access options.

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Serial Port Mode

Select the baud rate you want the serial port to use for console redirection. The options are **115200 8,n,1**; **57600 8,n,1**; **19200 8,n,1**; and **09600 8,n,1**.

Flow Control

Set this option to select Flow Control for console redirection. The settings for this value are **None**, **Hardware**, or **Software**.

Redirection After BIOS POST

This option allows you to set Redirection configuration after BIOS POST. The settings for this value are **Disabled**, **Boot Loader**, or **Always**.

- **Disabled:** Set this value to turn off the redirection after POST
- **Boot Loader:** Set this value to allow the redirection to be active during POST and Boot Loader.
- **Always:** Set this value to allow the redirection to be always active.

Terminal Type

This option is used to select either VT100/VT-UTF8 or ANSI terminal type. The settings for this value are **ANSI**, **VT100**, or **VT-UTF8**.

VT-UTF8 Combo Key Support

This option enables VT-UTF8 Combination Key Support for ANSI/VT100 terminals. The settings for this value are **Enabled** or **Disabled**.

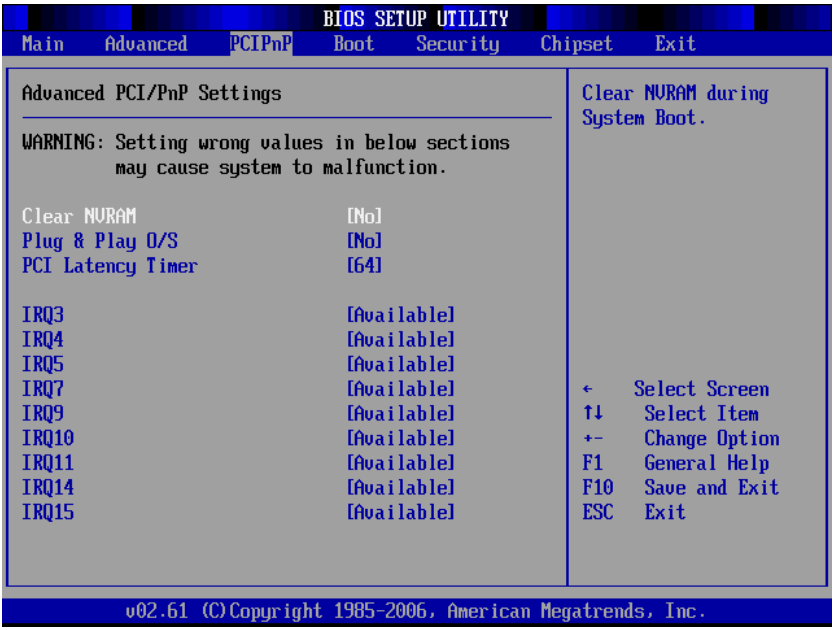
Sredir Memory Display Delay

This option gives the delay in seconds to display memory information. The options for this value are **No Delay**, **Delay 1 Sec**, **Delay 2 Sec**, or **Delay 4 Sec**.

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8.4 Advanced PCI/PnP Settings

Select the PCI/PnP tab from the setup screen to enter the Plug and Play BIOS Setup screen. You can display a Plug and Play BIOS Setup option by highlighting it using the < Arrow > keys. The Plug and Play BIOS Setup screen is shown below.



Clear NVRAM

Set this to enable/disable Clear NVRAM during system boot. NVRAM content like ESCD will be cleared and updated at next boot.

Plug & Play O/S

- **No:** Let the BIOS configure all the devices in the system.
- **Yes:** Let the operating system configure Plug and Play (PnP) devices not required for boot if your system has a Plug and Play operating system.

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PCI Latency Timer

Set this value to allow the PCI Latency Timer to be adjusted. This option sets the latency of all PCI devices on the PCI bus.

IRQ Channel

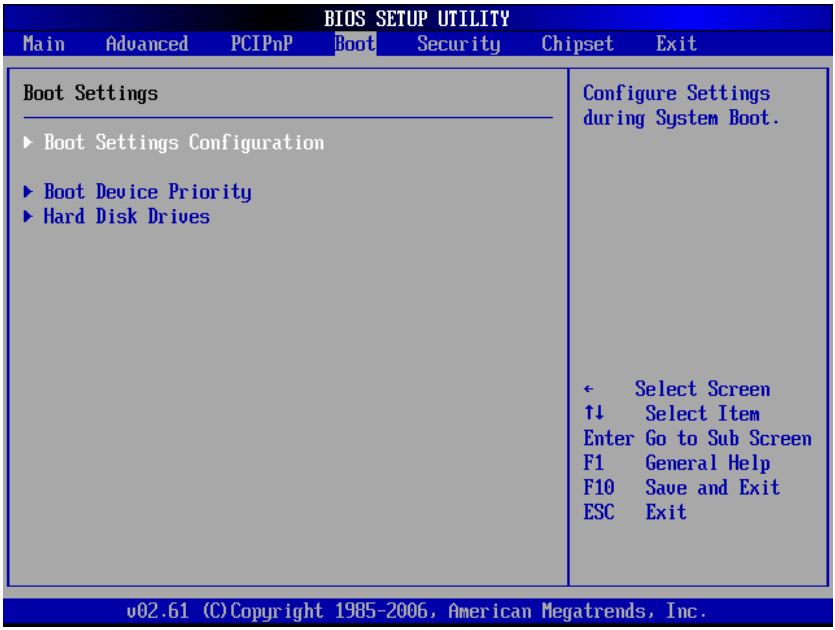
Set this value to allow the IRQ/DMA channel settings to be modified.

- **Available:** This setting allows the specified IRQ/DMA channel to be used by a PCI/PnP device.
- **Reserved:** This setting allows the specified IRQ/DMA channel to be used by a legacy ISA device.

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8.5 Boot Settings

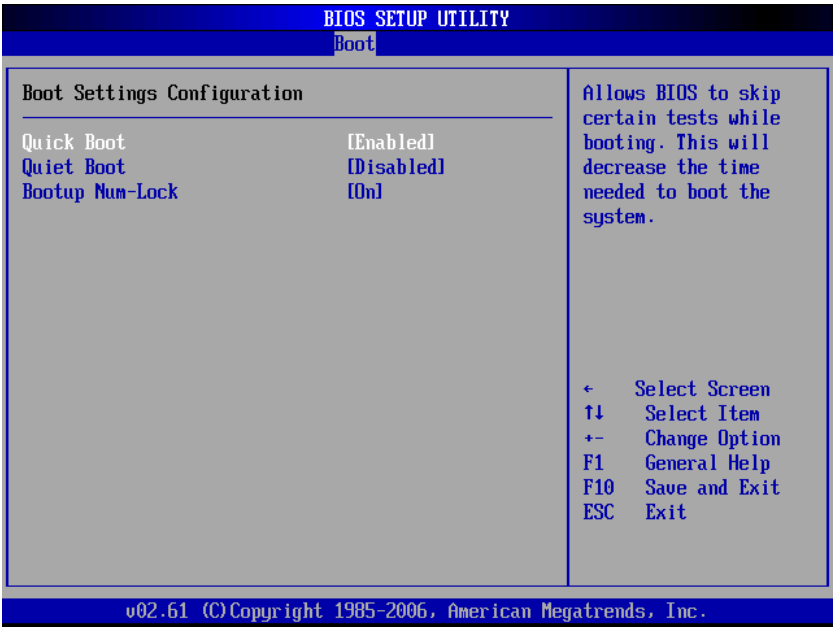
Select the Boot tab from the setup screen to enter the Boot BIOS Setup screen. You can select any of the items in the left frame of the screen, such as Boot Device Priority, to go to the sub menu for that item. You can display a Boot BIOS Setup option by highlighting it using the < Arrow > keys. The Boot Settings screen is shown below:



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8.5.1 Boot Settings Configuration

Use this screen to select options for the Boot Settings Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



Quick Boot

Disabled – Set this value to allow the BIOS to perform all POST tests.

Enabled – Set this value to allow the BIOS to skip certain POST tests to boot faster.

Quiet Boot

Disabled – Set this value to allow the computer system to display the POST messages.

Enabled – Set this value to allow the computer system to display the OEM logo.

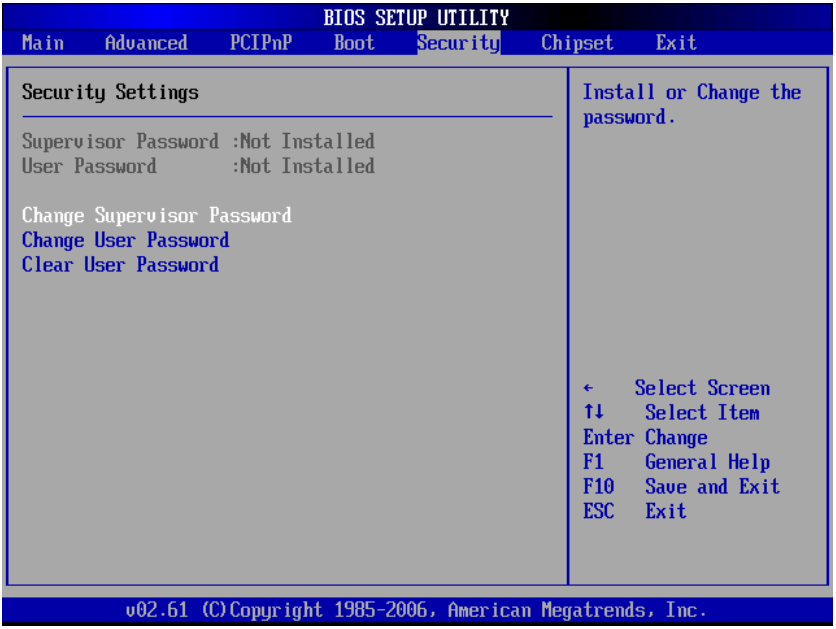
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Bootup Num-Lock

Set this value to allow the Number Lock setting to be modified during boot up. **Off** – This option does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard will light up when the Number Lock is engaged. **On** – Set this value to allow the Number Lock on the keyboard to be enabled automatically when the computer system is boot up. This allows the immediate use of 10-keys numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard will be lit.

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8.6 Security Setup



Password Support

Two Levels of Password Protection

Provides both a Supervisor and a User password. If you use both passwords, the Supervisor password must be set first.

The system can be configured so that all users must enter a password every time the system boots or when Setup is executed, using either or either the Supervisor password or User password.

The Supervisor and User passwords activate two different levels of password security. If you select password support, you are prompted for a one to six character password. Type the password on the keyboard. The password does not appear on the screen when typed. Make sure you write it down. If you forget it, you must drain NVRAM and re-configure.

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Remember the Password

Keep a record of the new password when the password is changed. If you forget the password, you must erase the system configuration information in NVRAM.

To access the sub menu for the following items, select the item and press < Enter >:

- Change Supervisor Password
- Change User Password
- Clear User Password

Supervisor Password

Indicates whether a supervisor password has been set.

User Password

Indicates whether a user password has been set.

Change Supervisor Password

Select this option and press < Enter > to access the sub menu. You can use the sub menu to change the supervisor password.

Change User Password

Select this option and press < Enter > to access the sub menu. You can use the sub menu to change the user password.

Clear User Password

Select this option and press < Enter > to access the sub menu. You can use the sub menu to clear the user password.

Change Supervisor Password

Select Change Supervisor Password from the Security Setup menu and press < Enter >.

Enter New Password:

Type the password and press < Enter >. The screen does not display the characters entered. Retype the password as prompted and press < Enter >. If the password confirmation is incorrect, an

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error message appears. The password is stored in NVRAM after completes.

Change User Password

Select Change User Password from the Security Setup menu and press < Enter >.

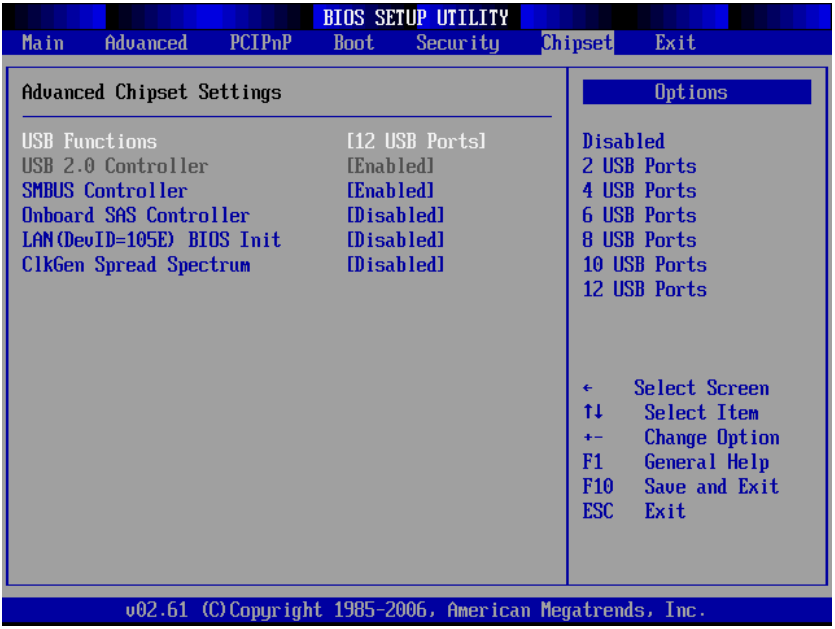
Enter New Password:

Type the password and press < Enter >. The screen does not display the characters entered. Retype the password as prompted and press < Enter >. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after completes.

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8.7 Chipset Setup

Select the Chipset tab from the setup screen to enter the Chipset BIOS Setup screen. You can select any of the items in the left frame of the screen to go to the sub menu for that item. The Chipset BIOS Setup screen is shown below.



USB Functions

Set this value to allow the system to disable, enable, and select a set number of onboard USB ports.

USB 2.0 Controller

This option takes effect only when USB Functions are enabled. Enabling will allow USB 2.0 functionality to all USB ports.

SMBUS Controller

Set this value to enable/disable the SMBUS Controller

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Onboard SAS Controller

Set this value to Enable/Disable to initialize SAS BIOS at POST. If there are any SAS disks on the system, it must be set to Enabled. POST time can be shortened if this item is configured to Disabled.

LAN(DevID=105E) BIOS Init

Set this value to Enable/Disable PXE functionality on the Ethernet controller (device ID 105EH). The PXE function can be set to either the front or rear LAN port.

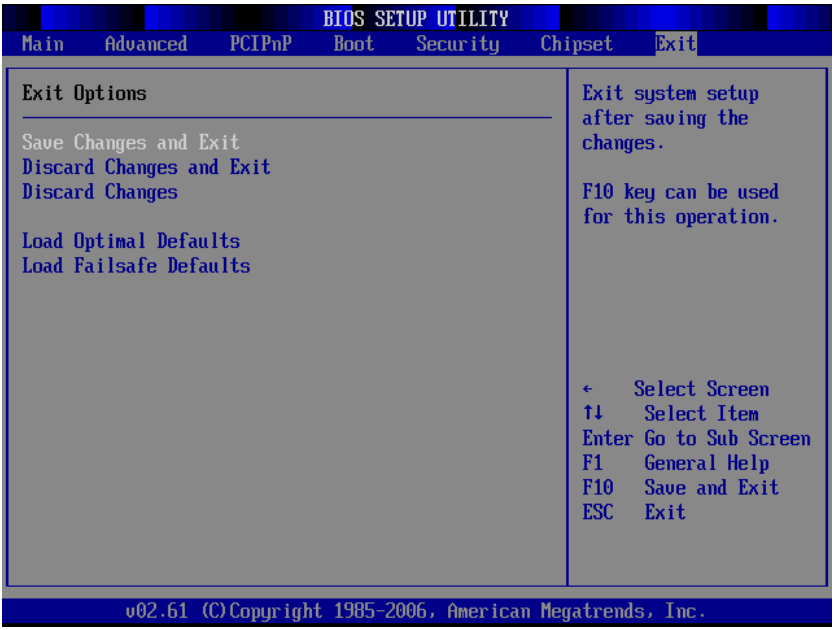
ClkGen Spread Spectrum

This field enables/disables support of the ClkGen Spread Spectrum function.

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8.8 Exit Menu

Select the Exit tab from the setup screen to enter the Exit BIOS Setup screen. You can display an Exit BIOS Setup option by highlighting it using the < Arrow > keys. The Exit BIOS Setup screen is shown below.



Save Changes and Exit

When you have completed the system configuration changes, select this option to leave Setup and reboot the computer so the new system configuration parameters can take effect.

Save Configuration Changes and Exit Now?

[Ok] [Cancel]

appears in the window. Select Ok to save changes and exit.

Discard Changes and Exit

Select this option to quit Setup without making any permanent changes to the system configuration.

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Discard Changes and Exit Setup Now?

[Ok] [Cancel]

appears in the window. Select Ok to discard changes and exit.

Discard Changes

Select Discard Changes from the Exit menu and press < Enter >.

Select Ok to discard changes.

Load Optimal Defaults

Automatically sets all Setup options to a complete set of default settings when you select this option. The Optimal settings are designed for maximum system performance, but may not work best for all computer applications. In particular, do not use the Optimal Setup options if your computer is experiencing system configuration problems.

Select Load Optimal Defaults from the Exit menu and press < Enter >.

Select Ok to load optimal defaults.

Load Failsafe Defaults

Automatically sets all Setup options to a complete set of default settings when you select this option. The Failsafe settings are designed for maximum system stability, but not maximum performance. Select the FailSafe Setup options if your computer is experiencing system configuration problems.

Select Load Fail-Safe Defaults from the Exit menu and press < Enter >.

Load FailSafe Defaults?

[Ok] [Cancel]

appears in the window. Select Ok to load FailSafe defaults.

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8.9 BIOS Update Procedure

Download the BIOS binary file from ADLINK web site or Technical Service department. Extract the compressed file and execute P.BAT to update the BIOS. Please note that the name of the BIOS file will reflect the BIOS revision. The example below will update the BIOS using the file A6900T12. ROM.

```
*******************************************************
C:\BIOS\AT6900>dir/w

 Volume in drive C has no label
 Volume Serial Number is 0065-1CB9
 Directory of C:\BIOS\AT6900

[.]   [..]   A6900T12.ROM    AFUDOS.EXE     AFUWIN.EXE
HISTORY.TXT   P.BAT    UCORESYS.SYS    UCOREW64.SYS
         8 file(s)      2,623,464 bytes
         2 dir(s)     867,123,200 bytes free


C:\BIOS\ AT6900>p.bat

C:\BIOS\AT6900>afudos a6900t12.rom /p /b /reboot


*******************************************************
*       AMI Firmware Update Utility  Ver.4.12         *
  Copyright (C)2006 American Megatrends Inc. All Rights
                       Reserved
*******************************************************

- Bootblock checksum .... ok
- Bootblock checksum .... ok
- Module checksums ...... ok
- Erasing flash ......... done
- Writing flash ......... done
- Verifying flash ....... done
- Writing Bootblock ..... done
- Verifying Bootblock ... 0x000D3800 (100%)
*******************************************************
```

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Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.
- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

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A Lithium-type battery may be provided for uninterrupted, backup or emergency power.



Risk of explosion if battery is replaced with one of an incorrect type. Dispose of used batteries appropriately.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

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Getting Service

Contact us should you require any service or assistance.

ADLINK Technology, Inc.
Address: 9F, No.166 Jian Yi Road, Zhonghe District
New Taipei City 235, Taiwan
新北市中和區建一路 166 號 9 樓
Tel: +886-2-8226-5877
Fax: +886-2-8226-5717
Email: service@adlinktech.com

Ampro ADLINK Technology, Inc.
Address: 5215 Hellyer Avenue, #110, San Jose, CA 95138, USA
Tel: +1-408-360-0200
Toll Free: +1-800-966-5200 (USA only)
Fax: +1-408-360-0222
Email: info@adlinktech.com

ADLINK Technology (China) Co., Ltd.
Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203)
300 Fang Chun Rd., Zhangjiang Hi-Tech Park,
Pudong New Area, Shanghai, 201203 China
Tel: +86-21-5132-8988
Fax: +86-21-5132-3588
Email: market@adlinktech.com

ADLINK Technology Beijing
Address: 北京市海淀区上地东路 1 号盈创动力大厦 E 座 801 室(100085)
Rm. 801, Power Creative E, No. 1, B/D
Shang Di East Rd., Beijing, 100085 China
Tel: +86-10-5885-8666
Fax: +86-10-5885-8625
Email: market@adlinktech.com

ADLINK Technology Shenzhen
Address: 深圳市南山区科技园南区高新南七道 数字技术园
A1 栋 2 楼 C 区 (518057)
2F, C Block, Bldg. A1, Cyber-Tech Zone, Gao Xin Ave. Sec. 7,
High-Tech Industrial Park S., Shenzhen, 518054 China
Tel: +86-755-2643-4858
Fax: +86-755-2664-6353
Email: market@adlinktech.com

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神田 374 ビル 4F
KANDA374 Bldg. 4F, 3-7-4 Kanda Kajicho,
Chiyoda-ku, Tokyo 101-0045, Japan
Tel: +81-3-4455-3722
Fax: +81-3-5209-6013
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