ADLINK TECHNOLOGY INC.

aTCA-N700

Dual Cavium CN6880 Packet Processor GbE ATCA Processor Blade

Hardware User's Manual



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Revision History

Rev	Date	Description
1.00	28/08/2013	Initial release.
1.01	21/10/2013	Correct memory, flash specification; add French safety precautions

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Preface

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Table of Contents

Revision History 2
Preface 3
List of Figures 6
List of Tables 7
1. Introduction 8
2. Summary of Specifications 10
3. External Interfaces 12
3.1. Front Panel 12
3.1.1. Console Port 12
3.1.2. USB Port 13
3.1.3. Management Ethernet Port 13
3.1.4. Service Ports 13
3.1.5. Reset Switch 13
3.1.6. LEDs and Markers 14
3.2. Zone 2 Backplane Interfaces 15
3.3. Zone 3 Backplane Interface for Rear Transition Module 15
4. Installation and Operation 16
4.1. Hardware Configuration Setting 17
4.1.1. Headers and Jumpers 18
4.1.2. DIP Switch 19
4.1.3. Programmable Devices 21
4.2. Hardware Installation 21
4.2.1. Front Blade 21
4.2.2. RTM 22
4.2.3. Console Port Connection 23
5. Architecture Overview 24
6. Network Processor Subsystem 25
6.1. CN6880 Embedded Components 26
6.2. DRAM Memory 27
6.3. Boot/OS Memories on Boot-Bus 28
6.4. Data Plane Interface 28
6.5. Mezzanine Board Interface (Optional) 29
6.6. Host Interface 30
6.7. UART Interface 31
6.8. TWSI (I2C) Interface 31
6.9. Other Interfaces 31
6.10. GPIO 32
6.11. Clock 32
7. Data Plane Interconnection Subsystem 34
7.1. Switch Features: BCM56842 34
7.2. SerDes Interface 34
7.3. PCI-e Interface 36
7.4. Reset and Interrupts 36
7.5. Clock 37
7.6. Other Interfaces 37
7.6.1. MDC/MDIO: MIIM 37
7.6.2. BSC (I2C) Interface 37
7.6.3. LED Control 37
7.6.4. JTAG 40
8. Control Plane Subsystem 41
8.1. Local Management Processor, P2041 42
8.1.1. Features 42
8.1.2. DDR3 SDRAM Interface 43
8.1.3. PCI Express Interface 44
8.1.4. I2C (TWSI) Interface 44
8.1.5. UART Interface 46
8.1.6. Interrupts 47
8.1.7. SPI Interface 48

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8.1.8. SATA Interface for Chip SSD 48
8.1.9. Local Bus Interface (EBI) 49
8.1.10. USB Interface 49
8.1.11. MDC/MDIO Interface 50
8.1.12. GPIO Interface 50
8.2. Ethernet Controller Interface 50
8.2.1. 7-port Ethernet Switch BCM53115M 51
8.2.2. Ethernet Transceiver BCM54612E 52
9. Blade Management Subsystem 53
9.1. IPMC 55
9.2. I/O Ports 56
9.3. Ethernet Transceiver BCM5221 59
9.4. CPLD 59
9.5. Managed Objects 60
9.5.1. Temperature Sensor and Real Time Clock 60
9.5.2. Sensor Data Record (SDR) 60
9.5.3. System Event Log (SEL) 60
9.5.4. Field Replaceable Unit (FRU) Information 60
9.6. Storage for IPMC Firmware 60
9.7. Blade Reset 60
9.8. IPMC and MMC Control Operation 61
9.9. Power and Temperature Threshold 68
10. Power 71
10.1. Maximum Power Consumption 71
10.2. Power Distribution 71
10.3. Power Sequencing 72
11. Clock Tree 73
11.1. IPMC and CPLD Clocks 73
11.2. Major Device Clocks 73
12. Layout 75
12.1. Mechanical Drawing and Placement 75
12.2. PCB Layer Stack-up 76
Appendix 77
Safety 79
Consignes de Sécurité 80
Getting Service 81

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List of Figures

Figure 3-1 aTCA-N700 Front Panel 12
Figure 4-1 aTCA-N700 16
Figure 4-2 Configurable Component Locations 17
Figure 4-3 CPLD JTAG Header 18
Figure 4-4 COP Header 18
Figure 4-5 Standalone Mode Selector Header 18
Figure 4-6 In/Ejector handle (bottom side) 22
Figure 4-7 Plugging the Board 22
Figure 5-1 aTCA-N700 Architecture with optional RTMs 24
Figure 6-1 Network Processor Subsystem 26
Figure 6-2 CN68XX Internal Blocks 27
Figure 6-3 CN6880 DRAM Memory 27
Figure 6-4 Boot Memories 28
Figure 6-5 Data Path Interface 29
Figure 6-6 Mezzanine Board Interface 29
Figure 6-7 Mezzanine Board Connector 29
Figure 6-8 Host Interface – PCIe 30
Figure 6-9 Host Interface - Ethernet 30
Figure 6-10 Console Port Connection 31
Figure 6-11 TWSI (I2C) Connection 31
Figure 6-12 External clock to CN6880 requirements 33
Figure 7-1 Switch Port Connections 35
Figure 7-2 Switch Reset Requirements 36
Figure 7-3 Switch LED_DATA0 Format 37
Figure 8-1 Control Plane Subsystem 41
Figure 8-2 P2041 Internal Blocks (from datasheet) 42
Figure 8-3 P2041 DDR3 Interface 43
Figure 8-4 Host Interface – PCI-e 44
Figure 8-5 P2041 I2C Interface 45
Figure 8-6 P2041 UART Interface 46
Figure 8-7 P2041 SPI Interface 48
Figure 8-8 P2041 Local Bus (EBI) Interface 49
Figure 8-9 Ethernet Control Plane Interconnections 50
Figure 9-1 IPMC Block 53
Figure 9-2 Blade Reset Signals 61
Figure 9-3 Cold Reset Procedure 62
Figure 9-4 Deactivate Procedure 62
Figure 9-5 Activate Procedure 63
Figure 9-6 RTM Deactivate Procedure 63
Figure 9-7 RTM Activate Procedure 64
Figure 9-8 Shutdown Procedure 65
Figure 9-9 RTM Shutdown Procedure 65
Figure 9-10 Hot Swap Procedure 66
Figure 9-11 RTM Hot Swap Procedure 67
Figure 10-1 Power Distribution 71
Figure 10-2 Power Sequencing 72
Figure 11-1 IPMC and CPLD Clocks 73
Figure 11-2 Clocks for NPUs, LMP, and Switch Fabric 74
Figure 12-1 Faceplate and component placement 75
Figure 12-2 PCB layer stack-up (preliminary) 76

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List of Tables

Table 1-1 Glossary 9
Table 2-1 aTCA-N700 Specifications 10
Table 2-2 aTCA-N700 build options 11
Table 3-1 Serial Console Port Pin-out 12
Table 3-2 Serial Console Port Configuration Value 13
Table 3-3 RJ-45 Management Port Pin-out 13
Table 3-4 Front Panel LEDs and Markers 14
Table 4-1 Shelf Manager Interoperability Mode Setting: J25 19
Table 4-2 Shelf Manager Interoperability Mode Setting: SW3, SW6 19
Table 4-3 Faceplate serial port selection 19
Table 4-4 SPI Flash or SD Card selection 20
Table 4-5 Remote control selection 20
Table 4-6 Programmable devices 21
Table 6-1 GPIO Pins 32
Table 7-1 Trident+ Switch Fabric Scalability 34
Table 7-2 Switch Port Connections 35
Table 7-3 SFPs and LED Data 38
Table 8-1 I2C Bus Address 45
Table 8-2 P2041 Interrupt Signal Connections 47
Table 8-3 GPIO connections 50
Table 8-4 Base Switch Port Mapping 51
Table 9-1 A2F500 Features 55
Table 9-2 IPMC Pin map and on-board arrangement 56
Table 9-3 Board Shutdown and Reset Procedures 61
Table 9-4 Signals: Cold Reset Procedure 62
Table 9-5 Signals: Deactivate Procedure 63
Table 9-6 Signals: Activate Procedure 63
Table 9-7 Signals: RTM Deactivate Procedure 64
Table 9-8 Signals: RTM Activate Procedure 64
Table 9-9 Signals: Shutdown Procedure 65
Table 9-10 Signals: RTM Shutdown Procedure 66
Table 9-11 Signals: Hot Swap Procedure 67
Table 9-12 Signals: RTM Hot Swap Procedure 67
Table 9-13 Threshold Values: Voltage 68
Table 9-14 Threshold Values: Temperature 70
Table A-1 Zone 2 Connector Pin-out: J23 77
Table A-2 Zone 3 Connector Pin-out: J31 77
Table A-3 Zone 3 Connector Pin-out: J32 78

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1. Introduction

The aTCA-N700 is a single slot AdvancedTCA blade powered by dual OCTEON II multi-core processors for high performance packet processing applications such as IPTV, LTE wireless, security and many more areas. The blade provides up to 40Gbps full duplex packet processing performance with flexible network interfaces.

The aTCA-N700 is designed to provide high performance security enabled intelligent deep packet inspection and processing functions that are required by high-end network appliances, security appliances, switches, and servers. The major building block is the Cavium CN6880 packet processor subsystem.

The Cavium CN6880 has 2MB of L2 cache which is shared by 32 cnMIPS cores. Each cnMIPS core also has dedicated 37K Icache and 32K Dcache. DDR3 memory has a total of 400Gbps bandwidth. Hardware acceleration blocks are also available for the most advanced networking and security application. The RegEx engine enables high throughput pattern matching with optional co-processors.

The blade also has a high performance, non-blocking, local switch fabric to interconnect the CN6880, backplane, and I/O ports altogether. This feature allows the data path to be configured in many different ways to fully utilize the multi-core CPUs and provide the flexibility for application programming. There are 3 modes of data path operation: serial, parallel, and bypass, which can be configured depending on the application requirements.

The application areas of the blade are summarized but not limited to:

- Wireless backhaul aggregation Switch/Router, which requires Deep Packet Inspection capability
- Security Appliances such as Firewalls, VPN and IDS/IPS
- Content based fine grain load balancing switches
- Front end I/O card with traffic management for high capacity, value added appliances for multi-service offering
- Network Monitoring and Analysis Services
- Ethernet aggregation nodes

This document describes the hardware overview, specifications and the installation and basic operation along with the architecture of the aTCA-N700 front blade. Shown in Table 1-1 is the selected set of abbreviations that are frequently used throughout the document.

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Table 1-1 Glossary

Terms	Description
ASIC	Application Specific Integrated Circuit
ATCA	Advanced Telecom Computing Architecture
Base Interface	ATCA Base Interface on the Zone-2 connectors to connect to the dual hubs, 4 differential pairs per Base Channel.
Blade	A printed circuit board assembly that plugs into a chassis
BSP	Board Support Package
Boot-flash	Flash memory where the bootloader program is stored
Bootloader	Code used to boot the System before loading OS
DDR	Double Data Rate DRAM memory
DFT/DFM	Design For Test/Manufacturing
DIMM	Dual Inline Memory Module
ECC	Error Correction Control
E-keying	Standard defined by PICMG useful to verify whether the ATCA blade plugged in is compliant to the fabric link capabilities
Fabric Interface	ATCA Fabric Interface on the Zone-2 connectors to connect to the dual Switch Fabric Blades
Fabric Slot	A slot supporting a link connection to/from each node slot
FRU	Field Replaceable Unit
GPIO	General Purpose Input/Output
Hot-swap	Functions of replacing system components without shutting down the system
IPMB	Intelligent Platform Management Bus
IPMB-L	IPMB Local interface
IPMC	Intelligent Platform Management Controller
IPMI	Intelligent Platform Management Interface
JTAG	Joint Test Action Group
MAC	Media Access Controller
MMC	Module Management Controller
NPU	Network Processor Unit
OOS	Out Of Service
PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect-Express
PHY	Physical Layer or Physical Layer Device
PICMG	PCI Industrial Computer Manufacturers Group
RGMII	Reduced Gigabit Medium Independent Interface
RTM	Rear Transition Module
RXAUI	Reduced XAUI, having 2 lanes@6.25Gbps
SDR	Sensor Data Record
SDRAM	Synchronous Dynamic Random Access Memory
SFP	Small Form Pluggable (1G interface)
SFP+	Small Form Pluggable Plus (10G interface)
SGMII	Serial Gigabit Medium Independent Interface
SOL	Serial Over LAN
QSFP+	Quad Small Form Pluggable Plus (40G interface)
UART	Universal Asynchronous Receiver-Transmitter
VLP	Very Low Profile, DRAM Module Form Factor Spec
XAUI	10 Gigabit (X) Attachment Unit Interface, having 4 lanes@3.125Gbps
XLAUI	40 Gigabit (XL) Attachment Unit Interface

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2. Summary of Specifications

Summarized in Table 2-1 are the specifications of the aTCA-N700 platform.

Table 2-1 aTCA-N700 Specifications

Feature	Function	Description
Physical	Dimensions	8U x 6HP x 280mm AdvancedTCA, single slot
	Compliance	PICMG3.0 Rev 3.0 and PICMG3.1, Option 3, 9, Rev 2.0 and 40GBase-KR4
Processor Subsystem	Network Processor	Dual Cavium OCTEON II CN6880
	DRAM Memory/NP	4x DDR3-1066 DIMM, 32GB max
	Boot Flash Memory/NP	2x 8 MB (NOR Flash, redundant)
	OS Flash Memory/ NP	2x 2 GB (NAND Flash, redundant)
	Optional TCAM	Mezzanine board with Interlaken-LA
LMP Subsystem	Processor	QorIQ P2041@1.2GHz, Quad core
	DRAM Memory	1x mini VLP UDIMM, ECC DDR3 @666MHz, 2GB
	Boot Flash Memory	2x 8 Mbit (SPI EEPROM, redundant)
	OS Flash Memory	2x 8 GB (chip SSD, redundant)
Data Interconnection Subsystem	Ethernet Switching	BCM56842, Non-blocking L2/L3 switch fabric with QoS Support.
I/O Interface	10G Interface	4x SFP+ (10G/1G)
	10/100/1000BASE-T, Management	One RJ-45 for LMP One RJ-45 to Base Switch (for NPUs)
	Serial (UART), Console	3x RJ-45 serial ports – One for LMP or IPMC – Two for NPs
Shelf Management	Blade Operation and Management	IPMI v2.0
Backplane Connection	Base Interface	Zone 2, 1000BASE-T Ethernet, dual star
	Fabric Interface	Zone 2, PICMG 3.1 Option 3, Option 9, KR and 40G Ethernet in 40GBase-KR4, dual star
Power	Power distribution	Front Blade: 320 watts max. w/o TCAM RTM: 25 watts max.
Environment	Temperature	Operating: +0°C to 50°C Non-operating: -40° to +70°C
	Relative Humidity	Operating: 0 – 95% @40°C Non-operating: 5-95%
	Shock	Operating: TBD Non-operating: TBD
	Vibration (5-500Hz)	Operating: TBD Non-operating: TBD
	Altitude	TBD
Software	Bootloader	U-boot (LMP, NPs)
	BSP	ADLINK BSP (LMP, NPs)
	Operating System	Open Linux (LMP, NPUs)
	Development Environment	Cavium/Broadcom SDK

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The build options of the blade enable users to have cost efficient, application optimized version of the blade. Table 2-2 summarizes the build options of the blade. The build options are applied to the blade usually during the factory build procedure.

Table 2-2 aTCA-N700 build options

Feature	Build option	Description
Mezzanine Board	Pass through mezzanine	Traces only. Bare connections. TBD.
	TCAM mezzanine	TBD.
LMP DRAM	2GB (TBD)	This is a choice of VLP mini DIMM module capacity. Field replaceable.
NPU DRAM	8GB/DIMM (TBD)	This is a choice of VLP DIMM module capacity. Field replaceable.

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3. External Interfaces

The aTCA-N700 has common external interfaces and optional external interfaces depending on model type. The traffic ports are optionally available either from the front faceplate or from the RTM faceplate.

3.1. Front Panel

The face plate of the main blade has the following components:

- LED-OOS: Out Of Service indicator
- LED-Power GOOD: Power indicator
- LED-Health: Health indicator
- LED-Fabric Interface: Fabric Interface Link Activity indicator
- LED-Base Interface: Base Interface Link Activity indicator
- LED-HS: Hot Swap indicator
- LED-MGMT LINK/ACT: Management Port Link/ACT indicator
- LED-MGMT SPEED: Management Port Speed indicator
- LED-Service Ports Enable/Act: Service Port indicator
- Console Port #1~#3: serial ports
- USB Port: Connected to LMP
- Management Ethernet Port #1~#2: 10/100/1000BASE-T
- Reset Recess Button: System Reset PUSH switch
- Service Ports #1~#4: Four SFP+ ports for data plane interface



Figure 3-1 aTCA-N700 Front Panel

3.1.1. Console Port

Three console serial ports are provided in RJ45 shield connector outlets. One port is connected to the LMP, which enables access to all the major devices and command line interface commands for configuration and monitoring. This port is also configured to be shared with IPMC. Two additional ports are connected to the OCTEON II NPUs. The serial port configuration is RS232 compatible including XON/XOFF, baud rate, stop, and start bit setting. The label for the console port is visibly different from the management Ethernet port to avoid ambiguity that may be caused by the same RJ45 connector type. The pin-out of the serial interface RJ-45 connector is compatible to Cisco serial port pin out as shown in Table 3-1 and the configuration values in Table 3-2.

Table 3-1 Serial Console Port Pin-out

Pin	Function
1	RTS
2	NC
3	TXD
4	GND
5	GND
6	RXD
7	NC
8	CTS

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Table 3-2 Serial Console Port Configuration Value

Item	Value
Baud rate	115200
Data	8bit
Parity	None
Stop Bit	1bit
Flow control	None

3.1.2. USB Port

A single USB port is available on the face plate, which is connected to the LMP. The P2041 supports 2x USB compliant to USB specification Rev 2.0. On the board, USB2 is routed to the faceplate USB connector. USB1 is not used.

3.1.3. Management Ethernet Port

Two RJ-45 Ethernet ports are provided from the front panel. One 10/100/1000BASE-T port is connected to the LMP directly, for easier debugging/testing (such as simple connection to a different subnet console by configuring a necessary IP address for the port without involvement of the blade switch). Another port is connected to the base switch to reach the NPUs. The labels for the management Ethernet port are visibly different from the console port to avoid ambiguity that may be caused by the same RJ45 connector type.

Table 3-3 RJ-45 Management Port Pin-out

Pin	Signal Name	Comments
1	BI_DA+	Bi-directional lane 1, positive polarity
2	BI_DA-	Bi-directional lane 1, negative polarity
3	BI_DB+	Bi-directional lane 2, positive polarity
4	BI_DB-	Bi-directional lane 2, negative polarity
5	BI_DC+	Bi-directional lane 3, positive polarity
6	BI_DC-	Bi-directional lane 3, negative polarity
7	BI_DD+	Bi-directional lane 4, positive polarity
8	BI_DD-	Bi-directional lane 4, negative polarity

3.1.4. Service Ports

Four traffic service ports are provided with SFP+ outlets. Either a fiber optic cable or a copper cable with a mating SFP+ connector can be used to connect the blade with remote blades or appliances. The SFP+ ports will support IEEE 802.3ae (Clause 52), IEEE 802.3aq (Clause 68).

3.1.5. Reset Switch

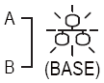
The front panel reset switch is a global reset switch of the blade. With a push, a payload reset event is notified to the IPMC to begin corresponding initialization procedures.

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3.1.6. LEDs and Markers

Various LEDs for system status monitoring are available from the faceplate. Shown in Table 3-4 are the LEDs and their descriptions.

Table 3-4 Front Panel LEDs and Markers

Name	Marker	Display	Description
HS LED		Blue Solid	DC-DC Power OFF(M1)
		Blue Short Blink	Hot swap Operation(M5/M6)
		Blue Long Blink	Hot swap Operation(M2)
		OFF	Normal Operation(M3/M4)
OOS LED		Red Solid	Out of Service(M1)
		Red Blink	Out of Service or Service Preparation (M5/M6)
		OFF	Normal Operation (M3/M4)
Power GOOD LED		Green Solid	Power GOOD
		OFF	Power Fail
Health LED	APP	Amber Solid	Health Check
		OFF	Normal Operation
Fabric I/F LED [2:1]		Amber Solid	Fabric Link ON
		Amber Blink	Fabric Link ON & Activity
		OFF	Fabric Link OFF
Base I/F LED [2:1]		Amber Solid	Base Link ON
		Amber Blink	Base Link ON & Activity
		OFF	Base Link OFF
MGMT Link/ACT LED		Green Solid	MGMT Link ON
		Green Blink	MGMT Link ON & Activity
		OFF	MGMT Link OFF
MGMT Speed LED		Yellow Solid	1G speed Indicator
		OFF	10/100Mbps Speed Indicator
Service Port	**E**	Green Solid	1G or 10G Link ON
		OFF	Link OFF
	L/A	Green Blink	1G or 10G Activity
		OFF	No Activity
Console Port		N/A	Section 3.1.1
USB Port		N/A	Section 3.1.2
MGMT Port		N/A	Section 3.1.3
Reset		N/A	Section 3.1.5

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3.2. Zone 2 Backplane Interfaces

ATCA specifications define Zone 2 for Fabric, Base and update channel interface interconnections. The Base Interface port is compliant to 1000BASE-T Ethernet. Two Base Interface ports from the backplane to support dual star hub are connected to the Ethernet switch in the blade. Through the switch, the Base Interface traffic goes to the LMP for necessary processing. The Fabric Interface supports a dual star configuration, in which the blade connects to two switch fabric boards in the chassis in a primary/redundant operation. The two Fabric Interface ports are connected to the high capacity on-board Ethernet switch, where the port speed is configurable to 1Gbps/10Gbps/40Gbps in the form of one SerDes lane at 1Gbps or 4 SerDes lanes at 2.5Gbps each or 4 SerDes lanes at 10Gbps each to be compliant with option 3/9, 10GBase-KR, 4x10GBase-KR or 40GBase-KR4 (40G Ethernet) respectively. Detailed signal definitions can be found in the Appendix.

3.3. Zone 3 Backplane Interface for Rear Transition Module

The Zone 3 connectors are reserved for the rear transition module (RTM). Supporting different types of RTMs per different application is an essential element for adaptation of the blade. The interface is composed of the data plane interface, the control plane interface, and the auxiliary interface. For the data plane interface, Twelve 10Gbps SerDes lanes are routed to the Zone 3 connectors. The twelve SerDes lanes are connected to the high capacity on-board switch. The SerDes lanes can be configured for either twelve SFI 10G ports or up to three XLAUI 40G or equivalent ports. Other auxiliary interfaces include an I2C connection to support managed RTMs. See Appendix for the detailed signal definitions.

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4. Installation and Operation

Before installing the ATCA-N700, make sure that the following are ready or checked to insure proper installation and operation:

- An ATCA chassis with a reserved slot for the aTCA-N700.
- A console PC that runs a serial port monitoring or terminal emulation program
- Software: All the necessary software and firmware are programmed into the EEPROM/flash memories upon delivery of the board



Figure 4-1 aTCA-N700

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4.1. Hardware Configuration Setting

For normal operation, it is not recommended to change any on-board hardware configuration settings, but there are some options on the board for those want to investigate more flexibility for testing. Figure 4-2 illustrates the locations of the configurable components

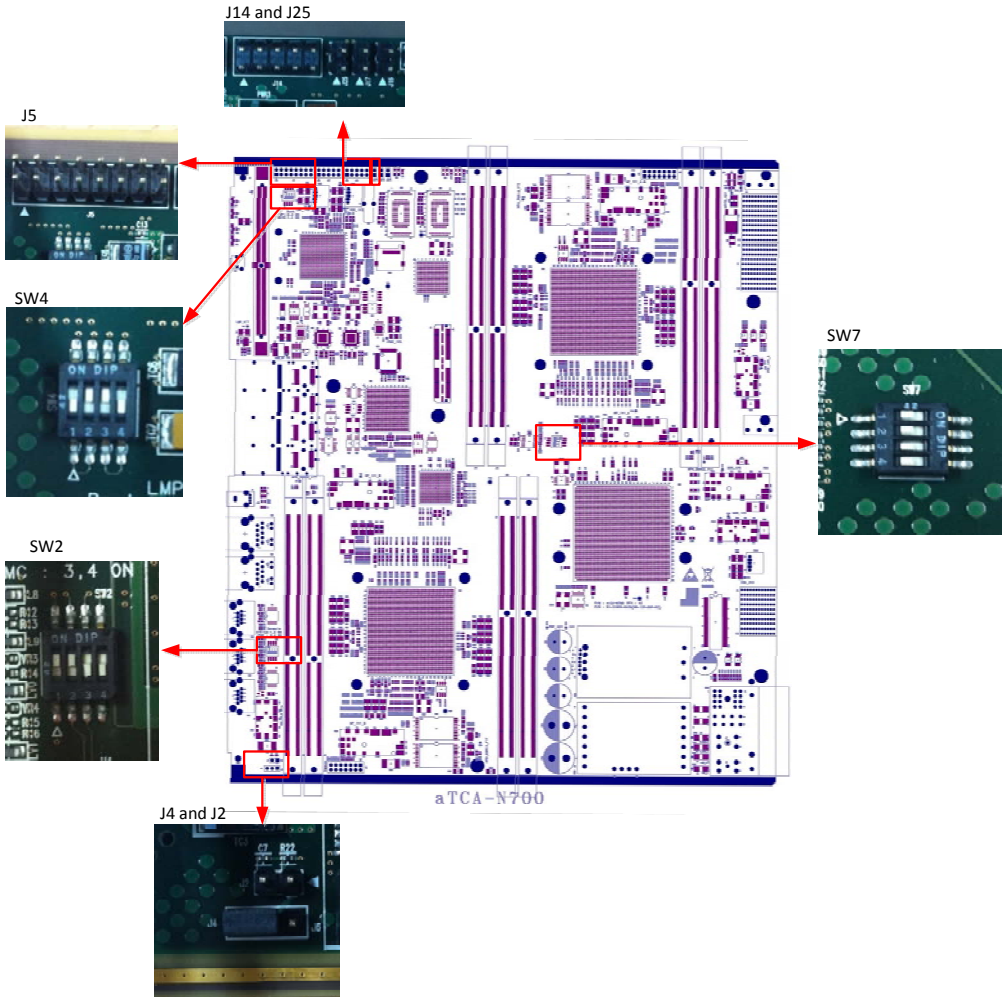


Figure 4-2 Configurable Component Locations

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4.1.1. Headers and Jumpers

1) CPLD JTAG Header (J14): This header is used to reprogram the CPLD bit file using a JTAG cable.

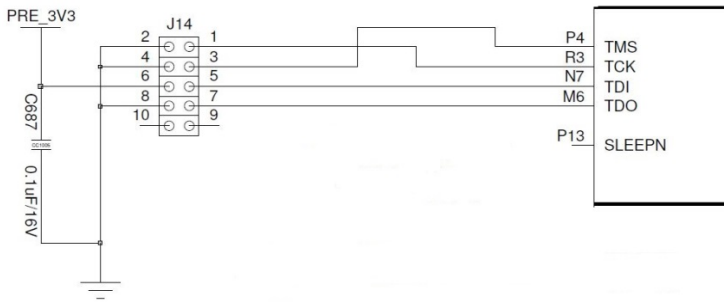


Figure 4-3 CPLD JTAG Header

2) COP-Header (J5): This header is used to access the LMP for a necessary debugging situation to connect to the debug monitor.

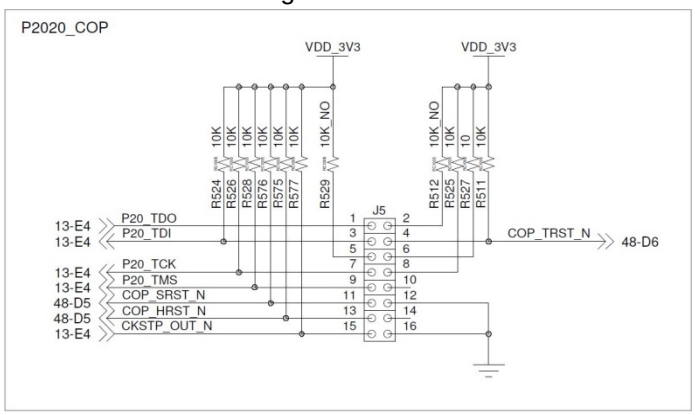


Figure 4-4 COP Header

3) Standalone mode selector Header (J25): The header is used when a shelf manager is not available. Put a cap on the header to connect pin 1 and pin 2 for stand-alone mode.

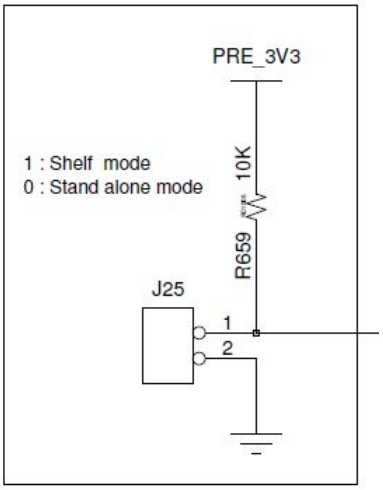


Figure 4-5 Standalone Mode Selector Header

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Table 4-1 Shelf Manager Interoperability Mode Setting: J25

Operating Mode	Condition
Stand-alone mode	Closed
Shelf mode	Open

4) Hot swap switch selector Header (J4): The Header can select SW6 or SW3

Hot swap switch close Header (J2): If Pin 1 and 2 of J2 are closed, it is the same as the closed Hot swap switch.

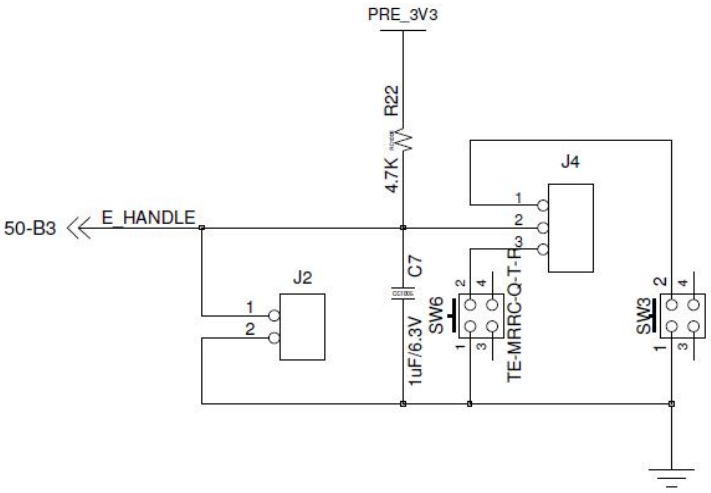


Table 4-2 Shelf Manager Interoperability Mode Setting: SW3, SW6

Switch	Condition
SW3	Pin1, 2 Closed, Pin3 Open
SW6	Pin 2,3 Closed, Pin1 Open

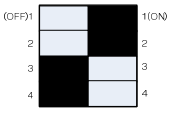
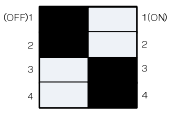
Note: SW6 is recommended.

4.1.2. DIP Switch

1) SW2:

The faceplate serial port is set for the LMP console as a default. For testing purposes, the serial port can be configured to connect to the IPMC console as depicted in the following table.

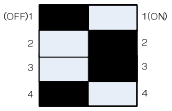
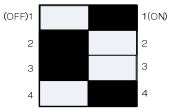
Table 4-3 Faceplate serial port selection

SW NO	Mode	Setting	Figure
SW2	LMP Console	1 ON 2 ON 3 OFF 4 OFF	
	IPMC Debug Console	1 OFF 2 OFF 3 ON 4 ON	

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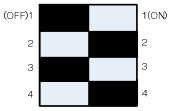
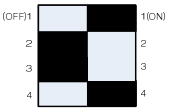
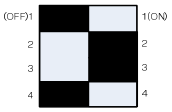
2) SW4:
SW4 can switch between an SPI flash boot or an SD Card boot.

Table 4-4 SPI Flash or SD Card selection

SW NO	Mode	Setting	Figure
SW2	SPI Flash	1 OFF 2 ON 3 ON 4 OFF	
	SD Card	1 ON 2 OFF 3 OFF 4 ON	

3) SW7:
SW7 supports remote booting from the LMP. Top (F) or Bottom (S) is supported respectively.

Table 4-5 Remote control selection

SW NO	Mode	Setting	Figure
SW7	Normal operation	1 OFF 2 ON 3 OFF 4 ON	
	F_OCTEON Remote Control select	1 ON 2 OFF 3 OFF 4 ON	
	S_OCTEON Remote Control select	1 OFF 2 ON 3 ON 4 OFF	

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4.1.3. Programmable Devices

There are programmable devices with their own images on the board. The board is provided with default images programmed for all the mandatory devices, and most of them are upgradable as described in Table 4-6.

Table 4-6 Programmable devices

Component	Part Number	Content	Remarks
NAND flash memory	MT29F16G08ABABA	Linux and user application	
SPI flash memory	SST25VF080B	Uboot image	
IPMC	A2F500M3G-FGG484I	IPMC image	
EEPROM	M24256 (256Kb)	IPMI variables	
NOR flash memory	JS48F4400P0TB00A	Linux and user application	Optional to replace NAND flash
Micro-SD card	4GB	Linux and user application	
CPLD	LCMX0640C-3FTN256C	CPLD Image	

4.2. Hardware Installation

The steps required to install the ATCA-N700 are the following: Front Blade installation, RTM installation, Monitoring Station connection, and Traffic Port connection.

4.2.1. Front Blade

The board should be plugged in as per the following procedures:

Step 1: The injector handles (top and bottom) shown in Figure 4-6 should be opened to plug the board into a chassis slot.
Step 2: The board should be aligned on to the rail (marked as (A)) in the reserved slot for the board
Step 3: Slide the board into the chassis until the guide of the faceplate and the hole of the chassis meet as in (B)
Step 4: Once the guide of the faceplate slides into the hole, close the upper injector handle so that the handle wedge goes into the handle hole and makes a click sound.

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Step 5: When the chassis is powered up and in operation, during plugging-in the board (Hot Swap situation), the board starts booting up as soon as the handles are fully closed in Step 4.

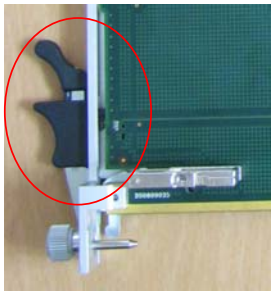


Figure 4-6 In/Ejector handle (bottom side)

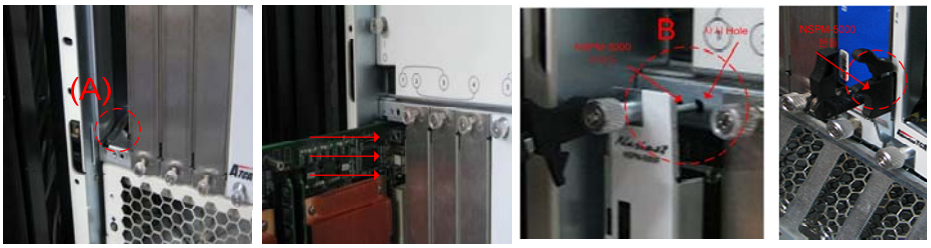


Figure 4-7 Plugging the Board

Note*: After plugging in the board, make sure that the injector handle is locked into the hole on the faceplate. This will trigger the hot swap switch activated and booting will start.

To pull out the main board, follow the steps described in the following:

Step 1: The bottom side injector handle should be slightly pulled out to the front from the hole without pulling out the board.
Step 2: Once the injector handle is out from the hole, the Hot Swap switch becomes OPEN
Step 3: The Hot Swap LED (or Blue LED) should then start blinking and it will stay ON after several seconds, which indicates the READY status.
Step 4: At the READY status, completely open the top and the bottom handles and pull out the board from the chassis.

4.2.2. RTM

The optional RTM1 that provides rear side loading of SFP+ ports can be installed to interwork with the front blade with the very similar procedures described in the front blade case. The front blade should be plugged in first. Refer to the RTM Users Guide for the details

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4.2.3. Console Port Connection

Use an RJ-45<->DB9 cable or an RJ-45<->USB cable provided to connect to the console PC depending on the outlet type of the PC. The RJ-45 plug should be plugged in to the faceplate RJ-45 receptacle.

To use a USB port from the console PC for serial connection, proper PC COM port emulation on USB software should be installed on the PC.

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5. Architecture Overview

The *aTCA-N700* is composed of several major subsystems: the network processor subsystem, the data plane interconnection subsystem, the control plane interconnection subsystem, the I/O subsystem, the shelf management subsystem, the power/clock distribution subsystem and the optional RTM subsystem.
The network processor subsystem has two sets of OCTEON II CN6880 network processor units and their essential components, which perform as the core functional block in the blade. The data plane interconnection subsystem includes a 320Gbps capacity Ethernet switch and its components, which are used for interconnecting the data plane traffic among the CN6880s, the backplane, and the service ports. The backplane connections include the Base Interface in 1000BASE-T Ethernet, and the Fabric Interface configurable to be compliant with PICMG3.1 Option 3 (4Gbps Ethernet, 4 lanes) or Option 9 (10Gbps Ethernet, 4 lanes), 10GBase-KR (10G Ethernet@1x lane) or 40GBase-KR4 (40Gbps Ethernet@4x lanes) support depending on the HUB slot configuration.
The control plane interconnection subsystem includes a dedicated Base Gigabit Ethernet switch that switches various control traffic among the control plan components including two Base Interface ports.
The I/O subsystem includes all the I/O related blocks such as the front panel interface, and the RTM interface. The shelf management subsystem includes the IPMC and its associated interfaces to support the ATCA chassis/shelf/blade management for the external Shelf Manager. The architecture is illustrated on Figure 5-1. The details of each subsystem are described in the following sections.

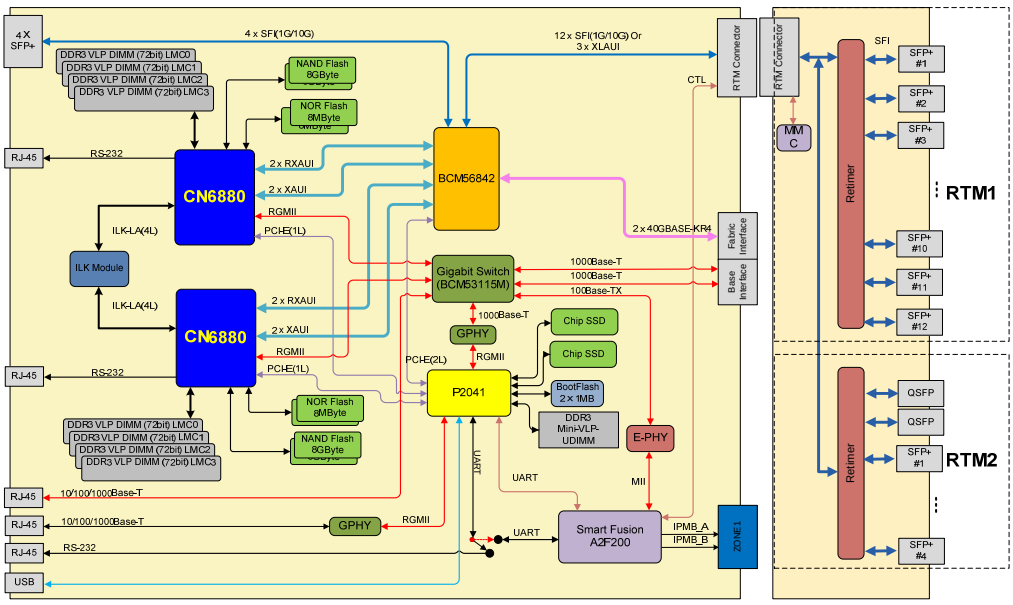


Figure 5-1 aTCA-N700 Architecture with optional RTMs

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6. Network Processor Subsystem

The major component of the network processor subsystem is the OCTEON II, CN6880 network processor from Cavium. OCTEON CN68XX family devices provide an architecture that guarantees software backward compatibility for CN5XXX family. The CN68XX family devices use the same cnMIPS II CPU core and same on-chip architecture. The features of the CN68XX are summarized as the following.

- Highly-integrated networking security/application processor
- MIPS64® integer instruction set, highly programmable
- High-performance architecture with up to 32 cnMIPS™ II processor cores
- Dual control- and data-plane support
- Standalone (i.e. self-bootable) or device support
- Core frequency up to 1.5 GHz, producing up to 96.0 GOPS in a single chip
- Line-rate performance of 40 Gbps with small packets
- Excellent performance/watt
- Hardware cryptographic (MD5, SHA-1, SHA-256, SHA-512, DES/3DES, AES, KASUMI, SNOW 3G, SMS4, modular exponentiation, and Galois field multiplication) and CRC acceleration
- Hardware packet processing acceleration
- Hardware work queuing, scheduling, ordering, and synchronization
- Hardware TCP acceleration, including checksum and timer
- High-bandwidth on-chip memory system including a 4MB 16-way set-associative L2 cache
- Fully coherent memory system
- Quad 72-bit DDR3 DRAM interfaces, up to 1333 MHz data rate
- Support for DDR3L 1.35-mode operation
- Hardware regular expression acceleration engine (3rd generation)
- One USB 2.0 MAC/PHY
- One RGMII or MII interface
- Up to three packet interfaces with either SGMII (up to ×4) or XAUI (×4)07/18/2011

- Up to two RXAUI interfaces
- Two optional PCI Express® (PCIe®) 2.0 interfaces with ×1/×2/×4/×8 lanes
- One optional Interlaken (ILK) controller with ×1/×2/×4 dedicated lanes or ×8 using four additional shared lanes (shared with one of the SGMII/XAUI interfaces)
- Secure on-chip key memory
- Cryptographic random-number generator
- Option to boot using NAND flash device
- Hardware compression/decompression acceleration
- Hardware RAID acceleration
- Hardware de-duplication acceleration

Figure 6-1 illustrates the Network Processor Subsystem. The blade has two identical sets of CN6880 circuitry. There is an optional mezzanine board which may have TCAM(s). The mezzanine board is connected to both CN6880s in 4 lanes of Interlaken-LA interface. Each set of NPUs has its own NOR boot flash memory and NAND OS flash memory in a redundant configuration. Four VLP DIMMs per NPU are populated on the board to host up to 32GB (8GB per DIMM module, but expandable further to 120GB with higher density memory modules when available). 40Gbps capacity of the data path per NPU is connected to the fabric switch with two RXAUIs and two XAUIs interfaces. The control path is connected to the base switch in RGMII interface and in PCI express to the P2041 LMP.

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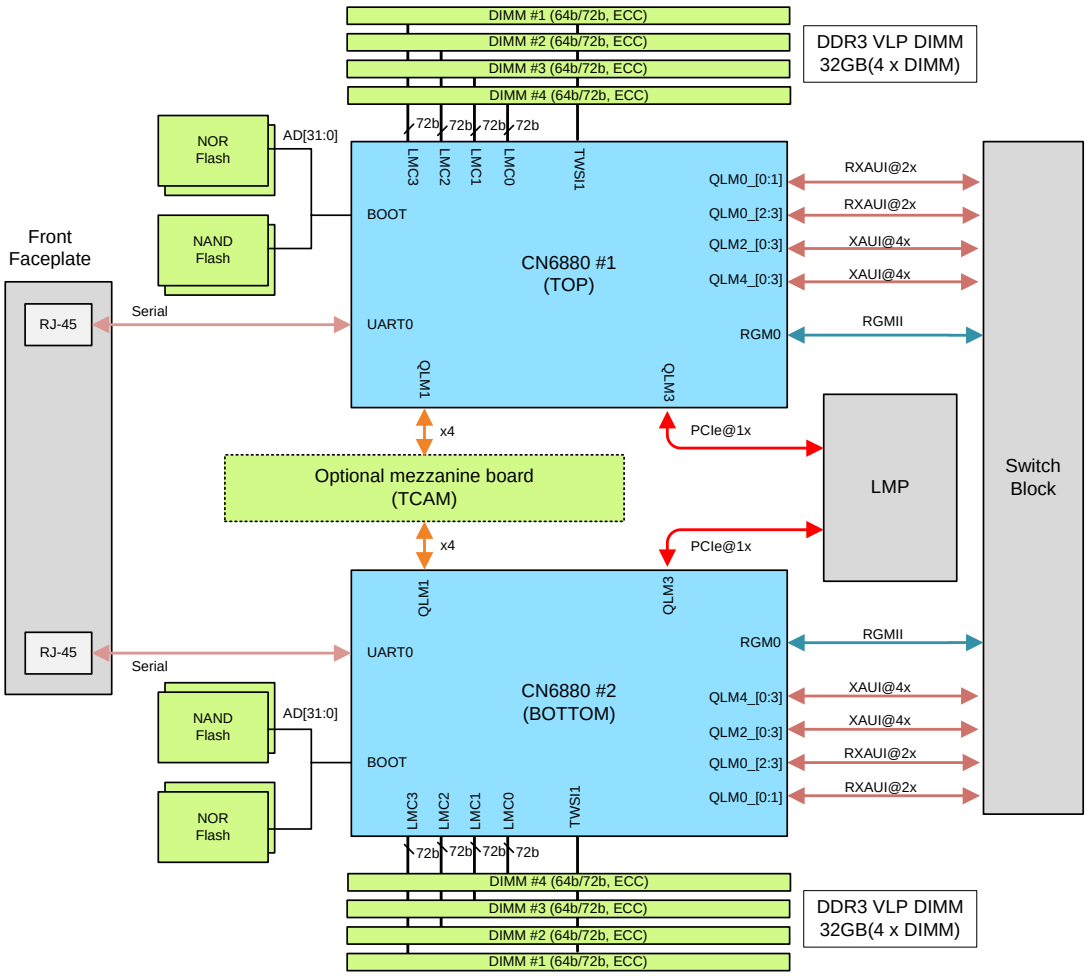


Figure 6-1 Network Processor Subsystem

6.1. CN6880 Embedded Components

Figure 6-2 illustrates the block diagram of the CN68XX devices. Detailed explanations can be found in the "*Cavium Networks OCTEON II CN68XX Hardware Reference Manual*". The biggest customization on the board may be the data plane interfaces along with their SerDes configurations. The CN6880 provides four internal SerDes blocks that can be configured to provide different types of the interfaces, which will be covered in later sections. The device has four internal DDR3 Memory Controllers (LMC0~LMC3) with four external DDR3 SDRAM interfaces connected to these controllers. These DDR3 interfaces enable up to 128GB of DDR3 memory installment or 32GB/Controller, if there are devices of enough capacity.

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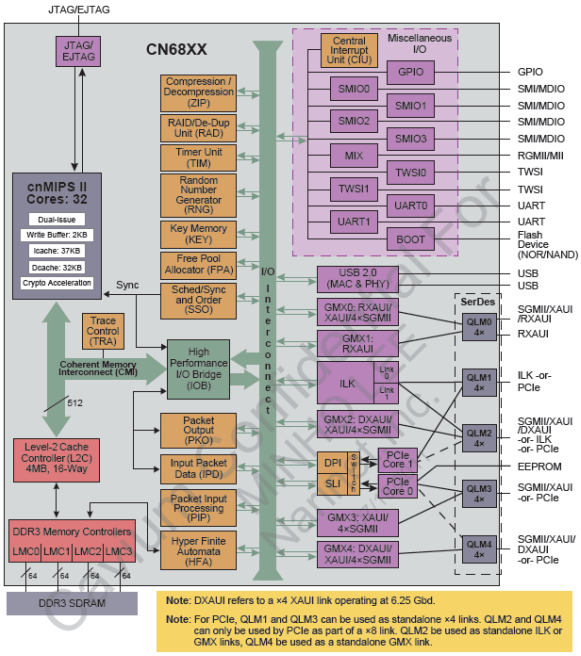


Figure 6-2 CN68XX Internal Blocks

6.2. DRAM Memory

Each DDR3 interface connected internally to each DDR3 Memory Controller is routed to a DIMM module. Total of four DIMM slot connections are attached to this interface. Such connections are illustrated in **Figure 6-3**.

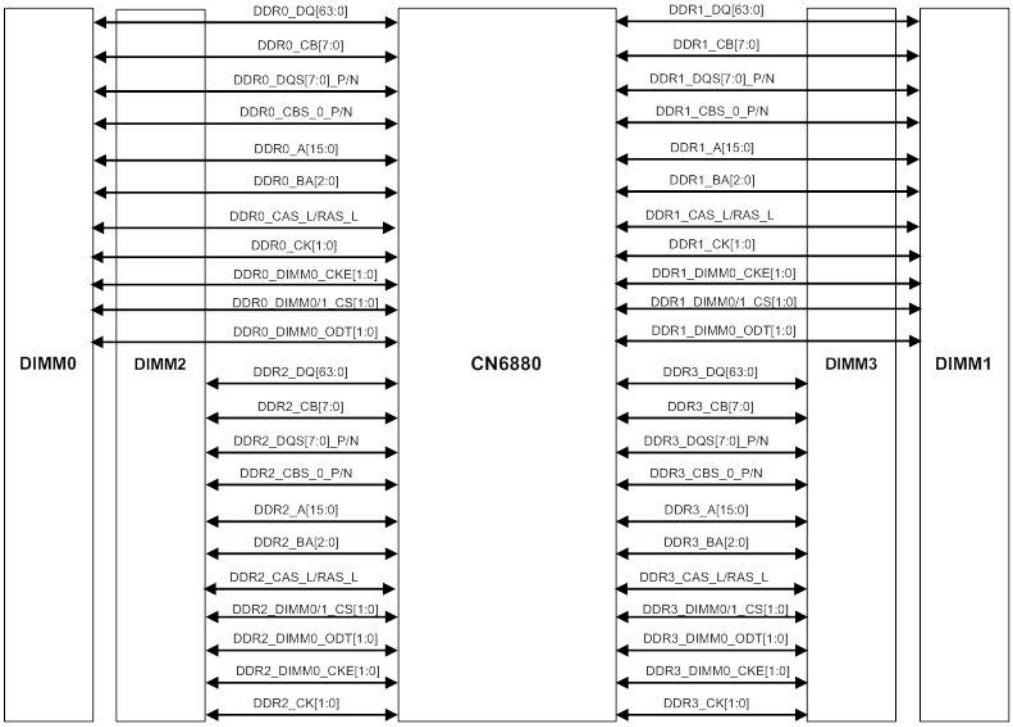


Figure 6-3 CN6880 DRAM Memory

Even though each internal controller LMC supports up to 32GB of capacity, due to the limitation on the devices of such capacity, each DIMM is anticipated to support only up to 8GB at the time of the design, or 32GB/NPU. The interface runs at up to 1333MHz of dual

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data rate operating at up to 667MHz of clock. Each DIMM interface is in 64bit + ECC (72bit). Two dual-rank DIMMs, x8, x16bit DRAM parts, registered and un-buffered DIMMs are supported. The DIMM configuration is done through the TWSI1 interface.

6.3. Boot/OS Memories on Boot-Bus

The CN6880 has an internal boot module, which provides an external booting device interface through a general purpose bus, or so called Boot-Bus. The Boot-Bus has 32bit address/data multiplexed lines, programmable to 8/16bit data width. The boot and the OS memories are installed through the Boot-Bus interface as illustrated in **Figure 6-4**. The NOR flash is used for u-boot image storage and the NAND flash is for OS/APP image storage. Both memories support 1:1 hardware redundancy.
The NOR flashes are installed in 2 (primary, secondary) x 8MB fashion per NPU on CE0. Likewise, the NAND flashes are installed in 2 (primary, secondary) x 8GB fashion per NPU on CE1, 2, 3 and 4.

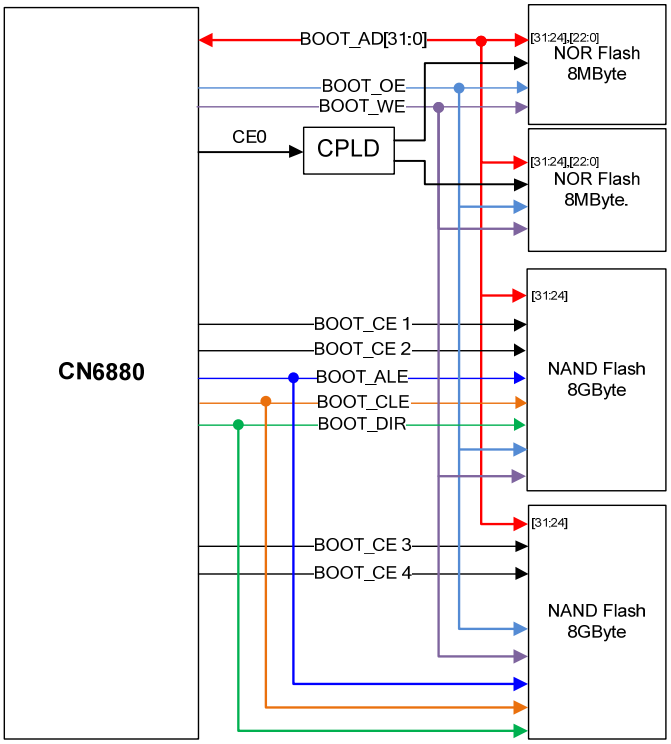


Figure 6-4 Boot Memories

6.4. Data Plane Interface

The CN6880 data plane interfaces are provided via QLM0 ~ QLM4, which are then, connected to the different types of internal interface modules.
On the board, QLM0 is connected to provide 2x RXAUI (20Gbps@*4 lanes*) to save SerDes lanes.
QLM2 and QLM4 are configured to provide 2x XAUI (20Gbps@*8 lanes*)
These 4x 10G ports are connected to the fabric switch BCM56842 as can be seen in **Figure 6-5**. Note that each RXAUI interface consumes two SerDes lanes, where each lane running at 6.25Gbps, whereas each XAUI consumes four lanes, each lane@3.125Gbps.

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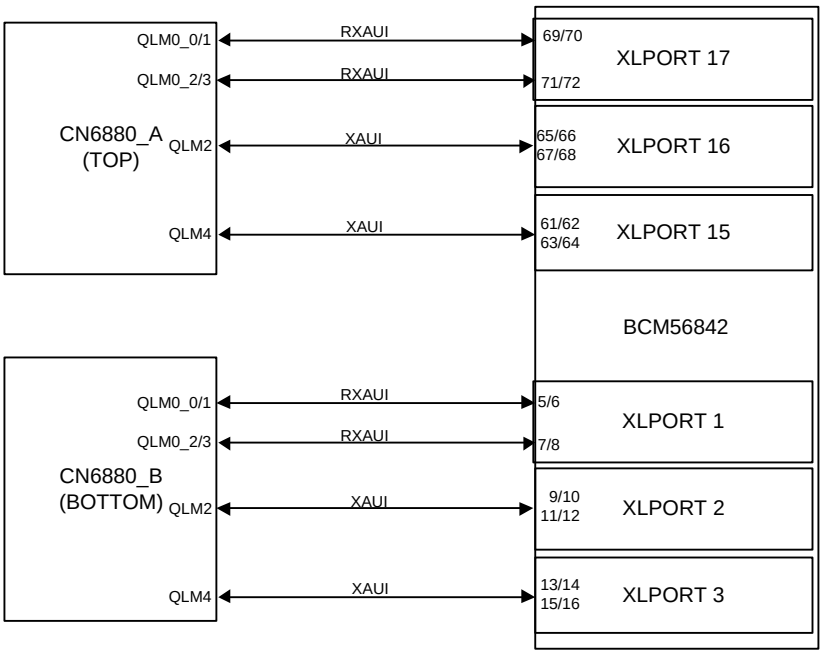


Figure 6-5 Data Path Interface

6.5. Mezzanine Board Interface (Optional)

The QLM1 interface of each NPU is routed to the optional mezzanine board connector in Interlaken-LA interface (aggregated rate of 25Gbps by 4 lanes). Depending on the mezzanine board type, two NPUs can be interconnected together with this interface or TCAM can be attached. Figure 6-6 illustrates the connections.

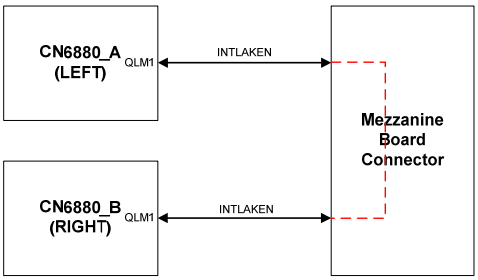


Figure 6-6 Mezzanine Board Interface

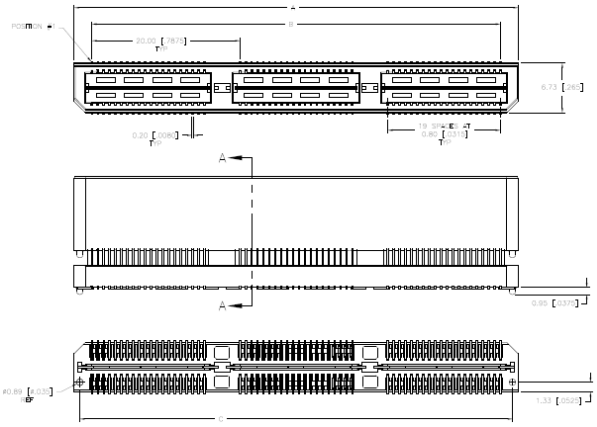


Figure 6-7 Mezzanine Board Connector

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The mezzanine connectors should be able to pass 6.25Gbps Interlaken-LA signals at sustainable quality. The MICTOR 1-1658016-2, 80 position connector as shown in Figure 6-7 is used. 12V supply voltage is fed to the mezzanine board with sufficient number of pins in the connector (signals require 32pins, and the rest are for power and GNDs).

6.6. Host Interface

The CN6880 is capable of providing a 4 lanes @5Gbps PCI-e interface, but due to limitation on the LMP, between the LMP and each CN6880, a 1x @2.5Gbps PCIe interface is provided on the board as can be seen in **Figure 6-8**. The PCIe interface is used for configuration and management of the CN6880. It could also be used for frame exchanges between the LMP and the CN6880, with DMA enabled. All the PCI-e clocks to devices are from a single clock buffer.

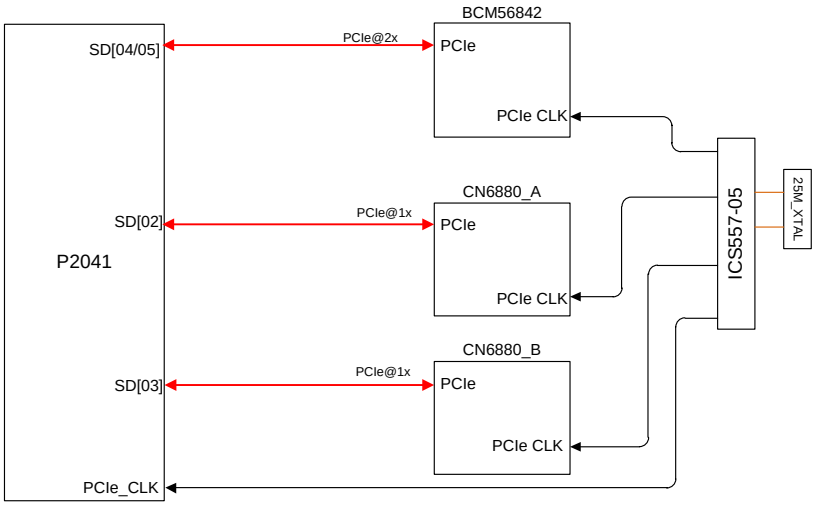


Figure 6-8 Host Interface – PCIe

The management Ethernet ports from each NPU are connected to the Base Interface switch as can be seen in **Figure 6-9** via RGM0 interface. The base switch also provides a connection to P2041 LMP, for the NPUs to connect to the LMP.

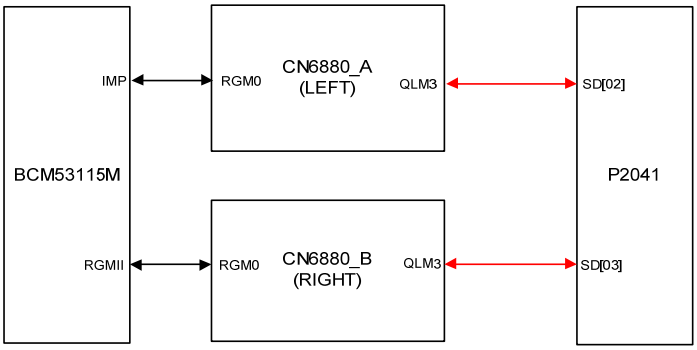


Figure 6-9 Host Interface - Ethernet

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6.7. UART Interface

The NPU provides UART interface from the device directly, which is modeled after the industry standard 16550. Each UART interface from *UART0* is routed to the faceplate of the board with an RJ-45 form factor outlet. Users can attach two independent console ports to simultaneously monitor both NPUs. The console pin maps and default setting can be found in 3.1.1.

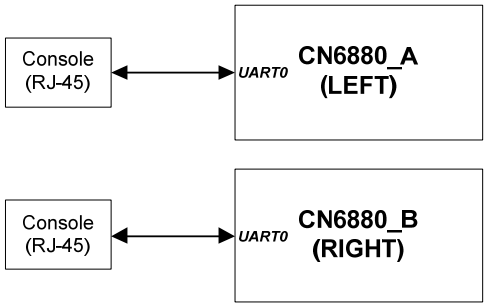


Figure 6-10 Console Port Connection

6.8. TWSI (I2C) Interface

The NPU provides 2x TWSI interfaces, namely, *TWSI0* and *TWSI1*. Of the two interfaces only *TWSI1* is used and connected as in **Figure 6-11**. It configures four DIMMs, where each hard-wired address is configured on the board as 0x50, 0x52, 0x54, and 0x56 respectively.

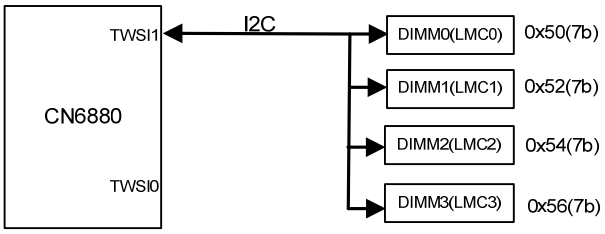


Figure 6-11 TWSI (I2C) Connection

The TWSI interface supports:

- Standard mode (100Kbps) and fast mode (400Kbps)
- 7bit and 10bit addressing. (7b is used on the board)
- Master and slave support
- Multi master support

6.9. Other Interfaces

The USB interfaces from the NPU are not used and are left unconnected.
The MDC/MDIO for external PHY control are not used and are left unconnected.

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6.10. GPIO

The GPIO pins are arranged on the board as shown in Table 6-1. The CPLD is responsible for the interfaces between the NPs and the LMP. Some of such interfaces depend on the GPIO connections to the CPLD, which may be used as I/O mapping on to the CPLD registers so that the LMP or the NPs can perform read/write operations to the other end. Interrupt forwarding from the NPs to the LMP is an example on using GPIO-to-CPLD connections.

Table 6-1 GPIO Pins

Signal Name	Description	Setting Value
GPIO0	Connected to CPLD	Reserved
GPIO1	Connected to CPLD	Reserved
GPIO2	Connected to CPLD	Reserved
GPIO3	Connected to CPLD	Reserved
GPIO4	EVENT of DIMM Memory	DIMM Memory Event Input
GPIO5	Connected to CPLD	Reserved
GPIO6	Connected to CPLD	Reserved
GPIO7	Connected to CPLD	Reserved
GPIO8	Connected to CPLD	Reserved
GPIO9	Connected to CPLD	Reserved
GPIO10	Connected to CPLD	Reserved
GPIO11	Connected to CPLD	Reserved
GPIO12	Connected to CPLD	Reserved
GPIO13	Connected to CPLD	Reserved
GPIO14	Connected to CPLD	Reserved
GPIO15	Connected to CPLD	Reserved

6.11. Clock

The CN6800 has a single reference-clock signal (PLL_REF_CLK, 50MHz) that feeds into three PLLs: Core PLL, Coprocessor PLL, and DDR PLL) that provide the clock signals for the rest of the chip.
Also, the clocks fed externally on the blade include: QLM reference (PCIe Gen2), QLM reference (ILK), QLM reference (XAUI), QLM reference (RXAUI/DXAUI) and RGMII reference clocks. Their requirements are copied to **Figure 6-12** from the datasheet, respectively. The on-board clock tree is described in Section 11 .

Table 33–1 Core/Coprocessor/DDR Reference-Clock

Clock Name	Frequency	Frequency Tolerance	Duty Cycle	Phase Jitter (rms)[1]	Phase Jitter (p-to-p)	Edge Rate [2]	Voltage Levels
PLL_REF_CLK	50 MHz	±150 ppm	60/40	4 ps	110 ps	4 ns	0–3.3V single-ended

1. From 12 kHz to 20 MHz.
2. Edge rate, defined as 20%–80% value, specifies worst case.

Table 33–8 QLM Reference-Clock Input: PCIe (Gen2)

Clock Name	Frequency	Frequency Tolerance	Duty Cycle	Phase Jitter (rms)	Phase Jitter (p-to-p)	Edge Rate[1]	V_{HIGH} Levels			V_{LOW} Levels		
							Min	Nom	Max	Min	Nom	Max
QLM*n*_REF_CLK_N/P	100 MHz	±300 ppm[2]	60/40	see spec[3]	see spec[3]	840ps	325mV	700mV	850mV	-150mV	0V	175mV

1. Edge rate is defined as 20%–80% value.
2. In links where a spread spectrum-modulated reference clock is used, both ends of the link must share the same master reference-clock source.
3. Refer to PCIe Base 2.1 Specifications Under Common Clock Architecture, Table 4-16.

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Table 33–11 QLM Reference-Clock Input: ILK

Clock Name	Frequency	Frequency Tolerance	Duty Cycle	Phase Jitter (rms)[1]	Phase Jitter (p-to-p)	Edge Rate[2]	V_{HIGH} Levels			V_{LOW} Levels		
							Min	Nom	Max	Min	Nom	Max
QLM*n*_REF_CLKN/P	156.25 MHz	±100 ppm[3]	60/40	2 ps	44 ps	840ps	325mV	700mV	850mV	–150mV	0V	175mV

1. From 12 kHz to 20 MHz.
2. Edge rate is defined as 20%–80% value.
3. In links where a spread spectrum-modulated reference clock is used, both ends of the link must share the same master reference-clock source.

Table 33–17 QLM Reference-Clock Input: XAUI

Clock Name	Frequency	Frequency Tolerance	Duty Cycle	Phase Jitter (rms)[1]	Phase Jitter (p-to-p)	Edge Rate[2]	V_{HIGH} Levels			V_{LOW} Levels		
							Min	Nom	Max	Min	Nom	Max
QLM*n*_REF_CLK_N/P	156.25 MHz	±100 ppm[3]	60/40	3 ps	70 ps	840ps	325mV	700mV	850mV	–150mV	0V	175mV

1. From 12 kHz to 20 MHz.
2. Edge rate is defined as 20%–80% value.
3. In links where a spread spectrum-modulated reference clock is used, both ends of the link must share the same master reference-clock source.

Table 33–20 QLM Reference-Clock Input: DXAUI/RXAUI

Clock Name	Frequency	Frequency Tolerance	Duty Cycle	Phase Jitter (rms)[1]	Phase Jitter (p-to-p)	Edge Rate[2]	V_{HIGH} Levels			V_{LOW} Levels		
							Min	Nom	Max	Min	Nom	Max
QLM*n*_REF_CLKN/P	156.25 MHz	±100 ppm[3]	60/40	2 ps	44 ps	840ps	325mV	700mV	850mV	–150mV	0V	175mV

1. From 12 kHz to 20 MHz.
2. Edge rate is defined as 20%–80% value.
3. In links where a spread spectrum-modulated reference clock is used, both ends of the link must share the same master reference-clock source.

Table 33–21 RGMII/MII Reference-Clock Input

Clock Name	Frequency	Frequency Tolerance	Duty Cycle	Period Jitter (P–P)[1]	Edge Rate[2]	Levels
RGM0/1_RXC_MI0/1_RXCLK (MII)	25 MHz	±150 ppm	60/40	1 ns	5 ns	0.0–VDD_MII
RGM0_REF_CLK_MI0_TXCLK/MI1_TXCLK (MII)	25 MHz	±150 ppm	60/40	1 ns	5 ns	0.0–VDD_MII
RGM0_REF_CLK_MI0_TXCLK (RGMII)	125 MHz	±150 ppm	45/55	100 ps	2 ns	0.0–VDD_MII

1. Cycle to cycle, peak to peak.
2. Edge rate is 10%–90% (rise) and 90%–10% (fall).

Figure 6-12 External clock to CN6880 requirements

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7. Data Plane Interconnection Subsystem

External I/O traffic through the Front/RTM service ports or the backplane fabric ports of the blade traverses a set of CN6880 network processors either for ingress processing or egress processing. The fabric Ethernet switch sits next to the set of CN6880 processors to interconnect various ports that are available in the blade, including the CN6880 ports, the backplane ports, the Front ports and the RTM ports. The features of the switch and the way the switch interconnects all the ports are therefore, critical for the design to meet the overall requirements. The blade has a 320Gbps capacity switch for these purposes.

7.1. Switch Features: BCM56842

The Trident+ switch family from Broadcom offers three pin-to-pin compatible devices that will include different functional feature sets. Any device can be selected to offer future feature sets by simply replacing a device and software additions. The selected switch, BCM56842, offers 320Gbps of bandwidth.
Some of the features are summarized in Table 7-1, where the details can be found in the expanded list (Table 4: BCM56840 Device Scalability) from the BCM56840_PLUS Advanced Data Sheet.

Table 7-1 Trident+ Switch Fabric Scalability

No	Items	BCM56842	BCM56844
1	Bandwidth	***320Gbps***	***480Gbps***
2	WarpCores	18	18
3	Integrated Packet Buffer Memory	9MB	9MB
4	MAC Entries	128K	128K
5	802.3ad Link Aggregation (LAG)	1024	1024
6	Members per LAG	256	256
7	TRILL Bridges	4K	4K
8	Content Aware Processor Rules		
	*Preclassifier	1K	1K
	*Ingress	2K	2K
	*Egress	1K	1K

7.2. SerDes Interface

The Trident+ switch device has 72 SerDes lanes associated with 18 WarpCores (4 SerDes links per Warp Core) with different types of the data plane speeds including 1G, 10G, and 40G enabled by the WarpCores. Actual SerDes bit rate varies according to data speeds including 1.25Gbps, 3.125Gbps, 6.25Gbps, and 10.3125Gbps per serial link. The SerDes port connections are illustrated in Figure 7-1 and Table 7-2.

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Table 7-2 Switch Port Connections

Block Name	Connected to	Description
XLPORT 0	Front ports (4x10G)	4x SFI
XLPORT 1	Bottom(B) CN6880 QLM0	2x RXAUI
XLPORT 2	Bottom(B) CN6880 QLM2	1x XAUI
XLPORT 3	Bottom(B) CN6880 QLM4	1x XAUI
XLPORT 4	N.C.	Not used
XLPORT 5	N.C.	Not used
XLPORT 6	N.C.	Not used
XLPORT 7	Backplane Fabric B	1x40G Base-KR4
XLPORT 8	Backplane Fabric A	1x40G Base-KR4
XLPORT 9	N.C.	Not used
XLPORT 10	N.C.	Not used
XLPORT 11	N.C.	Not used
XLPORT 12	RTM ports (4x10G, Zone 3)	4x SFI (RTM bottom ports)
XLPORT 13	RTM ports (4x10G, Zone 3)	4x SFI (RTM center ports)
XLPORT 14	RTM ports (4x10G, Zone 3)	4x SFI (RTM top ports)
XLPORT 15	Top (A) CN6880 QLM4	1x XAUI
XLPORT 16	Top (A) CN6880 QLM2	1x XAUI
XLPORT 17	Top (A) CN6880 QLM0	2x RXAUI

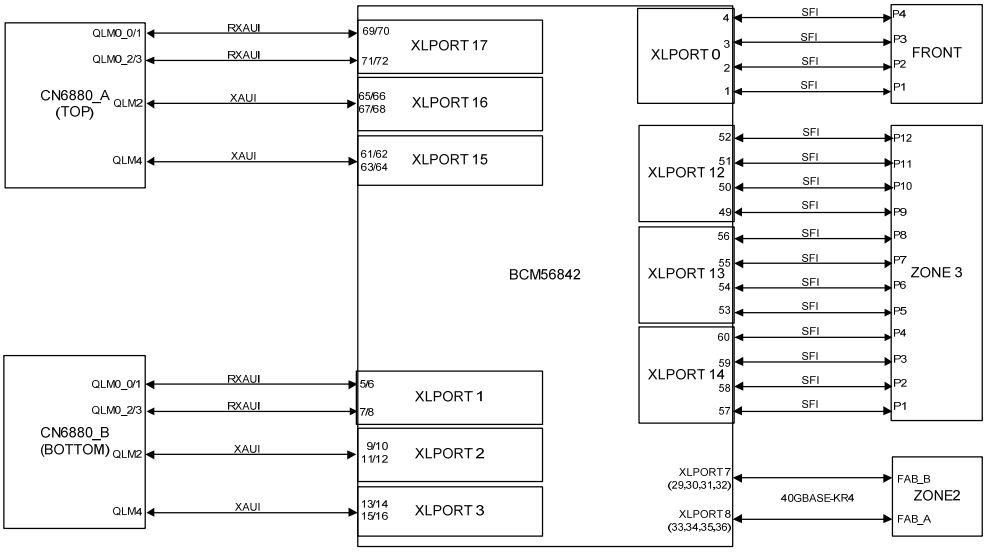


Figure 7-1 Switch Port Connections

The RXAUI interface is for 10Gbps data transfer in 2x lanes with each lane running at 6.25Gbps, thereby reducing the number of SerDes lanes required for XAUI interface. The Trident+ switch device requires four external clock sources for the WarpCores. Each 156.25MHZ reference clock connected to XG_PLL*n*_REF drives a WarpCore group. A Total of four such clocks are routed to the device on the blade to drive four Warp Core groups or 18 WarpCores.

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7.3. PCI-e Interface

Trident supports a 2-lane, PCI-Express (PCIe) Generation 2 interface for CPU configuration and control plane access. A single clock source of 100MHz differential for the PCIe is required and provided on the board to the PCIE_REFCLKp/n pin. The interface supports different types of the DMA operations:

- Scatter-gather DMA for packet transfer to CPU.
- Table DMA: For copying any switch table into system memory
- Statistics DMA: For gathering on-chip statistics counters
- Packet DMA: For transferring packets from/to the CPU

7.4. Reset and Interrupts

Figure 7-2 illustrates the Reset requirements of the switch, which is copied from the datasheet.
On the board, the Reset pin is driven by the CPLD which generates a compliant reset signal for the switch.

Table 13: $\overline{\text{RESET}}$ Timing

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Units*
Power up to $\overline{\text{RESET}}$ deassertion	T_{RESET_PU}	10	–	–	ms
$\overline{\text{RESET}}$ deassertion to normal PHY operation	T_{RESET_WAIT}	20	–	–	µs
$\overline{\text{RESET}}$ pulse length	T_{RESET_LEN}	2	–	–	µs
$\overline{\text{RESET}}$ rise/fall time	–	–	–	25	ns

Note: –
- $\overline{\text{RESET}}$ must be low when power supplies are ramping up.
- When $\overline{\text{RESET}}$ is low, there must be a valid clock signal at all clock inputs. All external power supplies must be stable.
- MII register read/write access and normal PHY operation can start at the end of the RESET_WAIT time.
- A RESET_PU must be performed when the device is first powered up.
- Software reset should not be performed until after RESET_PU and RESET_WAIT have been completed. After issuing a software reset or a RESET_LEN, normal PHY operation can begin after waiting the RESET_WAIT time of 20 µs.

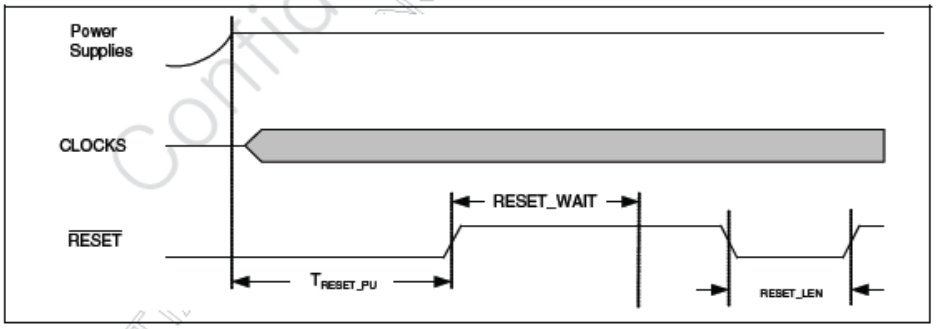


Figure 12: $\overline{\text{RESET}}$ Timing

Figure 7-2 Switch Reset Requirements

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7.5. Clock

There are six Trident input clocks:

- Four SerDes reference clocks: CML clocks at 156.25MHz. One clock per Warp Core group. XG_PLL[3:0].
- PCIe reference clock: 100MHz differential.
- Core clock: 25MHz CML.

The Trident switch runs in a self running mode without backplane sync clocks.
The Trident provides the two reference clocks RECOV_CLK_0/1 recovered from its SerDes ports for any global sync purpose, which is now unused. The board level clock tree is described in Section 11.

7.6. Other Interfaces

7.6.1. MDC/MDIO: MIIM

The Trident contains one CPU Management Interface Controller ((CMIC) supporting IEEE 802.3u standard MII management (MIIM) interface, so called MDC/MDIO interface. The MDIO interface allows the P2041 LMP to access MDIO devices through the switch. Such MDIO devices include the RTM PHY devices. The strapping for the MDIO_22_SEL is set to HIGH (*1: 2.5V or 3.3V*, 0: 1.2V) to set the MDIO signal level.

7.6.2. BSC (I2C) Interface

The Trident switch provides a Broadcom Serial Control (BSC) interface to communicate with other devices in I2C compatible format. The signals for the interface are BSC_SCL, BSC_SDA, BSC_SA0, and BSC_SA1. The operation mode is controlled by BSC_MODE and is set to be **0**. (0: BSC Master, 1: PCI I/F used and BSC Master)
On the blade, however, these signals are not used and left N.C.

7.6.3. LED Control

The LED interface consists of four signals: LED_CLK[1:0], LED_DATA [1:0].
These signals are used to send out the LED control signals based on MAC status data over the time multiplexed data pins. The LED_CLK operates at 5MHz. LED_DATA[0] contains the information for Serdes[36:1] and LED_DATA[1] for Serdes[72:37]. DATA[0] format is in 40bits and DATA[1] is in 80bit as shown in Figure 7-3. On the board, DATA[1] is being used as described in Table 7-3.



Figure 7-3 Switch LED_DATA0 Format

- LED_DATA1 format(80bit)

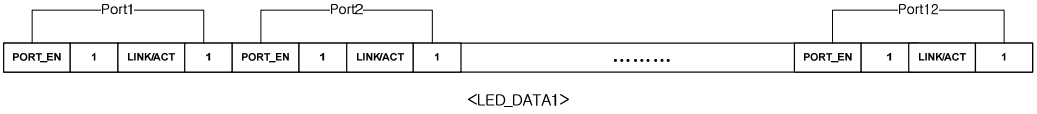


Figure 7-4 Switch LED_DATA1 Format

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Table 7-3 SFPs and LED Data

– LED_DATA0 Port map & Description

SFP Location	Switch SerDes No.	LED Description		
		Bitstream	INDEX	Description
FRONT_SFP1	1	1	PORT EN	0 : EN 1 : DISABLE
		2	1	Don't Care
		3	LINK/ACT	0 : LINK 1 : NO LINK BLINK : ACT
		4	1	Don't Care
FRONT_SFP2	2	5	PORT EN	0 : EN 1 : DISABLE
		6	1	Don't Care
		7	LINK/ACT	0 : LINK 1 : NO LINK BLINK : ACT
		8	1	Don't Care
FRONT_SFP3	3	9	PORT EN	0 : EN 1 : DISABLE
		10	1	Don't Care
		11	LINK/ACT	0 : LINK 1 : NO LINK BLINK : ACT
		12	1	Don't Care
FRONT_SFP4	4	13	PORT EN	0 : EN 1 : DISABLE
		14	1	Don't Care
		15	LINK/ACT	0 : LINK 1 : NO LINK BLINK : ACT
		16	1	Don't Care
FABRIC_B	29,30,31,32	17	PORT EN	0 : EN 1 : DISABLE
		18	1	Don't Care
		19	LINK/ACT	0 : LINK 1 : NO LINK BLINK : ACT
		20	1	Don't Care
FABRIC_A	33,34,35,36	21	PORT EN	0 : EN 1 : DISABLE
		22	1	Don't Care
		23	LINK/ACT	0 : LINK 1 : NO LINK BLINK : ACT
		24	1	Don't Care

– LED_DATA1 Port map & Description

SFP Location	Switch SerDes No.	LED Description		
RTM SFP1	57	1	PORT EN	0 : EN 1 : DISABLE
		2	1	Don't Care
		3	LINK/ACT	0 : LINK 1 : NO LINK BLINK : ACT
		4	1	Don't Care
RTM SFP2	58	5	PORT EN	0 : EN 1 : DISABLE
		6	1	Don't Care
		7	LINK/ACT	0 : LINK 1 : NO LINK BLINK : ACT
		8	1	Don't Care

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RTM SFP3	59	9	PORT EN	0 : EN 1 : DISABLE
		10	1	Don't Care
		11	LINK/ACT	0 : LINK 1 : NO LINK BLINK : ACT
		12	1	Don't Care
RTM SFP4	60	13	PORT EN	0 : EN 1 : DISABLE
		14	1	Don't Care
		15	LINK/ACT	0 : LINK 1 : NO LINK BLINK : ACT
		16	1	Don't Care
RTM SFP5	53	17	PORT EN	0 : EN 1 : DISABLE
		18	1	Don't Care
		19	LINK/ACT	0 : LINK 1 : NO LINK BLINK : ACT
		20	1	Don't Care
RTM SFP6	54	21	PORT EN	0 : EN 1 : DISABLE
		22	1	Don't Care
		23	LINK/ACT	0 : LINK 1 : NO LINK BLINK : ACT
		24	1	Don't Care
RTM SFP7	55	25	PORT EN	0 : EN 1 : DISABLE
		26	1	Don't Care
		27	LINK/ACT	0 : LINK 1 : NO LINK BLINK : ACT
		28	1	Don't Care
RTM SFP8	56	29	PORT EN	0 : EN 1 : DISABLE
		30	1	Don't Care
		31	LINK/ACT	0 : LINK 1 : NO LINK BLINK : ACT
		32	1	Don't Care
RTM SFP9	49	33	PORT EN	0 : EN 1 : DISABLE
		34	1	Don't Care
		35	LINK/ACT	0 : LINK 1 : NO LINK BLINK : ACT
		36	1	Don't Care
RTM SFP10	50	37	PORT EN	0 : EN 1 : DISABLE
		38	1	Don't Care
		39	LINK/ACT	0 : LINK 1 : NO LINK BLINK : ACT
		40	1	Don't Care
RTM SFP11	51	41	PORT EN	0 : EN 1 : DISABLE
		42	1	Don't Care
		43	LINK/ACT	0 : LINK 1 : NO LINK BLINK : ACT
		44	1	Don't Care
RTM SFP12	52	45	PORT EN	0 : EN 1 : DISABLE
		46	1	Don't Care
		47	LINK/ACT	0 : LINK 1 : NO LINK BLINK : ACT
		48	1	Don't Care

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7.6.4. JTAG

The JTAG controller is compliant to the IEEE 1149.6 specification (Also known as AC-JTAG). The maximum frequency of operation is 20MHz. The JTAG provides basic external chip debug features: Access to an identification register, Access to the boundary scan, and Access to the internal scan chains and Ability to Clamp and High-Z all outputs.
For a boundary test purpose, the JTAG pins are accessible with TPs, not as a part of a JTAG chain, but as a standalone device.

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8. Control Plane Subsystem

The Control Plane Subsystem includes all the devices and its interconnection system for the control of the devices on the blade. The main device for the control domain on the blade is the LMP, which communicates with appliance's main control unit sitting in a different slot, outside of the blade, as well as the components on the blade. Shown in Figure 8-1 is the Control Plane Subsystem block diagram, where the P2041 LMP takes a central role. The control plane interface includes all the control related traffic interconnection among the entities on the blade. Depending on the characteristics of the entities, the interface is provided in the form of either Ethernet or PCI express (PCIe) or local bus.

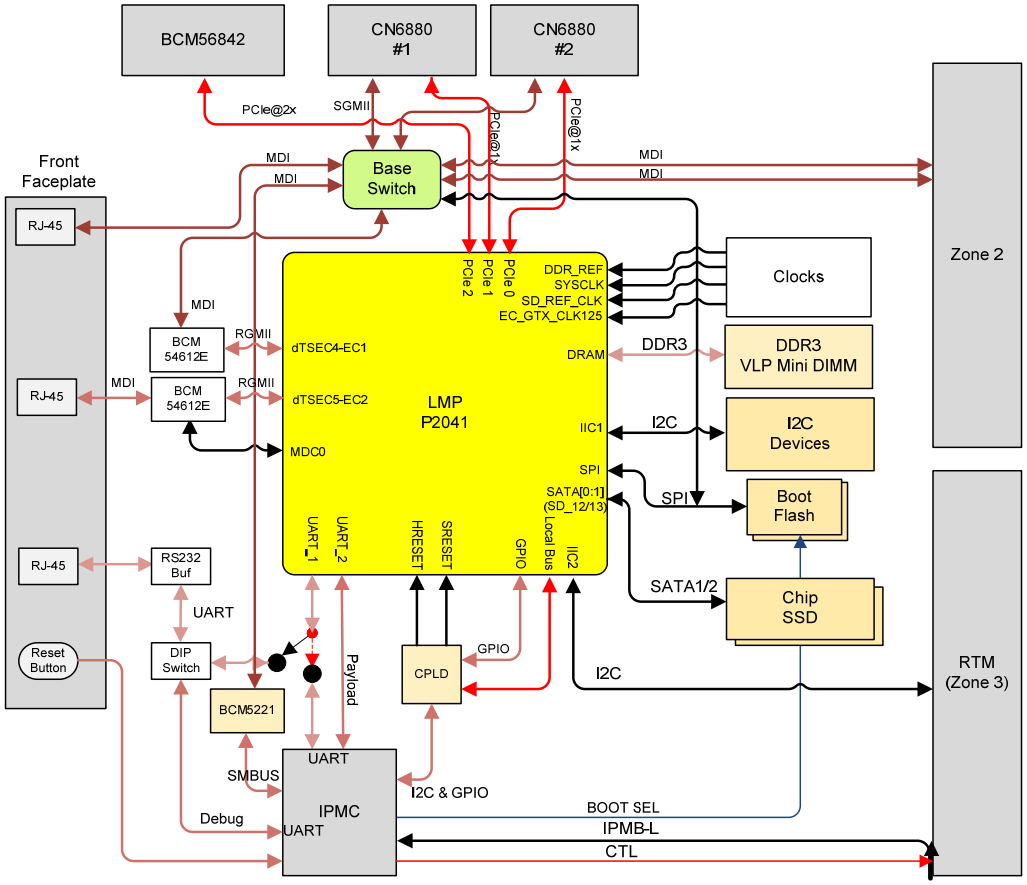


Figure 8-1 Control Plane Subsystem

The Ethernet interface is mainly used for NIC operations among Ethernet capable entities such as the NPUs and the LMP. Single entities can have both interfaces to be used for different purposes.
The entities with Ethernet interconnection include the base switch, the LMP, two CN6880s, the IPMC, two faceplate Ethernet ports and the backplane Base Interface which will connect to the chassis main control hub. Single BCM53115M, a 7 port Ethernet switch, is responsible for control plane Ethernet switching.
10/100/1000BASE-T interface type is supported from the switch.
The entities with PCI express interconnection include the LMP, two CN6880s, and the BCM56842 switch. Since the LMP functions as a master for all the PCIe devices, all the connections from the other PCIe clients go to the LMP.

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8.1. Local Management Processor, P2041

The Local Management Processor or LMP, P2041, is responsible for all the device management including configuration and monitoring with device drivers for the devices to control. The LMP is equipped with major interfaces, PCIe, local bus and Ethernet to achieve these goals. Most of the interactions between the CN6880s and the CPU are executed through the PCIe interface. The status report or other miscellaneous traffic may be exchanged through the Ethernet ports, which is up to a software architecture choice. Another major device to be controlled by the CPU is the switch fabric device. The BCM56842 switch has a PCIe x2 interface.

The LMP has four CPU cores running at up to 1.2GHz with 64-bit DDR2/3 support. For SerDes interfaces on the board, it provides three PCIe interfaces and two SATA interfaces. Shown in Figure 8-2 is the internal architecture of P2041.

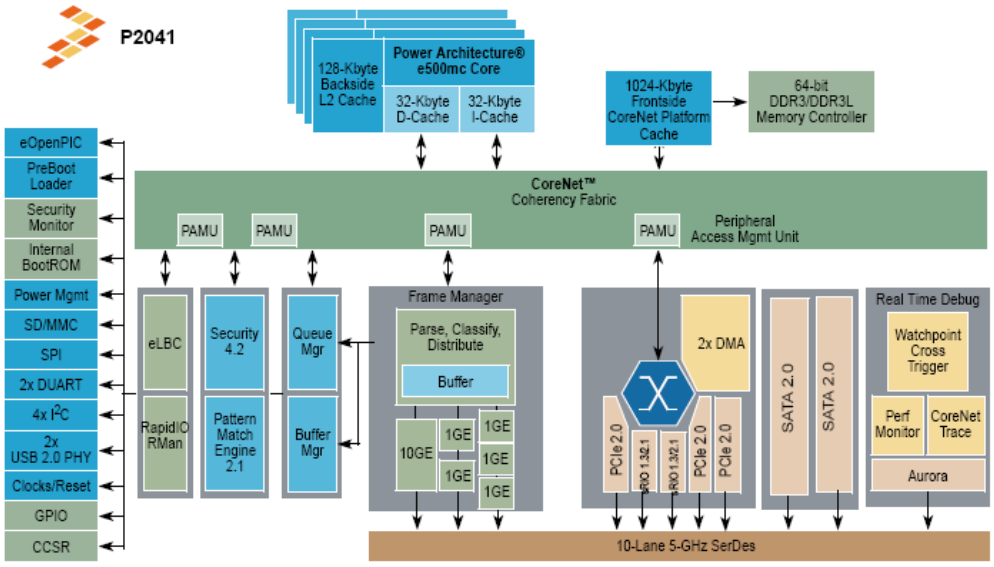


Figure 1. P2041 Preliminary Block Diagram

Figure 8-2 P2041 Internal Blocks (from datasheet)

8.1.1. Features

Key features of the P2041 include:

- e500v2 Core Processor@1.2GHz – Dual Cores
  - 36-bit physical addressing
  - Double-precision floating-point support
  - L1 instruction-cache of 32KB and L1 data cache of 32KB per Core
- L2 Cache of 512Kbyte with ECC
- Three 10/100/1000 Mbps enhanced three-speed Ethernet controllers (eTSECs): EC1, EC2 are used on the board.
- High-speed interfaces:
  - Three PCI Express interfaces with Two x1 and one x2
  - Two SATA interfaces each with x1
- Serial peripheral interface
- Integrated Security Engine
  - XOR Acceleration
  - Protocol support includes SNOW, ARC4, 3DES, AES, RSA/ECC, RNG, single-pass SSL/TLS, Kasumi

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- DDR2/3 SDRAM memory controller with ECC support
- Two four-channel DMA controllers
- Two I2C Controllers, DUART, Timers
- Enhanced local bus controller
- 16 GPIO signals

8.1.2. DDR3 SDRAM Interface

The P2041 supports DDR2 and DDR3 SDRAM and a single VLP mini DIMM DDR3 module is installed on the blade. The features of this interface include:

- Up to 4GByte DDR 400MHz on the blade
- 64 bit data + 8 bit ECC(optional)
- DDR3 Support: Unbuffered and registered DIMMs
- x8/x16/x32 data width support
- 64-/72-bit SDRAM data bus, 32-/40-bit SDRAM
- Four physical bank support (four chip selects)
- Up to eight post refreshes
- Very Low Profile (VLP) mini DIMM form factor
  - 244 pin in 82.1mm x 18mm x 3.8mm (**L** x **H** x **W)**

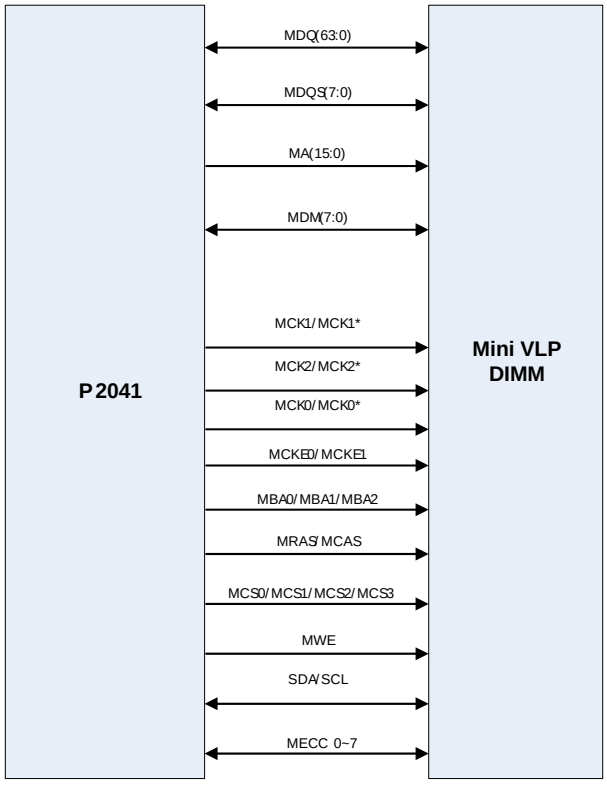


Figure 8-3 P2041 DDR3 Interface

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8.1.3. PCI Express Interface

The PCIe interface is compatible with the *PCI Express Base Specification, Revision 1.0a.* The features of the interface are:

- 4 Lanes supporting x4, x2, x1 link configurations at 2.5Gbps serial lane speed
- Three PCIe interfaces with 2x 1 Lane and 1x 2 Lane on the board
- Root complex(RC) and endpoint(EP) configurations
- 32bit and 64bit address support
- DMA
- One Virtual channel (VC0)
- Max Payload size at 256bytes
- Host/Agent Mode Configuration(Default)

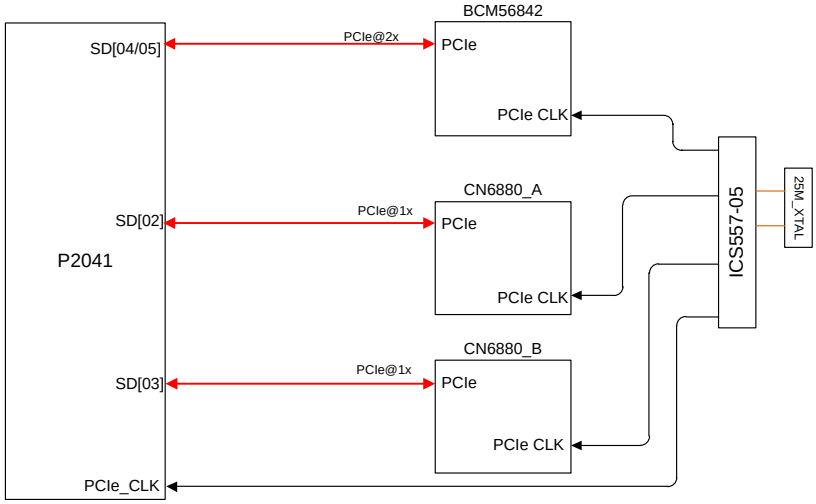


Figure 8-4 Host Interface – PCI-e
PCI-e configuration for both the NPUs and the switch fabric.

8.1.4. I2C (TWSI) Interface

The P2041 provides I2C interfaces with following features:

- 4x I2C interface support
- Multiple master operation
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- START and STOP signal generation/detection
- Acknowledge bit generation/detection
- Bus busy detection
- Software programmable clock frequency
- Software selectable acknowledge bit
- On-chip filtering for spikes on the bus

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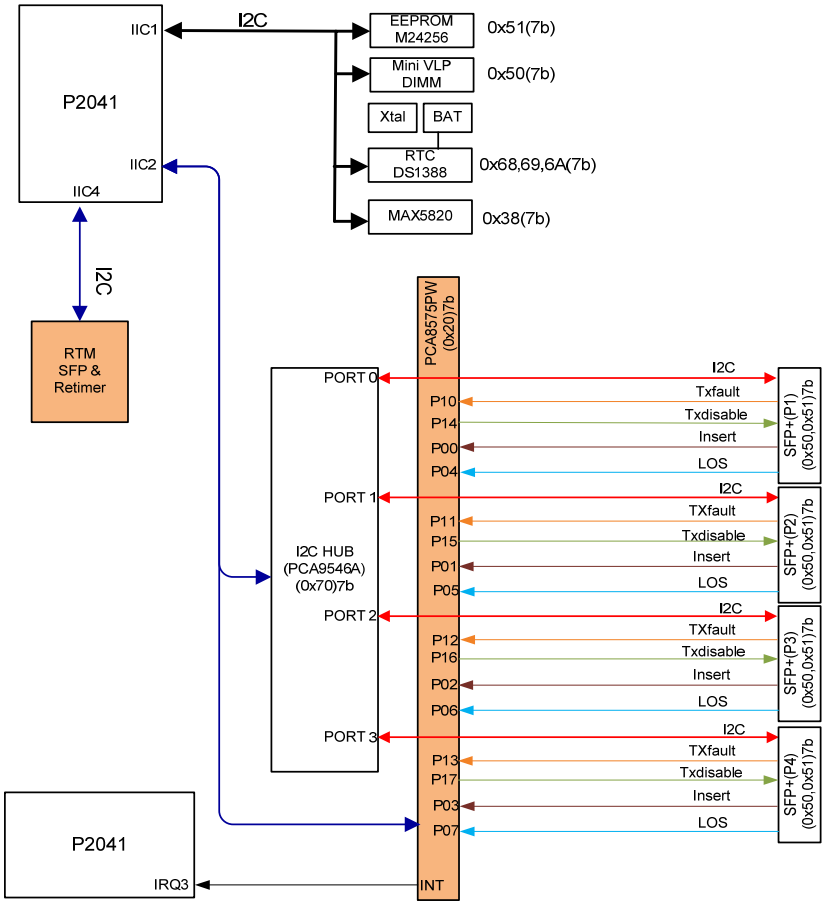


Figure 8-5 P2041 I2C Interface

Illustrated in Figure 8-5 are the I2C interface block details around P2041, which contain miscellaneous devices including the EEPROM, the VLP Mini DIMM, the RTC, and the MAX5820. Table 8-1 shows the I2C bus address of the target devices.

Table 8-1 I2C Bus Address

Bus Name	Target Device	Address
IIC_1	VLP Mini DIMM	0x50(1010000x)
	Serial EEPROM(M24256-BWDW6TP)	0X51(1010001x)
	RTC(DS1388)	0x68(1101000x) 0x69(1101001x) 0x6A(1101010x)
	AVS DAC(MAX5820L)	0x38(0111000x)
IIC_2	I2C HUB(PCA9546A)	0x70(1110000x)
	I2C IO Expender(PCA8575PW)	0x20(0100000x)
IIC_3	N.C.	
IIC_4	RTM	Subject to RTM Hardware Specification.

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I2C HUB(PCA9546A)		SFP+	
I2C Address	Port No.	I2C Address	Port No.
0x70(1110000x)	P0	0x50(1010000x) 0x51(1010001x)	SFP+1
	P1	0x50(1010000x) 0x51(1010001x)	SFP+2
	P2	0x50(1010000x) 0x51(1010001x)	SFP+3
	P3	0x50(1010000x) 0x51(1010001x)	SFP+4

I2C IO Expander(PCA8575PW)			SFP+	
I2C Address	Port No.	I/O	Signal Name	Port No.
0x20(0100000x)	P00	I	INSERT 0 : Module Present 1 : No Present	SFP+1
	P01	I	INSERT	SFP+2
	P02	I	INSERT	SFP+3
	P03	I	INSERT	SFP+4
	P04	I	RX_LOS 0 : Signal Detect 1 : Loss of Signal	SFP+1
	P05	I	RX_LOS	SFP+2
	P06	I	RX_LOS	SFP+3
	P07	I	RX_LOS	SFP+4
	P10	I	TX_FAULT 0 : Normal 1 : TX_FAULT	SFP+1
	P11	I	TX_FAULT	SFP+2
	P12	I	TX_FAULT	SFP+3
	P13	I	TX_FAULT	SFP+4
	P14	O	TX_DISABLE 0 : TX Enable 1 : TX Disable	SFP+1
	P15	O	TX_DISABLE	SFP+2
	P16	O	TX_DISABLE	SFP+3
	P17	O	TX_DISABLE	SFP+4

8.1.5. UART Interface

Shown in Figure 8-6 is the interconnections for the dual UART ports of the P2041. UART#1 is used either for the front panel console port or Serial over LAN port via the IPMC. UART #2 is used for payload transmission from P2041 to the IPMC.

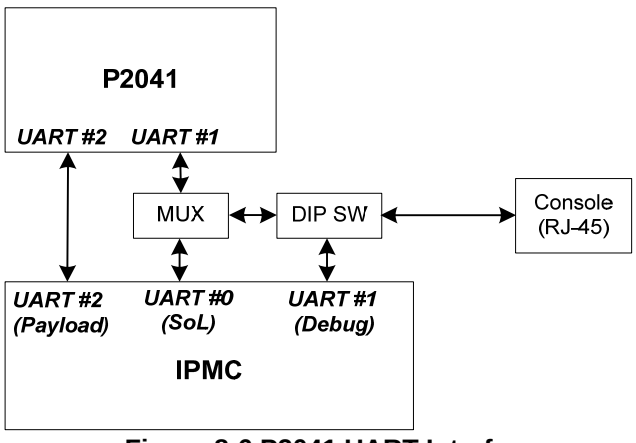


Figure 8-6 P2041 UART Interface

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The MUX selection enables to select one of the two destinations of the UART #1 port and controlled by the P2041. Some selected UART features include:

- Full-duplex operation.
- Programming model compatible with original PCI16450 UART and PC16550D (Improved version of PC16450 that also operates in FIFO mode).
- FIFO mode for both transmitter and receiver, providing 16-byte FIFOs.
- Line-break detection and generation.
- Internal diagnostic support, local loopback, and break functions.

The UART_1 pin out of the serial interface RJ-45 connector is compliant to Cisco pin out as can be seen in Table 3-1 and Table 3-2.

8.1.6. Interrupts

The P2041 has an internal Programmable Interrupt Controller (PIC) which handles various external and internal interrupts connected to the pins. All the interrupt sources and their handlings are found in the P2041 datasheet and some are summarized as:

- IRQ[0:11] Signal support
- Interrupts generated from within the PIC itself, which are as follows:
  - Global timers A and B internal to the PIC
  - Inter-Processor Interrupts(IPI)
  - Message registers
  - Shared message signaled registers
- Three types of programmable interrupt outputs:
  - External Interrupt : int0, int1
  - Critical Interrupt : cint0, cint1
  - IRQ_OUT#
- Programming model compliant with the OpenPIC architecture
- Support for two processors
- Processor core initialization control
- Programmable resetting of the PIC through the global configuration register
- Pass-through mode(PIC disable) in which the PIC directs interrupts off-chip for external servicing

The external interrupt signals are routed as the following table.

Table 8-2 P2041 Interrupt Signal Connections

Pin Name	Connection	I/O	Description
IRQ0	Connected to CPLD	-	Reserved
IRQ1	BCM53115M Interrupt pin	I	
IRQ2	SYS CPLD Interrupt pin	I	
IRQ3/GPIO[21]	CPLD Interrupt for SFP information	I	
IRQ4/GPIO[22]	Connected to CPLD	I	
IRQ5/GPIO[23]	RTM Interrupt pin	I	
IRQ6/GPIO[24]	Connected to CPLD	-	Reserved
IRQ7/GPIO[25]	Connected to CPLD	-	Reserved
IRQ8/GPIO[26]	USB1_DRVVBUS	O	USB Power Enable
IRQ9/GPIO[27]	USB1_PWRFAULT	I	USB Power fault alarm
IRQ10/GPIO[28]	RTM RESET	O	RTM RESET 0 : RESET 1 : Normal
IRQ11/GPIO[29]	BOOT FLASH Selection of IPMC	I	BOOT Flash select 0 : Master flash 1 : Slave flash
IRQ_OUT#	Interrupt output	O	

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8.1.7. SPI Interface

The SPI interface provides SPI_MOSI, SPI_MISO, SPI_CLK and four chip select signals. Only two CSs are used on the board.
The SPI interface handles two serial flashes and the base switch, which is illustrated as in Figure 8-7.

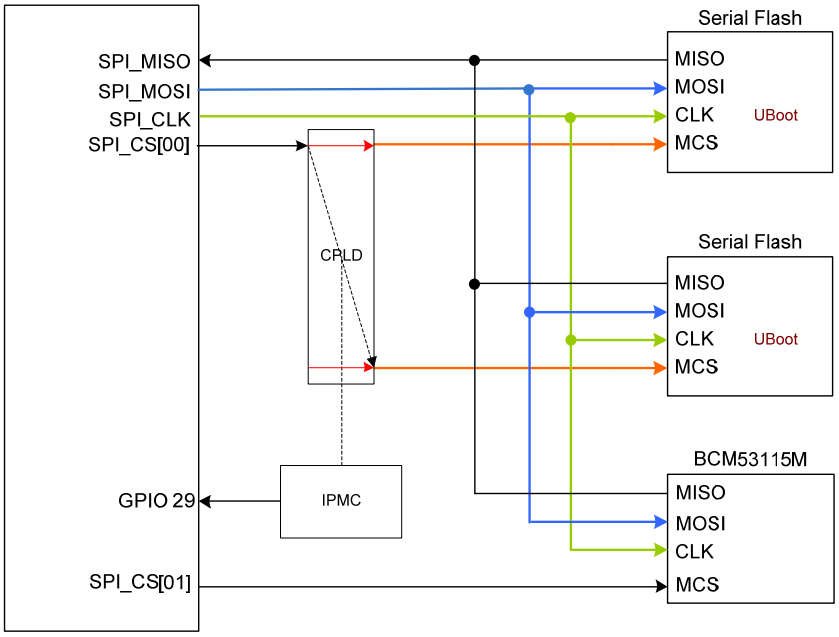


Figure 8-7 P2041 SPI Interface

The serial flashes contain the boot images and they are selected by the IPMC and IPMC forwards the selection information to *P2041 GPIO_3*.
Summarized below are selected features of the SPI interface:

- Supports eSPI master.
- Supports RapidS full clock cycle operations
- Full-duplex or half-duplex master operation
- Supports Winbond dual output read
- Command in transaction level – easier for accessing eSPI devices
- Works with a range from 4-bit to 16-bit data characters
- Supports back-to-back character transmission and reception
- Supports single-master environment
- Maximum clock rate possible is (platform clock rate / 2)
- Independent programmable baud rate generator
- Programmable clock phase and polarity
- Support 4 different configurations per chip select
- Local loopback capability for testing
- Support booting from eSPI Interface.

8.1.8. SATA Interface for Chip SSD

The P2041 provides SATA1 and SATA2 interfaces through one of the external configurable SerDes interfaces (Bank2 C and D). The SerDes interfaces *SD_12 and SD13* are connected to the two Chip SSD devices respectively to provide redundancy. To enable this configuration, the Reset Code Word, RCW[***SRDS_PRTCL]*** should be set to ***0x16*** allowing three PCIe, two SGMIIs, and two SATAs for the external SerDes interface mapping.
The Chip SSD used is *GLS85LS1008P Industrial Grade SATA NANDrive* are from Greenliant. The features of the device are summarized as the following.

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- SATA 1.5Gbps/3.0Gbps
- Sustained sequential data read – up to 70MByte/sec at 128KB block size
- Sustained sequential data write – up to 60MByte/sec at 128KB block size
- 3.3V and 1.2V power supply
- 580mW typical
- Integrated Voltage Detector to generate reset to prevent inadvertent writes
- Robust built-in ECC
- FBGA packet: 14.0 mm x 24.0 mm x 1.95 mm, 145-ball.

The GLS85LS1008P is a high performance, fully integrated solid state drive. It combines an integrated SATA NAND flash memory controller and 8 GB of single-level cell (SLC) NAND flash in a multi-chip package. Two of these are populated on the board for redundancy purpose and used for OS and application image storage.

8.1.9. Local Bus Interface (EBI)

Illustrated in Figure 8-8 is the Local Bus Interface (EBI) block and its external connections. The chip selects available for the local bus is LCS[3:0], but only LCS[3] is used and connected to the system CPLD to access the CPLD registers.

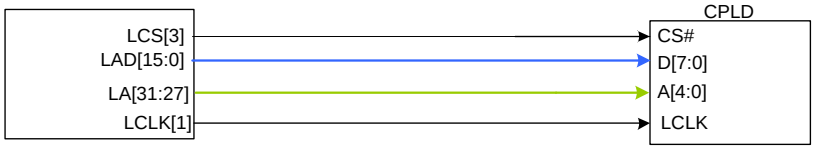


Figure 8-8 P2041 Local Bus (EBI) Interface

Summarized below are selected features of the EBI interface:

- Support memory controller with eight memory banks
  - Variable memory block sizes(32Kbytes to 4Gbytes)
  - Selection of control signal generation on a per-bank basis
  - Data buffer controls activated on a per-bank basis
- General-purpose chip-select machine(GPCM)
  - Compatible with SRAM,EPROM,NOR Flash, EEPROM and peripherals
  - Global chip-select available at system reset.
  - Boot chip-select support for 8- and 16-bit devices.
  - Minimum three-clock access to external devices.
- NAND Flash control machine(FCM)
  - Compatible with small(512+16byte) and large(2048+64bytes) page parallel NAND Flash EEPROM
  - Global chip-select available at system reset, with 4-Kbyte boot block buffer for execute-in-place boot loading.
  - ECC checking enable/disable feature supported during boot.
  - Boot chip-select support for 8-bit devices.
  - Dual 2Kbyte/eight 512byte buffers allow simultaneous data transfer during flash reads and programming.
- Three user-programmable machines(UPMs)
  - Support for 8- and 16-bit devices
  - Page mode support for successive transfers within a burst
  - Internal address multiplexing supporting 64-,128-,256- and 512Kbyte and 1-,2-,4-,8-,16-,32-,64-,128- and 256Mbyte page banks
  - 16-bit interface to peripherals

8.1.10. USB Interface

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P2041 supports 2x USB compliant to USB specification Rev 2.0. On the board, USB2 is routed to the faceplate USB connector. USB1 is not used.

8.1.11. MDC/MDIO Interface

The MDC/MDIO interface is used for the Ethernet PHY BCM54612E and the base switch BCM54115M management.
The MDC frequency is set by the following relation:

MDC Frequency = core frequency/(MDC_CLK0/1[PHASE] x 2)

8.1.12. GPIO Interface

Table 8-3 shows the connections on the 16 bit GPIO pins.

Table 8-3 GPIO connections

Pin Name	Connection	I/O	Description
GPIO[0:3]	SPI_CS[0:3]	O	SPI Chip select
GPIO[8]	UART1_SOUT	O	UART1_SOUT
GPIO[9]	UART2_SOUT	O	UART2_SOUT
GPIO[10]	UART1_SIN	I	UART1_SIN
GPIO[11]	UART2_SIN	I	UART2_SIN
GPIO[12]	DIAG_EN	O	DIAG_EN
GPIO[13]	Connected to CPLD	I	Reserved
GPIO[14]	Connected to CPLD	I	Reserved
GPIO[15]	SPI Write Protect	O	SPI Write Protect 0 : Write Protect 1 : Normal
GPIO[16]	Connected to CPLD	I/O	Reserved
GPIO[17]	Connected to CPLD	I/O	Reserved
GPIO[18]	IIC_4 SCL for RTM	I/O	RTM I2C
GPIO[19]	IIC_4 SDA for	I/O	RTM I2C

8.2. Ethernet Controller Interface

The interconnections between Ethernet capable devices (Tri-speed) are routed by the 7-port base Ethernet switch, BCM53115M. To support different types of the physical layer interfaces, some connections require PHY devices as can be seen in Figure 8-9. Two different types of Ethernet PHY devices are used: two BCM54612Es and one BCM5221. The BCM54612E connecting to the RJ-45 enables *Energy Efficient Ethernet (EEE) IEEE P802.3az draft standard* compliant operation on the port which saves power during idle period. The two backplane Base Interface ports are directly support from the switch in TDI types. One port from BCM5221 is for Serial-over-LAN (SOL) interface for IPMC. The switch configuration from the LMP is done through the SPI interface. Note that the two NIC interfaces from the LMP are EC_1 for a base switch connection and EC_2 for the faceplate RJ-45 connection.

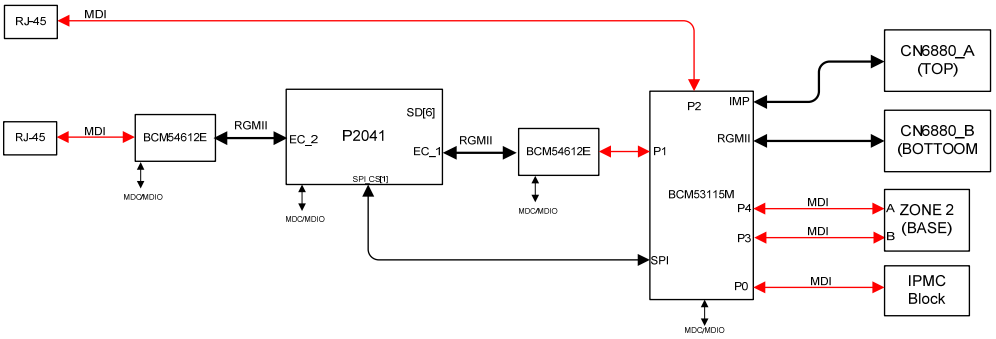


Figure 8-9 Ethernet Control Plane Interconnections

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8.2.1. 7-port Ethernet Switch BCM53115M

The BCM53115 is a 7-port Ethernet switch with five tri-speed MACs and two GMACs respectively. On the board, five tri-speed MAC ports (P0 ~ P4) and one GMAC port are used. Figure 8-9 shows such connections and the port mapping can be found in Table 8-4. The features of the switch are summarized in the following:

- One GMII/RGMII/MII/RvMII/TMII/RvTMII Interface for an inband management port (IMP) for connection to a CPU/management entity without PHY.
- One GMII/RGMII/MII/RvMII or SGMII/SerDes Interface for WAN management port
- Five-port 10/100/1000 transceiver for TX
- Dual IPM port support, WAN Interface(Port5) to be management port-capable
- IEEE802.1p
- Port-based VLAN
- IEEE802.1Q-based VLAN with 4K entries
- MAC-based trunking with automatic link failover
- Port-based rate control
- Port mirroring
- BroadSync HD for IEEE802.1AS support
- DoS stack prevention
- IGMP snooping, MLD snooping support
- Spanning tree support(multiple spanning trees, up to eight)
- CableChecker with unmanaged mode support
- Double tagging/QinQ
- Egress VID remarking
- IEEE802,3az EEE(Energy Efficient Ethernet)
- IEEE802.1AS support
- 4K entry MAC address table with automatic learning and aging.
- 128KB packet buffer(1KB = 1024bytes)
- 128 multicast group support
- Jumbo frame support up to 9720 byte

The port LED configurations are:

- Port0 : LED[15]: SPEED 1G, LED[18]: LINK/ACT
- Port1 : LED[14]: LINK/ACT
- Port2 : LED[10]: LINK/ACT
- Port3 : LED[6]: LINK/ACT
- PHY Register setting for the LED control stays with a default value.

The base switch requires three power rails of 3.3V, 2.5V and 1.2V, which requires power sequencing in the following order: 3.3V->2.5V->1.2V.
.

Table 8-4 Base Switch Port Mapping

Switch Port	Interface	PHY Address	Connected to
P0	MDI	00000b	SOL, BCM5221 to IPMC
P1	MDI	00001b	BCM54612E, to P2041
P2	MDI	00010b	Faceplate RJ-45
P3	MDI	00011b	Base Interface B
P4	MDI	00100b	Base Interface A
RGMII	RGMII	-	Bottom CN6880
IMP(P6)	RGMIII	-	Top CN6880

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8.2.2. Ethernet Transceiver BCM54612E

The BCM54612E is a triple-speed 10/100/1000BASE-T Ethernet transceiver that supports RGMII interface on the system (MAC) side and unshielded twisted-pair (UTP) cabling and performs all of the physical layer functions of tri-speed Ethernet. The transceiver supports Green Ethernet technology, so called Energy Efficient Ethernet (EEE), IEEE 802.3az, and an extension of the IEEE 802.3 standard. Two BCM54612E are installed on the board as shown in Figure 8-9.
For the device installed on P2041 EC2 interface, the MAC side interface is connected to the P2041 LMP and the other side is connected to the faceplate RJ-45 connector. The port operates as a blade LMP management port. The status and control registers of the device are accessible through the MDIO and MDC serial interface that are also connected to the P2041 MDC and MDIO interface. Another device is installed on P2041 EC1 interface at the MAC side, and the other side is connected to the base switch. Following are board settings.

- PHY address: 11000b and 11001b
  PHYA[0] = pulled down.
- Test Mode TEST[3:2] = 01 : JTAG Test
  LED[1]: TMS
  LED[2]: TDI
  LED[3]: TDO
  PHY[0]: TCK

- Test Mode TEST[3:2] = 11 : Normal Mode
- Power rails: OVDD = 2.5V, AVDD = 3.3V, AVDDL = 1.2V.

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9. Blade Management Subsystem

The Intelligent Management Controller (IPMC) sits at the center of the blade management architecture. The IPMC enables hot-swap, E-keying, power management, environment/device monitoring and management with or without the ATCA Shelf Manager. The IPMC is initialized as soon as the dedicated power is supplied, and works completely independent of the LMP. Since the dedicated power is separate from the main power for other devices, the IPMC can work when the power to the other devices are not supplied.

The IPMC has embedded flash memory, RAM, and System Event Log memory and multiple I2C bus interfaces for interconnection to other devices. The firmware for the IPMC is saved into the flash. The serial port connected to the IPMC enables access to all management information and commands.

The Field Replacement Unit (FRU) information is saved into the EEPROM, which is connected to the IPMC through an I2C interface. Two I2C buses are provided as a redundant connection for the IPMB bus to the backplane to communicate with the Shelf Manager. One I2C bus is reserved for the RTM MMC connection. The remaining I2C bus is used to monitor the sensors, the power modules, and to read from or write to the EEPROM in master-only mode. During monitoring, when one of the monitored values goes over the threshold, the IPMC reports to the Shelf Manager for the event.

When a fault is detected on one of the redundant IPMB buses, the IPMC isolates the troublesome bus and re-establishes the communication path again on the new IPMB bus.

Shown in Figure 9-1 is the structure of the IPMC block. The IPMC on the board is Smart Fusion A2F500, a SmartFusion Customizable System-on-Chip (cSOC) from Microsemi (formerly Actel). The IPMC and the CPLD form a key functional block for the ATCA blade management tasks.

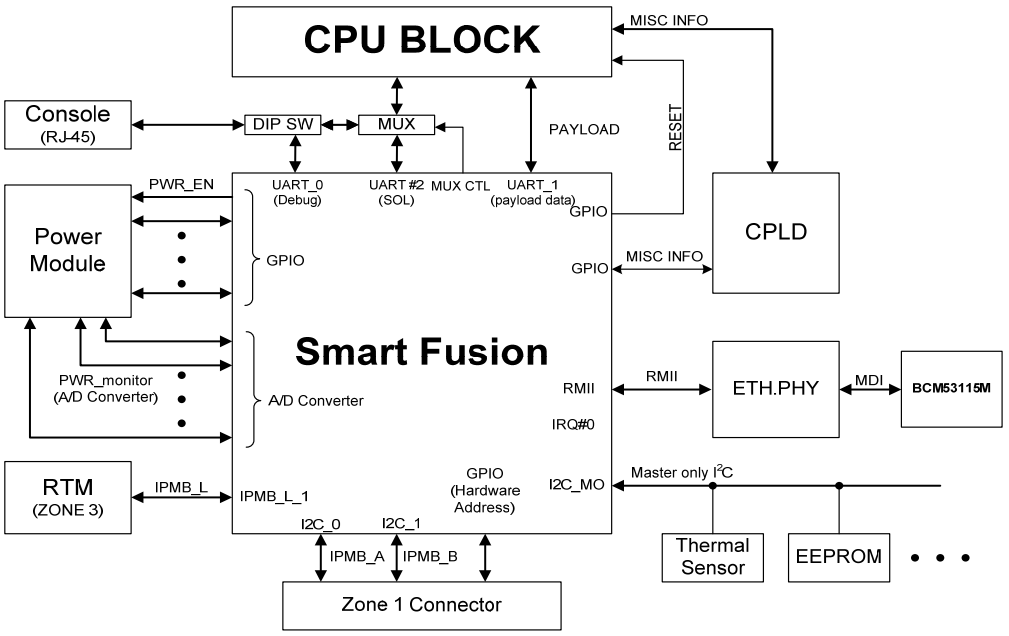


Figure 9-1 IPMC Block

The IPMC block interconnections are summarized as:

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- Serial Over LAN (SOL): The A2F500 connects to the BCM5221, which is connected to the base switch. The LMP serial console connects to either the front panel RJ-45 console port or to the SOL port (UART #0), but not at the same time.
- Payload Interface: By UART #1 port, the IPMC communicates with the LMP.
- RTM Management: The IPMC communicates with the RTM MMC through the hot-swap buffer and IPMB-L for FRU information and Command exchange.
- IPMB-A/B Interface: The IPMC communicates with the Shelf Manager via the redundant IPMB-A and IPMB-B interfaces on ZONE 1 connector through the hot-swap buffer.
- Blade Power Sequence: All the power rail enable/disables are controlled by the IPMC GPIO.
- Power Monitoring: All the power rails are monitored by the IPMC and any violation on the level is reported to the Shelf Manager. When a violation is observed, the IPMC shutdowns the FRU.
- FRU Information: The EEPROM that contains the FRU information, Log, alarm information, etc is connected to the IPMC via the master only I2C.
- Sensor: Various sensors including thermal and power are connected to the IPMC via the master only I2C. The IPMC monitors sensor information.

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9.1. IPMC

The SmartFusion cSOC A2F500 is made by integrating FPGA technology with programmable high performance analog and hardened ARM Cortex-M3 microcontroller blocks on a flash semiconductor process. The three key building blocks include: Microcontroller Subsystem (MSS), Programmable Analog, and ProASIC3 FPGA Fabric. The MSS is composed of a 100 MHz Cortex-M3 processor and integrated peripherals, which are SPI, I2C, and UART serial ports, embedded FlashROM (EFROM), 10/100 Ethernet MAC, timers, PLLs, oscillators, RTC, and peripheral DMA controller. The Programmable Analog Subsystem has Analog Front-End (AFE) and Analog Compute Engine (ACE). The ProASIC3 FPGA Fabric gives benefits from the advantages only flash-based devices offer such as reduced cost of ownership, low power and security. The features of the IPMC A2F500 are summarized in Table 9-1.

Table 9-1 A2F500 Features

SmartFusion Device Feature		**A2F500**
FPGA Fabric	System Gates	**500,000**
	Tiles (D-flip-flops)	**11,520**
	RAM Blocks (4,608 bits)	**24**
Microcontroller Subsystem (MSS)	Flash (Kbytes)	**512**
	SRAM (Kbytes)	**64**
	Cortex-M3 with memory protection unit (MPU)	**Yes**
	10/100 Ethernet MAC	**Yes**
	External Memory Controller (EMC)	**24-bit address,16-bit data**
	DMA	**8 Ch**
	I2C	**2**
	SPI	**2**
	16550 UART	**2**
	32-Bit Timer	**2**
	PLL	**2**
	32 KHz Low Power Oscillator	**1**
	100 MHz On-Chip RC Oscillator	**1**
	Main Oscillator (32 KHz to 20 MHz)	**1**
Programmable Analog	ADCs (8-/10-/12-bit SAR)	**3**
	DACs (12-bit sigma-delta)	**3**
	Signal Conditioning Blocks (SCBs)	**5**
	Comparators2	**10**
	Current Monitors2	**5**
	Temperature Monitors2	**5**
	Bipolar High Voltage Monitors2	**10**

The operating system on embedded ARM processor is FreeRTOS, which is a portable, open source, royalty free, mini real-time kernel (www.freertos.org). Most essential driver packages are available from the SmartFusion SDK.

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9.2. I/O Ports

Due to the nature of the blade management, the IPMC is equipped with the many I/O ports that are configurable. Table 9-2 illustrates most of the I/O ports and connections on the blade.

Table 9-2 IPMC Pin map and on-board arrangement

Pin Name	Pin No.	Connection	I/O	Description
MSS I/O				
MSS_RESET_N	R1	IPMC_MSS_RESET_L	I	Core Reset 0 : Reset 1 : Normal operating
I2C Interface				
I2C_0_SDA_GPIO_22	V21	IPMC_IPMBA_SDA - Connected to Zone 1 Connector via I2C Buffer	I/O	IPMB_A I2C Address/data signal
I2C_0_SCL_GPIO_23	U21	IPMC_IPMBA_SCL - Connected to Zone 1 Connector via I2C Buffer	I	IPMB_A I2C Clock signal
I2C_1_SDA_GPIO_30	U20	IPMC_IPMBB_SDA - Connected to Zone 1 Connector via I2C Buffer	I/O	IPMB_B I2C address/data signal
I2C_1_SCL_GPIO_31	V22	IPMBC_IPMBB_SCL - Connected to Zone 1 Connector via I2C Buffer	I	IPMB_B I2C Clock signal
GPIO_0_IO47RSB4V0	V1	IPMC_MO_SCL	O	IPMI I2C Clock signal for I2C Devices I2C Address(Base) - M24256 : 0x1010010X(SDR/SEL) - M24256 : 0x1010001X(COLD/NV Data) - DS75 : 0x1001000X - PIM400 : 0x0101000x - MAX11605 : 0x1100101X (0 : MSW_1V0, 1 : MSW_AVS, 2 : SW_1V2, 3 : 1V5, 4 : LMP_1V0, 5 : LMP_VTT, 6 : RTC_VAT, 7 : IPMC_1V5)
GPIO_1_IO46_RSB4V0	R3	IPMC_MO_SDA	I/O	IPMI I2C Address/data signal I2C Address for I2C Devices
GPIO_2_IO45RSB4V0	W1	NC	O	Not used
GPIO_3_IO44RSB4V0	Y1	NC	O	Not used
GPIO_4_IO43RSB4V0	AA1	IPMB_L_SCL1	O	IPMB-L I2C Clock signal for RTM
GPIO_7_IO40RSB4V0	W2	IPMB_L_SDA1	I/O	IPMB-L I2C Address/Data signal for RTM
GPIO_5_IO42RSB4V0	U2	NC	O	Not used
GPIO_6_IO41RSB4V0	V2	NC	O	Not used
SPI Interface				
SPI_0_DO_GPIO_16	U17	IPMC_SPI0_DO	O	SPI Data Output
SPI_0_DI_GPIO_17	V18	IPMC_SPI0_DI	I	SPI Data Input
SPI_0_CLK_GPIO_18	W19	IPMC_SPI0_CLK	O	SPI Clock output
SPI_0_SS_GPIO_19	Y20	IPMC_SPI0_nSS	O	SPI Chip select
SPI_1_DO_GPIO_24	T17	NC	O	Not used
SPI_1_DI_GPIO_25	V19	NC	O	Not used
SPI_1_CLK_GPIO_26	AA22	NC	O	Not used
SPI_1_SS_GPIO_27	W21	NC	O	Not used
JTAG Interface				
TMS	P20	IPMC_JTAG_TMS	I	JTAG Test mode select
TCK	P18	IPMC_JTAG_TCK	I	JTAG Test clock
TDI	P17	IPMC_JTAG_TDI	I	JTAG Test Data Input
TRSTB	P22	IPMC_JTAG_nTRST	I	JTAG Test Reset
TDO	P21	IPMC_JTAG_TDO	O	JTAG Test Data Output
JTAGSEL	R16	J8 2 PIN Jumper conn	I	JTAG Enable Select 0 : JTAG Mode 1 : Normal Mode

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VJTAG	M19	VJTAG	I	JTAG Power
VPP	M21	VPUMP	I	
Ethernet Interface				
MAC_MDC_IO48RSB4V0	AA3	RMII_MDC	O	PHY Management Clock
MAC_MDIO_IO49RSB4V0	V4	RMII_MDIO	I/O	PHY Management Data
MAC_CRSDV_IO51RSB4V0	W4	RMII_CRS_DV	I	RMII Data Valid
MAC_RXER_IO50RSB4V0	AA4	RMII_RX_ER	I	RMII Rx Error
MAC_TXEN_IO52RSB4V0	Y4	RMII_TX_EN0	O	RMII TX Enable
MAC_TXD_0_IO56RSB4V0	AA5	RMII_TXD0	O	RMII TX DATA0
MAC_TXD_1_IO55RSB4V0	W5	RMII_TXD1	O	RMII TX DATA1
MAC_RXD_0_IO54RSB4V0	V5	RMII_RXD0	I	RMII RX DATA0
MAC_RXD_1_IO53RSB4V0	U5	RMII_RXD1	I	RMII RX DATA1
MAC_CLK	T6	RMII_REF_CLK	I	RMII Reference Clock
UART Interface				
UART_0_TXD_GPIO_20	Y22	DBG_TXD	O	IPMC Console for Debug
UART_0_RXD_GPIO_29	U18	DBG_RXD	I	
UART_1_TXD_GPIO_28	V20	PAYLD_TXD	O	CPU & IPMC Communication for payload data
UART_1_RXD_GPIO_29	W22	PAYLD_RXD	I	
Reserved GPIOs				
GPIO_11_IO57RSB4V0	T4	Connected to CPLD	I/O	IPMC_GPIO11
GPIO_12_IO37RSB4V0	AA2	Connected to CPLD	I/O	IPMC_GPIO12
GPIO_13_IO36RSB4V0	AB2	Connected to CPLD	I/O	IPMC_GPIO13
GPIO_14_IO35RSB4V0	AB3	Connected to CPLD	I/O	IPMC_GPIO14
GPIO_15_IO34RSB4V0	Y3	Connected to CPLD	I/O	IPMC_GPIO15
FPGA GPIOs				
GFA2_IO68PDB5V0	E3	IPMC_CLK1	I	FPGA Clock
GCB0_IO27NDB1V0	H22	IPMC_FPGA_LB_nRST	I	FPGA Reset
IPMC Mode				
GFC2_IO67PPB5V0	E1	J6(Pull up & Pull down jump)	I	IPMC MODE SELECT 0 : Stand-alone mode 1 : Shelf mode
HOT SWAP				
EMC_AB_0_IO04NDB0V0	A8	E_HANDLE(Base Hot swap switch pin)	I	Hot-swap Handle switch 0 : Hot-swap Handle closed 1 : Hot-swap Handle open
Payload RESET Control				
EMC_AB_5_IO06PDB0V0	E12	COLD_RST_B(Cold reset command)	O	Payload will be reset. 0 : Reset 1 : Normal operation
GFB0_IO65NDB5V0	G2	IPMC_PUSH_RESET_L (Push button switch)	I	Reset request from Push Button 0 : Reset detect 1 : Normal operation
GCA0_IO28NDB1V0	J19	P20_HRST_REQ_N(Connected from P2041)	I	Reset request from LMP 0 : Reset detect 1 : Normal operation
Slot ID				
EMC_AB_19_IO13PDB0V0	B17	HA0 to ZONE1(Power connector)	I	ATCA Slot ID0
EMC_DB_13_GAC2_IO70PDB5V0	D3	HA1 to ZONE1(Power connector)	I	ATCA Slot ID1
EMC_CS0_N_GAB0_IO01NDB0V0	A5	HA2 to ZONE1(Power connector)	I	ATCA Slot ID2
EMC_AB_6_IO07NDB0V0	B12	HA3 to ZONE1(Power connector)	I	ATCA Slot ID3
EMC_BYEN_0_GAC0_IO02NDB0V0	B9	HA4 to ZONE1(Power connector)	I	ATCA Slot ID4
GFB2_IO68NDB5V0	F3	HA5 to ZONE1(Power connector)	I	ATCA Slot ID5
EMC_DB_9_GEC1_IO63PDB5V0	G3	HA6 to ZONE1(Power connector)	I	ATCA Slot ID6
GFB1_IO65PDB5V0	F1	HA7 to ZONE1(Power connector)	I	ATCA Slot ID7
Module Control				
EMC_DB_6_GEB0_IO62NDB5V0	J1	RTM_INSERT	I	RTM Present 0 : Insert 1 : Extract
EMC_AB_10_IO09NDB0V0	D11	RTM_ENABLE	O	RTM Module Enable 0 : Enable

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				1 : Disable
EMC_AB_17_IO12PDB0V0	C15	IPMC_RTM_MP_EN	O	RTM Management Power Enable 0 : Disable 1 : Enable
EMC_DB_14_GAB2_IO71NDB5V0	C1	RTM_MP_GOOD	I	RTM Management Power Good 0 : Bad 1 : Good
EMC_DB_7_GEB1_IO62PDB5V0	H1	IPMC_RTM_PWR_EN	O	RTM Power Enable signal 0 : Disable 1 : Enable
EMC_DB_12_IO70NDB5V0	D2	RTM_PWR_GOOD	I	RTM Power Good signal 0 : Bad 1 : Good
IPMB Buffer Control				
GBC2_IO21PDB1V0	C21	IPMC_IPMBA_ENABLE	O	IPMB-A I2C Buffer Enable 0 : Disable 1 : Enable
EMC_AB_1_IO04PDB0V0	A9	IPMC_IPMBA_READY	I	IPMB-A I2C Buffer Ready 0 : Disabled 1 : Enabled
GCA1_IO28PDB1V0	J20	IPMC_IPMBB_ENABLE	O	IPMB-B I2C Buffer Enable 0 : Disable 1 : Enable
EMC_AB_15_IO11PDB0V0	B14	IPMC_IPMBB_READY	I	IPMB-B I2C Buffer Ready 0 : Disabled 1 : Enabled
IO22NDB1V0	E22	NC	O	Not used
EMC_AB_14_IO11NDB0V0	B13	NC	O	Not used
GFC1_IO66PPB5V0	G4	IPMC_RTM_I2C_EN	O	RTM IPMB-L I2C Buffer Enable 0 : Disable 1 : Enable
EMC_AB_21_IO14PDB0V0	F14	IPMC_RTM_I2C_RDY	I	RTM IPMB-L I2C Buffer Ready 0 : Disabled 1 : Enabled
LED Control				
GCB1_IO27PDB1V0	J22	BASE_HS_LED(Blue LED)	O	Hot-swap LED Indicator 0 : Off 1 : On
IO25NDB1V0	H17	BASE_OOS_LED(Red LED)	O	OOS LED Indicator 0 : Off 1 : On
EMC_BYEN_1_GAC1_IO02PDB0V0	C9	BASE_RUN_LED(Green LED)	O	RUN LED Indicator 0 : Off 1 : On
GCC1_IO26PPB1V0	J21	BASE_APP_LED(Amber LED)	O	APP LED Indicator 0 : Off 1 : On
SOL Control				
EMC_AB_13_IO10PDB0V0	A15	SOL_TXD	O	CPU console print to IPMC
GBC0_IO17NPB1V0	E14	SOL_RXD	I	
EMC_DB_3_GEC2_IO60PPB5V0	J4	E_MUX_SEL	O	Console Select 0 : Console print to IPMC 1 : Console print to Front
Power Control				
EMC_DB_10_IO69NPB5V0	F4	12V_EN	O	12V Enable 0 : Off 1 : On
EMC_AB_3_IO05PDB0V0	B11	3V3_EN	O	3.3V Enable 0 : On 1 : Off
EMC_DB_11_IO69PPB5V0	G5	2V5_EN	O	2.5V Enable 0 : Off 1 : On
GFC0_IO66NPB5V0	H5	LMP_1V0_EN	O	LMP 1.0V Enable 0 : On 1 : Off
EMC_DB_2_IO60NPB5V0	K5	NP_1V1_SW_1V0_EN	O	NP 1.1V, SW 1V Enable

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				0 : Off 1 : On
EMC_DB_1_GEB2_IO59PDB5V0	K3	1V5_AVS_EN	O	1.5V,BCM AVS Enable 0 : Off 1 : On
EMC_DB_0_GEA2_IO59NDB5V0	K2	1V2_EN	O	1.2V Enable 0 : On 1 : Off
GBB1_IO18PDB1V0	B20	IPMC_PWR_OK	O	Power OK 0 : Off 1 : On
Reserved GPIO (To CPLD)				
EMC_AB_9_IO08PDB0V0	D13	Connected to CPLD	I/O	FPGA_GPIO0
EMC_AB_7_IO07PDB0V0	A12	Connected to CPLD	I/O	FPGA_GPIO1
EMC_AB_2_IO05NDB0V0	B10	Connected to CPLD	I/O	FPGA_GPIO2
EMC_OEN1_N_IO03PDB0V0	C10	Connected to CPLD	I/O	FPGA_GPIO3
GFA0_IO64NDB5V0	J6	Connected to CPLD	I/O	FGPA_GPIO4
GCC2_IO25PDB1V0	H18	Connected to CPLD	O	RTM Buffer Enable 0 : Enable 1 : Disable
EMC_AB_12_IO10NDB0V0	A14	PLD_TSALL	O	CPLD I/O Floating 0 : Normal 1 : Float
ADC_DAC				
TM0	W8	CN6880_A	O	Thermal monitor
GNDTM0	Y8	CN6880_A	O	Thermal monitor
ADC0	Y9	VDD_2V5	I	Monitoring Power
ADC1	AA8	VDD_3V3	I	Monitoring Power
ADC2	V9	12V	I	Monitoring Power
ADC3	AB8	NP_1V1_A	I	Monitoring Power
TM2	AB12	CN6880_B	O	Thermal monitor
GNDTM1	AA12	CN6880_B	O	Thermal monitor
ADC4	U12	NP_1V1_B	I	Monitoring Power
ADC5	V12	MSW_1V0	I	Monitoring Power
ADC6	V11	MSW_AVS	I	Monitoring Power
ADC7	T12	1V5_A	I	Monitoring Power
ADC8	V14	1V5_B	I	Monitoring Power
TM4	T13	P2041	O	Thermal monitor
GNDTM2	U13	P2041	O	Thermal monitor

9.3. Ethernet Transceiver BCM5221

The BCM5221 is a 10/100 BASE-T Ethernet transceiver that supports MII to MDI interface conversion. The RMII side is connected to the IPMC and the MDI side is connected to the base switch. This port is used for Serial-over-LAN (SOL). The IPMC configures the device through the MDIO interface.

9.4. CPLD

The CPLD LCMXO640C-3FTN256C from Lattices plays important roles in collecting and distributing many hardware signals among the IPMC, the CPU P2041 and many other devices. The LMP configures the CPLD registers for the management. Refer to the CPLD datasheet for details.

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9.5. Managed Objects

The IPMC is responsible to collect and manage the various status of the hardware on the blade such as sensors, events, and other information.

9.5.1. Temperature Sensor and Real Time Clock

The aTCA-N700 has temperature sensors. The major processors including the CN6880s, the LMP and the BCM56842 have temperature monitoring sensors for themselves. The locations of the temperature sensors are all internal to the devices. There are no external sensors.
The real time clock device is required on the board for management purposes.

9.5.2. Sensor Data Record (SDR)

All the sensors on the board contribute to the Sensor Data Records (SDR). The SDR include information such as the sensor type, sensor name, and sensor unit. The SDRs also include the set values such as threshold/hysteresis and the rules for the event generation. IPMI commands can adjust the values. The IPMC is responsible for saving the SDR to the EEPROM on the master-only I2C bus. The Shelf Manager can access these SDR through Sensor Device Commands without knowing the details of the device characteristics on the board.

9.5.3. System Event Log (SEL)

The SEL is a set of the events generated by the IPMC. The triggering of the events is by the threshold values monitored by different kinds of sensors. The IPMC is responsible for the management of the events including detection and saving the SEL information into the EEPROM. The information includes time stamp, the name of the sensor, and the cause of the event.

9.5.4. Field Replaceable Unit (FRU) Information

The FRU information contains the service related information that the blade provides, which includes the board part number, the version, etc. The information is stored in the EEPROM.

9.6. Storage for IPMC Firmware

The IPMC firmware is composed of the boot code and the operational code, which are stored into the embedded flash memory of the IPMC, at 512Kbyte. Upon IPMC reset, the IPMC performs the following operations.

- Device inspection on the master-Only I2C
- IPMC SRAM checking
- IPMB Channel inspection
- IPMC EEPROM information inspection
- FRU information inspection
- Operational Code Checksum inspection
- IPMC active portion of the firmware sanity inspection

After completion of the jobs above, the operational code is executed.

9.7. Blade Reset

The blade level reset signals are controlled by the IPMC. **Figure 9-2** illustrates the device reset signals and their interconnections. The IPMC forwards the command either initiated by the CPU application or the IPMI application to the CPLD and the CPLD decodes the command and sends individual reset to the devices accordingly. Refer to the IPMC and the CPLD pin descriptions for the details.

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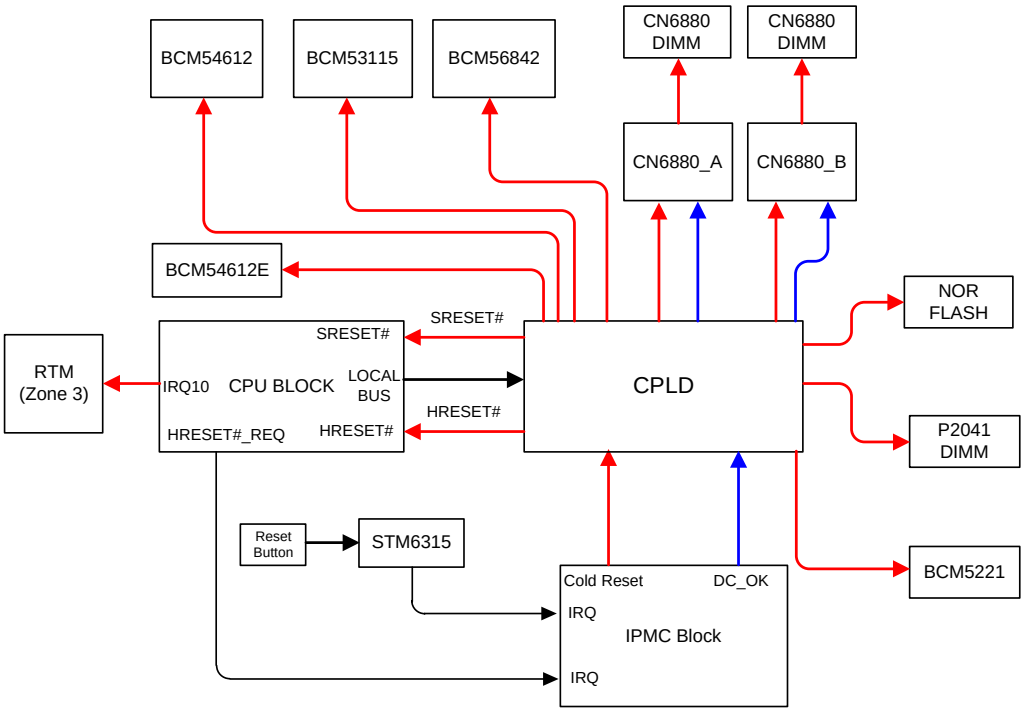


Figure 9-2 Blade Reset Signals

9.8. IPMC and MMC Control Operation

Some of the major chassis management operations are described in Table 9-3 and detailed explanations follow. The MMC is on the optional RTM.

Table 9-3 Board Shutdown and Reset Procedures

No	Item	Description
1	Cold Reset	Cold reset Command from Shelf manager
2	Front Blade Deactivate	Front Blade Deactivate Command from Shelf manager
3	Front Blade Activate	Front Blade activate Command from Shelf manager
4	RTM Deactivate	RTM Deactivate Command from Shelf manager
5	RTM Activate	RTM activate Command from Shelf manager
6	Front blade shutdown	Front Blade Shutdown Command from LMP
7	RTM shutdown	RTM Shutdown Command from LMP
8	Front Hot swap	Open the Hot-swap switch of Front blade
9	RTM Hot swap	Open the Hot-swap switch of RTM

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■ Cold Reset triggered by Shelf manager

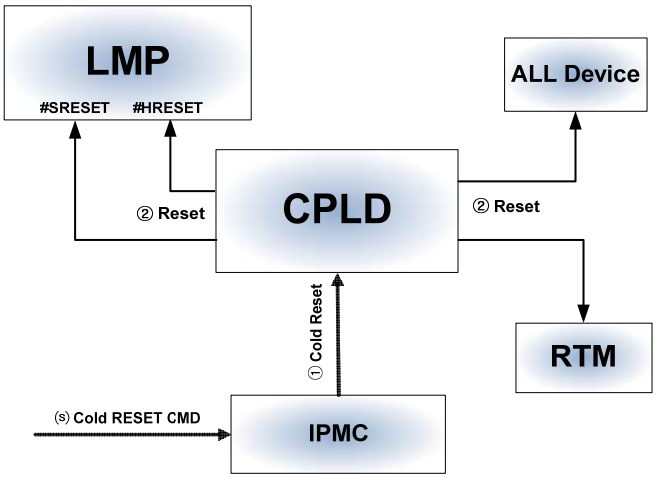


Figure 9-3 Cold Reset Procedure

(s) Shelf manager sends RESET command to IPMC.
① IPMC converts the command into Cold reset signal to FPGA.
② FPGA sends Resets to LMP and all Devices including RTM.

Table 9-4 Signals: Cold Reset Procedure

Signal name	Descriptions
Cold RESET	Cold RESET Command 0 : Cold RESET 1 : Normal operation
RESET	RESET Command 0 : RESET 1 : Normal operation

■ Deactivate

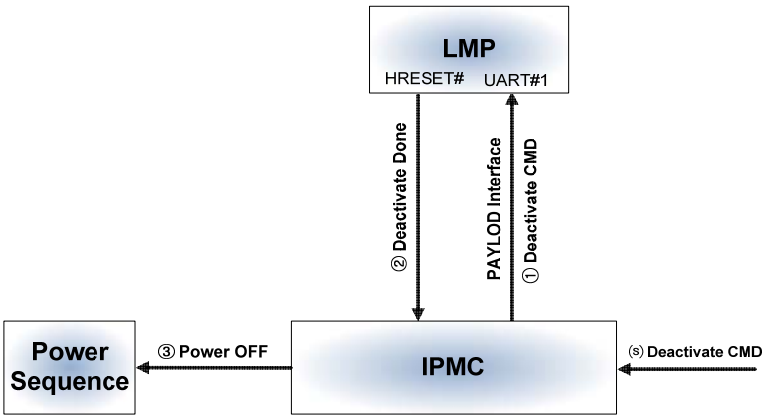


Figure 9-4 Deactivate Procedure

⑸ Shelf manager sends Deactivate to IPMC.
① IPMC sends Deactivate to LMP via PAYLOAD Interface (UART).
② LMP completes the operation and sends the completion message via PAYLOAD Interface (UART) to IPMC.
③ IPMC initiates Power Down sequence to power off Front Blade and RTM.

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Table 9-5 Signals: Deactivate Procedure

Signal name	Descriptions
PAYLOAD Interface	Deactivate Command - IPMI Message
HRESET#	Deactivate Done Indicator 0 : Deactivate Done 1 : Normal

- Activate

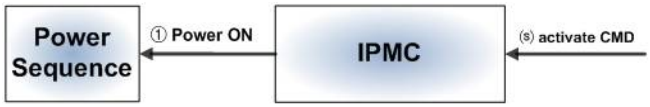


Figure 9-5 Activate Procedure

ⓢ Shelf manager sends Active Command to IPMC.
① IPMC initiates Power ON sequence to power ON Front Blade and RTM.

Table 9-6 Signals: Activate Procedure

Signal name	Descriptions
PAYLOAD Interface	Activate Command - IPMI Message Activate Done Indicator - IPMI Message

- RTM Deactivate

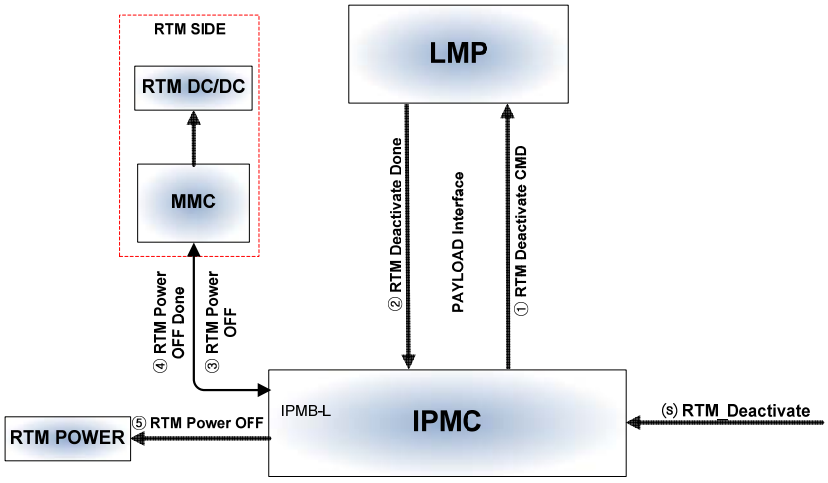


Figure 9-6 RTM Deactivate Procedure

ⓢ Shelf manager sends RTM Deactivate Command to IPMC.
① IPMC sends RTM Deactivate to LMP via PAYLOAD Interface (UART).
② LMP completes the operation and sends completion message to IPMC.
③ IPMC sends RTM Power OFF command to MMC via IPMB-L.
④ MMC completes RTM Power OFF operation and sends the completion message to IPMC.
⑤ IPMC turns off RTM Power 12V.

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Table 9-7 Signals: RTM Deactivate Procedure

Signal name	Descriptions
PAYLOAD Interface	RTM Deactivate Command - IPMI Message RTM Deactivate Done Indicator - IPMI Message
IPMB-L	RTM Power OFF - IPMI Message RTM Power OFF Done - IPMI Message
P1(4)	RTM Power 12V OFF 0 : Power OFF 1 : Power ON
IPMB-L	RTM Power OFF - IPMI Message RTM Power OFF Done - IPMI Message
MMC :	RTM Internal Power OFF 0 : Power ON 1 : Power OFF

■ RTM Activate

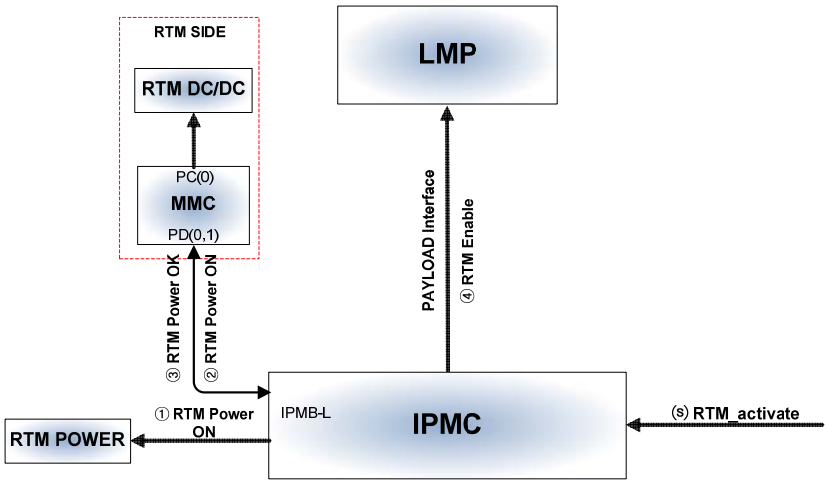


Figure 9-7 RTM Activate Procedure

ⓢ Shelf manager sends RTM Activate to IPMC.
① IPMC turns on RTM Power 12V.
② IPMC sends RTM Power ON Command to MMC via IPMB-L.
③ MMC sends Power OK to IPMC.
④ IPMC sends RTM Enable to LMP via PAYLOAD Interface (UART).

Table 9-8 Signals: RTM Activate Procedure

Signal name	Descriptions
PAYLOAD Interface	RTM Enable Indicator - IPMI Message
IPMB-L	RTM Power ON - IPMI Message RTM Power OK - IPMI Message

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P1(4)	RTM Power 12V ON 0 : Power ON 1 : Power OFF
IPMB-L MMC	RTM Power OFF - IPMI Message RTM Power OFF Done - IPMI Message
MMC	RTM Internal Power OFF 0 : Power ON 1 : Power OFF

■ Shutdown triggered by LMP

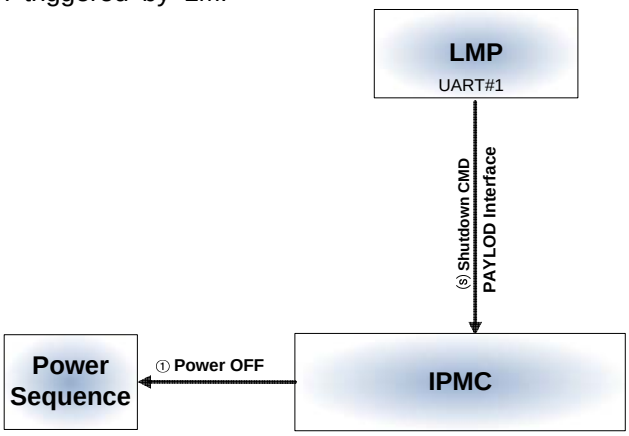


Figure 9-8 Shutdown Procedure

ⓢ LMP sends Shutdown Command to IPMC via PAYLOAD Interface (UART).
① IPMC initiates Power Down sequence to turn off Blade and RTM power.

Table 9-9 Signals: Shutdown Procedure

Signal name	Descriptions
PAYLOAD Interface	Shutdown Command - IPMI Message

■ RTM Shutdown triggered by LMP

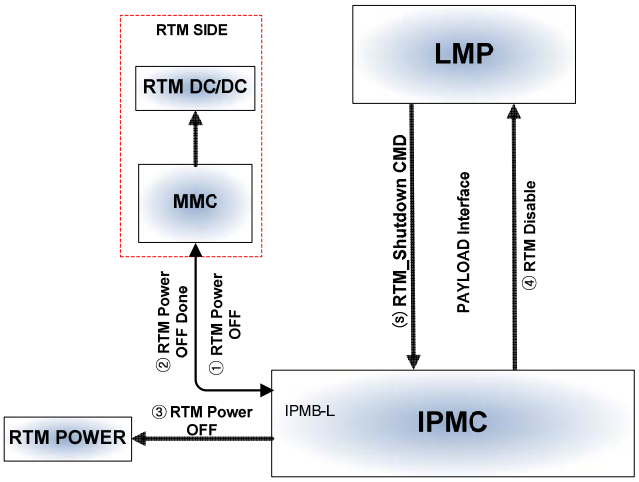


Figure 9-9 RTM Shutdown Procedure

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ⓢ LMP sends RTM Shutdown to IPMC via PAYLOAD Interface (UART).
① IPMC sends RTM Power OFF to MMC via IPMB-L.
② MMC completes RTM Power OFF operation and sends the completion message to IPMC.
③ IPMC turns off RTM Power 12V.
④ IPMC sends RTM Disable information to LMP via PAYLOAD Interface (UART).

Table 9-10 Signals: RTM Shutdown Procedure

Signal name	Descriptions
PAYLOAD Interface	RTM Shutdown Command - IPMI Message RTM Disable Indicator - IPMI Message
IPMB-L	RTM Power OFF - IPMI Message RTM Power OFF Done - IPMI Message
IPMC	RTM Power 12V OFF 0 : Power OFF 1 : Power ON
IPMB-L MMC	RTM Power OFF - IPMI Message RTM Power OFF Done - IPMI Message
MMC	RTM Internal Power OFF 0 : Power ON 1 : Power OFF

■ Hot Swap

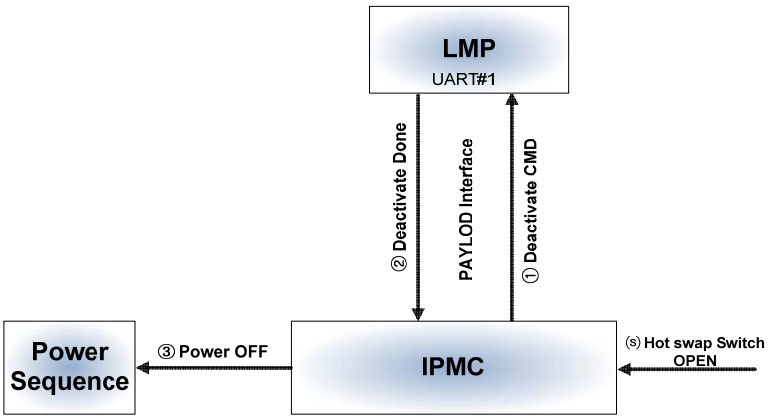


Figure 9-10 Hot Swap Procedure

ⓢ Hot swap Latch Open operation triggers a signal to IPMC.
① IPMC sends Deactivate command to PAYLOAD Interface (UART).
② LMP completes the operation and sends the completion message to IPMC via PAYLOAD Interface (UART).
③ IPMC initiates Power Down sequence and turns off Blade and RTM power.

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Table 9-11 Signals: Hot Swap Procedure

Signal name	Descriptions
PAYLOAD Interface	Deactivate Command - IPMI Message Deactivate Done Indicator - IPMI Message
	Hot swap Indicator 0 : Hot swap Indicator 1 : Normal operation

■ RTM Hot Swap

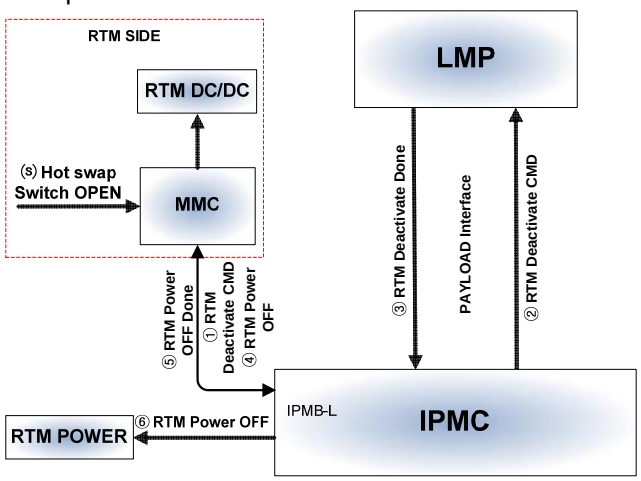


Figure 9-11 RTM Hot Swap Procedure

ⓢ RTM Hot swap switch open operation triggers a signal to MMC.
① MMC sends RTM Deactivate command to IPMC.
② IPMC forwards RTM Deactivate command to LMP via PAYLOAD Interface (UART).
③ LMP completes the operation and sends the completion message to IPMC via PAYLOAD Interface (UART).
④ IPMC sends RTM Power OFF to MMC via IPMB-L.
⑤ MMC completes operation and sends the completion message to IPMC.
⑥ IPMC turns off RTM Power 12V.

Table 9-12 Signals: RTM Hot Swap Procedure

Signal name	Descriptions
PAYLOAD Interface	RTM Deactivate Command - IPMI Message RTM Deactivate Done Indicator - IPMI Message
IPMB-L	RTM Power OFF - IPMI Message RTM Power OFF Done - IPMI Message
IPMC	RTM Power 12V OFF 0 : Power OFF 1 : Power ON

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IPMB-L MMC	RTM Power OFF - IPMI Message RTM Power OFF Done - IPMI Message
MMC	RTM Internal Power OFF 0 : Power ON 1 : Power OFF
MMC	Hot swap Indicator 0 : Hot swap Indicator 1 : Normal operation

9.9. Power and Temperature Threshold

The threshold values of the voltage rails and the temperatures of the devices are managed as summarized in Table 9-13 and Table 9-14.

Table 9-13 Threshold Values: Voltage

Title	Thresholds	Hysteresis
ATCA-N700 -48V_A	UNR : -77V UC : -72V UNC : -60V LNC : -40V LC : -36V LNR : -30V	0.7V
ATCA-N700 -48V_B	UNR : -77V UC : -72V UNC : -60V LNC : -40V LC : -36V LNR : -30V	0.7V
ATCA-N700 +12V	UNR : +14.75V UC : +13.2V UNC : +12.6V LNC : +11.4V LC : +10.8V LNR : +6V	0.1V
ATCA-N700 +3.3V_PRE	UNR : TBD UC : +3.6V UNC : +3.465V LNC : +3.135V LC : +3V LNR : TBD	0.04V
ATCA-N700 +3.3V	UNR : +3.66V UC : +3.46V UNC : N/A LNC : +3.135V LC : +2.97V LNR : +2.7V	0.04V
ATCA-N700 +2.5V	UNR : +2.96V UC : +2.62V UNC : N/A LNC : N/A LC : +2.38V LNR : _+1.9V	0.03V
ATCA-N700 +1.5V_A	UNR : +2.048V UC : +1.575V UNC : N/A LNC : N/A LC : +1.425V LNR : +0.9V	0.02V
ATCA-N700 +1.5V_B	UNR : +2.048V UC : +1.575V UNC : N/A LNC : N/A LC : +1.425V LNR : +0.9V	0.02V

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ATCA-N700 +1.2V	UNR : +1.8V UC : +1.32V UNC : +1.26V LNC : N/A LC : +1.14V LNR : +0.6V	0.01V
ATCA-N700 +1.0V	UNR : +1.6V UC : +1.05V UNC : N/A LNC : N/A LC : +0.95V LNR : +0.4V	0.01V
ATCA-N700 +1.1V_NPA	UNR : +1.7V UC : +1.13V UNC : N/A LNC : N/A LC : +1.07V LNR : +0.5V	0.01V
ATCA-N700 +1.1V_NPB	UNR : +1.7V UC : +1.13V UNC : N/A LNC : N/A LC : +1.07V LNR : +0.5V	0.01V
ATCA-N700 +1V_SWT	UNR : +1.6V UC : +1.03V UNC : N/A LNC : N/A LC : +0.97V LNR : +0.4V	0.01V
ATCA-N700 AVS_SWT	UNR : +1.6V UC : +1.03V UNC : N/A LNC : N/A LC : +0.875V LNR : +0.4V	0.01V
ATCA-N700 +0.75V_LMP	UNR : +1.35V UC : +1.02V UNC : +0.7875V LNC : +0.6625V LC : +0.65V LNR : +0.15V	0.01V
ATCA-N700 +0.75V_NPA_A	UNR : +1.35V UC : +1.02V UNC : +0.7875V LNC : +0.6625V LC : +0.65V LNR : +0.15V	0.01V

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ATCA-N700 +0.75V_NPA_B	UNR : +1.35V UC : +1.02V UNC : +0.7875V LNC : +0.6625V LC : +0.65V LNR : +0.15V	0.01V
ATCA-N700 +0.75V_NPB_A	UNR : +1.35V UC : +1.02V UNC : +0.7875V LNC : +0.6625V LC : +0.65V LNR : +0.15V	0.01V
ATCA-N700 +0.75V_NPB_B	UNR : +1.35V UC : +1.02V UNC : +0.7875V LNC : +0.6625V LC : +0.65V LNR : +0.15V	0.01V

Table 9-14 Threshold Values: Temperature

Title	Thresholds(Tmax = Tj)	Hysteresis
ATCA-N700 NPA Temp	UNR : 111℃ UC : 101℃ UNC : 91℃	2℃
ATCA-N700 NPB Temp	UNR : 111℃ UC : 101℃ UNC : 91℃	2℃
ATCA-N700 SWT Temp	UNR :120℃ UC : 110℃ UNC : 100℃	2℃
ATCA-N700 LMP Temp	UNR :115℃ UC : 105℃ UNC : 95℃	2℃

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10. Power

In this section, we describe the blade power consumption, power distribution, and power monitoring/control.

10.1. Maximum Power Consumption

Without the optional TCAM mezzanine board, the typical operating power max is estimated at about 273 watts and the maximum power consumption is at 307 watts. With the TCAM mezzanine board, it is anticipated to be 330W (typical max.) and 350W, respectively.

10.2. Power Distribution

The blade is fed by the dual -48V from the backplane. The incoming -48Vs are converted by an ATCA Bus Converter PIM400 and a DC-DC Converter QBVW033A0B bus converter into 12V, which again feeds different DC/DC converters to generate necessary voltages as can be seen in Figure 10-1.

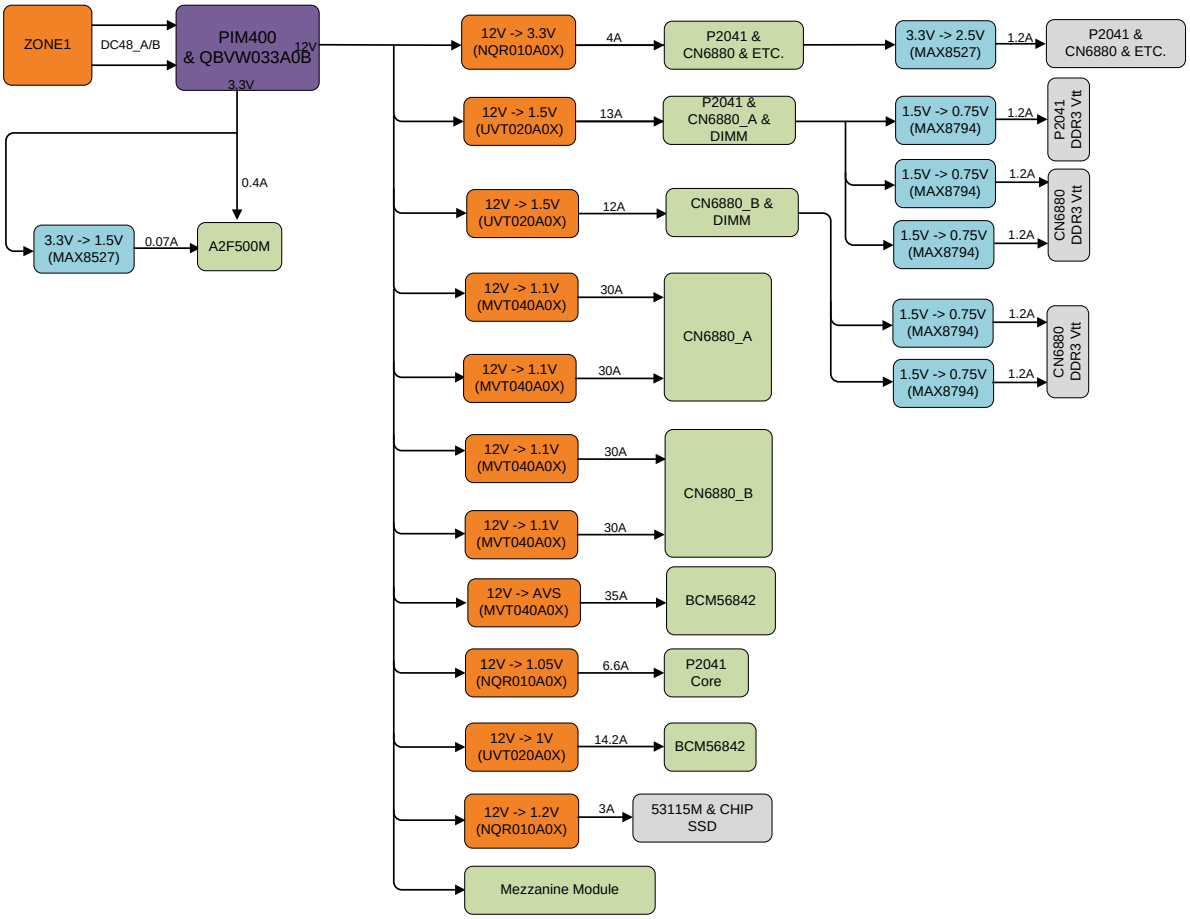


Figure 10-1 Power Distribution

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10.3. Power Sequencing

As illustrated in **Figure 10-2**, the different power rails are required to power up in sequence. The system CPLD along with the IPMC is responsible to generate the necessary signals. Monitoring of all the power rails is done by the IPMC.

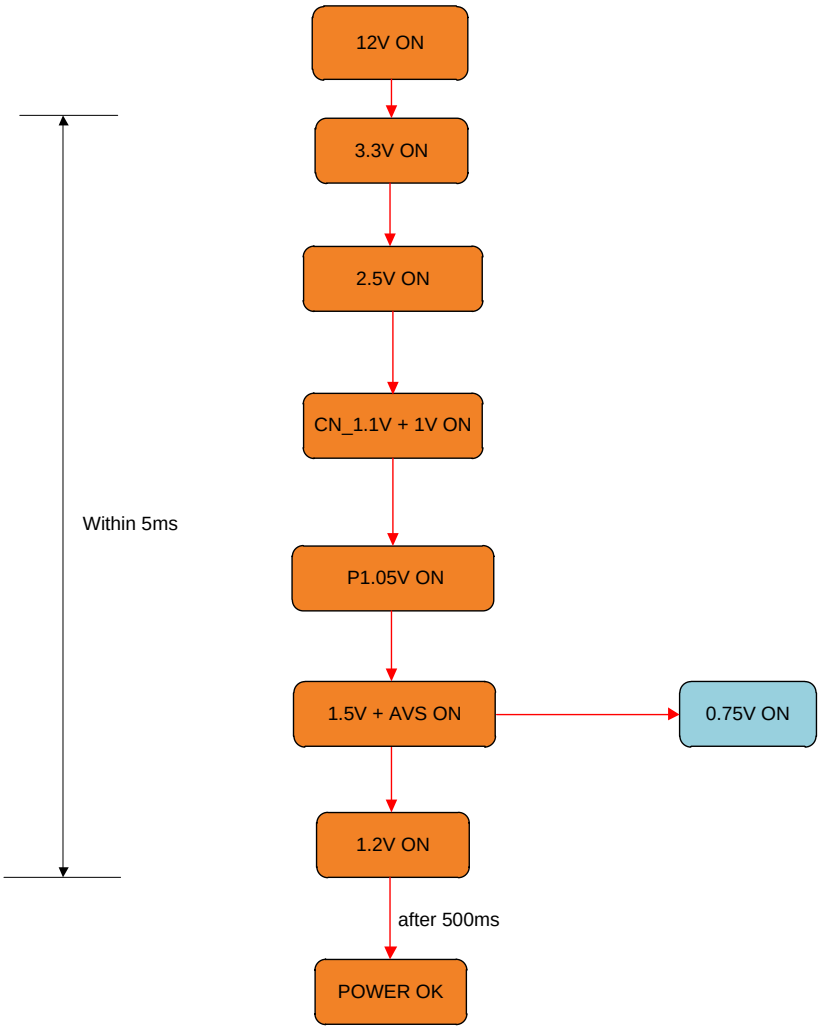


Figure 10-2 Power Sequencing

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11. Clock Tree

This section summarizes the clock tree of the board. Since there are no global synchronous operation requirements, the ATCA backplane sync clock interface (CLK1, 2 and 3) are not present on the blade.

11.1. IPMC and CPLD Clocks

The IPMC, and the CPLD are control domain devices, which are independent from the data plane. The clocks for these devices are shown in **Figure 11-1**.

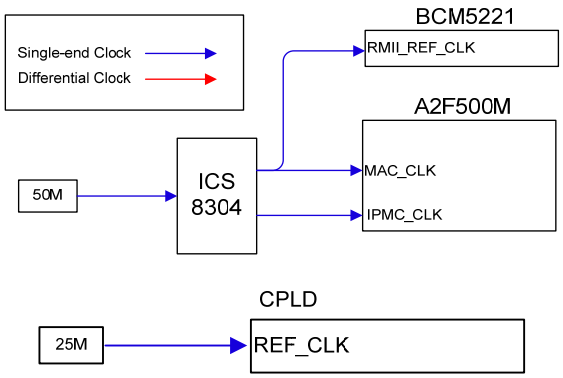


Figure 11-1 IPMC and CPLD Clocks

11.2. Major Device Clocks

The data plane devices require reference clocks to drive SerDes signals. Since there is no need for global synchronous operation on the SerDes ports, each device may get their own clock references according to the device clock requirements. Three ICS85104 clock buffers are used for the 10G SerDes interface references. **Figure 11-2** illustrates the clock distributions for the major devices, used for the data plane signals. All the PCI-e clock references come from a single source, ICS557-05, and are distributed to four different devices, two CN6880s, the LMP, and the BCM56842.

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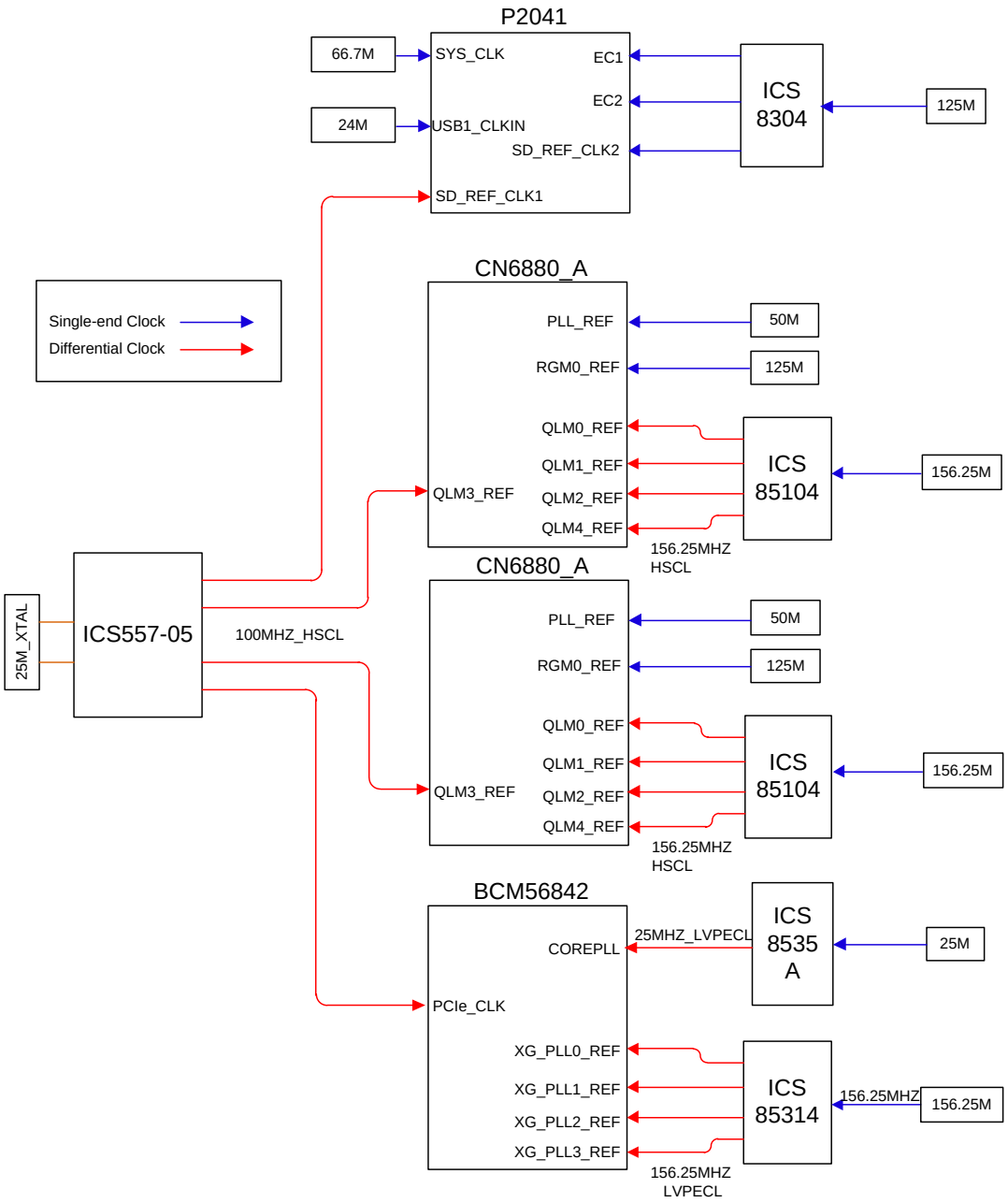


Figure 11-2 Clocks for NPUs, LMP, and Switch Fabric

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12. Layout

This section describes the board outline including major component placement and PCB layers.

12.1. Mechanical Drawing and Placement

The blade is complaint to PICMG 3.0 outline specifications. Shown in Figure 12-1 is the outline (preliminary) of the blade with its faceplate and a preliminary try for the placement. The final version of the layout may differ. Note that the air flow comes from the bottom left to the top right. The major devices and their heat sinks are aligned to maximize the benefit of such air flow direction.

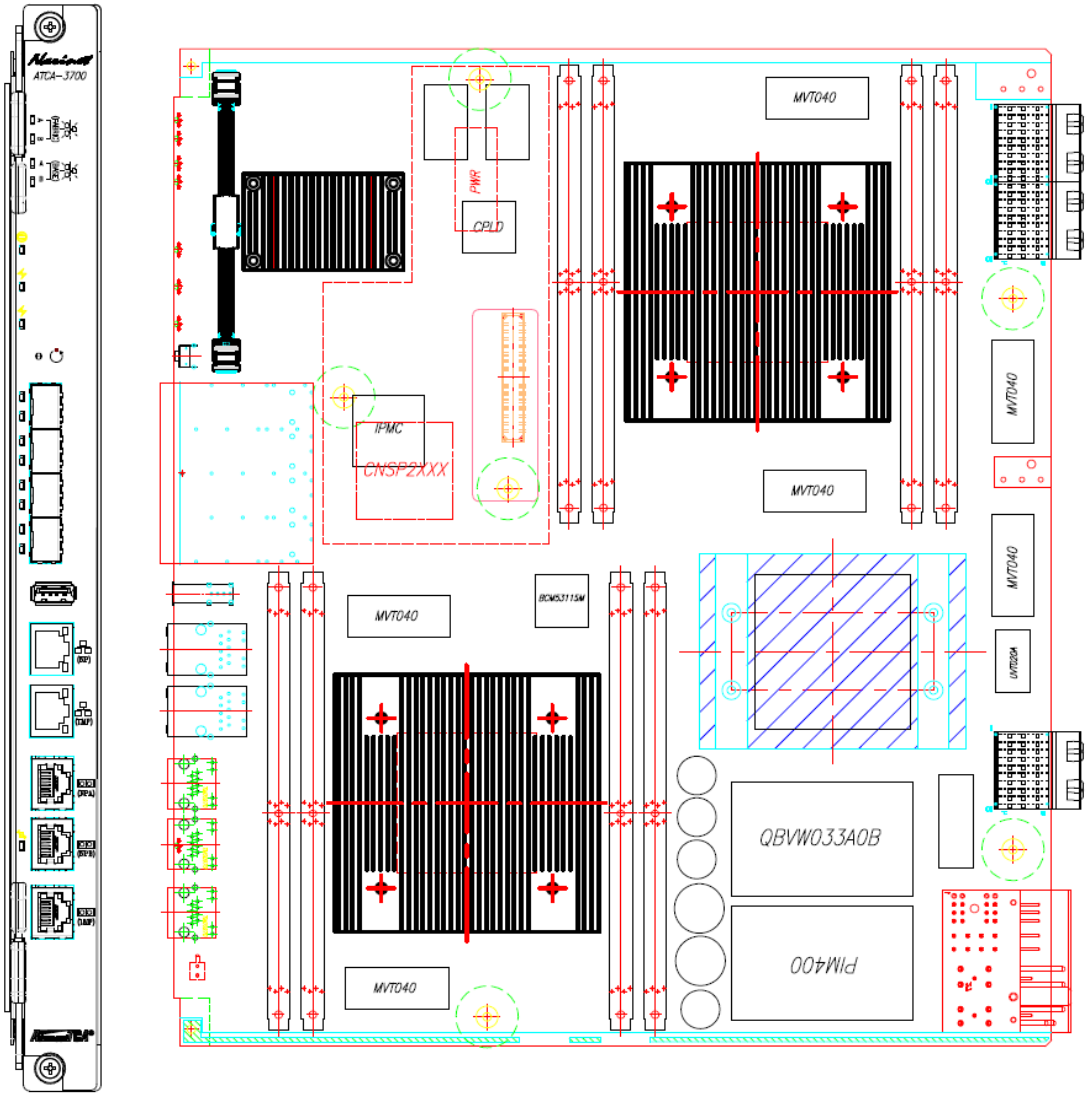


Figure 12-1 Faceplate and component placement

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12.2. PCB Layer Stack-up

At the specified thickness of 2.45mm, a PCB may have around 20 internal layers. The blade is targeted to have 20 layers of PCB laminate with a material compliant to a high speed, low loss epoxy such as TU872SLK, which has a low dielectric constant (Dk ~ 3.6 at 10GHz) and low dissipation factor (Df ~ 0.008 at 10GHz). Figure 12-2 shows a layer stack-up example, which is subject to change.

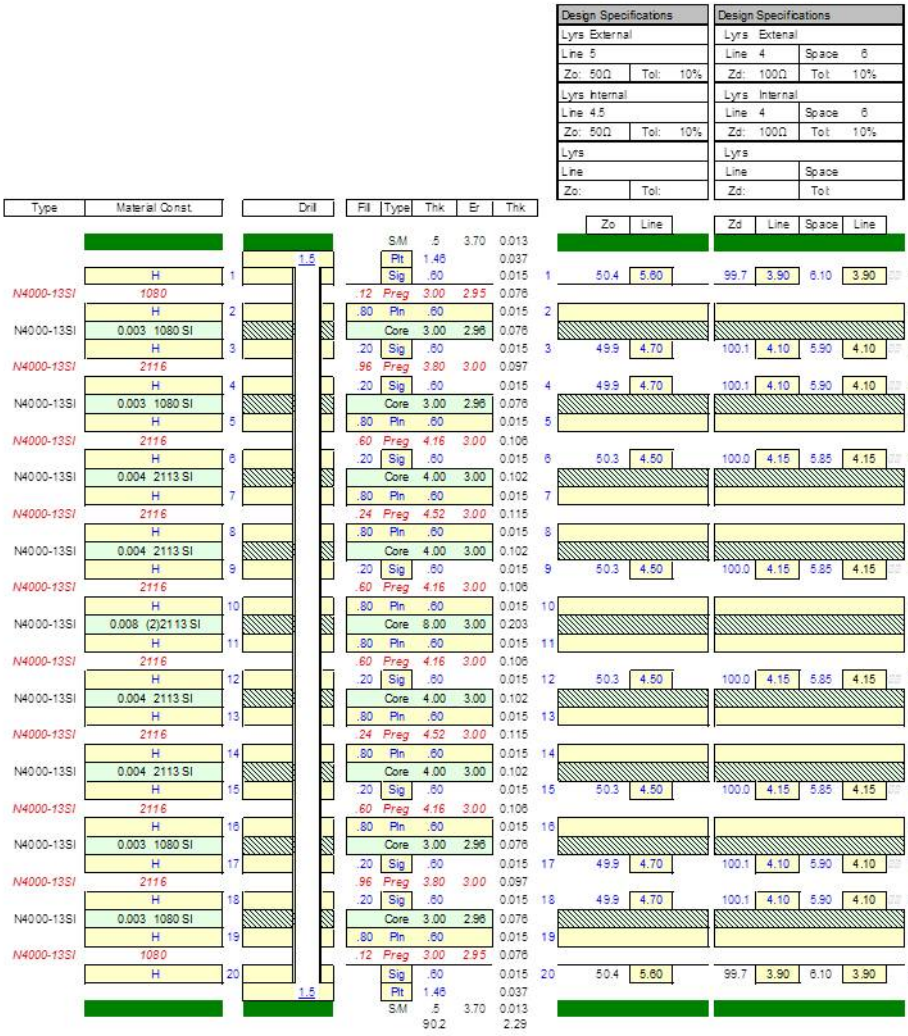


Figure 12-2 PCB layer stack-up (preliminary)

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Appendix

Note* I/O is from the viewpoint of the Front Blade. Unspecified pins are N.C.

Table A-1 Zone 2 Connector Pin-out: J23

PIN	A	B	C	D	E	F	G	H
1	FAB_B_TX_P_2	FAB_B_TX_N_2	FAB_B_RX_P_2	FAB_B_RX_N_2	FAB_B_TX_P_3	FAB_B_TX_N_3	FAB_B_RX_P_3	FAB_B_RX_N_3
2	FAB_B_TX_P_0	FAB_B_TX_N_0	FAB_B_RX_P_0	FAB_B_RX_N_0	FAB_B_TX_P_1	FAB_B_TX_N_1	FAB_B_RX_P_1	FAB_B_RX_N_1
3	FAB_A_TX_P_2	FAB_A_TX_N_2	FAB_A_RX_P_2	FAB_A_RX_N_2	FAB_A_TX_P_3	FAB_A_TX_N_3	FAB_A_RX_P_3	FAB_A_RX_N_3
4	FAB_A_TX_P_0	FAB_A_TX_N_0	FAB_A_RX_P_0	FAB_A_RX_N_0	FAB_A_TX_P_1	FAB_A_TX_N_1	FAB_A_RX_P_1	FAB_A_RX_N_1
5	B_GETH1_P0	B_GETH1_N0	B_GETH1_P1	B_GETH1_N1	B_GETH1_P2	B_GETH1_N2	B_GETH1_P3	B_GETH1_N3
6	B_GETH2_P0	B_GETH2_N0	B_GETH2_P1	B_GETH2_N1	B_GETH2_P2	B_GETH2_N2	B_GETH2_P3	B_GETH2_N3
7								
8								
9								
10								

Signal Name	I/O	Description
FAB_B_TX_P/N_2	O	Fabric Interface Port 2
FAB_B_RX_P/N_2	I	Fabric Interface Port 2
FAB_B_TX_P/N_3	O	Fabric Interface Port 3
FAB_B_RX_P/N_3	I	Fabric Interface Port 3
FAB_B_TX_P/N_0	O	Fabric Interface Port 0
FAB_B_RX_P/N_0	I	Fabric Interface Port 0
FAB_B_TX_P/N_1	O	Fabric Interface Port 1
FAB_B_RX_P/N_1	I	Fabric Interface Port 1
FAB_A_TX_P/N_2	O	Fabric Interface Port 2
FAB_A_RX_P/N_2	I	Fabric Interface Port 2
FAB_A_TX_P/N_3	O	Fabric Interface Port 3
FAB_A_RX_P/N_3	I	Fabric Interface Port 3
FAB_A_TX_P/N_0	O	Fabric Interface Port 0
FAB_A_RX_P/N_0	I	Fabric Interface Port 0
FAB_A_TX_P/N_1	O	Fabric Interface Port 1
FAB_A_RX_P/N_1	I	Fabric Interface Port 1
B_GETH1_P/N [0:3]	I/O	Base Interface Port 0
B_GETH2_P/N [0:3]	I/O	Base Interface Port 1

Table A-2 Zone 3 Connector Pin-out: J31

PIN	A	B	C	D	E	F	G	H
1	RTM_12V	RTM_12V	RTM_12V	RTM_MP		RTM_INSERT		RTM_ENABLE
2	RTM_12V	RTM_12V	RTM_12V		RTM_SCL_B	RTM_SDA_B		
3								
4			IRQ_RTM_B					RTM_RESET_B
5	RTM_DIAG_EN							
6							LMP_RTM_SCL	LMP_RTM_SDA
7						SW_MDC_B		
8							SW_MDIO_B	
9								
10								

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RTM_12V	O	RTM 12V from Front Blade
RTM_MP	O	RTM 3.3V from Front Blade
RTM_INSERT	I	RTM Presence signal to IPMC (to GPIO) 1: No presence (3.3V) 0: RTM Inserted
RTM_ENABLE	O	RTM Enable signal driven by IPMC (via GPIO). Implements ENABLE# per AMC.0 Section 3.6. 0: Enable 1: Disable
RTM_SCL_B	O	IPMB-L from IPMC (to RTM MMC)
RTM_SDA_B	I/O	IPMB-L from IPMC (to RTM MMC)
IRQ_RTM_B	I	Interrupt to LMP 0: Interrupt 1: Normal, no interrupt
RTM_RESET_B	O	LMP reset signal to MMC for RTM payload reset 0: Reset 1: Normal
LMP_RTM_SCL	O	LMP I2C for RTM
LMP_RTM_SDA	I/O	LMP I2C for RTM

Table A-3 Zone 3 Connector Pin-out: J32

PIN	A	B	C	D	E	F	G	H
1	RTM_SFP_RX_P_0	RTM_SFP_RX_N_0	RTM_SFP_RX_P_1	RTM_SFP_RX_N_1	RTM_SFP_RX_P_2	RTM_SFP_RX_N_2	RTM_SFP_RX_P_3	RTM_SFP_RX_N_3
2	RTM_SFP_TX_P_0	RTM_SFP_TX_N_0	RTM_SFP_TX_P_1	RTM_SFP_TX_N_1	RTM_SFP_TX_P_2	RTM_SFP_TX_N_2	RTM_SFP_TX_P_3	RTM_SFP_TX_N_3
3	RTM_SFP_RX_P_4	RTM_SFP_RX_N_4	RTM_SFP_RX_P_5	RTM_SFP_RX_N_5	RTM_SFP_RX_P_6	RTM_SFP_RX_N_6	RTM_SFP_RX_P_7	RTM_SFP_RX_N_7
4	RTM_SFP_TX_P_4	RTM_SFP_TX_N_4	RTM_SFP_TX_P_5	RTM_SFP_TX_N_5	RTM_SFP_TX_P_6	RTM_SFP_TX_N_6	RTM_SFP_TX_P_7	RTM_SFP_TX_N_7
5	RTM_SFP_RX_P_8	RTM_SFP_RX_N_8	RTM_SFP_RX_P_9	RTM_SFP_RX_N_9	RTM_SFP_RX_P_10	RTM_SFP_RX_N_10	RTM_SFP_RX_P_11	RTM_SFP_RX_N_11
6	RTM_SFP_TX_P_8	RTM_SFP_TX_N_8	RTM_SFP_TX_P_9	RTM_SFP_TX_N_9	RTM_SFP_TX_P_10	RTM_SFP_TX_N_10	RTM_SFP_TX_P_11	RTM_SFP_TX_N_11
7	RTM_LED_CLK0_B	RTM_LED_DATA0_B	RTM_LED_CLK1_B	RTM_LED_DATA1_B				
8								
9	BSC_SCL_B	BSC_SDA_B						
10								

Signal Name	I/O	Description
RTM_SFP_RX_P/N_[0:3]	I	SFP+ ports RX: Port 1~4
RTM_SFP_TX_P/N_[0:3]	O	SFP+ ports TX: Port 1~4
RTM_SFP_RX_P/N_[4:7]	I	SFP+ ports RX: Port 5~8
RTM_SFP_TX_P/N_[4:7]	O	SFP+ ports TX: Port 5~8
RTM_SFP_RX_P/N_[8:11]	I	SFP+ ports RX: Port 9~12
RTM_SFP_TX_P/N_[8:11]	O	SFP+ ports TX: Port 9~12
RTM_LED_CLK0/1_B	O	LED control CLK from Switch Fabric Device for the SFP+ ports
RTM_LED_DATA0/1_B	O	LED control DATA from Switch Fabric Device for the SFP+ ports
BSC_SCL_B	O	I2C connected to Switch Fabric Device
BSC_DATA_B	I/O	I2C connected to Switch Fabric Device

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Safety

1. Please read these safety instructions carefully.
2. Please keep this User‘s Manual for later reference.
3. One AC Inlets provided and service as Disconnect Devices, disconnect the equipment from both AC outlets use these AC Inlets before servicing or clearing. Use moisture sheet or cloth for cleaning.
4. For pluggable equipment, that the socket-outlet shall be installed near the equipment and shall be easily accessible.
5. Please keep this equipment from humidity.
6. Lay this equipment on a reliable surface when install. A drop or fall could cause injury.
7. Make sure the voltage of the power source when connect the equipment to the power outlet.
8. Place the power cord such a way that people can not step on it. Do not place anything over the power cord.
9. All cautions and warnings on the equipment should be noted.
10. If the equipment is not use for long time, disconnect the equipment from mains to avoid being damaged by transient overvoltage.
11. Never pour any liquid into openings; this could cause fire or electrical shock.
12. Never open the equipment. For safety reason, the equipment should only be opened by qualified service personnel.
13. If one of the following situations arises, get the equipment checked by a service personnel:
    a. The Power cord or plug is damaged.
    b. Liquid has penetrated into the equipment.
    c. The equipment has been exposed to moisture.
    d. The equipment has not work well or you can not get it work according to user‘s manual.
    e. The equipment has dropped and damaged.
    f. If the equipment has obvious sign of breakage.

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Consignes de Sécurité

1. Veuillez lire attentivement ces consignes de sécurité.
2. Veuillez garder ce manuel de l'utilisateur pour référence ultérieure.
3. Une entrée de courant est fournie pour l'entretien de l'appareil débranché. Débrancher l'appareil des prises de courant et utiliser cette entrée de courant avant entretien ou nettoyage. Utilisez un tissu humide ou un chiffon pour le nettoyage.
4. Pour les appareils raccordés, la prise de courant doit être installée près de l'appareil et doit être facilement accessible.
5. Ne pas exposer les appareils à l'humidité.
6. Posez ces appareils sur une surface stable pour les installer. Une chute peut provoquer des blessures.
7. Vérifiez la tension de la source d'alimentation lorsque vous branchez l'appareil à la prise de courant.
8. Placez le cordon d'alimentation de telle manière que personne ne puisse marcher dessus. Ne rien placer sur le cordon d'alimentation.
9. Tous les avertissements concernant ces appareils doivent être respectés.
10. Si un appareil n'est pas utilisé pendant longtemps, débranchez-le du réseau électrique pour éviter qu'il soit endommagé par une surtension.
11. Ne jamais verser de liquide dans les ouvertures, cela pourrait provoquer un incendie ou une décharge électrique.
12. Ne jamais ouvrir l'appareil. Pour des raisons de sécurité, l'appareil ne doit être ouvert que par un personnel qualifié.
13. Si l'une des situations suivantes se présente, faites vérifier l'appareil par le personnel de service :
    g. Le cordon d'alimentation ou la prise sont endommagés.
    h. Du liquide est entré dans l'appareil.
    i. L'appareil a pris l'humidité.
    j. L'appareil ne fonctionne pas bien ou vous ne pouvez pas le faire fonctionner conformément au manuel de l'utilisateur.
    k. L'appareil est tombé et est endommagé.
    l. L'appareil présente des signes évidents de bris.

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