cExpress-AL

User's Manual

COM Express Compact Size Type 6 Module with
Intel Atom®, Pentium®, Celeron® SoC



COM Express®

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Part Number:	50-1J068-1020

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Preface

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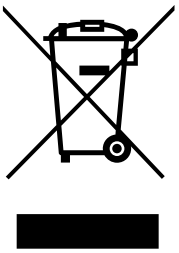
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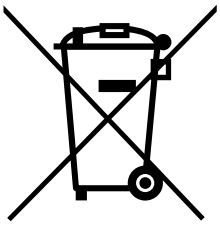
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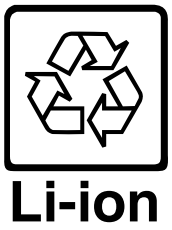
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Revision History

Revision	Description	Date	By
1.0	Initial release	2017-12-04	JC
1.1	Update specifications, PCIe port options, BIOS setup menu	2018-04-23	JC
1.2	Update dual BIOS to “build option”; update Ethernet controller temperature support	2019-12-06	JC

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1. Introduction

The cExpress-AL is a COM Express COM.0 R3.0 Type 6 module supporting the Intel Atom® processor, Intel® Pentium® processor and Intel® Celeron® processor system-on-chip (SoC). The cExpress-AL is specifically designed for customers who need optimized processing and graphics performance with low power consumption in a long product life solution.

The Intel Atom® processor, Intel® Pentium® processor and Intel® Celeron® processor and support non-ECC type DDR3L dual-channel memory at 1600/1867 MHz to provide excellent overall performance. Integrated Intel® Gen9 LP Graphics includes features such as OpenGL 4.3, DirectX 12, OpenCL 2.0; and support for H.265/HEVC, H.264, MPEG2, VC1, VP9, MVC, JPEG/MJPEG hardware decode. Up to three independent displays are available from DDI ports supporting HDMI/DVI/DisplayPort, optional VGA, single/dual-channel 18/24-bit LVDS and optional eDP. The cExpress-AL is specifically designed for customers with balanced performance/power consumption requirements who want to outsource the custom core logic of their systems for reduced development time.

The cExpress-AL has dual stacked SODIMM sockets for up to 8 GB non-ECC type DDR3L memory. Featured IO include a single Gigabit Ethernet port (IEEE 1588 support), USB 3.0 ports and USB 2.0 ports, SATA 6 Gb/s ports, and up to 5 PCIe x1 lanes. In addition, SD signals are muxed with GPIO. Support is provided for SMBus and I^2C. The module is equipped with SPI AMI EFI BIOS (dual BIOS by build option), supporting embedded features such as remote console, CMOS backup, hardware monitor, and watchdog timer. An optional eMMC 5.0 (8/16/32 GB) is supported.

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2. Specifications

2.1. Core System

CPU	Dual or quad-core Intel Atom®, Pentium® or Celeron® Processor SoC • Atom™ E3950 1.6/2.0GHz (Turbo), 400-650MHz (graphics), 12W (4C/1866) • Atom™ E3940 1.6/1.8GHz (Turbo), 400-600MHz (graphics), 9W (4C/1866) • Atom™ E3930 1.3/1.8GHz (Turbo), 400-550MHz (graphics), 6W (2C/1866) • Pentium® N4200 1.1/2.5GHz (Turbo), 200-750MHz (graphics), 6W (4C/1866) • Celeron® N3350 1.1/2.4GHz (Turbo), 200-650MHz (graphics), 6W (2C/1866) Supports: Dual or quad Out-of-Order Execution (OOE) processor cores, Intel® VT-x, Intel® VT-d, Intel® SSE4.1 and SSE4.2, Intel® 64 architecture, Intel® Turbo Boost Technology 2.0, Intel AES-NI, Intel® TXT, PCLMULQDQ instruction DRNG **Notes:** Availability of features may vary between processor SKUs and operating systems. Only Atom™ SKUs can support extreme temperature operating range. Pentium®, Celeron® SKUs are supported by project basis.
Cache	2MB for all SKUs
Memory	Dual channel non-ECC 1600/1867 MHz DDR3L memory up to 8GB in dual stacked SODIMM sockets (lower slot must be populated) **Notes:** maximum by 2pcs 4GB or 1pcs 8GB SODIMM
BIOS	AMI EFI with CMOS backup in 16MB SPI BIOS (dual BIOS by build option)

2.2. Expansion Busses

PCI Express	• 3 PCIe x1 (AB) by default: ports 0/1/2 (direct from SoC) • 5 PCIe x1 (AB) are supported by build option with a PCIe bridge IC (ports 2/3/4 from PCIe bridge IC support x1 only, see 2.16 Functional Diagram below).
Other	• LPC bus • SMBus (system) • I^2C (user)

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2.3. Video

Integrated on Processor	Intel® 9th generation LP graphics core architecture with up to 18 execution units supporting three independent displays
GPU Feature Support	• 3D graphics hardware acceleration • Support for DirectX12/11.3/10/9.3, OCL 2.0, OGL ES 3.0, OGL 4.3 • Video decode hardware acceleration including support for H.265 (HEVC), H.264, MVC, MPEG-2, VC-1, WMV9, VP8/VP9, JPEG/MJPEG formats • Video encode hardware acceleration including support for H.265 (HEVC), H.264, VP8/VP9, JPEG/MJPEG formats • Supports content protection using PAVP 2.0 and HDCP 1.4/2.0 **Note:** Availability of features may vary between operating systems.
Display Types	• **Dual/single channel 18/24-bit LVDS**, supports DE mode and H/V-Sync mode display • **eDP x4 lanes** (eDP 1.3, by build option in place of LVDS) • **DDI1/2** support DisplayPort (DP 1.2), HDMI (1.4b), DVI • **VGA** (via DP-to-VGA IC, by build option in place of DDI2) **Note:** Only two simultaneous HDMI/DVI outputs supported.

2.4. Audio

Integrated	Intel® HD Audio integrated on SoC
Codec	Located on carrier Express-BASE6 (ALC886 standard support)

2.5. LAN

MAC/PHY	Intel® Ethernet Controller I210 (Extreme Rugged operating temperature range) Intel® Ethernet Controller I211 (standard operating temperature range)
Interface	10/100/1000 Mbit/s connection, IEEE 1588 support

Note: Supports GBE0_SDP on A49 pin.

2.6. Multi I/O and Storage

USB	• 3x USB 3.0/2.0/1.1 (USB 0/1/2) • 5x USB 2.0/1.1 (USB 3/4/5/6/7) **Note:** USB port 0 supports USB 2.0 OTG on Yocto Linux OS
SATA	2x SATA 6Gb/s (SATA0, SATA1)
GPIO	4 GPO and 4 GPI **Note:** GPI with interruput supported on Linux.
eMMC 5.0 (build option)	8/16/32 GB (boot device support may vary between operating systems)*
SD	SD 3.0 signal is muxed with GPIO, switching controlled by BIOS setting (boot device support may vary between operating systems)* **Note:** Supports 3.3V SD cards only.

Note: See table below for detailed boot device support information.

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Boot Device Support

		Windows 10 Enterprise	Linux (Yocto)
Storage only	**eMMC 5.0**	Yes	Yes
	SD	Yes	Yes
OS Installation	**eMMC 5.0**	Yes	Yes
	SD	No	No

Note: eMMC and SD functionality as an OS installation device may change dependent on Intel updates. Please contact your local sales representative for more information.

2.7. Serial I/O

- **Ports:** 2x UART ports COM 1/2 (COM 1/2 supports console redirection), baud rate up to 115.2 kbps

Port	Description	IRQ	Address	Console Redirection Support
COM 1	Supported by module (SER0, A98/A99), via NCT5104D	10	0x240	Yes
COM 2	Supported by module (SER1, A101/A102), via NCT5104D	11	0x248	Yes
COM 3	Supported by Super I/O (W83627DHG) on carrier board	4	0x3F8	Yes
COM 4	Supported by Super I/O (W83627DHG) on carrier board	3	0x2F8	Yes

2.8. SEMA Board Controller

- **Type:** ADLINK Smart Embedded Management Agent (SEMA)
- **Functions:**
  - Voltage/Current monitoring
  - Power sequence debug support
  - AT/ATX mode control
  - Logistics and forensic information
  - Flat panel control
  - General purpose I2C
  - Failsafe BIOS (dual BIOS by build option)
  - Watchdog timer and fan control

2.9. Debug

- 40-pin flat cable connector to be used with DB-40 debug module
  Supports: BIOS POST code LED, BMC access, SPI BIOS flashing, power testpoints, debug LEDs
- MIPI60 60-pin header for debug of SoC (build option)

2.10. Trusted Platform Module (TPM)

- **Chipset:** Infineon (build option)
- **Type:** TPM 2.0

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2.11. Power Specifications

Power Modes	AT and ATX mode (AT mode startup controlled by SEMA Board Controller)
Standard Voltage Input	ATX: 12V ±5% / 5Vsb ±5% or AT = 12V ±5%
Wide Voltage Input	ATX: 4.75-20 V / 5Vsb ±5% or AT = 4.75-20 V
Power Management	ACPI 5.0 compliant, Smart Battery support
Power States	Supports C0, C1, C1E, C6L, C6, S0, S3, S4, S5, S5 ECO mode (Wake-on-USB S3/S4, WoL S3/S4/S5)
ECO Mode	Supports deep S5 for 5Vsb power saving

Please contact your ADLINK representative for the document “COM Express Module Power Consumption”.

2.12. Operating Temperatures

Standard Operating Temperature	0°C to +60°C (Wide Voltage Input) Storage: -20°C to +70°C
Extreme Rugged Operating Temperature (optional)	-40°C to +85°C (Standard Voltage Input only, build option supported by Atom™ SKUs only) Storage: -40°C to +85°C

2.13. Environmental

Humidity	Operating: 5-90% RH, non-condensing Storage: 5-95% RH (and operating with conformal coating)
Shock and Vibration	IEC 60068-2-64 and IEC-60068-2-27 MIL-STD-202F, Method 213B, Table 213-I, Condition A and Method 214A, Table 214-I, Condition D
HALT	Thermal Stress, Vibration Stress, Thermal Shock and Combined Test

2.14. Specification Compliance

- PICMG COM.0: Rev. 3.0 Type 6, Compact size 95 x 95 mm

2.15. Operating Systems

Standard Support	• Windows 10 Enterprise 64-bit • Linux 64-bit • VxWorks 64-bit
Extended Support (BSP)	• Linux (64-bit)

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2.16. Functional Diagram

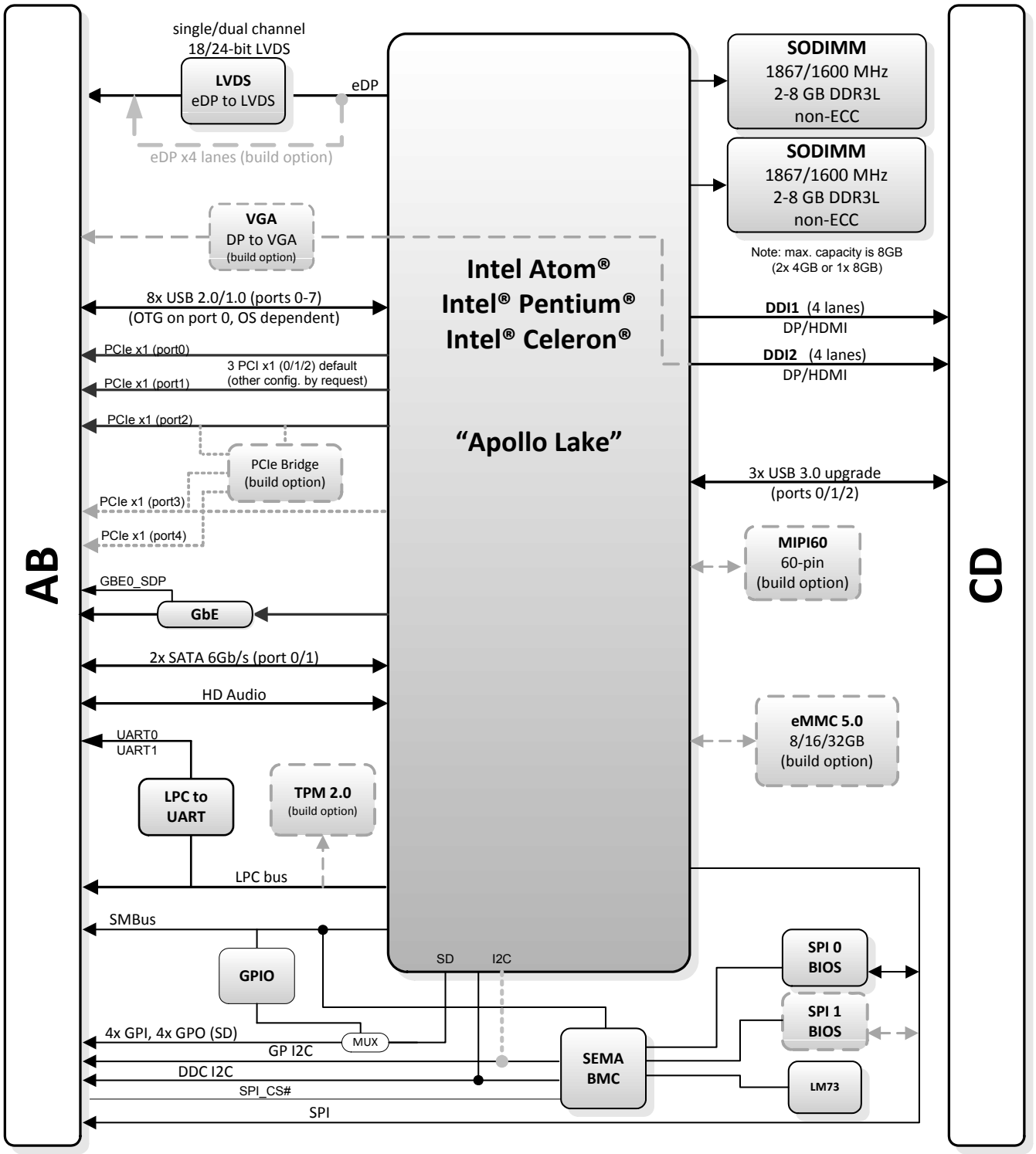
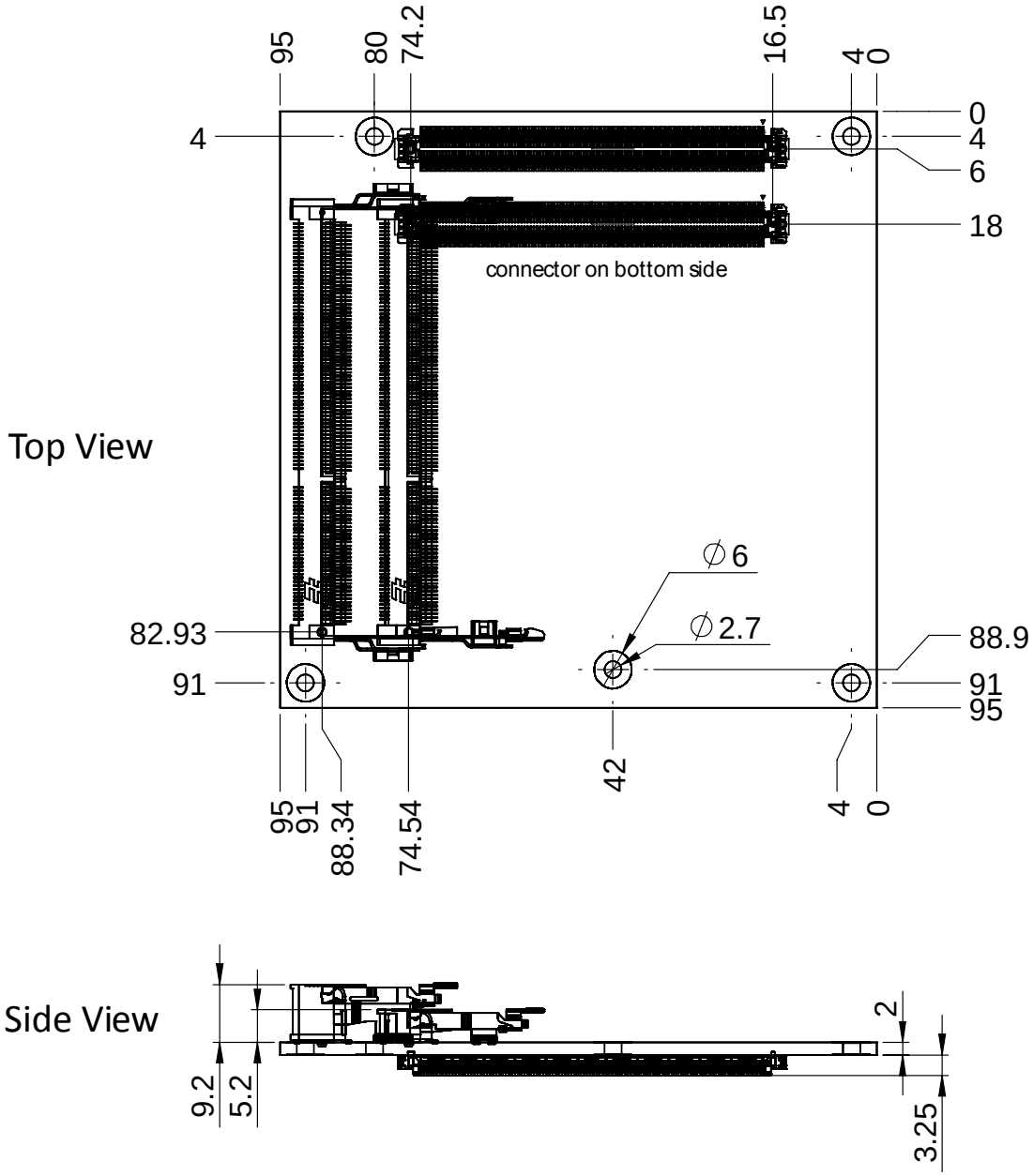


Figure 1: cExpress-AL Functional Block Diagram

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2.17. Mechanical Drawing



All are dimensions shown in millimeters.

Tolerances should be ± 0.25mm, unless otherwise noted. The tolerances of the module connector locating peg holes (16.50, 6.00] and [16.50, 18.00]) should be ±0.10mm.

Figure 2: cExpress-AL Mechanical Drawing

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3. Pinouts and Signal Descriptions

3.1. AB/CD Pin Definitions

The cExpress-AL is a Type 6 module supporting USB 3.0 upgrade signals and DDI channels on the CD connector

All pins in the COM Express specification are described, including those not supported on the cExpress-AL. Those not supported on the cExpress-AL module are ~~crossed out~~.

Table 1: cExpress-AL AB/CD Pin Definitions

	Row A		Row B		Row C		Row D
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**
A1	GND (FIXED)	**B1**	GND (FIXED)	**C1**	GND FIXED)	**D1**	GND FIXED)
A2	GBE0_MDI3-	**B2**	GBE0_ACT#	**C2**	GND	**D2**	GND
A3	GBE0_MDI3+	**B3**	LPC_FRAME#	**C3**	USB_SSRX0-	**D3**	USB_SSTX0-
A4	GBE0_LINK100#	**B4**	LPC_AD0	**C4**	USB_SSRX0+	**D4**	USB_SSTX0+
A5	GBE0_LINK1000#	**B5**	LPC_AD1	**C5**	GND	**D5**	GND
A6	GBE0_MDI2-	**B6**	LPC_AD2	**C6**	USB_SSRX1-	**D6**	USB_SSTX1-
A7	GBE0_MDI2+	**B7**	LPC_AD3	**C7**	USB_SSRX1+	**D7**	USB_SSTX1+
A8	GBE0_LINK#	**B8**	LPC_DRQ0#	**C8**	GND	**D8**	GND
A9	GBE0_MDI1-	**B9**	LPC_DRQ1#	**C9**	USB_SSRX2-	**D9**	USB_SSTX2-
A10	GBE0_MDI1+	**B10**	LPC_CLK	**C10**	USB_SSRX2+	**D10**	USB_SSTX2+
A11	GND (fixed)	**B11**	GND (fixed)	**C11**	GND (fixed)	**D11**	GND (fixed)
A12	GBE0_MDI0-	**B12**	PWRBTN#	**C12**	~~USB_SSRX3-~~	**D12**	~~USB_SSTX3-~~
A13	GBE0_MDI0+	**B13**	SMB_CK	**C13**	~~USB_SSRX3+~~	**D13**	~~USB_SSTX3+~~
A14	GBE0_CTREF	**B14**	SMB_DAT	**C14**	GND	**D14**	GND
A15	SUS_S3#	**B15**	SMB_ALERT#	**C15**	~~DDI1_PAIR6+~~	**D15**	DDI1_CTRLCLK_AUX+
A16	SATA0_TX+	**B16**	SATA1_TX+	**C16**	~~DDI1_PAIR6-~~	**D16**	DDI1_CTRLDATA_AUX
A17	SATA0_TX-	**B17**	SATA1_TX-	**C17**	RSVD	**D17**	RSVD
A18	SUS_S4#	**B18**	SUS_STAT#	**C18**	RSVD	**D18**	RSVD
A19	SATA0_RX+	**B19**	SATA1_RX+	**C19**	~~PCIE_RX6+~~	**D19**	~~PCIE_TX6+~~
A20	SATA0_RX-	**B20**	SATA1_RX-	**C20**	~~PCIE_RX6-~~	**D20**	~~PCIE_TX6-~~
A21	GND (fixed)	**B21**	GND (fixed)	**C21**	GND (fixed)	**D21**	GND (fixed)
A22	~~SATA2_TX+~~	**B22**	~~SATA3_TX+~~	**C22**	~~PCIE_RX7+~~	**D22**	~~PCIE_TX7+~~
A23	~~SATA2_TX-~~	**B23**	~~SATA3_TX-~~	**C23**	~~PCIE_RX7-~~	**D23**	~~PCIE_TX7-~~
A24	SUS_S5#	**B24**	PWR_OK	**C24**	DDI1_HPD	**D24**	RSVD
A25	~~SATA2_RX+~~	**B25**	~~SATA3_RX+~~	**C25**	~~DDI1_PAIR4+~~	**D25**	RSVD
A26	~~SATA2_RX-~~	**B26**	~~SATA3_RX-~~	**C26**	~~DDI1_PAIR4-~~	**D26**	DDI1_PAIR0+
A27	BATLOW#	**B27**	WDT	**C27**	RSVD	**D27**	DDI1_PAIR0-
A28	(S)ATA_ACT#	**B28**	~~HDA_SDIN2~~	**C28**	RSVD	**D28**	RSVD
A29	HDA_SYNC	**B29**	~~HDA_SDIN1~~	**C29**	~~DDI1_PAIR5+~~	**D29**	DDI1_PAIR1+
A30	HDA_RST#	**B30**	HDA_SDIN0	**C30**	~~DDI1_PAIR5-~~	**D30**	DDI1_PAIR1-
A31	GND (fixed)	**B31**	GND (fixed)	**C31**	GND (fixed)	**D31**	GND (fixed)
A32	HDA_BITCLK	**B32**	SPKR	**C32**	DDI2_CTRLCLK_AUX+	**D32**	DDI1_PAIR2+
A33	HDA_SDOUT	**B33**	I2C_CK	**C33**	DDI2_CTRLDATA_AUX-	**D33**	DDI1_PAIR2-
A34	BIOS_DIS0#	**B34**	I2C_DAT	**C34**	DDI2_DDC_AUX_SEL	**D34**	DDI1_DDC_AUX_SEL
A35	THRMTRIP#	**B35**	THRM#	**C35**	RSVD	**D35**	RSVD

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Row A		Row B		Row C		Row D	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
A36	USB6-	B36	USB7-	C36	~~DDI3_CTRLCLK_AUX+~~	D36	DDI1_PAIR3+
A37	USB6+	B37	USB7+	C37	~~DDI3_CTRLDATA_AUX~~	D37	DDI1_PAIR3-
A38	USB_6_7_OC#	B38	USB_4_5_OC#	C38	~~DDI3_DDC_AUX_SEL~~	D38	RSVD
A39	USB4-	B39	USB5-	C39	~~DDI3_PAIR0+~~	D39	DDI2_PAIR0+
A40	USB4+	B40	USB5+	C40	~~DDI3_PAIR0-~~	D40	DDI2_PAIR0-
A41	GND (fixed)	B41	GND (fixed)	C41	GND (fixed)	D41	GND (fixed)
A42	USB2-	B42	USB3-	C42	~~DDI3_PAIR1+~~	D42	DDI2_PAIR1+
A43	USB2+	B43	USB3+	C43	~~DDI3_PAIR1-~~	D43	DDI2_PAIR1-
A44	USB_2_3_OC#	B44	USB_0_1_OC#	C44	~~DDI3_HPD~~	D44	DDI2_HPD
A45	USB0-	B45	USB1-	C45	RSVD	D45	RSVD
A46	USB0+	B46	USB1+	C46	~~DDI3_PAIR2+~~	D46	DDI2_PAIR2+
A47	VCC_RTC	B47	~~ESPI_EN#~~	C47	~~DDI3_PAIR2-~~	D47	DDI2_PAIR2-
A48	RSVD	B48	USB0_HOST_PRSNT	C48	RSVD	D48	RSVD
A49	GBE0_SDP	B49	SYS_RESET#	C49	~~DDI3_PAIR3+~~	D49	DDI2_PAIR3+
A50	LPC_SERIRQ	B50	CB_RESET#	C50	~~DDI3_PAIR3-~~	D50	DDI2_PAIR3-
A51	GND (fixed)	B51	GND (fixed)	C51	GND (fixed)	D51	GND (fixed)
A52	~~PCIE_TX5+~~	B52	~~PCIE_RX5+~~	C52	~~PEG_RX0+~~	D52	~~PEG_TX0+~~
A53	~~PCIE_TX5-~~	B53	~~PCIE_RX5-~~	C53	~~PEG_RX0-~~	D53	~~PEG_TX0-~~
A54	GPI0	B54	GPO1	C54	TYPE0#	D54	~~PEG_LANE_RV#~~
A55	~~PCIE_TX4+ *~~	B55	~~PCIE_RX4+ *~~	C55	~~PEG_RX1+~~	D55	~~PEG_TX1+~~
A56	~~PCIE_TX4- *~~	B56	~~PCIE_RX4- *~~	C56	~~PEG_RX1-~~	D56	~~PEG_TX1-~~
A57	GND	B57	GPO2	C57	TYPE1#	D57	TYPE2#
A58	~~PCIE_TX3+ *~~	B58	~~PCIE_RX3+ *~~	C58	~~PEG_RX2+~~	D58	~~PEG_TX2+~~
A59	~~PCIE_TX3- *~~	B59	~~PCIE_RX3- *~~	C59	~~PEG_RX2-~~	D59	~~PEG_TX2-~~
A60	GND (fixed)	B60	GND (fixed)	C60	GND (fixed)	D60	GND (fixed)
A61	PCIE_TX2+	B61	PCIE_RX2+	C61	~~PEG_RX3+~~	D61	~~PEG_TX3+~~
A62	PCIE_TX2-	B62	PCIE_RX2-	C62	~~PEG_RX3-~~	D62	~~PEG_TX3-~~
A63	GPI1	B63	GPO3	C63	RSVD	D63	RSVD
A64	PCIE_TX1+	B64	PCIE_RX1+	C64	RSVD	D64	RSVD
A65	PCIE_TX1-	B65	PCIE_RX1-	C65	~~PEG_RX4+~~	D65	~~PEG_TX4+~~
A66	GND	B66	WAKE0#	C66	~~PEG_RX4-~~	D66	~~PEG_TX4-~~
A67	GPI2	B67	WAKE1#	C67	~~RAPID_SHUTDOWN~~	D67	GND
A68	PCIE_TX0+	B68	PCIE_RX0+	C68	~~PEG_RX5+~~	D68	~~PEG_TX5+~~
A69	PCIE_TX0-	B69	PCIE_RX0-	C69	~~PEG_RX5-~~	D69	~~PEG_TX5-~~
A70	GND (fixed)	B70	GND (fixed)	C70	GND (fixed)	D70	GND (fixed)
A71	LVDS_A0+	B71	LVDS_B0+	C71	~~PEG_RX6+~~	D71	~~PEG_TX6+~~
A72	LVDS_A0-	B72	LVDS_B0-	C72	~~PEG_RX6-~~	D72	~~PEG_TX6-~~
A73	LVDS_A1+	B73	LVDS_B1+	C73	GND	D73	GND
A74	LVDS_A1-	B74	LVDS_B1-	C74	~~PEG_RX7+~~	D74	~~PEG_TX7+~~
A75	LVDS_A2+	B75	LVDS_B2+	C75	~~PEG_RX7-~~	D75	~~PEG_TX7-~~
A76	LVDS_A2-	B76	LVDS_B2-	C76	GND	D76	GND
A77	LVDS_VDD_EN	B77	LVDS_B3+	C77	RSVD	D77	RSVD
A78	LVDS_A3+	B78	LVDS_B3-	C78	~~PEG_RX8+~~	D78	~~PEG_TX8+~~
A79	LVDS_A3-	B79	LVDS_BKLT_EN	C79	~~PEG_RX8-~~	D79	~~PEG_TX8-~~

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	Row A		Row B		Row C		Row D
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**
A80	GND (FIXED)	**B80**	GND (FIXED)	**C80**	GND (FIXED)	**D80**	GND (FIXED)
A81	LVDS_A_CK+	**B81**	LVDS_B_CK+	**C81**	~~PEG_RX9+~~	**D81**	~~PEG_TX9+~~
A82	LVDS_A_CK-	**B82**	LVDS_B_CK-	**C82**	~~PEG_RX9-~~	**D82**	~~PEG_TX9-~~
A83	LVDS_I2C_CK	**B83**	LVDS_BKLT_CTRL	**C83**	RSVD	**D83**	RSVD
A84	LVDS_I2C_DAT	**B84**	VCC_5V_SBY	**C84**	GND	**D84**	GND
A85	GPI3	**B85**	VCC_5V_SBY	**C85**	~~PEG_RX10+~~	**D85**	~~PEG_TX10+~~
A86	RSVD	**B86**	VCC_5V_SBY	**C86**	~~PEG_RX10-~~	**D86**	~~PEG_TX10-~~
A87	eDP_HPD	**B87**	VCC_5V_SBY	**C87**	GND	**D87**	GND
A88	PCIE0_CK_REF+	**B88**	BIOS_DIS1#	**C88**	~~PEG_RX11+~~	**D88**	~~PEG_TX11+~~
A89	PCIE0_CK_REF-	**B89**	~~VGA_RED~~*	**C89**	~~PEG_RX11-~~	**D89**	~~PEG_TX11-~~
A90	GND (fixed)	**B90**	GND (fixed)	**C90**	GND (fixed)	**D90**	GND (fixed)
A91	SPI_POWER	**B91**	~~VGA_GRN~~*	**C91**	~~PEG_RX12+~~	**D91**	~~PEG_TX12+~~
A92	SPI_MISO	**B92**	~~VGA_BLU~~*	**C92**	~~PEG_RX12-~~	**D92**	~~PEG_TX12-~~
A93	GPO0	**B93**	~~VGA_HSYNC~~*	**C93**	GND	**D93**	GND
A94	SPI_CLK	**B94**	~~VGA_VSYNC~~*	**C94**	~~PEG_RX13+~~	**D94**	~~PEG_TX13+~~
A95	SPI_MOSI	**B95**	~~VGA_I2C_CK~~*	**C95**	~~PEG_RX13-~~	**D95**	~~PEG_TX13-~~
A96	TPM_PP	**B96**	~~VGA_I2C_DAT~~*	**C96**	GND	**D96**	GND
A97	TYPE10#	**B97**	SPI_CS#	**C97**	RSVD	**D97**	RSVD
A98	SER0_TX	**B98**	RSVD	**C98**	~~PEG_RX14+~~	**D98**	~~PEG_TX14+~~
A99	SER0_RX	**B99**	RSVD	**C99**	~~PEG_RX14-~~	**D99**	~~PEG_TX14-~~
A100	GND (fixed)	**B100**	GND (fixed)	**C100**	GND (fixed)	**D100**	GND (fixed)
A101	SER1_TX	**B101**	FAN_PWMOUT	**C101**	~~PEG_RX15+~~	**D101**	~~PEG_TX15+~~
A102	SER1_RX	**B102**	FAN_TACHIN	**C102**	~~PEG_RX15-~~	**D102**	~~PEG_TX15-~~
A103	LID#	**B103**	SLEEP#	**C103**	GND	**D103**	GND
A104	VCC_12V	**B104**	VCC_12V	**C104**	VCC_12V	**D104**	VCC_12V
A105	VCC_12V	**B105**	VCC_12V	**C105**	VCC_12V	**D105**	VCC_12V
A106	VCC_12V	**B106**	VCC_12V	**C106**	VCC_12V	**D106**	VCC_12V
A107	VCC_12V	**B107**	VCC_12V	**C107**	VCC_12V	**D107**	VCC_12V
A108	VCC_12V	**B108**	VCC_12V	**C108**	VCC_12V	**D108**	VCC_12V
A109	VCC_12V	**B109**	VCC_12V	**C109**	VCC_12V	**D109**	VCC_12V
A110	GND (FIXED)	**B110**	GND (FIXED)	**C110**	GND (FIXED)	**D110**	GND (FIXED)

Notes:

- LID# and SLEEP# signals are not natively supported on the SoC. They instead connect to GPIO pins simulating their behaviour.
- *VGA is by build option, in place of DDI2
- eDP x4 lanes is by build option, in place of LVDS
- SD signal is muxed with GPIO, switching controlled by BIOS setting (see section 3.3.14)
- PCIe bridge IC is by build option to support 5 PCIe x1

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3.2. Signal Description Terminology

The following terms are used in the COM Express AB/CD Signal Descriptions below.

I	Input to the Module
O	Output from the Module
I/O	Bi-directional input/output signal
OD	Open drain output
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I/O 3.3Vsb	Input 3.3V tolerant active in standby state
P	Power Input/Output
REF	Reference voltage output that may be sourced from a module power plane.
PDS	Pull-down strap. This is an output pin on the module that is either tied to GND or not connected. The signal is used to indicate the PICMG module type to the Carrier Board.
PU	ADLINK implemented pull-up resistor on module
PD	ADLINK implemented pull-down resistor on module

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3.3. AB Signal Descriptions

3.3.1. Audio Signals

Signal	Pin	Description	I/O	PU/PD	Comment
HDA_RST#	A30	Reset output to CODEC, active low.	O 3.3V		
HDA_SYNC	A29	Sample-synchronization signal to the CODEC(s).	O 3.3V		
HDA_BITCLK	A32	Serial data clock generated by the external CODEC(s).	I/O 3.3V		
HDA_SDOUT	A33	Serial TDM data output to the CODEC.	O 3.3V		
HDA_SDIN[2:0]	B28 B30	Serial TDM data inputs from up to 3 CODECs.	I/O 3.3V	PD 680 ohm	Only supports HDA_SDIN0. PD 680 ohm, based on SoC vendor guidance.

3.3.2. Analog VGA (build option)

Signal	Pin	Description	I/O	PU/PD	Comment
VGA_RED	B89	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	VGA is by build option, in place of DDI 2
VGA_GRN	B91	Green for monitor Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3V		
VGA_VSYNC	B94	Vertical sync output to VGA monitor	O 3.3V		
VGA_I2C_CK	B95	DDC clock line (I²C port dedicated to identify VGA monitor capabilities)	I/O OD 3.3V	PU 2k2 3.3V	
VGA_I2C_DAT	B96	DDC data line.	I/O OD 3.3V	PU 2k2 3.3V	

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3.3.3. LVDS/eDP

LVDS

Signal	Pin	Description	I/O	PU/PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		LVDS is default. (through eDP to LVDS bridge) **Note:** eDP support available by build option
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS Channel A differential clock	O LVDS		
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	B71 B72 B73 B74 B75 B76 B77 B78	LVDS Channel B differential pairs	O LVDS		
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS Channel B differential clock	O LVDS		
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 10k	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V		
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V	PD 100k	ePD to LVDS requirement
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control.	O 3.3V	PU 2k2 3.3V	
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 2k2 3.3V	

eDP (build option)

Signal	Pin	Description	I/O	PU/PD	Comment
eDP_TX2+ eDP_TX2- eDP_TX1+ eDP_TX1- eDP_TX0+ eDP_TX0--	A71 A72 A73 A74 A75 A76	eDP differential pairs	O PCIE		AC coupled off module
eDP_TX3+ eDP_TX3--	A81 A82	eDP differential pairs	O PCIE		AC coupled off module
eDP_VDD_EN	A77	eDP power enable	O 3.3V	PD 10k	
eDP_BKLT_EN	B79	eDP backlight enable	O 3.3V		
eDP_BKLT_CTRL	B83	eDP backlight brightness control	O 3.3V	PD 100k	
eDP_AUX+	A83	eDP AUX+	I/O PCIE		AC coupled off module
eDP_AUX-	A84	eDP AUX-	I/O PCIE		AC coupled off module
eDP_HPD	A87	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100k	

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3.3.4. Gigabit Ethernet

Gigabit Ethernet	Pin	Description	I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A11 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: **1000 / 100 / 10** MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	I/O Analog		Twisted pair signals for external transformer.
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.	O 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.	O 3.3VSB		
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.	O 3.3VSB		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	O 3.3VSB		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 1 and 2 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be 250 mA or less.	GND min 3.3V max		Not supported (NC pin)
GBE0_SDP	A49	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1pps signal.			

3.3.5. SATA

Signal	Pin	Description	I/O	PU/PD	Comment
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		AC coupled on Module
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		AC coupled on Module
SATA2_TX+ SATA2_TX-	A22 A23	Serial ATA channel 2, Transmit Output differential pair.	O SATA		Not supported
SATA2_RX+ SATA2_RX-	A25 A26	Serial ATA channel 2, Receive Input differential pair.	I SATA		Not supported
SATA3_TX+ SATA3_TX-	B22 B23	Serial ATA channel 3, Transmit Output differential pair.	O SATA		Not supported
SATA3_RX+ SATA3_RX-	B25 B26	Serial ATA channel 3, Receive Input differential pair.	I SATA		Not supported
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	O 3.3V	PU 10k 3.3V	

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3.3.6. PCI Express

Signal	Pin	Description	I/O	PU/PD	Comment
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		AC coupled on module
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		AC coupled off module
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		AC coupled on module
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		AC coupled off module
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		AC coupled on module
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		AC coupled off module
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		AC coupled on module, PCIe port 3 is by build option
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		AC coupled on module, PCIe port 3 is by build option
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		AC coupled on module. PCIe port 4 is by build option, by PCIe bridge IC
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		AC coupled off module. PCIe port 4 is by build option, by PCIe bridge IC
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		AC coupled on module. PCIe port 5 is by build option, in place of GbE
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		AC coupled off module. PCIe port 5 is by build option, in place of GbE
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		

Note: PCIe bridge IC is by build option to support 5 PCIe x1.

3.3.7. LPC Bus

Signal	Pin	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V		
LPC_DRQ0# LPC_DRQ1#	B8 B9	LPC serial DMA request	I 3.3V		NC. Not supported by Apollo Lake
LPC_SERIRQ	A50	LPC serial interrupt	I/O 3.3V	PU 8k2 3.3V	
LPC_CLK	B10	LPC clock output –33MHz nominal	O 3.3V		The LPC_CLK frequency is 25MHz

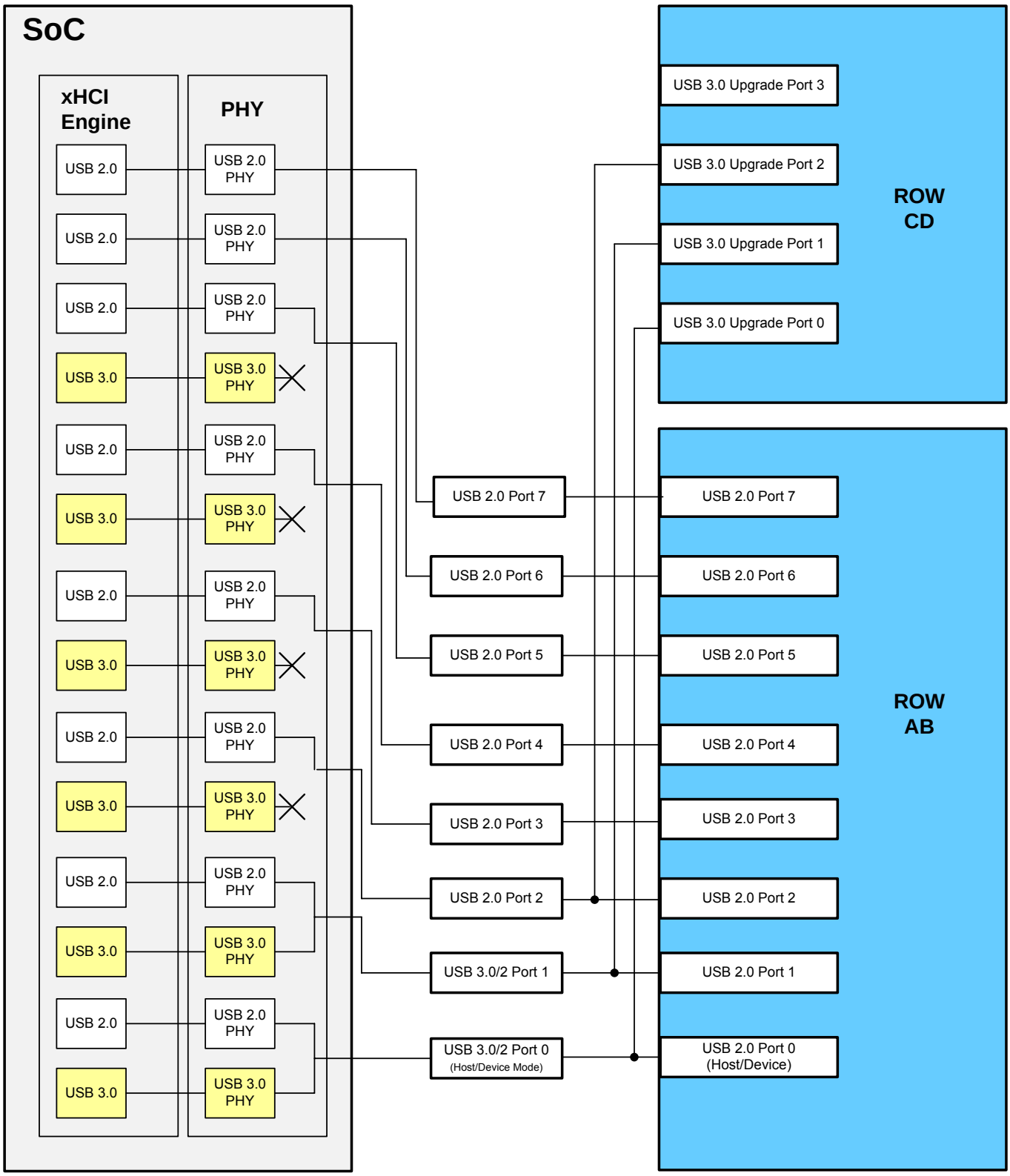
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3.3.8. USB

Signal	Pin	Description	I/O	PU/PD	Comment
USB0+ USB0-	A46 A45	USB differential data pairs for Port 0	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB1+ USB1-	B46 B45	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB2+ USB2-	A43 A42	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB3+ USB3-	B43 B42	USB differential data pairs for Port 2	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB4+ USB4-	A40 A39	USB differential data pairs for Port 3	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB5+ USB5-	B40 B39	USB differential data pairs for Port 4	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB6+ USB6-	A37 A36	USB differential data pairs for Port 5	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB7+ USB7-	B37 B37	USB differential data pairs for Port 6	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull high on carrier
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3VSB	PU 10k 3.3VSB	Do not pull high on carrier
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull high on carrier
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull high on carrier
USB0_HOST_PRSNT	B48	Module USB client may detect the presence of a USB host on USB0. A high value indicates that a host is present.	I/O 3.3VSB	PD 100k	OTG support depends on OS

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3.3.9. USB Root Segmentation



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3.3.10. SPI (BIOS only)

Signal	Pin	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3VSB	PU 10k 3.3VSB	Only supports CS0
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier	O P 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I	PU 10k 3.3VSB	Carrier shall pull to GND or leave not-connected.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I	PU 10k 3.3VSB	Carrier shall pull to GND or leave not-connected

3.3.11. Miscellaneous

Signal	Pin	Description	I/O	PU/PD	Comment
SPKR	B32	Output for audio enunciator, the “speaker” in PC-AT systems	O 3.3V	PU 10k 3.3V	
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V		
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3V		Recommend to add PU on carrier board
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3V		
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan’s RPM.	O OD 3.3V	PU 2.2k 3.3V	There shall be PD on carrier board
FAN_TACHIN	B102	Fan tachometer input for a fan with a two pulse output.	I OD 3.3V	PU 10k 3.3V	
TPM_PP	A96	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V		PD only when TPM on module
RAPID_SHUTDOWN	C67	Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for ≥ 20 µs.	I 5.0VSB		Not supported

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3.3.12. SMBus

Signal	Pin	Description	I/O	PU/PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line. Power sourced through 5V standby rail and main power rails.	I/O OD 3.3VSB	PU 8k2 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line. Power sourced through 5V standby rail and main power rails.	I/O OD 3.3VSB	PU 8k2 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 5V standby rail and main power rails.	I 3.3VSB	PU 10k 3.3VSB	

3.3.13. I2C Bus

Signal	Pin	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output/input	I/O OD 3.3VSB	PU 2k2 3.3VSB	Source SEMA BMC or Braswell SoC as alternative. (BMC by default)
I2C_DAT	B34	General purpose I²C port data I/O line	I/O OD 3.3VSB	PU 2k2 3.3VSB	Source SEMA BMC or Braswell SoC as alternative. (BMC by default)

3.3.14. General Purpose I/O (GPIO)

Signal	Pin	Description	I/O	PU/PD	Comment
GPO[0]	A93	General purpose output pins.	O 3.3V	PD 10k	After hardware RESET output low
GPO[1]	B54	General purpose output pins.	O 3.3V	PD 10k	After hardware RESET output low
GPO[2]	B57	General purpose output pins.	O 3.3V	PD 10k	After hardware RESET output low
GPO[3]	B63	General purpose output pins.	O 3.3V	PD 10k	After hardware RESET output low
GPI[0]	A54	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10k 3.3V	
GPI[1]	A63	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10k 3.3V	
GPI[2]	A67	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10k 3.3V	
GPI[3]	A85	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10k 3.3V	

Notes: GPO[0:3], PU 10k 3.3V is by build option for programming these pins to be GPI.
GPI[0:3], PD 10k is by build option for programming these pins to be GPO.
cExpress-AL supports an SD/GPIO muxed design, controlled by BIOS setting. See the table below for pin mapping.

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SD/GPIO Pin Mapping

GPIO Signal	SD Signal	Note
GPI0	SD_DATA0	Bidirectional signal
GPI1	SD_DATA1	Bidirectional signal
GPI2	SD_DATA2	Bidirectional signal
GPI3	SD_DATA3	Bidirectional signal
GPO0	SD_CLK	Output from COM Express, input to SD
GPO1	SD_CMD	Output from COM Express, input to SD
GPO2	SD_WP	Input to COM Express when used as SD_WP
GPO3	SD_CD#	Input to COM Express when used as SD_CD#

3.3.15. Serial Interface Signals

Signal	Pin	Description	I/O	PU/PD	Comment
SER0_TX	A98	General purpose serial port transmitter (TTL level output)	O CMOS	PU 1k 5V	Power rail tolerance 5V/12V There shall be PD on carrier board
SER0_RX	A99	General purpose serial port receiver (TTL level input)	I CMOS	PU 4.7k 5V	Power rail tolerance 5V/12V
SER1_TX	A101	General purpose serial port transmitter (TTL level output)	O CMOS	PU 1k 5V	Power rail tolerance 5V/12V There shall be PD on carrier board
SER1_RX	A102	General purpose serial port receiver (TTL level input)	I CMOS	PU 4.7k 5V	Power rail tolerance 5V/12V

3.3.16. Power And System Management

Signal	Pin	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge.	I 3.3VSB	PU 10k 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low request for module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.	I 3.3VSB	PU 10k 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3VSB		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow carrier based FPGAs or other configurable devices time to be programmed.	I 3.3V	PU 10k 3.3V	

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Signal	Pin	Description	I/O	PU/PD	Comment
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as “PS_ON”) may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB		
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		Not supported. connected to SUS_S4#
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 10k 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB		Not supported. Connected to WAKE0#
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I 3.3VSB	PU 10k 3.3VSB	
LID#	A103	LID button. Low active signal used by the ACPI operating system for a LID switch.	I OD 3.3VSB	PU 10k 3.3VSB*	Emulated on GPIO (BIOS)
SLEEP#	B103	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I OD 3.3VSB	PU 10k 3.3VSB*	Emulated on GPIO (BIOS)

***Note:** PU 47K 3.3VSB supported by project basis, Please contact your local representataive.

3.3.17. Power and Ground

Signal	Pin	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109	Primary power input: +12V nominal (wide range 5 ~ 20V). All available VCC_12V pins on the connector(s) shall be used.	P		4.75-20 V
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. See Section 7 “Electrical Specifications“ for allowable input range. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		5Vsb ±5%
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70 , A80, A90, A100, A110, B1, B11, B21,B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path.	P		

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3.4. CD Signal Descriptions

3.4.1. USB 3.0 extension

Signal	Pin	Description	I/O	PU/PD	Comment
USB_SSRX0- USB_SSRX0+	C3 C4	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB0	I PCIE		AC coupled off Module
USB_SSTX0- USB_SSTX0+	D3 D4	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB0	O PCIE		AC coupled on Module
USB_SSRX1- USB_SSRX1+	C6 C7	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB1	I PCIE		AC coupled off Module
USB_SSTX1- USB_SSTX1+	D6 D7	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB1	O PCIE		AC coupled on Module
USB_SSRX2- USB_SSRX2+	C9 C10	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB2	I PCIE		AC coupled off Module
USB_SSTX2- USB_SSTX2+	D9 D10	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB2	O PCIE		AC coupled on Module
USB_SSRX3- USB_SSRX3+	C12 C13	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB3	I PCIE		Not supported
USB_SSTX3- USB_SSTX3+	D12 D13	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB3	O PCIE		Not supported

3.4.2. PCI Express x1

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair.	I PCIE		Not supported

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3.4.3. DDI Channels

DDI 1

Signal	Pin	Description	I/O	PU/PD	Comment
DDI1_PAIR0+ DDI1_PAIR0- DDI1_PAIR1+ DDI1_PAIR1- DDI1_PAIR2+ DDI1_PAIR2- DDI1_PAIR3+ DDI1_PAIR3- DDI1_PAIR4+ DDI1_PAIR4- DDI1_PAIR5+ DDI1_PAIR5- DDI1_PAIR6+ DDI1_PAIR6-	D26 D27 D29 D30 D32 D33 D36 D37 C25 C26 C29 C30 C15 C16	Digital Display Interface1 differential pairs	O PCIE		Pair 4 to Pair 6 are NOT supported
DDI1_HPD	C24	Digital Display Interface Hot-Plug Detect	I PCIE	PD 100K	
DDI1_CTRLCLK_AUX+	D15	IF DDI1_DDC_AUX_SEL is floating	I/O PCIe	PD 100K	DP1_AUX+ AC coupled on Module
		IF DDI1_DDC_AUX_SEL pulled high	I/O OD 3.3V		HDMI1_CTRLCLK PU 10k 3.3V
DDI1_CTRLDATA_AUX-	D16	IF DDI1_DDC_AUX_SEL is floating	I/O PCIe	PU 100K 3.3V	DP1_AUX- AC coupled on Module
		IF DDI1_DDC_AUX_SEL pulled high	I/O OD 3.3V		HDMI1_CTRLDATA PU 10k 3.3V
DDI1_DDC_AUX_SEL	D34	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.	I/O OD 3.3V	PD 1M	

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DDI 2

Signal	Pin	Description	I/O	PU/PD	Comment
DDI2_PAIR0+ DDI2_PAIR0- DDI2_PAIR1+ DDI2_PAIR1- DDI2_PAIR2+ DDI2_PAIR2- DDI2_PAIR3+ DDI2_PAIR3-	D39 D40 D42 D43 D46 D47 D49 D50	Digital Display Interface2 differential pairs			
DDI2_HPD	D44			PD 100K	
DDI2_CTRLCLK_AUX+	C32	IF DDI2_DDC_AUX_SEL is floating	I/O PCIe	PD 100K	DP2_AUX+ AC coupled on Module
		IF DDI2_DDC_AUX_SEL pulled high	I/O OD 3.3V		HDMI2_CTRLCLK PU 10k 3.3V
DDI2_CTRLDATA_AUX-	C33	IF DDI2_DDC_AUX_SEL is floating	I/O PCIe	PU 100K 3.3V	DP2_AUX- AC coupled on Module
		IF DDI2_DDC_AUX_SEL pulled high	I/O OD 3.3V		HDMI2_CTRLDATA PU 10k 3.3V
DDI2_DDC_AUX_SEL	C34	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.		PD 1M	

DDI 3 (not supported on this product)

Signal	Pin	Description	I/O	PU/PD	Comment
DDI3_PAIR0+ DDI3_PAIR0- DDI3_PAIR1+ DDI3_PAIR1- DDI3_PAIR2+ DDI3_PAIR2- DDI3_PAIR3+ DDI3_PAIR3-	C39 C40 C42 C43 C46 C47 C49 C50	Digital Display Interface3 differential pairs			
DDI3_HPD	C44			PD 100K	
DDI3_CTRLCLK_AUX+	C36	IF DDI3_DDC_AUX_SEL is floating	I/O PCIe	PD 100K	DP3_AUX+; AC coupled on Module
		IF DDI3_DDC_AUX_SEL pulled high	I/O OD 3.3V		HDMI3_CTRLCLK; PU 10k 3.3V
DDI3_CTRLDATA_AUX-	C37	IF DDI3_DDC_AUX_SEL is floating	I/O PCIe	PU 100K 3.3V	DP3_AUX-; AC coupled on Module
		IF DDI3_DDC_AUX_SEL pulled high	I/O OD 3.3V		HDMI3_CTRLDATA; PU 10k 3.3V

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Signal	Pin	Description	I/O	PU/PD	Comment
DDI3_DDC_AUX_SEL	C38	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.		PD 1M	

3.4.4. DDI to DP/HDMI/SDVO Mapping

Pin	Pin Name	DP	HDMI \ DVI
D26	DDI1_PAIR0+	DP1_LANE0+	TMDS1_DATA2+
D27	DDI1_PAIR0-	DP1_LANE0-	TMDS1_DATA2-
D29	DDI1_PAIR1+	DP1_LANE1+	TMDS1_DATA1+
D30	DDI1_PAIR1-	DP1_LANE1-	TMDS1_DATA1-
D32	DDI1_PAIR2+	DP1_LANE2+	TMDS1_DATA0+
D33	DDI1_PAIR2-	DP1_LANE2-	TMDS1_DATA0-
D36	DDI1_PAIR3+	DP1_LANE3+	TMDS1_CLK+
D37	DDI1_PAIR3-	DP1_LANE3-	TMDS1_CLK-
C25	DDI1_PAIR4+		
C26	DDI1_PAIR4-		
C29	DDI1_PAIR5+		
C30	DDI1_PAIR5-		
C15	DDI1_PAIR6+		
C16	DDI1_PAIR6-		
C24	DDI1_HPD	DP1_HPD	HDMI1_HPD
D15	DDI1_CTRLCLK_AUX+	DP1_AUX+	HMDI1_CTRLCLK
D16	DDI1_CTRLDATA_AUX-	DP1_AUX-	HMDI1_CTRLDATA
D34	DDI1_DDC_AUX_SEL		
D39	DDI2_PAIR0+	DP2_LANE0+	TMDS2_DATA2+
D40	DDI2_PAIR0-	DP2_LANE0-	TMDS2_DATA2-
D42	DDI2_PAIR1+	DP2_LANE1+	TMDS2_DATA1+
D43	DDI2_PAIR1-	DP2_LANE1-	TMDS2_DATA1-
D46	DDI2_PAIR2+	DP2_LANE2+	TMDS2_DATA0+
D47	DDI2_PAIR2-	DP2_LANE2-	TMDS2_DATA0-
D49	DDI2_PAIR3+	DP2_LANE3+	TMDS2_CLK+
D50	DDI2_PAIR3-	DP2_LANE3-	TMDS2_CLK-
D44	DDI2_HPD	DP2_HPD	HDMI2_HPD
C32	DDI2_CTRLCLK_AUX+	DP2_AUX+	HDMI2_CTRLCLK
C33	DDI2_CTRLDATA_AUX-	DP2_AUX-	HDMI2_CTRLDATA
C34	DDI2_DDC_AUX_SEL		

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Pin	Pin Name	DP	HDMI \ DVI
C39	DDI3_PAIR0+	DP3_LANE0+	TMDS3_DATA2+
C40	DDI3_PAIR0-	DP3_LANE0-	TMDS3_DATA2-
C42	DDI3_PAIR1+	DP3_LANE1+	TMDS3_DATA1+
C43	DDI3_PAIR1-	DP3_LANE1-	TMDS3_DATA1-
C46	DDI3_PAIR2+	DP3_LANE2+	TMDS3_DATA0+
C47	DDI3_PAIR2-	DP3_LANE2-	TMDS3_DATA0-
C49	DDI3_PAIR3+	DP3_LANE3+	TMDS3_CLK+
C50	DDI3_PAIR3-	DP3_LANE3-	TMDS3_CLK-
C44	DDI3_HPD	DP3_HPD	HDMI3_HPD
C36	DDI3_CTRLCLK_AUX+	DP3_AUX+	HDMI3_CTRLCLK
C37	DDI3_CTRLDATA_AUX-	DP3_AUX-	HDMI3_CTRLDATA
C38	DDI3_DDC_AUX_SEL		

3.4.5. PCI Express Graphics x16 (not supported)

Signal	Pin	Description	I/O	PU/PD	Comment
PEG_RX0+ PEG_RX0- PEG_RX1+ PEG_RX1- PEG_RX2+ PEG_RX2- PEG_RX3+ PEG_RX3- PEG_RX4+ PEG_RX4- PEG_RX5+ PEG_RX5- PEG_RX6+ PEG_RX6- PEG_RX7+ PEG_RX7- PEG_RX8+ PEG_RX8- PEG_RX9+ PEG_RX9- PEG_RX10+ PEG_RX10- PEG_RX11+ PEG_RX11- PEG_RX12+ PEG_RX12- PEG_RX13+ PEG_RX13- PEG_RX14+ PEG_RX14- PEG_RX15+ PEG_RX15	C52 C53 C55 C56 C58 C59 C61 C62 C65 C66 C68 C69 C71 C72 C74 C75 C78 C79 C81 C82 C85 C86 C88 C89 C91 C92 C94 C95 C98 C99 C101 C102	PCI Express Graphics transmit differential pairs.	I PCIE		Not supported
PEG_TX0+ PEG_TX0- PEG_TX1+ PEG_TX1- PEG_TX2+ PEG_TX2- PEG_TX3+	D52 D53 D55 D56 D58 D57 D61	PCI Express Graphics receive differential pairs.	O PCIE		Not supported

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Signal	Pin	Description	I/O	PU/PD	Comment
PEG_TX3- PEG_TX4+ PEG_TX4- PEG_TX5+ PEG_TX5- PEG_TX6+ PEG_TX6- PEG_TX7+ PEG_TX7- PEG_TX8+ PEG_TX8- PEG_TX9+ PEG_TX9- PEG_TX10+ PEG_TX10- PEG_TX11+ PEG_TX11- PEG_TX12+ PEG_TX12- PEG_TX13+ PEG_TX13- PEG_TX14+ PEG_TX14- PEG_TX15+ PEG_TX15-	D62 D65 D66 D68 D69 D71 D72 D74 D75 D78 D79 D81 D82 D85 D86 D88 D89 D91 D92 D94 D95 D98 D99 D101 D102				
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the Carrier board to reverse lane order.	I 1.05V		Not supported

3.4.6. Module Type Definition

Signal	Pin #	Description	I/O	Comment
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pinout Type 1, these pins are don't care (X). TYPE2# TYPE1# TYPE0# X X X Pinout Type 1 NC NC NC Pinout Type 2 NC NC GND Pinout Type 3 (no IDE) NC GND NC Pinout Type 4 (no PCI) NC GND GND Pinout Type 5 (no IDE, no PCI) GND NC NC Pinout Type 6 (no IDE, no PCI) The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.		Type 6

3.4.7. Power and Ground

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	C104-C109 D104-D109	Primary power input: +12V nominal (wide range 5 ~ 20V). All available VCC_12V pins on the connector(s) shall be used	P		4.75 - 20V

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Signal	Pin #	Description	I/O	PU/PD	Comment
GND	C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70, C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane.	P		

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4. Module Interfaces

This chapter describes connectors and pinouts, LEDs and switches that are used on the module but are not included in the PICMG standard specification

4.1. Connector, Switch and LED Locations

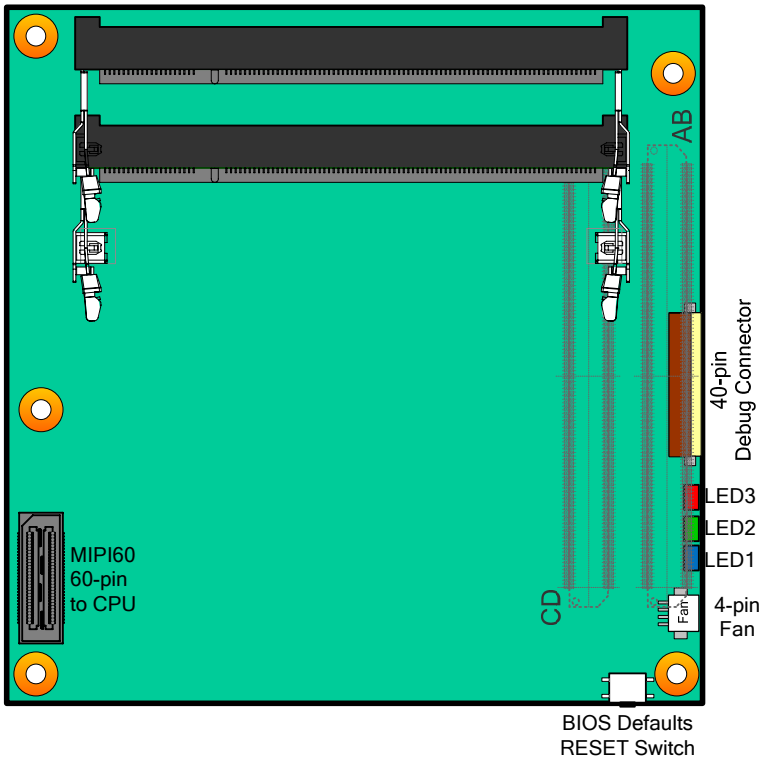


Figure 3: cExpress-AL Connector, Switch and LED Locations

cExpress-AL and the DB40 Debug Module

For illustration purposes only

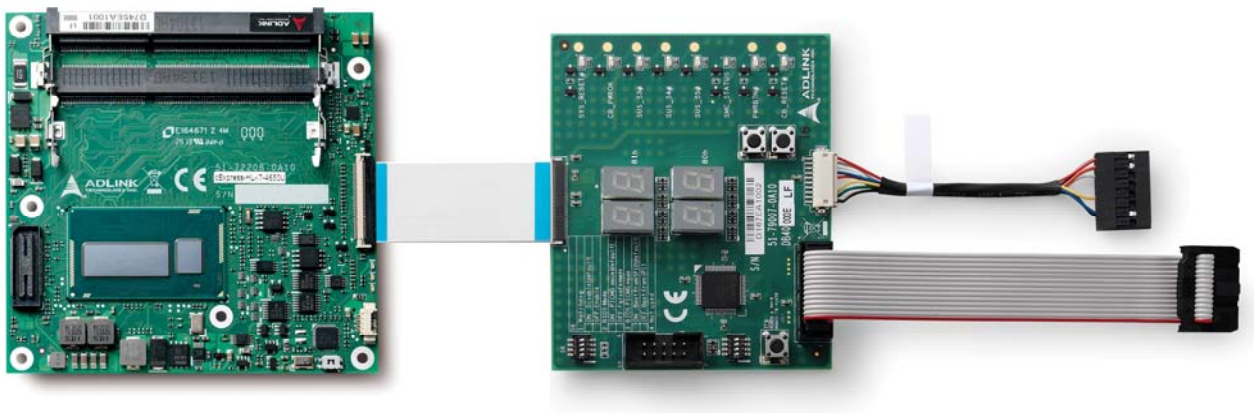


Figure 4: cExpress-AL and the DB40 Debug Module

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4.2. 40-pin Debug Connector

FPC Connector Type: FCI 59GF Flex 10042867

Pin Orientation



1 40

40-pin Debug Connector Pin Definition on the COM Express Module

Pin	Interface	Signal	Remark
1	SPI Program interface	VCC_SPI_IN	SPI Power Input from flash tool to module. HW need add MOS FET to switch SPI power for SPI ROM
2		GND	
3		SPI_BIOS_CS0#	
4		SPI_BIOS_CS1#	
5		SPI_BIOS_MISO	
6		SPI_BIOS_MOSI	
7		SPI_BIOS_CLK	
8	LPC Bus	3V3_LPC	System power 3.3V provide from COM module
9		GND	
10		BIOS_DIS0	
11		RST#	
12		CLK33_LPC	
13		LPC_FRAME#	
14		LPC_AD3	
15		LPC_AD2	
16		LPC_AD1	always power 3.3V provide from COM module
17		LPC_AD0	
18	BMC Program interface	3.3V_BMC	always power 3.3V provide from COM module
19		3.3V_BMC	always power 3.3V provide from COM module
20		GND	

Pin	Interface	Signal	Remark
21	BMC Program interface (cont'd)	TXD6	
22		RXD6	
23		FUMD0	
24		RESET_IN#	
25		DATA	
26		CLK	
27		OCD0A	Include a jumper to connect OCD0A via 1K0 pull-up to 3.3V_BMC
28		OCD0B	Include a jumper to connect OCD0A via 1K0 pull-up to 3.3V_BMC
29	Test points	PWRBTN#	
30		SYS_RESET#	
31		CB_RESET#	
32		CB_PWROK	
33		SUS_S3#	
34		SUS_S4#	
35		SUS_S5#	
36	BMC Debug signals	POSTWDT_DIS#	Connect to Jumper for Debug
37		SEL_BIOS	Connect to Jumper for Debug
38		BIOS_MODE	Connect to Jumper for Debug
39		BMC_STATUS	
40	Reserved		

Table 2: 40-pin Debug Connector Pin Definition

Note: The pin definition on the debug module is the inverse of that on the COM Express module.

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4.3. Status LEDs

To facilitate easier maintenance, status LED's are mounted on the board.



LED1 LED2 LED3

LED Descriptions

Name	Color	Connection	Function
LED1	Blue	BMC output	Power Sequence Status Code (BMC) Power Changes, RESET (see 5.1.4 Exception Codes)
LED2	Green	Power Source 3Vcc	S0 LED ON S3/S4/S5 LED OFF ECO mode LED OFF
LED3	Red	BMC output and same signal as WDT (B27) on BtB connector	Module power up WD LED = LED OFF Watchdog counting WD LED = Keep Last State Watchdog timed out WD LED = LED ON Watchdog RESET WD LED = LED ON Rebooted after WD RESET WD LED = LED ON Rebooted after PWRBTN WD LED = LED OFF Rebooted after RESET BTN WD LED = LED OFF

Table 3: cExpress-AL LED Descriptions

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4.4. MIPI60 Debug Header (build option)

Not all pins of the Intel® MIPI60 connector are connected to the CombiProbe Intel x86/x64 MIPI60-C.

Pin	Signal	Pin	XDP Signal
1	VREF_DEBUG	2	TMS
3	TCK0	4	TDO
5	TDI	6	Open Drain Reset Out
7	Reset In	8	No Connect
9	TRST_N	10	PREQ_N
11	PRDY_N	12	VREF_TRACE
13	PTI_0_CLK	14	PTI_1_CLK
15	GND	16	GND
17	No Connect	18	PTI_1_DATA[0]
19	PTI_0_DATA[0]	20	PTI_1_DATA[1]
21	PTI_0_DATA[1]	22	PTI_1_DATA[2]
23	PTI_0_DATA[2]	24	PTI_1_DATA[3]
25	PTI_0_DATA[3]	26	No Connect
27	PTI_0_DATA[4]	28	No Connect
29	PTI_0_DATA[5]	30	No Connect
31	PTI_0_DATA[6]	32	No Connect
33	PTI_0_DATA[7]	34	Reset Out
35	No Connect	36	Boot Stall
37	No Connect	38	CPU Boot Stall
39	No Connect	40	Power Button
41	No Connect	42	PWRGOOD
43	No Connect	44	No Connect
45	No Connect	46	No Connect
47	No Connect	48	I2C_SCL
49	No Connect	50	I2C_SDA
51	No Connect	52	No Connect
53	No Connect	54	DBG_UART_TX
55	No Connect	56	DBG_UART_RX
57	GND	58	GND
59	No Connect	60	No Connect

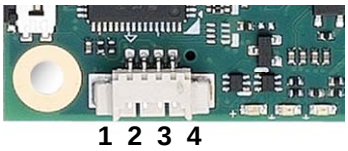
Table 4: MIPI60 Debug Header Pin Definition

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4.5. Fan Connector

Connector Type: JVE 24W1125A-04M00

Pin Orientation



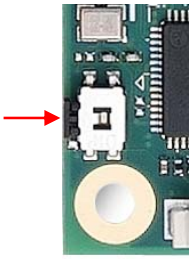
Pin Assignment

Name	Signal
1	FAN_PWMOUT
2	FAN_TACHIN
3	Ground
4	5V

Table 5: Fan Connector Pin Definition

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4.6. BIOS Setup Defaults Reset Button



To perform a hardware reset of BIOS default settings, perform the following steps:

1. Shut down the system.
2. Press the BIOS Setup Defaults RESET Button continuously and boot up the system. You can release the button when the BIOS prompt screen appears
3. The BIOS prompt screen will display a confirmation that BIOS defaults have been reset and request that you reboot the system.



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4.7. Switch Settings

Switch Locations

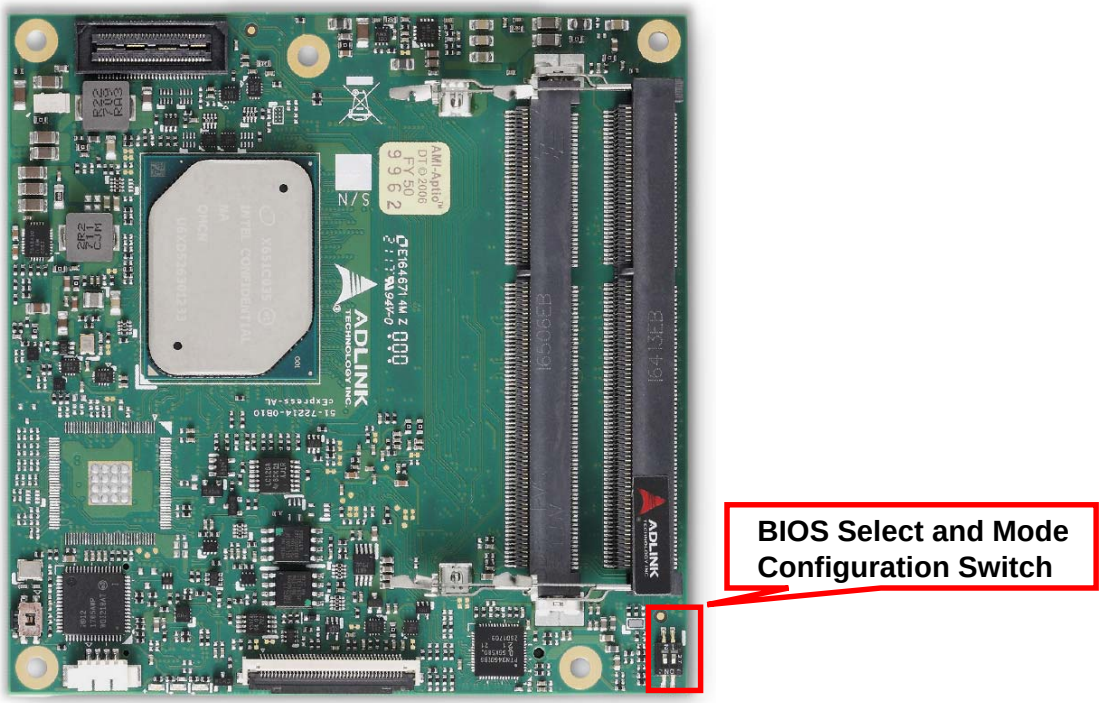


Figure 5: cExpress-AL Switch Locations

BIOS Select and Mode Configuration Switch

The module has two BIOS chips and BIOS operation can be configured to "PICMG" or dual-BIOS "Failsafe" modes using the BIOS Select and Mode Configuration Switch, Pin 2.

Setting the module to PICMG mode will configure the BIOS chips on the module as SPI0 and SPI1. In PICMG mode, a BIOS chip cannot be placed in the SPI0 slot on the carrier.

In dual-BIOS Failsafe mode, both BIOS chips on the module are configured as SPI1. Only one of the two is connected to the SPI bus at any given time. In case of failure of the primary SPI1 BIOS, the system will reboot and switch to the secondary SPI1 BIOS on the module. In Failsafe mode, the SPI0 BIOS socket on the carrier can be populated.

In either mode, BIOS Select and Mode Configuration Switch, Pin 1 is used to select whether to boot from SPI0 or SPI1.

Mode	Pin 1	Pin 2
Boot from SPI0 (default)	On	—
Boot from SPI1	Off	—
Set BIOS to PICMG mode	—	On
Set BIOS to Failsafe BIOS mode (default)	—	Off

Table 6: BIOS Select and Mode Configuration Switch Settings

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5. Smart Embedded Management Agent (SEMA)

The onboard microcontroller (BMC) implements power sequencing and Smart Embedded Management Agent (SEMA) functionality. The microcontroller communicates via the System Management Bus with the CPU/chipset. The following functions are implemented:

- Total operating hours counter. Counts the number of hours the module has been run in minutes.
- On-time minutes counter. Counts the seconds since last system start.
- Temperature monitoring of CPU and board temperature. Minimum and maximum temperature values of CPU and board are stored in flash.
- Power cycles counter
- Boot counter. Counts the number of boot attempts.
- Watchdog Timer. Set/Reset/Disable Watchdog Timer. Features auto-reload at power-up.
- System Restart Cause. Power loss/BIOS Fail/Watchdog/Internal Reset/External Reset
- Fail-safe BIOS support. In case of a boot failure, hardware signals tells external logic to boot from fail-safe BIOS.
- Flash area. 1kB Flash area for customer data
- 2K Bytes Protected Flash area. Keys, IDs, etc. can be stored in a write- and clear-protectable region.
- Board Identify. Vendor/Board/Serial number/Production Date
- Main-current & voltage. Monitors drawn current and main voltages

For a detailed description of SEMA features and functionality, please refer to **SEMA Technical Manual** and **SEMA Software Manual**, downloadable at: **http://www.adlinktech.com/sema/**.

Note: Due to limitations of the Intel “Apollo Lake” platform, SEMA can only obtain CPU temperature readings when the OS is running.

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5.1. Board Specific SEMA Functions

5.1.1. Voltages

The BMC of the cExpress-AL implements a voltage monitor and samples several onboard voltages. The voltages can be read by calling the SEMA function “Get Voltages”. The function returns a 16-bit value divided into high-byte (MSB) and low-byte (LSB).

ADC Channel	Voltage Name	Voltage Formula [V]
0	VCC_CORE	(MSB<<8 + LSB) x 3.3 / 1024
1	VGFX	(MSB<<8 + LSB) x 3.3 / 1024
2	VMEM	(MSB<<8 + LSB) x 3.3 / 1024
3	5VSB	(MSB<<8 + LSB) x 1.8 x 3.3 / 1024
4	VIN (12V)	(MSB<<8 + LSB) x 6 x 3.3 / 1024
5	5V	(MSB<<8 + LSB) x 1.8 x 3.3 / 1024
6	3.3V	(MSB<<8 + LSB) x 1.1 x 3.3 / 1024
7	3.3VSB	(MSB<<8 + LSB) x 1.1 x 3.3 / 1024
8	RTC (build option support)	(MSB<<8 + LSB) x 3.3 / 1024

Table 7: SEMA Onboard Voltage Monitor

5.1.2. Main Current

The BMC of the cExpress-AL implements a current monitor. The current can be read by calling the SEMA function “Get Main Current”. The function returns four 16-bit values divided in high-byte (MSB) and low-byte (LSB). These 4 values represent the last 4 currents drawn by the board. The values are sampled every 250ms. The order of the 4 values is NOT in chronological order. Access by the BMC may increase the drawn current of the whole system. In this case, there are still 3 samples not influenced by the read access.

Main Current = (MSB_n<<8 + LSB_n) x 8.06mA

5.1.3. BMC Status

This register shows the status of BMC controlled signals on the cExpress-AL.

Status Bit	Signal
0	WDT_OUT
1	LVDS_VDDEN
2	LVDS_BKLTEN
3	BIOS_MODE
4	POSTWDT_DISn
5	SEL_BIOS
6	BIOS_DIS0n
7	BIOS_DIS1n

Table 8: SEMA BMC Status

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5.1.4. Exception Codes

In case of an error, the BMC drives a blinking code on the blue Status LED (LED1). The same error code is also reported by the BMC Flags register. The Exception Code is not stored in the Flash Storage and is cleared when the power is removed. Therefore, a “Clear Exception Code” command is not needed or supported.

Exception Code	Error Message
0	NOERROR
2	NO_SUSCLK
3	NO_SLP_S4_S5
4	NO_SLP_S3
5	BIOS_FAIL
6	RESET_FAIL
7	RESETIN_FAIL
8	NO_CB_PWRGD
9	CRITICAL_TEMP
10	POWER_FAIL
11	VOLTAGE_FAIL
12	NO_3V3_5V_A_PG
13	NO_VNN_PG
14	NO_1V24_A_PG
15	NO_VDDQ_PG
16	NO_V1P05S_PG
17	NO_SYS_GD
18	NO_V12
19	MEMORY_ERROR
20	NO_P3V3_A_READY

Table 9: SEMA Exception Codes

5.1.5. BMC Flags

The BMC Flags register returns the last detected Exception Code since power-up and shows the BIOS in use and the power mode.

Bit	Description
[0 ~ 4]	Exception Code
[6]	0 = AT mode 1 = ATX mode
[7]	0 = Standard BIOS 1 = Fail-safe BIOS.

Table 10: SEMA BMC Flags

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6. System Resources

6.1. System Memory Map

Address Range (hex)	Description
FF00_0000 – FFFF_FFFF	IFAW (BIOS)
FED0_0000 – FEDF_33FF	HPET
FEC0_0000 – FECF_FFFF	IOAPIC
0K –1MB	DOS DRAM

6.2. I/O Map

I/O Address	IOSF Primary Target	IOSF SB Target
000h–01Fh	P2SB	Terminate
020h–021h	P2SB	ITSS (interrupt)
024h–025h	P2SB	ITSS (interrupt)
028h–029h	P2SB	ITSS (interrupt)
02Ch–02Dh	P2SB	ITSS (interrupt)
02Eh–02Fh	P2SB	LPC/eSPI
030h–031h	P2SB	ITSS (interrupt)
034h–035h	P2SB	ITSS (interrupt)
038h–039h	P2SB	ITSS (interrupt)
03Ch–03Dh	P2SB	ITSS (interrupt)
040h	P2SB	ITSS (Timer 0 Register)
041h	P2SB	Terminate
042h	P2SB	ITSS (Timer 2 Register)
043h	P2SB	ITSS (Timer Control Word Register)
04Eh–04Fh	LPC/eSPI	LPC/eSPI
050h	P2SB	ITSS (alias of 040h)
051h	P2SB	Terminate
052h	P2SB	ITSS (alias of 042h)
053h	P2SB	ITSS (alias of 043h)
060h	P2SB	LPC/eSPI
061h	P2SB	ITSS (CPU I/F)
062h	P2SB	LPC/eSPI
063h	P2SB	ITSS (CPU I/F)
064h	P2SB	LPC/eSPI

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I/O Address	IOSF Primary Target	IOSF SB Target
065h	P2SB	ITSS (CPU I/F)
066h	P2SB	LPC/eSPI
067h	P2SB	ITSS (CPU I/F)
070h	P2SB	ITSS (CPU I/F), RTC, PMC
071h	P2SB	RTC, PMC
072h–073h	P2SB	RTC, PMC
073h	P2SB	RTC, PMC
074h	P2SB	RTC, PMC
075h	P2SB	RTC, PMC
076h–077h	P2SB	RTC, PMC
080h	P2SB	LPC/eSPI or PMC
081h–083h	P2SB	Terminate
084h–086h	P2SB	LPC/eSPI or PMC
087h	P2SB	Terminate
088h	P2SB	LPC/eSPI or PMC
089h–08Bh	P2SB	Terminate
08Ch–08Eh	P2SB	LPC/eSPI or PMC
08Fh	P2SB	Terminate
090h	P2SB	LPC/eSPI
091h	P2SB	Terminate
092h	P2SB	ITSS (CPU I/F)
093h	P2SB	Terminate
094h–096h	P2SB	LPC/eSPI or PMC
097h	P2SB	Terminate
098h	P2SB	LPC/eSPI or PMC
099h–09Bh	P2SB	Terminate
09Ch–09Eh	P2SB	LPC/eSPI or PMC
09Fh	P2SB	Terminate
0A0h–0A1h	P2SB	ITSS (interrupt)
0A4h–0A5h	P2SB	ITSS (interrupt)
0A8h–0A9h	P2SB	ITSS (interrupt)
0ACh–0ADh	P2SB	ITSS (interrupt)
0B0h–0B1h	P2SB	ITSS (interrupt)
0B2h–0B3h	P2SB	PMC
0B4h–0B5h	P2SB	ITSS (interrupt)
0B8h–0B9h	P2SB	ITSS (interrupt)
0BCh–0BDh	P2SB	ITSS (interrupt)

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I/O Address	IOSF Primary Target	IOSF SB Target
0C0h–0DFh	P2SB	Terminate
0F0h	P2SB	Terminate
170h–177h	P2SB	Terminate
2F8h–2FFh	P2SB	Serial Port
240h–24Fh	P2SB	Serial Port
2F8h–2FFh	P2SB	Serial Port
376h	P2SB	Terminate
3F6h	P2SB	Terminate
3F8h–3FFh	P2SB	Serial Port
4D0h–4D1h	P2SB	ITSS (interrupt)
CF9h	P2SB	ITSS (CPU I/F)

6.3. Interrupt Request (IRQ) Lines

APIC Mode

The following table describes the APIC interrupt mapping. InThe Apollo Lake platform has 120 IRQs in total.

IO APIC Pin	Routing
0	8259 Apollo Lake
1	PS2 Keyboard
2	8254 Counter 0, HPET #0 (legacy mode)
3	Serial Port 3
4	Serial Port 4
5	NA
6	NA
7	NA
8	RTC, HPET #1 (legacy mode)
9	Option for configurable sources including internal ACPI/PCI devices, SCI and TCO
10	Serial Port 1
11	Serial Port 2
12	PS2 Mouse
13	xDCI
14	Option for configurable sources including GPIO, internal ACPI/PCI devices
15	Option for configurable sources including internal ACPI/PCI devices
16	Option for configurable sources including internal PIRQA, internal ACPI/PCI devices
17	PIRQB (xHCI)
18	Option for configurable sources including internal PIRQC, internal ACPI/PCI devices

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IO APIC Pin	Routing
19	Option for configurable sources including internal PIRQD, internal ACPI/PCI devices
20	Option for configurable sources including internal PIRQE, SCI, TCO, internal ACPI/PCI devices and HPET
21	Option for configurable sources including internal PIRQF, SCI, TCO, internal ACPI/PCI devices and HPET
22	Option for configurable sources including internal PIRQG, SCI, TCO, internal ACPI/PCI devices and HPET
23	Option for configurable sources including internal PIRQH, SCI, TCO, internal ACPI/PCI devices and HPET
24	Punit (DPTF)
25	Audio
26	ISH
27	I2C 0
28	I2C 1
29	I2C 2
30	I2C 3
31	I2C 4
32	I2C 5
33	I2C 6
34	I2C 7
35	SPI 0
36	SPI 1
37	SPI 2
38	UFS
39	EMMC
40	PMC IPC
41	PMC PMIC
42	SDIO
43	reserved
44	reserved
45	reserved
46	reserved
47	reserved
48	reserved
49	reserved
50 - 119	GPIO (Not for end user)

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6.4. PCI Configuration Space Map

Logical Function	Bus	Device	Function
Host Bridge	0	0	0
DPTF (Camarillo)	0	0	1
NPK	0	0	2
NPK (PSF ghost)	0	0	5
GMM	0	0	3
Gen	0	2	0
Iunit	0	3	0
Reserved (CSE)		7	0
P2SB	0	13	0
PMC	0	13	1
SPI	0	13	2
Shared SRAM	0	13	3
Audio	0	14	0
CSE-HECI1	0	15	0
CSE-HECI2	0	15	1
CSE-HECI3	0	15	2
CSE-fTPM (PSF ghost)	0	15	7
CSE-HOFFL	0	16	0
ISH	0	17	0
SATA	0	18	0
PCIe-A 1	0	19	0
PCIe-A 2	0	19	1
PCIe-A 3	0	19	2
PCIe-B 1 (multplexed with USB 3.0 port)	0	19	3
PCIe-B 2 (connect to onboard LAN)	0	20	0
PCIe-A 1	0	20	1
USB-Host (xHCI)	0	21	0
USB-Device (xDCI)	0	21	1
I2C 0	0	22	0
I2C 1	0	22	1
I2C 2	0	22	2
I2C 3	0	22	3
CSE I2C 6/7 access	0	22	6
CSE SSRAM access	0	22	7
I2C 4	0	23	0

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Logical Function	Bus	Device	Function
I2C 5	0	23	1
I2C 6	0	23	2
I2C 7	0	23	3
UART 0	0	24	0
UART 1	0	24	1
UART 2	0	24	2
UART 3	0	24	3
SPI 0	0	25	0
SPI 1	0	25	1
SPI 2	0	25	2
PWM	0	26	0
SD Card	0	27	0
eMMC	0	28	0
UFS	0	29	0
SDIO	0	30	0
LPC	0	31	0
SMBUS	0	31	1

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6.5. PCI Interrupt Routing Map

INT Line	PCIE port1	PCIE port 2	PCIE port 3	PCIE port 4	PCIE Port 5	PCIE Onboard LAN i210	Mobile IGFX	PUNIT Device
Int0	INTA:22	INTB:23	INTC:22	INTD:23	INTA:20	INTB:21	NTD:19	
Int1	INTB:23	INTC:20	INTD:23	INTA:20	INTB:21	INTC:22		INTF:24
Int2	INTC:20	INTD:21	INTA:20	INTB:21	INTC:22	INTD:23		
Int3	INTD:21	INTA:22	INTB:21	INTC:22	INTD:23	INTA:20		

INT Line	SMBus Controller	NPK Device	IUNT	PMC	HD Audio	CES	ISH	SATA Controller	XHCI	XDCI
Int0		INTA:16	INTF:21	INTA:40	INTA:25	INTE:20	INTE:26	INTA:19	INTB:17	
Int1	INTE:20									INTC:13
Int2										
Int3										

INT Line	I2C0	I2C1	I2C2	I2C3	I2C4	I2C5	I2C6	I2C7	SPI1
Int0	INTA:27				INTF:31				INTA:35
Int1		INTB:28				INTB:32			
Int2			INTC:29				INTC:33		
Int3				INTD:30				INTD:34	

INT Line	SPI3	SPI3	SD Host #0	SD Host #1	SD Host #2	SD Host #3
Int0			INTC:15	INTD:39	INTH:38	INTB:37
Int1	INTB:36					
Int2		INTC:37				
Int3						

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6.6. SMBus Address Table

Device	Address
DIMMA	A0h
DIMMB	A4h
BMC	50h
Extend GPIO	40h
I210	49h
USB2514BI	58h
LM73	92h
PEX8605	B7h,C1h
NXP(eDP to LVDS transmitter)	C0h

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7. BIOS Setup

7.1. Menu Structure

This section presents the six primary menus of the BIOS Setup Utility. Use the following table as a quick reference for the contents of the BIOS Setup Utility. The subsections in this section describe the submenus and setting options for each menu item. The default setting options are presented in **bold**, and the function of each setting is described in the right hand column of the respective table.

Main	Advanced	Chipset	Security	Boot	Save & Exit
BIOS Information System Information Board Information System Date and Time Access Level	CPU Configuration Graphics Configuration Power Management System Management Thermal Management Watchdog Timer CSM Configuration Super IO Configuration Serial Console Redirection USB Network Miscellaneous Driver Health Trusted Computing AMI Graphic Output Protocol Policy SDIO Configuration	North Bridge South Bridge Uncoe Configuration South Cluster Configuration	Setup Administrator Password User Password Secure Boot	Boot Configuration FIXED BOOT ORDER Priorities UEFI USB Key Drive BBS Priorities	Save Change and Exit Discard Changes and Exit Save Changes and Reset Discard Changes and Reset Save Options Boot Override

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7.2. Main

7.2.1. Main > BIOS Information

Feature	Options	Description
BIOS Vender	Info only	American Megatrends
BIOS Version	Info only	ADLINK BIOS version
Build Date	Info only	ADLINK BIOS Build Date
MRC Version	Info only	Display MRC Version
GOP Version	Info only	Display GOP Version
TXE FW Version	Info only	Display TXE FW Version
BIOS Boot Source	Info only	Display BIOS Boot Source

7.2.2. Main > System Information

Feature	Options	Description
Project Name	Info only	Display Project Name.
CPU Board version	Info only	Display CPU Board Version.
CPU Board String	Info only	Display CPU Board String.
CPU Frequency	Info only	Display CPU Frequency.
Total Memory	Info only	Display Installed Memory Size.
Memory Frequency	Info only	Display Memory Frequency.
SOC SKU	Info only	Display SOC SKU Version

7.2.3. Main > Board Information

Feature	Options	Description
Board Information	Submenu	
Board Information	Info only	
Serial Number	Info only	Display SEMA serial Number.
Manufacturing Date	Info only	Display SEMA manufacturing date.
Last Repair Date	Info only	Display SEMA last repair date.
MAC ID	Info only	Display SEMA MAC ID.
Runtime Statistics	Info only	
Total Runtime	Info only	The returned value specifies the total time in minutes the system is running in S0 state.
Current Runtime	Info only	The returned value specifies the time in seconds the system is running in S0 state. This counter is cleared when the system is removed from the external power supply.
Power Cycles	Info only	The returned value specifies the number of times the external power supply has been shut down

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Feature	Options	Description
Boot Cycles	Info only	The Boot counter is increased after a HW- or SW-Reset or after a successful power-up.
Boot Reason	Info only	The boot reason is the event which causes the reboot of the system.

7.2.4. Main >System Date/Time

Feature	Options	Description
System Date	Info only	
System Time	Info only	

7.2.5. Main >Access Level

Feature	Options	Description
Access Level	Info only	

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7.3. Advanced

This menu contains the settings for most of the user interfaces in the system.

7.3.1. Advanced > CPU Configuration

Feature	Options	Description
CPU Configuration	Info only	
Socket 0 CPU Information	Submenu	Socket Specific CPU Information.
Stocket 0 CPU information	Info only	
CPU Signature	Info only	Display CPU Signature.
Microcode Patch	Info only	Display Microcode Patch.
Max CPU Speed	Info only	Display Max CPU speed.
Min CPU speed	Info only	Display Min CPU speed.
Processor Cores	Info only	Display Processor Cores.
Intel HT Technology	Info only	Display Intel HT Technology support or not.
Intel VT-x Technology	Info only	Display Intel VT-x Technology support or not.
L1 Data Cache	Info only	Display cache info.
L1 Code Cache	Info only	Display cache info.
L2 Cache	Info only	Display cache info.
L3 Cache	Inf o only	Display cache info.
Speed	Info only	Display CPU Speed.
64-bit	Info only	Display 64-bit Support.
CPU Power Management	Submenu	CPU Power Management options.
CPU Power Management Configuration	Info only	
EIST	Disabled **Enabled**	Enable / Disable Intel SpeedStep
Burst Mode	Disabled **Enabled**	Enable / Disable Burst mode.
Boot performance mode	**Max Performance** Max Battery	Select the performance state that the BIOS will set before OS handoff.
C-States	Disabled **Enabled**	Enable / Disable C Sates.
Enhanced C-states	Disabled **Enabled**	Enable / Disable C1E. When enabled, CPU will switch to minimum speed when all core enter C-States.
Max Package C State	**PC2** PC1 C0	Controls the Max Package C State that the processor will support.
Max Core C State	**Fused value** Core C10	This option controls the Max Core C State that cores will Support.

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Feature	Options	Description
	Core C9 Core C8 Core C7 Core C6 Core C1 Unlimited	
C-State Auto Demotion	Disabled **C1**	Configure C-State Auto Demotion
C-State Un-demotion	Disabled **C1**	Configure C-State Auto Un-demotion
Power Limit 1 Enable	Disabled **Enabled**	Enable / Disable Power Limit 1
Power Limit 1	Info Only	Display Power Limit 1 Power Watts.
Power Limit 1 Clamp Mode	Disabled **Enabled**	Enable / Disable Power Limit 1 Clamp Mode.
Power Limit 1 Power	**Auto** 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25	Power Limit 1 in Watts. Auto will program Power Limit 1 based on silicon default support value.
Power Limit 1 Time Windows	**Auto** 1 2 3 4 5 6 7 8 10 12 14 16 20 24 28	Power Limit 1 Time Windows Value in Seconds. Auto will program Power Limit 1 Time Windows base on silicon default support value.

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Feature	Options	Description
	32 40 48 56 64 80 96 112 128	
Active Processor Cores	**Disabled** Enabled	Number of cores to enable in each processor package.
Intel Virtualization Technology	Disabled **Enabled**	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.
VT-d	Disabled **Enabled**	Enable / Disable CPU VT-d
Bi-directional PROCHOT	Disabled **Enabled**	When a processor thermal sensor trips (either core), the PROCHOT# will be driven. If bi-direction is enabled, external agents can drive PROCHOT# to throttle the processor.
Thermal Monitor	Disabled **Enabled**	Enable / Disable Thermal Monitor.
Monitor Mwait	Disabled Enabled **Auto**	Enable / Disable Monitor Mwait.
P-STATE Coordination	**HW_ALL** SW_ALL SW_ANY	Change P-STATE Coordination type.
DTS	Disabled **Enabled**	Enable / Disable Digital Thermal Sensor.

7.3.2. Advanced > Graphics Configuration

Feature	Options	Description
Graphics Configuration	Info only	
LVDS	Info only	
Data format and Color Depth	VESA 24 bpp JEIDA 24 bbp **JEIDA/vesa 18 bpp**	Data format and Color Depth select
LVDS Output Mode	Dual LVDS bus **Signal LVDS bus**	Signal / Dual mode select
DE Polaarity	**Active High** Active Low	DE Polaarity Select
Vsync Polarity	**Active High** Active Low	Vsync Polarity select
Hsync Polarity	**Active High** Active Low	Hsync Polarity select
LVDS Backlight Brightness	0 - **255**	LVDS Backlight Brightness adjust. A change takes effect immediately.

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7.3.3. Advanced > Power Management

Feature	Options	Description
Power Management	Info only	
Enable ACPI Auto Configuration	**Disabled** Enabled	Enables or Disables BIOS ACPI Auto Configuration.
Enable Hibernation	Disabled **Enabled**	Enable or Disable System ability to Hibernate (OS/S4 Sleep State). This option maybe not effective with some OS.
ACPI Sleep State	Suspend Disable **S3 (Suspend to RAM)**	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
Emulation AT/ATX	Emulation AT **ATX**	Select Emulation AT or ATX function. If this option set to [Emulation AT], BIOS will report no suspend functions to ACPI OS. In windows XP, it will make OS show shutdown message during system shutdown.
Lock Legacy Resources	**Disabled** Enabled	Enables or Disables Lock of Legacy Resources.
LID Function	**Disabled** Enabled	Enable / Disable LID Function.
ECO Mode	**Disabled** Enabled	Reduces the power consumption of the system, but after a shutdown, you have to wait at least 5 seconds before you can restart the system.
Power Consumption	Submenu	Power Consumption.

7.3.3.1. Advanced > Power Management > Power Consumption

Feature	Options	Description
Power Consumption	Info Only	
Current Input Current	Info Only	Display Current Input Current
Current Input Power	Info Only	Display Current Input Power
VCORE	Info Only	Display VCORE Voltage
VGFX	Info Only	Display VGFX Voltage
VMEM	Info Only	Display VMEM Voltage
5VSB	Info Only	Display 5VSB Voltage
VIN	Info Only	Display VIN Voltage
5V	Info Only	Display 5V Voltage
3.3V	Info Only	Display 3.3V Voltage
3.3VSB	Info Only	Display 3.3VSB Voltage

7.3.4. Advanced > System Management

Feature	Options	Description
System Management	Info Only	
Version	Info Only	Display SEMA Module Version.

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Feature	Options	Description
SEMA Firmware	Info Only	Display SEMA Firmware Version.
Build Date	Info Only	Display SEMA Firmware Build Date.
SEMA Bootloader	Info Only	Display SEMA Bootloader Version.
Build Date	Info Only	Display SEMA Bootloader Build Date.
SEMA Features	Submenu	Display SEMA Supported Features
SEMA Supported Features	Info only	Display SEMA Supported Features
Flags	Submenu	Flag
Flags	Info only	
BMC Flags	Info Only	
BIOS Select	Info Only	
ATX/AT-Mode	Info Only	
Exception Code	Info Only	

7.3.5. Advanced > Thermal Management

Feature	Options	Description
Thermal Configuration Parameters	Info Only	
Thermal and Fan Speed	Submenu	
Smart Fan	Submenu	
Critical Trip Point	**Disabled** 80 C 90 C 95 C 105 C	The value is the temperature threshold of the Critical Trip Point.
Passive Cooling Trip Point	Disabled 70 C 80 C 90 C **100 C**	The value is the temperature threshold of the Passive Cooling Trip Point.

7.3.5.1. Advanced > Thermal Management > Thermal and Fan Speed

Feature	Options	Description
Temperatures and Fan Speed	Info Only	
CPU Temperature	Info Only	
Current	Info Only	Display Current CPU Temperature
Board Temperature	Info Only	
Current	Info Only	Display Current Board Temperature
Startup	Info Only	Display Startup Board Temperature
Min	Info Only	Display Min Board Temperature
Max	Info Only	Display Max Board Temperature
CPU Fan Speed	Info Only	Display CPU Fan Speed

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7.3.5.2. Advanced > Thermal Management > Smart Fan

Feature	Options	Description
Smart Fan	Info Only	
CPU Smart Fan Temperature Source	CPU Sensor **Board Sensor**	CPU Smart Fan Temperature Source
CPU Fan Mode	AUTO (Smart Fan) **Fan Off** Fan On	CPU Fan Mode
PWM Level	0 - **100**	Control PWM Level

7.3.6. Advanced > Watchdog Timer

Feature	Options	Description
Watchdog Timer	Info only	
RunTime Watchdog	**Disabled** Enabled	The RunTime Watchdog resets the system after a certain amount of time after power up.

7.3.7. Advanced > CSM Configuration

Feature	Options	Description
Compatibility Support Module Configuration	Info only	
CSM Support	**Disableed** Enabled	Enabled / Disabled CSM Support.

7.3.8. Advanced > Super IO Configuration

Feature	Options	Description
NCT5104D	Info only	
Serial Port 1 Configuration	Submenu	Set Parameters of Serial Port 1 (COMA).
Serial Port 2 Configuration	Submenu	Set Parameters of Serial Port 2 (COMB).
W83627DHG	Info Only	
Serial Port 1 Configuration	Submenu	Set Parameters of Serial Port 1 (COMA).
Serial Port 2 Configuration	Submenu	Set Parameters of Serial Port 2 (COMB).

7.3.8.1. Advanced > Super IO Configuration > Serial Port 1 Configuration (NCT5104D)

Feature	Options	Description
NCT5104D	Info only	
Serial Port 1 Configuration	Submenu	Set Parameters of Serial Port 1 (COMA).
Serial Port 1 Configuration	Info only	
Serial Port	Disableed **Enabled**	Enable or Disable Serial Port (COM).

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Feature	Options	Description
Device Settings	Info Only	Display IO / IRQ information of COM Port.
Change Settings	**Auto** IO=240h; IRQ=10; IO=240h; IRQ=3,4,5,6,7,10,11,12 IO=248h; IRQ=3,4,5,6,7,10,11,12 IO=250h; IRQ=3,4,5,6,7,10,11,12 IO=258h; IRQ=3,4,5,6,7,10,11,12	Select an optimal setting for Super IO Device.

7.3.8.2. Advanced > Super IO Configuration > Serial Port 2 Configuration (NCT5104D)

Feature	Options	Description
Serial Port 2 Configuration	Submenu	Set Parameters of Serial Port 2 (COMB).
Serial Port 2 Configuration	Info only	
Serial Port	Disableed **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	Info Only	Display IO / IRQ information of COM Port.
Change Settings	**Auto** IO=248h; IRQ=11; IO=240h; IRQ=3,4,5,6,7,10,11,12 IO=248h; IRQ=3,4,5,6,7,10,11,12 IO=250h; IRQ=3,4,5,6,7,10,11,12 IO=258h; IRQ=3,4,5,6,7,10,11,12	Select an optimal setting for Super IO Device.

7.3.8.3. Advanced > Super IO Configuration > Serial Port 1 Configuration (W83627DHG)

Feature	Options	Description
Serial Port 1 Configuration	Submenu	Set Parameters of Serial Port 1 (COMA).
Serial Port 1 Configuration	Info only	
Serial Port	Disableed **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	Info Only	Display IO / IRQ information of COM Port.
Change Settings	**Auto** IO=3F8h; IRQ=4; IO=3F8h; IRQ=3,4,5,6,7,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,10,11,12	Select an optimal setting for Super IO Device.

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7.3.8.4. Advanced > Super IO Configuration > Serial Port 2 Configuration (W83627DHG)

Feature	Options	Description
Serial Port 2 Configuration	Submenu	Set Parameters of Serial Port 2 (COMB).
Serial Port 2 Configuration	Info only	
Serial Port	Disableed **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	Info Only	Display IO / IRQ information of COM Port.
Change Settings	**Auto** IO=2F8h; IRQ=3; IO=3F8h; IRQ=3,4,5,6,7,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,10,11,12	Select an optimal setting for Super IO Device.

7.3.9. Advanced > Serial Console Redirection

Feature	Options	Description
COM1	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. The item will be lunched before enable Console Redirection.
COM2	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. The item will be lunched before enable Console Redirection.
COM3	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. The item will be lunched before enable Console Redirection.

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Feature	Options	Description
COM4	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. The item will be lunched before enable Console Redirection.
Legacy Console Redirection	Info only	
Legacy Console Redirection Settings	Submenu	Legacy Console Redirection Settings

7.3.9.1. Advanced > Serial Console Redirection > Console Redirection Settings (if COM1 enabled)

Feature	Options	Description
COM1	Info only	
Console Redirection Settings	Info only	
Teriminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7 **8**	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.They can be used as an additional data bit.
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
VT-UTF8 Combo Key Support	**Enabled** Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals

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Feature	Options	Description
Recorder Mode	**Disabled** Enabled	With this mode enabled only text will be sent. This is to capture Terminal data.
Resolution 100x31	Enabled **Disabled**	On Legacy OS, the Number of Rows and Columns supported redirection
Legacy OS Redirection Resolution	**80x24** 80x25	On Legacy OS, the Number of Rows and Columns supported redirection
Putty KeyPad	**VT100** Intel Linux XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS POST	**Always Enable** BootLoader	When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always Enable.

7.3.9.2. Advanced > Serial Console Redirection > Console Redirection Settings (if COM2 enabled)

Feature	Options	Description
COM2	Info only	
Console Redirection Settings	Info only	
Teriminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7 **8**	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.They can be used as an additional data bit.
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.

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Feature	Options	Description
VT-UTF8 Combo Key Support	**Enabled** Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With this mode enabled only text will be sent. This is to capture Terminal data.
Resolution 100x31	Enabled **Disabled**	On Legacy OS, the Number of Rows and Columns supported redirection
Legacy OS Redirection Resolution	**80x24** 80x25	On Legacy OS, the Number of Rows and Columns supported redirection
Putty KeyPad	**VT100** Intel Linux XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS POST	**Always Enable** BootLoader	When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always Enable.

7.3.9.3. Advanced > Serial Console Redirection > Console Redirection Settings (if COM3 enabled)

Feature	Options	Description
COM3	Info only	
Console Redirection Settings	Info only	
Teriminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7 **8**	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.They can be used as an additional data bit.
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data

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Feature	Options	Description
		flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
VT-UTF8 Combo Key Support	**Enabled** Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With this mode enabled only text will be sent. This is to capture Terminal data.
Resolution 100x31	Enabled **Disabled**	On Legacy OS, the Number of Rows and Columns supported redirection
Legacy OS Redirection Resolution	**80x24** 80x25	On Legacy OS, the Number of Rows and Columns supported redirection
Putty KeyPad	**VT100** Intel Linux XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS POST	**Always Enable** BootLoader	When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always Enable.

7.3.9.4. Advanced > Serial Console Redirection > Console Redirection Settings (if COM4 enabled)

Feature	Options	Description
COM4	Info only	
Console Redirection Settings	Info only	
Teriminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7 **8**	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.They can be used as an additional data bit.
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.

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Feature	Options	Description
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
VT-UTF8 Combo Key Support	**Enabled** Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Recorder Mode	**Disabled** Enabled	With this mode enabled only text will be sent. This is to capture Terminal data.
Resolution 100x31	Enabled **Disabled**	On Legacy OS, the Number of Rows and Columns supported redirection
Legacy OS Redirection Resolution	**80x24** 80x25	On Legacy OS, the Number of Rows and Columns supported redirection
Putty KeyPad	**VT100** Intel Linux XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS POST	**Always Enable** BootLoader	When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always Enable.

7.3.9.5. Advanced > Serial Console Redirection > Legacy Console Redirection Settings

Feature	Options	Description
Legacy Serial Redirection Port	**COM1** COM2 COM3 COM4	Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages

7.3.10. Advanced > USB

Feature	Options	Description
USB	Info Only	
USB Module Version	Info Only	Display USB Module Version
USB Controllers:	Info Only	Display USB Controllers is XHCI or EHCI.
USB Devices:	Info Only	Display attatcment USB deviecs.
Legacy USB Support	**Enabled** Disabled Auto	Enables Legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices availiable only for EFI applications.
XHCI Hand-off	**Enabled** Disabled	This is a workaround for Oses without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	Disableed **Enabled**	Enable / Disable USB Mass Storge Driver Support.

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Feature	Options	Description
USB hardware delays and time-outs:	Info Only	
USB transfer rime-out	1 sec 5sec 10sec **20 sec**	The time-out value for Control, Bulk, and Interrupt transfers.
Device reset time-out	10 sec **20 sec** 30 sec 40 sec	USB mass storage device Start Unit command time-out.
Device power-up delay	**Auto** Manual	Maximum time the device will take before it properly reports itself to the Hot Controller. 'Auto' uses default value: for a Root po\rt it is 100 ms, for a Hub port the delay is taken form Hub descriptor.

7.3.11. Advanced > Network

Feature	Options	Description
Onboard LAN Controller	Disable **Enable**	Enable / Disable Onboard Intel I210LM Lan controller.
Network Stack	**Disable** Enable	Enable / Disable UEFI Network Stack.

7.3.12. Advanced > Miscellaneous

Feature	Options	Description
Miscellanous	Info Only	Control the PCI Express Root Port.
Smart Battery Function	**Disable** Enable	Enable / Disable Battery Function

7.3.13. Advanced > Driver Health

Feature	Options	Description
Driver Name	Info only	Provides Health Status for the Drivers / Controllers.

7.3.14. Advanced > Trusted Computing

Feature	Options	Description
TPM20 Device Found	Info Only	
Security Device Support	Disable **Enable**	Enables or Disable BIOS support for security device. OS will not show Security Device. TCG EFI protocol and available.
Active PCR banks	Info Only	
Available PCR banks	Info Only	
Pending operation	**None** TPM Clear	Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.

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Feature	Options	Description
Platform hierarchy	Disable **Enable**	Enable or Disable Platform Hierarchy
Storage Hierarchy	Disable **Enable**	Enable or Disable Storage Hierarchy
Endorsement Hierarchy	Disable **Enable**	Enable or Disable Endorsement Hierarchy
TPM2.0 UEFI Spec Version	TCG_1_2 **TCG_2**	Select the TCG2 Spec Version Support, TCG_1_2: the Compatible mode for Win8/Win10, TCG_2: Support new TCG2 protocol and event format for Win10 or later
Physical Presence Spec Version	**1.2** 1.3	Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.
TPM 20 Interface Type	Info only	

7.3.15. Advanced > AMI Graphic Output Protocol Policy

Feature	Options	Description
Intel (R) Graphics Controller	Info Only	
Intel (R) GOP Driver	Info Only	
Output Select	DVI	Output Interface

7.3.16. Advanced > SDIO Configuration

Feature	Options	Description
SDIO Configuration	Info Only	
SD Card/GPIO MODE	**GPIO** SD Card	Select SD Card or GPIO function.
SDIO Access Mode	**Auto** ADMA SDMA PIO	Auto Option: Access SD device in DMA mode if controller supports it,otherwise in PIO mode.DMA Option: Access SD device in DMA mode.PIO Option: Access SD device in PIO mode.
Mass Storage Devices:	Info Only	
Sdio Device 1 Details:	Info Only	
Bus 0 Dev 1c Func 0	Info Only	
MMC – xxxx(xx.xGB)	**Auto** Floppy Forced FDD Hard Disk	Mass storage device emulation type. 'AUTO' enumerates devices less than 530MB as floppies. Forced FDD option can be used to force HDD formatted drive to boot as FDD.

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7.4. Chipset

7.4.1. Chipset > North Bridge

Feature	Options	Description
Memory Information	Info only	
Total Memory	Info only	Display Total Memory Size.
Memory Vlotage	Info only	Display Memory Vlotage.
Memory Slot0	Info only	Display Installed Memory Slot0 Information.
Memory Slot1	Info only	Display Installed Memory Slot1 Information.
Max TOLUD	**2 GB** 2.25 GB 2.5 GB 2.75 GB 3 GB	Maximum Value of TOLUD.
PCIE VGA Workaround	Disable **Enable**	Enable it if your PCIe card cannot boot to DOS. This is for Test only.

7.4.2. Chipset > South Bridge

Feature	Options	Description
Serial IRQ Mode	Quiet **Continuous**	Configure Serial IRQ Mode.
SMBus Support	Disable **Enable**	Enable / Disable SMBus Support.
OS Selection	**Windows** Android Win7 Intel Linux	Select the target OS.
PCI CLOCK RUN	Disable **Enable**	Enables CLKRUN# logic to stop PCI clocks.

7.4.3. Chipset > Uncore Configuration

Feature	Options	Description
GOP Configuration	Info only	
Active LFP Config	**No LFP** eDP/LVDS	Active Local Flat Panel Config.
LVDS Backlight Mode	GTT Mode **BMC Mode**	Select LVDS Backlight control function.
DDI port 1	No Device Display Port HDMI **DisplayPort with HDMI/DVI Compatible**	DDI port 1 function choose to Display Port or HDMI.
DDI port 2	No Device Display Port HDMI **DisplayPort with HDMI/DVI Compatible**	DDI port 2 function choose to Display Port or HDMI.

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Feature	Options	Description
LFP Panel Type	**Auto** 640x480 800x600 1024x768 1280x1024 1400x1050 1600x1200 1366x768 1680x1050 1920x1200 1440x900 1600x900 1280x800 1920x1080 2048x1536	Select LFP panel used by Internal Graphics Device by selecting the appropriate setup item.
GOP Brightness Level	20 40 60 80 100 120 **140** 160 180 200 220 240 255	Set GOP Brightness Level.
IGD Configuration	Info only	
Integerated Graphics Devices	Disable **Enable**	Enable: Enable Integrated Graphics Device (IGD) when selected as the Primary Video Adaptor. Disable: Always disable IGD.
Primary Display	**IGD** PCIe HG	Select which of IGD / PCI Graphics device should be Primary Display.
Aperture Size	128MB **256MB** 512MB	Select the Aperture Size.
DVMT Pre-Allocated	**64M** 96M 128M 160M 192M 224M 256M 288M 320M 352M 384M 416M 448M 480M 512M	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device
DVMT Total Gfx Mem	128M **256M** MAX	Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device

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7.4.4. Chipset > South Cluster Configuration

Feature	Options	Description
HD-Audio Configuration	Submenu	HD-Audio Configuration Setting.
PCI Express Configuration	Submenu	PCI Express Configuration Setting.
SATA Drives	Submenu	Press <Enter> to select the SATA Device Configuration Setup option.
SSC Configuration	Submenu	SSC Configuration Settings.
USB Configuration	Submenu	USB Configuration Settings.
Miscellaneous Configuration	Submenu	Enable / Disable Misc. Feature.

7.4.4.1. Chipset > South Cluster Configuration > HD-Audio Configuration

Feature	Options	Description
HD-Audio Configuration	Info only	
HD-Audio Support	Disable **Enable**	Select the target OS.

7.4.4.2. Chipset > South Cluster Configuration > PCI Express Configuration

Feature	Options	Description
PCI Express Configuration	Info only	
PCIE Port assigned to LAN	Info only	Display PCIE Port assigned to LAN Information.
Complicace Mode	Disable **Enable**	Complicace Mode Enable / Disable.
PCIE Port 1-4 Configuration	**3 x1 Port**	**Note:** Default configuration for the lanes is 3 x1.Other configurations (1 x2, 2 x1 / 2 x2 / 4 x1) require a customized BIOS.
PCI ExpressRoot Port 1	Submenu	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port Disable: Disable PCIe root port
PCI ExpressRoot Port 2	Submenu	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port Disable: Disable PCIe root port
PCI ExpressRoot Port 3	Submenu	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port Disable: Disable PCIe root port
PCI ExpressRoot Port 4	Submenu	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port Disable: Disable PCIe root port

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Chipset > South Cluster Configuration > PCI Express Configuration > PCI Express Root Port 1

Feature	Options	Description
PCI Express Root Port 1	Disable **Enable** Auto	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port. Disable: Disable PCIe root port.
ASPM	**Disable** Enable	PCI Express Active State Power Management settings
L1 Substates	Disable L1.1 L1.2 **L1.1 & L1.2**	PCI Express L1 Substates settings.
ACS	Disable **Enable**	Enable/Disable Access Control Services Extended Capability
URR	**Disable** Enable	CI Express Unsupported Request Reporting Enable/Disable
FER	**Disable** Enable	PCI Express Device Fatal Error Reporting Enable/Disable
NFER	**Disable** Enable	PCI Express Device Non-Fatal Error Reporting Enable/Disable
CER	**Disable** Enable	PCI Express Device Correctable Error Reporting Enable/Disable
CTO	**Default Setting** 16-15 ms 65-210 ms 260-900 ms 1-3.5 s Disable	PCI Express Completion Timer TO Enable/Disable.
SEFE	**Disable** Enable	Root PCI Express System Error on Fatal Error Enable/Disable
SENFE	**Disable** Enable	Root PCI Express System Error on Non-Fatal Error Enable/Disable
SECE	**Disable** Enable	Root PCI Express System Error on Correctable Error Enable/Disable
PME SCI	Disable **Enable**	PCI Express PME SCI Enable/Disable
Hot Plug	**Disable** Enable	PCI Express Hot Plug Enable/Disable
PCIe Speed	**Auto** Gen1 Gen2	Configure PCIe Speed
Transmitter Half Swing	**Disable** Enable	Transmitter Half Swing Enable/Disable.
Extra Bus Reserved	**0**	Extra Bus Reserved (0-7) for bridges behind this Root Bridge
Reserved Memory	**10**	Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge
Reserved I/O	**4**	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge
PCH PCIe LTR Configuration	Info only	

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Feature	Options	Description
PCH PCIE LTR	Disable **Enable**	PCH PCIE Latency Reporting Enable/Disable
Snoop Latency Override	Disabled Manual **Auto**	Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Non Snoop Latency Override	Disabled Manual **Auto**	Non Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow
PCIE LTR Lock	**Disable** Enable	PCIE LTR Configuration Lock
PCIe Selection De0emphasis	Disable **Enable**	When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. 1b -3.5 dB 0b -6 dB

Chipset > South Cluster Configuration > PCI Express Configuration > PCI Express Root Port 2

Feature	Options	Description
PCI Express Root Port 2	Disable **Enable** Auto	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port. Disable: Disable PCIe root port.
ASPM	**Disable** Enable	PCI Express Active State Power Management settings
L1 Substates	Disable L1.1 L1.2 **L1.1 & L1.2**	PCI Express L1 Substates settings.
ACS	Disable **Enable**	Enable/Disable Access Control Services Extended Capability
URR	**Disable** Enable	CI Express Unsupported Request Reporting Enable/Disable
FER	**Disable** Enable	PCI Express Device Fatal Error Reporting Enable/Disable
NFER	**Disable** Enable	PCI Express Device Non-Fatal Error Reporting Enable/Disable
CER	**Disable** Enable	PCI Express Device Correctable Error Reporting Enable/Disable
CTO	**Default Setting** 16-15 ms 65-210 ms 260-900 ms 1-3.5 s Disable	PCI Express Completion Timer TO Enable/Disable.
SEFE	**Disable** Enable	Root PCI Express System Error on Fatal Error Enable/Disable
SENFE	**Disable** Enable	Root PCI Express System Error on Non-Fatal Error Enable/Disable
SECE	**Disable** Enable	Root PCI Express System Error on Correctable Error Enable/Disable

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Feature	Options	Description
PME SCI	Disable **Enable**	PCI Express PME SCI Enable/Disable
Hot Plug	**Disable** Enable	PCI Express Hot Plug Enable/Disable
PCIe Speed	**Auto** Gen1 Gen2	Configure PCIe Speed
Transmitter Half Swing	**Disable** Enable	Transmitter Half Swing Enable/Disable.
Extra Bus Reserved	**0**	Extra Bus Reserved (0-7) for bridges behind this Root Bridge
Reserved Memory	**10**	Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge
Reserved I/O	**4**	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge
PCH PCIe LTR Configuration	Info only	
PCH PCIE LTR	Disable **Enable**	PCH PCIE Latency Reporting Enable/Disable
Snoop Latency Override	Disabled Manual **Auto**	Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Non Snoop Latency Override	Disabled Manual **Auto**	Non Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow
PCIE LTR Lock	**Disable** Enable	PCIE LTR Configuration Lock
PCIe Selection De0emphasis	Disable **Enable**	When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. 1b -3.5 dB 0b -6 dB

Chipset > South Cluster Configuration > PCI Express Configuration > PCI Express Root Port 3

Feature	Options	Description
PCI Express Root Port 3	Disable **Enable** Auto	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port. Disable: Disable PCIe root port.
ASPM	**Disable** Enable	PCI Express Active State Power Management settings
L1 Substates	Disable L1.1 L1.2 **L1.1 & L1.2**	PCI Express L1 Substates settings.
ACS	Disable **Enable**	Enable/Disable Access Control Services Extended Capability
URR	**Disable** Enable	CI Express Unsupported Request Reporting Enable/Disable
FER	**Disable** Enable	PCI Express Device Fatal Error Reporting Enable/Disable

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Feature	Options	Description
NFER	**Disable** Enable	PCI Express Device Non-Fatal Error Reporting Enable/Disable
CER	**Disable** Enable	PCI Express Device Correctable Error Reporting Enable/Disable
CTO	**Default Setting** 16-15 ms 65-210 ms 260-900 ms 1-3.5 s Disable	PCI Express Completion Timer TO Enable/Disable.
SEFE	**Disable** Enable	Root PCI Express System Error on Fatal Error Enable/Disable
SENFE	**Disable** Enable	Root PCI Express System Error on Non-Fatal Error Enable/Disable
SECE	**Disable** Enable	Root PCI Express System Error on Correctable Error Enable/Disable
PME SCI	Disable **Enable**	PCI Express PME SCI Enable/Disable
Hot Plug	**Disable** Enable	PCI Express Hot Plug Enable/Disable
PCIe Speed	**Auto** Gen1 Gen2	Configure PCIe Speed
Transmitter Half Swing	**Disable** Enable	Transmitter Half Swing Enable/Disable.
Extra Bus Reserved	**0**	Extra Bus Reserved (0-7) for bridges behind this Root Bridge
Reserved Memory	**10**	Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge
Reserved I/O	**4**	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge
PCH PCIe LTR Configuration	Info only	
PCH PCIE LTR	Disable **Enable**	PCH PCIE Latency Reporting Enable/Disable
Snoop Latency Override	Disabled Manual **Auto**	Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Non Snoop Latency Override	Disabled Manual **Auto**	Non Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow
PCIE LTR Lock	**Disable** Enable	PCIE LTR Configuration Lock
PCIe Selection De0emphasis	Disable **Enable**	When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. 1b -3.5 dB 0b -6 dB

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Chipset > South Cluster Configuration > PCI Express Configuration > PCI Express Root Port 4

Feature	Options	Description
PCI Express Root Port 4	Disable **Enable** Auto	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port. Disable: Disable PCIe root port.
ASPM	**Disable** Enable	PCI Express Active State Power Management settings
L1 Substates	Disable L1.1 L1.2 **L1.1 & L1.2**	PCI Express L1 Substates settings.
ACS	Disable **Enable**	Enable/Disable Access Control Services Extended Capability
URR	**Disable** Enable	CI Express Unsupported Request Reporting Enable/Disable
FER	**Disable** Enable	PCI Express Device Fatal Error Reporting Enable/Disable
NFER	**Disable** Enable	PCI Express Device Non-Fatal Error Reporting Enable/Disable
CER	**Disable** Enable	PCI Express Device Correctable Error Reporting Enable/Disable
CTO	**Default Setting** 16-15 ms 65-210 ms 260-900 ms 1-3.5 s Disable	PCI Express Completion Timer TO Enable/Disable.
SEFE	**Disable** Enable	Root PCI Express System Error on Fatal Error Enable/Disable
SENFE	**Disable** Enable	Root PCI Express System Error on Non-Fatal Error Enable/Disable
SECE	**Disable** Enable	Root PCI Express System Error on Correctable Error Enable/Disable
PME SCI	Disable **Enable**	PCI Express PME SCI Enable/Disable
Hot Plug	**Disable** Enable	PCI Express Hot Plug Enable/Disable
PCIe Speed	**Auto** Gen1 Gen2	Configure PCIe Speed
Transmitter Half Swing	**Disable** Enable	Transmitter Half Swing Enable/Disable.
Extra Bus Reserved	**0**	Extra Bus Reserved (0-7) for bridges behind this Root Bridge
Reserved Memory	**10**	Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge
Reserved I/O	**4**	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge
PCH PCIe LTR Configuration	Info only	

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Feature	Options	Description
PCH PCIE LTR	Disable **Enable**	PCH PCIE Latency Reporting Enable/Disable
Snoop Latency Override	Disabled Manual **Auto**	Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Non Snoop Latency Override	Disabled Manual **Auto**	Non Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow
PCIE LTR Lock	**Disable** Enable	PCIE LTR Configuration Lock
PCIe Selection De0emphasis	Disable **Enable**	When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. 1b -3.5 dB 0b -6 dB

7.4.4.3. Chipset > South Cluster Configuration > SATA Drives

Feature	Options	Description
SATA Drives	Info only	
Chipset- SATA Controller Configuration	Info only	
Chipset SATA	Disable **Enable**	Enables or Disables the Chipset SATA Controller. The Chipset SATA controller supports the 2 black internal SATA ports (up to 3Gb/s supported per port).
SATA Mode Selection	**AHCI**	Determines how SATA controller(s) operate.
SATA Interface Speed	Gen1 **Gen2** Gen3	Select SATA Interface Speed, CHV A1 always with Gen Speed.
SATA Test Mode	**Disable** Enable	Test Mode Enable / Disable.
Aggressive LPM Support	**Disable** Enable	Enable PCH to Aggressively enter link power state.
SATA0	Info only	
Software Preserve	Info only	
Port 0	Disabled **Enabled**	Enable / Disable SATA Port
SATA Port 0 Hot Plug Capability	**Disabled** Enabled	If enabled, SATA port will be reported as Hot Plug capable.
Configured as eSATA	Info only	Display Configured as eSATA support.
Mechanical Presence Switch	Disabled **Enabled**	Controls reporting if this port has a Mechanical Presence Switch. Note. Request Hardware support.
Spin Up Device	**Disabled** Enabled	If enabled for any of ports Staggerred Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
SATA Device Type	**Hard Disk Drive** Solid State Drive	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.

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Feature	Options	Description
SATA Port 0 DevSlp	**Disabled** Enabled	Enable/Disable SATA Port 0 DevSlp. Board rework for LP needed before enable.
DITO Configuration	**Disabled** Enabled	Enable/Disable DITO Configuration
DITO Value	**625**	DITO Value. Note. DITO Value can be accessed if DITO Configuration item must enable.
DM Value	**15**	DM Value. Note. DM Value can be accessed if DITO Configuration item must enable.
SATA1	Info only	
Software Preserve	Info only	
Port 1	Disabled **Enabled**	Enable / Disable SATA Port
SATA Port 1 Hot Plug Capability	**Disabled** Enabled	If enabled, SATA port will be reported as Hot Plug capable.
Configured as eSATA	Info only	Display Configured as eSATA support.
Mechanical Presence Switch	Disabled **Enabled**	Controls reporting if this port has a Mechanical Presence Switch. Note. Request Hardware support.
Spin Up Device	**Disabled** Enabled	If enabled for any of ports Staggerred Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
SATA Device Type	**Hard Disk Drive** Solid State Drive	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.
SATA Port 1 DevSlp	**Disabled** Enabled	Enable/Disable SATA Port 1 DevSlp. Board rework for LP needed before enable.
DITO Configuration	**Disabled** Enabled	Enable/Disable DITO Configuration
DITO Value	**625**	DITO Value. Note. DITO Value can be accessed if DITO Configuration item must enable.
DM Value	**15**	DM Value. Note. DM Value can be accessed if DITO Configuration item must enable.

7.4.4.4. Chipset > South Cluster Configuration > SSC Configuration

Feature	Options	Description
SSC SD Card Support (D27:F0)	Disabled **Enabled**	Enable / Disable SCC SD Card Support.
SCC eMMC Support (D28:F0)	Disabled **Enabled**	Enable / Disable SCC eMMC Support.
eMMC Max Speed	**HS400** HS200 DDR50	Select the eMMC max Speed allowed.
SCC UFS Support (D29:F0)	**Disabled** Enabled	Enable / Disable UFS SDIO Support.
SCC SDIO Support (D30:F0)	**Disabled** Enabled	Enable / Disable SCC SDIO Support.

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Feature	Options	Description
SD Card/GPIO Mode	**GPIO** SD Card	Select SD Card or GPIO function.

7.4.4.5. Chipset > South Cluster Configuration > USB Configuration

Feature	Options	Description
XHCI Pre-Boot Driver	**Disabled** Enabled	Enable / Disable XHCI Pre-Boot Driver support.
XHCI Mode	Disabled **Enabled**	Once disabled, XHCI controller would be function disabled, none of the USB devices are detectable and usable during boot and in OS. Do not disable it unless for debug purpose.
USB Port Disable Override	**Disabled** Enabled	Selectively Enable/Disable the corresponding USB port from reporting a Device Connection to the controller.

7.4.4.6. Chipset > South Cluster Configuration > Miscellaneous Configuration

Feature	Options	Description
Miscellaneous Configuration	Info only	
State After G3	**S0 State** S5 State Last State	Specify what state to go to when power is re-applied after a power failure (G3 state). S0 State: System will boot directly as soon as power applied. S5 State: System keeps in power-off state until power button is pressed.
Wake On Lan	**Disabled** Enabled	Enable or Disable the Wake on Lan.
Spread Spectrum Clocking Configuration	Info only	
DDR SSC	Info only	
DDR SSC Selection Table	Info only	
DDR Clock Bending Selection Table	Info only	
HighSpeed SerialIO SSC	Info only	

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7.5. Security Menu

7.5.1. Security > Password Description

Feature	Options	Description
Password Description	Info only	
Setup Administrator Password	Enter Password	Set Setup Administrator Password
User Password	Enter Password	Set User Password
Secure Boot	Submenu	Customizable Secure Boot settings.
System Mode	Info only	
Secure Boot	Info only	
Secure Boot Control	**Disabled** Enabled	Secure Boot activated when Platform Key(PK) is enrolled, System mode is User / Deployed, and CSM function is disabled

7.6. Boot Menu

7.6.1. Boot > Boot Configuration

Feature	Options	Description
Boot Configuration	Info only	
Setup Prompt Timeout	**1**	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
Bootup NumLock State	**On** Off	Select the keyboard Number state.
Ouiet Boot	Disabled **Enabled**	Select the keyboard NumLock state.
Fast Boot	**Disabled** Enabled	Enable or Disable FastBoot features. Most probes are skipped to reduce time cost during boot.
New Boot Option Policy	**Default** Place First Place Last	Controls the placement of newly detected UEFI boot option.
Boot Mode select	LEGACY **UEFI**	Select boot mode LEGACY/UEFI

7.6.2. Boot > FIXED BOOT ORDER Priorities

Feature	Options	Description
Boot Option #1	Hardware	Set the system boot order.
Boot Option #2	CD/DVD	Set the system boot order.
Boot Option #3	USB Hard Disk	Set the system boot order.
Boot Option #4	USB CD/DVD	Set the system boot order.
Boot Option #5	USB Key	Set the system boot order.

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Feature	Options	Description
Boot Option #6	USB Floppy	Set the system boot order.
Boot Option #7	USB Lan	Set the system boot order.
Boot Option #8	Network	Set the system boot order.

7.7. Save & Exit Menu

7.7.1. Save and Exit

Feature	Options	Description
Save Changes and Exit		Exit system setup after saving the changes.
Discard Changes and Exit		Exit system setup without saving any changes.
Save Change and Reset		Reset the system after saving the changes.
Discard Changes and Reset		Reset system setup without saving any changes.
Save Options	Info only	
Save Changes		Save Changes done so far to any of the setup options.
Save as User Defaults		Save the changes done so far as User Defaults.
Restore User Defaults		Restore the User Defaults to all the setup options.
Boot Override	Info only	

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8. BIOS Checkpoints, Beep Codes

This section of this document lists checkpoints and beep codes generated by AMI Aptio BIOS. The checkpoints defined in this document are inherent to the AMIBIOS generic core, and do not include any chipset or board specific checkpoint definitions.

Checkpoints and Beep Codes Definition

A checkpoint is either a byte or word value output to I/O port 80h. The BIOS outputs checkpoints throughout bootblock and Power-On Self Test (POST) to indicate the task the system is currently executing. Checkpoints are very useful for debugging problems that occur during the preboot process.

Beep codes are used by the BIOS to indicate a serious or fatal error. They are used when an error occurs before the system video has been initialized, and generated by the system board speaker.

Aptio Boot Flow

While performing the functions of the traditional BIOS, Aptio 5.x core follows the firmware model described by the Intel Platform Innovation Framework for EFI (“the Framework”). The Framework refers the following “boot phases”, which may apply to various status code & checkpoint descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization[1]
- Driver Execution Environment (DXE) – main hardware initialization[2]
- Boot Device Selection (BDS) – system setup, pre-OS user interface & selecting a bootable device (CD/DVD, HDD, USB, Network, Shell, …)

Viewing BIOS Checkpoints

Viewing all checkpoints generated by the BIOS requires a checkpoint card, also referred to as a □OST Card or POST Diagnostic Card. These are PCI add-in cards that show the value of I/O port 80h on a LED display.

Some computers display checkpoints in the bottom right corner of the screen during POST. This display method is limited, since it only displays checkpoints that occur after the video card has been activated.

Keep in mind that not all computers using AMI Aptio BIOS enable this feature. In most cases, a checkpoint card is the best tool for viewing AMI Aptio BIOS checkpoints.

[1]Analogous to “bootblock” functionality of legacy BIOS
[2]Analogous to “POST” functionality in legacy BIOS

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8.1. Status Code Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

8.2. Standard Status Codes

8.2.1. SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization

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SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

8.2.2. SEC Beep Codes

None

8.2.3. PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization

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Status Code	Description
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes

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Status Code	Description
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

8.2.4. PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

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8.2.5. DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration

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Status Code	Description
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)

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Status Code	Description
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

8.2.6. DXE Beep Codes

# of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

8.2.7. ACPI/ASL Checkpoint

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state

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Status Code	Description
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

8.3. OEM-Reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

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9. Mechanical Information

9.1. Board-to-Board Connectors

To allow for different stacking heights, the receptacles for COM Express carrier boards are available in two heights: 5 mm and 8 mm. When 5 mm receptacles are chosen, the carrier board should be free of components.

Tyco 3-1827253-6

Foxconn QT002206-2131-3H

- 220-pin board-to-board connector with 0.5mm for a stacking height of 5 mm.
- This connector can be used with 5 mm through-hole standoffs (SMT type).



Tyco 3-6318491-6

Foxconn QT002206-4141-3H

- 220-pin board-to-board connector with 0.5mm for a stacking height of 8 mm.
- This connector can be used with 8 mm through-hole standoffs (SMT type).



Common Specifications

- Current capacity: 0.5A per pin
- Rated voltage: 50 VAC
- Insulation resistance: 100M or greater @ 500 VDC
- Temperature rating: -40°C ~ 85°C
- UL certification (ECBT2.E28476)
- Copper alloy (contacts)
- Housing: thermo-plastic molded compound (L.C.P.)

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9.2. Thermal Solution

9.2.1. Heat Spreaders

The function of the heat spreader is to ensure an identical mechanical profile for all COM Express modules. By using a heat spreader, the thermal solution that is built on top of the module is compatible with all COM Express modules.

9.2.2. Heat Sinks

A heat sink can be used as a thermal solution for a specific COM Express module and can have a fan or be fanless, depending on the thermal requirements.

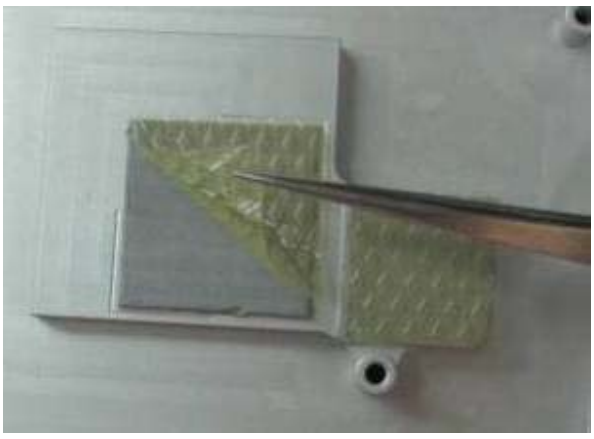
9.2.3. Installation

Install a heat spreader or heat sink using the following instructions.

Step 1: Before mounting the heatsink, install the required memory modules onto the SODIMM socket(s) on the COM Express module.

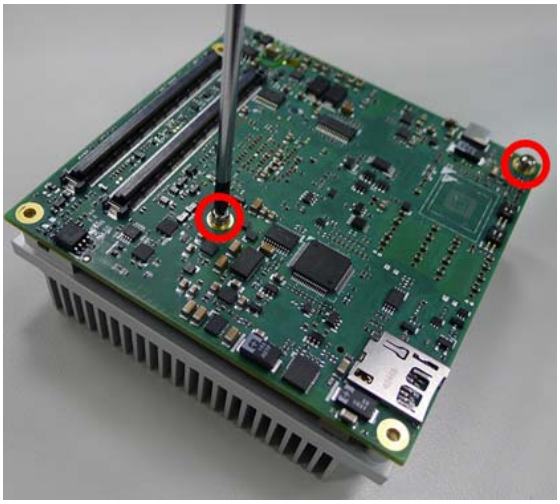


Step 2: Remove the protective membranes from the thermal pads.

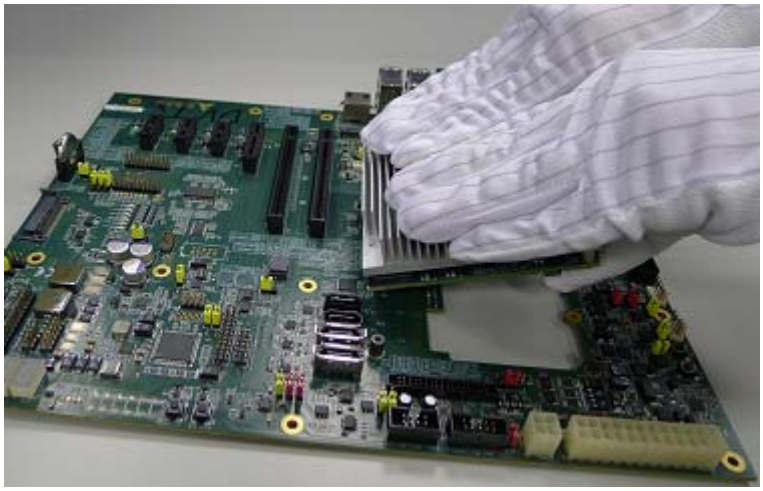


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Step 3: Assemble the heatsink onto the COM Express module. Use the four M2.5, L=6mm screws provided to fasten the heatsink to the module.

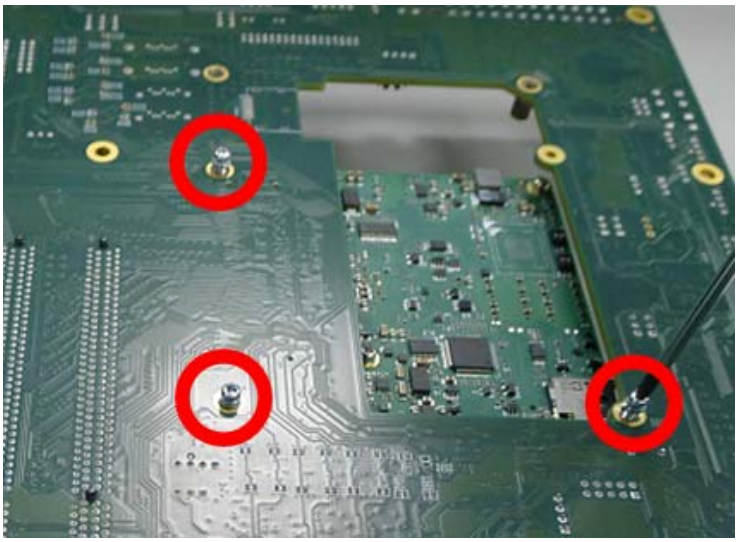


Step 4: Place the COM Express module and heatsink assembly onto the connectors on the carrier board as shown.



Then press down on the module until it is firmly seated on the carrier board.

Step 5: Use the five M2.5, L=16mm screws provided to secure the COM Express module to the carrier board from the solder side.



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Step 6: If you are installing a heatsink with a fan, plug the fan connector into the carrier board as shown.



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9.3. Mounting Methods

There are several standard ways to mount the COM Express module with a thermal solution onto a carrier board. In addition to the choice of 5 mm or 8mm board-to-board connectors, there is the choice of Top and Bottom mounting. In Top mounting, the threaded standoffs are on the carrier board and the thermal solution is equipped with through-hole standoffs. In Bottom mounting, the threaded standoffs are on the thermal solution and the carrier board has through-hole standoffs.

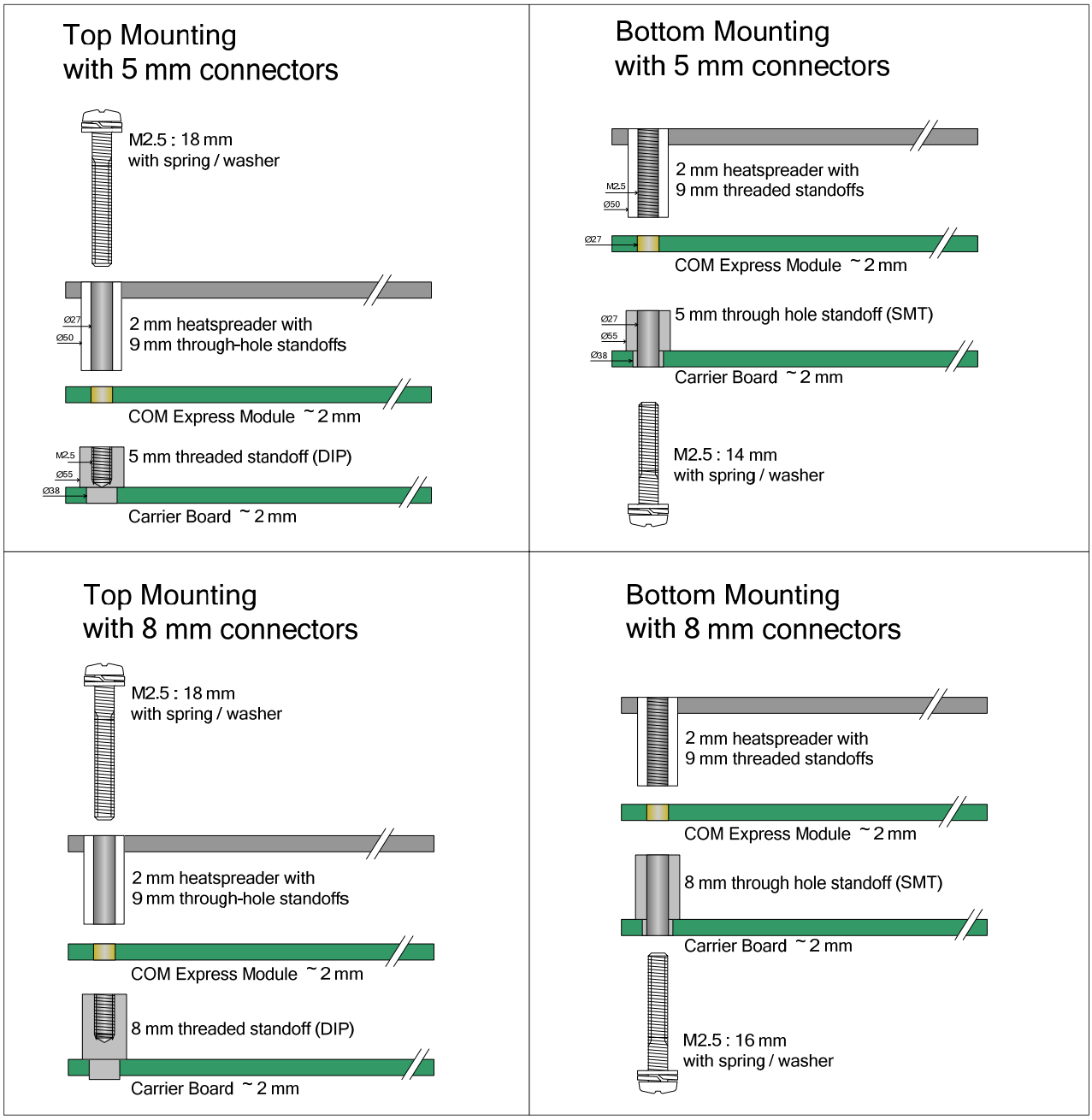


Figure 6: COM Express Mounting Methods

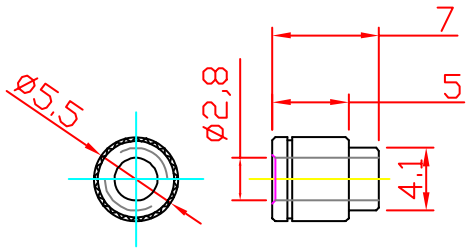
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9.4. Standoff Types

The standoffs available for Top and Bottom mounting methods are shown below. Note that threaded standoffs are DIP type and through-hole standoffs are SMT type. Other types not listed are available upon request.

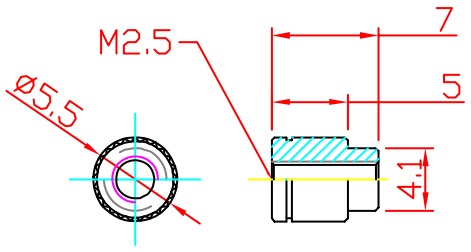
5mm through-hole standoff (SMT type)

P/N: 33-72000-0050



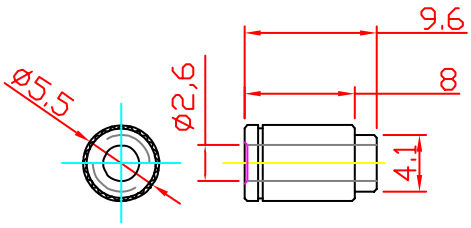
5mm threaded standoff (DIP type)

P/N: 33-72016-0050



8mm through-hole standoff (SMT type)

P/N: 33-72000-0080



8mm threaded standoff (DIP type)

P/N: 33-72015-0050

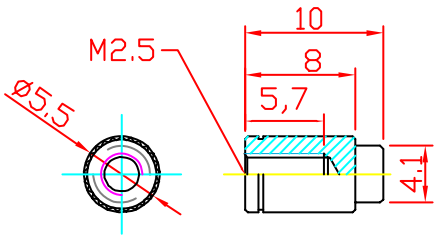


Figure 7: COM Express Standoff Types

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Safety Instructions

Read and follow all instructions marked on the product and in the documentation before you operate your system. Retain all safety and operating instructions for future use.

- Please read these safety instructions carefully.
- Please keep this User‘s Manual for later reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment, turn off the power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources.
  - Keep equipment away from high heat or high humidity.
  - Keep equipment properly ventilated (do not block or cover ventilation openings).
  - Make sure to use recommended voltage and power source settings.
  - Always install and operate equipment near an easily accessible electrical socket-outlet.
  - Secure the power cord (do not place any object on/over the power cord).
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings.
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.
- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

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Getting Service

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