cExpress-AR

User's Guide

AMD



COM Express®

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Revision History

Revision	Description	Date	Author
1.0	Initial release	2021-05-17	
1.1	Specifications and AB/CD connector signal descriptions updated	2021-08-03	
1.2	Yocto Linux support removed	2021-08-31	
1.3	BIOS tables and LAN LED function descriptions added	2024-06-18	AL

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Preface

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Safety Instructions

For user safety, please read and follow all Instructions, **Warning**s, **Caution**s, and **Note**s marked in this manual and on the associated equipment before handling/operating the equipment.

Read these safety instructions carefully.

- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

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Conventions

The following conventions may be used throughout this manual, denoting special levels of information

Note: This information adds clarity or specifics to text and illustrations.

Caution: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.

Warning: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

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Table of Contents

Revision History 2

Preface 3

Table of Contents 7

List of Figures 11

1. Introduction 12

2. Specifications 13
   - 2.1. Core System 13
   - 2.2. Video 14
     - 2.2.1 Display Interface Support 14
   - 2.3. Audio 15
   - 2.4. Expansion Busses 15
   - 2.5. Ethernet 15
   - 2.6. Multi I/O and Storage 16
   - 2.7. Trusted Platform Module (TPM) 17
   - 2.8. SEMA Board controller 17
   - 2.9. Debug 17
   - 2.10. Power 17
   - 2.11. Mechanical and Environmental 18

3. Block Diagram 19

4. Pinout and Signal Descriptions 20
   - 4.1. Pin Summary 20
   - 4.2. Signal Terminology Descriptions 25
   - 4.3. AB Connector Signal Descriptions 26
     - 4.3.1 Audio 26
     - 4.3.2 Analog VGA 27
     - 4.3.3 LVDS or eDP 28
     - 4.3.4 Gigabit Ethernet 31
     - 4.3.5 SATA 32
     - 4.3.6 PCI Express 33
     - 4.3.7 LPC bus 35

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4.3.8 USB ... 36
4.3.9 SPI Bus (BIOS only) ... 38
4.3.10 Miscellaneous ... 39
4.3.11 SMBus ... 40
4.3.12 I2C bus ... 40
4.3.13 General Purpose I/O (GPIO) ... 41
4.3.14 Serial Interface Signals ... 41
4.3.15 Power and System Management ... 42
4.3.16 Power and Ground ... 43
4.4. CD Connector Signal Descriptions ... 44
4.4.1 USB 3.0 Extensions ... 44
4.4.2 PCI Express ... 45
4.4.3 DDI1 Port ... 47
4.4.4 DDI2 Port ... 50
4.4.5 DDI3 Port ... 53
4.4.6 PCIe Graphics Port (PEG) ... 56
4.4.7 Module Type Definition ... 58
4.4.8 Power and Ground ... 59

5. Additional Features ... 60
5.1. Debug Connector ... 61
5.2. Status LEDs ... 62
5.3. Exception Codes ... 63
5.4. Fan Connector ... 64
5.5. BIOS Default Reset Button ... 65
5.6. BIOS Boot Select ... 66

6. System Resources ... 67
6.1 System Memory Map ... 67
6.2 I/O Map ... 68
6.3 Interrupt Request (IRQ) Lines ... 69
6.4 PCI Configuration Space Map ... 70
6.5 PCI Interrupt Routing Map ... 72
6.6 SMBus Address Table ... 73

7. BIOS Setup ... 74
7.1 Menu Structure ... 74
7.2 Main ... 75
7.2.1 BIOS Information ... 75
7.2.2 System Information ... 76

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7.2.3 Board Information 76
7.2.4 System Date and Time 77
7.3 Advanced 77
7.3.1 CPU Configuration 77
7.3.2 Graphic Configuration 78
7.3.3 Power Management 79
7.3.4 System Management 81
7.3.5 Thermal Management 83
7.3.6 Watchdog Timer 85
7.3.7 Super IO Configuration 85
7.3.8 Miscellaneous 89
7.3.9 Serial Console Redirection 90
7.3.10 Trusted Computing 93
7.3.11 AMD fTPM Configuration 94
7.3.12 Network Stack Configuration 95
7.3.13 PCI Subsystem Settings 96
7.3.14 USB Configuration 98
7.3.15 NVME Configuration 99
7.3.16 PCI/PCIe Configuration 100
7.3.17 SATA Configuration 101
7.3.18 RAM Disk Configuration 101
7.3.19 AMD CBS 102
7.3.20 AMD PBS 126
7.4 Chipset 130
7.4.1 Chipset > South Bridge 130
7.4.2 Chipset > GFX Configuration 135
7.4.3 Chipset > North Bridge 135
7.5 Security 136
7.5.1 Secure Boot menu 137
7.6. Boot 137
7.6.1 Boot Configuration 137
7.7 Save & Exit 138
7.7.1 Save Options 138
7.7.2 Default Options 139

8. BIOS Checkpoints, Beep Codes 140
8.1. Status Code Ranges 141
8.2. Standard Status Codes 142
8.2.1 SEC Phase 142

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8.2.2 SEC Beep Codes....143
8.2.3 PEI Phase....143
8.2.4 PEI Beep Codes....146
8.2.5 DXE Status Codes....147
8.2.6 DXE Beep Codes....150
8.2.7 ACPI/ASL Checkpoint....151
8.3. OEM-Reserved Checkpoint Ranges....151

9. Software Support....152
9.1. Operating Systems....152

10. Mechanical and Thermal....153
10.1. Module Dimensions....153
10.2. Thermal Solutions....154
10.2.1 Heatspreader: HTS....154
10.2.2 Heatsink: THS....155
10.2.3 Heatsink High Profile: THSH....156
10.2.4 Heatsink with Fan: THSF....157

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List of Figures

Figure 1 – Module function diagram 19
Figure 2 - Module rear side row and pin numbering 20
Figure 3 – Module feature locations 60
Figure 4 – cExpress-AR and Debug Module 61
Figure 5 – Module mechanical dimensions 153
Figure 6 – Heatspreader HTS 154
Figure 7 – Heatsink THS 155
Figure 8 – Heatsink High Profile: THSH 156
Figure 9 – Heatsink with Fan: THSF 157

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1. Introduction

The cExpress-AR is the first COM Express® COM.0 R3.0 Compact Size Type 6 module based on Octa-core (8 core) AMD® New Generation Ryzen™ Embedded V-Series SoC (formerly "Ryzen V2000") with up to 16 threads and an impressive turbo boost up to 4.25GHz. Compared to earlier generations, the additional cores combined with AMD's Zen2 architecture result in double the performance-per-watt efficiency. The cExpress-AR also features an upgraded high performance graphics core called AMD® Radeon™ with faster frequency and clocking. Industries in need of such high performance characteristics include ultrasound image processing, 4K high speed video encoding and streaming, gaming, AI inferencing at the Edge.

The cExpress-AR supports maximum 64GB DDR4 3200 MT/s memory capacity and supports ECC memory error correction based on selected SKUs. Combined with a configurable TDP as low as 10 watts while supporting 8-core/6-core makes fanless designs achievable, which are well suited for mission-critical, rugged applications.

The integrated AMD® Radeon™ Graphics include features such as OpenGL 4.6 and ES 3.x, DirectX 12, OpenCL 2.1/2.0/1.2, new generation multimedia engine, VCN2.2, supports for H.265/HEVC 10-bit hardware encode/decode, VP9 10-bit hardware decode. In addition, new generation display engine, DCN2.1, support maximum four independent display outputs include LVDS and three DDI ports supporting HDMI/DVI/DisplayPort and eDP/VGA as a build option.

Input/output features include up to eight PCIe Gen3 lanes (through a PCIe switch, project basis support) and one PCIe Gen3 x8 lanes that can be used for NVMe SSD, allowing applications access to the highest speed storage solutions, as well as a single onboard up to 2.5Gigabit Ethernet port supporting Time Sensitive Network (TSN), four USB 3.2 ports, four USB 2.0 ports, two SATA 6 Gb/s ports. Support is provided for SMBus and I2C. The module is equipped with SPI AMI EFI BIOS with CMOS backup, supporting embedded features such as remote console, hardware monitor, and watchdog timer.

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2. Specifications

2.1. Core System

CPU

AMD® Ryzen™ Embedded V2000 processor family, 7nm process

- AMD® V2748 2.9/4.25GHz, 4MB L2, 35-54W (8C/7CU)
- AMD® V2546 3.0/3.95GHz, 3MB L2, 35-54W (6C/6CU)
- AMD® V2718 1.7/4.15GHz, 4MB L2, 10-25W (8C/7CU)
- AMD® V2516 2.1/3.95GHz, 3MB L2, 10-25W (6C/7CU)

Memory

Up to 64GB 3200 MT/s DDR4 in two SODIMM sockets, max. 32GB per socket

ECC, non-ECC support

Cache

L2 Cache 4MB for V2748, V2718, 3MB for V2546, V2516

Embedded BIOS

AMI Aptio V UEFI with CMOS backup in 16MB SPI BIOS (dual BIOS by build option, project basis)

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2.2. Video

GPU

AMD® Radeon™ Graphics core architecture

GPU Feature Support

4 independent and simultaneous combinations of DisplayPort/HDMI/LVDS graphics outputs (up to 4x 4K60).

(eDP optional in place of LVDS, VGA optional in place of DDI 3.)

- HEVC/H.265 8/10b, H.264 8b, VP9 8/10b, JPEG HW decode
- HEVC/H.265 8/10b, H.264 8b HW encode
- DirectX up to 12
- OpenGL up to 4.6 and ES 3.x support
- OpenCL up to 2.1 support

Note: Availability of features dependent on operating system (Windows 10 64-bit, Linux 64-bit).

2.2.1 Display Interface Support

LVDS: Single/dual channel 18/24-bit LVDS through eDP to LVDS IC, supports DE mode and Hsync/Vsync mode.
Max. resolution is 1920x1200@60Hz in dual mode. Pixel clock frequency up to 112 MHz. VESA and JEIDA panel data formats supported.

eDP: eDP 1.3 up to 4 lane support, in place of LVDS (BOM option), max. resolution is 4096x2160 @60Hz, 30bpp

DDI x 3: Digital Display Ports (DDI) support DisplayPort 1.4a, HDMI 2.1 or DVI, max. resolution of Display Port 4096x2160 @60Hz, max. resolution of HDMI 4096x2160 @60Hz

VGA: VGA BOM option support, in place of DDI 3. Max. resolution is 1920x1200 @60Hz

Note: The achievable maximum resolution dependent on carrier design.

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2.3. Audio

Intel® Audio Co-processor integrated

Located on carrier Express-BASE6 (ALC886 standard support)

2.4. Expansion Busses

6 PCI Express x1 Gen3: Lanes 0,1,2,3 (configurable to x1, x2, x4) and Lanes 4,5 (x1 or x2)
A PCIe switch is HW BOM option by project basis to offer more x1 lanes via Lanes 6,7

1 PCI Express x8 Gen3: Lanes 16-23 (configurable to 1 x8 or 2 x4)

Other: SMBus (system), I2C (user), LPC

Note: General Purpose Ports GPP 2-9 can support up to 6 devices (SATA 0/1 count as one device), refer to Functional Diagram for details.

2.5. Ethernet

Intel® 2.5Gigabit Ethernet Controller i225 series (V or IT version)

Supports up to 2.5Gbits and 1000/100/10 Mbit/s connection
V version supports up to 2.5Gbits
IT version supports up to 2.5Gbits (supports TSN on Linux, by project basis, TBC)

Note: General Purpose Ports GPP 2-9 can support up to 6 devices (SATA 0/1 count as one device), refer to Functional Diagram for details.

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2.6. Multi I/O and Storage

USB

4x USB 3.2/2.0/1.1 (USB 0,1,2,3), 4x USB 2.0/1.1 (USB 4,5,6,7)
SuperSpeedPlus, SuperSpeed, High-Speed, Full-Speed and Low-Speed USB signalling

Notes: Carrier board must be designed for Gen2 operation.
USB 3.2 upgrade signal lanes 1,2,3 are from USB Hub.

UART

Two UART interfaces SER0 and SER1 RX/TX on module
Console Redirection COM 1 or COM 2 selectable in BIOS

Up to 4 serial ports are supported in standard BIOS including Super I/O on the carrier

COM Port	Description	IRQ	Address	Console Redirection Support
COM 1	Supported by module (SER0, A98/A99), via embedded controller	4	0x3F8	Yes
COM 2	Supported by module (SER1, A101/A102), via embedded controller	3	0x2F8	Yes
COM 3	Supported by Super I/O (W83627DHG) on carrier board	5	0x240	Yes
COM 4	Supported by Super I/O (W83627DHG) on carrier board	7	0x248	Yes

SER0, SER1 from SoC HSUART are BOM option support by project basis

GPIO ~~or SD~~

4 GPO and 4 GPI (GPI with interrupt)

SATA

2x SATA 6Gb/s (SATA 0,1)

Note: General Purpose Ports GPP 2-9 can support up to 6 devices (SATA 0/1 count as one device), refer to Functional Diagram for details.

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2.7. Trusted Platform Module (TPM)

Chipset: Infineon solution

Type: TPM 2.0 (LPC bus based)

TPM chip is BOM option

2.8. SEMA Board controller

Supports: Voltage/current monitoring, power sequence debug support, AT/ATX mode control, logistics and forensic information, flat panel control, general purpose I2C, failsafe BIOS (dual BIOS, opt. support), watchdog timer and fan control

2.9. Debug

30-pin flat cable connector for use with DB-30 x86 debug module

Supports BIOS POST code LED, embedded controller access, SPI BIOS flashing, internal power rail test points, debug LEDs

2.10. Power

Power Modes: AT and ATX mode (AT mode startup controlled by SEMA Board Controller)

Standard Voltage Input:	ATX: 12V±5% / 5Vsb ±5%	or	AT: 12V±5%
Wide Voltage Input:	ATX: 8.5-20V, 5Vsb ±5%	or	AT: 8.5-20V

Power Management: ACPI 5.0 compliant, Smart Battery support
Power States: C1-C6, S0, S1, S3, S4, S5, S5 ECO mode (Wake-on-USB S3/S4, WoL S3/S4/S5)

ECO Mode support for deep S5 for 5Vsb power saving

Power Consumption
Please contact your ADLINK representative for the document "COM Express Module Power Consumption".

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2.11. Mechanical and Environmental

Form Factor and specification

PICMG COM Express Rev 3.0 (COM.0 R3.0), Type 6, Compact size 95 x 95 mm

Operating Temperature

Standard	0°C to 60°C (Wide Voltage Input)	Storage: -20°C to 80°C

Humidity

5-90% RH operating, non-condensing, 5-95% RH storage (and operating with conformal coating)

Shock and Vibration

IEC 60068-2-64 and IEC-60068-2-27
MIL-STD-202F, Method 213B, Table 213-I, Condition A and Method 214A, Table 214-I, Condition D

HALT tested

Thermal Stress, Vibration Stress, Thermal Shock and Combined Test

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3. Block Diagram

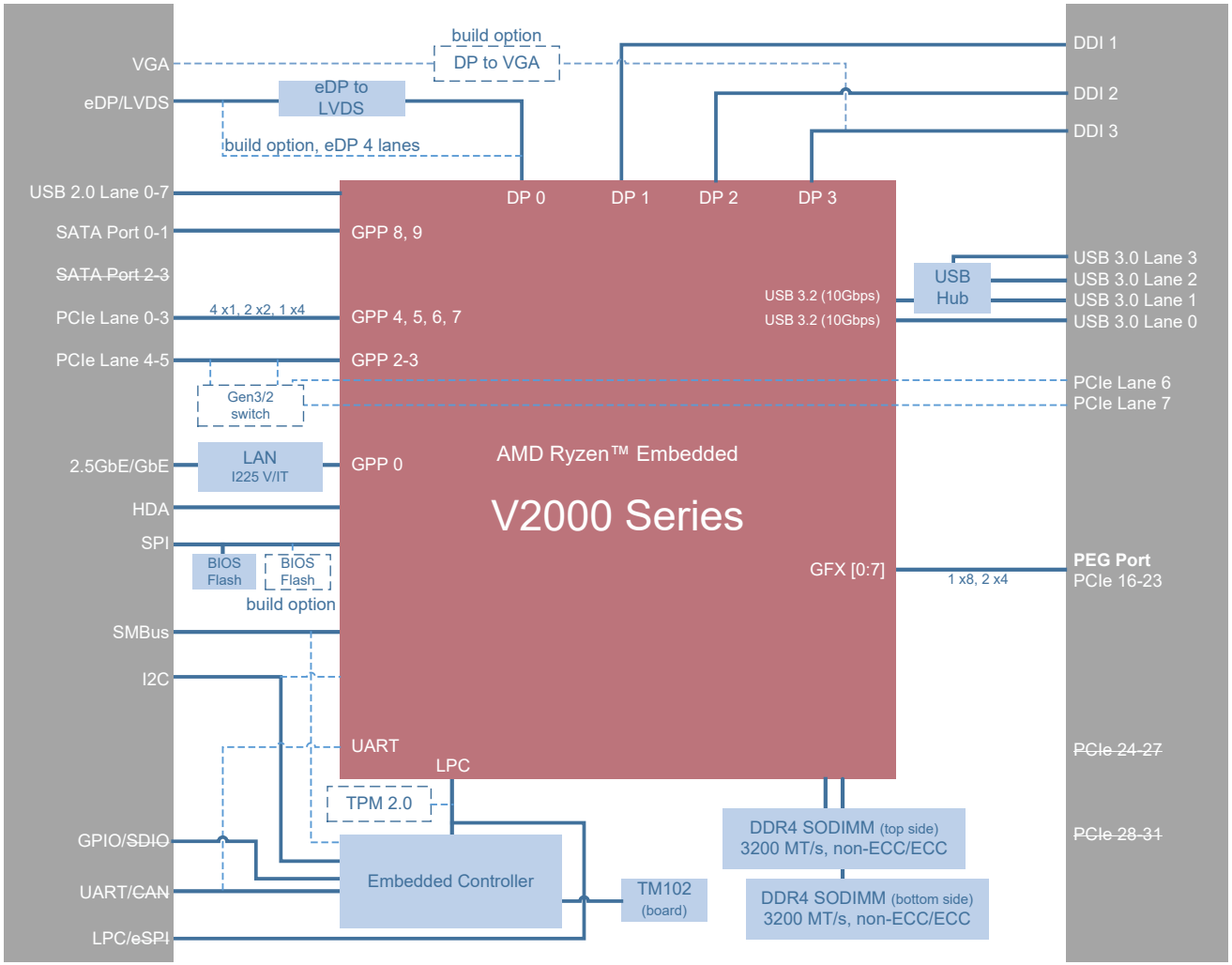


Figure 1 – Module function diagram

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4. Pinout and Signal Descriptions

4.1. Pin Summary

The table below is a comprehensible list of all signal pins supported on the dual 220-pin COM Express connectors as defined for Type 6 in the PICMG COM.0 R3.0 specification. Signals described in the specification but not supported on the cExpress-AR are strikethrough ~~STRIKETHROUGH.~~

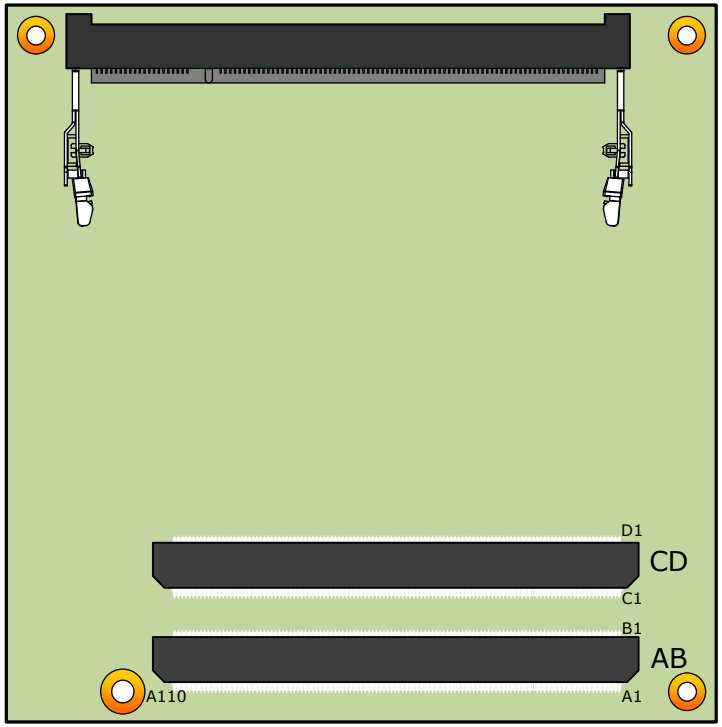


Figure 2 - Module rear side row and pin numbering

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Row A			Row B			Row C			Row D	
A1	GND (FIXED)		B1	GND (FIXED)		C1	GND FIXED)		D1	GND FIXED)
A2	GBE0_MDI3-		B2	GBE0_ACT#		C2	GND		D2	GND
A3	GBE0_MDI3+		B3	LPC_FRAME#/~~ESPI_CS0#~~		C3	USB_SSRX0-		D3	USB_SSTX0-
A4	GBE0_LINK100#		B4	LPC_AD0/~~ESPI_IO_0~~		C4	USB_SSRX0+		D4	USB_SSTX0+
A5	GBE0_LINK1000#		B5	LPC_AD1/~~ESPI_IO_1~~		C5	GND		D5	GND
A6	GBE0_MDI2-		B6	LPC_AD2/~~ESPI_IO_2~~		C6	USB_SSRX1-		D6	USB_SSTX1-
A7	GBE0_MDI2+		B7	LPC_AD3/~~ESPI_IO_3~~		C7	USB_SSRX1+		D7	USB_SSTX1+
A8	GBE0_LINK#		B8	LPC_DRQ0#/~~ESPI_ALERT0#~~		C8	GND		D8	GND
A9	GBE0_MDI1-		B9	~~LPC_DRQ1#/ESPI_ALERT1#~~		C9	USB_SSRX2-		D9	USB_SSTX2-
A10	GBE0_MDI1+		B10	LPC_CLK/~~ESPI_CK~~		C10	USB_SSRX2+		D10	USB_SSTX2+
A11	GND (FIXED)		B11	GND (FIXED)		C11	GND (FIXED)		D11	GND (FIXED)
A12	GBE0_MDI0-		B12	PWRBTN#		C12	USB_SSRX3-		D12	USB_SSTX3-
A13	GBE0_MDI0+		B13	SMB_CK		C13	USB_SSRX3+		D13	USB_SSTX3+
A14	~~GBE0_CTREF~~		B14	SMB_DAT		C14	GND		D14	GND
A15	SUS_S3#		B15	SMB_ALERT#		C15	~~DDI1_PAIR6+~~		D15	DDI1_CTRLCLK_AUX+
A16	SATA0_TX+		B16	SATA1_TX+		C16	~~DDI1_PAIR6-~~		D16	DDI1_CTRLDATA_AUX-
A17	SATA0_TX-		B17	SATA1_TX-		C17	RSVD		D17	RSVD
A18	SUS_S4#		B18	SUS_STAT#/~~ESPI_RESET#~~		C18	RSVD		D18	RSVD
A19	SATA0_RX+		B19	SATA1_RX+		C19	PCIE_RX6+ *		D19	PCIE_TX6+ *
A20	SATA0_RX-		B20	SATA1_RX-		C20	PCIE_RX6- *		D20	PCIE_TX6- *
A21	GND (FIXED)		B21	GND (FIXED)		C21	GND (FIXED)		D21	GND (FIXED)
A22	~~SATA2_TX+~~		B22	~~SATA3_TX+~~		C22	PCIE_RX7+ *		D22	PCIE_TX7+ *
A23	~~SATA2_TX-~~		B23	~~SATA3_TX-~~		C23	PCIE_RX7- *		D23	PCIE_TX7- *
A24	SUS_S5#		B24	PWR_OK		C24	DDI1_HPD		D24	RSVD
A25	~~SATA2_RX+~~		B25	~~SATA3_RX+~~		C25	~~DDI1_PAIR4+~~		D25	RSVD
A26	~~SATA2_RX-~~		B26	~~SATA3_RX-~~		C26	~~DDI1_PAIR4-~~		D26	DDI1_PAIR0+
A27	BATLOW#		B27	WDT		C27	RSVD		D27	DDI1_PAIR0-
A28	(S)ATA_ACT#		B28	AC/HDA_SDIN2		C28	RSVD		D28	RSVD
A29	AC/HDA_SYNC		B29	AC/HDA_SDIN1		C29	~~DDI1_PAIR5+~~		D29	DDI1_PAIR1+
A30	AC/HDA_RST#		B30	AC/HDA_SDIN0		C30	~~DDI1_PAIR5-~~		D30	DDI1_PAIR1-
A31	GND (FIXED)		B31	GND (FIXED)		C31	GND (FIXED)		D31	GND (FIXED)
A32	AC/HDA_BITCLK		B32	SPKR		C32	DDI2_CTRLCLK_AUX+		D32	DDI1_PAIR2+
A33	AC/HDA_SDOUT		B33	I2C_CK		C33	DDI2_CTRLDATA_AUX-		D33	DDI1_PAIR2-
A34	BIOS_DIS0#/~~ESPI_SAFS~~		B34	I2C_DAT		C34	DDI2_DDC_AUX_SEL		D34	DDI1_DDC_AUX_SEL
A35	THRMTRIP#		B35	THRM#		C35	RSVD		D35	RSVD

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Row A			Row B			Row C			Row D	
A36	USB6-		B36	USB7-		C36	DDI3_CTRLCLK_AUX+		D36	DDI1_PAIR3+
A37	USB6+		B37	USB7+		C37	DDI3_CTRLDATA_AUX-		D37	DDI1_PAIR3-
A38	USB_6_7_OC#		B38	USB_4_5_OC#		C38	DDI3_DDC_AUX_SEL		D38	RSVD
A39	USB4-		B39	USB5-		C39	DDI3_PAIR0+		D39	DDI2_PAIR0+
A40	USB4+		B40	USB5+		C40	DDI3_PAIR0-		D40	DDI2_PAIR0-
A41	GND (FIXED)		B41	GND (FIXED)		C41	GND (FIXED)		D41	GND (FIXED)
A42	USB2-		B42	USB3-		C42	DDI3_PAIR1+		D42	DDI2_PAIR1+
A43	USB2+		B43	USB3+		C43	DDI3_PAIR1-		D43	DDI2_PAIR1-
A44	USB_2_3_OC#		B44	USB_0_1_OC#		C44	DDI3_HPD		D44	DDI2_HPD
A45	USB0-		B45	USB1-		C45	RSVD		D45	RSVD
A46	USB0+		B46	USB1+		C46	DDI3_PAIR2+		D46	DDI2_PAIR2+
A47	VCC_RTC		B47	~~ESPI_EN#~~		C47	DDI3_PAIR2-		D47	DDI2_PAIR2-
A48	RSVD		B48	~~USB0_HOST_PRSNT~~		C48	RSVD		D48	RSVD
A49	GBE0_SDP		B49	SYS_RESET#		C49	DDI3_PAIR3+		D49	DDI2_PAIR3+
A50	LPC_SERIRQ~~/ESPI_CS1#~~		B50	CB_RESET#		C50	DDI3_PAIR3-		D50	DDI2_PAIR3-
A51	GND (FIXED)		B51	GND (FIXED)		C51	GND (FIXED)		D51	GND (FIXED)
A52	PCIE_TX5+		B52	PCIE_RX5+		C52	PEG_RX0+		D52	PEG_TX0+
A53	PCIE_TX5-		B53	PCIE_RX5-		C53	PEG_RX0-		D53	PEG_TX0-
A54	GPI0		B54	GPO1		C54	TYPE0#		D54	~~PEG_LANE_RV#~~
A55	PCIE_TX4+		B55	PCIE_RX4+		C55	PEG_RX1+		D55	PEG_TX1+
A56	PCIE_TX4-		B56	PCIE_RX4-		C56	PEG_RX1-		D56	PEG_TX1-
A57	GND		B57	GPO2		C57	TYPE1#		D57	TYPE2#
A58	PCIE_TX3+		B58	PCIE_RX3+		C58	PEG_RX2+		D58	PEG_TX2+
A59	PCIE_TX3-		B59	PCIE_RX3-		C59	PEG_RX2-		D59	PEG_TX2-
A60	GND (FIXED)		B60	GND (FIXED)		C60	GND (FIXED)		D60	GND (FIXED)
A61	PCIE_TX2+		B61	PCIE_RX2+		C61	PEG_RX3+		D61	PEG_TX3+
A62	PCIE_TX2-		B62	PCIE_RX2-		C62	PEG_RX3-		D62	PEG_TX3-
A63	GPI1		B63	GPO3		C63	RSVD		D63	RSVD
A64	PCIE_TX1+		B64	PCIE_RX1+		C64	RSVD		D64	RSVD
A65	PCIE_TX1-		B65	PCIE_RX1-		C65	PEG_RX4+		D65	PEG_TX4+
A66	GND		B66	WAKE0#		C66	PEG_RX4-		D66	PEG_TX4-
A67	GPI2		B67	WAKE1#		C67	~~RAPID_SHUTDOWN~~		D67	GND
A68	PCIE_TX0+		B68	PCIE_RX0+		C68	PEG_RX5+		D68	PEG_TX5+
A69	PCIE_TX0-		B69	PCIE_RX0-		C69	PEG_RX5-		D69	PEG_TX5-
A70	GND (FIXED)		B70	GND (FIXED)		C70	GND (FIXED)		D70	GND (FIXED)

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Row A			Row B			Row C			Row D	
A71	LVDS_A0+ / eDP_TX2+		B71	LVDS_B0+		C71	PEG_RX6+		D71	PEG_TX6+
A72	LVDS_A0- / eDP_TX2-		B72	LVDS_B0-		C72	PEG_RX6-		D72	PEG_TX6-
A73	LVDS_A1+ / eDP_TX1+		B73	LVDS_B1+		C73	GND		D73	GND
A74	LVDS_A1- / eDP_TX1-		B74	LVDS_B1-		C74	PEG_RX7+		D74	PEG_TX7+
A75	LVDS_A2+ / eDP_TX0+		B75	LVDS_B2+		C75	PEG_RX7-		D75	PEG_TX7-
A76	LVDS_A2- / eDP_TX0-		B76	LVDS_B2-		C76	GND		D76	GND
A77	LVDS_VDD_EN / eDP_VDD_EN		B77	LVDS_B3+		C77	RSVD		D77	RSVD
A78	LVDS_A3+		B78	LVDS_B3-		C78	~~PEG_RX8+~~		D78	~~PEG_TX8+~~
A79	LVDS_A3-		B79	LVDS_BKLT_EN		C79	~~PEG_RX8-~~		D79	~~PEG_TX8-~~
A80	GND (FIXED)		B80	GND (FIXED)		C80	GND (FIXED)		D80	GND (FIXED)
A81	LVDS_A_CK+ / eDP_TX3+		B81	LVDS_B_CK+		C81	~~PEG_RX9+~~		D81	~~PEG_TX9+~~
A82	LVDS_A_CK- / eDP_TX3-		B82	LVDS_B_CK-		C82	~~PEG_RX9-~~		D82	~~PEG_TX9-~~
A83	LVDS_I2C_CK / eDP_AUX+		B83	LVDS_BKLT_CTRL / eDP_BKLT_CTRL		C83	RSVD		D83	RSVD
A84	LVDS_I2C_DAT / eDP_AUX-		B84	VCC_5V_SBY		C84	GND		D84	GND
A85	GPI3		B85	VCC_5V_SBY		C85	~~PEG_RX10+~~		D85	~~PEG_TX10+~~
A86	RSVD		B86	VCC_5V_SBY		C86	~~PEG_RX10-~~		D86	~~PEG_TX10-~~
A87	eDP_HPD		B87	VCC_5V_SBY		C87	GND		D87	GND
A88	PCIE0_CK_REF+		B88	BIOS_DIS1#		C88	~~PEG_RX11+~~		D88	~~PEG_TX11+~~
A89	PCIE0_CK_REF-		B89	VGA_RED *		C89	~~PEG_RX11-~~		D89	~~PEG_TX11-~~
A90	GND (FIXED)		B90	GND (FIXED)		C90	GND (FIXED)		D90	GND (FIXED)
A91	SPI_POWER		B91	VGA_GRN *		C91	~~PEG_RX12+~~		D91	~~PEG_TX12+~~
A92	SPI_MISO		B92	VGA_BLU *		C92	~~PEG_RX12-~~		D92	~~PEG_TX12-~~
A93	GPO0		B93	VGA_HSYNC *		C93	GND		D93	GND
A94	SPI_CLK		B94	VGA_VSYNC *		C94	~~PEG_RX13+~~		D94	~~PEG_TX13+~~
A95	SPI_MOSI		B95	VGA_I2C_CK *		C95	~~PEG_RX13-~~		D95	~~PEG_TX13-~~
A96	TPM_PP		B96	VGA_I2C_DAT *		C96	GND		D96	GND
A97	TYPE10#		B97	SPI_CS#		C97	RSVD		D97	RSVD
A98	SER0_TX		B98	RSVD		C98	~~PEG_RX14+~~		D98	~~PEG_TX14+~~
A99	SER0_RX		B99	RSVD		C99	~~PEG_RX14-~~		D99	~~PEG_TX14-~~
A100	GND (FIXED)		B100	GND (FIXED)		C100	GND (FIXED)		D100	GND (FIXED)
A101	SER1_TX~~/CAN_TX~~		B101	FAN_PWMOUT		C101	~~PEG_RX15+~~		D101	~~PEG_TX15+~~
A102	SER1_RX~~/CAN_RX~~		B102	FAN_TACHIN		C102	~~PEG_RX15-~~		D102	~~PEG_TX15-~~
A103	LID#		B103	SLEEP#		C103	GND		D103	GND
A104	VCC_12V		B104	VCC_12V		C104	VCC_12V		D104	VCC_12V
A105	VCC_12V		B105	VCC_12V		C105	VCC_12V		D105	VCC_12V

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Row A			Row B			Row C			Row D	
A106	VCC_12V		B106	VCC_12V		C106	VCC_12V		D106	VCC_12V
A107	VCC_12V		B107	VCC_12V		C107	VCC_12V		D107	VCC_12V
A108	VCC_12V		B108	VCC_12V		C108	VCC_12V		D108	VCC_12V
A109	VCC_12V		B109	VCC_12V		C109	VCC_12V		D109	VCC_12V
A110	GND (FIXED)		B110	GND (FIXED)		C110	GND (FIXED)		D110	GND (FIXED)

Notes: ~~STRIKETHROUGH~~ entries are functions not supported by this product.
PCIe lane 6,7 are BOM options supported (through a PCIe switch) by project basis.
eDP (in place of LVDS) and VGA (in place of DDI 3) are BOM options supported by project basis.
General Purpose Ports GPP 2-9 can support up to a maximum of 6 devices (SATA 0/1 count as one device).

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4.2. Signal Terminology Descriptions

Meaning of the terms used for signal description tables.

Term	Description
I	Input to the module
O	Output from the module
I/O	Bi-directional Input / Output
OD	Open drain output from the module
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I/O $3.3V_{SB}$	Input or output 3.3V tolerant active in standby state
DDC	Display Data Channel
PCIE	PCI Express compatible differential signal
PEG	PCI Express Graphics
SATA	Serial ATA specification Revision 2.6 and 3
LVDS	Low Voltage Differential Signal - 330 mV nominal; 450 mV maximum differential signal
P	Power Input / Output
REF	Reference voltage output. May be sourced from a Module power plane.
PDS	Pull-down strap. A Module output pin that is either tied to GND or is not connected. Used to signal Module capabilities to the Carrier Board.
PU	PU (pull-up) resistor on module
PD	PD (pull-down) resistor on module

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4.3. AB Connector Signal Descriptions

4.3.1 Audio

Name	Pin #	Description	I/O	PU / PD	Comment
AC_RST# / HDA_RST#	A30	Reset output to CODEC, active low.	O 3.3VSB		
AC_SYNC / HDA_SYNC	A29	Sample-synchronization signal to the CODEC(s).	O 3.3V		
AC_BITCLK / HDA_BITCLK	A32	Serial data clock generated by the external CODEC(s).	I/O 3.3V		
AC_SDOUT / HDA_SDOUT	A33	Serial TDM data output to the CODEC.	O 3.3V		
AC_SDIN[2:0] / HDA_SDIN[2:0]	B28- B30	Serial TDM data inputs from up to 3 CODECs.	I/O 3.3VSB		

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4.3.2 Analog VGA

Name	Pin #	Description	I/O	PU / PD	Comment
VGA_RED	B89	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Shall also be terminated on the carrier with 150Ω resistor to ground close to VGA connector
VGA_GRN	B91	Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Shall also be terminated on the carrier with 150Ω resistor to ground close to VGA connector
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Shall also be terminated on the carrier with 150Ω resistor to ground close to VGA connector
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3V		
VGA_VSYNC	B94	Vertical sync output to VGA monitor	O 3.3V		
VGA_I2C_CK	B95	DDC clock line (I^2C port dedicated to identifying VGA monitor capabilities)	I/O OD 3.3V	PU 2k2 3.3V	
VGA_I2C_DAT	B96	DDC data line.	I/O OD 3.3V	PU 2k2 3.3V	

Note: VGA is BOM option supported (in place of DDI 3) by project basis.

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4.3.3 LVDS or eDP

The module default supports a single or dual channel LVDS display panel with up to 24-bit colours.
There is a BOM option that removes the eDP to LVDS bridge IC and outputs the eDP signals directly. eDP vs LVDS pin mapping is described below.

Pin #	LVDS mode	eDP mode
A71	LVDS_A0+	eDP_TX2+
A72	LVDS_A0-	eDP_TX2-
A73	LVDS_A1+	eDP_TX1+
A74	LVDS_A1-	eDP_TX1-
A75	LVDS_A2+	eDP_TX0+
A76	LVDS_A2-	eDP_TX0-
A78	LVDS_A3+	-
A79	LVDS_A3-	-
A81	LVDS_A_CK+	eDP_TX3+
A82	LVDS_A_CK-	eDP_TX3-
B71	LVDS_B0+	-
B72	LVDS_B0-	-
B73	LVDS_B1+	-
B74	LVDS_B1-	-
B75	LVDS_B2+	-
B76	LVDS_B2-	-
B77	LVDS_B3+	-
B78	LVDS_B3-	-
B81	LVDS_B_CK+	-
B82	LVDS_B_CK-	-
A77	LVDS_VDD_EN	eDP_VDD_EN
B79	LVDS_BKLT_EN	eDP_BKLT_EN
B83	LVDS_BKLT_CTRL	eDP_BKLT_CTRL
A83	LVDS_I2C_CK	eDP_AUX+
A84	LVDS_I2C_DAT	eDP_AUX-
A87	-	eDP_HPD

Note: LVDS by default, and eDP is a BOM option.

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4.3.3.1. Single/Dual Channel LVDS (default)

Name	Pin #	Description	I/O	PU / PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS Channel A differential clock	O LVDS		
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	B71 B72 B73 B74 B75 B76 B77 B78	LVDS Channel B differential pairs	O LVDS		
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS Channel B differential clock	O LVDS		
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 100K	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V	PD 100K	
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V	PD 100K	
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control.	I/O OD 3.3V	PU 2.2K 3.3V	
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/O OD 3.3V	PU 2.2K 3.3V	

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4.3.3.2. 4-lane eDP

Name	Pin #	Description	I/O	PU / PD	Comment
eDP_TX3+ eDP_TX3- eDP_TX2+ eDP_TX2- eDP_TX1+ eDP_TX1- eDP_TX0+ eDP_TX0-	A81 A82 A71 A72 A73 A74 A75 A76	eDP differential pairs	O PCIE		AC coupled off module
eDP_VDD_EN	A77	eDP power enable	O 3.3V	PD 100K	
eDP_BKLT_EN	B79	eDP backlight enable	O 3.3V	PD 100K	
eDP_BKLT_CTRL	B83	eDP backlight brightness control	O 3.3V	PD 100K	
eDP_AUX+	A83	eDP AUX+	I/O PCIE		AC coupled off module
eDP_AUX-	A84	eDP AUX-	I/O PCIE		AC coupled off module
eDP_HPD	A87	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	PD 100K on this pin when eDP is supported

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4.3.4 Gigabit Ethernet

Name	Pin #	Description	I/O	PU / PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: **1000 / 100 / 10** MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	I/O Analog		Twisted pair signals for external transformer.
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.	OD 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.	OD 3.3VSB		
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.	OD 3.3VSB		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	OD 3.3VSB		
~~GBE0_CTREF~~	~~A14~~	~~Reference voltage for Carrier Board Ethernet channel 1 and 2 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be 250 mA or less.~~	~~REF GND min 3.3V max~~		Not supported
GBE0_SDP	A49	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as 1pps signal.	IO 3.3VSB		

Note: This product supports up to 2.5GbE. The LAN LED behavior is optimized for a maximum of 2.5GbE. GBE0_LINK1000# is active for 2.5GbE speed, and GBE0_LINK100# is active for 1GbE or lower, while GBE0_ACT# and GBE0_LINK# share the same source from the LAN controller. For speeds of 100Mbit/sec and 10Mbit/sec, the LAN LED will be turned OFF.

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4.3.5 SATA

Name	Pin #	Description	I/O	PU / PD	Comment
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		AC coupled on Module
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		AC coupled on Module
~~SATA2_TX+ SATA2_TX-~~	~~A22 A23~~	~~Serial ATA channel 2, Transmit Output differential pair.~~	~~O SATA~~		Not supported
~~SATA2_RX+ SATA2_RX-~~	~~A25 A26~~	~~Serial ATA channel 2, Receive Input differential pair.~~	~~I SATA~~		Not supported
~~SATA3_TX+ SATA3_TX-~~	~~B22 B23~~	~~Serial ATA channel 3, Transmit Output differential pair.~~	~~O SATA~~		Not supported
~~SATA3_RX+ SATA3_RX-~~	~~B25 B26~~	~~Serial ATA channel 3, Receive Input differential pair.~~	~~I SATA~~		Not supported
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	O 3.3V	PU 10K 3.3V	

4.3.5.1. PCH HSIO Lane Assignments (SATA)

Name	HSIO name on SOC	Comment
SATA0	GPP 8	
SATA1	GPP 9	
SATA2	N/A	Not supported
SATA3	N/A	Not supported

Note: General Purpose Ports GPP 2-9 can support up to a maximum of 6 devices (SATA 0/1 count as one device).

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4.3.6 PCI Express

Name	Pin #	Description	I/O	PU / PD	Comment
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		

Note: PCIe Lane 6, 7 are supported by PCIe switch, by project basis.

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4.3.6.1. PCH HSIO Lane Assignments (PCI Express)

Name	HSIO name on SOC	Comment
PCIE0	GPP 4	
PCIE1	GPP 5	
PCIE2	GPP 6	
PCIE3	GPP 7	
PCIE4	GPP 2	
PCIE5	GPP 3	
PCIE6	N/A	BOM option support by project basis through a PCIe switch
PCIE7	N/A	BOM option support by project basis through a PCIe switch

Notes: General Purpose Ports GPP 2-9 can support up to a maximum of 6 devices (SATA 0/1 count as one device).
PCIe 0-3 can be x4, x2 or x1, PCIe 4-5 can be x2 or x1.

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4.3.7 LPC bus

Name	Pin #	Description	I/O	PU / PD	Comment
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	B4 B5 B6 B7	LPC multiplexed address, command and data bus	I/O 3.3V		Chipset has internal PU, 50K ±30%
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V		Chipset has internal termination, 50K ±30%
LPC_DRQ0# ~~LPC_DRQ1#~~	B8 ~~B9~~	LPC serial DMA request	I 3.3V		LPC_DRQ1 is not connected
LPC_SERIRQ	A50	LPC serial interrupt	I/O 3.3V		Chipset has internal PU, 50K ±30%
LPC_CLK	B10	LPC clock output –33MHz nominal	O 3.3V		The LPC_CLK frequency is 33MHz on this platform

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4.3.8 USB

Name	Pin #	Description	I/O	PU / PD	Comment
USB0+ USB0-	A46 A45	USB differential data pairs for Port 0	I/O 3.3VSB		USB 1.1/2.0 compliant
USB1+ USB1-	B46 B45	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/2.0 compliant
USB2+ USB2-	A43 A42	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/2.0 compliant
USB3+ USB3-	B43 B42	USB differential data pairs for Port 2	I/O 3.3VSB		USB 1.1/2.0 compliant
USB4+ USB4-	A40 A39	USB differential data pairs for Port 3	I/O 3.3VSB		USB 1.1/2.0 compliant
USB5+ USB5-	B40 B39	USB differential data pairs for Port 4	I/O 3.3VSB		USB 1.1/2.0 compliant
USB6+ USB6-	A37 A36	USB differential data pairs for Port 5	I/O 3.3VSB		USB 1.1/2.0 compliant
USB7+ USB7-	B37 B37	USB differential data pairs for Port 6	I/O 3.3VSB		USB 1.1/2.0 compliant
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10K 3.3VSB	
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3VSB	PU 10K 3.3VSB	
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10K 3.3VSB	

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Name	Pin #	Description	I/O	PU / PD	Comment
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10K 3.3VSB	
~~USB0_HOST_PRSNT~~	~~B48~~	~~Module USB client may detect the presence of a USB host on USB0. A high value indicates that a host is present.~~	~~I 3.3VSB~~		Not supported

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4.3.9 SPI Bus (BIOS only)

Name	Pin #	Description	I/O	PU / PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3VSB		
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier	O P 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I	PU 10K 3.3VSB	Carrier shall pull to GND or leave not- connected.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I	PU 10K 3.3VSB	Carrier shall pull to GND or leave not- connected

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4.3.10 Miscellaneous

Name	Pin #	Description	I/O	PU / PD	Comment
SPKR	B32	Output for audio enunciator, the "speaker" in PC-AT systems	O 3.3V		
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V		
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3VSB		
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3V	PU 1K 3.3V	
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD 3.3V		There shall be PD on carrier board
FAN_TACHIN	B102	Fan tachometer input for a fan with a two-pulse output.	I OD 3.3V	PU 47K 3.3V	
TPM_PP	A96	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V	PD 100K	

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4.3.11 SMBus

Name	Pin #	Description	I/O	PU / PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line. Power sourced through 3.3V standby rail and main power rails.	I/O OD 3.3VSB	PU 8.2K 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line. Power sourced through 3.3V standby rail and main power rails.	I/O OD 3.3VSB	PU 8.2K 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 3.3V standby rail and main power rails.	I 3.3VSB		

Note: SMBus from EC is build option support, by project basis.

4.3.12 I2C bus

Name	Pin #	Description	I/O	PU / PD	Comment
I2C_CK	B33	General purpose I^2C port clock output/input	I/O OD 3.3VSB	PU 2.2K 3.3VSB	Source SEMA BMC as default (chipset by BOM option)
I2C_DAT	B34	General purpose I^2C port data I/O line	I/O OD 3.3VSB	PU 2.2K 3.3VSB	Source SEMA BMC as default (chipset by BOM option)

Note: I2C default from EC. I2C from SoC is build option support, by project basis.

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4.3.13 General Purpose I/O (GPIO)

Name	Pin #	Description	I/O	PU / PD	Comment
GPO[0]	A93	General purpose output pins.	O 3.3V	PD 10K 3.3V	After hardware RESET output low
GPO[1]	B54	General purpose output pins.	O 3.3V	PD 10K 3.3V	After hardware RESET output low
GPO[2]	B57	General purpose output pins.	O 3.3V	PD 10K 3.3V	After hardware RESET output low
GPO[3]	B63	General purpose output pins.	O 3.3V	PD 10K 3.3V	After hardware RESET output low
GPI[0]	A54	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[1]	A63	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[2]	A67	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[3]	A85	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	

4.3.14 Serial Interface Signals

Name	Pin #	Description	I/O	PU / PD	Comment
SER0_TX	A98	General purpose serial port transmitter	O CMOS 3.3V		Power rail tolerance 5V, 12V There shall be PD on carrier board
SER0_RX	A99	General purpose serial port receiver	I CMOS 3.3V	PU 10K 3.3V	Power rail tolerance 5V, 12V
SER1_TX	A101	General purpose serial port transmitter	O CMOS 3.3V		Power rail tolerance 5V, 12V There shall be PD on carrier board
SER1_RX	A102	General purpose serial port receiver	I CMOS 3.3V	PU 10K 3.3V	Power rail tolerance 5V, 12V

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4.3.15 Power and System Management

Name	Pin #	Description	I/O	PU / PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge.	I 3.3VSB	PU 10K 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low request for module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.	I 3.3VSB	PU 10K 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow carrier-based FPGAs or other configurable devices time to be programmed.	I 3.3VSB	PU 10K 3.3VSB	Should have weak pull up.
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as "PS_ON") may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB		
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 8.2K 3.3VSB	
WAKE1#	B67	General purpose wake-up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 8.2K 3.3VSB	Connect to WAKE 0#
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low or may be used to signal some other external power-management event.	I 3.3VSB	PU 10K 3.3VSB	
LID#	A103	LID button. Low active signal used by the ACPI operating system for a LID switch.	I OD 3.3VSB	PU 47K 3.3VSB	Emulated on GPIO (BIOS)
SLEEP#	B103	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I OD 3.3VSB	PU 47K 3.3VSB	Emulated on GPIO (BIOS)
~~RAPID_ SHUTDOWN~~	~~C67~~	~~Trigger for Rapid Shutdown. Must be driven to 5V though a <=50-ohm source impedance for ≥ 20 µs.~~	~~I CMOS 5VSB~~		Not supported

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4.3.16 Power and Ground

Name	Pin #	Description	I/O	PU / PD	Comment
VCC_12V	A104, A105, A106, A107, A108, A109, B104, B105, B106, B107, B109	Primary power input supports wide range 5~ 20V input All available VCC_12V pins on the connector(s) shall be used.	P		8.5-20 V
VCC_5V_SBY	B84, B85, B86, B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		5Vsb ±5%
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path.	P		

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4.4. CD Connector Signal Descriptions

4.4.1 USB 3.0 Extensions

Name	Pin #	Description	I/O	PU / PD	Comment
USB_SSRX0- USB_SSRX0+	C3 C4	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB0	I PCIE		AC coupled on module
USB_SSTX0- USB_SSTX0+	D3 D4	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB0	O PCIE		AC coupled on module
USB_SSRX1- USB_SSRX1+	C6 C7	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB1	I PCIE		AC coupled on module
USB_SSTX1- USB_SSTX1+	D6 D7	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB1	O PCIE		AC coupled on module
USB_SSRX2- USB_SSRX2+	C9 C10	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB2	I PCIE		AC coupled on module
USB_SSTX2- USB_SSTX2+	D9 D10	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB2	O PCIE		AC coupled on module
USB_SSRX3- USB_SSRX3+	C12 C13	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB3	I PCIE		AC coupled on module
USB_SSTX3- USB_SSTX3+	D12 D13	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB3	O PCIE		AC coupled on module

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4.4.1.1. USB Root Segmentation

Name	HSIO name on SOC	Comment
USB 0	USB Port 1	
USB 1	-	From a USB Hub, USB Hub connect to SoC's USB Port 5
USB 2	-	From a USB Hub, USB Hub connect to SoC's USB Port 5
USB 3	-	From a USB Hub, USB Hub connect to SoC's USB Port 5

4.4.2 PCI Express

Name	Pin #	Description	I/O	PU / PD	Comment
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair.	O PCIE		AC coupled on Module By a PCIe switch, project basis
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair.	I PCIE		AC coupled off Module By a PCIe switch, project basis
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair.	O PCIE		AC coupled on Module By a PCIe switch, project basis
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair.	I PCIE		AC coupled off Module By a PCIe switch, project basis

Note: PCIe Lane 6, 7 are supported by PCIe switch, by project basis.

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4.4.2.1. PCH HSIO Lane Assignments (PCI Express)

Name	HSIO name on SOC	Comment
PCIE0	GPP 4	
PCIE1	GPP 5	
PCIE2	GPP 6	
PCIE3	GPP 7	
PCIE4	GPP 2	
PCIE5	GPP 3	
PCIE6	N/A	BOM option support by project basis through a PCIe switch
PCIE7	N/A	BOM option support by project basis through a PCIe switch

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4.4.3 DDI1 Port

Name	Pin #	DisplayPort (DP)	HDMI
DDI1_PAIR0+ DDI1_PAIR0-	D26 D27	DP1_LANE0+ DP1_LANE0-	TMDS1_DATA2+ TMDS1_DATA2-
DDI1_PAIR1+ DDI1_PAIR1-	D29 D30	DP1_LANE1+ DP1_LANE1-	TMDS1_DATA1+ TMDS1_DATA1-
DDI1_PAIR2+ DDI1_PAIR2-	D32 D33	DP1_LANE2+ DP1_LANE2-	TMDS1_DATA0+ TMDS1_DATA0-
DDI1_PAIR3+ DDI1_PAIR3-	D36 D37	DP1_LANE3+ DP1_LANE3-	TMDS1_CLK+ TMDS1_CLK-
DDI1_PAIR4+ DDI1_PAIR4-	C25 C26	-	-
DDI1_PAIR5+ DDI1_PAIR5-	C29 C30	-	-
DDI1_PAIR6+ DDI1_PAIR6-	C15 C16	-	-
DDI1_HPD	C24	DP1_HPD	HDMI1_HPD
DDI1_CTRLCLK_AUX+	D15	DP1_AUX+	HMDI1_CTRLCLK
DDI1_CTRLCLK_AUX-	D16	DP1_AUX-	HMDI1_CTRLDATA
DDI1_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL	DDI1_DDC_AUX_SEL

Note: Dual Mode (HDMI and DisplayPort on the same pins) implementations may be realized. This is desirable for SOCs that natively implement this capability. With such SOCs, the primary Dual Mode implementation challenge is that the HDMI_CTRL_DAT and HDMI_CTRL_CK lines are DC coupled, but the DP_AUX+ /- pair must be AC coupled. A set of FET switches is usually used to sort this out. The FET gates can be controlled by the AUX_SEL pin function.

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4.4.3.1. DisplayPort (DP) Mode (DDI1)

Name	Pin #	Description	I/O	PU / PD	Comment
DP1_LANE0+ DP1_LANE0- DP1_LANE1+ DP1_LANE1- DP1_LANE2+ DP1_LANE2- DP1_LANE3+ DP1_LANE3-	D26 D27 D29 D30 D32 D33 D36 D37	DP Port 1, differential pair data lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors ***shall*** be placed on the Carrier
DP1_HPD	C24	DP Port 1, detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	Module must tolerate high level in stand-by mode. The carrier board shall include a blocking FET on DP1_HPD to prevent back-drive current from damaging the Module.
DP1_AUX+	D15	DP Port 1, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PD 100K	AC coupled on Module
DP1_AUX-	D16	DP Port 1, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PU 100K 3.3V	AC coupled on Module
DDI1_DDC_AUX_SEL	D34	Strapping Signal to select HDMI or DP output 1M pull-down on the module and floating on the carrier enable DisplayPort mode	I 3.3V	PD 1M	DP mode enabled

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4.4.3.2. HDMI Mode (DDI1)

Name	Pin #	Description	I/O	PU / PD	Comment
TMDS1_DATA2+ TMDS1_DATA2- TMDS1_DATA1+ TMDS1_DATA1- TMDS1_DATA0+ TMDS1_DATA0-	D26 D27 D29 D30 D32 D33	HDMI / DVI Port, Differential Pair Data Lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
TMDS1_CLK+ TMDS1_CLK-	D36 D37	HDMI Port, Differential Pair Clock Lines			
HDMI_HPD	C24	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	
HDMI1_CTRLCLK	D15	I2C_CLK Line for HDMI	I/O OD CMOS		
HDMI1_CTRLDATA	D16	I2C_DAT Line for HDMI	I/O OD CMOS		
DDI1_DDC_AUX_SEL	D34	Strapping Signal to select HDMI or DP output 1M pull-down on the module and floating on the carrier enable DisplayPort mode	I 3.3V	PD 1M	HDMI mode enabled

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4.4.4 DDI2 Port

Name	Pin #	DisplayPort (DP)	HDMI
DDI2_PAIR0+ DDI2_PAIR0-	D39 D40	DP2_LANE0+ DP2_LANE0-	TMDS2_DATA2+ TMDS2_DATA2-
DDI2_PAIR1+ DDI2_PAIR1-	D42 D43	DP2_LANE1+ DP2_LANE1-	TMDS2_DATA1+ TMDS2_DATA1-
DDI2_PAIR2+ DDI2_PAIR2-	D46 D47	DP2_LANE2+ DP2_LANE2-	TMDS2_DATA0+ TMDS2_DATA0-
DDI2_PAIR3+ DDI2_PAIR3-	D49 D50	DP2_LANE3+ DP2_LANE3-	TMDS2_CLK+ TMDS2_CLK-
DDI2_HPD	D44	DP2_HPD	HDMI2_HPD
DDI2_CTRLCLK_AUX+	C32	DP2_AUX+	HMDI2_CTRLCLK
DDI2_CTRLCLK_AUX-	C33	DP2_AUX-	HMDI2_CTRLDATA
DDI2_DDC_AUX_SEL	C34	DDI2_DDC_AUX_SEL	DDI2_DDC_AUX_SEL

Note: Dual Mode (HDMI and DisplayPort on the same pins) implementations may be realized. This is desirable for SOCs that natively implement this capability. With such SOCs, the primary Dual Mode implementation challenge is that the HDMI_CTRL_DAT and HDMI_CTRL_CK lines are DC coupled, but the DP_AUX+ /- pair must be AC coupled. A set of FET switches is usually used to sort this out. The FET gates can be controlled by the AUX_SEL pin function.

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4.4.4.1. DisplayPort (DP) Mode (DDI2)

Name	Pin #	Description	I/O	PU / PD	Comment
DP2_LANE0+ DP2_LANE0- DP2_LANE1+ DP2_LANE1- DP2_LANE2+ DP2_LANE2- DP2_LANE3+ DP2_LANE3-	D39 D40 D42 D43 D46 D47 D49 D50	DP Port 2, differential pair data lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors ***shall*** be placed on the Carrier
DP2_HPD	D44	DP Port 2, detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	Module must tolerate high level in stand-by mode. The carrier board shall include a blocking FET on DP1_HPD to prevent back-drive current from damaging the Module.
DP2_AUX+	C32	DP Port 2, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PD 100K	AC coupled on Module
DP2_AUX-	C33	DP Port 2, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PU 100K 3.3V	AC coupled on Module
DDI2_DDC_AUX_SEL	C34	Strapping Signal to select HDMI or DP output 1M pull-down on the module and floating on the carrier enable DisplayPort mode	I 3.3V	PD 1M	DP mode enabled

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4.4.4.2. HDMI Mode (DDI2)

Name	Pin #	Description	I/O	PU / PD	Comment
TMDS2_DATA2+ TMDS2_DATA2- TMDS2_DATA1+ TMDS2_DATA1- TMDS2_DATA0+ TMDS2DATA0-	D39 D40 D42 D43 D46 D47	HDMI / DVI Port, Differential Pair Data Lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
TMDS2_CLK+ TMDS2_CLK-	D49 D50	HDMI Port, Differential Pair Clock Lines			
HDM2_HPD	D44	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	
HDMI2_CTRLCLK	C32	I2C_CLK Line for HDMI	I/O OD CMOS		
HDMI2_CTRLDATA	C33	I2C_DAT Line for HDMI	I/O OD CMOS		
DDI2_DDC_AUX_SEL	C34	Strapping Signal to select HDMI or DP output 1M pull-down on the module and floating on the carrier enable DisplayPort mode	I 3.3V	PD 1M	HDMI mode enabled

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4.4.5 DDI3 Port

Name	Pin #	DisplayPort (DP)	HDMI
DDI3_PAIR0+ DDI3_PAIR0-	C39 C40	DP3_LANE0+ DP3_LANE0-	TMDS3_DATA2+ TMDS3_DATA2-
DDI3_PAIR1+ DDI3_PAIR1-	C42 C43	DP3_LANE1+ DP3_LANE1-	TMDS3_DATA1+ TMDS3_DATA1-
DDI3_PAIR2+ DDI3_PAIR2-	C46 C47	DP3_LANE2+ DP3_LANE2-	TMDS3_DATA0+ TMDS3_DATA0-
DDI3_PAIR3+ DDI3_PAIR3-	C49 C50	DP3_LANE3+ DP3_LANE3-	TMDS3_CLK+ TMDS3_CLK-
DDI3_HPD	C44	DP3_HPD	HDMI3_HPD
DDI3_CTRLCLK_AUX+	C36	DP3_AUX+	HMDI3_CTRLCLK
DDI3_CTRLCLK_AUX-	C37	DP3_AUX-	HMDI3_CTRLDATA
DDI3_DDC_AUX_SEL	C38	DDI3_DDC_AUX_SEL	DDI3_DDC_AUX_SEL

Note: Dual Mode (HDMI and DisplayPort on the same pins) implementations may be realized. This is desirable for SOCs that natively implement this capability. With such SOCs, the primary Dual Mode implementation challenge is that the HDMI_CTRL_DAT and HDMI_CTRL_CK lines are DC coupled, but the DP_AUX+ /- pair must be AC coupled. A set of FET switches is usually used to sort this out. The FET gates can be controlled by the AUX_SEL pin function.

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4.4.5.1. DisplayPort (DP) Mode (DDI3)

Name	Pin #	Description	I/O	PU / PD	Comment
DP3_LANE0+ DP3_LANE0- DP3_LANE1+ DP3_LANE1- DP3_LANE2+ DP3_LANE2- DP3_LANE3+ DP3_LANE3-	C39 C40 C42 C43 C46 C47 C49 C50	DP Port 3, differential pair data lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors ***shall*** be placed on the Carrier
DP3_HPD	C44	DP Port 3, detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	Module must tolerate high level in stand-by mode. The carrier board shall include a blocking FET on DP1_HPD to prevent back-drive current from damaging the Module.
DP3_AUX+	C36	DP Port 3, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PD 100K	AC coupled on Module
DP3_AUX-	C37	DP Port 3, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PU 100K 3.3V	AC coupled on Module
DDI3_DDC_AUX_SEL	C38	Strapping Signal to select HDMI or DP output 1M pull-down on the module and floating on the carrier enable DisplayPort mode	I 3.3V	PD 1M	DP mode enabled

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4.4.5.2. HDMI Mode (DDI3)

Name	Pin #	Description	I/O	PU / PD	Comment
TMDS3_DATA2+ TMDS3_DATA2- TMDS3_DATA1+ TMDS3_DATA1- TMDS3_DATA0+ TMDS3_DATA0-	C39 C40 C42 C43 C46 C47	HDMI / DVI Port, Differential Pair Data Lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
TMDS3_CLK+ TMDS3_CLK-	C49 C50	HDMI Port, Differential Pair Clock Lines			
HDM3_HPD	C44	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	
HDMI3_CTRLCLK	C36	I2C_CLK Line for HDMI	I/O OD CMOS		
HDMI3_CTRLDATA	C37	I2C_DAT Line for HDMI	I/O OD CMOS		
DDI3_DDC_AUX_SEL	C38	Strapping Signal to select HDMI or DP output 1M pull-down on the module and floating on the carrier enable DisplayPort mode	I 3.3V	PD 1M	HDMI mode enabled

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4.4.6 PCIe Graphics Port (PEG)

Name	Pin #	Description	I/O	PU / PD	Comment
PEG_TX0+ PEG_TX0-	D52 D53	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX0+ PEG_RX0-	C52 C53	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX1+ PEG_TX1-	D55 D56	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX1+ PEG_RX1-	C55 C56	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX2+ PEG_TX2-	D58 D59	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX2+ PEG_RX2-	C58 C59	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX3+ PEG_TX3-	D61 D62	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX3+ PEG_RX3-	C61 C62	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX4+ PEG_TX4-	D65 D66	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX4+ PEG_RX4-	C65 C66	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module

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Name	Pin #	Description	I/O	PU / PD	Comment
PEG_TX5+ PEG_TX5-	D68 D69	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX5+ PEG_RX5-	C68 C69	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX6+ PEG_TX6-	D71 D72	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX6+ PEG_RX6-	C71 C72	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX7+ PEG_TX7-	D74 D75	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX7+ PEG_RX7-	C74 C75	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
~~PEG_LANE_RV#~~	~~D54~~	~~PCI Express Graphics lane reversal input strap. Pull low on the Carrier Board to reverse lane order.~~	~~I 3.3V~~		Not supported

Note: Only lanes 0-7 from the 16 lanes of the PEG port are supported. The available configurations are one x8 or two x4.

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4.4.7 Module Type Definition

Name	Pin #	Description	I/O	PU / PD	Comment
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module. The pins are tied on the Module to either ground (GND) or are no-connects (NC). For Pin-out Type 1 and Type 10 that lack a CD connector, these pins are not present (X) **TYPE2# TYPE1# TYPE0#** X X X Pinout Type 1 X X X Pinout Type 10 NC NC NC Pinout Type 2 NC NC GND Pinout Type 3 NC GND NC Pinout Type 4 NC GND GND Pinout Type 5 GND NC NC Pinout Type 6 GND NC GND Pinout Type 7 The Carrier Board ***should*** implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.	???	???	Type 6
TYPE10#	A97	In case of a type 10 module this pin signal is tied to GND through a 47K resistor on the module.			Not Connected

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4.4.8 Power and Ground

Name	Pin #	Description	I/O	PU / PD	Comment
VCC_12V	C104, C105, C106, C107, C108, C109, D104, D105, D106, D107, D108, D109	Primary power input supports a wide range of 5~ 20V input. All available VCC_12V pins on the connector(s) shall be used.	P		8.5-20 V
GND	C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70, C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path.	P		

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5. Additional Features

This chapter describes connectors, LEDs, switches, and additional items located on the module and not necessarily included in the PICMG standard specification. The locations of these items is as below:

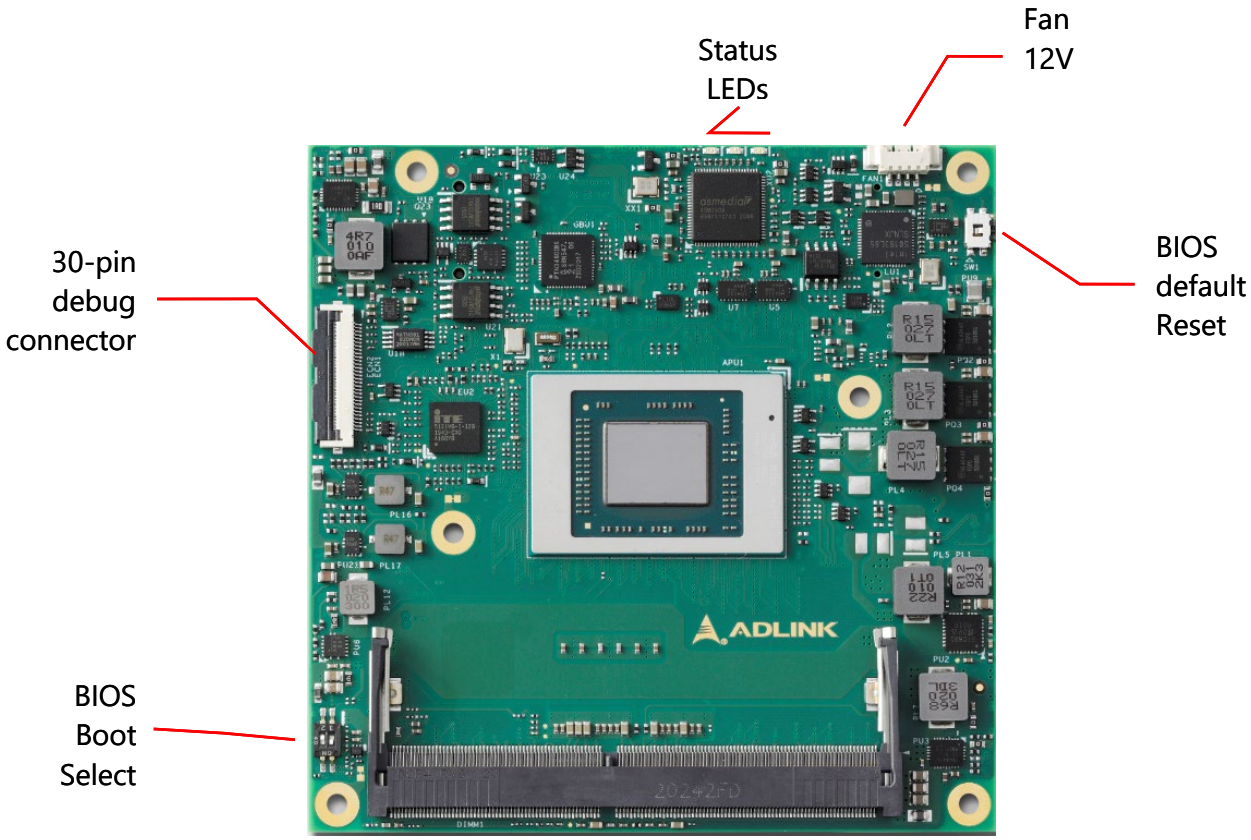


Figure 3 – Module feature locations

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5.1. Debug Connector

This connector is particular useful during carrier design and bring up phase. It offers access to the following critical parts of the module:

- Test points measurement of internal power rails
- I2C bus for BIOS POST code readout
- SPI BIOS programming interface
- Embedded Controller programming interface

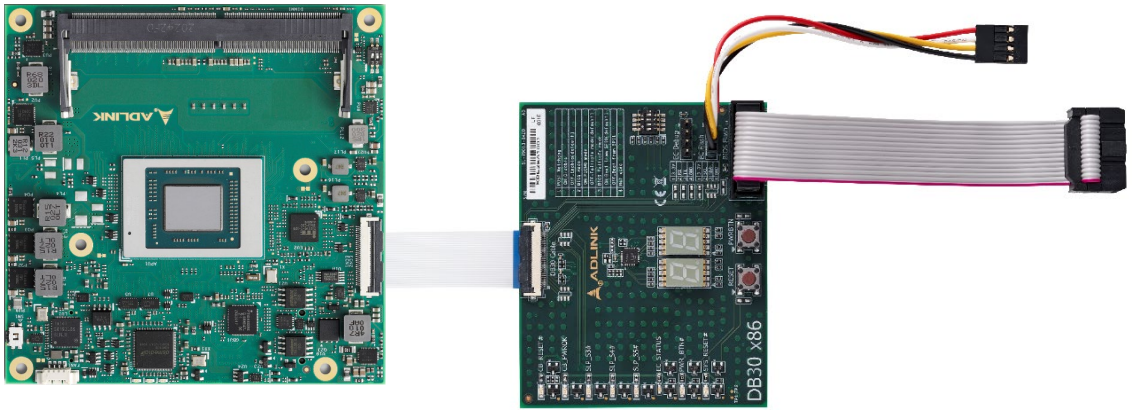


Figure 4 – cExpress-AR and Debug Module

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5.2. Status LEDs

Status LED's are mounted on the module to facilitate easier maintenance.



Name	Color	Connection	Function
LED1	Blue	BMC output	Power Sequence Status Code (BMC) Power Changes, RESET (see Exception Codes Table below)
LED2	Green	Power Source 3Vcc	S0 LED ON S3/S4/S5 LED OFF ECO mode LED OFF
LED3	Red	BMC output and same signal as WDT (B27) on BtB connector	Module power up WD LED = LED OFF Watchdog counting WD LED = Keep Last State Watchdog timed out WD LED = LED ON Watchdog RESET WD LED = LED ON Rebooted after WD RESET WD LED = LED ON Rebooted after PWRBTN WD LED = LED OFF Rebooted after RESET BTN WD LED = LED OFF Note: only a RESET not initiated by the BMC can clear the WD LED (user action)

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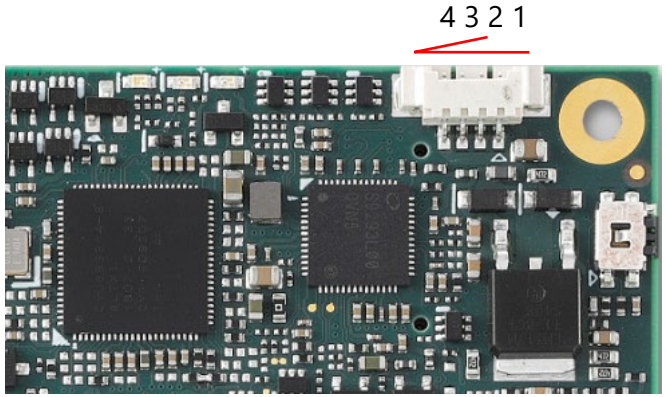
5.3. Exception Codes

Exception Code	Error Message
0	NOERROR
2	NO_SUSCLK
3	NO_SLP_S5
4	NO_SLP_S4
5	NO_SLP_S3
6	BIOS_FAIL
7	RESET_FAIL
8	RESETIN_FAIL
9	NO_CB_PWROK
10	CRITICAL_TEMP
11	POWER_FAIL
12	VOLTAGE_FAIL
13	RFID_MEMFAIL (No Used)
14	NO_VDDQ_PG
15	NO_V1P05A_PG
16	NO_VCORE_PG
17	NO_SYS_GD
18	NO_V5SBY
19	NO_V3P3A
20	NO_V5_DUAL
21	NO_PWRSRC_GD
22	NO_P_5V_3V3_S0_PG
23	NO_SAME_CHANNEL
24	NO_1V2A_PG

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5.4. Fan Connector

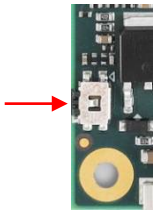
Connector type: JVE 24W1125A-04M00



Name	Description
1	FAN_PWMOUT
2	FAN_TACHIN
3	GND
4	12V

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5.5. BIOS Default Reset Button



To perform a hardware reset of BIOS default settings, perform the following steps:

1. Shut down the system.
2. Keep the BIOS Setup Defaults Reset Button pressed and boot up the system. You can release the button when the BIOS prompt screen appears
3. The BIOS prompt screen will display a confirmation that BIOS defaults have been reset and request that you reboot the system.



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5.6. BIOS Boot Select

The module has two BIOS chips (BOM option) and BIOS operation can be configured to "PICMG" and dual-BIOS "Failsafe" modes using BIOS Select and Mode Configuration Switch, Pin 2.

Setting the module to PICMG mode will configure the BIOS chips on the module as SPI0 and SPI1. In PICMG mode, a BIOS chip cannot be placed in the SPI0 slot on the carrier.

In dual-BIOS Failsafe mode, both BIOS chips on the module are configured as SPI1. Only one of the two is connected to the SPI bus at any given time. In case of failure of the primary SPI1 BIOS, the system will reboot and switch to the secondary SPI1 BIOS on the module. In Failsafe mode, the SPI0 BIOS socket on the carrier can be populated.

In either mode, BIOS Select and Mode Configuration Switch Pin 1 is used to select whether to boot from SPI0 or SPI1.

Mode	Pin 1	Pin 2
Boot from SPI0 (default)	On	-
Boot from SPI1	Off	-
Set BIOS to PICMG mode (default)	-	On
Set BIOS to Failsafe BIOS mode	-	Off

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6. System Resources

6.1 System Memory Map

Address Range (hex)	Description
FEE00000-FFFFFFFF	PCI Express Root Complex
FEDC9000-FEDC9FFF	AMD UART Controller
FEDC7000-FEDC7FFF	AMD UART Controller
FEDC2000-FEDC2FFF	AMD I2C Controller
FEDC0000-FEDC0FFF	Motherboard Resources
FED80000-FED8FFFF	Motherboard Resources
FED00000-FED003FF	High Precision Event Timer
FEC10000-FEC10FFF	Motherboard Resources
FEC01000-FEC01FFF	Motherboard Resources
FEC00000-FEC00FFF	Motherboard Resources
B0000000-FEBFFFFF	PCI Express Root Complex
AC733000-AC776FFF	Trusted Platform Module 2.0
AC76F000-AC772FFF	Trusted Platform Module 2.0
000C0000-000DFFFF	PCI Express Root Complex
000A0000-000BFFFF	PCI Express Root Complex
00000 – FFFFF	DOS Compatibility Memory

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6.2 I/O Map

Hex Range	Device
00h - 0Fh	DMA Controller
20h - 21h	Programmable Interrupt Controller 1
2Eh - 2Fh 4Eh - 4Fh	LPC SIO (W83627DHGSEC / IT5121E) Configuration Index/Data Registers
40h - 43h	System Timer
60h and 64h	8742 Equivalent (Keyboard)
61h	System Speaker
70h - 71h	Real Time Clock Controller
81h - 83h, 87h, 89h - 8Bh and 8Fh	DMA Controller
A0h - A1h	Programmable Interrupt Controller 2
C0h - DFh	DMA Controller
240h - 247h	Serial Port 3 (COM3)
248h - 24Fh	Serial Port 4 (COM4)
2F8h – 2FFh	Serial Port 2 (COM2)
3F8h - 3FFh	Serial Port 1 (COM1)
B00h	SMBUS 0 IO Base
B20h	SMBUS 1 IO Base
CF9h	Reset Generator

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6.3 Interrupt Request (IRQ) Lines

APIC Mode

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
0	High Precision Event Timer/System Timer		No
1	Standard PS/2 Keyboard		No
3	Serial Port 2 / AMD UART Controller		No
4	Serial Port 1		Note (1)
5	Serial Port 3		Note (1)
7	Serial Port 4		Note (1)
8	High Precision Event Timer		Note (1)
10	AMD I2C Controller		No
11	AMD GPIO Controller		Note (1)
36	High Definition Audio Controller		Note (1)
37	AMD Sensor Fusion Hub		Note (1)
39	AMD Audio Coprocessor / High Definition Audio Controller		Note (1)

Note (1): These IRQs can be used for PCI devices when onboard device is disabled.

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6.4 PCI Configuration Space Map

Bus Number	Device Number	Function Number	Routing	Description
00h	24h	00h	N/A	Data Fabric: Device 18h; Function 0
00h	24h	01h	Internal	Data Fabric: Device 18h; Function 1
00h	24h	02h	Internal	Data Fabric: Device 18h; Function 2
00h	24h	03h	Internal	Data Fabric: Device 18h; Function 3
00h	24h	04h	Internal	Data Fabric: Device 18h; Function 4
00h	24h	05h	Internal	Data Fabric: Device 18h; Function 5
00h	24h	06h	Internal	Data Fabric: Device 18h; Function 6
00h	24h	07h	Internal	Data Fabric: Device 18h; Function 7
00h	00h	00h	Internal	Root Complex
00h	00h	02h	Internal	IOMMU
00h	01h	00h	Internal	PCIe® Dummy Host Bridge
00h	01h	01h	Internal	PCIe® GPP Bridge 0
00h	01h	02h	Internal	PCIe® GPP Bridge 1
00h	01h	03h	Internal	PCIe® GPP Bridge 2
00h	02h	00h	Internal	PCIe® Dummy Host Bridge
00h	02h	01h	Internal	PCIe® GPP Bridge 0
00h	02h	02h	Internal	PCIe® GPP Bridge 1
00h	02h	03h	Internal	PCIe® GPP Bridge 2
00h	02h	04h	Internal	PCIe® GPP Bridge 3
00h	02h	06h	Internal	PCIe® GPP Bridge 5
00h	02h	07h	Internal	PCIe® GPP Bridge 6

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Bus Number	Device Number	Function Number	Routing	Description
00h	08h	00h	Internal	PCIe® Dummy Host Bridge
00h	08h	01h	Internal	Internal PCIe® GPP Bridge 0 to Bus A
00h	08h	02h	Internal	Internal PCIe® GPP Bridge 1 to Bus B
00h	08h	03h	Internal	Internal PCIe® GPP Bridge 2 to Bus C
0Ah	00h	00h	Internal	PCIe® Dummy Function
0Ah	00h	02h	Internal	Cryptographic Coprocessor (PSP/CCP)
0Ah	00h	03h	Internal	USB3.1 (USB0)
0Ah	00h	04h	Internal	USB3.1 (USB1)
0Ah	00h	05h	Internal	Audio Processor (ACP)
0Ah	00h	06h	Internal	Audio Processor – HD Audio Controller (Standalone AZ)
0Ah	00h	07h	Internal	Sensor Fusion Hub (MP2) / Non-Sensor Fusion Hub device (MP2)
0Bh	00h	00h	Internal	PCIe® Dummy Function /SATA AHCI Mode with MS Driver support / SATA AHCI Mode with AMD driver support
00h	20h	00h	Internal	SMBus Controller
0Bh	00h	01h	Internal	SATA Controller; SATA Raid/AHCI Mode / SATA Raid AHCI Mode for second vendor
0Bh	00h	02h	Internal	10 GbE Controller Port 0 (XGBE0)
0Bh	00h	03h	Internal	10 GbE Controller Port 1 (XGBE1)
0Ch	00h	00h	Internal	PCIe® Dummy Function
0Ch	00h	02h	Internal	I2S/AC'97 Audio
0Ah	00h	00h	Internal	Internal GPU (GFX)
0Ah	00h	01h	Internal	Display HD Audio Controller (GFXAZ)

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6.5 PCI Interrupt Routing Map

INT Line	P.E.G. Root Port	IGFX	Lpc Bridge	HD Audio Controller	SMBus	SATA Controller
Int0	INTA:32	INTG:38	INTA:16	INTG:38	INTA:16	INTC:34
Int1	INTB:33	INTH:39	INTB:17	INTH:39	INTB:17	INTD:35
Int2	INTC:34	INTE:36	INTC:18	INTE:36	INTC:18	INTA:32
Int3		INTF:37	INTD:19	INTF:37	INTD:19	INTB:33

INT Line	XHCI Controller				
Int0	INTG:38				
Int1	INTH:39				
Int2	INTE:36				
Int3	INTF:37				

INT Line	PCIE Port1	PCIE Port 2	PCIE Port 3	PCIE Port 4	PCIE Port 5	PCIE Port 6	PCIE Port 7	PCIE Port 8
Int0	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Int1	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Int2	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Int3	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

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6.6 SMBus Address Table

Device	Address
DDR4 Channel A(SO-DIMM1)	A0h
DDR4 Channel B(SO-DIMM2)	A4h
SEMA(EC)	50h
PCIE Switch (ASM 2806i)	69h
Thermal Sensor	92h
NXP (eDP to LVDS transmitter)	C0h

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7. BIOS Setup

7.1 Menu Structure

This section presents the six primary menus of the BIOS Setup Utility. Use the following table as a quick reference for the contents of the BIOS Setup Utility. The subsections in this section describe the submenus and setting options for each menu item. The default setting options are presented in **bold**, and the function of each setting is described in the right-hand column of the respective table.

Main	Advanced	Chipset	Security	Boot	Save & Exit
BIOS Information System Information Board Information► System Date System Time	CPU Configuration► Graphics Configuration► Power Management► System Management► Thermal Management► Watchdog Timer► Super IO Configuration► Miscellaneous► Serial Port Console Redirection► Trusted Computing► AMD fTPM configuration► Network Stack Configuration► PCI Subsystem Settings► USB Configuration► NVME Configuration► PCI/PCIe Configuration► SATA Configuration► RAM Disk Configuration► AMD CBS► AMD PBS► Intel Ethernet Controller►	South Bridge► GFX Configuration► North Bridge►	Password Description Secure Boot Menu►	Boot Configuration	Save Options Default Options Boot Override

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Notes: ► indicates a submenu
Gray text indicates info only

7.2 Main

The Main Menu provides read-only information about your system and also allows you to set the System Date and Time. Refer to the tables below the screen shot of this menu for details of the submenus and settings.

7.2.1 BIOS Information

Feature	Options	Description
BIOS Vender	Info only	American Megatrends
BIOS Version	Info only	Display Core Version
Build Date	Info only	Display Compliancy Information
AGESA Version	Info only	Display Compliancy Information
GOP Driver Version	Info only	ADLINK BIOS Version.
BIOS Boot Source	Info only	SPI Boot Source

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7.2.2 System Information

Board Information	Info only	Description
Project Name	Info only	Display Project Name.
CPU Board Version	Info only	Display CPU Signature.
CPU Brand String	Info only	Display CPU Brand Name.
CPU Frequency	Info only	Display CPU Frequency.
Total Memory	Info only	Display installed memory size.
Memory Frequency	Info only	Display memory frequency.

7.2.3 Board Information

Board Information	Info only	Description
SEMA Firmware version	Read only	Display SEMA Firmware version
Serial Number	Read only	Display SMC serial number
Manufacturing Date	Read only	Display SMC manufacturing date.
Last Repair Date	Read only	Display SMC last repair date.
MAC ID	Read only	Display SMC MAC ID.
Runtime Statistics	Info only	
Total Runtime	Read only	The returned value specifies the total time in minutes the system is running in S0 state.
Current Runtime	Read only	The returned value specifies the time in seconds the system is running in S0 state. This counter is cleared when the system is removed from the external power supply.
Power Cycles	Read only	The returned value specifies the number of times the external power supply has been shut down.
Boot Cycles	Read only	The Bootcounter is increased after a HW- or SW-Reset or after a successful power-up.

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Board Information	Info only	Description
Boot Reason	Read only	The boot reason is the event which causes the reboot of the system.

7.2.4 System Date and Time

Feature	Options	Description
System Date	Weekday, MM/DD/YYYY	Requires the alpha-numeric entry of the day of the week, day of the month, calendar month, and all 4 digits of the year, indicating the century and year (Fri XX/XX/20XX).
System Time	HH/MM/SS	Presented as a 24-hour clock setting in hours, minutes, and seconds.
Access Level	Info only	

7.3 Advanced

This menu contains the settings for most of the user interfaces in the system

7.3.1 CPU Configuration

Feature	Options	Description
PSS support	Disabled **Enabled**	Enable/disable the generation of ACPI _PPC, _PSS, and _PCT objects.
NX Mode	Disabled **Enabled**	Enable/disable No-execute page protection Function.
SVM Mode	Disabled **Enabled**	Enable/disable CPU Virtualization
Node 0 Information	Info only	Display the information of process.

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7.3.2 Graphic Configuration

Feature	Options	Description
NXP configuration	Info only	
Data format and Color Depth	VESA 24 bpp JEIDA 24 bpp **JEIDA/vesa 18 bpp**	Data format and Color Depth select
LVDS Output Mode	Dual LVDS bus **Single LVDS bus**	Single/Dual mode select.
DE Polarity	**Active High** Active Low	DE Polarity select.
Vsync Polarity	**Active High** Active Low	Vsync Polarity select.
Hsync Polarity	**Active High** Active Low	Hsync Polarity select.
Spreading depth	**No Spreading** 0.5% 1.0% 1.5% 2.0% 2.5%	Clock frequency center spreading depth.
Integrated Display Configuration	Info only	
eDP/LVDS	**Disable** Enable	Enable/Disable eDP/LVDS
DDI port 1	Disable **Display Port** HDMI	DDI port 1 function choose to Display Port or HDMI.
DDI port 2	**Disable**	DDI port 2 function choose to Display Port or

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	Display Port HDMI	HDMI.
DDI port 3	**Disable** Display Port HDMI	DDI port 3 function choose to Display Port or HDMI.

7.3.3 Power Management

Feature	Options	Description
Power Management	Info only	
Enable ACPI Auto Configuration	**Disabled** Enabled	Enables or Disables BIOS ACPI Auto Configuration.
ACPI Sleep State	Suspend Disabled **S3 (Suspend to RAM)**	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
LID Function	**Disabled** Enabled	Enable/Disable LID Function
Sleep Function	Disabled **Enabled**	Enable/Disable Sleep Button Function
ECO Mode	**Disabled** Enabled	Reduces the power consumption of the system, but after a shut down, you have to wait at least 5 seconds before you can restart the system.
Power-Up Mode	**Turn On** Remain Off Last State	Turn On: The machine starts automatically when the power supply is turned on. Remain off: To start the machine the power button has to pressed. Last State: The machine will power up to last power state

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Feature	Options	Description
ATTENTION: The Power-Up Mode only has effect, if the module is in ATX-Mode.	Info only	
Power Consumption	Submenu	

7.3.3.1 Power Management > Power Consumption

Feature	Options	Description
Power Consumption	Info only	
Main Current	Read only	Display input current.
Current Input Power	Read only	Display input power.
VRTC	Read only	Display actual voltage of the VRTC.
V5VSB	Read only	Display actual voltage of the V5VSB.
VIN	Read only	Display actual voltage of the VIN.
V3.3S	Read only	Display actual voltage of the V3.3S.
VMEM	Read only	Display actual voltage of the VMEM.
V3V3_A	Read only	Display actual voltage of the V3V3_A.
VCORE	Read only	Display actual voltage of the VCORE.

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7.3.4 System Management

Feature	Options	Description
System Management	Info only	
SEMA Firmware Version	Info only	
SEMA Flags	Submenu	
SEMA Features	Info only	
Uptime & Power Cycles Counter	Read only	
System Restart Event	Read only	
4096 Bytes User-Flash	Read only	
Runtime Watchdog	Read only	
Temperatures	Read only	
Voltage Monitor	Read only	
Display Backlight Control	Read only	
Power-up Watchdog	Read only	
Power Monitor (Current Sense)	Read only	
Boot Counter	Read only	
Dual-BIOS	Read only	
I2C Bus 1	Read only	
I2C Bus 2	Read only	
CPU Fan	Read only	
System Fan 1	Read only	
AT/ATX Mode	Read only	
ACPI Thermal Trigger	Read only	

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Feature	Options	Description
Power-up to Last State	Read only	
Backlight Restore	Read only	
Ext - GPIO	Read only	
I2C Bus 3	Read only	
Other BMC	Read only	
Error Log	Read only	
Wake-by-BMC	Read only	
Soft Fan	Read only	
Parameter Memory	Read only	
Ext-GPIO Input Interrupt Support	Read only	

7.3.4.1 System Management > SEMA Flags

Feature	Options	Description
SEMA Flags	Info only	
BMC Flags	Read only	
BIOS Select	Read only	
ATX/AT-Mode	Read only	

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7.3.5 Thermal Management

Feature	Options	Description
Active Cooling Trip Point	Disable 40 C 50 C 60 C 70 C **Refer to BMC**	This value is the temperature threshold of the active cooling trip point.
Passive Cooling Trip Point	**Disable** 70 C 80 C 90 C	This value is the temperature threshold of the passive cooling trip point.
Critical Trip Point	**Disable** 80 C 90 C 95 C	This value is the temperature threshold of the critical trip point.
Watchdog ACPI Event Shutdown	**Disabled** Enabled	Watchdog ACPI Event Shutdown Enabled/Disabled
Temperatures and Fan Speed	Info only	
CPU Temperature	Info only	
Current	Read only	
Startup	Read only	
Min	Read only	
Max	Read only	
Board Temperatures	Info only	
Current	Read only	
Startup	Read only	

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Feature	Options	Description
Min	Read only	
Max	Read only	
CPU Fan Speed	Read only	
Smart Fan	Submenu	

7.3.5.1 Thermal Management > Smart Fan

Feature	Options	Description
Smart Fan	Info only	
CPU Smart FanTemperature Source	**CPU Sensor** Board Sensor	CPU Smart FanTemperature Source.
CPU Fan Mode	**AUTO (Smart Fan)** Fan Off Fan On	CPU Fan Mode
Trigger Point 1	Info only	
Trigger Temperature	40	Trigger Temperature
PWM Level	40	PWM Level
Trigger Point 2	Info only	
Trigger Temperature	50	Trigger Temperature
PWM Level	60	PWM Level
Trigger Point 3	Info only	
Trigger Temperature	60	Trigger Temperature
PWM Level	63	PWM Level
Trigger Point 4	Info only	

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Feature	Options	Description
Trigger Temperature	70	Trigger Temperature
PWM Level	100	PWM Level

7.3.6 Watchdog Timer

Feature	Options	Description
Watchdog Timer	**Info only**	
Power-Up watchdog	**Disabled** Enabled	The Power Up Watchdog resets the system after a certain amount of time after power up. Press F12 during start up disables the Power Up Watchdog.
ATTENTION: Pressing F12 during start up disables the Power Up Watchdog.	Info only	
RunTime Watchdog	**Disabled** Enabled	The RunTime Watchdog resets the system after a certain amount of time after power up.

7.3.7 Super IO Configuration

Feature	Options	Description
Super IO Configuration	Info only	
ITE5121 Super IO Configuration	submenu	
W83627DHGSEC Super IO Configuration	submenu	

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7.3.7.1 Super IO Configuration > ITE5121 Super IO Configuration

Feature	Options	Description
IT5121E Super IO Configuration	Info only	
Super IO Chip	Info only	
Serial Port 1 Configuration	submenu	
Serial Port 2 Configuration	submenu	

7.3.7.2 Super IO Configuration > W83627DHGSEC Super IO Configuration

Feature	Options	Description
W83627DHGSEC Super IO Configuration	Info only	
Super IO Chip	Info only	
Serial Port 1 Configuration	submenu	
Serial Port 2 Configuration	submenu	

7.3.7.3 Super IO Configuration > ITE5121 Super IO Configuration > Serial Port 1 Configuration

Feature	Options	Description
Serial Port 1 Configuration	Info only	
Serial Port 1 Configuration	**Enabled** Disabled	Enable or Disable Serial Port (COM).
Device Settings	IO=3F8h; IRQ=4	Fixed configuration of serial port.
Change Settings	**Auto**	Select an optimal setting for Super IO device.

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Feature	Options	Description
	IO=3F8h; IRQ=4 IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12	
Change Settings	**Normal** High Speed	Select an optimal setting for Super IO Device.

7.3.7.4 Super IO Configuration > ITE5121 Super IO Configuration > Serial Port 2 Configuration

Feature	Options	Description
Serial Port 2 Configuration	Info only	
Serial Port 2 Configuration	**Enabled** Disabled	Enable or Disable Serial Port (COM).
Device Settings	IO=2F8h; IRQ=3	Fixed configuration of serial port.
Change Settings	**Auto** IO=2F8h; IRQ=3 IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12	Select an optimal setting for Super IO device.

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7.3.7.5 Super IO Configuration > W83627DHGSEC Super IO Configuration > Serial Port 1 Configuration

Feature	Options	Description
Serial Port 1 Configuration	Info only	
Serial Port	**Enabled** Disabled	Enable or Disable Serial Port (COM).
Device Settings	IO=240h; IRQ=5	Fixed configuration of serial port.
Change Settings	**Auto** IO=240h; IRQ=10 IO=240h; IRQ=3,4,5,6,7,10,11,12 IO=248h; IRQ=3,4,5,6,7,10,11,12 IO=250h; IRQ=3,4,5,6,7,10,11,12 IO=258h; IRQ=3,4,5,6,7,10,11,12 IO=260h; IRQ=3,4,5,6,7,10,11,12 IO=268h; IRQ=3,4,5,6,7,10,11,12	Select an optimal setting for Super IO device.

7.3.7.6 Super IO Configuration > W83627DHGSEC Super IO Configuration > Serial Port 2 Configuration

Feature	Options	Description
Serial Port 2 Configuration	Info only	
Serial Port	**Enabled** Disabled	Enable or Disable Serial Port (COM).
Device Settings	IO=248h; IRQ=7	Fixed configuration of serial port.
Change Settings	**Auto** IO=248h; IRQ=10	Select an optimal setting for Super IO device.

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Feature	Options	Description
	IO=240h; IRQ=3,4,5,6,7,10,11,12 IO=248h; IRQ=3,4,5,6,7,10,11,12 IO=250h; IRQ=3,4,5,6,7,10,11,12 IO=258h; IRQ=3,4,5,6,7,10,11,12 IO=260h; IRQ=3,4,5,6,7,10,11,12 IO=268h; IRQ=3,4,5,6,7,10,11,12	
Device Mode	**Standard Serial Port Mode** IrDA Active pulse 1.6 uS IrDA Active pulse 3/16 bit time ASKIR Mode	Change the Serial Port mode.

7.3.8 Miscellaneous

Feature	Options	Description
Miscellaneous	Info only	
Power Supply Unit	Emulate AT Mode **ATX Mode**	ATX: OS will turn off system power when shutdown. NOTE: AT mode will not support S3 & S4 & S5, so it will change Power Loss State to Power On.
I2C Speed Control	**100 Kbps** 400 Kbps	I2C Speed Control
WOL From S5	OFF **ON**	This Config to control power on/off LAN in S5 State by SEMA(EC).
Smart Battery Function	**Disabled** Enabled Auto	Enable/Disable Smart Battery function. Auto: disable Smart Battery function if charger IC not be detected.

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7.3.9 Serial Console Redirection

Feature	Options	Description
Serial Port Console	Info only	
COM0	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	
COM1	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	
COM2	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	
COM3	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	
Serial Port for Out-of-Band Management/	Info only	
Windows Emergency Management Services (EMS)	Info only	
Console Redirection EMS	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	

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7.3.9.1 Serial Port Console > Console Redirection Settings

Feature	Options	Description
COM0	Info only	
Console Redirection Settings	Info only	
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7 **8**	Data Bits.
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: The parity bit is 0 if the num of 1's in the data bits is even. Odd: The parity bit is 0 if num of 1's in the data bits is odd. Mark: The parity bit is always 1. Space: The parity bit is always 0. Mark and Space Parity bits do not allow for error detection.
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
VT-UTF8 Combo Key Support	Disabled **Enable**	Enables VT-UTF8 Combination Key Support for ANSI/VT100 terminals.
Recorder Mode	**Disabled** Enable	With this mode enabled only text will be sent. This is to capture Terminal data.

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Feature	Options	Description
Resolution 100x31	**Disabled** Enable	Enables or disables extended terminal resolution
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Selects FunctionKey and KeyPad on Putty.

7.3.9.2 Serial Port Console > Console Redirection Settings

Feature	Options	Description
Out-of-Band Mgmt Port	**COM0** COM1 COM2 COM3	Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.
Terminal Type EMS	VT100 VT100+ **VT-UTF8** ANSI	VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Flow Control	**None** Hardware RTS/CTS Software Xon/Xoff	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.

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Feature	Options	Description
Data Bits EMS	**8**	
Parity EMS	**None**	
Stop Bits EMS	**1**	

7.3.10 Trusted Computing

Feature	Options	Description
TPM 2.0 Device Found	Info only	
Firmware Version	Info only	
Vendor	Info only	
Security Device Support	**Disabled** Enabled	Security Device Support
Active PCR banks	Info only	
Available PCR banks	Info only	
SHA-1 PCR Bank	Disabled **Enabled**	Enable or Disable SHA-1 PCR Bank
SHA256 PCR Bank	Disabled **Enabled**	Enable or Disable SHA256 PCR Bank
Pending operation	**None** TPM Clear	Pending operation
Platform Hierarchy	Disabled **Enabled**	Enable or Disable Platform Hierarchy
Storage Hierarchy	Disabled **Enabled**	Enable or Disable Storage Hierarchy
Endorsement Hierarchy	Disabled	Enable or Disable Endorsement Hierarchy

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Feature	Options	Description
	Enabled	
TPM 2.0 UEFI Spec Version	TCG_1_2 **TCG_2**	Select the TCG2 Spec Version Support,\n\r\n\rTCG_1_2: the Compatible mode for Win8/Win10,\n\r\n\rTCG_2: Support new TCG2 protocol and event format for Win10 or later
Physical Presence Spec Version	1.2 **1.3**	Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.
TPM 2.0 InterfaceType	Info only	Select the Communication Interface to TPM 20 Device.
Device Select	TPM 1.2 TPM 2.0 **Auto**	TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated
Disable Block Sid	**Disabled** Enabled	Override to allow SID authentication in TCG Storage device

7.3.11 AMD fTPM Configuration

Feature	Options	Description
AMD fTPM switch	**AMD CPU fTPM** Route to LPC TPM	To select. 0: AMD CPU fTPM. 1: AMD CPU fTPM Disabled.
Erase fTPM NV for factory reset	Disabled **Enabled**	When New CPU is installed, Select \"Enabled\" to reset fTPM, if you have BitLocker or encryption-enabled system, the system will not boot without a recovery key. Select \"Disabled\" to keep previous fTPM record and continue system boot, fTPM will NOT be enabled with new CPU unless fTPM is reset (reinitialized), you could swap back to the old CPU to recover TPM related keys and data.

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7.3.12 Network Stack Configuration

Feature	Options	Description
Network Stack Configuration	Info only	Enable/Disable UEFI Network Stack
Network Stack	**Disabled** Enabled	Enable/Disable UEFI network stack.
Ipv4 PXE Support	**Disabled** Enabled	Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.
IPv4 HTTP Support	**Disabled** Enabled	Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.
Ipv6 PXE Support	**Disabled** Enabled	Enable/Disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.
IPv6 HTTP Support	**Disabled** Enabled	Enable/Disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.
PXE boot wait time	**0**	Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.
Media detect count	**1**	Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

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7.3.13 PCI Subsystem Settings

Feature	Options	Description
PCI Bus Driver Version	Info only	
PCI Devices Common Settings	Info only	
PCI Latency Timer	**32 PCI Bus Clocks** 64 PCI Bus Clocks 96 PCI Bus Clocks 128 PCI Bus Clocks 160 PCI Bus Clocks 192 PCI Bus Clocks 224 PCI Bus Clocks 248 PCI Bus Clocks	Value to be programmed into PCI Latency Timer Register.
PCI-X Latency Timer	32 PCI Bus Clocks **64 PCI Bus Clocks** 96 PCI Bus Clocks 128 PCI Bus Clocks 160 PCI Bus Clocks 192 PCI Bus Clocks 224 PCI Bus Clocks 248 PCI Bus Clocks	Value to be programmed into PCI Latency Timer Register.
VGA Palette Snoop	**Disabled** Enabled	Enables or Disables VGA Palette Registers Snooping.
PERR# Generation	**Disabled** Enabled	Enables or Disables PCI Device to Generate PERR#.
SERR# Generation	**Disabled** Enabled	Enables or Disables PCI Device to Generate SERR#.
Above 4G Decoding	**Disabled** Enabled	Enables or Disables 64bit capable Devices to be Decoded in Above 4G Address Space (Only if System Supports 64-bit PCI Decoding).
SR-IOV Support	**Disabled**	If system has SR-IOV capable PCIe Devices, this option Enables or Disables Single Root IO Virtualization

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Feature	Options	Description
	Enabled	Support.
BME DMA Mitigation	**Disabled** Enabled	Re-enable Bus Master Attribute disabled during Pci enumeration for PCI Bridges after SMM Locked
PCI Express Settings	submenu	

7.3.13.1. PCI Subsystem Settings > PCI Express Settings

Feature	Options	Description
PCI Express Device Register Settings	Info only	
Relaxed Ordering	Disabled **Enabled**	Enables or Disables PCI Express Device Relaxed Ordering.
Extended Tag	**Disabled** Enabled	If ENABLED allows Device to use 8-bit Tag field as a requester.
No Snoop	Disabled **Enabled**	Enables or Disables PCI Express Device No Snoop option.
Maximum Payload	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.
Maximum Read Request	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes	Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value.

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Feature	Options	Description
	4096 Bytes	
PCI Express Link Register Settings. ARNING: Enabling ASPM may cause some PCI-E devices to fail	Info only	
Extended Synch	**Disabled** Enabled	If ENABLED allows generation of Extended Synchronization patterns.
Link Training Retry	Disable 2 3 **5**	Defines number of Retry Attempts software will take to retrain the link if previous training attempt was unsuccessful.
Link Training Timeout (uS)	**1000**	Defines number of Microseconds software will wait before polling 'Link Training' bit in Link Status register. The value range is from 10 to 10000 uS.
Unpopulated Links	**Keep Link ON** Disable Link	In order to save power, software will disable unpopulated PCI Express links, if this option set to 'Disable Link'.

7.3.14 USB Configuration

Feature	Options	Description
USB Configuration	Info only	
USB Module Version	Info only	
USB Controllers:	Info only	
USB Devices:	Info only	
Legacy USB Support	Disabled **Enabled**	Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
XHCI Hand-off	Disabled **Enabled**	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

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Feature	Options	Description
USB Mass Storage Device Configuration	Disabled **Enabled**	Configure the USB Mass Storage Devices.
USB hardware delays and time-outs	Info only	
USB transfer time-out	1 sec 5 sec 10 sec **20 sec**	The time-out value for Control, Bulk, and Interrupt transfers.
Device reset time-out	10 sec **20 sec** 30 sec 40 sec	USB mass storage device Start Unit command time-out.
Device power-up delay	**Auto** Manual	Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.
Mass Storage Devices	Info only	

7.3.15 NVME Configuration

Feature	Options	Description
NVME Configuration	Info only	

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7.3.16 PCI/PCIe Configuration

Feature	Options	Description
PCI/PCIe Configuration	Info only	
GFX Configuration	**1X8** 2X4	To set the GFX Configuration
PCIE Ports 1-4 Configuration	**1X4 Port** 2X1 1X2 Port 1X2 2X1 Port 2X2 Port	To set PCIE Ports 1-4 Configuration
PCI Express Gen Speed	**Auto** Gen 3 Gen 2 Gen 1	Select PCI Express Gen speed
PCI Express Root Port 0(COMe Lane 4)	Disabled **Enabled**	Enable/Disable PCI Express root port 0
PCI Express Root Port 4(COMe Lane 2	Disabled **Enabled**	Enable/Disable PCI Express root port 4
PCI Express Root Port 6	**Disabled** Enabled	
PCI Express Root Port 7	**Disabled** Enabled	

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7.3.17 SATA Configuration

Feature	Options	Description
SATA MAXGEN2 CAP Option	Disabled **Enabled**	Set SATA Max Gen2 Mode

7.3.18 RAM Disk Configuration

Feature	Options	Description
Disk Memory Type	**Boot Service Data** Reserved	Specifies type of memory to use from available memory pool in system to create a disk.
Create raw	submenu	Create a raw RAM disk.
Create from file		Create a RAM disk from a given file.
Created RAM disk list	Info only	
Remove selected RAM disk(s)		Remove selected RAM disk(s)

7.3.18.1 RAM Disk Configuration > Create raw

Feature	Options	Description
Size (Hex)	**1**	The valid RAM disk size should be multiples of the RAM disk block size.
Create & Exit		Create a new RAM disk with the given starting and ending address.
Discard & Exit		Discard and exit.

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7.3.19 AMD CBS

Feature	Options	Description
AMD CBS	Info only	
CPU Common Options	submenu	CPU Common Options
DF Common Options	submenu	DF Common Options
UMC Common Options	submenu	UMC Common Options
NBIO Common Options	submenu	NBIO Common Options
FCH Common Options	submenu	FCH Common Options
Soc Miscellaneous Control	submenu	Soc Miscellaneous Control

7.3.19.1 AMD CBS > CPU Common Options

Feature	Options	Description
Performance	submenu	Performance
Prefetcher Settings	submenu	Prefetcher settings
Core Watchdog	submenu	Prefetcher settings
RedirectForReturnDis	**Auto** 0 1	From a workaround for GCC/C000005 issue for XV Core on CZ A0, setting MSRC001_1029 Decode Configuration (DE_CFG) bit 14 [DecfgNoRdrctForReturns] to 1
Platform First Error Handling	Enable Disable **Auto**	Enable/disable PFEH, cloak individual banks, and mask deferred error interrupts from each bank.
Core Performance Boost	Disable **Auto**	Disable CPB
Global C-State Control	Enable	Controls IO based C-state generation and DF C-states.\nThere is another DF Cstate option which will be synchronized with this option if DF Cstate option is auto.

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Feature	Options	Description
	Disable **Auto**	
Opcache Control	Enable Disable **Auto**	Enables or disables the Opcache
SEV ASID Count	253 ASIDs 509 ASIDs **Auto**	This fields specifies the maximum valid ASID, which affects the maximum system physical address space. 16TB of physical address space is available for systems that support 253 ASIDs, while 8TB of physical address space is available for systems that support 509 ASIDs.
SEV-ES ASID Space Limit Control	**Auto** Manual	No help string
Streaming Stores Control	Enable Disable **Auto**	Enables or disables the streaming stores functionality
Local APIC Mode	xAPIC x2APIC **Auto**	No help string
ACPI _CST C1 Declaration	Enable Disable **Auto**	Determines whether or not to declare the C1 state to the OS.
MCA Error Thresh Enable	False **True**	Enable MCA error thresholding.
MCA Error Thresh Count	**ff5**	Effective error threshold count = 4095(0xFFF) - <this value> (e.g., the default value of 0xFF5 results in a threshold of 10).
SMU and PSP Debug Mode	Enable Disable **Auto**	When this option is enabled, specific uncorrected errors detected by the PSP FW or SMU FW will hang and not reset the system
PPIN Opt-In	Enable Disable	Turn on PPIN feature

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Feature	Options	Description
	Auto	

7.3.19.1.1 AMD CS > CPU Common Options > Performance

Feature	Options	Description
Performance	Info only	
Custom Core Pstate	submenu	

7.3.19.1.2 AMD CBS > CPU Common Options > Prefetcher settings

Feature	Options	Description
Prefetcher settings	Info only	
L1 Stream HW Prefetcher	Enable Disable **Auto**	Option to Enable | Disable L1 Stream HW Prefetcher
L2 Stream HW Prefetcher	Enable Disable **Auto**	Option to Enable | Disable L2 Stream HW Prefetcher

7.3.19.1.3 AMD CBS > CPU Common Options > Core Watchdog

Feature	Options	Description
Core Watchdog Timer Enable	Enable Disable **Auto**	Enable or disable CPU Watchdog Timer

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7.3.19.2 AMD CBS > DF Common Options

Feature	Options	Description
DF Common Options	Info only	
Scrubber	submenu	
Memory Addressing	submenu	
CC6 Memory Region Encryption	Enable Disable **Auto**	Control whether or not the CC6 save/restore memory is encrypted
Memory Clear	Enable Disable **Auto**	When this feature is disabled, BIOS does not implement MemClear after memory training (only if non-ECC DIMMs are used).
Disable DF to External Downstream IP SyncFloodPropagation	Sync flood disabled Sync flood enabled **Auto**	Disables Error propagation to UMC or any downstream slaves eg. FCH. Use this to avoid reset in failure scenario
Disable DF Sync Flood Propagation	Sync flood disabled Sync flood enabled **Auto**	Control DF::PIEConfig[DisSyncFloodProp]\nDisables propagation from PIE to other DF components and eventually to SDP ports
Freeze DF Module Queues on Error	Enable Disable **Auto**	Disabling this option sets DF:DfGlobalCtrl[DisImmSyncFloodOnFatalError]\nEnables freezing of all DF queues on error and also forces a sync flood on HWA even if MCAs are disabled
DF Cstates	Enable Disable **Auto**	When DF Cstate feature is enabled, FW programs the registers required to enable this feature is the DF HW. (For auto option, it means this option will synchronized with Global C State.)

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7.3.19.2.1 AMD CBS > DF Common Options > Scrubber

Feature	Options	Description
Scrubber	Info only	
DRAM scrub time	Disable 1 hour 4 hours 8 hours 16 hours 24 hours 48 hours **Auto**	Provide a value that is the number of hours to scrub memory.
Poison scrubber control	Enable Disable **Auto**	Control DF::RedirScrubCtrl[RedirScrubMode[1]]
Redirect scrubber control	Enable Disable **Auto**	Control DF::RedirScrubCtrl[RedirScrubMode[0]]
Redirect scrubber limit	Enable Disable **Auto**	Controls the number of redirect scrubs allowed at any one time (DF::RedirScrubCtrl[RedirScrubReqLmt])

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7.3.19.2.2 AMD CBS > DF Common Options > Memory Addressing

Feature	Options	Description
Memory Addressing	Info only	
Memory interleaving	Disable **Auto**	Allows for disabling memory channel interleaving.
Memory interleaving size	256 Bytes 512 Bytes 1 KB 2 KB **Auto**	Controls the memory interleaving size. The valid values are AUTO, 256 bytes, 512 bytes, 1 Kbytes or 2Kbytes. This determines the starting address of the interleave (bit 8, 9, 10 or 11).
DRAM map inversion	Enable Disable **Auto**	Inverting the map will cause the highest memory channels to get assigned the lowest addresses in the system.

7.3.19.3 AMD CBS > DF Common Options > UMC Common Options

Feature	Options	Description
UMC Common Options	Info only	
DDR4 Common Options	submenu	DDR4 Common Options
DRAM Memory Mapping	submenu	DRAM Memory Mapping
Phy Configuration	submenu	Phy Configuration
NVDIMM	submenu	NVDIMM
Memory MBIST	submenu	Memory MBIST

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7.3.19.3.1 AMD CBS > DF Common Options > UMC Common Options > DDR4 Common Options

Feature	Options	Description
DDR4 Common Options	Info only	
DRAM Timing Configuration	submenu	DRAM Timing Configuration
DRAM Controller Configuration	submenu	DRAM Controller Configuration
CAD Bus Configuration	submenu	CAD Bus Configuration
Data Bus Configuration	submenu	Data Bus Configuration
Common RAS	submenu	Common RAS
Security	submenu	Security

7.3.19.3.1.1 AMD CBS > DF Common Options > UMC Common Options > DDR4 Common Options > DRAM Controller Configuration

Feature	Options	Description
DRAM Controller Configuration	Info only	
DRAM Power Options	submenu	DRAM Power Options
Cmd2T	1T 2T **Auto**	Select between 1T and 2T mode on ADDR/CMD
Gear Down Mode	Disabled Enabled **Auto**	No help string
LPDDR4 Refresh Mode	**Auto** All Banks Per Bank	Auto will result in all banks being enabled. Per bank enables refreshes to be sent on a per bank basis.

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7.3.19.3.1.1.1 AMD CBS > DF Common Options > UMC Common Options > DDR4 Common Options > DRAM Controller Configuration > DRAM Power Options

Feature	Options	Description
DRAM Power Options	Info only	
Power Down Enable	Disabled Enabled **Auto**	Enable or disable DDR power down mode.

7.3.19.3.1.2 AMD CBS > DF Common Options > UMC Common Options > DDR4 Common Options > CAD Bus Configuration

Feature	Options	Description
CAD Bus Configuration	Info only	
CAD Bus Timing User Controls	**Auto** Manual	Setup time on CAD bus signals to Auto or Manual
CAD Bus Drive Strength User Controls	**Auto** Manual	Drive Strength on CAD bus signals to Auto or Manual

7.3.19.3.1.3 AMD CBS > DF Common Options > UMC Common Options > DDR4 Common Options > Data Bus Configuration

Feature	Options	Description
Data Bus Configuration	Info only	
Data Bus Configuration User Controls	**Auto** Manual	Specify the mode for drive strength to Auto or Manual

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7.3.19.3.1.4 AMD CBS > DF Common Options > UMC Common Options > DDR4 Common Options > Common RAS

Feature	Options	Description
Common RAS	Info only	
Data Poisoning	Disabled Enabled **Auto**	No help string
DRAM Post Package Repair	**Disabled** Enabled	Enable or Disable DRAM Post Package Repair.
RCD Parity	**Auto** Disabled Enabled	No help string
DRAM Address Command Parity Retry	**Auto** Disabled Enabled	UMC_CH::RecCtrl[RecEn][0] and UMC_CH::RecCtrl[MaxParRply]
Max Parity Error Replay	Info only	
Write CRC Enable	**Auto** Disabled Enabled	No help string
DRAM Write CRC Enable and Retry Limit	**Auto** Disabled Enabled	UMC_CH::RecCtrl[RecEn][1] and UMC_CH::RecCtrl[MaxCrcRply]
Max Write CRC Error Replay	Info only	
Disable Memory Error Injection	**Ture** False	True: UMC::CH::MiscCfg[DisErrInj]=1
ECC Configuration	submenu	

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7.3.19.3.1.4.1 AMD CBS > DF Common Options > UMC Common Options > DDR4 Common Options > ECC Configuration

Feature	Options	Description
ECC Configuration	Info only	
DRAM ECC Symbol Size	x4 x8 **Auto**	DRAM ECC Symbol Size (x4/x8) - UMC_CH::EccCtrl[EccSymbolSize]
DRAM ECC Enable	Disabled Enabled **Auto**	Use this option to enable / disable DRAM ECC. Auto will set ECC to enable.
DRAM UECC Retry	**Disabled** Enabled	Use this option to enable / disable DRAM UECC Retry.

7.3.19.3.1.5 AMD CBS > DF Common Options > UMC Common Options > DDR4 Common Options > Security

Feature	Options	Description
Security	Info only	
TSME	**Auto** Enabled Disabled	No help string
Data Scramble	Enabled Disabled **Auto**	Data scrambling: DataScrambleEn

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7.3.19.3.2 AMD CBS > DF Common Options > UMC Common Options > DRAM Memory Mapping

Feature	Options	Description
DRAM Memory Mapping	Info only	
Chipselect Interleaving	Disable **Auto**	Interleave memory blocks across the DRAM chip selects for node 0.
BankGroupSwap	**Auto** Disable CPU Mode APU Mode ALT Mode	No help string
Address Hash Bank	Disabled Enabled **Auto**	Enable or disable bank address hashing
Address Hash CS	**Auto** Enabled Disabled	Enable or disable CS address hashing
Address Hash Rm	**Auto** Enabled Disabled	Enable or disable RM address hashing
SPD Read Optimization	Auto **Enabled** Disabled	Enable or disable SPD Read Optimization, Enabled - SPD reads are skipped for Reserved fields and most of upper 256 Bytes, Disabled - read all 512 SPD Bytes

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7.3.19.3.3 AMD CBS > DF Common Options > UMC Common Options > Phy Configuration

Feature	Options	Description
Phy Configuration	Info only	
PMU Training	submenu	PMU Training

7.3.19.3.3.1 AMD CBS > DF Common Options > UMC Common Options > PMU Training

Feature	Options	Description
PMU Training	Info only	
DFE Read Training	**Auto** Enabled Disabled	Perform 2D Read Training with FFE on.
FFE Write Training	**Auto** Enabled Disabled	Perform 2D Write Training with FFE on.

7.3.19.3.4 AMD CBS > DF Common Options > UMC Common Options > Memory MBIST

Feature	Options	Description
Memory MBIST	Info only	
MBIST Enable	**Disabled** Enabled	Enable or disable Memory MBIST
MBIST Test Mode	Interface Mode Data Eye Mode Both **Auto**	Select MBIST Test Mode -Interface Mode (Tests Single and Multiple CS transactions and Basic Connectivity) or Data Eye Mode (Measures Voltage vs. Timing)
MBIST Aggressors	Disabled	Enable or disable MBIST Aggressor test

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Feature	Options	Description
	Enabled **Auto**	
MBIST Per Bit Slave Die Reporting	Disabled Enabled **Auto**	Reports 2D Data Eye Results in ABL Log for each DQ, Chipselect, and Channel
Data Eye	submenu	Data Eye

7.3.19.3.4.1 AMD CBS > DF Common Options > UMC Common Options > Memory MBIST > Data Eye

Feature	Options	Description
Data Eye	Info only	
Pattern Select	**PRBS** SSO Both	No help string
Pattern Length	**3**	This token helps to determine the pattern length. The possible options are N=3...12
Aggressor Channel	Disable **1 Aggressor Channel** 3 Aggressor Channels 7 Aggressor Channels	This helps read the aggressors channels. If it is enabled, you can read from one or more than one aggressor channel. The default is set to disabled.
Aggressor Static Lane Control	**Disabled** Enabled	This option, if enabled, will control the Aggressor Static Lane Controls.
Aggressor Static Lane Select Upper 32 bits	**0**	Static Lane Select for Upper 32 bits. The bit mask represents the bits to be read
Aggressor Static Lane Select Lower 32 Bits	**0**	Static Lane Select for Lower 32 bits. The bit mask represents the bits to be read
Aggressor Static Lane Select ECC	**0**	Static Lane Select for ECC Lanes. The bit mask represents the bits to be read
Aggressor Static Lane Value	**0**	TBD
Target Static Lane Control	**Disabled**	No help string

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Feature	Options	Description
	Enabled	
Target Static Lane Select Upper 32 bit	**0**	Static Lane Select for Upper 32 bit. The bit mask represents the bits to be read
Target Static Lane Select Lower 32 Bits	**0**	Static Lane Select for Lower 32 bit. The bit mask represents the bits to be read
Target Static Lane Select ECC	**0**	TBD
Target Static Lane Value	**0**	No help string
Data Eye Type	1D Voltage Sweep 1D Timing Sweep 2D Full Data Eye **Worst Case Margin Only**	No help string
Worst Case Margin Granularity	**Per Chip Select** Per Nibble	No help string
Read Voltage Sweep Step Size	**1** 2 4	This option determines the step size for Read Data Eye voltage sweep, supported options are 1,2 and 4
Read Timing Sweep Step Size	**1** 2 4	This option supports step size for Read Data Eye. Supported options are 1, 2 and 4
Write Voltage Sweep Step Size	**1** 2 4	This option determines the step size for write Data Eye voltage sweep, supported options are 1,2 and 4
Write Timing Sweep Step Size	**1** 2 4	This option supports step size for write Data Eye. Supported options are 1, 2 and 4

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7.3.19.4 AMD CBS > NBIO Common Options

Feature	Options	Description
NBIO Common Options	Info only	
IOMMU	Disabled Enabled **Auto**	Enable/Disable IOMMU
PCIe ARI Support	Disabled Enabled **Auto**	Enable/Disable ARI
PSPP Policy	Disabled Enabled **Auto**	No help string
GFX Configuration	submenu	GFX Configuration
Audio Configuration	submenu	Audio Configuration
SMU Common Options	submenu	SMU Common Options

7.3.19.4.1 AMD CBS > NBIO Common Options > GFX Configuration

Feature	Options	Description
GFX Configuration	Info only	
iGPU Configuration	**Auto** iGPU Disabled UMA_SPECIFIED UMA_AUTO UMA_GAME_OPTIMIZED	UMA Mode
UMA Version	Legacy Non-Legacy	UMA Legacy Version\nUMA Non Legacy Version\nHybrid Secure

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Feature	Options	Description
	Hybrid Secure **Auto**	
GPU Host Translation Cache	Disabled Enabled **Auto**	Option to disable GPU Host Translation Cache

7.3.19.4.2 AMD CBS > NBIO Common Options > Audio Configuration

Feature	Options	Description
Audio Configuration	Info only	
NB Azalia	Disabled Enabled **Auto**	Enable Integrate HD Audio controller
Audio IOs	**Auto** Azalia SoundWire Azalia and SoundWire I2STDM and I2SBT Azalia and I2SBT SoundWire and I2SBT Azalia mHDA	Audio IOs control
PDM Mic Selection	**Auto** Use 4 Channel Use 6 Channel	PDM Mic Selection

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7.3.19.4.3 AMD CBS > NBIO Common Options > SMU Common Options

Feature	Options	Description
SMU Common Options	Info only	
Fan Control	submenu	Fan Control
System Temperature Tracking	submenu	System Temperature Tracking
STAPM Control	submenu	STAPM Control
SmartShift Control	submenu	SmartShift Control
System Configuration	10W POR Configuration - 1 Commercial/Consumer 15W POR Configuration - 2 Commercial/Consumer 25W POR Configuration - 3 Commercial/Consumer 35W POR Configuration - 4 Consumer 45W POR Configuration - 5 Consumer 54W POR Configuration - 6 Consumer **Auto**	Warning: Select System Configuration may cause the system to hang, as some System Configuration may not be supported by your OPN.
CPPC	submenu	CPPC

7.3.19.4.3.1 AMD CBS > NBIO Common Options > SMU Common Options> Fan Control

Feature	Options	Description
Fan Control	Info only	
Fan Control	Manual **Auto**	Auto = Use the default fan controller settings Manual = User can set customized fan controller settings
Force PWM Control	Force **Unforce**	Unforce = Do not force the fan PWM Force = Force the fan PWM to the use specified value
Fan Table Control	Manual	Auto = Use the default fan table

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Feature	Options	Description
	Auto	Manual = User can set customized fan table

7.3.19.4.3.2 AMD CBS > NBIO Common Options > SMU Common Options> System Temperature Tracking

Feature	Options	Description
System Temperature Tracking	Info only	
STT Control	Manual **Auto**	Auto = Use the default STT controller settings Manual = User can set customized STT controller settings
System Temperature Tracking	**Auto** Disable Enable	System Temperature Tracking [0 = disabled; 1 = enabled]

7.3.19.4.3.3 AMD CBS > NBIO Common Options > SMU Common Options> STAPM Control

Feature	Options	Description
STAPM Control	Info only	
STAPM Control	Manual **Auto**	No help string
STAPM Boost	**Auto** Disable Enable	STAPM Boost Enable [1 = boost disabled; 2 = boost enabled]

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7.3.19.4.3.4 AMD CBS > NBIO Common Options > SMU Common Options> SmartShift Control

Feature	Options	Description
SmartShift Control	Info only	
SmartShift Control	Manual **Auto**	No help string
SmartShift Enable	**Auto** Disable Enable	A+A Support Enable
APU Only sPPT Limit	**0**	APU Only sPPT Limit in mW
Sustained PowerLimit	**0**	PcdMsgSetSustainedPowerLimit
Fast PPT Limit	**0**	PcdMsgSetFastPPTLimit
Slow PPT Limit	**0**	PcdMsgSetSlowPPTLimit

7.3.19.4.3.5 AMD CBS > NBIO Common Options > SMU Common Options> CPPC

Feature	Options	Description
CPPC	Info only	
CPPC CTRL	**Auto** Enabled Disabled	No help string
Perf Limit Max Range	**ff**	Range of CppcPerfLimitMax: 0 - 255
Perf Limit Min Range	**0**	Range of CppcPerfLimitMin: 0 - 255
EPP Max Range	**ff**	Range of EPP Max: 0 - 255
EPP Min Range	**0**	Range of EPP Min: 0 - 255

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7.3.19.5 AMD CBS > FCH Common Options

Feature	Options	Description
FCH Common Options	Info only	
SATA Configuration Options	submenu	SATA Configuration Options
USB Configuration Options	submenu	USB Configuration Options
Ac Power Loss Options	submenu	Ac Power Loss Options
I2C Configuration Options	submenu	I2C Configuration Options
Uart Configuration Options	submenu	Uart Configuration Options
ESPI Configuration Options	submenu	ESPI Configuration Options
XGBE Configuration Options	submenu	XGBE Configuration Options
LPC Options	submenu	LPC Options
HFP Options	submenu	HFP Options

7.3.19.5.1 AMD CBS > FCH Common Options > SATA Configuration Options

Feature	Options	Description
SATA Configuration Options	Info only	
SATA Controller	Disabled Enabled **Auto**	Disable or enable OnChip SATA controller
SATA Auto Shutdown	Disabled Enabled **Auto**	Disable SATA controller if there is no port connection.
SATA RAS Support	Disabled Enabled **Auto**	Disable or enable SATA RAS Support

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Feature	Options	Description
SATA Disabled AHCI Prefetch Function	Disabled Enabled **Auto**	Disable or enable SATA Disabled AHCI Prefetch Function
Aggressive SATA Device Sleep Port 0	Disabled Enabled **Auto**	No help string
Aggressive SATA Device Sleep Port 1	Disabled Enabled **Auto**	No help string

7.3.19.5.2 AMD CBS > FCH Common Options > USB Configuration Options

Feature	Options	Description
USB Configuration Options	Info only	
XHCI0 Controller Enable	Disabled Enabled **Auto**	Enable or disable USB3 controller.
XHCI1 Controller Enable	Disabled Enabled **Auto**	Enable or disable USB3 controller.

7.3.19.5.3 AMD CBS > FCH Common Options > Ac Power Loss Options

Feature	Options	Description
Ac Power Loss Options	Info only	
Ac Loss Control	**Always Off** Always On	Select Ac Loss Control Method

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Feature	Options	Description
	Reserved Previous Auto	

7.3.19.5.4 AMD CBS > FCH Common Options > I2C Configuration Options

Feature	Options	Description
I2C Configuration Options	Info only	
I2C 0 Enable	Disabled **Enabled** Auto	No help string
I2C 1 Enable	Disabled Enabled **Auto**	No help string
I2C 2 Enable	Disabled Enabled **Auto**	No help string
I2C 3 Enable	Disabled Enabled **Auto**	No help string

7.3.19.5.5 AMD CBS > FCH Common Options > Uart Configuration Options

Feature	Options	Description
Uart Configuration Options	Info only	
Uart 0 Enable	Disabled Enabled	Uart 0 has no HW FC if Uart 2 is enabled

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Feature	Options	Description
	Auto	
Uart 1 Legacy Options	Disable 0x2E8 0x2F8 0x3E8 0x3F8 **Auto**	Uart 1 has no HW FC if Uart 3 is enabled
Uart 1 Enable	Disabled Enabled **Auto**	Uart 1 has no HW FC if Uart 3 is enabled
Uart 2 Legacy Options	Disable 0x2E8 0x2F8 0x3E8 0x3F8 **Auto**	No help string

7.3.19.5.6 AMD CBS > FCH Common Options > ESPI Configuration Options

Feature	Options	Description
ESPI Configuration Options	Info only	
ESPI Enable	Disabled Enabled **Auto**	No help string

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7.3.19.5.7 AMD CBS > FCH Common Options > XGBE Configuration Options

Feature	Options	Description
XGBE Configuration Options	Info only	
XGBE0 Enable	Enabled Disabled **Auto**	Enable or disable Ethernet controller.
XGBE1 Enable	Enabled Disabled **Auto**	Enable or disable Ethernet controller.

7.3.19.5.8 AMD CBS > FCH Common Options > LPC Options

Feature	Options	Description
LPC Options	Info only	
LPC Clock Run control	Disabled Enabled **Auto**	No help string

7.3.19.5.9 AMD CBS > FCH Common Options > HFP Options

Feature	Options	Description
HFP Options	Info only	
HFP Enable	Disable Eanble HFP on SPI_CS3_L **Auto**	No help string

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7.3.19.6 AMD CBS > Soc Miscellaneous Control

Feature	Options	Description
Soc Miscellaneous Control	Info only	
ABL Console Out Control	**Auto** Enable Disable	Enable: Enable ConsoleOut Function for ABL Disable: Disable ConsoleOut Function for ABL Auto: Keep default behavior
ABL Console Out Boot Mode Select	**ALL** S3/S0i3 only Normal boot only	No help string
ABL PMU message Control	Detailed debug message Coarse debug message Stage completion Firmware completion message only **Auto**	To control the total number of PMU debug messages. Several major controls are listed below. Detailed debug messages (e.g., Eye delays). Coarse debug messages (e.g., rank information). Stage completion. Firmware completion messages only

7.3.20 AMD PBS

Feature	Options	Description
AMD Firmware Version	submenu	Show all of AMD Firmware Version
SSD Power Enable	Disable SSD x1 : Test only.The item breaks WWAN,LAN,WLAN Pcie Slot **SSD x2** SSD x4	Enable or disable the power of SSD
GPP8/9 Select	PCIE **SATA**	Usage of GPP8/9
EVAL CARD T-Diode Routing Select	Info only	Select which APU eSPI port route to EC

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Feature	Options	Description
Special Display Features	**Disable** HybridGraphics	Enable/Disable HybridGraphics
D3Cold Support	**Disable** Enable	Enable/Disable PCIe x8 Slot D3Cold
NVIDIA DGPU Power Enable	**Disable** Enable	For NVIDIA mobile DGPU card only. Output DGPU_EN# A19 pin and DGPU_SEL# B17 pin to high at every power on state.
Non-Eval Discrete GPU Support	**Disable** Enable	Enable to support Non-Eval Discrete GPU that doesn't have specific EVAL_PWRGD(B30), EVAL_PRESENT#(A5)
Discrete GPU HPD Circuitry	**OR Circuitry** Pulse Circuitry	Enable/Disable Discrete GPU Display HPD Circuitry
Discrete GPU's Audio	**Disable** Keep ROM Strap Setting	Disable Discrete GPU's Audio or keep its ROM strap setting
Discrete GPU BOMACO Support	**Disable** Enable	Enable/Disable Discrete GPU BOMACO Support
Primary Video Adaptor	**Int Graphics (IGD)** Ext Graphics (PEG)	Select Internal/External Graphics
Wake On Voice	Disable **Enable**	Enable or Disable Wake On Voice
ACP Power Gating	**Disable** Enable	Enable or Disable ACP Power Gating
ACP CLock Gating	Disable **Enable**	Enable or Disable ACP CLOCK Gating
Above 4GB MMIO Limit	35bit (32GB) 36bit (64GB) 37bit (128GB) 38bit (256GB) 39bit (512GB)	Select Above 4GB MMIO Limit to 35~48bits limit.

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Feature	Options	Description
	40bit (1TB) 41bit (2TB) 42bit (4TB) 43bit (8TB) 44bit (16TB) 45bit (32TB) 46bit (64TB) 47bit (128TB) 48bit (256TB)	
UCSI Support	Disable **Enable**	Enable/Disable UCSI (USB Type-C Connector System Software Interface)
S3/Modern Standby Support	S3 Enable **Modern Standby Enable**	Switch S3/Modern Standby
Modern Standby Type	Modern Standby + S0i2 **Modern Standby + S0i3** Modern Standby + S0i2 + S0i3	Select S0I2 or S0I3 type for Modern Standby.
MS Resource	Disable **Enable**	Enable: Enable USB current resource for MS; Disable: Disable USB current resource for MS.
Wake on PME	Disable **Enable**	Determines the action taken when the system power is off and a PCI Power Management Enable wake up event occurs.
Sensor Fusion User Mode Driver	**Disable** Enable	Enable/Disable Sensor Fusion User Mode Driver
MITT/WITT Selection	MITT Only WITT Only **Both disable**	MITT/WITT Selection
KBC Support	Disable **Enable**	Enable/Disable KBC Support under OS
BLINK LED	Disable	Enable/Disable BLINK LED to identify S3/S4 state

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Feature	Options	Description
	Enable GPIO 11 Output Low GPIO 11 Output High	
iLA TraceMemoryEn	**Disable** Enable	Reserved 1M bytes MMIO space on 1M boundary when iLA TraceMemoryEn enabled
iLA TraceMemoryEn reserved MMIO	**0**	

7.3.20.1 AMD PBS > AMD Firmware Version

Feature	Options	Description
AMD Firmware Version	Info only	
AGESA Version	Info only	
PSP BootLoader Version	Info only	
PSP SecureOS Version	Info only	
ABL Version	Info only	
APCB Version	Info only	
APOB Version	Info only	
Ucode Patch Version	Info only	
SMU FW Version	Info only	
DXIO FW Version	Info only	
MP2 FW Version	Info only	
KVM Engine Version	Info only	
XHCI FW Version	Info only	
VBIOS FW Version	Info only	

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Feature	Options	Description
GOP Driver Version	Info only	
EC FW Version	Info only	
USB PD Section 1 FW Version	Info only	
USB PD Section 2 FW Version	Info only	
TI PD FW MODE	Info only	
TI PD FW Version	Info only	

7.4 Chipset

Feature	Options	Description
South Bridge	submenu	
GFX Configuration	submenu	
North Bridge	submenu	

7.4.1 Chipset > South Bridge

Feature	Options	Description
AMD Reference Code Version	Info only	
SB USB Configuration	submenu	
SB Power Saving	submenu	
SB Debug Configuration	submenu	

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7.4.1.1 Chipset > SB USB Configuration

Feature	Options	Description
Memory Configuration	Info only	
XHCI0 Port 0	Disabled **Enabled**	Enabled/Disabled XHCI0 Port 0(XHCI/EHCI)
XHCI0 Port 1	Disabled **Enabled**	Enabled/Disabled XHCI0 Port 1(XHCI/EHCI)
XHCI0 Port 2	Disabled **Enabled**	Enabled/Disabled XHCI0 Port 2(XHCI/EHCI)
XHCI0 Port 3	Disabled **Enabled**	Enabled/Disabled XHCI0 Port 3(XHCI/EHCI)
XHCI1 Port 0	Disabled **Enabled**	Enabled/Disabled XHCI1 Port 0(XHCI/EHCI)
XHCI1 Port 1	Disabled **Enabled**	Enabled/Disabled XHCI1 Port 1(XHCI/EHCI)
XHCI1 Port 2	Disabled **Enabled**	Enabled/Disabled XHCI1 Port 2(XHCI/EHCI)
XHCI1 Port 3	Disabled **Enabled**	Enabled/Disabled XHCI1 Port 3(XHCI/EHCI)

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7.4.1.2 Chipset > SB Power Saving

Feature	Options	Description
AB Clock Gating	Disabled Enabled **Auto**	Enable/Disable AB Internal Clock Gating
PCIB Clock Run	Disabled Enabled **Auto**	Enable The Auto Clkrun Functionality

7.4.1.3 Chipset > SB Debug Configuration

Feature	Options	Description
SB SATA DEBUG Configuration	submenu	
SB FUSION DEBUG Configuration	submenu	
SB MISC DEBUG Configuration	submenu	

7.4.1.3.1 Chipset > SB Debug Configuration > SB SATA DEBUG Configuration

Feature	Options	Description
SATA MAXGEN2 CAP Option	Disabled **Enabled** Auto	Set SATA Max Gen2 Mode
SATA CLK Mode Option	EXT 25MHz INT 48MHz INT 100MHz **Auto**	SATA Reference Clock Selector And Divider
Aggressive Link PM Capability	Disabled	Indicates Whether Host Bus Adapter (HBA) Can Support Auto-Generating Link Requests To The Partial Or

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Feature	Options	Description
	Enabled **Auto**	Slumber States When There Are No Commands To Process
Port Multiplier Capability	Disabled Enabled **Auto**	Indicates Whether Host Bus Adapter (HBA) Can Support A Port Multiplier
SATA Ports Auto Clock Control	Disabled Enabled **Auto**	Enable/Disable SATA Ports Auto Clock Control
SATA Partial State Capability	Disabled Enabled **Auto**	Indicates Whether SATA Host Bus Adapter (HBA) Can Support Transitions To The Partial State
SATA FIS Based Switching	Disabled Enabled **Auto**	Indicates Whether SATA Host Bus Adapter (HBA) Can Support Port Multiplier FIS-Based Switching
SATA Command Completion Coalescing Support	Disabled Enabled **Auto**	Indicates Whether SATA Host Bus Adapter (HBA) Can Support Command Completion Coalescing
SATA Slumber State Capability	Disabled Enabled **Auto**	Indicates Whether SATA Host Bus Adapter (HBA) Can Support Transitions To The Slumber State
SATA MSI Capability Support	Disabled Enabled **Auto**	SATA Controller Message-Based Interrupts Capability Support
SATA Target Support 8 Devices	Disabled Enabled **Auto**	Indicates Whether SATA Target Support 8 Devices Function
Generic Mode	Disabled Enabled	SATA Disable Generic Mode

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Feature	Options	Description
	Auto	
SATA AHCI Enclosure	Disabled Enabled **Auto**	SATA AHCI Enclosure Management
SATA SGPIO 0	Disabled Enabled **Auto**	Enable/Disable SATA Serial General Purpose Input/Output (SGPIO) 0

7.4.1.3.2 Chipset > SB Debug Configuration >SB FUSION DEBUG Configuration

Feature	Options	Description
Clock Interrupt Tag	Disabled Enabled **Auto**	Mark The Periodic Timer Interrupt

7.4.1.3.3 Chipset > SB Debug Configuration >SB MISC DEBUG Configuration

Feature	Options	Description
SB Clock Spread Spectrum	**Disabled** Enabled Auto	Enable/Disable CG1_PLL Spread Spectrum
HPET In SB	Disabled **Enabled** Auto	HPET Function Switch
MsiDis in HPET	Disabled Enabled **Auto**	Expose MSI capability in HPET Capability register

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Feature	Options	Description
_OSC For PCI0	Disabled Enabled **Auto**	PCIe NativePcieSupport - Debug function.
GPP Serial Debug Bus Enable	Disabled Enabled **Auto**	GPP Serial Debug Bus Enable

7.4.2 Chipset > GFX Configuration

Feature	Options	Description
GFX Configuration	Info only	
IGD - AmdGop Output Priority	**Default** Manually	
LVDS Backlight Brightness	**255**	Lcd Only, Range 0 - 255

7.4.3 Chipset > North Bridge

Feature	Options	Description
North Bridge Configuration	Info only	
Memory Information	Info only	
Total Memory	Info only	
Socket 0 Information	submenu	

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7.4.3.1 Chipset > North Bridge > Socket 0 Information

Feature	Options	Description
Socket 0 Information	Info only	
Starting address	Info only	
Ending Address	Info only	
ChannelA	Info only	
Dimm0	Info only	
Current speed	Info only	
MAX speed	Info only	
ChannelB	Info only	
Dimm0	Info only	
Current speed	Info only	
MAX speed	Info only	

7.5 Security

Feature	Options	Description
Administrator Password	Enter password	Set Admonistrator Password
User Password	Enter password	Set User Password
HDD Security Configuration	Info only	
Secure Boot	submenu	

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7.5.1 Secure Boot menu

Feature	Options	Description
Secure Mode	Info only	
Secure Boot	**Disabled** Enabled	Secure Boot feature is Active if Secure Boot is Enabled,platform Key(PK) is enrolled and the System is in User mode, The mode change requires platform reset
Secure Boot Mode	**Standard** Custom	Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full
Restore Factory Keys	Info only	Force System to User Mode. Install factory default Secure Boot key databases
Reset To Setup Mode	Info only	
Key Management		Enables expert users to modify Secure Boot Policy variables without full authentication

7.6. Boot

7.6.1 Boot Configuration

Feature	Options	Description
Boot Configuration	Info only	
Setup Prompt Timeout	**1**	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
Bootup NumLock State	**On** Off	Select the keyboard NumLock state
Quiet Boot	Disabled **Enabled**	Enables or disables Quiet Boot option
Fast Boot	Disabled **Enabled**	Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot option.

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Feature	Options	Description
SATA Support	**Last Boot SATA Devices Only** All SATA Devices	If Last Boot SATA Devices Only, Only last boot SATA device will be available in Post. If All SATA Devices, all SATA devices will be available in OS and Post.
NVME Support	Disabled **Enabled**	If Disabled, NVMe device will be skipped.
VGA Support	Auto **EFI Driver**	If Auto, only install Legacy OpRom with Legacy OS and logo would NOT be shown during post. Efi driver will still be installed with EFI OS.
USB Support	Disabled **Full Initial** Partial Initial	If Disabled, all USB devices will NOT be available until after OS boot. If Partial Initial, USB Mass Storage and specific USB port/device will NOT be available before OS boot. If Enabled, all USB devices will be available in OS and Post.
PS2 Devices Support	Disabled **Enabled**	If Disabled, PS2 devices will be skipped.
NetWork Stack Driver Support	**Disabled** Enabled	If Disabled, NetWork Stack Driver will be skipped.
Redirection Support	**Disabled** Enabled	If disable, Redirection function will be disabled.

7.7 Save & Exit

7.7.1 Save Options

Feature	Options	Description
Save Option	Info only	
Save Changes and Exit		Exit system setup after saving the changes.
Discard Changes and Exit		Exit system setup without saving any changes.
Save Changes and Reset		Reset the system after saving the changes.
Discard Changes and Reset		Reset system setup without saving any

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Feature	Options	Description
		changes.
Save Changed		Save changes done so far to any of the setup options.
Discard Changes		Discard Changes done so far to any of the setup options.

7.7.2 Default Options

Feature	Options	Description
Default Options	Info only	
Restore Defaults		Restore/Load Default values for all the setup options.
Save as User Defaults		Save the changes done so far as User Defaults.
Restore User Defaults		Restore the User Defaults to all the setup options.
Boot Override	Info only	

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8. BIOS Checkpoints, Beep Codes

This document section lists checkpoints and beep codes generated by AMI Aptio BIOS. The checkpoints defined in this document are inherent to the AMIBIOS generic core, and do not include any chipset or board-specific checkpoint definitions.

Checkpoints and Beep Codes Definition

A checkpoint is either a byte or word value output to I/O port 80h. The BIOS outputs checkpoints throughout the bootblock and Power-On Self-Test (POST) to indicate the task the system is currently executing. Checkpoints are very useful for debugging problems that occur during the preboot process.

Beep codes are used by the BIOS to indicate a serious or fatal error. They are used when an error occurs before the system video has been initialized, and generated by the system board speaker.

Aptio Boot Flow

While performing the functions of the traditional BIOS, Aptio 5.x core follows the firmware model described by the Intel Platform Innovation Framework for EFI ("the Framework"). The Framework refers to the following "boot phases", which may apply to various status code & checkpoint descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization[1]
- Driver Execution Environment (DXE) – main hardware initialization[2]
- Boot Device Selection (BDS) – system setup, pre-OS user interface & selecting a bootable device (CD/DVD, HDD, USB, Network, Shell, …)

Viewing BIOS Checkpoints

Viewing all checkpoints generated by the BIOS requires a checkpoint card, also referred to as an OST Card or POST Diagnostic Card. These are PCI add-in cards that show the value of I/O port 80h on a LED display.

Some computers display checkpoints in the bottom right corner of the screen during POST. This display method is limited, since it only displays checkpoints that occur after the video card has been activated.

Keep in mind that not all computers using AMI Aptio BIOS enable this feature. In most cases, a checkpoint card is the best tool for viewing AMI Aptio BIOS checkpoints.

[1]Analogous to "bootblock" functionality of legacy BIOS
[2]Analogous to "POST" functionality in legacy BIOS

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8.1. Status Code Ranges

Status Code Range	Description
0x01 – 0x0F	SEC Execution
0x10 – 0x2F	PEI CAR Execution
0x30 – 0x4F	PEI Execution After Memory Detection
0x50 – 0x5F	PEI Errors
0x60 – 0xCF	DXE Execution
0xD0 – 0xDF	DXE Errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume Errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery Errors (PEI)

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8.2. Standard Status Codes

8.2.1 SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization

SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

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8.2.2 SEC Beep Codes

None

8.2.3 PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12 – 0x14	Reserved for CPU
0x15	Pre-memory North Bridge initialization is started
0x16 – 0x18	Reserved for North Bridge
0x19	Pre-memory South Bridge initialization is started
0x1A – 0x1C	Reserved for South Bridge
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization

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Status Code	Description
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38 – 0x3A	Reserved for North Bridge initialization
0x3B	Post-Memory South Bridge initialization is started
0x3C -0x3E	Reserved for South Bridge
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self-test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error

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Status Code	Description
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes

Status Code	Description
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded

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Status Code	Description
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

8.2.4 PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

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8.2.5 DXE Status Codes

Status Code	Description
0x60	DXE Core has Started
0x61	NVRAM Initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization has Started
0x64 – 0x67	Reserved for CPU DXE Initialization (CPU module specific)
0x68	PCI Host Bridge Initialization
0x69	North Bridge DXE Initialization has Started
0x6A	North Bridge DXE SMM Initialization has Started
0x6B – 0x6F	Reserved for North Bridge DXE Initialization (North Bridge module specific)
0x70	South Bridge DXE Initialization has Started
0x71	South Bridge DXE SMM Initialization has Started
0x72	South Bridge Devices Initialization
0x73 – 0x77	Reserved for South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI Module Initialization
0x79	CSM Initialization
0x7A – 0x7F	Reserved for Future AMI DXE Codes
0x80 – 0x8F	OEM DXE Initialization Codes
0x90	Boot Device Selection (BDS) Phase has Started
0x91	Driver Connecting has Started
0x92	PCI Bus initialization has Started
0x93	PCI Bus Hot Plug Controller Initialization

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Status Code	Description
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output Devices Connect
0x98	Console Input Devices Connect
0x99	Super IO Initialization
0x9A	USB Initialization has Started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for Future AMI Codes
0xA0	IDE Initialization has Started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization has Started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (See ASL Status Codes section below)

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Status Code	Description
0xAB	Setup Input Wait
0xAC	Reserved for ASL (See ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM

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Status Code	Description
0xD6	No Console Output Devices are Found
0xD7	No Console Input Devices are Found
0xD8	Invalid Password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is Failed (StartImage returned error)
0xDB	Flash update is Failed
0xDC	Reset Protocol is Not Available

8.2.6 DXE Beep Codes

# of Beeps	Description
1	Invalid Password
4	Some of the Architectural Protocols are Not Available
5	No Console Output Devices are Found
5	No Console Input Devices are Found
6	Flash update is Failed
7	Reset protocol is Not Available
8	Platform PCI Resource Requirements Cannot be Met (Out of resource)

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8.2.7 ACPI/ASL Checkpoint

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

8.3. OEM-Reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

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9. Software Support

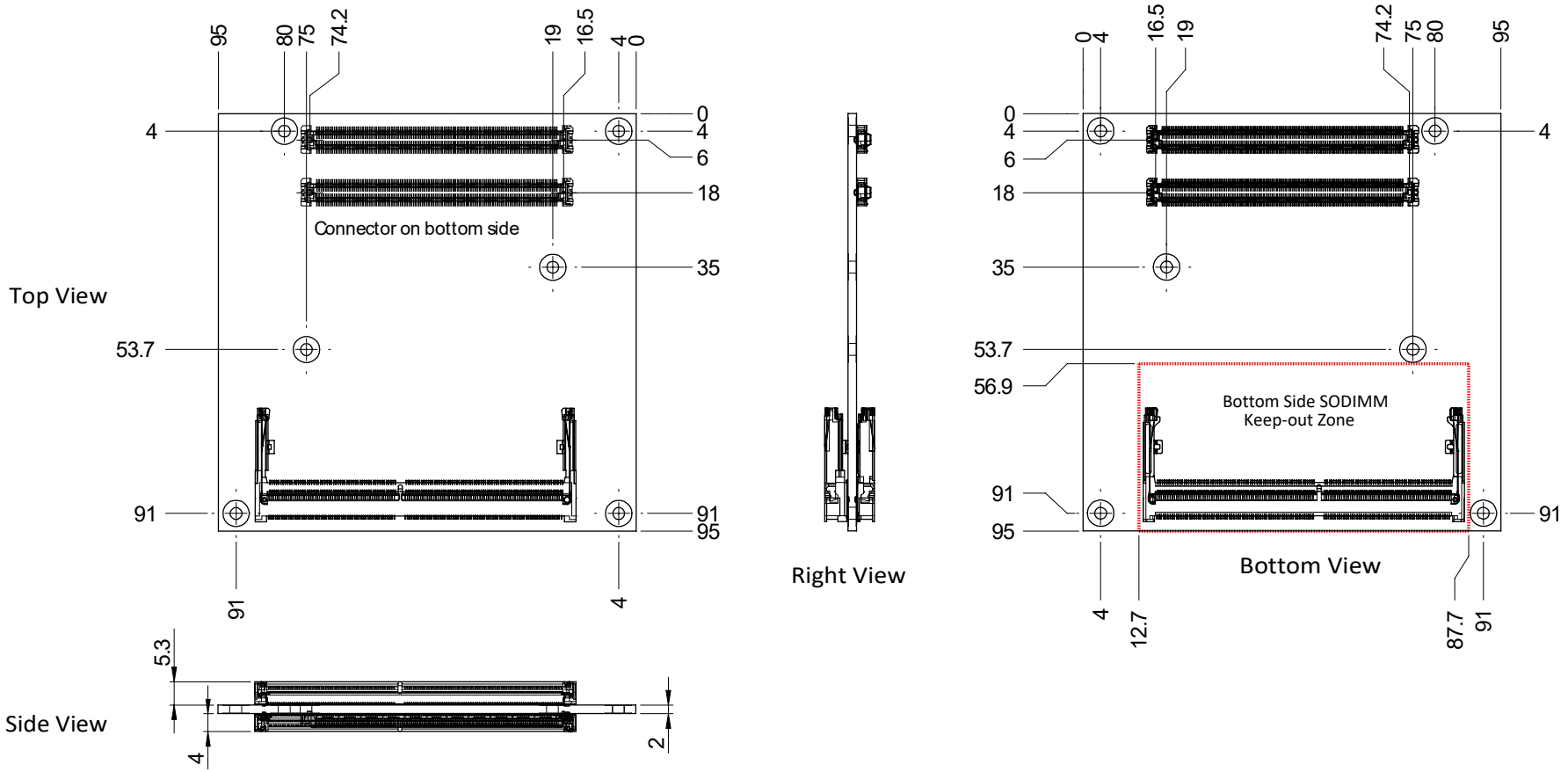
9.1. Operating Systems

- Windows 10 IOT Enterprise 64-bit
- Windows 10 64-bit
- Ubuntu 20.04 (planning)

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10. Mechanical and Thermal

10.1. Module Dimensions



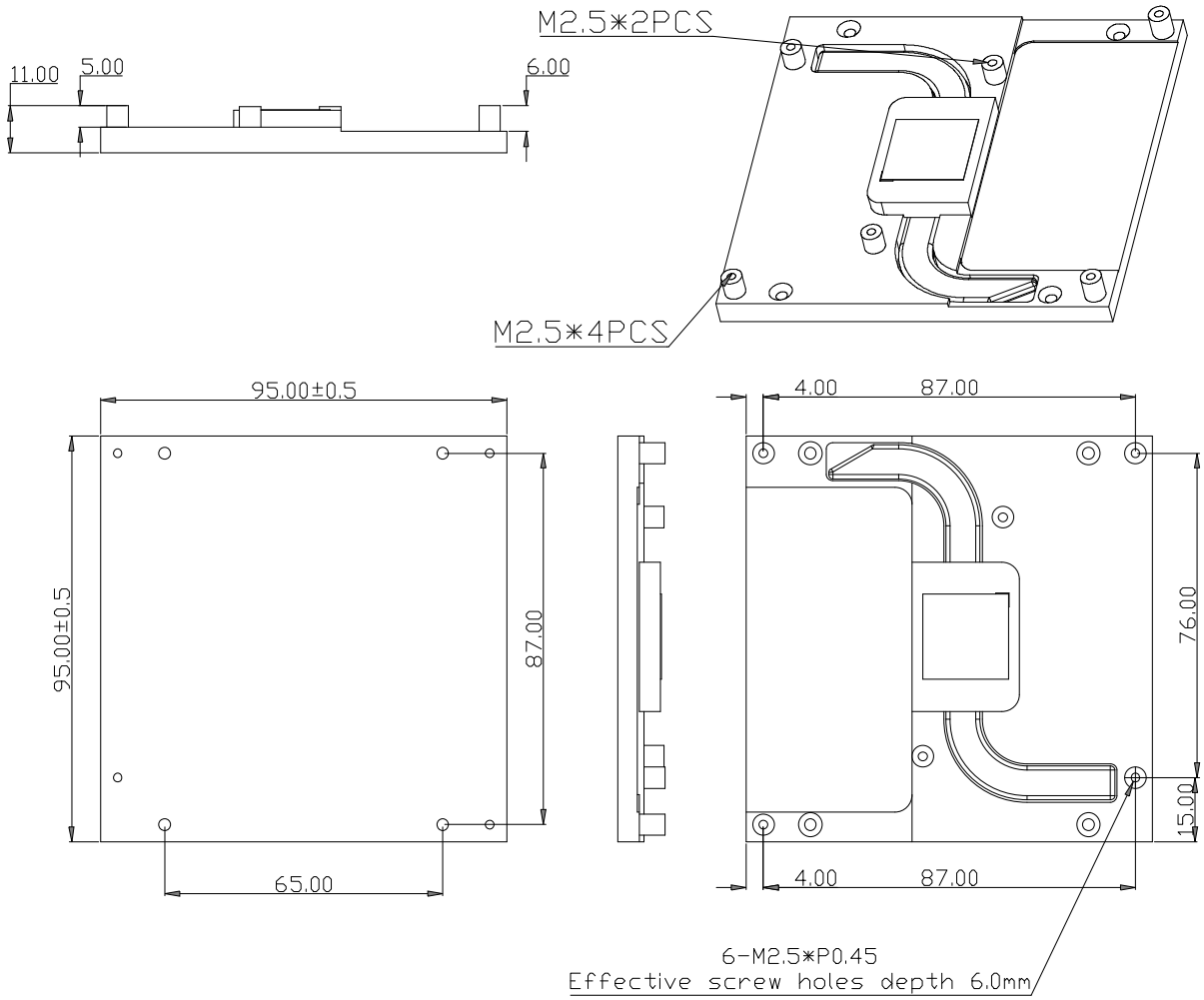
All dimensions are shown in millimeters. Tolerances should be ± 0.25mm, unless otherwise noted.
The tolerances on the module connector locating peg holes (dimensions [16.50, 6.00]&[16.50,18.00]) should be ± 0.10mm.

Figure 5 – Module mechanical dimensions

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10.2. Thermal Solutions

10.2.1 Heatspreader: HTS

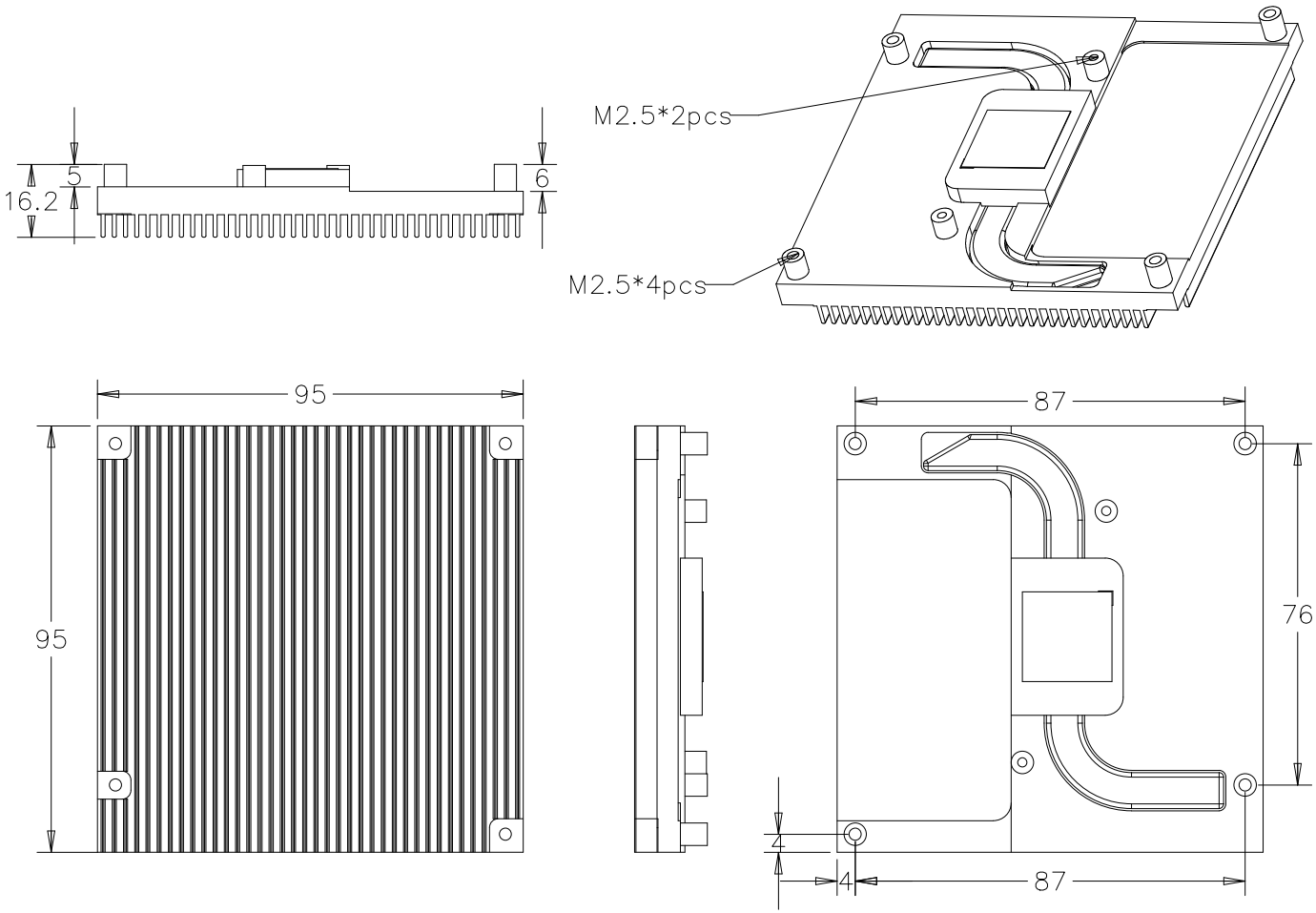


Dimensions: mm

Figure 6 – Heatspreader HTS

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10.2.2 Heatsink: THS

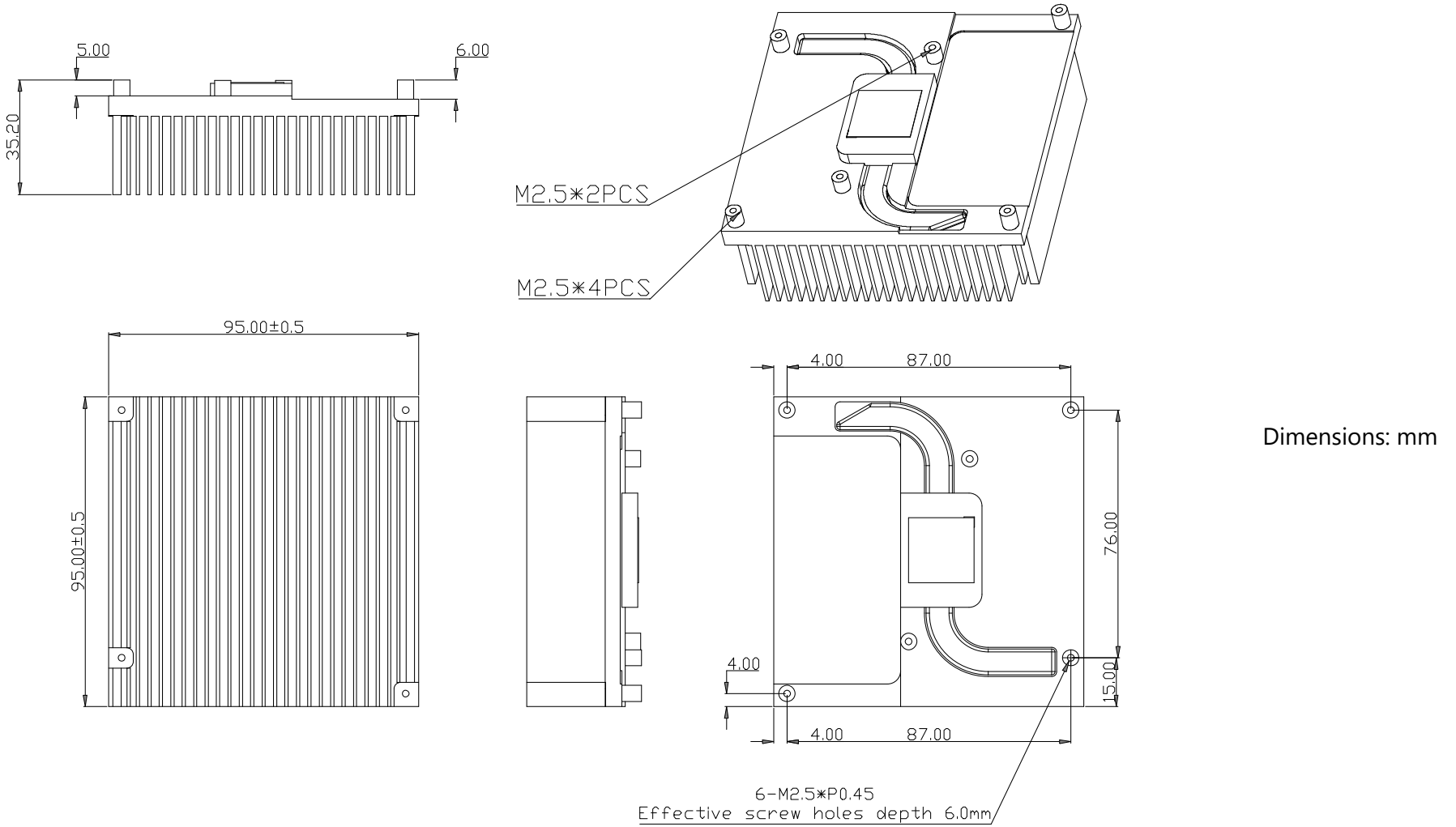


Dimensions: mm

Figure 7 – Heatsink THS

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10.2.3 Heatsink High Profile: THSH

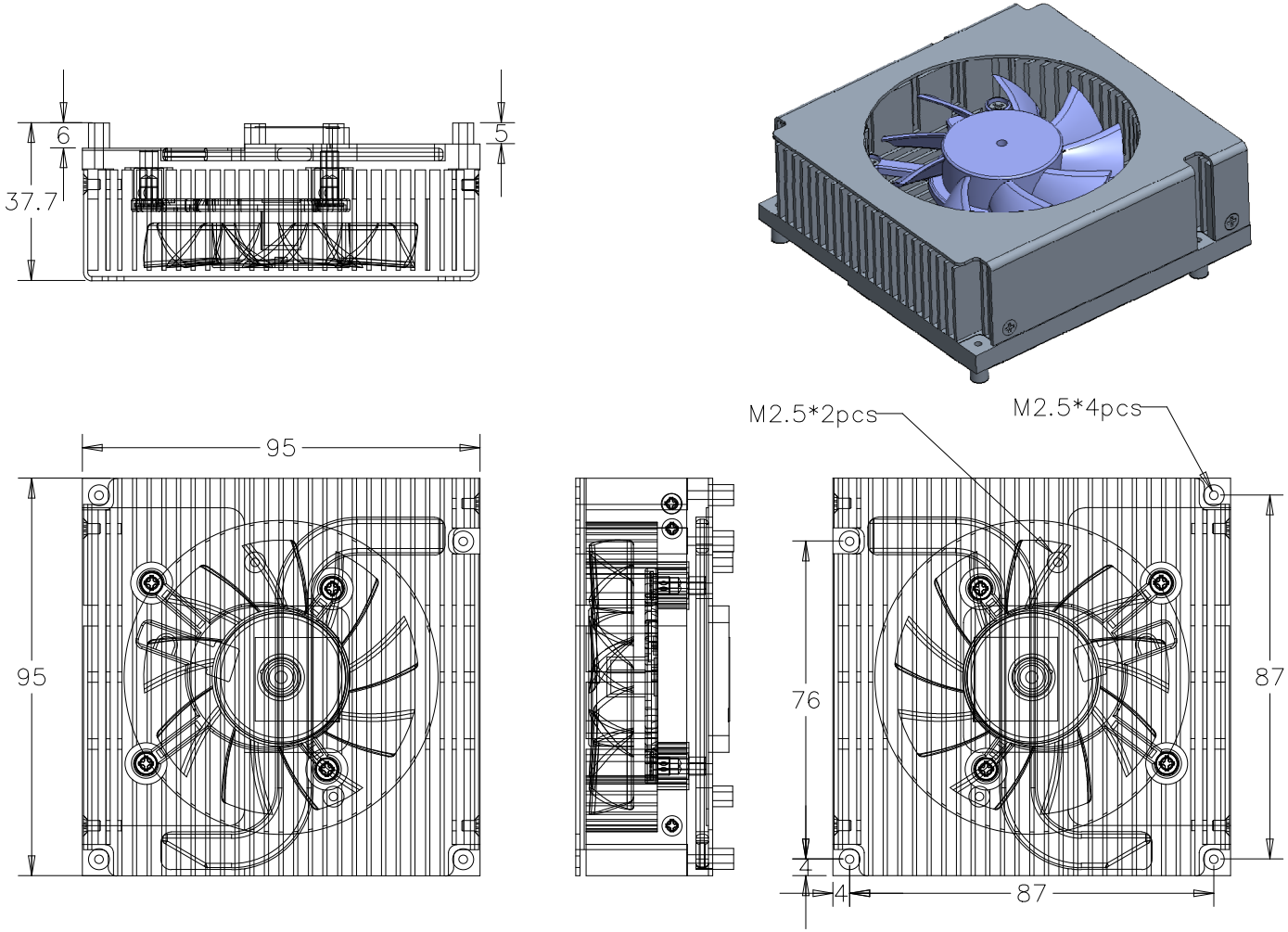


Dimensions: mm

Figure 8 – Heatsink High Profile: THSH

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10.2.4 Heatsink with Fan: THSF



Dimensions: mm

Figure 9 – Heatsink with Fan: THSF

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