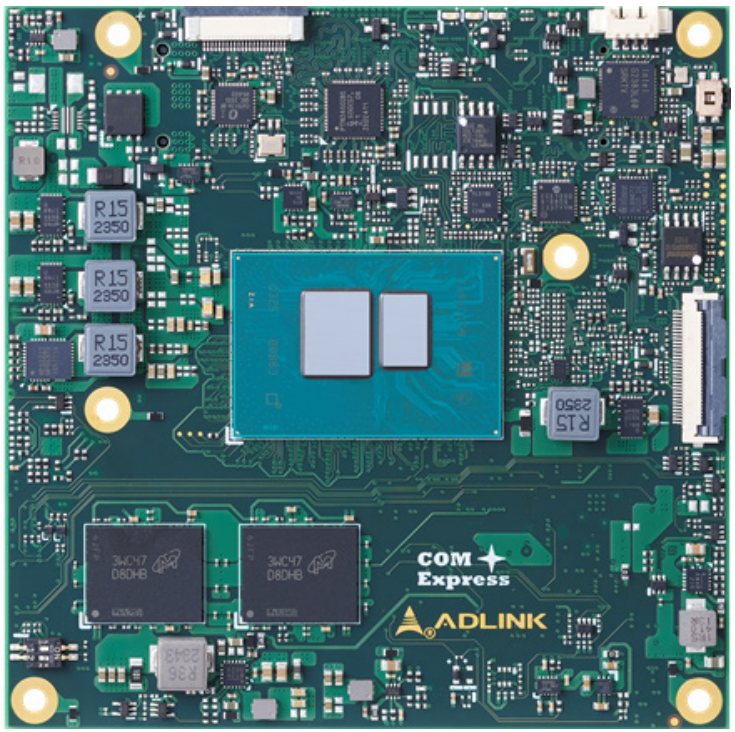
cExpress-ASL/ALN

User's Guide



COM Express®

Revision:	Rev. 1.3
Date:	2026-10-02
Part Number:	50M-72220-1030

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Revision History

Revision	Description	Date	Author
1.0	Initial release	2025-02-05	AL
1.1	Software support updated	2025-07-10	AL
1.2	Pinout and signal descriptions updated	2026-08-07	AL
1.3	Block diagram updated	2026-10-02	AL

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Preface

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Safety Instructions

For user safety, please read and follow all Instructions, **WARNING**s, **CAUTION**s, and **NOTE**s marked in this manual and on the associated equipment before handling/operating the equipment.

Read these safety instructions carefully.

- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

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Conventions

The following conventions may be used throughout this manual, denoting special levels of information

Note: This information adds clarity or specifics to text and illustrations.

Caution: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.

Warning: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

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Table of Contents

Revision History 2
Preface 3
List of Figures 11
1. Introduction 12
2. Specifications 13
2.1 Core System 13
2.2 Video 14
2.2.1 Display Interface Support 15
2.3 Audio 16
2.4 Expansion Bus 16
2.5 Ethernet 16
2.6 Multi I/O and Storage 17
2.7 Trusted Platform Module (TPM) 18
2.8 SEMA Board Controller 18
2.9 Debug 19
2.10 Power 19
2.11 Mechanical and Environmental 20
3. Block Diagram 21
4. Pinout and Signal Descriptions 22
4.1 Pin Summary 22
4.2 Signal Terminology Descriptions 27
4.3 AB Connector Signal Descriptions 28
4.3.1 Audio 28
4.3.2 Analog VGA 29
4.3.3 LVDS or eDP 30
4.3.4 Gigabit Ethernet 33
4.3.5 SATA 34
4.3.6 PCI Express 35
4.3.7 LPC Bus 37
4.3.8 USB 38
4.3.9 SPI Bus (BIOS only) 39
4.3.10 Miscellaneous 40
4.3.11 SMBus 41

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4.3.12 I²C Bus 41
4.3.13 General Purpose I/O (GPIO) 42
4.3.14 Serial Interface Signals 42
4.3.15 Power and System Management 43
4.3.16 Power and Ground 44
4.4 CD Connector Signal Descriptions 45
4.4.1 USB 3.0 Extensions 45
4.4.2 PCI Express 46
4.4.3 DDI1 Port 47
4.4.4 DDI2 Port 50
4.4.5 DDI3 Port 53
4.4.6 PCIe Graphics Port (PEG) 53
4.4.7 Module Type Definition 53
4.4.8 Power and Ground 54
5. Additional Features 55
5.1 Module Feature Locations 55
5.2 Debug Connector 56
5.3 Status LEDs 57
5.4 Exception Codes 58
5.5 Fan Connector 59
5.6 BIOS Default Reset Button 60
5.7 BIOS Boot Select 61
6. System Resources 62
6.1 System Memory Map 62
6.2 I/O Map 66
6.3 Interrupt Request (IRQ) Lines 68
6.4 PCI Configuration Space Map 70
6.5 PCI Interrupt Routing Map 71
6.6 SMBus Address Table 71
7. BIOS Setup 72
7.1 Menu Structure 72
7.2 Main 73
7.2.1 BIOS Information 73
7.2.2 System Information 74
7.2.3 Board Information 74
7.2.4 System Date and Time 75
7.3 Advanced 76

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7.3.1 CPU Configuration 76
7.3.2 Power & Performance Configuration 77
7.3.3 Intel® Time Coordinated Computing 87
7.3.4 Graphic Configuration 89
7.3.5 Power Management 91
7.3.6 System Management 92
7.3.7 Thermal Management 93
7.3.8 Watchdog Timer 94
7.3.9 Super I/O Configuration 95
7.3.10 Miscellaneous 96
7.3.11 USB Configuration 97
7.3.12 NVMe Configuration 98
7.3.13 AMI Graphics Output Protocol Policy 98
7.3.14 Serial Console Redirection 98
7.3.15 Network Stack Configuration 100
7.3.16 Trusted Computing 100
7.4 Chipset 101
7.4.1 System Agent (SA) Configuration 101
7.4.2 PCH-I/O Configuration 106
7.5 Security 114
7.5.1 Secure Boot menu 114
7.6 Boot 115
7.6.1 Boot Configuration 115
7.7 Save & Exit 116

8. BIOS Checkpoints, Beep Codes 117
8.1 Status Code Ranges 118
8.2 Standard Status Codes 119
8.2.1 SEC Phase 119
8.2.2 SEC Beep Codes 120
8.2.3 PEI Phase 120
8.2.4 PEI Beep Codes 124
8.2.5 DXE Status Codes 125
8.2.6 DXE Beep Codes 129
8.2.7 ACPI/ASL Checkpoint 130
8.3 OEM-Reserved Checkpoint Ranges 131

9. Software Support 132
9.1 Operation System 132
9.2 Other Software 132

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10. Mechanical and Thermal 133
10.1 Module Dimensions – Top View 133
10.2 Module Dimensions – Side View 134
10.3 Height of Processor and Static Compressive Load 134
10.4 Thermal Solutions 135
10.4.1 Heatspreader: HTS 135
10.4.2 Heatsink: THS 136
10.4.3 Heatsink High Profile: THSH 137
10.4.4 Heatsink with Fan: THSF 138
10.5 Board to Board Connectors 139
10.6 Mounting Method 140
10.7 Standoff Types 141
10.8 Installation 142

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List of Figures

Figure 1 – Module function diagram 21
Figure 2 - Module rear side row and pin numbering 22
Figure 3 – Module feature locations (top side) 55
Figure 5 – cExpress-ASL and debug module 56
Figure 6 – Module mechanical dimensions 134
Figure 7 – Heatspreader: HTS 135
Figure 8 – Heatsink: THS 136
Figure 9 – Heatsink high profile: THSH 137
Figure 10 – Heatsink with fan: THSF 138

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1. Introduction

The cExpress-ASL/ALN is a COM.0 R3.1-compliant COM Express® Compact Size Type 6 module powered by Intel® Atom® x7000 series processors (formerly "Amston Lake and Alder Lake N"). It features up to 8 Gracemont architecture cores, offering scalability from 2 to 8 cores with a thermal design power (TDP) range of 6-15W. The module integrates Intel® UHD Graphics Gen12 with up to 32 execution units (EUs), making it ideal for a wide range of IoT applications. Its low power consumption is excellent for industrial automation and robotics control, edge medical equipment, multi-function printers, and more.

The cExpress-ASL/ALN supports up to 16GB (2x 8GB) LPDDR5 memory with a maximum frequency of 4800 MT/s. With Intel's real-time TCC/TSN features and extended longevity in its class, it is designed for mission-critical stationary and mobile edge applications.

The integrated Intel® UHD Graphics Gen12 includes support for OpenGL 4.6, DirectX 12, OpenCL 3.0, Vulkan 1.2, Intel® Clear Video HD Technology, and DirectX Video Acceleration (DXVA) for H.265/HEVC 4K60 10-bit, VP9 hardware codecs, and AV1 hardware decode. It also offers a High Dynamic Range for enhanced picture quality and has upgraded digital content protection to HDCP 2.2. Graphics outputs include LVDS and two DDI ports, which facilitate HDMI®/DVI/DisplayPort and eDP/VGA, with a maximum 4K resolution. Additionally, an optional USB-C port that enables data transfer data and DisplayPort ALT Mode is available as an alternative to DDI 1, based on project requirements. The cExpress-ASL is specifically designed for customers needing essential graphics processing with different configurations, providing a solution to reduce development time by outsourcing custom core logic.

The cExpress-ASL/ALN additionally offers headless CPU SKUs with up to 8 cores at HFM of 2.4GHz. It is well-suited for compute-intensive workload applications, such as entry networks and edge equipment with software-defined network security.

Input/output capabilities include default five PCIe Gen3 lanes, with the option to expand to a maximum of eight PCIe Gen3 lanes based on project requirements. The module provides a single onboard 2.5 Gigabit Ethernet port with optional Time-Sensitive Network (TSN) support, up to 4x USB 3.2/2.0 ports via USB hub, 4x USB 2.0 ports, and up to 2x SATA 6 Gb/s ports. An optional onboard eMMC with a minimum capacity of 32GB is available based on project needs, as well as an additional FFC connector for one MIPI-CSI 4 lanes camera, also provided on a project basis. Support is provided for SMBus and I2C. The module features SPI AMI EFI BIOS with CMOS backup, supporting a remote console, a hardware monitor, and a watchdog timer.

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2. Specifications

2.1 Core System

CPU

Intel® Atom® x7000 RE and C series Processor (formerly Amston Lake)

- Intel® Atom® x7835RE, 1.3(3.6) GHz, 12W, 8C/32EU (IBECC, TCC/TSN capable)
- Intel® Atom® x7433RE, 1.5(3.4) GHz, 9W, 4C/32EU (IBECC, TCC/TSN capable)
- Intel® Atom® x7213RE, 2.0(3.4) GHz, 9W, 2C/16EU (IBECC, TCC/TSN capable)
- Intel® Atom® x7211RE, 1.0(3.2) GHz, 6W, 2C/16EU (IBECC, TCC/TSN capable)
- Intel® Atom® x7809C, 2.4(3.6) GHz, 25W, 8C (IBECC, TCC/TSN capable) (no GPU/Headless)
- Intel® Atom® x7405C, 2.2(3.4) GHz, 12W, 4C (IBECC, TCC/TSN capable) (no GPU/Headless)
- Intel® Atom® x7203C, 2.0(3.2) GHz, 9W, 2C (IBECC, TCC/TSN capable) (no GPU/Headless)

Intel® Atom® x7000 E & N series Processor (formerly Alder Lake N)

- Intel® Atom® x7425E, 1.5(3.4) GHz, 12W, 4C/24EU (IBECC, TCC/TSN capable)
- Intel® Atom® x7213E, 1.7(3.2) GHz, 10W, 2C/16EU (IBECC, TCC/TSN capable)
- Intel® Atom® x7211E, 1.0(3.2) GHz, 6W, 2C/16EU (IBECC, TCC/TSN capable)
- Intel® Atom® x7211RE, 1.0(3.2) GHz, 6W, 2C/16EU (IBECC, TCC/TSN capable)
- Intel® Core® i3-N305, 1.8(3.8) GHz, 15W, 8C/32EU (IBECC capable)
- Intel® Processor® N200, 1.0(3.7) GHz, 6W, 4C/32EU (IBECC capable)
- Intel® Processor® N97, 2.0(3.6) GHz, 12W, 4C/24EU (IBECC capable)
- Intel® Processor® N50, 1.0(3.4) GHz, 6W, 2C/16EU (IBECC capable)

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Supporting: Intel® VT (including VT-x, VT-d, VT-x with Extended Page Tables), Intel® SSE4.2, Intel® 64 Architecture, Intel® AVX2, Intel® OS Guard, Intel® Boot Guard, Mode-based Execute Control, Intel® AES-NI (availability of features may vary between processor SKUs)

Note: TCC/TSN and IBECC capabilities and headless SKUs are available on a project basis. Please note that not all SKUs are standard in terms of features, they may vary based on specific requirements. For detailed ordering information, refer to the datasheet or contact your local ADLINK representative.

Memory

Up to 16GB (2x 8GB) soldered down LPDDR5, maximum 4800 MT/s. Memory capacity ranges from 4GB, 8GB to 16GB.
IBECC is supported on a project basis with specific BIOS and HW settings.

Note: Please contact your local ADLINK representative for the standard memory configuration.

Embedded BIOS

AMI Aptio V UEFI with CMOS backup in 32 MB SPI BIOS, dual BIOS by build option

2.2 Video

GPU

Gen12 Intel® UHD Graphics architecture with up to 32 execution units

Supported Features

- 3 independent and simultaneous combinations of DisplayPort/HDMI/LVDS/eDP/VGA and display alternative mode through USB-C graphics outputs (4x 4K @60Hz)
- eDP optional in place of LVDS, VGA optional in place of DDI 2, USB-C optional in place of DDI 1 (build option required)
- DirectX Video Acceleration (DXVA) support for accelerated video processing
- 4K60 8b AVC, 4K60 10b HEVC/VP9/SCC, 4K60 10b AV1 HW decode

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- 4K60 8b AVC, 4K60 10b HEVC/VP9/SCC HW encode
- DirectX up to 12
- OpenGL up to 4.6 support
- OpenCL up to 3.0 support
- Vulkan up to 1.2 support
- Graphics HW Virtualization (SR-IOV) support
- HDCP 2.2 capable

Note: Availability of features is dependent on the operating system used (Windows 10 LTSC 64-bit, Windows 11 LTSC 64-bit, Linux 64-bit).

2.2.1 Display Interface Support

LVDS: Single/dual channel 18/24-bit LVDS through eDP to LVDS IC, it supports DE mode and Hsync/Vsync mode.
Max. resolution 1920x1200@60Hz in dual mode. Pixel clock frequency up to 112 MHz. VESA and JEIDA panel data formats are supported.

eDP: eDP 1.4b up to 4 lane support, in place of LVDS (build option)

DDI x2: Digital Display Ports (DDI) support DisplayPort 1.4, HDMI 2.0b or DVI

VGA: VGA support, in place of DDI 2; max. resolution 1920x1200@60Hz (build option)

USB-C DP Alternative mode: DP output through USB Type C connector, in place of DDI 1 (build option)

Note: USB-C is a build option (HW and BIOS) supported on a project basis in place of DDI 1 channels. USB-C support also requires specific carrier board design.

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2.3 Audio

Intel® HD Audio integrated

Located on the carrier Express-BASE6 or Express-BASE6 R3.1 (ALC886 standard support)

2.4 Expansion Bus

5 PCI Express x1 Gen3 default, maximum 8 PCI Express Lanes:

Lane 0-1 (configurable to 2 x1 or 1 x2)

Lane 2-3 (configurable to 2 x1 or 1 x2)

Lane 4 (1 x1)

Lane 5-7 (3 x1) (build option, PCIe lane 5 muxed with SATA 1, PCIe lane 6 muxed with SATA 0, PCIe lane 7 muxed with GbE Ethernet)

Up to 5 PCIe based devices, including on-board i226 LAN controller

Other: SMBus (system), I^2C (user), LPC bus (via eSPI to LPC bridge IC), GSPI (build option)

I2C from CPU is supported by build option and project basis

SMBus from EC (embedded controller) is supported by build option and project basis

Additional GP_SPI (general purpose SPI by project basis)

2.5 Ethernet

2.5GbE Intel® Ethernet Controller I226 Series (V, IT or LM version)

Supports up to 2.5GbE and 1000/100/10 Mbit/s connections

IT version supports the TSN feature on Linux OS. GbE0_SDP is available if TSN support is enabled (build option, also paired with selected CPU SKU).

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2.6 Multi I/O and Storage

USB

2x USB 3.2/2.0/1.1 (USB 0,1), 6x USB 2.0/1.1 (USB 2,3,4,5,6,7)

Up to 4x USB 3.2/2.0/1.1 (USB 0,1,2,3) through a USB 3 hub (build option)

SuperSpeedPlus, SuperSpeed, High-Speed, Full-Speed and Low-Speed USB signaling

Note: The carrier board must be designed for Gen2 operation.
USB 0,1,2, and 3 are backward compatible with USB 2.0/1.1.

USB Type-C

1x USB-C is supported as a build option, in place of DDI 1. HW and BIOS settings are required and it also depends on the carrier board design.
Up to USB 3.2 speed data transmission and DP alternative mode.

SATA

2x SATA 6Gb/s (SATA 0,1)

SATA 0 muxed with PCIe lane 6. SATA 1 muxed with PCIe lane 5.

Note: For SATA 6Gb/s compatibility, it is strongly recommended to use a SATA redriver on the carrier board

GPIO ~~or SD~~

4 GPO and 4 GPI (GPI with interrupt)

GPIO default from EC, build option from CPU

On-board Storage

Soldered type eMMC 5.1, available capacities: 32GB to 128GB. Build option supported on a project basis.

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UART

Two UART interfaces SER0 and SER1 RX/TX on module

Console Redirection via COM 1 or COM 2 selectable in BIOS

Up to 4 serial ports supported by standard BIOS, including Super I/O on carrier board

COM Port	Description	IRQ	Address	Console Redirection Support
COM 1	Supported by module (SER0, A98/A99), via the embedded controller	4	0x3F8	Yes
COM 2	Supported by module (SER1, A101/A102), via the embedded controller	3	0x2F8	Yes
COM 3	Supported by Super I/O (W83627DHG) on the carrier board	5	0x240	Yes
COM 4	Supported by Super I/O (W83627DHG) on the carrier board	7	0x248	Yes

Note: SER0 and SER1 from the SoC HSUART are build options supported on a project basis.

2.7 Trusted Platform Module (TPM)

Chipset: Infineon solution

Type: TPM 2.0 (SPI bus based)

2.8 SEMA Board Controller

Supports: Voltage/current monitoring, power sequence debug support, AT/ATX mode control, logistics and forensic information, flat panel control, general-purpose I^2C, failsafe BIOS (dual BIOS, build option support), watchdog timer, and fan control.

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2.9 Debug

30-pin flat cable connector for use with DB-30 x86 debug module.

Supports embedded controller access, SPI BIOS flashing, internal power rail test points, and debug LEDs.

2.10 Power

Power Modes: AT and ATX mode (AT mode startup controlled by SEMA Board Controller)

Standard Voltage Input:	ATX: 12V±5% / 5Vsb ±5%	or	AT: 12V±5%
Wide Voltage Input:	ATX: 8.5-20V, 5Vsb ±5%	or	AT: 8.5-20V

Power Management: ACPI 5.0 compliant, Smart Battery support
Power States: C1-C6, S0, S3, S4, S5, S5 ECO mode (Wake-on-USB S3/S4, WoL S3/S4/S5)
ECO Mode support for deep S5 for 5Vsb power saving

Power Consumption
Please contact your ADLINK representative for the document "COM Express Module Power Consumption".

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2.11 Mechanical and Environmental

Form Factor and specification

PICMG COM Express Rev 3.1 (COM.0 R3.1), Type 6, Compact size 95 x 95 mm

Operating Temperature

Standard	0°C to 60°C (wide voltage input)	Storage: -20°C to 80°C
Extreme Rugged	-40°C to 85°C	Storage: -40°C to 85°C (extreme rugged, build option by project basis)

Humidity

5-90% RH operating, non-condensing, 5-95% RH storage (and operating with conformal coating)

Shock and Vibration

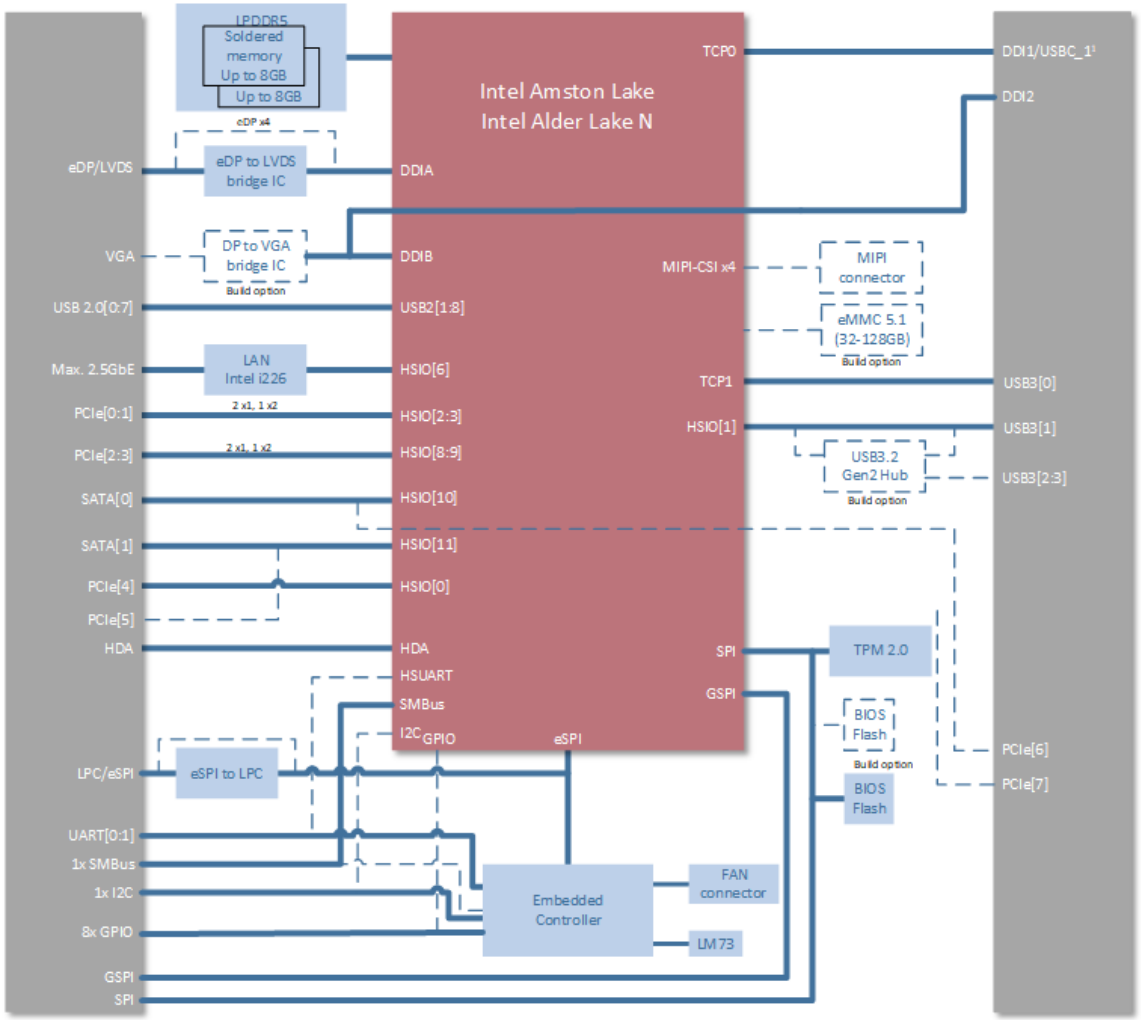
IEC 60068-2-64 and IEC-60068-2-27
MIL-STD-202F, Method 213B, Table 213-I, Condition A and Method 214A, Table 214-I, Condition D

HALT tested

Thermal Stress, Vibration Stress, Thermal Shock and Combined Test

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3. Block Diagram



Note: OEM BIOS can support USB-C via DDI1 port.

Figure 1 – Module function diagram

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4. Pinout and Signal Descriptions

4.1 Pin Summary

The table below is a comprehensible list of all signal pins supported on the dual 220-pin COM Express connectors as defined for Type 6 in the PICMG COM.0 R3.1 specification. Signals described in the specification but not supported on the cExpress-ASL/ALN are marked with ~~strikethrough.~~

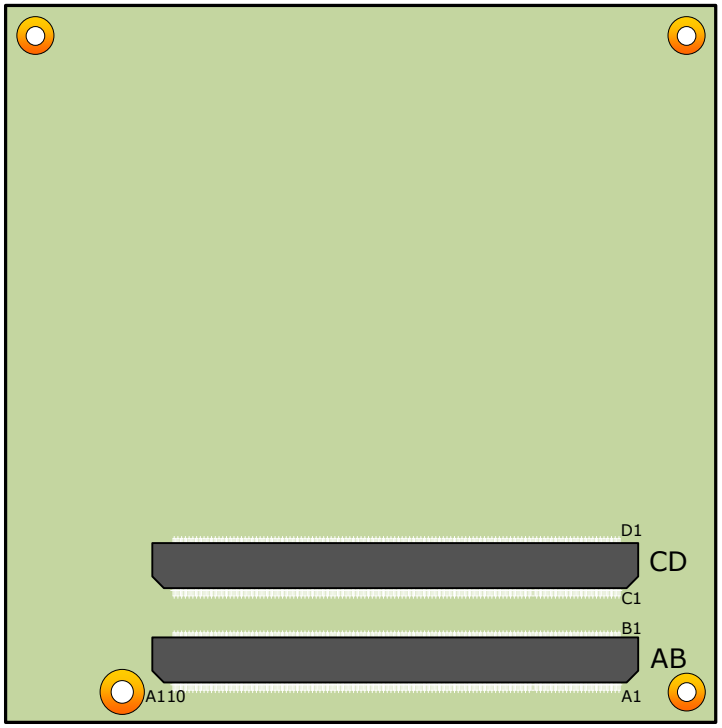


Figure 2 - Module rear side row and pin numbering

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Row A		Row B		Row C		Row D	
A1	GND (FIXED)	B1	GND (FIXED)	C1	GND FIXED)	D1	GND FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#	C2	GND	D2	GND
A3	GBE0_MDI3+	B3	LPC_FRAME#/ESPI_CS0#[1]	C3	USB_SSRX0-	D3	USB_SSTX0-
A4	GBE0_LINK_MID#	B4	LPC_AD0/ESPI_IO_0[1]	C4	USB_SSRX0+	D4	USB_SSTX0+
A5	GBE0_LINK_MAX#	B5	LPC_AD1/ESPI_IO_1[1]	C5	GND	D5	GND
A6	GBE0_MDI2-	B6	LPC_AD2/ESPI_IO_2[1]	C6	USB_SSRX1-	D6	USB_SSTX1-
A7	GBE0_MDI2+	B7	LPC_AD3/ESPI_IO_3[1]	C7	USB_SSRX1+	D7	USB_SSTX1+
A8	GBE0_LINK#	B8	~~LPC_DRQ0#/ESPI_ALERT0#~~	C8	GND	D8	GND
A9	GBE0_MDI1-	B9	~~LPC_DRQ1#/ESPI_ALERT1#~~	C9	USB_SSRX2-[1]	D9	USB_SSTX2-[1]
A10	GBE0_MDI1+	B10	LPC_CLK/ESPI_CK[1]	C10	USB_SSRX2+[1]	D10	USB_SSTX2+[1]
A11	GND (FIXED)	B11	GND (FIXED)	C11	GND (FIXED)	D11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#	C12	USB_SSRX3-[1]	D12	USB_SSTX3-[1]
A13	GBE0_MDI0+	B13	SMB_CK	C13	USB_SSRX3+[1]	D13	USB_SSTX3+[1]
A14	~~GBE0_CTREF~~	B14	SMB_DAT	C14	GND	D14	GND
A15	SUS_S3#	B15	SMB_ALERT#	C15	USB4_1_LSTX[1]	D15	DDI1_CTRLCLK_AUX+ /USB4_1_AUX+[1]
A16	SATA0_TX+	B16	SATA1_TX+	C16	USB4_1_LSRX[1]	D16	DDI1_CTRLDATA_AUX- /USB4_1_AUX-[1]
A17	SATA0_TX-	B17	SATA1_TX-	C17	USB4_RT_ENA[1]	D17	USB4_PD_I2C_ALERT#[1]
A18	SUS_S4#	B18	SUS_STAT#/ESPI_RESET#[1]	C18	GND	D18	PMCALERT#[1]
A19	SATA0_RX+	B19	SATA1_RX+	C19	PCIE_RX6+[1]	D19	PCIE_TX6+[1]
A20	SATA0_RX-	B20	SATA1_RX-	C20	PCIE_RX6-[1]	D20	PCIE_TX6-[1]
A21	GND (FIXED)	B21	GND (FIXED)	C21	GND (FIXED)	D21	GND (FIXED)
A22	~~SATA2_TX+~~	B22	~~SATA3_TX+~~	C22	PCIE_RX7+[1]	D22	PCIE_TX7+[1]
A23	~~SATA2_TX-~~	B23	~~SATA3_TX-~~	C23	PCIE_RX7-[1]	D23	PCIE_TX7-[1]
A24	SUS_S5#	B24	PWR_OK	C24	DDI1_HPD	D24	GND
A25	~~SATA2_RX+~~	B25	~~SATA3_RX+~~	C25	SML0_CLK[1]	D25	GND
A26	~~SATA2_RX-~~	B26	~~SATA3_RX-~~	C26	SML0_DAT[1]	D26	DDI1_PAIR0+ /USB4_1_SSTX0+[1]
A27	BATLOW#	B27	WDT	C27	SML1_CLK[1]	D27	DDI1_PAIR0- /USB4_1_SSTX0-[1]
A28	(S)ATA_ACT#	B28	~~HDA_SDIN2~~/SNDW0_CLK[2]	C28	SML1_DAT[1]	D28	GND
A29	HDA_SYNC	B29	HDA_SDIN1/SNDW0_DAT[2]	C29	USB4_PD_I2C_CLK[1]	D29	DDI1_PAIR1+ /USB4_1_SSRX0+[1]
A30	HDA_RST#	B30	HDA_SDIN0	C30	USB4_PD_I2C_DAT[1]	D30	DDI1_PAIR1- /USB4_1_SSRX0-[1]

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Row A		Row B		Row C		Row D	
A31	GND (FIXED)	B31	GND (FIXED)	C31	GND (FIXED)	D31	GND (FIXED)
A32	HDA_BITCLK	B32	SPKR	C32	DDI2_CTRLCLK_AUX+ ~~/USB4_2_AUX+~~	D32	DDI1_PAIR2+ /USB4_1_SSTX1+[1]
A33	HDA_SDOUT	B33	I2C_CK	C33	DDI2_CTRLDATA_AUX- ~~/USB4_2_AUX-~~	D33	DDI1_PAIR2- /USB4_1_SSTX1-[1]
A34	BIOS_DIS0#/ESPI_SAFS[1]	B34	I2C_DAT	C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL
A35	THRMTRIP#	B35	THRM#	C35	USB4_2_LSTX[1]	D35	USB4_2_LSRX[1]
A36	USB6-	B36	USB7-	C36	~~DDI3_CTRLCLK_AUX+~~	D36	DDI1_PAIR3+ /USB4_1_SSRX1+[1]
A37	USB6+	B37	USB7+	C37	~~DDI3_CTRLDATA_AUX-~~	D37	DDI1_PAIR3- /USB4_1_SSRX1-[1]
A38	USB_6_7_OC#	B38	USB_4_5_OC#	C38	~~DDI3_DDC_AUX_SEL~~	D38	GND
A39	USB4-	B39	USB5-	C39	~~DDI3_PAIR0+~~	D39	DDI2_PAIR0+ ~~/USB4_2_SSTX0+~~
A40	USB4+	B40	USB5+	C40	~~DDI3_PAIR0-~~	D40	DDI2_PAIR0- ~~/USB4_2_SSTX0-~~
A41	GND (FIXED)	B41	GND (FIXED)	C41	GND (FIXED)	D41	GND (FIXED)
A42	USB2-	B42	USB3-	C42	~~DDI3_PAIR1+~~	D42	DDI2_PAIR1+ ~~/USB4_2_SSRX0+~~
A43	USB2+	B43	USB3+	C43	~~DDI3_PAIR1-~~	D43	DDI2_PAIR1- ~~/USB4_2_SSRX0-~~
A44	USB_2_3_OC#	B44	USB_0_1_OC#	C44	~~DDI3_HPD~~	D44	DDI2_HPD
A45	USB0-	B45	USB1-	C45	GP_SPI_CS#[2]	D45	GND
A46	USB0+	B46	USB1+	C46	~~DDI3_PAIR2+~~	D46	DDI2_PAIR2+ ~~/USB4_2_SSTX1+~~
A47	VCC_RTC	B47	ESPI_EN#[1]	C47	~~DDI3_PAIR2-~~	D47	DDI2_PAIR2- ~~/USB4_2_SSTX1-~~
A48	RSMRST_OUT#	B48	~~USB0_HOST_PRSNT~~	C48	RSVD	D48	GND
A49	GBE0_SDP[1]	B49	SYS_RESET#	C49	~~DDI3_PAIR3+~~	D49	DDI2_PAIR3+ ~~/USB4_2_SSRX1+~~
A50	LPC_SERIRQ/ESPI_CS1#[1]	B50	CB_RESET#	C50	~~DDI3_PAIR3-~~	D50	DDI2_PAIR3- ~~/USB4_2_SSRX1-~~
A51	GND (FIXED)	B51	GND (FIXED)	C51	GND (FIXED)	D51	GND (FIXED)
A52	PCIE_TX5+[1]	B52	PCIE_RX5+[1]	C52	~~PEG_RX0+~~	D52	~~PEG_TX0+~~
A53	PCIE_TX5-[1]	B53	PCIE_RX5-[1]	C53	~~PEG_RX0-~~	D53	~~PEG_TX0-~~
A54	GPI0	B54	GPO1	C54	TYPE0#	D54	~~PEG_LANE_RV#~~
A55	PCIE_TX4+	B55	PCIE_RX4+	C55	~~PEG_RX1+~~	D55	~~PEG_TX1+~~

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A56	PCIE_TX4-	B56	PCIE_RX4-	C56	~~PEG_RX1-~~	D56	~~PEG_TX1-~~
A57	GND	B57	GPO2	C57	TYPE1#	D57	TYPE2#
A58	PCIE_TX3+	B58	PCIE_RX3+	C58	~~PEG_RX2+~~	D58	~~PEG_TX2+~~
A59	PCIE_TX3-	B59	PCIE_RX3-	C59	~~PEG_RX2-~~	D59	~~PEG_TX2-~~
A60	GND (FIXED)	B60	GND (FIXED)	C60	GND (FIXED)	D60	GND (FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+	C61	~~PEG_RX3+~~	D61	~~PEG_TX3+~~
A62	PCIE_TX2-	B62	PCIE_RX2-	C62	~~PEG_RX3-~~	D62	~~PEG_TX3-~~
A63	GPI1	B63	GPO3	C63	GND	D63	GND
A64	PCIE_TX1+	B64	PCIE_RX1+	C64	GND	D64	GND
A65	PCIE_TX1-	B65	PCIE_RX1-	C65	~~PEG_RX4+~~	D65	~~PEG_TX4+~~
A66	GND	B66	WAKE0#	C66	~~PEG_RX4-~~	D66	~~PEG_TX4-~~
A67	GPI2	B67	WAKE1#	C67	~~RAPID_SHUTDOWN~~	D67	GND
A68	PCIE_TX0+	B68	PCIE_RX0+	C68	~~PEG_RX5+~~	D68	~~PEG_TX5+~~
A69	PCIE_TX0-	B69	PCIE_RX0-	C69	~~PEG_RX5-~~	D69	~~PEG_TX5-~~
A70	GND (FIXED)	B70	GND (FIXED)	C70	GND (FIXED)	D70	GND (FIXED)
A71	LVDS_A0+ / eDP_TX2+[1]	B71	LVDS_B0+	C71	~~PEG_RX6+~~	D71	~~PEG_TX6+~~
A72	LVDS_A0- / eDP_TX2-[1]	B72	LVDS_B0-	C72	~~PEG_RX6-~~	D72	~~PEG_TX6-~~
A73	LVDS_A1+ / eDP_TX1+[1]	B73	LVDS_B1+	C73	GND	D73	GND
A74	LVDS_A1- / eDP_TX1-[1]	B74	LVDS_B1-	C74	~~PEG_RX7+~~	D74	~~PEG_TX7+~~
A75	LVDS_A2+ / eDP_TX0+[1]	B75	LVDS_B2+	C75	~~PEG_RX7-~~	D75	~~PEG_TX7-~~
A76	LVDS_A2- / eDP_TX0-[1]	B76	LVDS_B2-	C76	GND	D76	GND
A77	LVDS_VDD_EN / eDP_VDD_EN[1]	B77	LVDS_B3+	C77	GND	D77	GND
A78	LVDS_A3+	B78	LVDS_B3-	C78	~~PEG_RX8+~~	D78	~~PEG_TX8+~~
A79	LVDS_A3-	B79	LVDS_BKLT_EN	C79	~~PEG_RX8-~~	D79	~~PEG_TX8-~~
A80	GND (FIXED)	B80	GND (FIXED)	C80	GND (FIXED)	D80	GND (FIXED)
A81	LVDS_A_CK+ / eDP_TX3+[1]	B81	LVDS_B_CK+	C81	~~PEG_RX9+~~	D81	~~PEG_TX9+~~
A82	LVDS_A_CK- / eDP_TX3-[1]	B82	LVDS_B_CK-	C82	~~PEG_RX9-~~	D82	~~PEG_TX9-~~
A83	LVDS_I2C_CK / eDP_AUX+[1]	B83	LVDS_BKLT_CTRL / eDP_BKLT_CTRL[1]	C83	GND	D83	GND
A84	LVDS_I2C_DAT / eDP_AUX-[1]	B84	VCC_5V_SBY	C84	GND	D84	GND
A85	GPI3	B85	VCC_5V_SBY	C85	~~PEG_RX10+~~	D85	~~PEG_TX10+~~
A86	GP_SPI_MOSI[2]	B86	VCC_5V_SBY	C86	~~PEG_RX10-~~	D86	~~PEG_TX10-~~
A87	eDP_HPD	B87	VCC_5V_SBY	C87	GND	D87	GND
A88	PCIE_CK_REF+	B88	BIOS_DIS1#	C88	~~PEG_RX11+~~	D88	~~PEG_TX11+~~
A89	PCIE_CK_REF-	B89	VGA_RED[1]	C89	~~PEG_RX11-~~	D89	~~PEG_TX11-~~
A90	GND (FIXED)	B90	GND (FIXED)	C90	GND (FIXED)	D90	GND (FIXED)
A91	SPI_POWER	B91	VGA_GRN[1]	C91	~~PEG_RX12+~~	D91	~~PEG_TX12+~~
A92	SPI_MISO	B92	VGA_BLU[1]	C92	~~PEG_RX12-~~	D92	~~PEG_TX12-~~

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Row A		Row B		Row C		Row D	
A93	GPO0	B93	VGA_HSYNC[1]	C93	GND	D93	GND
A94	SPI_CLK	B94	VGA_VSYNC[1]	C94	~~PEG_RX13+~~	D94	~~PEG_TX13+~~
A95	SPI_MOSI	B95	VGA_I2C_CK[1]	C95	~~PEG_RX13-~~	D95	~~PEG_TX13-~~
A96	TPM_PP	B96	VGA_I2C_DAT[1]	C96	GND	D96	GND
A97	TYPE10#	B97	SPI_CS#	C97	GND	D97	GND
A98	SER0_TX	B98	GP_SPI_MISO[2]	C98	~~PEG_RX14+~~	D98	~~PEG_TX14+~~
A99	SER0_RX	B99	GP_SPI_CK[2]	C99	~~PEG_RX14-~~	D99	~~PEG_TX14-~~
A100	GND (FIXED)	B100	GND (FIXED)	C100	GND (FIXED)	D100	GND (FIXED)
A101	SER1_TX~~/CAN_TX~~	B101	FAN_PWMOUT	C101	~~PEG_RX15+~~	D101	~~PEG_TX15+~~
A102	SER1_RX~~/CAN_RX~~	B102	FAN_TACHIN	C102	~~PEG_RX15-~~	D102	~~PEG_TX15-~~
A103	LID#	B103	SLEEP#	C103	GND	D103	GND
A104	VCC_12V	B104	VCC_12V	C104	VCC_12V	D104	VCC_12V
A105	VCC_12V	B105	VCC_12V	C105	VCC_12V	D105	VCC_12V
A106	VCC_12V	B106	VCC_12V	C106	VCC_12V	D106	VCC_12V[1]
A107	VCC_12V	B107	VCC_12V	C107	VCC_12V	D107	VCC_12V
A108	VCC_12V	B108	VCC_12V	C108	VCC_12V	D108	VCC_12V
A109	VCC_12V	B109	VCC_12V	C109	VCC_12V	D109	VCC_12V
A110	GND (FIXED)	B110	GND (FIXED)	C110	GND (FIXED)	D110	GND (FIXED)

Note: ~~Strike-through~~ entries are not supported functions on this product.

1. eDP (in place of LVDS), VGA (in place of DDI 2), eSPI (in place of LPC), PCIe lanes 5-7 (muxed with SATA 1/0 and GbE Ethernet), USB4_1 (in place of DDI 1, used as USB Type-C, not USB4), and GBE0_SDP (for selected LAN controller versions) are build options supported on a project basis

2. GP_SPI support is to be confirmed (TBC).

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4.2 Signal Terminology Descriptions

Definitions of terms used for signal description tables

Term	Description
I	Input to the module
O	Output from the module
I/O	Bi-directional Input / Output
OD	Open drain output from the module
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I/O $3.3V_{SB}$	Input or output 3.3V tolerant active in standby state
DDC	Display Data Channel
PCIE	PCI Express compatible differential signal
PEG	PCI Express Graphics
SATA	Serial ATA specification Revision 2.6 and 3
LVDS	Low Voltage Differential Signal - 330 mV nominal; 450 mV maximum differential signal
P	Power Input / Output
REF	Reference voltage output. May be sourced from a Module power plane.
PDS	Pull-down strap. A Module output pin that is either tied to GND or is not connected. Used to signal Module capabilities to the Carrier Board.
PU	PU (pull-up) resistor on module
PD	PD (pull-down) resistor on module

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4.3 AB Connector Signal Descriptions

4.3.1 Audio

Name	Pin #	Description	I/O	PU / PD	Comment
AC_RST# / HDA_RST#	A30	Reset output to CODEC, active low.	O 3.3VSB		
AC_SYNC / HDA_SYNC	A29	Sample-synchronization signal to the CODEC(s).	O 3.3VSB		PCH internal PD 20Kohm
AC_BITCLK / HDA_BITCLK	A32	Serial data clock generated by the external CODEC(s).	I/O 3.3VSB		
AC_SDOUT / HDA_SDOUT	A33	Serial TDM data output to the CODEC.	O 3.3VSB		
AC_SDIN[2:0] / HDA_SDIN[2:0]	~~B28~~ B29 B30	Serial TDM data inputs from up to 3 CODECs.	I/O 3.3VSB		PCH internal PD 20Kohm AC_SDNI2/HDA_SDIN2 not supported

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4.3.2 Analog VGA

Name	Pin #	Description	I/O	PU / PD	Comment
VGA_RED	B89	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	
VGA_GRN	B91	Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3V		
VGA_VSYNC	B94	Vertical sync output to VGA monitor	O 3.3V		
VGA_I2C_CK	B95	DDC clock line (I^2C port dedicated to identifying VGA monitor capabilities)	I/O OD 3.3V	PU 2k2 3.3V	
VGA_I2C_DAT	B96	DDC data line.	I/O OD 3.3V	PU 2k2 3.3V	

Note: VGA is a build option supported on a project basis (in place of DDI 2).

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4.3.3 LVDS or eDP

The module default supports a single or dual channel LVDS display panel with up to 24-bit colors. A BOM option is available that removes the eDP to LVDS bridge IC and outputs the eDP signals directly. The pin mapping between eDP vs LVDS modes is described below.

Pin #	LVDS mode	eDP mode
A71	LVDS_A0+	eDP_TX2+
A72	LVDS_A0-	eDP_TX2-
A73	LVDS_A1+	eDP_TX1+
A74	LVDS_A1-	eDP_TX1-
A75	LVDS_A2+	eDP_TX0+
A76	LVDS_A2-	eDP_TX0-
A78	LVDS_A3+	-
A79	LVDS_A3-	-
A81	LVDS_A_CK+	eDP_TX3+
A82	LVDS_A_CK-	eDP_TX3-
B71	LVDS_B0+	-
B72	LVDS_B0-	-
B73	LVDS_B1+	-
B74	LVDS_B1-	-
B75	LVDS_B2+	-
B76	LVDS_B2-	-
B77	LVDS_B3+	-
B78	LVDS_B3-	-
B81	LVDS_B_CK+	-
B82	LVDS_B_CK-	-
A77	LVDS_VDD_EN	eDP_VDD_EN
B79	LVDS_BKLT_EN	eDP_BKLT_EN
B83	LVDS_BKLT_CTRL	eDP_BKLT_CTRL
A83	LVDS_I2C_CK	eDP_AUX+
A84	LVDS_I2C_DAT	eDP_AUX-
A87	-	eDP_HPD

Note: LVDS is the default mode, and eDP is a build option.

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4.3.3.1 Single/Dual Channel LVDS (default)

Name	Pin #	Description	I/O	PU / PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS Channel A differential clock	O LVDS		
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	B71 B72 B73 B74 B75 B76 B77 B78	LVDS Channel B differential pairs	O LVDS		
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS Channel B differential clock	O LVDS		
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 100K	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V	PD 100K	
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V	PD 100K	
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control.	O 3.3V	PU 2k2 3.3V	
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 2k2 3.3V	

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4.3.3.2 4-lane eDP

Name	Pin #	Description	I/O	PU / PD	Comment
eDP_TX3+ eDP_TX3- eDP_TX2+ eDP_TX2- eDP_TX1+ eDP_TX1- eDP_TX0+ eDP_TX0-	A81 A82 A71 A72 A73 A74 A75 A76	eDP differential pairs	O PCIe		AC coupled off module
eDP_VDD_EN	A77	eDP power enable function	O 3.3V	PD 100K	
eDP_BKLT_EN	B79	eDP backlight enable function	O 3.3V	PD 100K	
eDP_BKLT_CTRL	B83	eDP backlight brightness control	O 3.3V	PD 100K	
eDP_AUX+	A83	eDP AUX+	I/O PCIe		AC coupled off module
eDP_AUX-	A84	eDP AUX-	I/O PCIe		AC coupled off module
eDP_HPD	A87	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	PD 100K on this pin when eDP is supported

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4.3.4 Gigabit Ethernet

Name	Pin #	Description	I/O	PU / PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: **1000 / 100 / 10** MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	I/O Analog		Twisted pair signals for external transformer.
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.	OD 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.	OD 3.3VSB		
GBE0_LINK_MID#	A4	Gigabit Ethernet Controller MID Speed Link indicator. Active low. If active, the link is established but at a speed lower than the maximum speed supported by the Ethernet controller. Note that, based on capabilities of the Ethernet controller used, this signal might not be active for all possible lower link speeds. This module pin should be capable of sinking up to 20 mA at a Voh of 0.4 max. It was GBE0_LINK100# in COM Express Rev. 3.0.	OD 3.3VSB		
GBE0_LINK_MAX#	A5	Gigabit Ethernet Controller MAX Speed Link Indicator. Active low. If active, the link is established at the maximum link speed supported by the controller. This module pin should be capable of sinking up to 20 mA at a Voh of 0.4 max. It was GBE0_LINK1000# in COM Express Rev. 3.0.	OD 3.3VSB		
~~GBE0_CTREF~~	~~A14~~	~~Reference voltage for Carrier Board Ethernet channel 1 and 2 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be 250 mA or less.~~	~~REF~~ ~~GND min~~ ~~3.3V max~~		Not supported
GBE0_SDP	A49	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as 1pps signal.	IO 3.3VSB	GBE0_SDP	Depends on the selection of LAN controller. i226-IT support this pin

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Note: This product supports up to 2.5GbE. The LAN LED behavior is optimized for maximum 2.5GbE speed.
GBE0_LINK_MAX# will be active for 2.5GbE speed indication.
GBE0_LINK_MID# will be active for 1GbE speed indication or lower.
GBE0_ACT# and GBE0_LINK# share the same source from the LAN controller.
For 100Mbit/sec and 10Mbit/sec speed, the LAN LED will be OFF.

4.3.5 SATA

Name	Pin #	Description	I/O	PU / PD	Comment
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		AC coupled on Module
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		AC coupled on Module
~~SATA2_TX+ SATA2_TX-~~	~~A22 A23~~	~~Serial ATA channel 2, Transmit Output differential pair.~~	~~O SATA~~		Not supported
~~SATA2_RX+ SATA2_RX-~~	~~A25 A26~~	~~Serial ATA channel 2, Receive Input differential pair.~~	~~I SATA~~		Not supported
~~SATA3_TX+ SATA3_TX-~~	~~B22 B23~~	~~Serial ATA channel 3, Transmit Output differential pair.~~	~~O SATA~~		Not supported
~~SATA3_RX+ SATA3_RX-~~	~~B25 B26~~	~~Serial ATA channel 3, Receive Input differential pair.~~	~~I SATA~~		Not supported
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	O 3.3V	PU 10K 3.3V	AC coupled on Module

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4.3.5.1 PCH HSIO Lane Assignments

Name	HSIO name on SoC	Comment
SATA0	HSIO 10	SATA 0 muxed with PCIe lane 6. SATA is default
SATA1	HSIO 11	SATA 1 muxed with PCIe lane 5. SATA is default
~~SATA2~~		Not supported
~~SATA3~~		Not supported

4.3.6 PCI Express

Name	Pin #	Description	I/O	PU / PD	Comment
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIe		AC coupled on Module
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIe		AC coupled off Module
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIe		AC coupled on Module
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIe		AC coupled off Module
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIe		AC coupled on Module
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIe		AC coupled off Module
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIe		AC coupled on Module
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIe		AC coupled off Module
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIe		AC coupled on Module
PCIE_RX4+	B55	PCI Express channel 4, Receive Input differential pair.	I PCIe		AC coupled off Module

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PCIE_RX4-	B56				
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIe		AC coupled on Module Build option
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIe		AC coupled off Module Build option
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIe		

4.3.6.1 PCH HIS Lane Assignments

Name	HSIO name on SoC / Switch IC	Comment
PCIE0	HSIO 2	
PCIE1	HSIO 3	
PCIE2	HSIO 8	
PCIE3	HSIO 9	
PCIE4	HSIO 0	
PCIE5	HSIO 11	PCIe laned 5 muxed with SATA 1, SATA is default
PCIE6	HSIO 10	PCIe laned 6 muxed with SATA 0, SATA is default
PCIE7	HSIO 6	PCIe laned 7 muxed with GbE Ethernet, Ethernet is default

Note: Up to 5 PCIe devices can operate at the same time, including the on-board i226 LAN controller for the GbE Ethernet feature.

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4.3.7 LPC Bus

Name	Pin #	Description	I/O	PU / PD	Comment
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	B4 B5 B6 B7	LPC multiplexed address, command and data bus	I/O 3.3VSB		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3VSB		
LPC_DRQ0# LPC_DRQ1#	B8 B9	LPC serial DMA request	I 3.3V		Not connected
LPC_SERIRQ	A50	LPC serial interrupt	I/O 3.3VSB	PU 8.2K 3.3VSB	
LPC_CLK	B10	LPC clock output –33MHz nominal	O 3.3VSB		The LPC_CLK frequency is 24MHz on this platform

Note: LPC Bus is supported by an eSPI to LPC bridge IC.

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4.3.8 USB

Name	Pin #	Description	I/O	PU / PD	Comment
USB0+ USB0-	A46 A45	USB differential data pairs for Port 0	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB1+ USB1-	B46 B45	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB2+ USB2-	A43 A42	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB3+ USB3-	B43 B42	USB differential data pairs for Port 2	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB4+ USB4-	A40 A39	USB differential data pairs for Port 3	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB5+ USB5-	B40 B39	USB differential data pairs for Port 4	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB6+ USB6-	A37 A36	USB differential data pairs for Port 5	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB7+ USB7-	B37 B37	USB differential data pairs for Port 6	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1 (see *Note)	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on carrier
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3 (see *Note)	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on carrier
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5 (see *Note)	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on carrier
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7 (see *Note)	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on carrier
USB0_HOST_PRSNT	B48	Module USB client may detect the presence of a USB host on USB0. A high value indicates that a host is present.	I 3.3VSB		Not supported

***Note**: A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.

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4.3.9 SPI Bus (BIOS only)

Name	Pin #	Description	I/O	PU / PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3VSB	PU 10K 3.3VSB	
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3VSB	PU 10K 3.3VSB	
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier	O P 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I	PU 10K 3.3VSB	Carrier shall pull to GND or leave not- connected.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I	PU 10K 3.3VSB	Carrier shall pull to GND or leave not- connected

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4.3.10 Miscellaneous

Name	Pin #	Description	I/O	PU / PD	Comment
SPKR	B32	Output for audio enunciator, the "speaker" in PC-AT systems	O 3.3V		
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V	PU 10K 3.3V	
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3VSB	PU 10K 3.3V	
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3VSB	PU 10K 3.3VSB	
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD 3.3V		There shall be PD on the carrier board.
FAN_TACHIN	B102	Fan tachometer input for a fan with a two-pulse output.	I OD 3.3V	PU 47K 3.3V	
TPM_PP	A96	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V	PD 100K	PD is present only when TPM on the module. Modules implementing a TPM shall pull down the signal.

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4.3.11 SMBus

Name	Pin #	Description	I/O	PU / PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line. Power is sourced through the 3.3V standby rail and the main power rails.	I/O OD 3.3VSB	PU 4.7K 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line. Power is sourced through the 3.3V standby rail and the main power rails.	I/O OD 3.3VSB	PU 4.7K 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – an active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power is sourced through the 3.3V standby rail and the main power rails.	I 3.3VSB	PU 10K 3.3VSB	

4.3.12 I²C Bus

Name	Pin #	Description	I/O	PU / PD	Comment
I2C_CK	B33	General purpose I²C port clock output/input	I/O OD 3.3VSB	PU 2.2K 3.3VSB	Source EC as default (chipset by BOM option)
I2C_DAT	B34	General purpose I²C port data I/O line	I/O OD 3.3VSB	PU 2.2K 3.3VSB	Source EC as default (chipset by BOM option)

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4.3.13 General Purpose I/O (GPIO)

Name	Pin #	Description	I/O	PU / PD	Comment
GPO[0]	A93	General purpose output pins.	O 3.3V	PD 10K	After hardware RESET output low
GPO[1]	B54	General purpose output pins.	O 3.3V	PD 10K	After hardware RESET output low
GPO[2]	B57	General purpose output pins.	O 3.3V	PD 10K	After hardware RESET output low
GPO[3]	B63	General purpose output pins.	O 3.3V	PD 10K	After hardware RESET output low
GPI[0]	A54	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[1]	A63	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[2]	A67	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[3]	A85	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	

4.3.14 Serial Interface Signals

Name	Pin #	Description	I/O	PU / PD	Comment
SER0_TX	A98	General purpose serial port transmitter	O CMOS 3.3V		Power rail tolerance 5V, 12V There shall be PD on carrier board
SER0_RX	A99	General purpose serial port receiver	I CMOS 3.3V	PU 10K 3.3V	Power rail tolerance 5V, 12V
SER1_TX	A101	General purpose serial port transmitter	O CMOS 3.3V		Power rail tolerance 5V, 12V There shall be PD on carrier board
SER1_RX	A102	General purpose serial port receiver	I CMOS 3.3V	PU 10K 3.3V	Power rail tolerance 5V, 12V

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4.3.15 Power and System Management

Name	Pin #	Description	I/O	PU / PD	Comment
PWRBTN#	B12	Power button to bring the system out of S5 (soft off), active on the falling edge.	I 3.3VSB	PU 10K 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low request for module to reset and reboot. It may be falling edge sensitive. In situations where SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.	I 3.3VSB	PU 10K 3.3VSB	
CB_RESET#	B50	Reset output from the module to the carrier board. Active low. Issued by module chipset, it may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or it may be initiated by the module software.	O 3.3V		
PWR_OK	B24	Power OK from the main power supply. A high value indicates that the power is good. This signal can be used to delay module startup to allow carrier-based FPGAs or other configurable devices time to be programmed.	I 3.3VSB	PU 10K 3.3VSB	Should have weak pull up.
SUS_STAT#	B18	Indicates an imminent suspend operation; used to notify LPC devices.	O 3.3VSB		
SUS_S3#	A15	Indicates the system is in the Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as "PS_ON") may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
SUS_S4#	A18	Indicates the system is in the Suspend to Disk state. Active low output.	O 3.3VSB		
SUS_S5#	A24	Indicates the system is in the Soft Off state.	O 3.3VSB		
WAKE0#	B66	PCI Express wake-up signal.	I 3.3VSB	PU 8.2K 3.3VSB	
WAKE1#	B67	General purpose wake-up signal. It may be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 8.2K 3.3VSB	Connect to WAKE 0#
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low or it may be used to signal some other external power-management event.	I 3.3VSB	PU 10K 3.3VSB	
LID#	A103	LID button. Low active signal is used by the ACPI operating system for a LID switch.	I OD 3.3VSB	PU 47K 3.3VSB	Emulated on GPIO (BIOS)
SLEEP#	B103	Sleep button. Low active signal is used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I OD 3.3VSB	PU 47K 3.3VSB	Emulated on GPIO (BIOS)
RAPID_ SHUTDOWN	C67	~~Trigger for Rapid Shutdown. Must be driven to 5V though a <=50-ohm source impedance for ≥ 20 µs.~~	I CMOS 5VSB		Not supported

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4.3.16 Power and Ground

Name	Pin #	Description	I/O	PU / PD	Comment
VCC_12V	A104, A105, A106, A107, A108, A109, B104, B105, B106, B107, B109	Primary power input supports a wide range input of 5 — 20V. All available VCC_12V pins on the connector(s) shall be used.	P		8.5-20 V
VCC_5V_SBY	B84, B85, B86, B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		5Vsb ±5%
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path.	P		

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4.4 CD Connector Signal Descriptions

4.4.1 USB 3.0 Extensions

Name	Pin #	Description	I/O	PU / PD	Comment
USB_SSRX0- USB_SSRX0+	C3 C4	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB0	I PCIe		AC coupled off module
USB_SSTX0- USB_SSTX0+	D3 D4	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB0	O PCIe		AC coupled on module
USB_SSRX1- USB_SSRX1+	C6 C7	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB1	I PCIe		AC coupled off module
USB_SSTX1- USB_SSTX1+	D6 D7	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB1	O PCIe		AC coupled on module
USB_SSRX2- USB_SSRX2+	C9 C10	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB2	I PCIe		AC coupled off module Build option through USB Hub
USB_SSTX2- USB_SSTX2+	D9 D10	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB2	O PCIe		AC coupled on module Build option through USB Hub
USB_SSRX3- USB_SSRX3+	C12 C13	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB3	I PCIe		AC coupled off module Build option through USB Hub
USB_SSTX3- USB_SSTX3+	D12 D13	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB3	O PCIe		AC coupled on module Build option through USB Hub

4.4.1.1 USB Root Segmentation

All USB interfaces are derived from the xHCI controller.

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4.4.2 PCI Express

Name	Pin #	Description	I/O	PU / PD	Comment
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair.	O PCIe		AC coupled on Module Build option
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair.	I PCIe		AC coupled off Module Build option
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair.	O PCIe		AC coupled on Module Build option
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair.	I PCIe		AC coupled off Module Build option

4.4.2.1 PCH HSIO Lane Assignments

Refer to section, 4.3.6.1 PCH HSIO Lane Assignments, on page 37.

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4.4.3 DDI1 Port

Name	Pin #	DisplayPort (DP)	HDMI
DDI1_PAIR0+ DDI1_PAIR0-	D26 D27	DP1_LANE0+ DP1_LANE0-	TMDS1_DATA2+ TMDS1_DATA2-
DDI1_PAIR1+ DDI1_PAIR1-	D29 D30	DP1_LANE1+ DP1_LANE1-	TMDS1_DATA1+ TMDS1_DATA1-
DDI1_PAIR2+ DDI1_PAIR2-	D32 D33	DP1_LANE2+ DP1_LANE2-	TMDS1_DATA0+ TMDS1_DATA0-
DDI1_PAIR3+ DDI1_PAIR3-	D36 D37	DP1_LANE3+ DP1_LANE3-	TMDS1_CLK+ TMDS1_CLK-
DDI1_PAIR4+ DDI1_PAIR4-	C25 C26	-	-
DDI1_PAIR5+ DDI1_PAIR5-	C29 C30	-	-
DDI1_PAIR6+ DDI1_PAIR6-	C15 C16	-	-
DDI1_HPD	C24	DP1_HPD	HDMI1_HPD
DDI1_CTRLCLK_AUX+	D15	DP1_AUX+	HMDI1_CTRLCLK
DDI1_CTRLCLK_AUX-	D16	DP1_AUX-	HMDI1_CTRLDATA
DDI1_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL	DDI1_DDC_AUX_SEL

Note: Dual Mode (HDMI and DisplayPort on the same pins) implementations may be realized. This is desirable for SoCs that natively implement this capability. For such SoCs, the primary Dual Mode implementation challenge is that the HDMI_CTRL_DAT and HDMI_CTRL_CK lines are DC coupled, but the DP_AUX+ /- pair must be AC coupled. A set of FET switches is usually used to sort this out. The FET gates can be controlled by the AUX_SEL pin function.

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4.4.3.1 DisplayPort (DP) Mode

Name	Pin #	Description	I/O	PU / PD	Comment
DP1_LANE0+ DP1_LANE0- DP1_LANE1+ DP1_LANE1- DP1_LANE2+ DP1_LANE2- DP1_LANE3+ DP1_LANE3-	D26 D27 D29 D30 D32 D33 D36 D37	DP Port 1, differential pair data lines	O PCIe		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
DP1_HPD	C24	DP Port 1, detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	The module must tolerate a high level in stand-by mode. The carrier board shall include a blocking FET on DP1_HPD to prevent back-drive current from damaging the module.
DP1_AUX+	D15	DP Port 1, Bidirectional Channel used for Link Management and Device Control	I/O PCIe	PD 100K	AC coupled on Module
DP1_AUX-	D16	DP Port 1, Bidirectional Channel used for Link Management and Device Control	I/O PCIe	PU 100K	AC coupled on Module
DDI1_DDC_AUX_SEL	D34	Strapping Signal to select HDMI or DP output 1M pull-down on the module and floating on the carrier that enables DisplayPort mode	I 3.3V	PD 1M	DP mode enabled

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4.4.3.2 HDMI Mode

Name	Pin #	Description	I/O	PU / PD	Comment
TMDS1_DATA2+ TMDS1_DATA2- TMDS1_DATA1+ TMDS1_DATA1- TMDS1_DATA0+ TMDS1_DATA0-	D26 D27 D29 D30 D32 D33	HDMI / DVI Port, Differential Pair Data Lines	O PCIe		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the carrier
TMDS1_CLK+ TMDS1_CLK-	D36 D37	HDMI Port, Differential Pair Clock Lines			
HDMI_HPD	C24	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	
HDMI1_CTRLCLK	D15	I2C_CLK Line for HDMI	I/O PCIe	PU 2.2K	AC couple on module
HDMI1_CTRLDATA	D16	I2C_DAT Line for HDMI	I/O PCIe	PU 2.2K	AC couple on module
DDI1_DDC_AUX_SEL	D34	Strapping Signal to select HDMI or DP output	I 3.3V	PD 1M	HDMI mode enabled

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4.4.4 DDI2 Port

Name	Pin #	DisplayPort (DP)	HDMI
DDI2_PAIR0+ DDI2_PAIR0-	D39 D40	DP2_LANE0+ DP2_LANE0-	TMDS2_DATA2+ TMDS2_DATA2-
DDI2_PAIR1+ DDI2_PAIR1-	D42 D43	DP2_LANE1+ DP2_LANE1-	TMDS2_DATA1+ TMDS2_DATA1-
DDI2_PAIR2+ DDI2_PAIR2-	D46 D47	DP2_LANE2+ DP2_LANE2-	TMDS2_DATA0+ TMDS2_DATA0-
DDI2_PAIR3+ DDI2_PAIR3-	D49 D50	DP2_LANE3+ DP2_LANE3-	TMDS2_CLK+ TMDS2_CLK-
DDI2_HPD	D44	DP2_HPD	HDMI2_HPD
DDI2_CTRLCLK_AUX+	C32	DP2_AUX+	HMDI2_CTRLCLK
DDI2_CTRLCLK_AUX-	C33	DP2_AUX-	HMDI2_CTRLDATA
DDI2_DDC_AUX_SEL	C34	DDI2_DDC_AUX_SEL	DDI2_DDC_AUX_SEL

Note:
Dual Mode (HDMI and DisplayPort on the same pins) implementations may be realized. This is desirable for SoCs that natively implement this capability. For such SoCs, the primary Dual Mode implementation challenge is that the HDMI_CTRL_DAT and HDMI_CTRL_CK lines are DC coupled, but the DP_AUX+ /- pair must be AC coupled. A set of FET switches is usually used to sort this out. The FET gates can be controlled by the AUX_SEL pin function.

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4.4.4.1 DisplayPort (DP) Mode

Name	Pin #	Description	I/O	PU / PD	Comment
DP2_LANE0+ DP2_LANE0- DP2_LANE1+ DP2_LANE1- DP2_LANE2+ DP2_LANE2- DP2_LANE3+ DP2_LANE3-	D39 D40 D42 D43 D46 D47 D49 D50	DP Port 2, differential pair data lines	O PCIe		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
DP2_HPD	D44	DP Port 2, detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	The module must tolerate a high level in stand-by mode. The carrier board shall include a blocking FET on DP1_HPD to prevent back-drive current from damaging the module.
DP2_AUX+	C32	DP Port 2, Bidirectional Channel used for Link Management and Device Control	I/O PCIe	PD 100K	AC coupled on Module
DP2_AUX-	C33	DP Port 2, Bidirectional Channel used for Link Management and Device Control	I/O PCIe	PU 100K	AC coupled on Module
DDI2_DDC_AUX_SEL	C34	Strapping Signal to select HDMI or DP output 1M pull-down on the module and floating on the carrier that enables DisplayPort mode	I 3.3V	PD 1M	DP mode enabled

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4.4.4.2 HDMI Mode

Name	Pin #	Description	I/O	PU / PD	Comment
TMDS2_DATA2+ TMDS2_DATA2- TMDS2_DATA1+ TMDS2_DATA1- TMDS2_DATA0+ TMDS2DATA0-	D39 D40 D42 D43 D46 D47	HDMI / DVI Port, Differential Pair Data Lines	O PCIe		AC coupled off module 100 nF DC blocking capacitors shall be placed on the carrier
TMDS2_CLK+ TMDS2_CLK-	D49 D50	HDMI Port, Differential Pair Clock Lines			
HDM2_HPD	D44	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	
HDMI2_CTRLCLK	C32	I2C_CLK Line for HDMI	I/O PCIe	PU 2.2K	AC couple on module
HDMI2_CTRLDATA	C33	I2C_DAT Line for HDMI	I/O PCIe	PU 2.2K	AC couple on module
DDI2_DDC_AUX_SEL	C34	Strapping Signal to select HDMI or DP output	I 3.3V	PD 1M	HDMI mode enabled

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4.4.5 DDI3 Port

Not supported

4.4.6 PCIe Graphics Port (PEG)

Not supported

4.4.7 Module Type Definition

Name	Pin #	Description	I/O	PU / PD	Comment
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The TYPE pins indicate to the carrier board the Pin-out Type that is implemented on the module. The pins are tied to either ground (GND) or are left as no-connects (NC) on the module. For Pin-out Type 1 and Type 10, which lack a CD connector, these pins are not present (X) **TYPE2# TYPE1# TYPE0#** X X X Pinout Type 1 X X X Pinout Type 10 NC NC NC Pinout Type 2 NC NC GND Pinout Type 3 NC GND NC Pinout Type 4 NC GND GND Pinout Type 5 GND NC NC Pinout Type 6 GND NC GND Pinout Type 7 The carrier board should implement combinatorial logic to monitor the module TYPE pins and keep power off (e.g., deactivates the ATX_ON signal for an ATX			Type 6

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		power supply) if an incompatible module pin-out type is detected. The carrier board logic may also implement a fault indicator, such as an LED.			
TYPE10#	A97	In case of a type 10 module this pin signal is tied to GND through a 47K resistor on the module.			No PD

4.4.8 Power and Ground

Name	Pin #	Description	I/O	PU / PD	Comment
VCC_12V	C104, C105, C106, C107, C108, C109, D104, D105, D106, D107, D108, D109	Primary power input supports a wide input range of 5~ 20V. All available VCC_12V pins on the connector(s) shall be used.	P		8.5-20 V
GND	C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70, C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path.	P		

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5. Additional Features

This chapter describes connectors, LEDs, switches, and additional items located on the module and not necessarily included in the PICMG standard specification. The locations of these items are as illustrated below:

5.1 Module Feature Locations

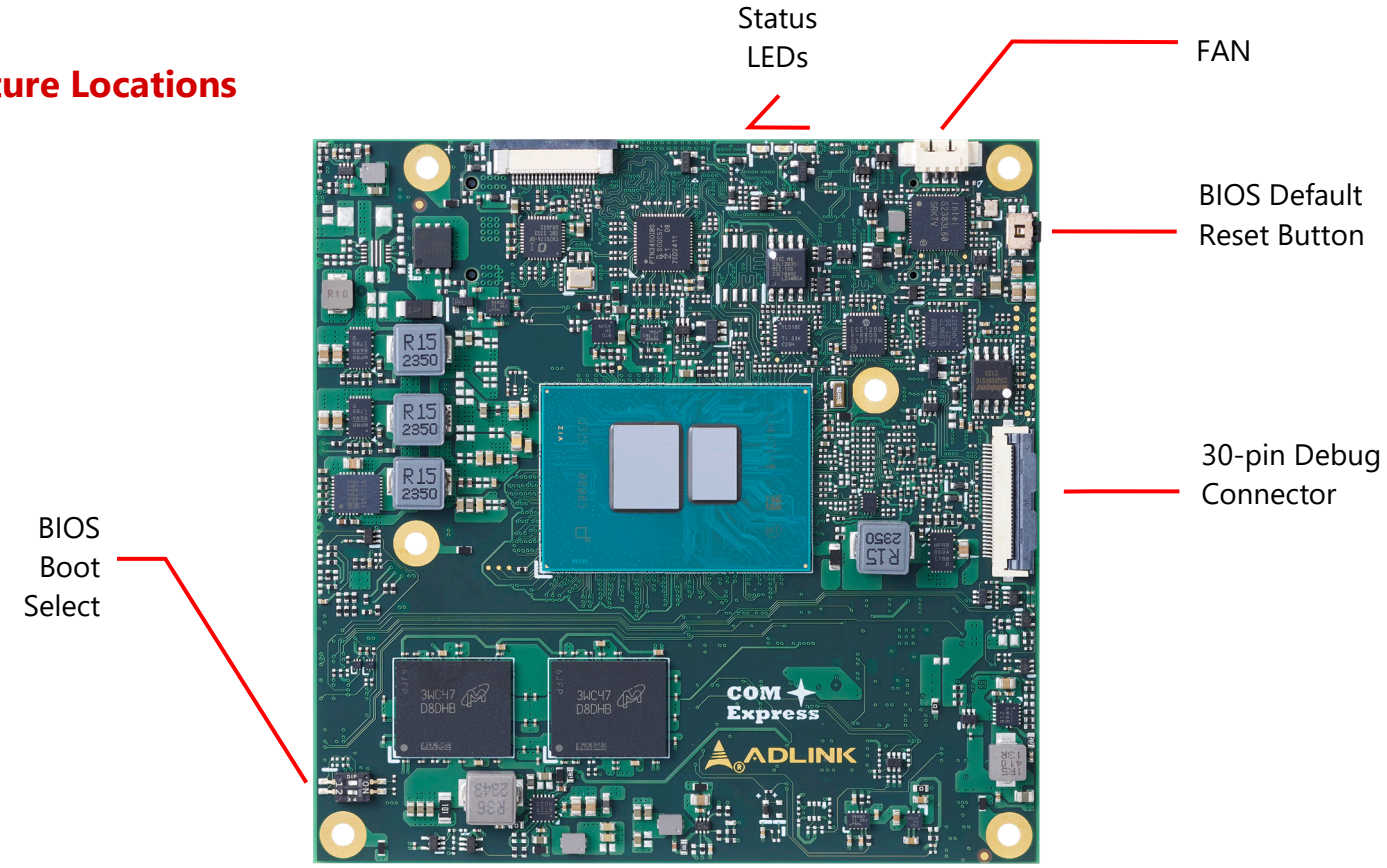


Figure 3 – Module feature locations (top side)

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5.2 Debug Connector

This connector is particularly useful during the carrier design and bring up phase. It provides access to the following critical parts of the module:

- Test points measurement of internal power rails
- SPI BIOS programming interface
- I2C bus for BIOS Post Code readout
- Embedded Controller programming interface

Picture below is for illustration purposes only:

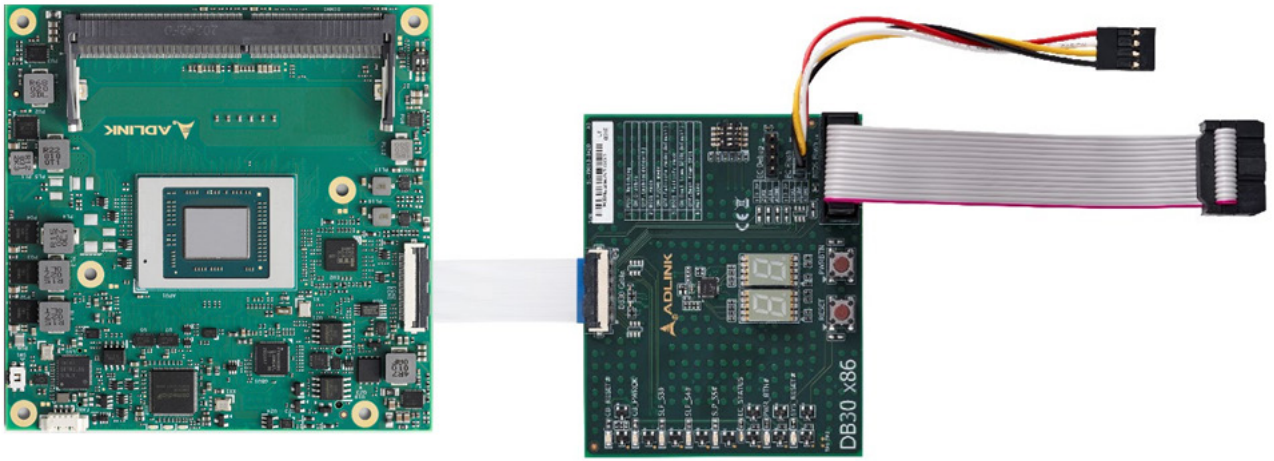
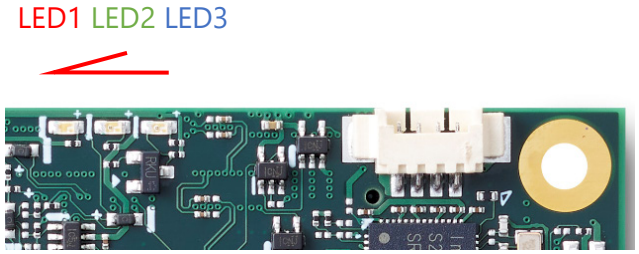


Figure 4 – cExpress-ASL and debug module

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5.3 Status LEDs

Status LEDs are mounted on the module to facilitate easier maintenance.



Name	Color	Connection	Function
LED1	Blue	EC output	Power Sequence Status Code (EC) Power Changes, RESET (see Exception Codes below)
LED2	Green	Power Source 3Vcc	S0 LED ON S3/S4/S5 LED OFF ECO mode LED OFF
LED3	Red	EC output and same signal as WDT (B27) on BtB connector	Module power up WD LED = LED OFF Watchdog counting WD LED = Keep Last State Watchdog timed out WD LED = LED ON Watchdog RESET WD LED = LED ON Rebooted after WD RESET WD LED = LED ON Rebooted after PWRBTN WD LED = LED OFF Rebooted after RESET BTN WD LED = LED OFF Note: only a RESET not initiated by the BMC can clear the WD LED (user action)

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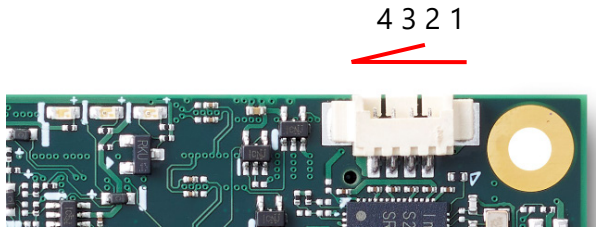
5.4 Exception Codes

Exception Code	Error Message
0	NOERROR
3	NO_SLP_S5
4	NO_SLP_S4
5	NO_SLP_S3
6	BIOS_FAIL
7	RESET_FAIL
9	NO_CB_PWROK
10	CRITICAL_TEMP
11	POWER_FAIL
12	VOLTAGE_FAIL
13	RSMRST_FAIL
14	NO_VDDQ_PG
16	NO_VCORE_PG
17	NO_SYS_GD
19	NO_V3P3A
21	NO_PWRSRC_GD

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5.5 Fan Connector

Connector type: JVE 24W1125A-04M00



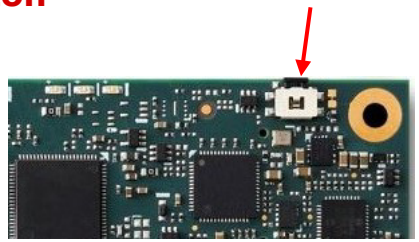
Name	Description
1	FAN_PWMOUT
2	FAN_TACHIN
3	GND
4	12V

The on-board FAN connector is a mini 4-pin type. The reference heatsink with an active FAN uses a standard 4-pin connector.

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5.6 BIOS Default Reset Button



To perform a hardware reset of the BIOS default settings, perform the following steps:

1. Shut down the system.
2. Press and hold the BIOS Setup Defaults Reset Button, then boot up the system. You can release the button when the BIOS prompt screen appears.
3. The BIOS prompt screen will display a confirmation that the BIOS defaults have been reset and will request that you reboot the system.



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5.7 BIOS Boot Select

The module has two BIOS chips (BOM option), and BIOS operation can be configured to "PICMG" and dual-BIOS "Failsafe" modes using the BIOS Select and Mode Configuration Switch, Pin 2.

Setting the module to PICMG mode configures the BIOS chips on the module as SPI0 and SPI1. In PICMG mode, a BIOS chip cannot be placed in the SPI0 slot on the carrier.

In dual-BIOS Failsafe mode, both BIOS chips on the module are configured as SPI1. Only one of the two is connected to the SPI bus at any given time. In case of failure of the primary SPI1 BIOS, the system will reboot and switch to the secondary SPI1 BIOS on the module. In Failsafe mode, the SPI0 BIOS socket on the carrier can be populated.

In either mode, BIOS Select and Mode Configuration Switch Pin 1 is used to select whether to boot from SPI0 or SPI1.

Mode	Pin 1	Pin 2
Boot from SPI0 (default)	On	-
Boot from SPI1	Off	-
Set BIOS to PICMG mode (default)	-	On
Set BIOS to Failsafe BIOS mode	-	Off

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6. System Resources

6.1 System Memory Map

Memory Range	Target	Dependency/Comments
000A0000 – 000B FFFF	PCIe port	PCIe root port
000E 0000 - 000F 3FFF	PCIe port	PCIe root port
000E 4000 - 000F 7FFF	PCIe port	PCIe root port
000E 8000 - 000F BFFF	PCIe port	PCIe root port
000E C000 – 000E FFFF	PCIe port	PCIe root port
000F 0000 - 000F FFFF	PCIe port	PCIe root port
0080400000 – 00BFFFFFFF	PCIe port	PCIe root port
00C0000000- 00CFFFFFFF	Motherboard resources	
00FD690000 – 00FD69FFFF	Serial I/O GPIO Host Controller	Serial I/O GPIO Host Controller – INTC1057
00FD6A0000 – 00FD6AFFFF	Serial I/O GPIO Host Controller	Serial I/O GPIO Host Controller – INTC1057

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00FD6D0000 – 00FD6DFFFF	Serial I/O GPIO Host Controller	Serial I/O GPIO Host Controller – INTC1057
00FD6E0000 – 00FD6EFFFF	Serial I/O GPIO Host Controller	Serial I/O GPIO Host Controller – INTC1057
00FE010000- 00FE010FFF	SPI Controller	SPI Controller – 54A4
00FED00000- 00FED003FF	High precision event timer	
00FED20000-00FED7FFFF	Motherboard resources	
00FED45000-00FED8FFFF	Motherboard resources	
00FED90000-00FED93FFF	Motherboard resources	
00FEDA0000-00FEDA0FFF	Motherboard resources	
00FEDA1000-00FEDA1FFF	Motherboard resources	
00FEDC0000-00FEDC7FFF	Motherboard resources	
00FEE00000-00FEEFFFFF	Motherboard resources	

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004000000000 – 00 400FFFFFFF	Intel UHD Graphics	
006000000000 – 00600FFFFFFF	Intel UHD Graphics	
006001100000-00600110FFFF	XHCI Controller	Intel USB3.0 XHCI Controller
006001118000-0060011180FF	SMBus	SMBus-54A3
00600111B000-00600111BFFF	Intel SD Host Contoller	
007FFFEF3000- 007FFFEF3FFF	UART#0	Intel Serial I/O UART Host Controller – 54A8
007FFFEF4000- 007FFFEF4FFF	UART#1	Intel Serial I/O UART Host Controller – 54C7
007FFFEF5000- 007FFFEF5FFF	I2C#0	Intel Serial I/O I2C Host Controller – 54C6
007FFFEF6000- 007FFFEF6FFF	I2C#1	Intel Serial I/O I2C Host Controller-54C5
007FFFEF7000- 007FFFEF7FFF	Intel ME	Intel ME Interface #1
007FFFEF8000- 007FFFEF8FFF	I2C#2	Intel Serial I/O I2C Host Controller-54E9

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007FFFEF9000- 007FFFEF9FFF	I2C#3	Intel Serial I/O I2C Host Controller-54E8
007FFFEFA000- 007FFFEFAFFF	UART#2	Intel Serial I/O UART Host Controller – 54A9
007FFFEFB000- 007FFFEFBFFF	GNA	Intel GNA Scoring Accelerator module
007FFFEFC000- 007FFFEFCFFF	HDA	High Definition Audio Controller
007FFFF00000- 007FFFFFFFFF	HDA	High Definition Audio Controller
128 KB anywhere in 4 GBrange	LAN Controller (CSRregisters)	Enable via standard PCI mechanism (Device 31:Function 6)
4 KB anywhere in 4 GBrange	LAN Controller (LAN space onFlash)	Enable via standard PCI mechanism (Device 31:Function 6)
64 KB anywhere in 64-bitaddress range	USB Host Controller	Enable via standard PCI mechanism (Device 20, Function 0)
2 MB anywhere in 4 GBrange	USB Device Controller	Enable via standard PCI mechanism (Device 20, Function 1)
24 KB anywhere in 4 GBrange	USB Device Controller	Enable via standard PCI mechanism (Device 20, Function 1)
16 KB anywhere in 64-bitaddressing space	Intel® HD Audio Subsystem	Enable via standard PCI mechanism (Device 31, Function 3)
4 KB anywhere in 64-bitaddressing space	Intel® HD Audio Subsystem	Enable via standard PCI mechanism (Device 31, Function 3)
64 KB anywhere in 64-bitaddressing space	Intel® HD Audio Subsystem	Enable via standard PCI mechanism (Device 31, Function 3)
32 Bytes anywhere in 64-bit address range	SMBus	Enable via standard PCI mechanism (Device 31: Function 4)
2 KB anywhere above 64KB to 4 GB range	SATA Host Controller	AHCI memory-mapped registers. Enable via standard PCImechanism (Device 23: Function 0)

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Memory Base/Limit anywhere in 4 GB range	PCI Express* Root Ports 1-12	Enable via standard PCI mechanism
Prefetchable Memory Base/Limit anywhere in64-bit address range	PCI Express* Root Ports 1-12	Enable via standard PCI mechanism
16 Bytes anywhere in 64-bit address range	Intel® CSMEI #1, #2, #3, #4	Enable via standard PCI mechanism
4 KB anywhere in 4 GBrange	Intel® AMT Keyboard and Text	Enable via standard PCI mechanism (Device 22: Function 3)
16 MB anywhere in 64-bitaddress range	P2SB	Enable via standard PCI mechanism
Eight 4 KB slots anywherein 64-bit address range	UART, GPI and I2C controllers	Enable via standard PCI mechanism
1 MB (BAR0) or 4 KB (BAR1) in 4GB range	Integrated Sensor Hub	Enable via standard PCI mechanism (Device 19: Function 0)
8 KB slot anywhere in 4GB range	Integrated Wi-Fi*	Enable via standard PCI mechanism
8 KB slot and 4 KB slot anywhere in 4 GB range	PMC	Enable via standard PCI mechanism
8 KB slot and 4 KB slot anywhere in 4 GB range	Shared SRAM	Enable via standard PCI mechanism

6.2 I/O Map

Variable I/O Decode Ranges

Hex Range	Device
Anywhere in 64K I/O Space	ACPI
Anywhere in 64K I/O Space	IDE Bus Master
Anywhere in 64K I/O Space	SMBus
Anywhere in 64K I/O Space	TCO
3 Ranges in 64K I/O Space	Parallel Port
8 Ranges in 64K I/O Space	Serial Port 1

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Hex Range	Device
8 Ranges in 64K I/O Space	Serial Port 2
8 Ranges in 64K I/O Space	Serial Port 3
Anywhere in 64K I/O Space	I/O Trapping Ranges
Anywhere in 64K I/O Space	Serial ATA Index/Data Pair
Anywhere in 64K I/O Space	PCI Express* Root Ports
Anywhere in 64K I/O Space	Keyboard and Text(KT)

Fixed I/O Decode Ranges

Hex Range	Device
020h – 02Dh & 030h – 03Dh	Programmable interrupt controller
02Eh – 02Fh	Motherboard resource
040h – 043h & 050h – 053h	System Timer
04Eh – 04Fh	Motherboard resource
062h, 066h	Microsoft ACPI-Compliant Embedded Controller
061h, 063h, 065h, 067h, 070h, 080h, 092h	Motherboard resource
0A0h – 0B1h & 0B4h – 0BDh	Interrupt Controller
0B2h and 0B3h	Motherboard resource
0E0h – 0EFh	Available
0F0h	Co-processor error register
200h - 201h	SEMA Embedded Controller
2F8h – 2FFh	Serial Port 2
3F8h – 3FFh	Serial Port 1
378h – 37Fh	Available

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Hex Range	Device
380h – 3AFh	Available
4D0h-4D1h	Interrupt Controller
680h – 69Fh & 0A00h – 0A6Fh & 164Eh - 164Fh & 1854h-1857h & 2000h-20FEh	Motherboard resource
3000h-303Fh	Intel UHD Graphics
EFA0h- EFBFh	SMBus – 54A3
020h – 02Dh & 030h – 03Dh	Programmable interrupt controller
02Eh – 02Fh	Motherboard resource

6.3 Interrupt Request (IRQ) Lines

APIC Mode

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
0	System timer	N/A	No
3	Serial Port 2 (COM2)	IRQ3 via SERIRQ/PIRQ	No
4	Serial Port 1 (COM1)	IRQ4 via SERIRQ/PIRQ	No
14	Intel Serial I/O GPIO Host Controller	N/A	No
16	Intel SD Host Controller	PCI Usage	No
16	Intel Serial I/O UART Host Controller-54A8	PCI Usage	No
17	Intel Serial I/O UART Host Controller-54A9	PCI Usage	No
19	High-Definition Audio Controller	PCI Usage	No
27	Intel Serial I/O I2C Host Controller-54E8	PCI Usage	No

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IRQ#	Typical Interrupt Resource	Connected to Pin	Available
31	Intel Serial I/O I2C Host Controller-54C5	PCI Usage	No
32	Intel Serial I/O I2C Host Controller-54C6	PCI Usage	No
36	Intel Serial I/O SPI Host Controller-54AA	PCI Usage	No
40	Intel Serial I/O I2C Host Controller-54E9	PCI Usage	No
42	Intel Serial I/O UART Host Controller-54C7	PCI Usage	No
43-511	Microsoft ACPI-Compliant System	N/A	Yes

Note: These IRQs can be used for PCI devices when onboard device is disabled.

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6.4 PCI Configuration Space Map

Bus Number	Device Number	Function Number	Routing	Description
00h	00h	00h	N/A	Intel Corporation Host Bridge
00h	02h	00h	Internal	Intel VGA Controller
00h	08h	00h	Internal	Intel system device
00h	14h	00h	Internal	USB xHCI Controller
00h	14h	02h	Internal	RAM Controller
00h	15h	00h	Internal	I2C Controller #0
00h	15h	01h	Internal	I2C Controller #1
00h	16h	00h	Internal	Intel® CSME Interface #1
00h	19h	00h	Internal	I2C Controller #2
00h	19h	01h	Internal	I2C Controller #3
00h	19h	02h	Internal	UART #0
00h	1Ah	00h	Internal	SD Host Controller
00h	1Ch	00h	Internal	Intel PCI Express Root port 4
00h	1Eh	00h	Internal	UART #1
00h	1Eh	01h	Internal	UART #2
00h	1Fh	00h	Internal	Intel ISA bridge
00h	1Fh	03h	Internal	HD Audio
00h	1Fh	04h	Internal	SMBus Controller
00h	1Fh	05h	Internal	SPI Controller
01h	00h	00h	Internal	Intel Ethernet controller I226-V

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6.5 PCI Interrupt Routing Map

INT Line	Audio Controller	xHCI Controller	CSME Controller	SMBus Controller
Int0	INTD: 16	INTA: 16	INTA: 16	INTA: 16
Int1		INTB: 17	INTB: 17	
Int2		INTC: 18	INTC: 18	
Int3		INTD: 19	INTD: 19	

INT Line	PCIe Port 3	PCIe Port 4	PCIe Port 7	PCIe Port 9	PCIe Port 10
Int0	INTA: 16	INTB: 17	INTC: 18	INTD: 19	INTA: 16
Int1	INTB: 17	INTC: 18	INTD: 19	INTA: 16	INTB: 17
Int2	INTC: 18	INTD: 19	INTA: 16	INTB: 17	INTC: 18
Int3	INTD: 19	INTA: 16	INTB: 17	INTC: 18	INTD: 19

6.6 SMBus Address Table

Device	Address
PTN3460	0C0h

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7. BIOS Setup

7.1 Menu Structure

This section presents the six primary menus of the BIOS Setup Utility. Use the following table as a quick reference for the contents of the BIOS Setup Utility. Subsections in this section describe the submenus and setting options for each menu item. The default setting options are presented in **bold**, and the function of each setting is described in the right-hand column of the respective table.

Main	Advanced	Chipset	Security	Boot	Save & Exit
BIOS Information System Information Board Information ► System Date System Time	CPU Configuration ► Power & Performance ► Inter(R) Time Coordinated Computing ► Power Management ► System Management ► Thermal Management ► Watchdog Timer ► Super I/O Configuration ► Miscellaneous ► USB Configuration ► NVMe Configuration ► AMI Graphics Output Protocol Policy ► Serial Port Console Redirection ► Network Stack Configuration ► Trusted Computing ►	System Agent (SA) Configuration ► PCH-I/O Configuration ►	Password Description Secure Boot ►	Boot Configuration	Save Options Boot Override

Note: ► Indicates a submenu
Gray text indicates info only

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7.2 Main

The Main Menu provides read-only information about your system and also allows you to set the system date and time. Refer to the tables below the screenshot of this menu for details of the submenus and settings.

7.2.1 BIOS Information

Feature	Options	Description
BIOS Vendor	Info only	American Megatrends
BIOS Version	Info only	Displays core version
Build Date	Info only	Displays compliancy information
MRC Version	Info only	Displays compliancy information
GOP Version	Info only	ADLINK BIOS version.
ME FW Version	Info only	ADLINK BIOS version.

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7.2.2 System Information

Board Information	Info only	Description
Project Name	Info only	Displays Project Name
CPU Board Version	Info only	Displays CPU Signature
CPU Brand String	Info only	Displays CPU Brand Name
CPU Frequency	Info only	Displays CPU Frequency
Total Memory	Info only	Displays Installed Memory Size
Memory Frequency	Info only	Displays Memory Frequency
PCH SKU	Info only	Displays PCH Information
Board Information	Submenu	

7.2.3 Board Information

Board Information	Info only	Description
Serial Number	Read only	Displays SMC serial number
Manufacturing Date	Read only	Displays SMC manufacturing date
Last Repair Date	Read only	Displays SMC last repair date
MAC ID	Read only	Displays SMC MAC ID
MAC ID 2	Read only	Displays SMC MAC ID 2
UUID	Read only	Displays SMC UUID
Runtime Statistics	Info only	
Total Runtime	Read only	The returned value specifies the total time, in minutes, that the system has been running in S0 state.
Current Runtime	Read only	The returned value specifies the time, in seconds, that the system has been running in S0 state.

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Board Information	Info only	Description
		This counter is cleared when the system is removed from the external power supply.
Power Cycles	Read only	The returned value specifies the number of times the external power supply has been shut down.
Boot Cycles	Read only	The Bootcounter is increased after a HW- or SW-Reset or after a successful power-up.
Boot Reason	Read only	The boot reason is the event which causes the reboot of the system.

7.2.4 System Date and Time

Feature	Options	Description
System Date	Weekday, MM/DD/YYYY	Requires the alpha-numeric entry of the day of the week, day of the month, calendar month, and all 4 digits of the year, indicating the century and year (Fri XX/XX/20XX)
System Time	HH/MM/SS	Presented as a 24-hour clock setting in hours, minutes, and seconds
Access Level	Read only	It shows what access level is used to enter the BIOS setup menu.

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7.3 Advanced

This menu contains the settings for most of the user interfaces in the system.

7.3.1 CPU Configuration

Feature	Options	Description
Efficient-core Information	submenu	Displays the E-core Information
ID	Info only	Display CPU information
Brand String	Info only	Display CPU information
Stepping	Info only	Display CPU Stepping
Microcode Revision	Info only	Display Microcode Revision
VMX	Info only	Display Intel Virtualization Technology support or not.
SMX/TXT	Info only	Display Intel SMX Technology support or not.
Intel (VMX) Virtualization Technology	Disabled, **Enabled**	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.
Active Efficient-cores	**All**,1,0	Number of E-cores to enable in each processor package. Note: Number of Cores and E-cores are looked at together. When both are {0,0}, Pcode will enable all cores.

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7.3.2 Power & Performance Configuration

7.3.2.1 Power & Performance Configuration > CPU - Power Management Control

Feature	Options	Description
Boot Performance Mode	Max Battery, Max Non-Turbo Performance, **Turbo Performance**	Select the performance state that the BIOS will set starting from reset vector.
Intel(R) SpeedStep(tm)	Disabled, **Enabled**	Allows more than two frequency ranges to be supported.
Race To Halt (RTH)	Disabled, **Enabled**	Enable/Disable the Race To Halt feature. RTH will dynamically increase CPU frequency in order to enter pkg C-State faster to reduce overall power. (RTH is controlled through MSR 1FC bit 20)
Intel(R) Speed Shift Technology	Disabled, **Enabled**	Enable/Disable Intel(R) Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware-controlled P-states.
Per Core P State OS control P-State	Disabled, **Enabled**	Enable/Disable Per Core P state OS control mode. Disabling will set Bit 31 = 1 command 0x06. When set, the highest core request is used for all other core requests.
HWP Autonomous Per Core P-State	Disabled, **Enabled**	Disable Autonomous PCPS (Bit 30 = 1, command 0x11) Autonomous will request the same value for all cores all the time. Enable PCPS (default Bit 30 = 0, command 0x11)
HWP Autonomous EPP Grouping	Disabled, **Enabled**	Enable EPP grouping (default Bit 29 =0, command 0x11) Autonomous will request the same values for all cores with same EPP. Disable EPP grouping (Bit 29 =1 , command 0x11) autonomous will not necessarily request same values for all cores with same EPP.
EPB override over PECI	**Disabled**, Enabled	Enable/Disable EPB override over PECI. Enable by sending pcode command 0x2b , subcommand 0x3 to 1. This will allow OOB EPB PECI override control
HWP Lock	Disabled, **Enabled**	Enable/Disable HWP Lock support in Miscellaneous Power Management MSR.
HDC Control	Disabled, **Enabled**	This option allows HDC configuration.
Turbo Mode	Disabled, **Enabled**	Enable/Disable processor Turbo Mode (requires EMTTM to be enabled). AUTO means enabled.
View/Configure Turbo Options	Submenu	
Current Turbo Settings		

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Feature	Options	Description
Max Turbo Power Limit	Info only	
Min Turbo Power Limit	Info only	
Package TDP Limit	Info only	
Power Limit 1	Info only	
Power Limit 2	Info only	
Turbo Ratio Limit Options	Submenu	
Energy Efficient P-state	Disabled, **Enabled**	Enable/Disable the Energy Efficient P-state feature. When set to 0, will disable access to ENERGY_PERFORMANCE_BIAS MSR and CPUID Function 6 ECX[3] will read 0 indicating no support for Energy Efficient policy setting. When set to 1 will enable access to ENERGY_PERFORMANCE_BIAS MSR 1B0h and CPUID Fun
Package Power Limit MSR Lock	**Disabled**, Enabled	Enable/Disable locking of Package Power Limit settings. When enabled, PACKAGE_POWER_LIMIT MSR will be locked and a reset will be required to unlock the register.
Power Limit 1 Override	**Disabled**, Enabled	Enable/Disable Power Limit 1 override. If this option is disabled, BIOS will program the default values for Power Limit 1 and Power Limit 1 Time Window.
Power Limit 2 Override	Disabled, **Enabled**	Enable/Disable Power Limit 2 override. If this option is disabled, BIOS will program the default values for Power Limit 2.
Power Limit 2	0	Power Limit 2 value in milliwatts. BIOS will round to the nearest 1/8W when programming. If the value is 0, BIOS will program this value as 1.25* Processor Base Power (TDP). For 12.50W, enter 12500. The processor applies control policies to ensure that the package power does not exceed this limit.
Energy Efficient Turbo	Disabled, **Enabled**	Enable/Disable the Energy Efficient Turbo Feature. This feature will opportunistically lower the turbo frequency to increase efficiency. Recommended only to disable in overclocking situations where turbo frequency must remain constant. Otherwise, leave enabled.
Config TDP Configurations	Submenu	

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Feature	Options	Description
Config TDP Configurations		
Enable Configurable TDP	Applies to non-cTDP, **Applies to cTDP**	Applies TDP initialization settings based on non-cTDP or cTDP. Default is 1: Applies to cTDP; if 0 then applies non-cTDP and BIOS will bypass cTDP initialzation flow
Configurable TDP Boot Mode	**Nominal**, Down2, Down1, Deactivate	Configurable TDP Mode as Nominal/Up/Down/Deactivate TDP selection. Deactivate option will set MSR to Nominal and MMIO to Zero.
Configurable TDP Lock	Enabled, **Disabled**	Configurable TDP Mode Lock sets the Lock bits on TURBO_ACTIVATION_RATIO and CONFIG_TDP_CONTROL. Note: When CTDP Lock is enabled Custom ConfigTDP Count will be forced to 1 and Custom ConfigTDP Boot Index will be forced to 0.
CTDP BIOS control	Enabled, **Disabled**	
ConfigTDP Levels	2	
ConfigTDP Turbo Activation Ratio	17 (Unlocked)	
Power Limit 1	15.0W (MSR:15.0)	
Power Limit 2	15.0W (MSR:15.0)	
Custom Settings Nominal		
ConfigTDP Nominal	Ratio:18 TAR:1 PL1:13.0W	
Power Limit 1	0	Power Limit 1 in milliwatts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Overclocking SKU: Value must be between Max and Min Power Limits (specified by PACKAGE_POWER_SKU_MSR). Other SKUs: This value must be between Min Power Limit and TDP
Power Limit 2	0	Power Limit 2 value in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. The processor applies control policies to ensure that the package power does not exceed this limit.
Power Limit 1 Time Window*	**0**, 1, 2, 3, 4, 5, 6, 7, 8, 10, 12, 14, 16, 20, 24, 28, 32, 40, 48, 56, 64,	Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0 = default value (28 sec for Mobile and 8 sec for Desktop). Defines time window which TDP value should be maintained.

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Feature	Options	Description
	80, 96, 112, 128	
ConfigTDP Turbo Activation Ratio	[Max-Value, Min-Value, Step-Value] = [0xFF, 0x00, 0x01]	Custom value for Turbo Activation Ratio. Needs to be configured with valid values from LFM to Max Turbo. 0 means don't use custom value.
Custom Settings Nominal		
ConfigTDP Nominal	Ratio:18 TAR:17 PL1:15.0W	
Power Limit 1	0	Power Limit 1 in milliwatts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Overclocking SKU: Value must be between Max and Min Power Limits (specified by PACKAGE_POWER_SKU_MSR). Other SKUs: This value must be between Min Power Limit and TDP
Power Limit 2	15000	Power Limit 2 value in milliwatts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. The processor applies control policies to ensure that the package power does not exceed this limit.
Power Limit 1 Time Window*	**0**, 1, 2, 3, 4, 5, 6, 7, 8, 10, 12, 14, 16, 20, 24, 28, 32, 40, 48, 56, 64, 80, 96, 112, 128	Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0 = default value (28 sec for Mobile and 8 sec for Desktop). Defines time window which TDP value should be maintained.
ConfigTDP Turbo Activation Ratio	0	Custom value for Turbo Activation Ratio. Needs to be configured with valid values from LFM to Max Turbo. 0 means don't use custom value.
Custom Settings Level1		
ConfigTDP Level1	Ratio:28 TAR:27 PL1:1.0W	
Power Limit 1	0	Power Limit 1 in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Overclocking SKU: Value must be between Max and Min Power Limits (specified by PACKAGE_POWER_SKU_MSR). Other SKUs: This value must be between Min Power Limit and TDP
Power Limit 2	0	Power Limit 2 value in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. The processor applies control policies to ensure that the package power does not exceed this limit.

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Feature	Options	Description
Power Limit 1 Time Window*	**0**, 1, 2, 3, 4, 5, 6, 7, 8, 10, 12, 14, 16, 20, 24, 28, 32, 40, 48, 56, 64, 80, 96, 112, 128	Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0 = default value (28 sec for Mobile and 8 sec for Desktop). Defines time window which TDP value should be maintained.
ConfigTDP Turbo Activation Ratio	0	Custom value for Turbo Activation Ratio. Needs to be configured with valid values from LFM to Max Turbo. 0 means don't use custom value.
CPU VR Settings	Submenu	
CPU VR Settings		
Current VccIn Aux Icc Max	108	
PSYS Slope	0	PSYS Slope defined in 1/100 increments. Range is 0-200. For a 1.25 slope, enter 125. 0 = AUTO. Uses BIOS VR mailbox command 0x9."
PSYS Offset	0	PSYS Offset defined in 1/1000 increments. Range is 0-63999. For an offset of 25.348, enter 25348. PSYS Uses BIOS VR mailbox command 0x4.
PSYS Prefix	**+**, -	Sets the offset value as positive or negative.
PSYS PMax Power	0	PSYS PMax power, defined in 1/8 Watt increments. Range 0-8192. For a PMax of 125W, enter 1000. 0 = AUTO. Uses BIOS VR mailbox command 0xB.
Min Voltage Override	**Disabled**, Enabled	Min Voltage Override. Enable to override minimum voltage for runtime and for C8.
VccIn Aux Icc Max	0	Sets the Max Icc VccIn Aux value defined in 1/4A increments. Range is 0-512. For an IccMax 32A, enter 128(32*4).
VccIn Aux IMON Slope	111	VccIN Aux IMON Slope defined in 1/100 increments. Range is 0-200. For a 1.25 slope, enter 125. 0 = AUTO. Uses BIOS VR mailbox command 0x18.
VccIn Aux IMON Offset	0	VccIN Aux IMON Offset defined in 1/1000 increments. Range is 0-63999. For an offset of 25.348, enter 25348. IMON Uses BIOS VR mailbox command 0x18.
VccIn Aux IMON Prefix	**+.-**	Sets the offset value as positive or negative.
Vsys/Psys Critical	**Disabled**,Psys	Vsys/Psys Critical enable or disable

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Feature	Options	Description
	Critical,Vsys Critical	
Assertion Deglitch Mantissa	**1**	Assertion Deglitch Mantissa 0x4F[7-3]. Assertion Deglitch = 2µs * Mantissa * 2^(Exponent)
Assertion Deglitch Exponent	**0**	Assertion Deglitch Exponent 0x4F[3-0]. Assertion Deglitch = 2µs * Mantissa * 2^(Exponent)
De assertion Deglitch Mantissa	**13**	De Assertion Deglitch Mantissa 0x49[7-3]. Assertion Deglitch = 2µs * Mantissa * 2^(Exponent)
De assertion Deglitch Exponent	**2**	De Assertion Deglitch Exponent 0x49[3-0]. Assertion Deglitch = 2µs * Mantissa * 2^(Exponent)
VR Power Delivery Design	**Auto**	Specifies the ADL Desktop board design used for the VR settings override values. By default, BIOS will override the default Desktop VR settings based on the board design. A value of AUTO(0) will use the board ID to determine the board design. Any other value will override the board id logic to provide a custom VR Power Delivery Design value. This is intended primarily for validation.
Acoustic Noise Settings	Submenu	
Acoustic Noise Mitigation	**Disabled**, Enabled	Enabling this option will help mitigate acoustic noise on certain SKUs when the CPU is in deeper C state
Pre Wake Time	0	Set the maximum Pre Wake randomization time in micro ticks. Range is 0-255. This is for acoustic noise mitigation through Dynamic Periodicity Alteration (DPA) tuning.
Ramp Up Time	0	Set the maximum Ramp Up randomization time in micro ticks. Range is 0-255. This is for acoustic noise mitigation through Dynamic Periodicity Alteration (DPA) tuning.
Ramp Down Time	0	Set the maximum Ramp Down randomization time in micro ticks. Range is 0-255. This is for acoustic noise mitigation through Dynamic Periodicity Alteration (DPA) tuning.
IA VR Domain		
Disable Fast PKG C State Ramp for IA Domain	**FALSE**, TRUE	This option needs to be configured to reduce acoustic noise during deeper C states. False: Don't disable Fast ramp during deeper C states; True: Disable Fast ramp during the deeper C state.
Slow Slew Rate for IA Domain	**Fast/2,** Fast/4, Fast/8, Fast/16	Set VR IA Slow Slew Rate for Deep Package C State ramp time; Slow slew rate equals to Fast divided by number, the number is 2, 4, 8, 16 to slow down the slew rate to help minimize acoustic noise
GT VR Domain		

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Feature	Options	Description
Disable Fast PKG C State Ramp for GT Domain	**FALSE**, TRUE	This option needs to be configured to reduce acoustic noise during deeper C states. False: Don't disable Fast ramp during deeper C states; True: Disable Fast ramp during the deeper C state
Slow Slew Rate for GT Domain	**Fast/2,** Fast/4, Fast/8	Set VR GT Slow Slew Rate for Deep Package C State ramp time; Slow slew rate equals to Fast divided by number, the number is 2, 4, 8 to slow down the slew rate to help minimize acoustic noise; divide by 16 is disabled
Core/IA VR Settings	Submenu	
Core/IA VR Domain		
VR Config Enable	Disabled, **Enabled**	VR Config Enable
Current AC Loadline	470	
Current DC Loadline	470	
Current Psi1 Threshold	16	
Current Psi2 Threshold	8	
Current Psi3 Threshold	4	
Current Imon Slope	0	
Current Imon Offset	1	
Current VR Current Limit	212	
Current Tdc Current Limit	272	
Current Voltage Limit	1600	
AC Loadline	0	AC Loadline defined in 1/100 mOhms. A value of 100 = 1.00 mOhm, and 1255 = 12.55 mOhm. Range is 0-6249 (0-62.49 mOhms). 0 = AUTO/HW default. Uses BIOS mailbox command 0x2.

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Feature	Options	Description
DC Loadline	0	DC Loadline defined in 1/100 mOhms. A value of 100 = 1.00 mOhm, and 1255 = 12.55 mOhm. Range is 0-6249 (0-62.49 mOhms). 0 = AUTO/HW default. Uses BIOS mailbox command 0x2.
PS Current Threshold1	16	PS Current Threshold1, defined in 1/4 A increments. A value of 400 = 100A. Range 0-512, which translates to 0-128A. 0 = AUTO. Uses BIOS VR mailbox command 0x3.
PS Current Threshold2	8	PS Current Threshold2, defined in 1/4 A increments. A value of 400 = 100A. Range 0-512, which translates to 0-128A. 0 = AUTO. Uses BIOS VR mailbox command 0x3.
PS Current Threshold3	4	PS Current Threshold3, defined in 1/4 A increments. A value of 400 = 100A. Range 0-512, which translates to 0-128A. 0 = AUTO. Uses BIOS VR mailbox command 0x3.
PS3 Enable	Disabled, **Enabled**	PS3 Enable/Disable. 0 - Disabled, 1 - Enabled.Uses BIOS VR mailbox command 0x3.
PS4 Enable	Disabled, **Enabled**	PS4 Enable/Disable. 0 - Disabled, 1 - Enabled.Uses BIOS VR mailbox command 0x3.
IMON Slope	0	IMON Slope defined in 1/100 increments. Range is 0-200. For a 1.25 slope, enter 125. 0 = AUTO. Uses BIOS VR mailbox command 0x4.
IMON Offset	0	IMON Offset defined in 1/1000 increments. Range is 0-63999. For an offset of 25.348, enter 25348. IMON Uses BIOS VR mailbox command 0x4.
IMON Prefix	**+**,-	Sets the offset value as positive or negative.
VR Current Limit	0	Voltage Regulator Current Limit (IccMax). This value represents the Maximum instantaneous current allowed at any given time. The value is represented in 1/4 A increments. A value of 400 = 100A. 0 means AUTO. Uses BIOS VR mailbox command 0x6.
VR Voltage Limit	0	Voltage Limit (VMAX). This value represents the Maximum instantaneous voltage allowed at any given time. Range is 0 - 7999mV. Uses BIOS VR mailbox command 0x8.
TDC Enable	Disabled, **Enabled**	TDC Enable. 0- Disable, 1 - Enable
TDC Current Limit	0	TDC Current Limit, defined in 1/8A increments. Range 0-32767. For a TDC Current Limit of 125A, enter 1000. 0 = 0 Amps. Uses BIOS VR mailbox command 0x1A.
TDC Time Window	1 sec	VR TDC Time Window, value in seconds. 1s is default. Range from 1s to 448s.
TDC Lock	**Disabled**, Enabled	TDC Lock

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Feature	Options	Description
IRMS	Disabled, **Enabled**	Enable/Disable IRMS – Current root mean square
GT VR Settings	Submenu	
RFI Settings	Submenu	
RFI Domain		
RFI Current Frequency	139.200MHz	
RFI Frequency	0	Set desired RFI frequency, in increments of 100KHz. (For a frequency of 100.6MHz, enter 1006.)
FIVR Spread Spectrum	Disabled, **Enabled**	Enable or Disable the Spread Spectrum
RFI Spread Spectrum	0.5%, 1%, **1.5%**, 2%, 3%, 4%, 5%, 6%	Set the Spread Spectrum
Platform PL1 Enable	**Disabled**, Enabled	Enable/Disable Platform Power Limit 1 programming. If this option is enabled, it activates the PL1 value to be used by the processor to limit the average power of given time window.
Platform PL2 Enable	**Disabled**, Enabled	Enable/Disable Platform Power Limit 2 programming. If this option is disabled, BIOS will program the default values for Platform Power Limit 2.
Power Limit 4 Override	**Disabled**, Enabled	Enable/Disable Power Limit 4 override. If this option is disabled, BIOS will leave the default values for Power Limit 4.
C states	**Disabled**, Enabled	Enable/Disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized.
Thermal Monitor	Disabled, **Enabled**	Enable/Disable Thermal Monitor
Interrupt Redirection Mode Selection	**Fixed Priority,**Round robin,Hash Vector,No Change	Interrupt Redirection Mode Select for Logical Interrupts
Timed MWAIT	**Disabled**, Enabled	Enable/Disable Timed MWAIT Support

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Feature	Options	Description
Custom P-state Table	Submenu	
Custom P-state Table		
Number of P-states	**0**	Sets the number of custom P-states. At lease 2 states must be present.
EC Turbo Control Mode	**Disabled**, Enabled	Enable/Disable EC Turbo Control mode
Energy Performance Gain	**Disabled**, Enabled	Enable/Disable Enerfy Performance Gain.
EPG DIMM Idd3N	**26**	
EPG DIMM Idd3P	**11**	
Power Limit 3 Settings	Submenu	
Power Limit 3 Override	**Disabled**, Enabled	Enable/DisablePower Limit 3 override. If this option is disabled, BIOS will leave the hardware default values for Power Limit 3 and Power Limit 3 Time Window.
CPU Lock Configuration	Submenu	Enable/DisablePower Limit 3 override. If this option is disabled, BIOS will leave the hardware default values for Power Limit 3 and Power Limit 3 Time Window.
CFG Lock	Disabled, **Enabled**	Configure MSR 0Xe2[15], CFG Lock bit
Overclocking Lock	Disabled, **Enabled**	Enable/Disable Overclocking Lock (BIT 20) in FLEX_RATIO(194) MSR

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7.3.2.2 Power & Performance Configuration > GT Power Management Control

Feature	Options	Description
RC6(Render Standby)*	Disabled, **Enabled**	Check to enable render standby support.
Maximum GT frequency	**Default Max Frequency**, 100Mhz, 150Mhz, 200Mhz, 250Mhz, 300Mhz, 350Mhz, 400Mhz, 450Mhz, 500Mhz, 550Mhz, 600Mhz, 650Mhz, 700Mhz, 750Mhz, 800Mhz, 850Mhz, 900Mhz, 950Mhz, 1000Mhz, 1050Mhz, 1100Mhz, 1150Mhz, 1200Mhz	Maximum GT frequency is limited by the user. Choose between 100MHz (RPN) and 1350MHz (RP0). Values beyond the range will be clipped to min/max supported by SKU
Disable Turbo GT frequency	Enabled, **Disabled**	Enabled: Disables Turbo GT frequency. Disabled: GT frequency is not limited

7.3.3 Intel® Time Coordinated Computing

Feature	Options	Description
#AC Split Lock*	Enabled, **Disabled**	Enable or disable Alignment Check Exception (#AC). When enabled, this will assert an #AC when any atomic operation has an operand that crosses two cache lines.
#GP Fault UC Lock	Enabled, **Disabled**	Enable or disable GP Fault Exception (GP#). When enabled, this will assert an GP# when encountering a Lock to un-cacheable memory before the bus is locked.
Intel(R) TCC Authentication*	**OEM Enrolled Key**	Intel(R) TCC Authentication determines the key to be used. OEM Enrolled Key is built in by OEM. Non-OEM Enrolled Key can be added by the user.
Intel(R) TCC Mode*	Enabled, **Disabled**	Enable or disable Intel(R) TCC Mode. When enabled, this will modify system settings to improve real-time performance. The full list of settings and their current state are displayed below when Intel(R) TCC mode is enabled.
Intel(R) TCC Mode Affected Settings		
I/O Fabric Low Latency*	**Disabled**, Enabled	Enable or disable I/O Fabric Low Latency. This will turn off some power management features in the PCH IO

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		fabrics. This option provides the most aggressive I/O Fabric performance settings. S3 state is NOT supported.
GT CLOS*	**Disabled**, Enabled	Enable or Disable Graphics Technology (GT) Class of Service. Enable will reduce Gfx LLC allocation to minimize impact of Gfx workload on LLC
C states*	**Disabled**, Enabled	Enable/Disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized.
Intel(R) Speed Shift Technology*	Disabled, **Enabled**	Enable/Disable Intel(R) Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware-controlled P-states.
Intel(R) SpeedStep(tm)*	Disabled, **Enabled**	Allows more than two frequency ranges to be supported.
ACPI D3Cold Support*	**Disabled**, Enabled	Enable/Disable ACPI D3Cold support to be executed on D3 entry and exit
Low Power S0 Idle Capability*	**Disabled**, Enabled	This variable determines whether to enable ACPI Lower Power S0 Idle Capability (Mutually exclusive with Smart connect). When enabled, it also disables the 8254 timer for SLP_S0 support.
SA GV*	Disabled, Fixed to 1st Point,Fixed to 2nd Point, Fixed to 3rd Point, Fixed to 4th Point, **Enabled**	System Agent Geyserville. Can disable, fix to a specific point, or enable frequency switching.
Page Close Idle Timeout*	**Enabled**, Disabled	Page Close Idle Timeout Control
Power Down Mode*	**Auto**, No Power Down, APD, PPD-DLLoff	CKE Power Down Mode Control
RC6(Render Standby) *	Disabled, **Enabled**	Check to enable render standby support.
DMI Link ASPM Control*	**Disabled**, L0s, L1, Auto	The control of Active State Power Management of the DMI Link.
Legacy I/O Low Latency*	Disabled, **Enabled**	Set to enable low latency of legacy I/O. Some systems require lower I/O latency irrespective of power consumption. This is a tradeoff between power usage and I/O latency.
CPU PCI Express Configuration	Submenu	
PCH PCI Express Configuration	Submenu	

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7.3.4 Graphic Configuration

Feature	Options	Description
NXP configuration	Info Only	
Data format and Color Depth	VESA 24 bpp JEIDA 24 bpp **JEIDA/vesa 18 bpp**	Data format and Color Depth select
LVDS Output Mode	Dual LVDS bus **Single LVDS bus**	Single/Dual mode select
DE Polarity	**Active High** Active Low	DE Polarity select
Vsync Polarity	**Active High** Active Low	Vsync Polaity select
Hsync Polarity	**Active High** Active Low	Hsync Polarity select
Spreading depth	**No Spreading** 0.5% 1.0% 1.5% 2.0% 2.5%	Clock frequency center spreading depth.
Integrated Display Configuration	Info only	
eDP/LVDS	**Disabled** Enabled	Enable/Disable eDP/LVDS
LFP Panel Type	**VBIOS Default** 640x480 800x600 1024x768 1280x1024	Select LFP panel used by Internal Graphics Device by selecting the appropriate setup item.

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	1400x1050 LVDS1 1400x1050 LVDS2 1600x1200 1366x768 1680x1050 1920x1200 1440x900 1600x900 1024x768 1280x800 1920x1080 2048x1536	
LVDS Backlight Mode	**EC Mode** GTT Mode	Select LVDS Backlight control function.
LVDS Backlight	Submenu	
LVDS Backlight Brightness	Value Range(0-255)	A change takes effect immediately. The value range starts at 0 and ends at 255.
DDI port 1	No Device Display Port HDMI **DisplayPort with HDMI/DVI Compatibility**	Choose between DisplayPort or HDMI for DDI port function
DDI port 2	No Device Display Port HDMI **DisplayPort with HDMI/DVI Compatibility**	Choose between DisplayPort or HDMI for DDI port function

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7.3.5 Power Management

Feature	Options	Description
Enable ACPI Auto Configuration	**Disabled**, Enabled	Enables or Disables BIOS ACPI Auto Configuration.
Enable Hibernation	Disabled, **Enabled**	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may not be effective with some operating systems.
ACPI Sleep State*	Suspend Disabled, **S3 (Suspend to RAM)**	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
LID Function	**Disabled**, Enabled	Enable/Disable LID Function
Sleep Function	Disabled, **Enabled**	Enable/Disable Sleep Button Function
ECO Mode*	**Disabled**, Enabled	Reduces the power consumption of the system, but after a shut down, you have to wait at least 5 seconds before you can restart the system.
Power-Up Mode*	**Turn On,** Remain Off, Last State	Turn On:
ATTENTION: The Power-Up Mode only has effect, if the module is in ATX-Mode.		
Power Consumption	Submenu	

7.3.5.1 Power Management > Power Consumption

Feature	Options	Description
Power Consumption	Info only	
Main Current	Read only	Displays input current.
Current Input Power	Read only	Displays input power.
RTC	Read only	Displays the sensed voltage based on hardware design.
5VSB	Read only	Displays the sensed voltage based on hardware design.
VIN	Read only	Displays the sensed voltage based on hardware design

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Feature	Options	Description
3.3V	Read only	Displays the sensed voltage based on hardware design
VMEM	Read only	Displays the sensed voltage based on hardware design
3.3VSB	Read only	Displays the sensed voltage based on hardware design
VCORE	Read only	Displays the sensed voltage based on hardware design

7.3.6 System Management

Feature	Options	Description
System Management	Info Only	
Version	Info Only	Displays SEMA Module Version.
SEMA Firmware	Info Only	Displays SEMA Firmware Version.
SEMA Flags	Submenu	Displays SEMA Flags
SEMA Features	Info	Displays SEMA Supported Features

7.3.6.1 System Management > SEMA Flags

Feature	Options	Description
SEMA Flags	Info Only	
BIOS Select	Info Only	
ATX/AT-Mode	Info Only	

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7.3.7 Thermal Management

Feature	Options	Description
Thermal Management	Info Only	
Critical Trip Point	**Disabled** 80 C 90 C 95 C	The value is the temperature threshold of the Critical Trip Point.
Passive Cooling Trip Point	**Disabled** 70 C 80 C 90 C 100 C	The value is the temperature threshold of the Passive Cooling Trip Point.
Active Cooling Trip Point	40C, 50C, 60C, 70C, **Refer to BMC**	This value is the temperature threshold of the active cooling trip point.
Watchdog ACPI Event Shutdown	**Disabled** Enabled	Watchdog ACPI Event Shutdown Enabled/Disabled
Temperature and Fan Speed	Submenu	

7.3.7.1 Thermal Management-> Temperature and Fan Speed

Feature	Options	Description
Temperatures and Fan Speed	Info Only	
CPU Temperature	Info Only	
Current	Info Only	Displays Current CPU Temperature
Startup	Info Only	Displays Startup Board Temperature
Min	Info Only	Displays Min Board Temperature
Max	Info Only	Displays Max Board Temperature

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Feature	Options	Description
Board Temperature	Info Only	
Current	Info Only	Displays Current Board Temperature
Startup	Info Only	Displays Startup Board Temperature
Min	Info Only	Displays Min Board Temperature
Max	Info Only	Displays Max Board Temperature

7.3.8 Watchdog Timer

Feature	Options	Description
Watchdog Timer	Info only	
Power-Up Watchdog	**Disabled** Enabled	The Power Up Watchdog resets the system after a certain amount of time after power up. Pressing F12 during start up disables the Power Up Watchdog
Timeout	**65535**	Here you can enter the time the Power Up Watchdog should wait until it resets the system. The value range starts at 24 and ends at 65535.
RunTime Watchdog	**Disabled** Enabled	The RunTime Watchdog resets the system after a certain amount of time after power up.
Timeout	**24**	Here you can enter the time the Runtime Watchdog should wait until it resets the system. The value range starts at 30 and ends at 65535.

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7.3.9 Super I/O Configuration

Feature	Options	Description
Super I/O Configuration	Info only	
IT5121E Super I/O Configuration	Submenu	System Super I/O Chip Parameters.
W83627DHGSEC Super I/O Configuration	Submenu	System Super I/O Chip Parameters.

7.3.9.1 Super I/O Configuration > IT5121E Super I/O Configuration (W83627DHGSEC Super IO Configuration)

Feature	Options	Description
IT5121E Super I/O Configuration (W83627DHGSEC Super I/O Configuration)		
Serial Port 1 Configuration	Submenu	
Serial Port 2 Configuration	Submenu	

Submenu: Super I/O Configuration > Serial Port x Configuration

Feature	Options	Description
Serial Port 1 Configuration		
Serial Port 1 Configuration	Disabled, **Enabled**	Set Parameters of Serial Port 1
Device Settings	4;	
Change Settings	Auto, IO=3F8h; IRQ=4; IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12;, IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12;, IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12;, IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12;	Select an optimal setting for Super I/O Device
Change Settings	Normal, High Speed	Select an optimal setting for Super I/O Device
Serial Port 2 Configuration		

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Serial Port 2 Configuration	Disabled, **Enabled**	Set Parameters of Serial Port 2
Device Settings	3;	
Change Settings	Auto, IO=2F8h; IRQ=3;, IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12;, IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12;, IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12;, IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12;, Normal, High Speed	Select an optimal setting for Super IO Device

7.3.10 Miscellaneous

Feature	Options	Description
Power Supply Unit	Emulate AT Mode **ATX Mode**	Select the Emulation AT or ATX function. If this option is set to [Emulation AT], BIOS will report no suspend functions (S3 & S4) to ACPI OS. In windows XP, the OS will show shutdown message during a system shutdown. ATX: OS will turn off system power during a shutdown.
I2C Speed Control	**100 kbps** 400 kbps	I2C Speed Control
SMBUS Select Configuration	From EC, **From PCH**	SMBUS select configuration from PCH or EC.
WOL From S5	OFF **ON**	This Config to control power on/off LAN in S5 State by SEMA(EC).
LID Function	**Disabled** Enabled	Enable/Disable LID function.
Sleep Function	Disabled **Enabled**	Enable/Disable Sleep Function.
Smart Battery Function	**Disabled**	Enable/Disable Smart Battery function. Auto: disable Smart Battery function if charger IC not be detected.

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	Enabled Auto	

7.3.11 USB Configuration

Feature	Options	Description
USB Configuration	Info Only	
USB Module Version	Info Only	Display USB Module Version
USB Controllers:	Info Only	Display USB Controllers is XHCI or EHCI.
USB Devices:	Info Only	Display attachment USB devices.
Legacy USB Support	**Enabled** Disabled Auto	Enables Legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications.
XHCI Hand-off	**Enabled** Disabled	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by the XHCI driver.
USB Mass Storage Driver Support	Disabled **Enabled**	Enable/Disable USB Mass Storge Driver Support.
USB hardware delays and time-outs:	Info Only	
USB transfer rime-out	1 sec 5sec 10sec **20 sec**	The time-out value for Control, Bulk, and Interrupt transfers.
Device reset time-out	10 sec **20 sec** 30 sec 40 sec	USB mass storage device Start Unit command time-out.
Device power-up delay	**Auto** Manual	Maximum time the device will take before it properly reports itself to the Hot Controller. 'Auto' uses default value: for a Root port it is 100ms., for a Hub port the delay is taken from the Hub descriptor.

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Feature	Options	Description
Mass Storage Device	Info Only	

7.3.12 NVMe Configuration

Feature	Options	Description
NVMe Configuration	Info Only	

7.3.13 AMI Graphics Output Protocol Policy

Feature	Options	Description
Intel(R) Graphics Controller		
Intel(R) GOP Driver [21.0.10XX]		
Output Select	Output Select	Output Select

7.3.14 Serial Console Redirection

Feature	Options	Description
Console Redirection	**Disabled,** Enabled	To enable or disable console redirection of COMx.
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

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7.3.14.1 Serial Console Redirection > Console Redirection Settings

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Configure the type of console emulation. Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects the serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require a lower speed.
Data Bits	7 **8**	Configure the number of data bits in each transmitted or received serial character for both serial ports.
Parity	**None** Even Odd	Configures whether a parity bit is generated (transmit data) or checked. A parity bit can be sent with the data bits to detect some transmission errors. Even: The parity bit is 0 if the num of 1's in the data bits is even. Odd: The parity bit is 0 if num of 1's in the data bits is odd. Mark: The parity bit is always 1. Space: The parity bit is always 0. Mark and Space parity do not allow for error detection. They can be used as an additional data bit.
Stop Bits	**1** 2	Configures the number of stop bits transmitted and received in each serial character for both serial ports. Stop bits indicate the end of a serial data packet (a start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware Software	Configures flow control for console redirection. Hardware flow control uses RTC/CTS. Software flow control uses XON/XOFF.
VT-UTF8 Combo Key Support	Disabled **Enabled**	Enable VT-UTF8 combination key support for ANSI/VT100 terminals.
Recorder Mode	**Disabled** Enabled	With this mode enabled, only text will be sent. This is to capture terminal data.
Resolution 100x31	**Disabled** Enabled	Enables or disables extended terminal resolution.

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Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Select Function Keys and Key Pad on Putty.

7.3.15 Network Stack Configuration

Feature	Options	Description
Network Stack	**Disabled**, Enabled	Enable/Disable UEFI Network Stack
IPv4 PXE Support	**Disabled**, Enabled	Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.
IPv4 HTTP Support	**Disabled**, Enabled	Enable/Disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.
IPv6 PXE Support	**Disabled**, Enabled	Enable/Disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.
IPv6 HTTP Support	**Disabled**, Enabled	Enable/Disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.
PXE boot wait time	[Max-Value, Min-Value, Step-Value] = [0x05, **0x00**, 0x01]	Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.
Media detect count	[Max-Value, Min-Value, Step-Value] = [0x32, **0x01**, 0x01]	Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

7.3.16 Trusted Computing

Feature	Options	Description
Security Device Support	**Disable**, Enable	Enables or disables BIOS support for a security device. The O.S. will not show the security device. TCG EFI protocol and INT1A interface will not be available.
NO Security Device Found		

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7.4 Chipset

Feature	Options	Description
System Agent (SA) Configuration	submenu	
PCH-IO Configuration	submenu	

7.4.1 System Agent (SA) Configuration

Feature	Options	Description
Memory Configuration	submenu	
Graphics Configuration	submenu	
TCSS setup menu	submenu	
Stop Grant Configuraion	**Auto,** Manual	Automatic/Manual stop grant configuration
VT-d	**Enabled,** Disabled	VT-d capability
Control Iommu Pre-boot Behavior	**Disable IOMMU** Enable IOMMU during boot	Enable IOMMU in Pre-boot environment (If DMAR table is installed in DXE and If VTD_INFO_PPI is installed in PEI.)
X2APIC Opt Out	Enabled**, Disabled**	Enable/Disable X2APIC_OPT_OUT bit
DMA Control Guarantee	**Enabled,** Disabled	Enable/Disable DMA_CONTROL_GUARANTEE bit
WRC Feature	Enabled**, Disabled**	Enable/Disable SA WRC (Write Cache) Feature of IOP. When enabled, supports I/O devices allocating onto the ring and into LLC.
Above 4GB MMIO BIOS assignment	**Enabled,** Disabled	Enable/Disable above 4GB MemoryMappedIO BIOS assignment. This is enabled automatically when Aperture Size is set to 2048MB.
IPU Device (B0:D5:F0)	Enabled**, Disabled**	Enable/Disable SA IPU Device
IPU 1181 Dash Camera	Enabled**, Disabled**	Enable/Disable SA IPU 1181 Dash Camera support

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7.4.1.1 System Agent (SA) Configuration > Memory Configuration

Feature	Options	Description
Memory RC Version	**Info-only**	
Memory Frequency	**Info-only**	
Memory Timings (tCL-tRCD-tRP-tRAS)	**Info-only**	
Controller x Channel x Slot x	**Info-only**	
Size	**Info-only**	
Number of Ranks	**Info-only**	
Manufacturer	**Info-only**	
Memory Test on Warm Boot	**Enabled,** Disabled	Enable Or Disable Base Memory Test Run on Warm Boot
Maximum Memory Frequency	**Auto** 1067 1333 1400 1600 1800 1867 2000 2133 2200 2400 2600 2667 2800 2933 3000 3200 12800	Maximum Memory Frequency Selections in Mhz.
Max TOLUD	**Dynamic**	Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO

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	1 GB 1.25 GB 1.5 GB 1.75 GB 2 GB 2.25 GB 2.5 GB 2.75 GB 3 GB 3.25 GB 3.5 GB	length of installed graphic controller
SA GV	**Enabled,** Disabled	System Agent Geyserville. Can disable, fix to a specific point, or enable frequency swithing.
Controller 0, Channel X DIMM Control	**Enabled,** Disabled	Controller 0, Channel X DIMM Control Support - Enable or Disable Dimms on Controller 0, Channel X.
Controller 1, Channel X DIMM Control	**Enabled,** Disabled	Controller 1, Channel X DIMM Control Support - Enable or Disable Dimms on Controller 1, Channel X.
Force Single Rank	**Disabled,** Enabled	When enabled, only Rank 0 will be used in each DIMM
In-Band ECC Support (Industrial SKU only)	Enabled**, Disabled**	Enable/Disable In-Band ECC. Either the IBECC or the TME can be enabled.

7.4.1.2 System Agent (SA) Configuration > Graphics Configuration

Feature	Options	Description
Skip Scaning of External Gfx Card	**Disabled**, Enabled	If enabled, it will not scan for External Gfx Card on the PEG and PCH PCIe ports.
Primary Display	**Auto**, IGFX, PEG Slot, PCH PCI, HG	Select which of the IGFX/PEG/PCI Graphics devices should be the primary display or select HG for Hybrid Gfx.
External Gfx Card Primary Display Configuration	submenu	
Internal Graphics	**Auto**, Disabled, Enabled	Keep IGFX enabled based on the setup options.
GTT Size	2MB, 4MB, **8MB**	Select the GTT Size
Aperture Size	128MB, **256MB**, 512MB,	Select the Aperture Size

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	1024MB	
DVMT Pre-Allocated	0M, 32M, 64M, 96M, 128M, 160M, 4M, 8M, 12M, 16M, 20M, 24M, 28M, 32M/F7, 36M, 40M, 44M, 48M, 52M, 56M, **60M**	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.
Intel Graphics Pei Display Peim	Enabled, **Disabled**	Enable/Disable Pei (Early) Display

7.4.1.3 System Agent (SA) Configuration > TCSS setup menu

Feature	Options	Description
IOM FW version:	**Info-only**	
PHY FW version:	**Info-only**	
TBT FW IMR Status:	**Info-only**	
TBT FW version:	**Info-only**	
Deepest TC state:	**Info-only**	
TCSS xHCI Support	Disabled, **Enabled**	Enable/Disable TCSS xHCI
TCSS USB Configuration	submenu	SA TCSS USB Configuraion settings
VCCST status of IOM	Disabled, **Enabled**	Enables/Disables VCCST. Enable: Sends VCCST ON message to EC or PMC Disable: Sends VCCST OFF message to EC or PMC
D3 Cold Enable/Disable	**Disabled**, Enabled	Enables/Disables D3 Cold. Enable: D3 cold support for IOM is enabled. Disable: D3 cold support for IOM is Disabled
D3Hot	Disabled, **Enabled**	Enables/Disables D3 Hot. Enable: D3 Hot support for IOM is enabled. Disable: D3 Hot support for IOM is Disabled
Tc C-State Limit	Disable, 1, 2, 4, 5, 6, 7, 10	BIOS mailbox to limit deepest TCx state
TC Cold Power Saving Factor	**Disabled**, Enabled	TC Cold Power Saving Factor Switch

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7.4.1.3.1 System Agent (SA) Configuration > TCSS setup menu > TCSS USB Configuration

Feature	Options	Description
USB CONNECT OVERRIDE	**Disabled**, Enabled	This option will allow VCCSTTPC to turn off even when there is a connection for a USB3 port.
TCSS xDCI Support	**Disabled**, Enabled	Enable/Disable TCSS xDCI
TCSS CPU USB PDO Programming	Disabled, **Enabled**	Select 'Enabled' if the Port Disable Override functionality is used.
TCSS CPU USB Port Disable Override	**Disabled**, Select Per-Pin	Selectively Enable/Disable the corresponding USB port from reporting a device connection to the controller.

7.4.1.3.2 System Agent (SA) Configuration > MIPI Camera Configuration

Feature	Options	Description
CVF Support	**Disabled**, Enabled	Disables/Enables CVF using either Native IOs or USB IOs expansion.
Control Logic 1	Disabled, **Enabled**	Control Logic 1
Control logic options	submenu	Control logic options
Control logic 2	Disabled, **Enabled**	Control logic 2
Control logic options	submenu	Control logic options
Camera1	Disabled, **Enabled**	Camera1
Link options	submenu	Link options
Camera2	Disabled, **Enabled**	Camera2
Link options	submenu	Link options

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7.4.2 PCH-I/O Configuration

Feature	Options	Description
PCI Express Configuration	Submenu	
SATA Configuration	Submenu	
USB Configuration	Submenu	
Security Configuration	Submenu	
HD Audio Configuration	Submenu	
Serial IO Configuration	Submenu	
SCS Configuration	Submenu	
PCH LAN Controller	Info-Only	No GbE Region
Port 80h Redirection	Fixed setting - LPC Bus	Control where the Port 80h cycles are sent.
Enhance Port 80h LPC Decoding	**Enabled**, Disabled	Support the word/dword decoding of port 80h behind LPC
Enable TCO Timer	**Disabled**, Enabled	Enable/Disable TCO timer. When disabled, it disables the PCH ACPI timer, stops TCO timer, and ACPI WDAT table will not be published.
PCIe Ref Pll SSC	**Auto**, 0.0%, 0.1%, 0.2%, 0.3%, 0.4%, 0.5%, Disabled	PCIe Pll SSC percentage. AUTO - Keeps hardware default, no BIOS override. Range is 0.0%-0.5%.
SPD Write Disable	**TRUE**, FALSE	Enable/Disable the SPD Write Disable setting. For security recommendations, the SPD write disable bit must be set.

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7.4.2.1 PCH-I/O Configuration > PCI Express Configuration

Feature	Options	Description
DMI Link ASPM Control	**Disabled**, L0s, L1, L0sL1, Auto	The control of Active State Power Management of the DMI Link.
Port8xh Decode	**Disabled**, Enabled	PCI Express Port8xh Decode Enable/Disable.
PCIe Ports 3-4 Configuration	**2x1 Port,** 1x2 Port	Notes: Please make sure to complete the system boots after changing the configuration. Do Not Attempt to Shut Down Your Computer, doing that may lead to system malfunction.
PCIe Ports 9-10 Configuration	**2x1 Port,** 1x2 Port	Notes: Please make sure to complete the system boots after changing the configuration. Do Not Attempt to Shut Down Your Computer, doing that may lead to system malfunction.
PCI Express Root Port 1	Submenu	
PCI Express Root Port 2	**Info-Only**	
PCI Express Root Port 3 (COMe Lane 0)	Submenu	
PCI Express Root Port 4 (COMe Lane 1)	Submenu	
PCI Express Root Port 5	**Info-Only**	
PCI Express Root Port 6	**Info-Only**	
PCI Express Root Port 7	Submenu	.
PCI Express Root Port 8	**Info-Only**	
PCI Express Root Port 9 (COMe Lane 2)	Submenu	
PCI Express Root Port 10 (COMe Lane 3)	Submenu	
PCI Express Root Port 11	**Info-Only**	
PCI Express Root Port 12	**Info-Only**	

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7.4.2.2 PCH-I/O Configuration > PCI Express Configuration > PCI Express Root Port#

Feature	Options	Description
PCI Express Root Port	Disabled **Enable**	Control the PCI Express Root Port.
Connection Type	Built-in **Slot**	Built-In: a built-in device is connected to this rootport. SlotImplemented bit will be clear. Slot: this rootport connects to user-accessible slot. SlotImplemented bit will be set.
ASPM	**Disabled** L0s L1 L0sL1 Auto	Set the ASPM Level. Force L0s - Force all links to L0s State Auto - BIOS auto configure; Disabled - Disables ASPM
L1 Substates	Disabled L1.1 **L1.1 & L1.2**	PCI Express L1 Substates settings.
L1 Low	Disabled **Enable**	PCI Express L1 Low Substate Enable/Disable.
ACS	Disabled **Enable**	Enable/Disable Access Control Services Extended Capability
PTM	Disabled **Enable**	Enable/Disable Precision Time Measurement
DPC	**Disabled** Enable	Enable/Disable Downstream Port Containment
EDPC	Disabled **Enable**	Enable/Disable Rootport extensions for Downstream Port Containment
URR	**Disabled** Enable	PCI Express Unsupported Request Reporting Enable/Disable.
FER	**Disabled** Enable	PCI Express Device Fatal Error Reporting Enable/Disable.

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Feature	Options	Description
NFER	**Disabled** Enable	PCI Express Device Non-Fatal Error Reporting Enable/Disable.
CER	**Disabled** Enable	PCI Express Device Correctable Error Reporting Enable/Disable.
CTO	**Disabled** Enable	PCI Express Completion Timer TO Enable/Disable
SEFE	**Disabled** Enable	Root PCI Express System Error on Fatal Error Enable/Disable.
SENFE	**Disabled** Enable	Root PCI Express System Error on Non-Fatal Error Enable/Disable.
SECE	**Disabled** Enable	Root PCI Express System Error on Correctable Error Enable/Disable.
PME SCI	Disabled **Enable**	PCI Express PME SCI Enable/Disable.
Hot Plug	**Disabled** Enable	PCI Express Hot Plug Enable/Disable.
Advanced Error Reporting	Disabled **Enable**	Advanced Error Reporting Enable/Disable.
PCIe Speed	**Auto** Gen1 Gen2 Gen3	Configure PCIe Speed.
Transmitter Half Swing	**Disabled** Enabled	Transmitter Half Swing Enable/Disable.
Detect Non-Compliance	**Disabled** Enable	Detect Non-Compliance PCI Express Device. If enabled, it will take more time at POST time.
Detect Timeout	**0**	The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming

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Feature	Options	Description
		there is no device and potentially disabling the port.
Extra Bus Reserved	**0**	Extra Bus Reserved (0-7) for bridges behind this Root Bridge.
Reserved Memory	**10**	Reserved Memory for this Root Bridge (1-20) MB.
Reserved I/O	**4**	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.
PCH PCIe LTR Configuration	Info only	
LTR	Disabled **Enable**	PCH PCIe Latency Reporting Enable/Disable.
Snoop Latency Override	Disabled Manual **Auto**	Snoop Latency Override for PCH PCIe. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow."
Non-Snoop Latency Override	Disabled Manual **Auto**	Non-Snoop Latency Override for PCH PCIe. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
LTR Lock	**Disabled** Enable	PCIe LTR Configuration Lock

7.4.2.3 PCH-I/O Configuration > SATA Configuration

Feature	Options	Description
SATA Controller(s)	Disabled, **Enabled**	Enable/Disable SATA Device.
SATA Mode Selection	AHCI	Determines how SATA controller(s) operate.
SATA Controller Speed	Default, Gen1, **Gen2**, Gen3	Indicates the maximum speed the SATA controller can support.
SATA Test Mode	**Disabled**, Enabled	Test Mode Enable/Disable (Loop Back).

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Aggressive LPM Support	Disabled, **Enabled**	Enable PCH to aggressively enter link power state.
Serial ATA Port X	Info-Only	
Software Preserve	Info-Only	
Port X	Disabled, **Enabled**	Enable or Disable SATA Port
Hot Plug	**Disabled**, Enabled	Designates this port as Hot Pluggable.
Configured as eSATA	Info Only	
External	**Disabled**, Enabled	Marks this port as external.
Spin Up Device	**Disabled**, Enabled	If enabled for any of ports Staggered Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise, all drives spin up at boot.
SATA Device Type	**Hard Disk Drive**, Solid State Drive	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive
Topology	**Unknown** ISATA Direct Connect Flex M2	Identify the SATA Topology if it is Default or ISATA or Flex or DirectConnect or M2
SATA Port X DevSlp	**Disabled**, Enabled	
DITO Configuration	**Disabled**, Enabled	
DITO Value	**625**	
DM Value	**15**	

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7.4.2.4 PCH-I/O Configuration >USB Configuration

Feature	Options	Description
xDCI Support	**Disabled**, Enabled	Enable/Disable xDCI (USB OTG Device).
USB2 PHY Sus Well Power Gating	Disabled, **Enabled**	Select 'Enabled' to enable SUS Well PG for USB2 PHY. This option has no effect on PCH-H
USB PDO Programming	Disabled, **Enabled**	Select 'Enabled' if the Port Disable Override functionality is used.
USB Overcurrent	Disabled, **Enabled**	Select 'Disabled' for the pin-based debug. If the pin-based debug is enabled but USB overcurrent is not disabled, USB DbC will not work.
USB Overcurrent Lock	Disabled, **Enabled**	Select 'Enabled' if the Overcurrent functionality is used. Enabling this will make xHCI controller consume the Overcurrent mapping data
USB Audio Offload	Disabled, **Enabled**	Enable/Disable USB Audio Offload functionality
Enable HSII on xHCI	Disabled, **Enabled**	Enable/Disable the HSII feature. It may lead to increased power consumption.
USB3.1 Portx Speed Selection	0	Port Selection value in decimal for Gen1; Default - Gen2; Bit 0 corresponds to Port 0 and so on
USB Port Disable Override	**Disabled**, Select Per-Pin	Selectively Enable/Disable the corresponding USB port from reporting a device connection to the controller.

7.4.2.5 PCH-I/O Configuration > Security Configuration

Feature	Options	Description
RTC Memory Lock	Disabled, **Enabled**	Enabling it will lock bytes 38h-3Fh in the lower/upper 128-byte bank of RTC RAM
BIOS Lock	**Disabled**, Enabled	Enable/Disable the PCH BIOS Lock Enable feature. Required to be enabled to ensure the SMM protection of flash.
Force unlock on all GPIO pads	**Disabled**, Enabled	If Enabled BIOS will force all GPIO pads to be in unlocked state

7.4.2.6 PCH-I/O Configuration > HD Audio Configuration

Feature	Options	Description
HD Audio	Disabled **Enabled**	Control Detection of the HD-Audio device.

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7.4.2.7 PCH-I/O Configuration > Serial IO Configuration

Feature	Options	Description
I2C0 Controller	Disabled**, Enabled**	Enables/Disables Serial IO Controller
I2C1 Controller	Disabled**, Enabled**	Enables/Disables Serial IO Controller
SPI0 Controller	**Disabled,** Enabled	Enables/Disables SPI0 Controller
UART0 Controller	Disabled**, Enabled**, Communication port (COM)	Enables/Disables Serial IO Controller
UART1 Controller	**Disabled,** Enabled, Communication port (COM)	Enables/Disables Serial IO Controller
GPIO IRQ Route	**IRQ14,** IRQ15	Route all GPIOs to one of the IRQ.

7.4.2.8 PCH-I/O Configuration > SCS Configuration

Feature	Options	Description
eMMC 5.1 Controller	Disabled**, Enabled**	Enable or Disable SCS eMMC 5.1 Controller
eMMC 5.1 HS400 Mode	Disabled**, Enabled**	Enable or Disable SCS eMMC 5.1 HS400 Mode
Enable HS400 software tuning	**Disabled,** Enabled	Software tuning should improve eMMC HS400 stability at the expense of boot time
Driver Strength	33 Ohm**, 40 Ohm**, 50 Ohm	Sets I/O driver strength
UFS 2.0 Controller 1	**Disabled,** Enabled,	Enable or Disable UFS 2.0 Controller

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7.5 Security

Feature	Options	Description
Password Description	Info only	
Administrator Password	Enter password	
User Password	Enter password	
Secure Boot menu	submenu	

7.5.1 Secure Boot menu

Feature	Options	Description
Secure Boot	**Disabled** Enabled	The Secure Boot feature is Active if Secure Boot is Enabled, the platform Key(PK) is enrolled and the system is in User mode, The mode change requires a platform reset
Secure Boot Mode	**Standard** Custom	Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication
Restore Factory Keys		Force System to User Mode. Install factory default Secure Boot key databases
Reset To Setup Mode		Delete all Secure Boot Key databases from NVRAM.
Key Management	**Submenu**	Enables expert users to modify. Secure Boot Policy variables without variable authentication.

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7.6 Boot

7.6.1 Boot Configuration

Feature	Options	Description
Boot Configuration	Info only	
Setup Prompt Timeout	**1**	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
Bootup NumLock State	On **Off**	Select the keyboard NumLock state
Quiet Boot	Disabled **Enabled**	Enables or disables Quiet Boot option
Fast Boot	Disabled **Enabled**	Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot option.
SATA Support	**Last Boot SATA Devices Only** All Sata Devices	If Last Boot SATA Devices Only is selected, only the SATA device in the last boot will be available in POST. If All SATA devices is selected, all SATA devices will be available in the OS and Post.
VGA Support	Auto **EFI Driver**	If Auto, only install Legacy OpRom with Legacy OS and logo would NOT be shown during post. Efi driver will still be installed with EFI OS.
USB Support	Disabled **Full Initial** Partial Initial	If disabled, all USB devices will NOT be available until after the OS boots. If Partial Initial, USB Mass Storage and specific USB port/device will NOT be available before the OS boots. If enabled, all USB devices will be available in OS and Post.
PS2 Devices Support	Disabled **Enabled**	If disabled, PS2 devices will be skipped.
NetWork Stack Driver Support	**Disabled** Enabled	If disabled, NetWork Stack Driver will be skipped.
Redirection Support	Disabled **Enabled**	If disabled, the Redirection function will be disabled.

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Feature	Options	Description
Boot Mode select	**UEFI** LEGACY	Select boot mode LEGACY/UEFI
FIXED BOOT ORDER Priorities	Info only	
UEFI Hard Disk Drive BBS Priorities	**Submenu**	
UEFI Application Boot Prioriries	**Submenu**	

7.7 Save & Exit

Feature	Options	Description
Save Changes and Exit		Exit system setup after saving the changes.
Discard Changes and Exit		Exit system setup without saving any changes.
Save Change and Reset		Reset the system after saving the changes.
Discard Changes and Reset		Reset system setup without saving any changes.
Save Options	Info only	
Save Changes		Save the changes done to any of the setup options.
Discard Changes		
Restore Defaults		
Save as User Defaults		Save the changes done as user defaults.
Restore User Defaults		Restore the User Defaults to all the setup options.
Boot Override	Info only	

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8. BIOS Checkpoints, Beep Codes

This section of this document lists the checkpoints and beep codes generated by AMI Aptio BIOS. The checkpoints defined here are inherent to the AMIBIOS generic core, and do not include any chipset or board-specific checkpoint definitions.

Checkpoints and Beep Codes Definition

A checkpoint is either a byte or word value output to I/O port 80h. The BIOS outputs checkpoints throughout bootblock and Power-On Self Test (POST) to indicate the task the system is currently executing. Checkpoints are very useful for debugging problems that occur during the preboot process.

Beep codes are used by the BIOS to indicate a serious or fatal error. They are used when an error occurs before the system video has been initialized, and generated by the system board speaker.

Aptio Boot Flow

While performing the functions of the traditional BIOS, Aptio 5.x core follows the firmware model described by the Intel Platform Innovation Framework for EFI ("the Framework"). The Framework refers the following "boot phases", which may apply to various status code & checkpoint descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization[1]
- Driver Execution Environment (DXE) – main hardware initialization[2]
- Boot Device Selection (BDS) – system setup, pre-OS user interface, and selecting a bootable device (CD/DVD, HDD, USB, Network, Shell, and more)

Viewing BIOS Checkpoints

Viewing all checkpoints generated by the BIOS requires a checkpoint card, also referred to as a POST Card or POST Diagnostic Card. These are PCI add-in cards that show the value of I/O port 80h on a LED display.

Some computers display checkpoints in the bottom right corner of the screen during POST. However, this display method is limited, since it only displays checkpoints that occur after the video card has been activated.

Keep in mind that not all computers using AMI Aptio BIOS enable this feature. In most cases, a checkpoint card is the best tool for viewing AMI Aptio BIOS checkpoints.

[1]Analogous to "bootblock" functionality of legacy BIOS
[2]Analogous to "POST" functionality in legacy BIOS

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8.1 Status Code Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

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8.2 Standard Status Codes

8.2.1 SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization

SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

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8.2.2 SEC Beep Codes

None

8.2.3 PEI Phase

Status Code Progress Codes	Description
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information

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Status Code	Description
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes

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Status Code	Description
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self-test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes

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Status Code	Description
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

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8.2.4 PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

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8.2.5 DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)

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Status Code	Description
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes

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Status Code	Description
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug

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Status Code	Description
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

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8.2.6 DXE Beep Codes

# of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

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8.2.7 ACPI/ASL Checkpoint

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

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8.3 OEM-Reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

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9. Software Support

9.1 Operation System

Microsoft Windows 64-bit

Windows 10 IoT Enterprise LTSC 2021

Windows 11 IoT Enterprise LTSC 24H2

Canonical Ubuntu 64-bit

Ubuntu 20.04.4 LTSC (desktop version)

Yocto Project based on Linux 64-bit

https://github.com/ADLINK/meta-adlink-x86-64bit (TBC)

Note: Other OS might be supported by project basis. Please contact your local ADLINK representative for further discussion

x7000C SKUs (Headless SKUs) support Linux only (TBC)

9.2 Other Software

SEMA Library

Support PICMG COM Express defined EAPI and ADLINK's extensions for more embedded features. Get details in link below:

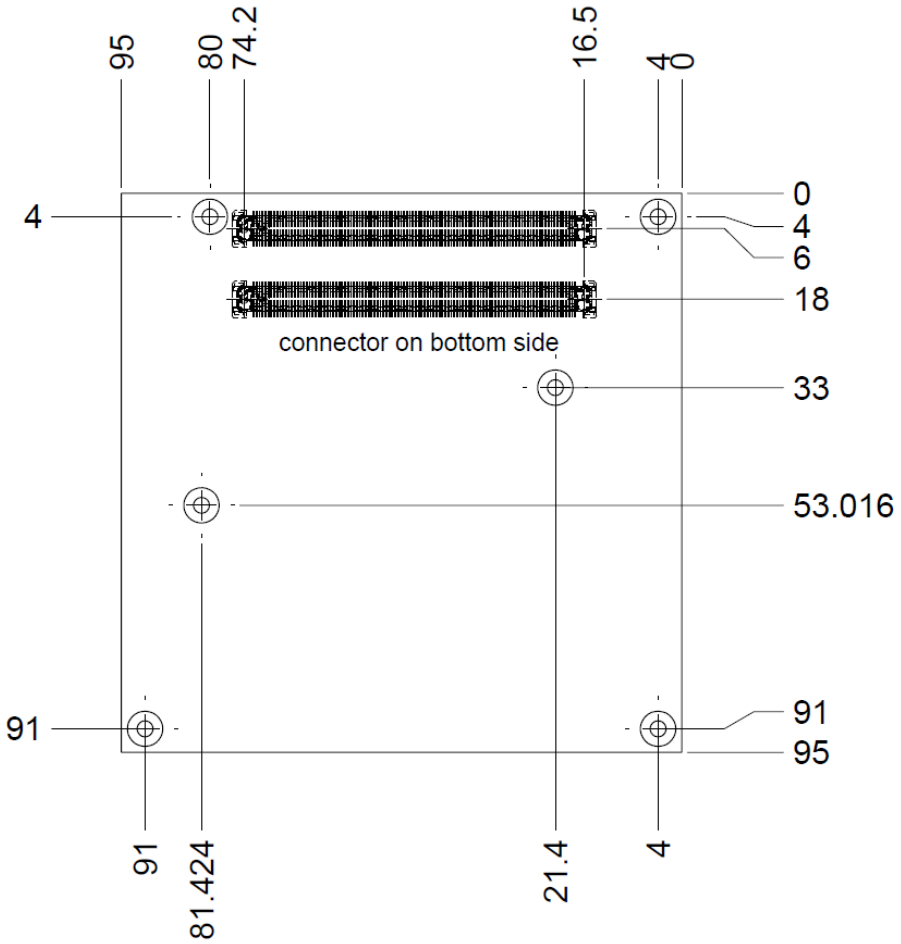
https://www.adlinktech.com/Products/DownloadMDownload?lang=en&pdNo=1274&MainCategory=Industrial_IoT_and_Cloud_solutions&kind=M

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10. Mechanical and Thermal

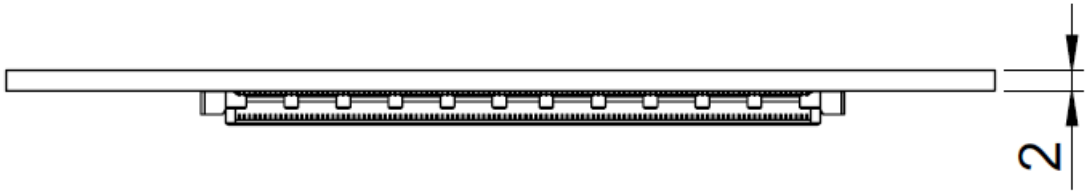
All dimensions are shown in mm with a tolerance of +/- 0.25mm unless otherwise noted.

10.1 Module Dimensions – Top View



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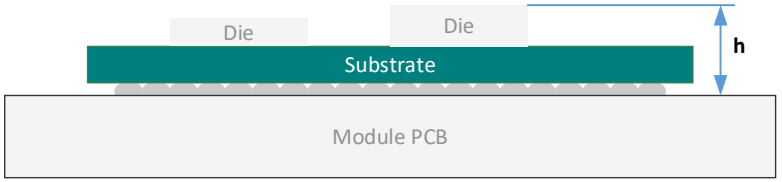
10.2 Module Dimensions – Side View



10.3 Height of Processor and Static Compressive Load

Processor Height Tolerance

The tolerance of the processor height is one of the key factors to consider when designing your thermal solution, as illustrated below. Please contact our ADLINK representative for further details.



	Typical	Tolerance
h	1.345 mm	+/- 0.109mm

Static Compressive Load

Another key factor to consider is the static compressive load. The cExpress-ASL/ALN module exhibits a maximum processor pressure die of 15 lbf.

Figure 5 – Module mechanical dimensions

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10.4 Thermal Solutions

10.4.1 Heatspreader: HTS

Dimensions: mm

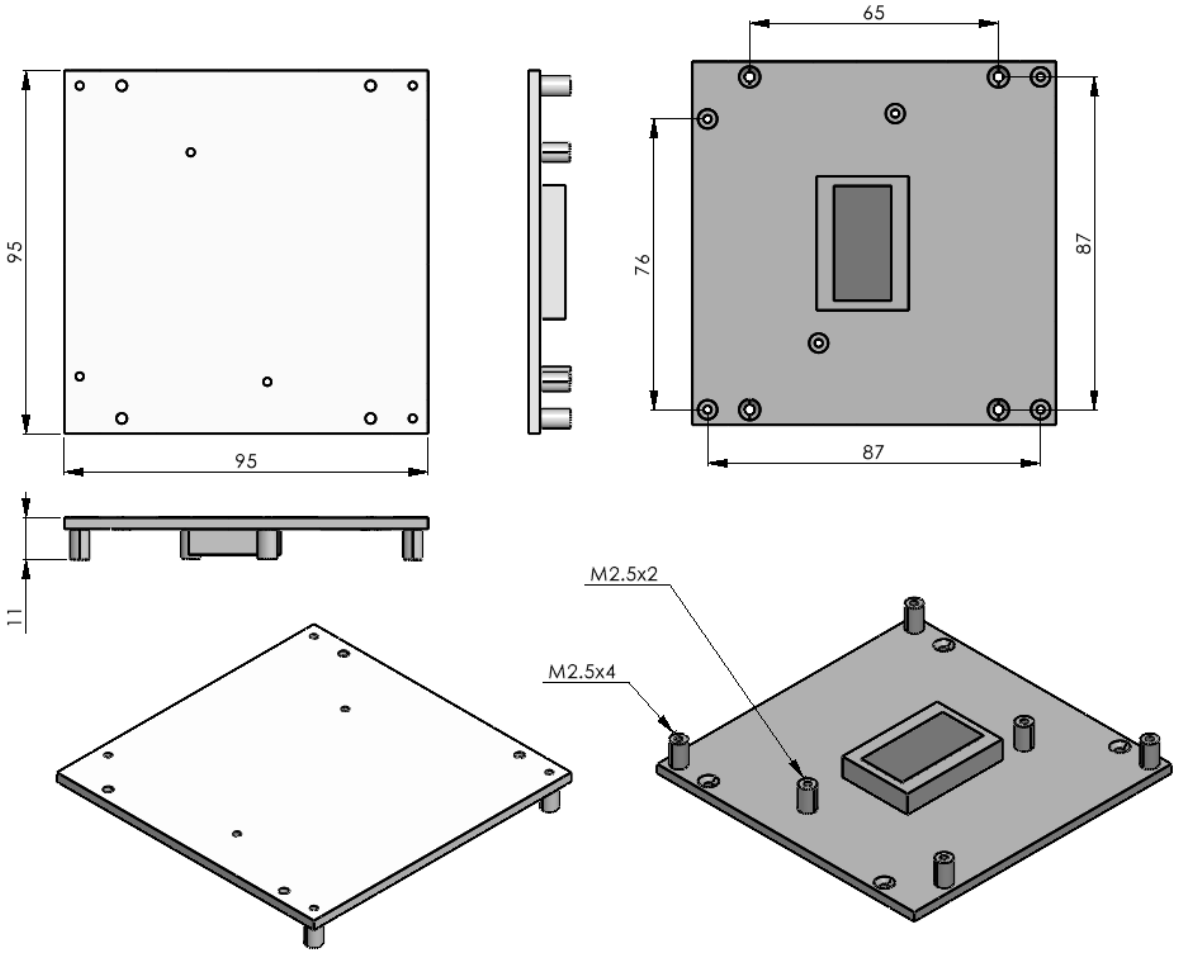


Figure 6 – Heatspreader: HTS

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10.4.2 Heatsink: THS

Dimensions: mm

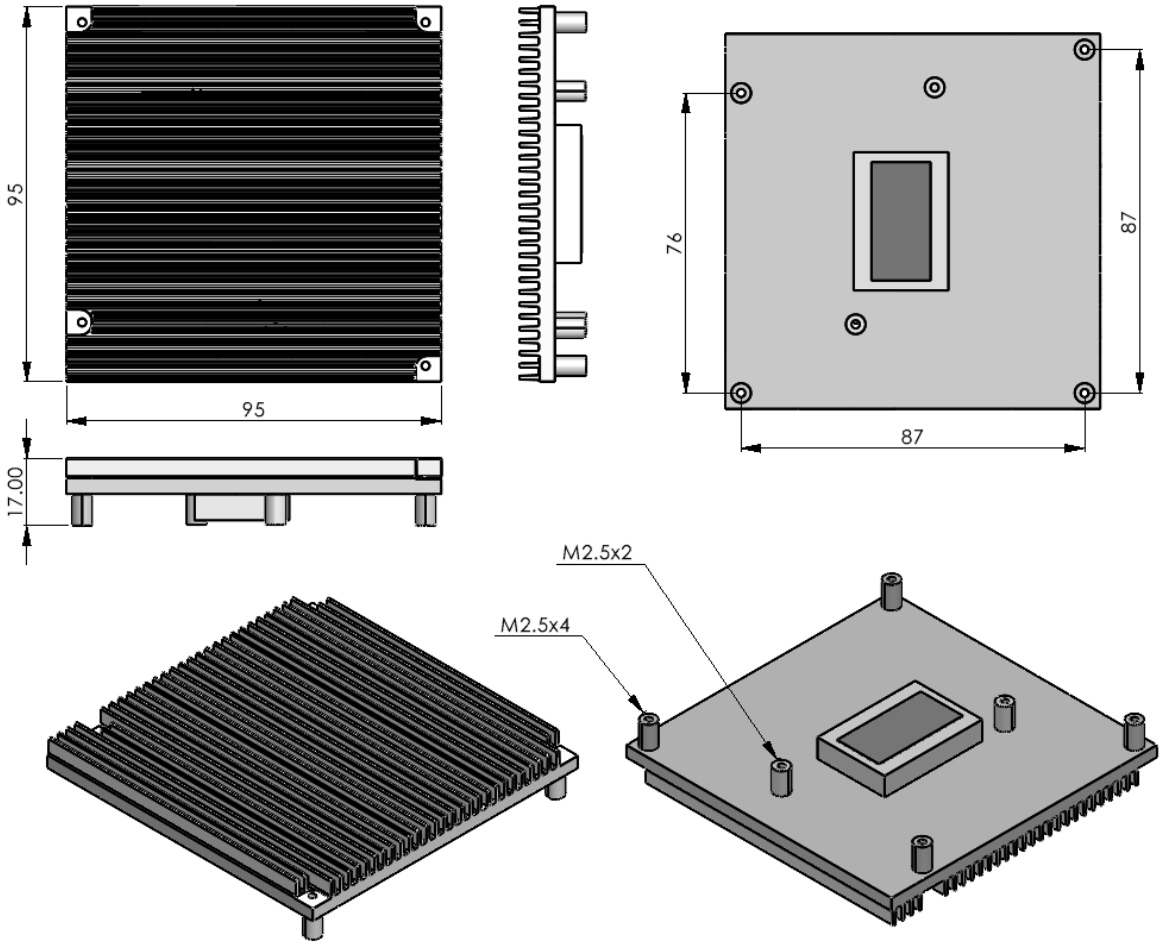


Figure 7 – Heatsink: THS

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10.4.3 Heatsink High Profile: THSH

Dimensions: mm

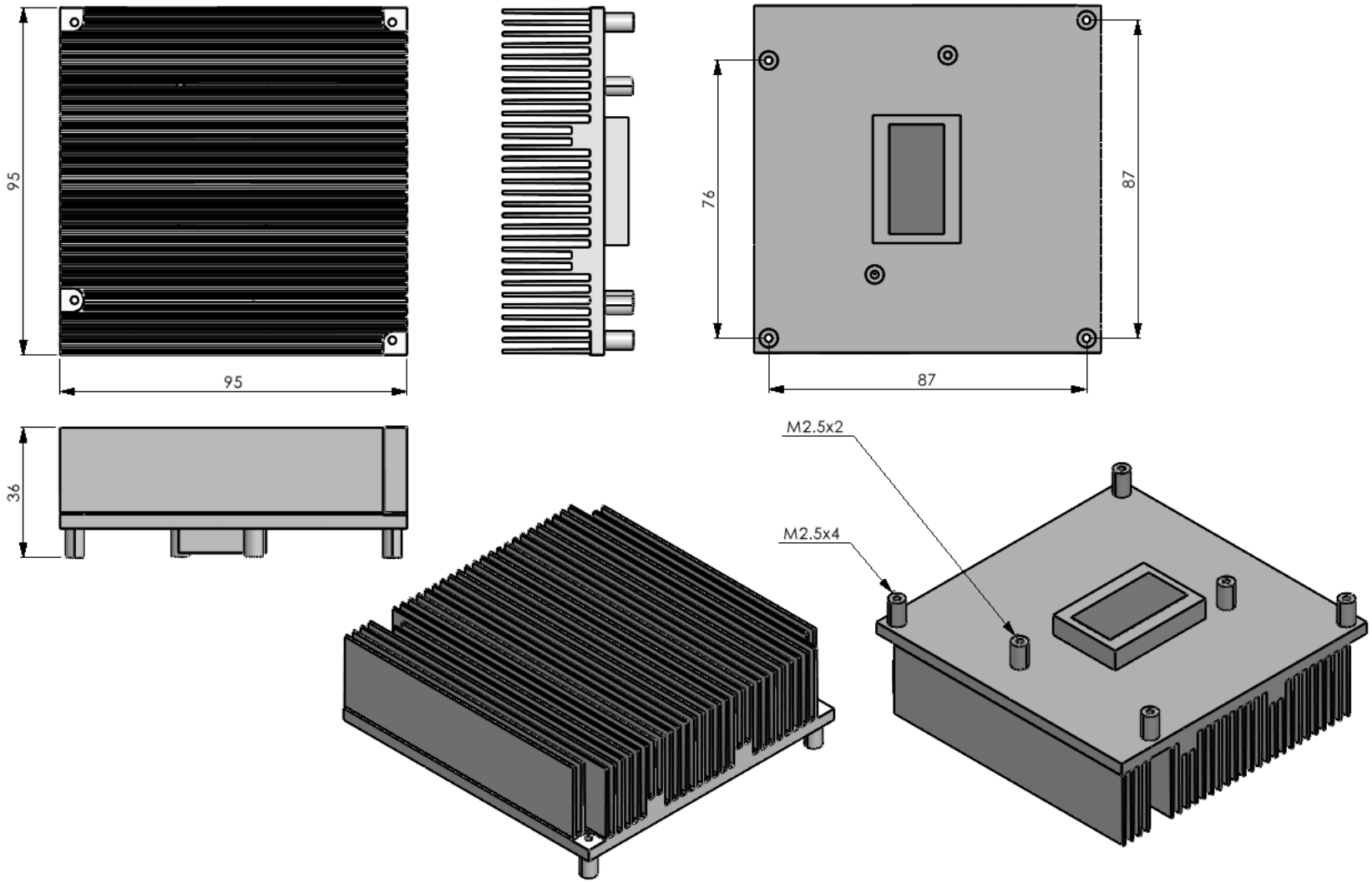


Figure 8 – Heatsink high profile: THSH

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10.4.4 Heatsink with Fan: THSF

Dimensions: mm

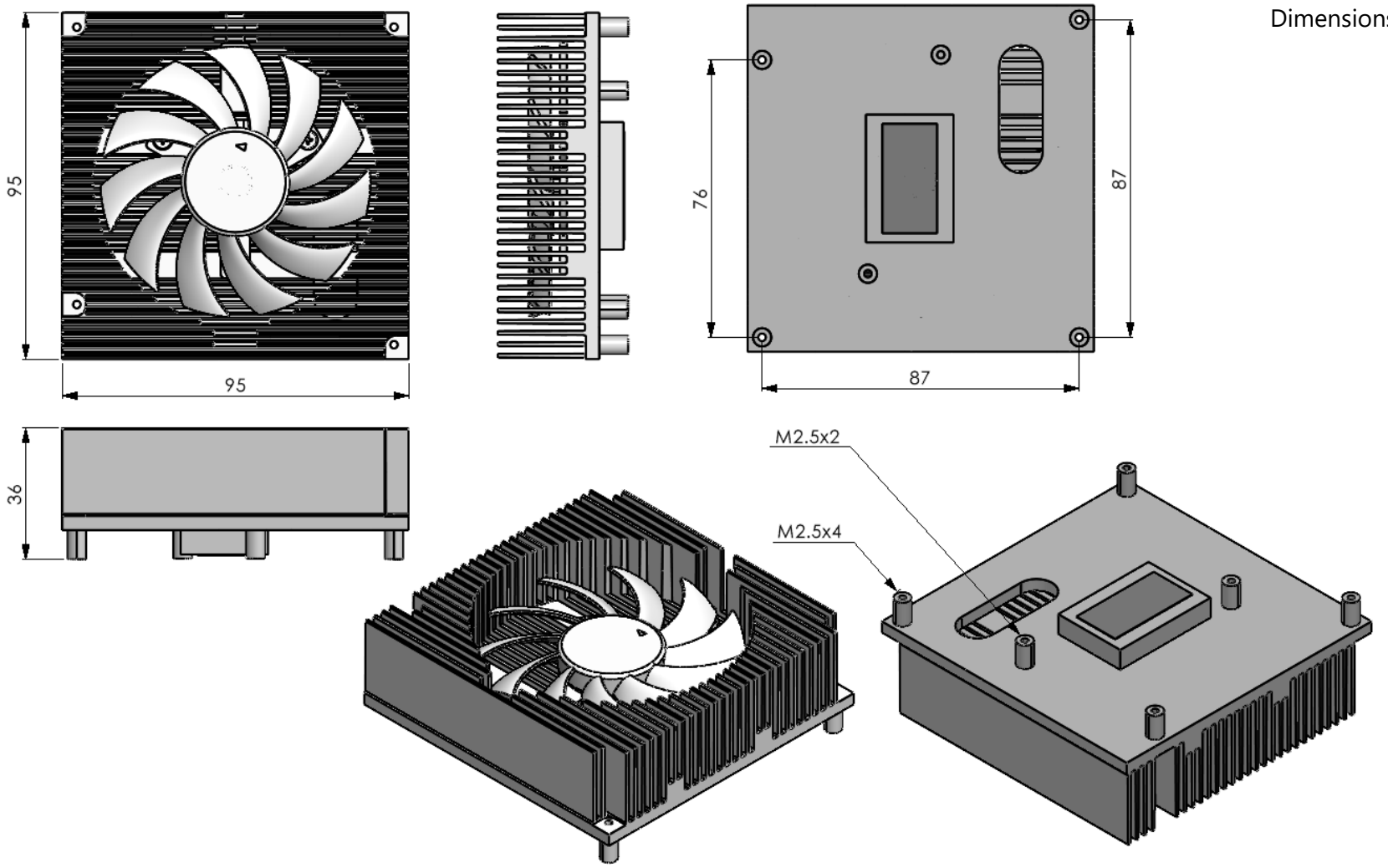


Figure 9 – Heatsink with fan: THSF

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10.5 Board to Board Connectors

To allow for different stacking heights, the receptacles for COM Express carrier boards are available in two heights: 5 mm and 8 mm. When 5 mm receptacles are chosen, the carrier board should be free of components.

220-pin board-to-board connector with 0.5mm for a stacking height of 5 mm

This connector can be used with 5 mm through-hole standoffs (SMT type).

- Tyco 3-1827253-6, Tyco 2357787-1
- ept 401-51101-51, ept 401-51103-51
- Foxconn QT002206-2141-3H, Foxconn QT5GB26-44703-3H

220-pin board-to-board connector with 0.5mm for a stacking height of 8 mm

This connector can be used with 8 mm through-hole standoffs (SMT type)

- Tyco 3-6318491-6, Tyco 2357798-1
- ept 401-55101-51, ept 401-55103-51
- Foxconn QT002206-4141-3H, Foxconn QT5GB26-74703-3H

Common Specifications

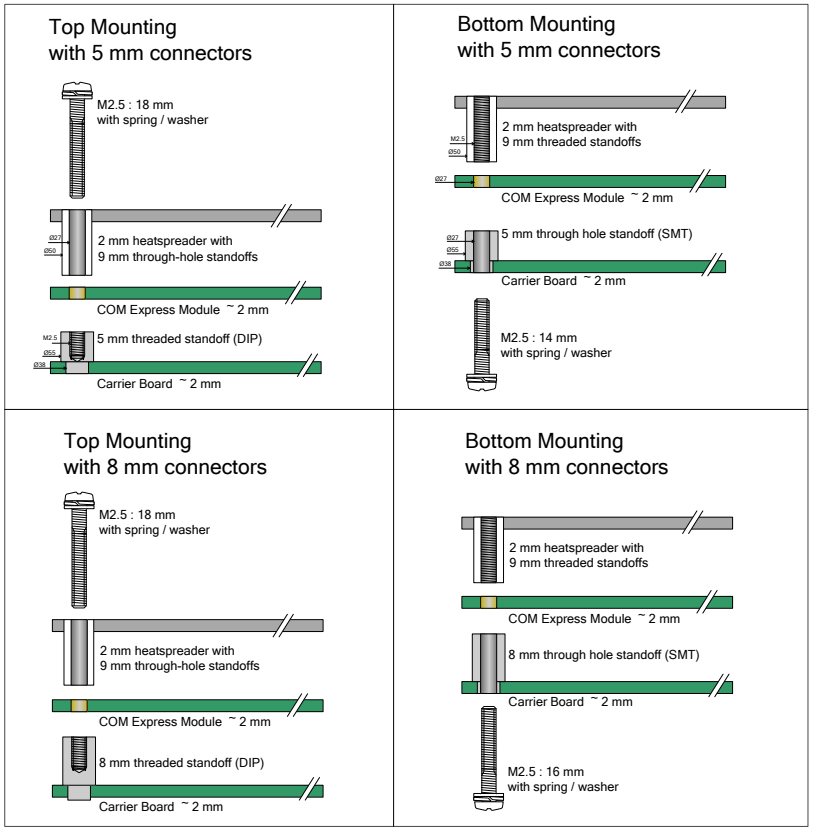
- Current capacity: 0.5A per pin
- Rated voltage: 50 VAC
- Insulation resistance: 100M or greater @ 500 VDC
- Temperature rating: -40°C ~ 85°C
- UL certification (ECBT2.E28476)

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- Copper alloy (contacts)
- Housing: thermo-plastic molded compound (L.C.P.)

10.6 Mounting Method

There are several standard ways to mount the COM Express module with a thermal solution onto a carrier board. Apart from choosing 5 mm or 8mm board-to-board connectors, you can opt for either top and bottom mounting. In top mounting, the threaded standoffs are on the carrier board and the thermal solution is equipped with through-hole standoffs. In bottom mounting, the threaded standoffs are on the thermal solution and the carrier board has through-hole standoffs.

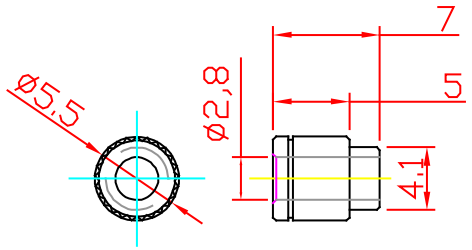


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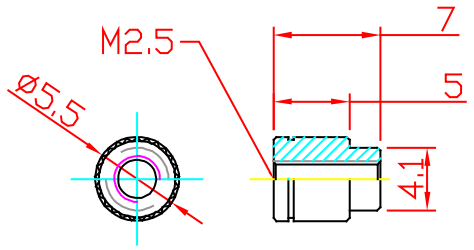
10.7 Standoff Types

The standoffs available for Top and Bottom mounting methods are shown below. Note that threaded standoffs are DIP type and through-hole standoffs are SMT type. Other types not listed are available upon request.

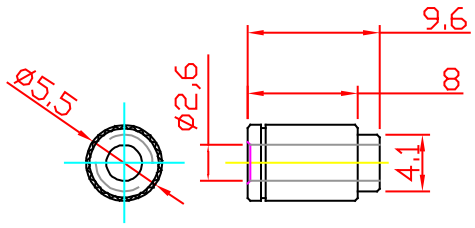
5mm through-hole standoff (SMT type)
P/N: 33-72000-0050



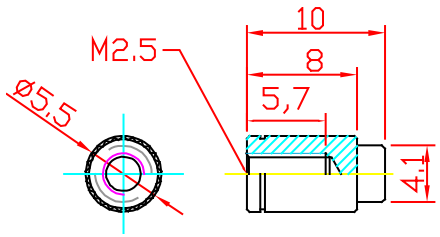
5mm threaded standoff (DIP type)
P/N: 33-72016-0050



8mm through-hole standoff (SMT type)
P/N: 33-72000-0080



8mm threaded standoff (DIP type)
P/N: 33-72015-0050

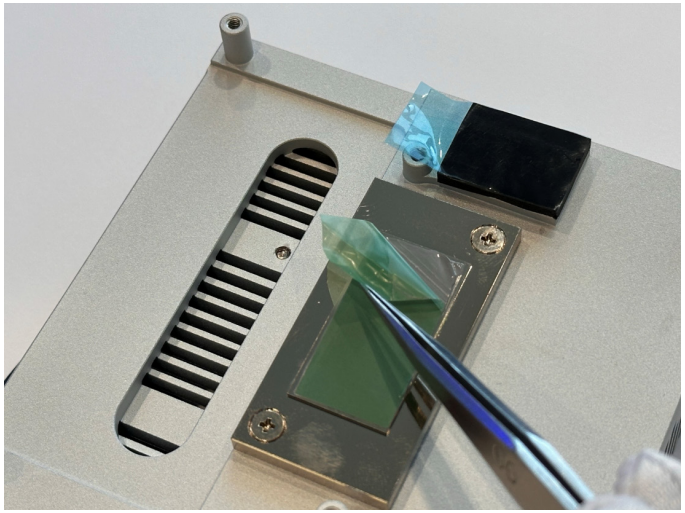


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10.8 Installation

Install a heatspreader or heatsink using the following instructions. The pictures below are for illustration purpose only.

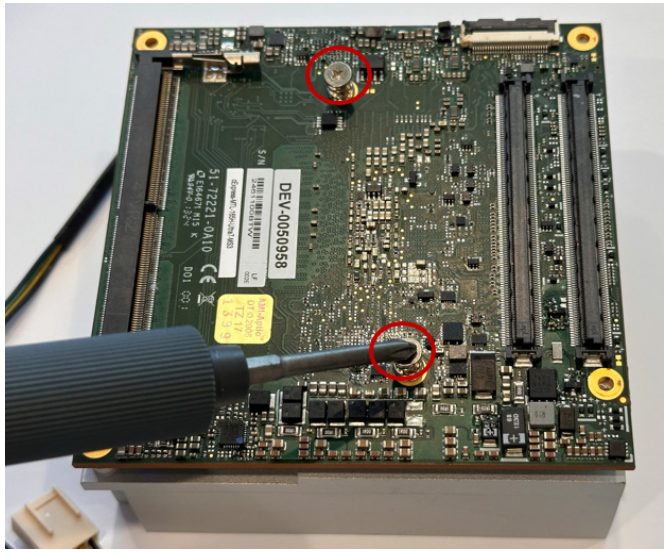
Step 1: Remove the protective membranes from the thermal pads.



Note: All thermal pads have a protective membrane, depending on the module.

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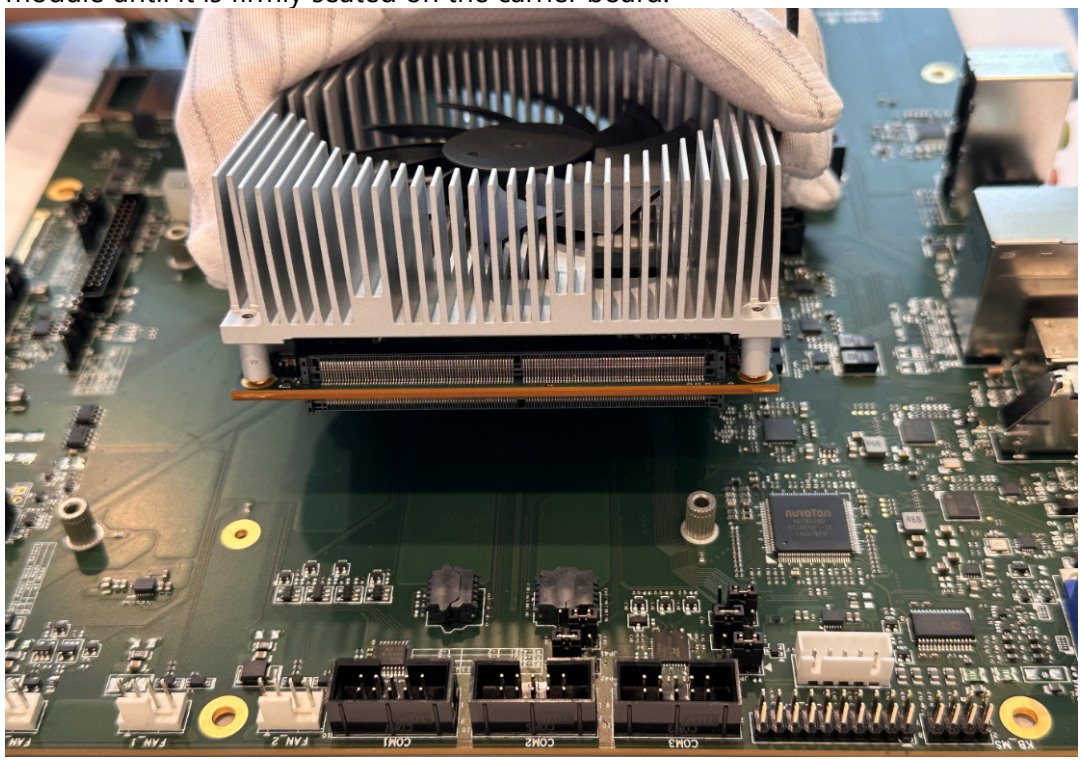
Step 2: Assemble the heatsink onto the COM Express module. Use the provided M2.5, L=6 mm screws to secure the heatsink to the module. The number of screw holes and screws depends on the module.





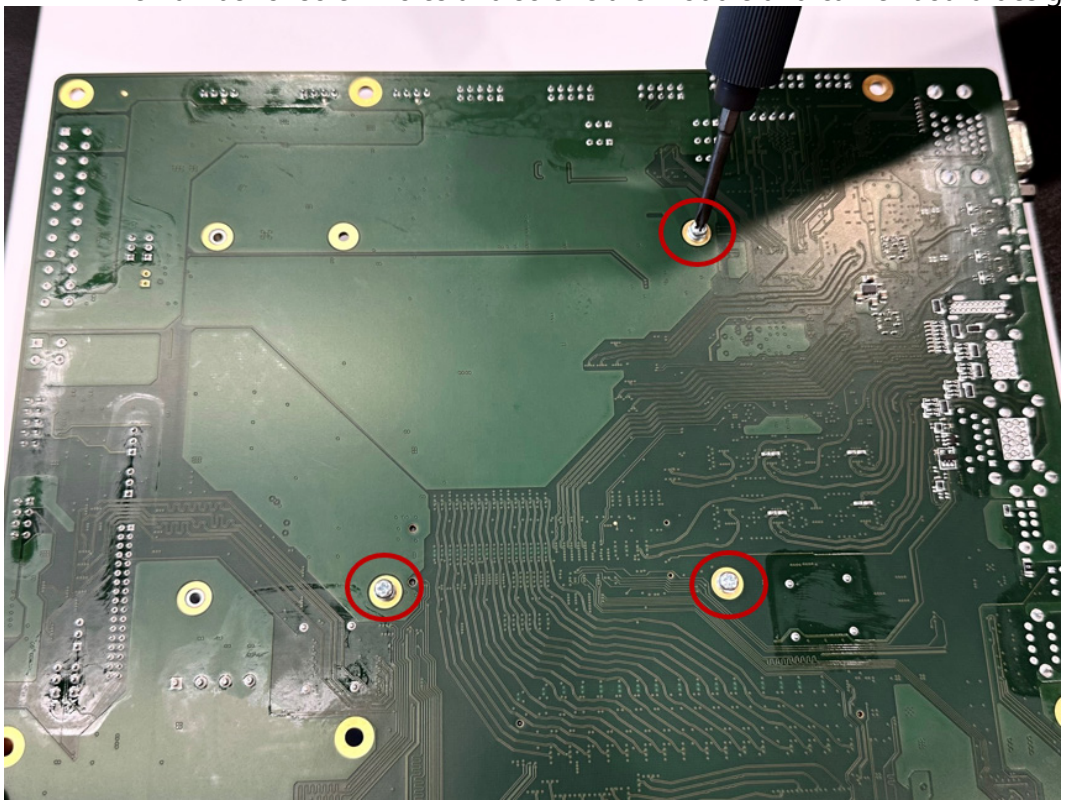
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Step 3: Place the COM Express module and heatsink assembly onto the connectors on the carrier board, as shown below. Then press down on the module until it is firmly seated on the carrier board.



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Step 4: Use the M2.5, L=16mm screws provided to secure the COM Express module to the carrier board from the solder side.
The number of screw holes and screws are module and carrier board design dependent.

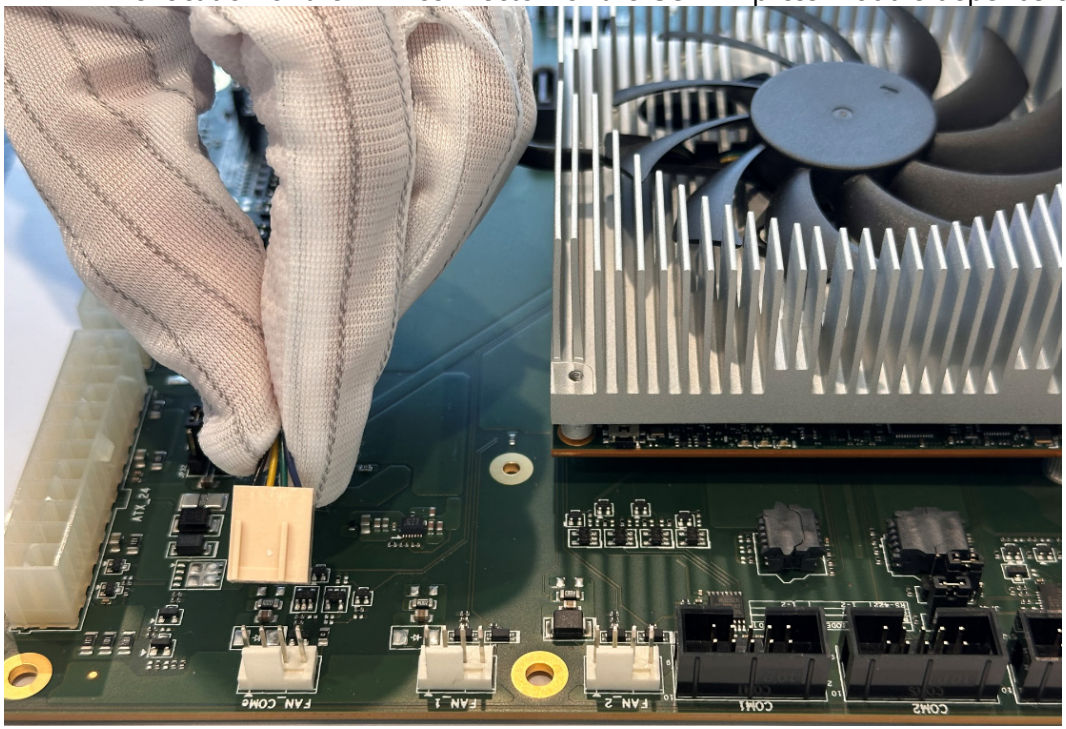




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Step 5: If you are installing a heatsink with a fan, plug the fan connector into the carrier board.

The location of the FAN connector for the COM Express module depends on carrier board design.



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