ADLINK

COM Express®

cExpress-BL

User's Manual



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Leading EDGE COMPUTING

Revision History

Revision	Description	Date	By
1.00	Initial release	2015-05-07	JC
1.01	Update CPU, COM port, power mgmt. specifications; correct LVDS pinout; correct audio, LVDS, eDP, GbE, SATA, SPI, Fan, SMBus, DDI signal descriptions; update BIOS setup	2015-07-22	JC
1.2	Update switch information	2018-01-02	JC

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Preface

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1. Introduction

The cExpress-BL is a COM Express® COM.0 R2.1 Type 6 Compact size module featuring the 64-bit 5th Generation Intel® Core™ i7/i5/i3 and Intel® Celeron® Ultra-Low TDP processors (formerly “Broadwell-U”) with CPU, memory controller, graphics processor and I/O hub on a single chip. Leveraging the benefits provided by the 5th generation Intel® Core™ and Celeron™ System-on-Chip, the cExpress-BL is specifically designed for customers who need optimum processing and graphics performance with low power consumption in a long product life solution. The cExpress-BL’s Intel® processors support Intel® Hyper-Threading Technology (up to 2 cores, 4 threads) and up to 16 GB of non-ECC DDR3L dual-channel memory at 1333/1600 MHz in dual stacked SODIMM sockets to provide excellent overall performance.

Integrated Intel® Generation 8 Graphics includes features such as OpenGL 4.2, DirectX 11.1, Intel® Clear Video HD Technology, Advanced Scheduler 2.0, 1.0, XPDM support, and DirectX Video Acceleration (DXVA) support for full AVC/VC1/MPEG2 hardware decode. Graphics outputs include dual-channel 18/24-bit LVDS (eDP optional) and two DDI ports supporting HDMI/DVI/DisplayPort. The cExpress-BL is specifically designed for customers with high-performance processing graphics requirements who want to outsource the custom core logic of their systems for reduced development time.

The cExpress-BL features a single onboard Gigabit Ethernet port, two USB 3.0 ports, six USB 2.0 ports, and four SATA 6Gb/s ports. Support is provided for SMBus and I²C. The module is equipped with SPI AMI EFI BIOS with CMOS backup, supporting embedded features such as remote console, CMOS backup, hardware monitor, and watchdog timer.

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2. Specifications

2.1. Core System

- CPU: 5th Generation Intel® Core™ processor SoC (formerly “Broadwell-U”)
  - Intel® Core™ i7-5650U 2.2 GHz (3.1 GHz Turbo), 15W (2C/GT3)
  - Intel® Core™ i5-5350U 1.8 GHz (2.7 GHz Turbo), 15W (2C/GT3)
  - Intel® Core™ i3-5010U 2.1 GHz (no Turbo), 15W (2C/GT2)
  - Intel® Celeron® 3765U 1.9 GHz (no Turbo), 15W (2C/GT1)

  Supporting: Intel® VT, Intel® TXT, Intel® SSE4.2, Intel® HT Technology, Intel® 64 Architecture, Execute Disable Bit, Intel® Turbo Boost Technology 2.0, Intel® AVX2, Intel® AES-NI, PCLMULQDQ Instruction, Intel® Device Protection Technology with Intel® Secure Key, Intel® TSXNI

  Note: Availability of features may vary between processor SKUs.
- L3 Cache: 4MB for Core™ i7, 3MB for Core™ i5 and Core™ i3, 2MB for Celeron®
- Memory: Dual channel non-ECC 1600/1333 MHz DDR3L memory up to 16 GB in dual SODIMM socket
- BIOS: AMI EFI with CMOS backup in 8MB SPI BIOS with Intel® AMT 10.0 support (AMT supported on i7/i5 SKUs only)

2.2. Expansion Busses

- 4x PCI Express x1 (AB): Lanes 0/1/2/3
- LPC bus, SMBus (system), I^2C (user)

2.3. Video

- Integrated on Processor: Intel® Generation 8 Graphics core architecture
- GPU Feature Support:
  - 3 independent and simultaneous display combinations of DisplayPort/HDMI/LVDS monitors (eDP optional in place of LVDS)
  - Encode/transcode HD content
  - Playback of high definition content including Blu-ray Disc
  - Playback of Blu-ray disc S3D content using HDMI (1.4a spec compliant with 3D)
  - DirectX Video Acceleration (DXVA) support for accelerated video processing
  - Full AVC/VC1/MPEG2 HW decode
  - Advanced Scheduler 2.0, 1.0, XPDM support
  - DirectX 11.1
  - Multi Display Support: 3 independent displays

  Note: Availability of features may vary between operating systems.

- Display Types
  - Single/dual channel 18/24-bit LVDS via eDP-to-LVDS chip

    (eDP available as BOM option in place of LVDS)
  - 2x Digital Display Ports
    DDI1 supports DisplayPort/HDMI/DVI
    DDI2 supports DisplayPort/HDMI/DVI

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2.4. Audio

- Integrated: Intel® HD Audio integrated on SoC
- Codec: Realtek ALC886 on Express-BASE6 Reference Carrier Board

2.5. LAN

- Integrated: MAC integrated on SoC
- Intel PHY: Intel® Ethernet Controller i218LM
- Interface: 10/100/1000 GbE connection

2.6. Multi I/O and Storage

- I/O Hub: Integrated on SOC
- USB: 2x USB 3.0 ports (USB0,1) and 6x USB 2.0 ports (USB2,3,4,5,6,7)
- SATA: 4x SATA 6Gb/s ports
- GPIO: 4 GPO and 4 GPI

2.7. Serial I/O on Module

- Chipset: Nuvoton NCT5104D
- Ports: 2x UARTs Rx/Tx only
- Console Redirection: selectable in BIOS, supported during BIOS POST

COM Port	Description	IRQ	Address	Console redirection support
COM 1	Supported by module (SER0, A98/A99) via NCT5104D	10	0x240	Yes
COM 2	Supported by module (SER1, A101/A102) via NCT5104D	11	0x248	Yes
COM 3	Supported by Super I/O (W83627DHG) on carrier board	4	0x3F8	Yes
COM 4	Supported by Super I/O (W83627DHG) on carrier board	3	0x2F8	Yes

2.8. Trusted Platform Module (TPM)

- Chipset: Atmel AT97SC3204
- Type: TPM 1.2

2.9. SEMA Board Controller

- Type: ADLINK Smart Embedded Management Agent (SEMA)
- Functions:
  - Voltage/Current monitoring
  - Power sequence debug support
  - AT/ATX mode control
  - Logistics and forensic information
  - Flat panel control
  - General purpose I2C
  - Failsafe BIOS (dual BIOS)
  - Watchdog timer and fan control

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2.10. Debug

- 40-pin flat cable connector to be used with DB-40 debug module
  Supports: BIOS POST code LED, BMC access, SPI BIOS flashing, power testpoints, debug LEDs
- 60-pin XDP header for ICE debug of CPU/chipset

2.11. Power Specifications

- Power Modes: AT and ATX mode (AT mode startup controlled by SEMA Board Controller)
- Standard Voltage Input: ATX = 12V±5% / 5Vsb ±5% or AT = 12V±5%
- Wide Voltage Input: ATX = 5~20 V / 5Vsb ±5% or AT = 5 ~20V
- Power Management: ACPI 5.0 compliant, Smart Battery support
- Power States: supports C1-C6, S0, S3, S4, S5 (Wake-on-USB S3/S4, WoL S3/S4/S5)
- ECO mode: supports deep S5 for 5Vsb power saving

2.12. Operating Temperatures

- Standard Operating Temperature: 0°C to +60°C (Wide Voltage Input)
- Extreme Rugged™ Operating Temperature (optional): -40°C to +85°C (Standard Voltage Input)

2.13. Environmental

- Humidity: 5-90% RH operating, non-condensing
  5-95% RH storage (and operating with conformal coating).
- Shock and Vibration: IEC 60068-2-64 and IEC-60068-2-27
  MIL-STD-202F, Method 213B, Table 213-I, Condition A and Method 214A, Table 214-I, Condition D
- HALT: Thermal Stress, Vibration Stress, Thermal Shock and Combined Test

2.14. Specification Compliance

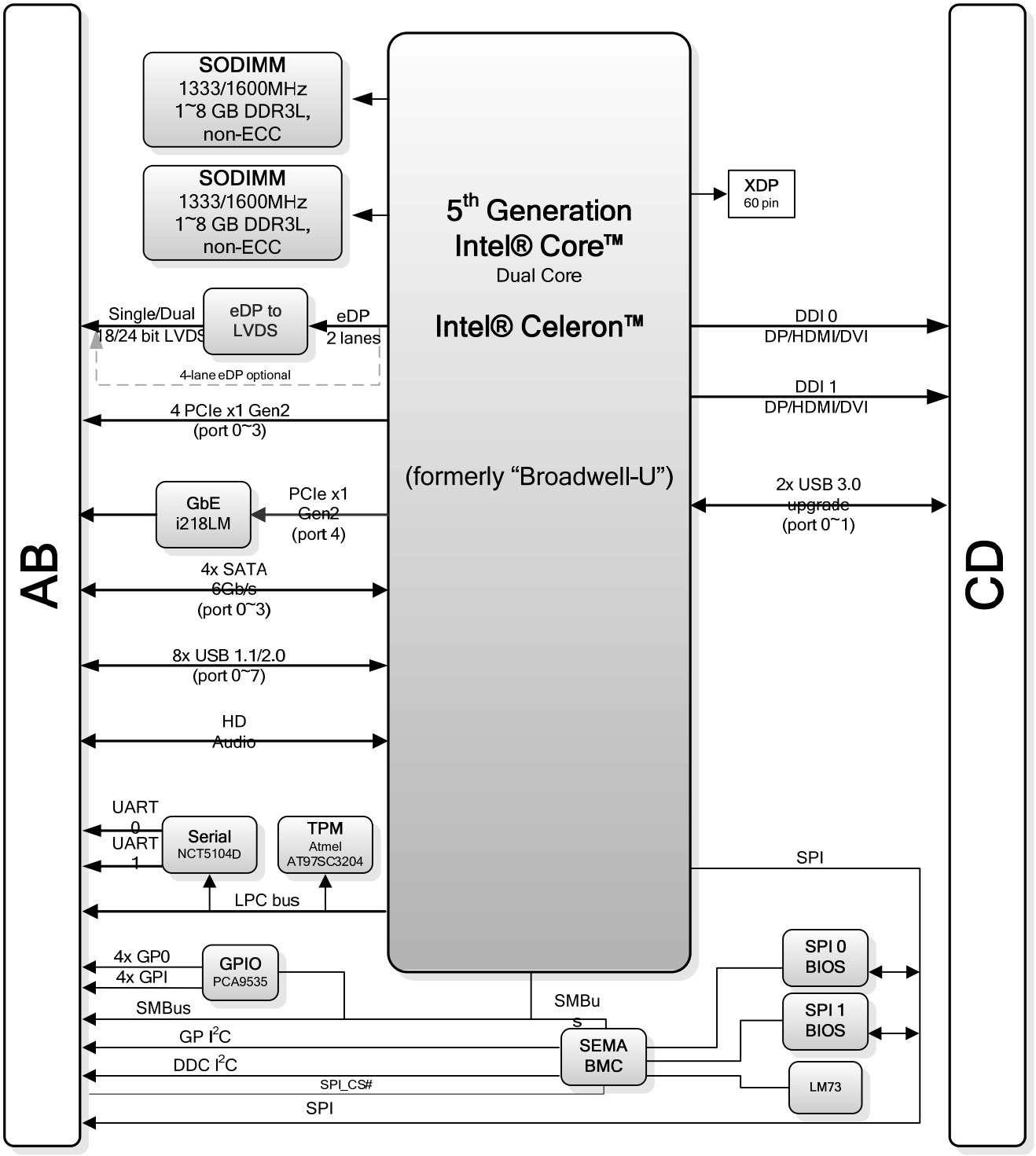
- PICMG COM.0: Rev 2.1 Type 6, Compact size 95 x 95 mm

2.15. Operating Systems

- Standard Support: Windows 7/8.1u 32/64-bit, Linux 32/64-bit
- Extended Support (BSP): Windows Embedded Standard 7 (WES7), Windows Embedded 8 Standard (WE8S), Linux, VxWorks

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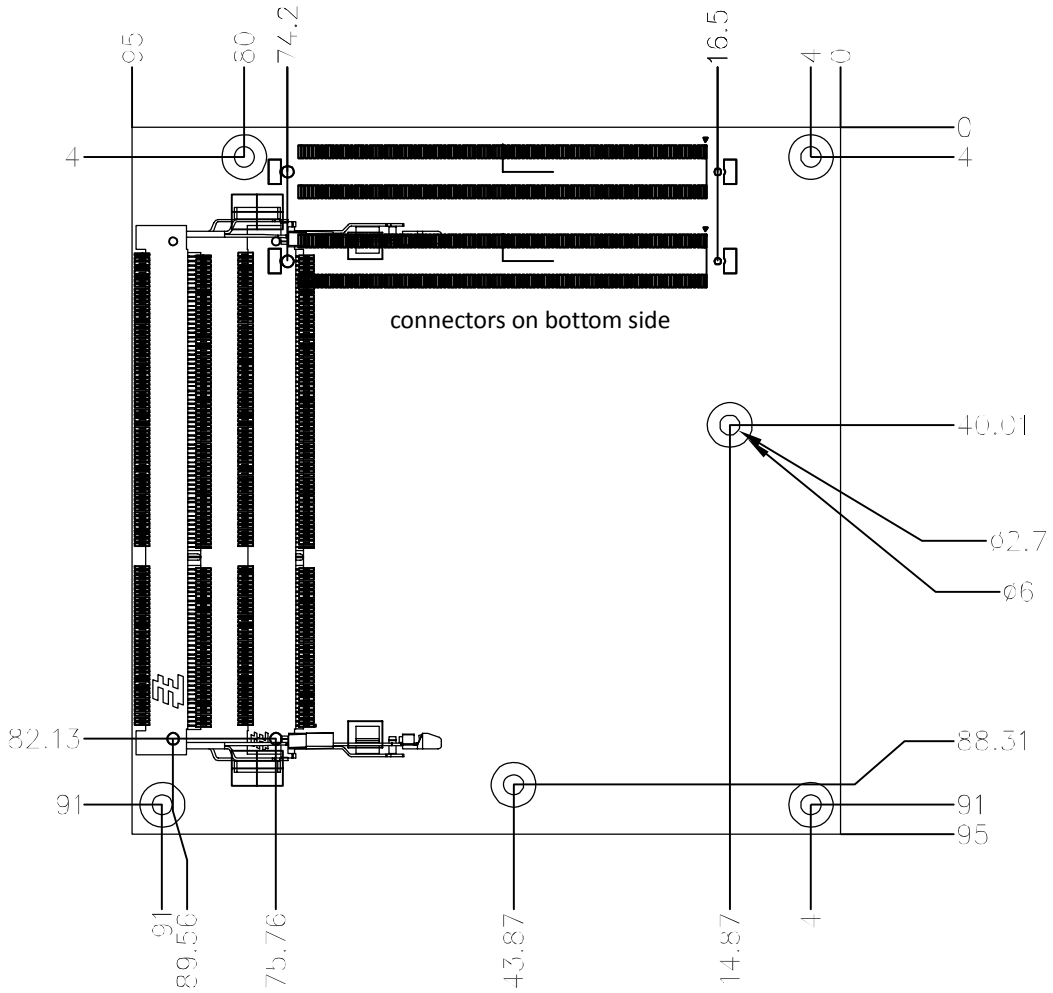
2.16. Functional Diagram



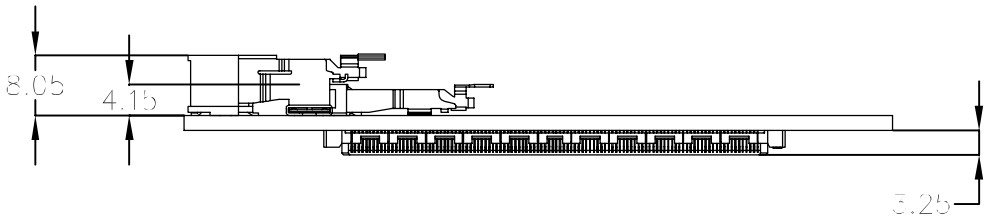
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2.17. Mechanical Drawing

Top View



Side View



All tolerances ± 0.05 mm
Other tolerances ± 0.2 mm

Dimensions: mm

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3. Pinouts and Signal Descriptions

3.1. AB/CD Pin Definitions

The cExpress-BL is a Type 6 module supporting USB 3.0 upgrade signals and DDI channels on the CD connector

All pins in the COM Express specification are described, including those not supported on the cExpress-BL. Those not supported on the cExpress-BL module are ~~crossed out~~.

	Row A		Row B		Row C		Row D
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**
A1	GND (FIXED)	**B1**	GND (FIXED)	**C1**	GND FIXED)	**D1**	GND FIXED)
A2	GBE0_MDI3-	**B2**	GBE0_ACT#	**C2**	GND	**D2**	GND
A3	GBE0_MDI3+	**B3**	LPC_FRAME#	**C3**	USB_SSRX0-	**D3**	USB_SSTX0-
A4	GBE0_LINK100#	**B4**	LPC_AD0	**C4**	USB_SSRX0+	**D4**	USB_SSTX0+
A5	GBE0_LINK1000#	**B5**	LPC_AD1	**C5**	GND	**D5**	GND
A6	GBE0_MDI2-	**B6**	LPC_AD2	**C6**	USB_SSRX1-	**D6**	USB_SSTX1-
A7	GBE0_MDI2+	**B7**	LPC_AD3	**C7**	USB_SSRX1+	**D7**	USB_SSTX1+
A8	GBE0_LINK#	**B8**	LPC_DRQ0#	**C8**	GND	**D8**	GND
A9	GBE0_MDI1-	**B9**	LPC_DRQ1#	**C9**	~~USB_SSRX2-~~	**D9**	~~USB_SSTX2-~~
A10	GBE0_MDI1+	**B10**	LPC_CLK	**C10**	~~USB_SSRX2+~~	**D10**	~~USB_SSTX2+~~
A11	GND (FIXED)	**B11**	GND (FIXED)	**C11**	GND (FIXED)	**D11**	GND (FIXED)
A12	GBE0_MDI0-	**B12**	PWRBTN#	**C12**	~~USB_SSRX3-~~	**D12**	~~USB_SSTX3-~~
A13	GBE0_MDI0+	**B13**	SMB_CK	**C13**	~~USB_SSRX3+~~	**D13**	~~USB_SSTX3+~~
A14	~~GBE0_CTREF~~	**B14**	SMB_DAT	**C14**	GND	**D14**	GND
A15	SUS_S3#	**B15**	SMB_ALERT#	**C15**	~~DDI1_PAIR6+~~	**D15**	DDI1_CTRLCLK_AUX+
A16	SATA0_TX+	**B16**	SATA1_TX+	**C16**	~~DDI1_PAIR6-~~	**D16**	DDI1_CTRLDATA_AUX
A17	SATA0_TX-	**B17**	SATA1_TX-	**C17**	RSVD	**D17**	RSVD
A18	SUS_S4#	**B18**	SUS_STAT#	**C18**	RSVD	**D18**	RSVD
A19	SATA0_RX+	**B19**	SATA1_RX+	**C19**	~~PCIE_RX6+~~	**D19**	~~PCIE_TX6+~~
A20	SATA0_RX-	**B20**	SATA1_RX-	**C20**	~~PCIE_RX6-~~	**D20**	~~PCIE_TX6-~~
A21	GND (FIXED)	**B21**	GND (FIXED)	**C21**	GND (FIXED)	**D21**	GND (FIXED)
A22	SATA2_TX+	**B22**	SATA3_TX+	**C22**	~~PCIE_RX7+~~	**D22**	~~PCIE_TX7+~~
A23	SATA2_TX-	**B23**	SATA3_TX-	**C23**	~~PCIE_RX7-~~	**D23**	~~PCIE_TX7-~~
A24	SUS_S5#	**B24**	PWR_OK	**C24**	DDI1_HPD	**D24**	RSVD
A25	SATA2_RX+	**B25**	SATA3_RX+	**C25**	~~DDI1_PAIR4+~~	**D25**	RSVD
A26	SATA2_RX-	**B26**	SATA3_RX-	**C26**	~~DDI1_PAIR4-~~	**D26**	DDI1_PAIR0+
A27	BATLOW#	**B27**	WDT	**C27**	RSVD	**D27**	DDI1_PAIR0-
A28	(S)ATA_ACT#	**B28**	~~AC/HDA_SDIN2~~	**C28**	RSVD	**D28**	RSVD
A29	AC/HDA_SYNC	**B29**	AC/HDA_SDIN1	**C29**	~~DDI1_PAIR5+~~	**D29**	DDI1_PAIR1+
A30	AC/HDA_RST#	**B30**	AC/HDA_SDIN0	**C30**	~~DDI1_PAIR5-~~	**D30**	DDI1_PAIR1-
A31	GND (FIXED)	**B31**	GND (FIXED)	**C31**	GND (FIXED)	**D31**	GND (FIXED)
A32	AC/HDA_BITCLK	**B32**	SPKR	**C32**	DDI2_CTRLCLK_AUX+	**D32**	DDI1_PAIR2+
A33	AC/HDA_SDOUT	**B33**	I2C_CK	**C33**	DDI2_CTRLDATA_AUX-	**D33**	DDI1_PAIR2-
A34	BIOS_DIS0#	**B34**	I2C_DAT	**C34**	DDI2_DDC_AUX_SEL	**D34**	DDI1_DDC_AUX_SEL
A35	THRMTRIP#	**B35**	THRM#	**C35**	RSVD	**D35**	RSVD

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	Row A		Row B		Row C		Row D
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**
A36	USB6-	**B36**	USB7-	**C36**	~~DDI3_CTRLCLK_AUX+~~	**D36**	DDI1_PAIR3+
A37	USB6+	**B37**	USB7+	**C37**	~~DDI3_CTRLDATA_AUX-~~	**D37**	DDI1_PAIR3-
A38	USB_6_7_OC#	**B38**	USB_4_5_OC#	**C38**	~~DDI3_DDC_AUX_SEL~~	**D38**	RSVD
A39	USB4-	**B39**	USB5-	**C39**	~~DDI3_PAIR0+~~	**D39**	DDI2_PAIR0+
A40	USB4+	**B40**	USB5+	**C40**	~~DDI3_PAIR0-~~	**D40**	DDI2_PAIR0-
A41	GND (FIXED)	**B41**	GND (FIXED)	**C41**	GND (FIXED)	**D41**	GND (FIXED)
A42	USB2-	**B42**	USB3-	**C42**	~~DDI3_PAIR1+~~	**D42**	DDI2_PAIR1+
A43	USB2+	**B43**	USB3+	**C43**	~~DDI3_PAIR1-~~	**D43**	DDI2_PAIR1-
A44	USB_2_3_OC#	**B44**	USB_0_1_OC#	**C44**	~~DDI3_HPD~~	**D44**	DDI2_HPD
A45	USB0-	**B45**	USB1-	**C45**	RSVD	**D45**	RSVD
A46	USB0+	**B46**	USB1+	**C46**	~~DDI3_PAIR2+~~	**D46**	DDI2_PAIR2+
A47	VCC_RTC	**B47**	EXCD1_PERST#	**C47**	~~DDI3_PAIR2-~~	**D47**	DDI2_PAIR2-
A48	EXCD0_PERST#	**B48**	EXCD1_CPPE#	**C48**	RSVD	**D48**	RSVD
A49	EXCD0_CPPE#	**B49**	SYS_RESET#	**C49**	~~DDI3_PAIR3+~~	**D49**	DDI2_PAIR3+
A50	LPC_SERIRQ	**B50**	CB_RESET#	**C50**	~~DDI3_PAIR3-~~	**D50**	DDI2_PAIR3-
A51	GND (FIXED)	**B51**	GND (FIXED)	**C51**	GND (FIXED)	**D51**	GND (FIXED)
A52	~~PCIE_TX5+~~	**B52**	~~PCIE_RX5+~~	**C52**	~~PEG_RX0+~~	**D52**	~~PEG_TX0+~~
A53	~~PCIE_TX5-~~	**B53**	~~PCIE_RX5-~~	**C53**	~~PEG_RX0-~~	**D53**	~~PEG_TX0-~~
A54	GPI0	**B54**	GPO1	**C54**	TYPE0#	**D54**	PEG_LANE_RV#
A55	~~PCIE_TX4+~~	**B55**	~~PCIE_RX4+~~	**C55**	~~PEG_RX1+~~	**D55**	~~PEG_TX1+~~
A56	~~PCIE_TX4-~~	**B56**	~~PCIE_RX4-~~	**C56**	~~PEG_RX1-~~	**D56**	~~PEG_TX1-~~
A57	GND	**B57**	GPO2	**C57**	TYPE1#	**D57**	TYPE2#
A58	PCIE_TX3+	**B58**	PCIE_RX3+	**C58**	~~PEG_RX2+~~	**D58**	~~PEG_TX2+~~
A59	PCIE_TX3-	**B59**	PCIE_RX3-	**C59**	~~PEG_RX2-~~	**D59**	~~PEG_TX2-~~
A60	GND (FIXED)	**B60**	GND (FIXED)	**C60**	GND (FIXED)	**D60**	GND (FIXED)
A61	PCIE_TX2+	**B61**	PCIE_RX2+	**C61**	~~PEG_RX3+~~	**D61**	~~PEG_TX3+~~
A62	PCIE_TX2-	**B62**	PCIE_RX2-	**C62**	~~PEG_RX3-~~	**D62**	~~PEG_TX3-~~
A63	GPI1	**B63**	GPO3	**C63**	RSVD	**D63**	RSVD
A64	PCIE_TX1+	**B64**	PCIE_RX1+	**C64**	RSVD	**D64**	RSVD
A65	PCIE_TX1-	**B65**	PCIE_RX1-	**C65**	~~PEG_RX4+~~	**D65**	~~PEG_TX4+~~
A66	GND	**B66**	WAKE0#	**C66**	~~PEG_RX4-~~	**D66**	~~PEG_TX4-~~
A67	GPI2	**B67**	WAKE1#	**C67**	RSVD	**D67**	GND
A68	PCIE_TX0+	**B68**	PCIE_RX0+	**C68**	~~PEG_RX5+~~	**D68**	~~PEG_TX5+~~
A69	PCIE_TX0-	**B69**	PCIE_RX0-	**C69**	~~PEG_RX5-~~	**D69**	~~PEG_TX5-~~
A70	GND (FIXED)	**B70**	GND (FIXED)	**C70**	GND (FIXED)	**D70**	GND (FIXED)
A71	LVDS_A0+ (eDP_TX2+)*	**B71**	LVDS_B0+	**C71**	~~PEG_RX6+~~	**D71**	~~PEG_TX6+~~
A72	LVDS_A0- (eDP_TX2+)*	**B72**	LVDS_B0-	**C72**	~~PEG_RX6-~~	**D72**	~~PEG_TX6-~~
A73	LVDS_A1+ (eDP_TX1+)*	**B73**	LVDS_B1+	**C73**	GND	**D73**	GND
A74	LVDS_A1- (eDP_TX1-)*	**B74**	LVDS_B1-	**C74**	~~PEG_RX7+~~	**D74**	~~PEG_TX7+~~
A75	LVDS_A2+ (eDP_TX0+)*	**B75**	LVDS_B2+	**C75**	~~PEG_RX7-~~	**D75**	~~PEG_TX7-~~
A76	LVDS_A2- (eDP_TX0-)*	**B76**	LVDS_B2-	**C76**	GND	**D76**	GND
A77	LVDS_VDD_EN (eDP_VDD_EN)*	**B77**	LVDS_B3+	**C77**	RSVD	**D77**	RSVD
A78	LVDS_A3+	**B78**	LVDS_B3-	**C78**	~~PEG_RX8+~~	**D78**	~~PEG_TX8+~~
A79	LVDS_A3-	**B79**	LVDS_BKLT_EN (eDP_BKLT_EN)*	**C79**	~~PEG_RX8-~~	**D79**	~~PEG_TX8-~~

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	Row A		Row B		Row C		Row D
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**
A80	GND (FIXED)	**B80**	GND (FIXED)	**C80**	GND (FIXED)	**D80**	GND (FIXED)
A81	LVDS_A_CK+ (eDP_TX3+)	**B81**	LVDS_B_CK+	**C81**	~~PEG_RX9+~~	**D81**	~~PEG_TX9+~~
A82	LVDS_A_CK- (eDP_TX3-)	**B82**	LVDS_B_CK-	**C82**	~~PEG_RX9-~~	**D82**	~~PEG_TX9-~~
A83	LVDS_I2C_CK /eDP_AUX+ *	**B83**	LVDS_BKLT_CTRL /eDP_BKLT_CTRL *	**C83**	RSVD	**D83**	RSVD
A84	LVDS_I2C_DAT /eDP_AUX- *	**B84**	VCC_5V_SBY	**C84**	GND	**D84**	GND
A85	GPI3	**B85**	VCC_5V_SBY	**C85**	~~PEG_RX10+~~	**D85**	~~PEG_TX10+~~
A86	RSVD	**B86**	VCC_5V_SBY	**C86**	~~PEG_RX10-~~	**D86**	~~PEG_TX10-~~
A87	RSVD /eDP_HPD *	**B87**	VCC_5V_SBY	**C87**	GND	**D87**	GND
A88	PCIE0_CK_REF+	**B88**	BIOS_DIS1#	**C88**	~~PEG_RX11+~~	**D88**	~~PEG_TX11+~~
A89	PCIE0_CK_REF-	**B89**	~~VGA_RED~~	**C89**	~~PEG_RX11-~~	**D89**	~~PEG_TX11-~~
A90	GND (FIXED)	**B90**	GND (FIXED)	**C90**	GND (FIXED)	**D90**	GND (FIXED)
A91	SPI_POWER	**B91**	~~VGA_GRN~~	**C91**	~~PEG_RX12+~~	**D91**	~~PEG_TX12+~~
A92	SPI_MISO	**B92**	~~VGA_BLU~~	**C92**	~~PEG_RX12-~~	**D92**	~~PEG_TX12-~~
A93	GPO0	**B93**	~~VGA_HSYNC~~	**C93**	GND	**D93**	GND
A94	SPI_CLK	**B94**	~~VGA_VSYNC~~	**C94**	~~PEG_RX13+~~	**D94**	~~PEG_TX13+~~
A95	SPI_MOSI	**B95**	~~VGA_I2C_CK~~	**C95**	~~PEG_RX13-~~	**D95**	~~PEG_TX13-~~
A96	TPM_PP	**B96**	~~VGA_I2C_DAT~~	**C96**	GND	**D96**	GND
A97	TYPE10#	**B97**	SPI_CS#	**C97**	RSVD	**D97**	RSVD
A98	SER0_TX	**B98**	RSVD	**C98**	~~PEG_RX14+~~	**D98**	~~PEG_TX14+~~
A99	SER0_RX	**B99**	RSVD	**C99**	~~PEG_RX14-~~	**D99**	~~PEG_TX14-~~
A100	GND (FIXED)	**B100**	GND (FIXED)	**C100**	GND (FIXED)	**D100**	GND (FIXED)
A101	SER1_TX	**B101**	FAN_PWMOUT	**C101**	~~PEG_RX15+~~	**D101**	~~PEG_TX15+~~
A102	SER1_RX	**B102**	FAN_TACHIN	**C102**	~~PEG_RX15-~~	**D102**	~~PEG_TX15-~~
A103	LID#	**B103**	SLEEP#	**C103**	GND	**D103**	GND
A104	VCC_12V	**B104**	VCC_12V	**C104**	VCC_12V	**D104**	VCC_12V
A105	VCC_12V	**B105**	VCC_12V	**C105**	VCC_12V	**D105**	VCC_12V
A106	VCC_12V	**B106**	VCC_12V	**C106**	VCC_12V	**D106**	VCC_12V
A107	VCC_12V	**B107**	VCC_12V	**C107**	VCC_12V	**D107**	VCC_12V
A108	VCC_12V	**B108**	VCC_12V	**C108**	VCC_12V	**D108**	VCC_12V
A109	VCC_12V	**B109**	VCC_12V	**C109**	VCC_12V	**D109**	VCC_12V
A110	GND (FIXED)	**B110**	GND (FIXED)	**C110**	GND (FIXED)	**D110**	GND (FIXED)

*Note: eDP is available as BOM option in place of LVDS.

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3.2. Signal Description Terminology

The following terms are used in the COM Express AB/CD Signal Descriptions below.

I	Input to the Module
O	Output from the Module
I/O	Bi-directional input/output signal
OD	Open drain output
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I/O 3.3Vsb	Input 3.3V tolerant active in standby state
P	Power Input/Output
REF	Reference voltage output that may be sourced from a module power plane.
PDS	Pull-down strap. This is an output pin on the module that is either tied to GND or not connected. The signal is used to indicate the PICMG module type to the Carrier Board.
PU	ADLINK implemented pull-up resistor on module
PD	ADLINK implemented pull-down resistor on module

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3.3. AB Signal Descriptions

3.3.1. Audio Signals

Signal	Pin #	Description	I/O	PU/PD	Comment
AC_RST# / HDA_RST#	A30	Reset output to codec, active low.	O 3.3VSB		VSB because PCH uses suspend power for RESET
AC_SYNC / HDA_SYNC	A29	Sample-synchronization signal to the codec(s).	O 3.3V		
AC_BITCLK / HDA_BITCLK	A32	Serial data clock generated by the external codec(s).	I/O 3.3V		
AC _SDOUT / HDA_SDOUT	A33	Serial TDM data output to the codec.	O 3.3V		
AC _SDIN[2:0] HDA_SDIN[2:0]	B28 B29 B30	Serial TDM data inputs from up to 3 codecs.	I/O 3.3VSB	PD 1M	No AC/HDA_SDIN 2 (B28) support on this platform

3.3.2. Analog VGA

Signal	Pin #	Description	I/O	PU/PD	Comment
VGA_RED	B89	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog		Not supported
VGA_GRN	B91	Green for monitor Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog		Not supported
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog		Not supported
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3V		Not supported
VGA_VSYNC	B94	Vertical sync output to VGA monitor	O 3.3V		Not supported
VGA_I2C_CK	B95	DDC clock line (I²C port dedicated to identify VGA monitor capabilities)	I/O OD 3.3V		Not supported
VGA_I2C_DAT	B96	DDC data line.	I/O OD 3.3V		Not supported

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3.3.3. LVDS/eDP

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- - LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		LVDS is default. (through eDP to LVDS bridge) Note: eDP support is a BOM option
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS Channel A differential clock	O LVDS		
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	B71 B72 B73 B74 B75 B76 B77 B78	LVDS Channel B differential pairs	O LVDS		
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS Channel B differential clock	O LVDS		
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 100K	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V	PD 100K	
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V		ePD to LVDS requirement
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control.	O 3.3V	PU 2k2 3.3V	
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 2k2 3.3V	

eDP BOM Option Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
eDP_TX2+ eDP_TX2- eDP_TX1+ eDP_TX1- eDP_TX0+ eDP_TX0--	A71 A72 A73 A74 A75 A76	eDP differential pairs	O PCIE		AC coupled off module
eDP_TX3+ eDP_TX3--	A81 A82	eDP differential pairs	O PCIE		AC coupled off module
eDP_VDD_EN	A77	eDP power enable	O 3.3V	PD 100K	
eDP_BKLT_EN	B79	eDP backlight enable	O 3.3V	PD 100K	
eDP_BKLT_CTRL	B83	eDP backlight brightness control	O 3.3V		
eDP_AUX+	A83	eDP AUX+	I/O PCIE		AC coupled off module
eDP_AUX-	A84	eDP AUX-	I/O PCIE		AC coupled off module
eDP_HPD	A87	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V		

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3.3.4. Gigabit Ethernet

Gigabit Ethernet	Pin #	Description	I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: 1000BASE-T / 100BASE-TX / 10BASE-T MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	I/O Analog		Twisted pair signals for external transformer.
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.	O 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.	O 3.3VSB		
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.	O 3.3VSB		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	O 3.3VSB		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 1 and 2 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be 250 mA or less.	GND min 3.3V max		No support on this product

3.3.5. Serial ATA

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		AC coupled on Module
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		AC coupled on Module
SATA2_TX+ SATA2_TX-	A22 A23	Serial ATA channel 2, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA2_RX+ SATA2_RX-	A25 A26	Serial ATA channel 2, Receive Input differential pair.	I SATA		AC coupled on Module
SATA3_TX+ SATA3_TX-	B22 B23	Serial ATA channel 3, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA3_RX+ SATA3_RX-	B25 B26	Serial ATA channel 3, Receive Input differential pair.	I SATA		AC coupled on Module
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	O 3.3V	PU 10K 3.3V	

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3.3.6. PCI Express

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		PCIe port 4 is Connected to LAN
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		PCIe port 4 is Connected to LAN
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		Not supported
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		

3.3.7. Express Card

Signal	Pin #	Description	I/O	PU/PD	Comment
EXCD0_CPPE# EXCD1_CPPE#	A49 B48	PCI ExpressCard: PCI Express capable card request	I 3.3V	PU 10k 3.3V	
EXCD0_PERST# EXCD1_PERST#	A48 B47	PCI ExpressCard: reset	O 3.3V		

3.3.8. LPC Bus

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V		
LPC_DRQ0# LPC_DRQ1#	B8 B9	LPC serial DMA request	I 3.3V		
LPC_SERIRQ	A50	LPC serial interrupt	I/O OD 3.3V	PU 8k2 3.3V	
LPC_CLK	B10	LPC clock output - 33MHz nominal	O 3.3V		

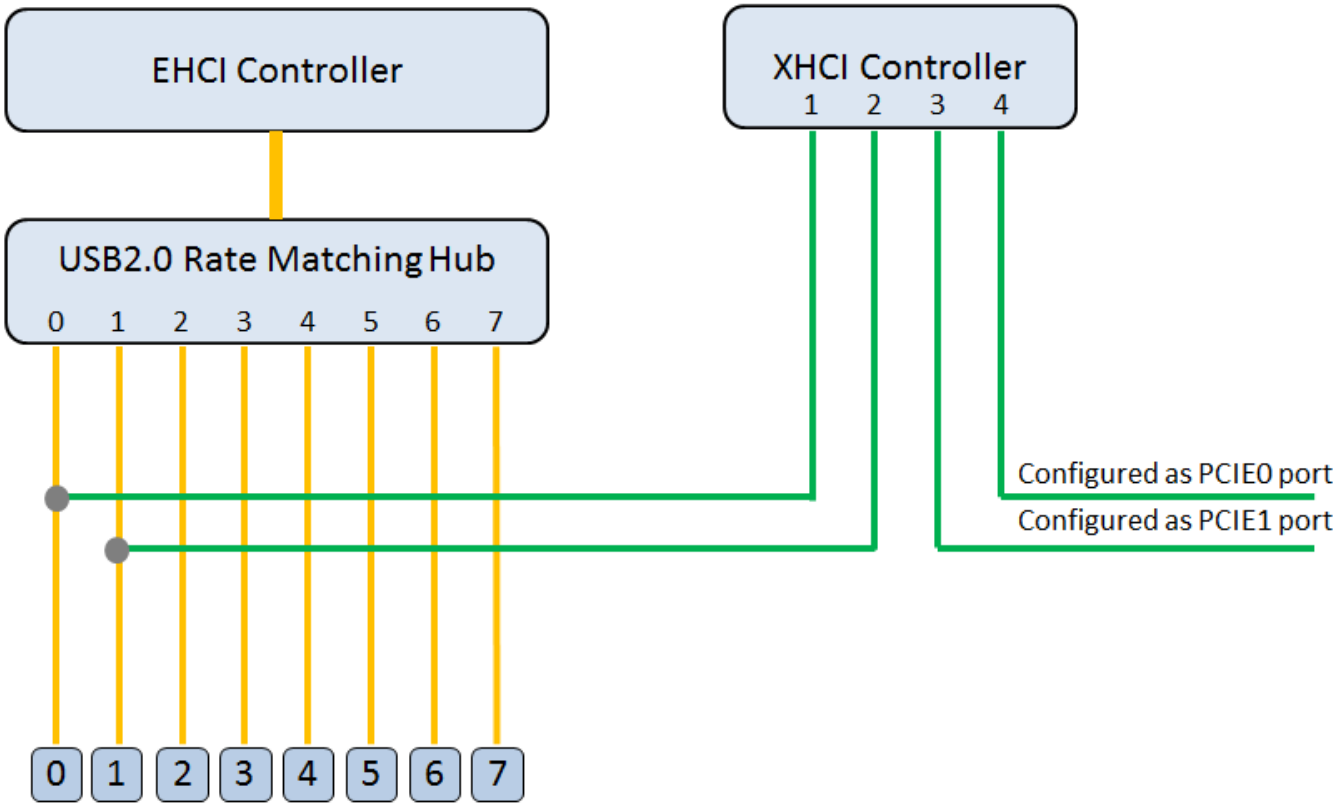
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3.3.9. USB

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+ USB0-	A46 A45	USB differential data pairs for Port 0	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB1+ USB1-	B46 B45	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB2+ USB2-	A43 A42	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB3+ USB3-	B43 B42	USB differential data pairs for Port 2	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB4+ USB4-	A40 A39	USB differential data pairs for Port 3	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB5+ USB5-	B40 B39	USB differential data pairs for Port 4	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB6+ USB6-	A37 A36	USB differential data pairs for Port 5	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB7+ USB7-	B37 B37	USB differential data pairs for Port 6	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull high on carrier
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3VSB	PU 10k 3.3VSB	Do not pull high on carrier
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull high on carrier
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull high on carrier

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3.3.10. USB Root Segmentation



3.3.11. SPI (BIOS only)

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3VSB	PU 10K 3.3VSB	
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier	O P 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I	PU 10K 3.3VSB	Carrier shall pull to GND or leave no-connect.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I	PU 10K 3.3VSB	Carrier shall pull to GND or leave no-connect

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3.3.12. Miscellaneous

Signal	Pin #	Description	I/O	PU/PD	Comment
SPKR	B32	Output for audio enunciator, the “speaker” in PC-AT systems	O 3.3V		
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V		
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3V		
THERMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3V	PU 330 ohm 3.3V	
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan’s RPM.	O OD 3.3V	PU 2.2K 3.3V	
FAN_TACHIN11	B102	Fan tachometer input for a fan with a two pulse output.	I OD 3.3V	PU 10k 3.3V	
TPM_PP11	C83	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V	PD 10k 3.3V	PD is only placed when TPM is installed on module

3.3.13. SMBus

Signal	Pin #	Description	I/O	PU/PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line. Power sourced through 5V standby rail and main power rails.	I/O OD 3.3VSB	PU 8k2 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line. Power sourced through 5V standby rail and main power rails.	I/O OD 3.3VSB	PU 8k2 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 5V standby rail and main power rails.	I 3.3VSB	PU 10k 3.3VSB	

3.3.14. I2C Bus

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output/input	I/O OD 3.3VSB	PU 2k2 3.3VSB	
I2C_DAT	B34	General purpose I²C port data I/O line	I/O OD 3.3VSB	PU 2k2 3.3VSB	

3.3.15. General Purpose I/O (GPIO)

Signal	Pin #	Description	I/O	PU/PD	Comment
GPO[0]	A93	General purpose output pins.	O 3.3V	PU 10K 3.3V	After hardware RESET output low
GPO[1]	B54	General purpose output pins.	O 3.3V	PU 10K 3.3V	After hardware RESET output low
GPO[2]	B57	General purpose output pins.	O 3.3V	PU 10K 3.3V	After hardware RESET output low

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Signal	Pin #	Description	I/O	PU/PD	Comment
GPO[3]	B63	General purpose output pins.	O 3.3V	PU 10K 3.3V	After hardware RESET output low
GPI[0]	A54	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[1]	A63	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[2]	A67	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[3]	A85	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	

3.3.16. Serial Interface Signals

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX	A98	General purpose serial port transmitter (TTL level output)	O CMOS		Power rail tolerance 5V/12V
SER0_RX	A99	General purpose serial port receiver (TTL level input)	I CMOS		Power rail tolerance 5V/12V
SER1_TX	A101	General purpose serial port transmitter (TTL level output)	O CMOS		Power rail tolerance 5V/12V
SER1_RX	A102	General purpose serial port receiver (TTL level input)	I CMOS		Power rail tolerance 5V/12V

3.3.17. Power and System Management

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge.	I 3.3VSB	PU 10k 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low request for module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.	I 3.3VSB	PU 10k 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3VSB		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow carrier based FPGAs or other configurable devices time to be programmed.	I 3.3V	PU 100k 3.3VSB	
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as “PS_ON”) may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB		
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 10k 3.3VSB	Not supported connected to WAKE1#
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 10k 3.3VSB	

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Signal	Pin #	Description	I/O	PU/PD	Comment
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I 3.3VSB	PU 10k 3.3VSB	
LID#		LID button. Low active signal used by the ACPI operating system for a LID switch.	I OD 3.3VSB	PU 10k 3.3VSB	Emulated on GPIO (BIOS)
SLEEP#		Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I OD 3.3VSB	PU 10K 3.3VSB	Emulated on GPIO (BIOS)

3.3.18. Power and Ground

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109	Primary power input: +12V nominal (5 ~ 20V wide input). All available VCC_12V pins on the connector(s) shall be used.	P		5~20 V
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		5Vsb ±5%
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A66, A80, A90, A96, A100, A110, B1, B11, B21 ,B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path.	P		

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3.4. CD Signal Descriptions

3.4.1. USB 3.0 extension

Signal	Pin	Description	I/O	PU/PD	Comment
USB_SSRX0- USB_SSRX0+	C3 C4	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB0	I PCIE		
USB_SSTX0- USB_SSTX0+	D3 D4	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB0	O PCIE		AC coupled on Module
USB_SSRX1- USB_SSRX1+	C6 C7	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB1	I PCIE		
USB_SSTX1- USB_SSTX1+	D6 D7	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB1	O PCIE		AC coupled on Module
USB_SSRX2- USB_SSRX2+	C9 C10	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB2	I PCIE		Not supported
USB_SSTX2- USB_SSTX2+	D9 D10	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB2	O PCIE		Not supported
USB_SSRX3- USB_SSRX3+	C12 C13	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB3	I PCIE		Not supported
USB_SSTX3- USB_SSTX3+	D12 D13	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB3	O PCIE		Not supported

3.4.2. PCI Express x1

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair.	I PCIE		Not supported
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair.	O PCIE		Not supported
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair.	I PCIE		Not supported

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3.4.3. DDI Channels

DDI 1

Signal	Pin	Description	I/O	PU/PD	Comment
DDI1_PAIR0+ DDI1_PAIR0- DDI1_PAIR1+ DDI1_PAIR1- DDI1_PAIR2+ DDI1_PAIR2- DDI1_PAIR3+ DDI1_PAIR3- DDI1_PAIR4+ DDI1_PAIR4- DDI1_PAIR5+ DDI1_PAIR5- DDI1_PAIR6+ DDI1_PAIR6-	D26 D27 D29 D30 D32 D33 D36 D37 C25 C26 C29 C30 C15 C16	Digital Display Interface1 differential pairs	O PCIE		 Pair 4 to Pair 6 Not supported
DDI1_HPD	C24	Digital Display Interface Hot-Plug Detect	I PCIE	PD 10M	
DDI1_CTRLCLK_AUX+	D15	IF DDI1_DDC_AUX_SEL is floating	I/O PCIe		DP1_AUX+
		IF DDI1_DDC_AUX_SEL pulled high	I/O OD 3.3V		HDMI1_CTRLCLK
DDI1_CTRLCLK_AUX-	D16	IF DDI1_DDC_AUX_SEL is floating	I/O PCIe		DP1_AUX+
		IF DDI1_DDC_AUX_SEL pulled high	I/O OD 3.3V		HDMI1_CTRLDATA
DDI1_DDC_AUX_SEL	D34	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.	I/O OD 3.3V	PD 1M	

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DDI 2

Signal	Pin	Description	I/O	PU/PD	Comment
DDI2_PAIR0+ DDI2_PAIR0- DDI2_PAIR1+ DDI2_PAIR1- DDI2_PAIR2+ DDI2_PAIR2- DDI2_PAIR3+ DDI2_PAIR3-	D39 D40 D42 D43 D46 D47 D49 D50	Digital Display Interface2 differential pairs			
DDI2_HPD	D44			PD 10M	
DDI2_CTRLCLK_AUX+	C32	IF DDI2_DDC_AUX_SEL is floating	I/O PCIe		DP2_AUX+
		IF DDI2_DDC_AUX_SEL pulled high	I/O OD 3.3V		HDMI2_CTRLCLK
DDI2_CTRLCLK_AUX-	C33	IF DDI2_DDC_AUX_SEL is floating	I/O PCIe		DP2_AUX+
		IF DDI2_DDC_AUX_SEL pulled high	I/O OD 3.3V		HDMI2_CTRLDATA
DDI2_DDC_AUX_SEL	C34	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.		PD 1M	

DDI 3

Signal	Pin	Description	I/O	PU/PD	Comment
DDI3_PAIR0+ DDI3_PAIR0- DDI3_PAIR1+ DDI3_PAIR1- DDI3_PAIR2+ DDI3_PAIR2- DDI3_PAIR3+ DDI3_PAIR3-	C39 C40 C42 C43 C46 C47 C49 C50	Digital Display Interface3 differential pairs			Not supported
DDI3_HPD	C44				Not supported
DDI3_CTRLCLK_AUX+	C36	IF DDI3_DDC_AUX_SEL is floating	I/O PCIe		Not supported
		IF DDI3_DDC_AUX_SEL pulled high	I/O OD 3.3V		Not supported
DDI3_CTRLCLK_AUX-	C37	IF DDI3_DDC_AUX_SEL is floating	I/O PCIe		Not supported
		IF DDI3_DDC_AUX_SEL pulled high	I/O OD 3.3V		Not supported
DDI3_DDC_AUX_SEL	C38	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.		PD 1M	Not supported

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3.4.4. DDI to DP/HDMI/SDVO Mapping

Pin	Pin Name	DP	HDMI \ DVI
D26	DDI1_PAIR0+	DP1_LANE0+	TMDS1_DATA2+
D27	DDI1_PAIR0-	DP1_LANE0-	TMDS1_DATA2-
D29	DDI1_PAIR1+	DP1_LANE1+	TMDS1_DATA1+
D30	DDI1_PAIR1-	DP1_LANE1-	TMDS1_DATA1-
D32	DDI1_PAIR2+	DP1_LANE2+	TMDS1_DATA0+
D33	DDI1_PAIR2-	DP1_LANE2-	TMDS1_DATA0-
D36	DDI1_PAIR3+	DP1_LANE3+	TMDS1_CLK+
D37	DDI1_PAIR3-	DP1_LANE3-	TMDS1_CLK-
C25	DDI1_PAIR4+	Not supported	Not supported
C26	DDI1_PAIR4-	Not supported	Not supported
C29	DDI1_PAIR5+	Not supported	Not supported
C30	DDI1_PAIR5-	Not supported	Not supported
C15	DDI1_PAIR6+	Not supported	Not supported
C16	DDI1_PAIR6-	Not supported	Not supported
C24	DDI1_HPD	DP1_HPD	HDMI1_HPD
D15	DDI1_CTRLCLK_AUX+	DP1_AUX+	HMDI1_CTRLCLK
D16	DDI1_CTRLDATA_AUX-	DP1_AUX-	HMDI1_CTRLDATA
D34	DDI1_DDC_AUX_SEL		
D39	DDI2_PAIR0+	DP2_LANE0+	TMDS2_DATA2+
D40	DDI2_PAIR0-	DP2_LANE0-	TMDS2_DATA2-
D42	DDI2_PAIR1+	DP2_LANE1+	TMDS2_DATA1+
D43	DDI2_PAIR1-	DP2_LANE1-	TMDS2_DATA1-
D46	DDI2_PAIR2+	DP2_LANE2+	TMDS2_DATA0+
D47	DDI2_PAIR2-	DP2_LANE2-	TMDS2_DATA0-
D49	DDI2_PAIR3+	DP2_LANE3+	TMDS2_CLK+
D50	DDI2_PAIR3-	DP2_LANE3-	TMDS2_CLK-
D44	DDI2_HPD	DP2_HPD	HDMI2_HPD
C32	DDI2_CTRLCLK_AUX+	DP2_AUX+	HDMI2_CTRLCLK
C33	DDI2_CTRLDATA_AUX-	DP2_AUX-	HDMI2_CTRLDATA
C34	DDI2_DDC_AUX_SEL		

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3.4.5. PCI Express Graphics x16 (PEG)

Signal	Pin	Description	I/O	PU/PD	Comment
PEG_RX0+ PEG_RX0- PEG_RX1+ PEG_RX1- PEG_RX2+ PEG_RX2- PEG_RX3+ PEG_RX3- PEG_RX4+ PEG_RX4- PEG_RX5+ PEG_RX5- PEG_RX6+ PEG_RX6- PEG_RX7+ PEG_RX7- PEG_RX8+ PEG_RX8- PEG_RX9+ PEG_RX9- PEG_RX10+ PEG_RX10- PEG_RX11+ PEG_RX11- PEG_RX12+ PEG_RX12- PEG_RX13+ PEG_RX13- PEG_RX14+ PEG_RX14- PEG_RX15+ PEG_RX15	C52 C53 C55 C56 C58 C59 C61 C62 C65 C66 C68 C69 C71 C72 C74 C75 C78 C79 C81 C82 C85 C86 C88 C89 C91 C92 C94 C95 C98 C99 C101 C102	PCI Express Graphics transmit differential pairs.	I PCIE		Not supported
PEG_TX0+ PEG_TX0- PEG_TX1+ PEG_TX1- PEG_TX2+ PEG_TX2- PEG_TX3+ PEG_TX3- PEG_TX4+ PEG_TX4- PEG_TX5+ PEG_TX5- PEG_TX6+ PEG_TX6- PEG_TX7+ PEG_TX7- PEG_TX8+ PEG_TX8- PEG_TX9+ PEG_TX9- PEG_TX10+ PEG_TX10- PEG_TX11+ PEG_TX11- PEG_TX12+ PEG_TX12- PEG_TX13+ PEG_TX13- PEG_TX14+ PEG_TX14-	D52 D53 D55 D56 D58 D57 D61 D62 D65 D66 D68 D69 D71 D72 D74 D75 D78 D79 D81 D82 D85 D86 D88 D89 D91 D92 D94 D95 D98 D99	PCI Express Graphics receive differential pairs.	O PCIE		Not supported

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Signal	Pin	Description	I/O	PU/PD	Comment
PEG_TX15+ PEG_TX15-	D101 D102				
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the Carrier board to reverse lane order.	I 1.05V		Not supported

3.4.6. Module Type Definition

Signal	Pin #	Description	I/O	Comment
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pinout Type 1, these pins are don't care (X). TYPE2# TYPE1# TYPE0# X X X Pinout Type 1 NC NC NC Pinout Type 2 NC NC GND Pinout Type 3 (no IDE) NC GND NC Pinout Type 4 (no PCI) NC GND GND Pinout Type 5 (no IDE, no PCI) GND NC NC Pinout Type 6 (no IDE, no PCI) The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.		Type 6

3.4.7. Power and Ground

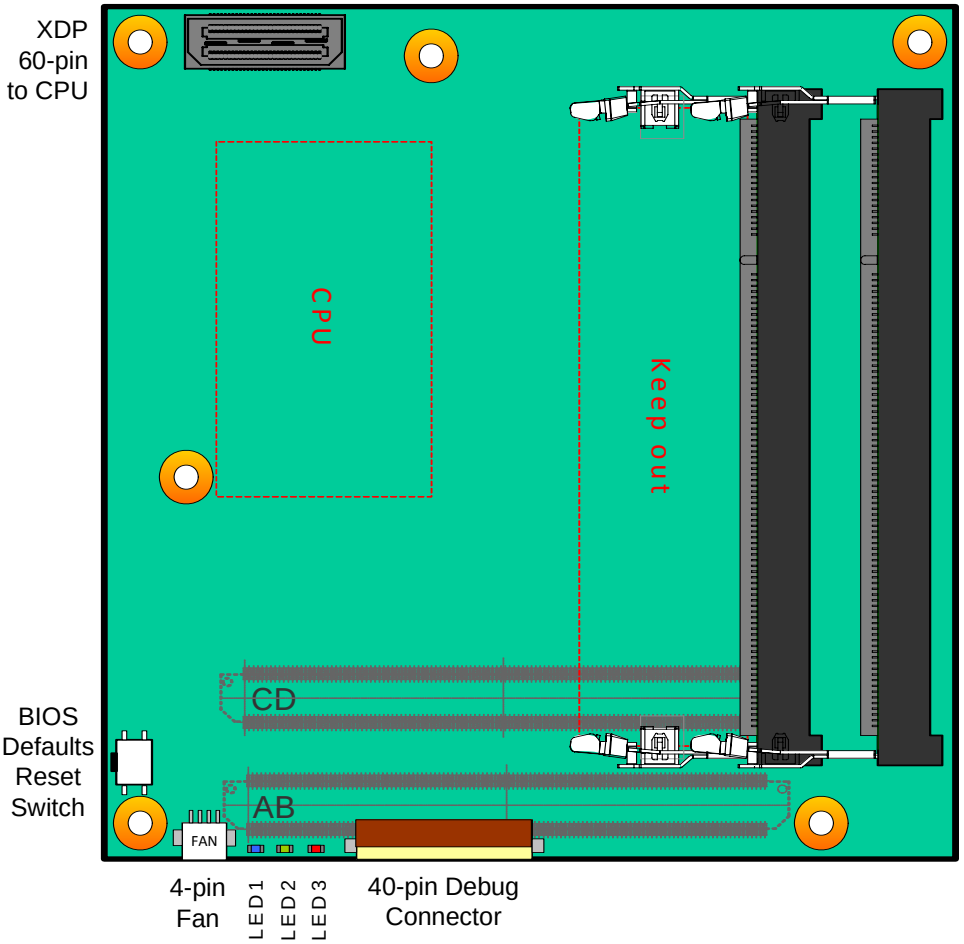
Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	C104-C109 D104-D109	Primary power input: +12V nominal (5 ~ 20V wide input). All available VCC_12V pins on the connector(s) shall be used.	P		5~20 V
GND	C1, C11, C21, C31, C41, C51, C60, C70, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D11, D21, D31, D41, D51, D60, D67, D70, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane.	P		

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4. Connector Pinouts on Module

This chapter describes connectors and pinouts, LEDs and switches that are used on the module but are not included in the PICMG standard specification

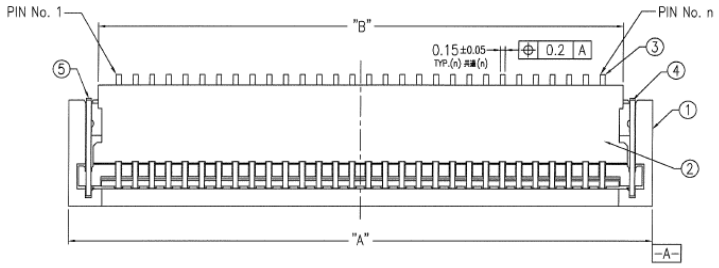
- Connector and LED Locations



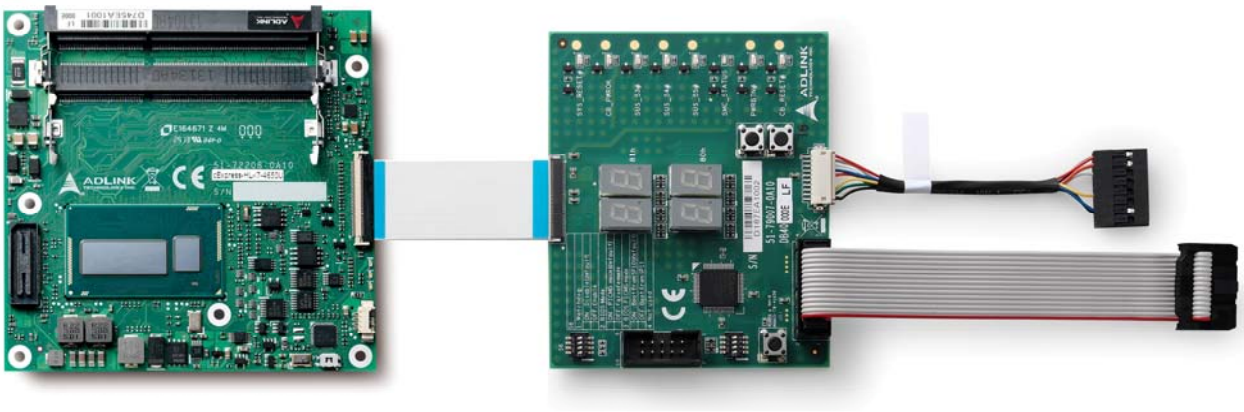
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4.1. 40-pin Debug Connector

- FPC Connector Type: FCI 59GF Flex 10042867
- Pin Orientation



- cExpress-BL and the DB40 Debug Module



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➢ 40-pin Debug Connector Pin Definition on the COM Express Module

Pin	Interface	Signal	Remark
1	SPI Program interface	VCC_SPI_IN	SPI Power Input from flash tool to module. HW need add MOS FET to switch SPI power for SPI ROM
2		GND	
3		SPI_BIOS_CS0#	
4		SPI_BIOS_CS1#	
5		SPI_BIOS_MISO	
6		SPI_BIOS_MOSI	
7		SPI_BIOS_CLK	
8	LPC Bus	3V3_LPC	System power 3.3V provide from COM module
9		GND	
10		BIOS_DIS0	
11		RST#	
12		CLK33_LPC	
13		LPC_FRAME#	
14		LPC_AD3	
15		LPC_AD2	
16		LPC_AD1	always power 3.3V provide from COM module
17		LPC_AD0	
18	BMC Program interface	3.3V_BMC	always power 3.3V provide from COM module
19		3.3V_BMC	always power 3.3V provide from COM module
20		GND	

Pin	Interface	Signal	Remark
21	BMC Program interface (continued)	TXD6	
22		RXD6	
23		FUMD0	
24		RESET_IN#	
25		DATA	
26		CLK	
27		OCD0A	Include a jumper to connect OCD0A via 1K0 pull-up to 3.3V_BMC
28		OCD0B	Include a jumper to connect OCD0A via 1K0 pull-up to 3.3V_BMC
29	Test points	PWRBTN#	
30		SYS_RESET#	
31		CB_RESET#	
32		CB_PWROK	
33		SUS_S3#	
34		SUS_S4#	
35		SUS_S5#	
36	BMC Debug signals	POSTWDT_DIS#	Connect to Jumper for Debug
37		SEL_BIOS	Connect to Jumper for Debug
38		BIOS_MODE	Connect to Jumper for Debug
39		BMC_STATUS	
40	Reserved		

Note: The pin definition on the debug module is the inverse of that on the COM Express module.

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4.2. Status LEDs

To facilitate easier maintenance, status LED's are mounted on the board.

➢ LED Descriptions

Name	Color	Connection	Function
LED1	Blue	BMC output	Power Sequence Status Code (BMC) Power Changes, RESET (see 5.1.4 Exception Codes below)
LED2	Green	Power Source 3Vcc	S0 LED ON S3/S4/S5 LED OFF ECO mode LED OFF
LED3	Red	BMC output and same signal as WDT (B27) on BtB connector	Module power up WD LED = LED OFF Watchdog counting WD LED = LED OFF Watchdog timed out WD LED = LED ON Watchdog RESET WD LED = LED ON Rebooted after WD RESET WD LED = LED ON Rebooted after PWRBTN WD LED = LED ON Rebooted after RESET BTN WD LED = LED OFF Note: only a RESET not initiated by the BMC can clear the WD LED (user action)

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4.3. XDP Debug header

The debug port is a connection into a target-system environment that provides access to JTAG, run control, system control, and observation resources. The XDP target system connector is a Samtec™ 60-pin BSH-030-01 series connector.

Pin	XDP Signal	Target Signal	I/O	Device
1	GND	GND	NA	
3	OBSFN_A0	PREQ#	I/O	Processor
5	OBSFN_A1	PRDY#	I/O	Processor
7	GND	GND	NA	
9	OBSDATA_A0	CFG[0][2]	I/O	Processor
11	OBSDATA_A1	CFG[1][2]	I/O	Processor
13	GND	GND	NA	
15	OBSDATA_A2	CFG[2][2]	I/O	Processor
17	OBSDATA_A3	CFG[3][2]	I/O	Processor
19	GND	GND	NA	
21	OBSFN_B0	BPM#[0][1]	I/O	Processor
23	OBSFN_B1	BPM#[1][1]	I/O	Processor
25	GND	GND	NA	
27	OBSDATA_B0	CFG[4][2]	I/O	Processor
29	OBSDATA_B1	CFG[5][2]	I/O	Processor
31	GND	GND	NA	
33	OBSDATA_B2	CFG[6][2]	I/O	Processor
35	OBSDATA_B3	CFG[7][2]	I/O	Processor
37	GND	GND	NA	
39	HOOK0	PWRGOOD	I	System
41	HOOK11	BP_PWRGD_RST#	O	System
43	VCC_OBS_AB	VCCIO_OUT	I	System
45	HOOK2	PWR_DEBUG	O	Processor
47	HOOK3	PCH_SYS_PWROK	O	System
49	GND	GND	NA	
51	SDA1	SDA	I/O	System
53	SCL1	SCL	I/O	System
55	TCK1	Open	NA	
57	TCK0	TCK	O	Processor
59	GND	GND	NA	

Pin	XDP Signal	Target Signal	I/O	Device
2	GND	GND	NA	
4	OBSFN_C0	CFG[17][2]	I	Processor
6	OBSFN_C1	CFG[16][2]	I	Processor
8	GND	GND	NA	
10	OBSDATA_C0	CFG[8][2]	I/O	Processor
12	OBSDATA_C1	CFG[9][2]	I/O	Processor
14	GND	GND	NA	
16	OBSDATA_C2	CFG[10][2]	I/O	Processor
18	OBSDATA_C3	CFG[11][2]	I/O	Processor
20	GND	GND	NA	
22	OBSFN_D0	CFG[19][2]	I/O	Processor
24	OBSFN_D1	CFG[18][2]	I/O	Processor
26	GND	GND	NA	
28	OBSDATA_D0	CFG[12][2]	I	Processor
30	OBSDATA_D1	CFG[13][2]	I	Processor
32	GND	GND	NA	
34	OBSDATA_D2	CFG[14][2]	I/O	Processor
36	OBSDATA_D3	CFG[15][2]	I/O	Processor
38	GND	GND	NA	
40	ITPCLK/HOOK4	Open	NA	
42	ITPCLK#/HOOK5	Open	NA	
44	VCC_OBS_CD	VCCIO_OUT	I	System
46	HOOK6/RESET#	PLTRSTIN#	I	System
48	HOOK7/DBR#	DBR#	O	System
50	GND	GND	NA	
52	TDO	TDO	I	Processor
54	TRSTn	TRST#	O	Processor
56	TDI	TDI	O	Processor
58	TMS	TMS	O	Processor
60	GND	GND (or XDP_PRESENT# if required)	NA	

Notes:

1. These signals are optional, can be left as OPEN/No-Connect if debug by Intel will not be needed.
2. These CFG signals can be left as Open/No Connect if not used as a strapping signal and top side probe will be used to debug processor.

Refer to the "Shark Bay, Denlow and Broadwell U/Y Platforms Debug Port Design Guide", Document Number: 479493, Revision: 2.0

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4.4. Fan Connector

- Connector Type: JVE 24W1125A-04M00
- Pin Assignment

Name	Signal	Description
1	BMC_FAN_OUT	FAN_PWMOUT
2	BMC_FAN_PWM_IN	FAN_TACHIN
3	GND	Ground
4	P5V_S	5V

4.5. BIOS Setup Defaults Reset Button

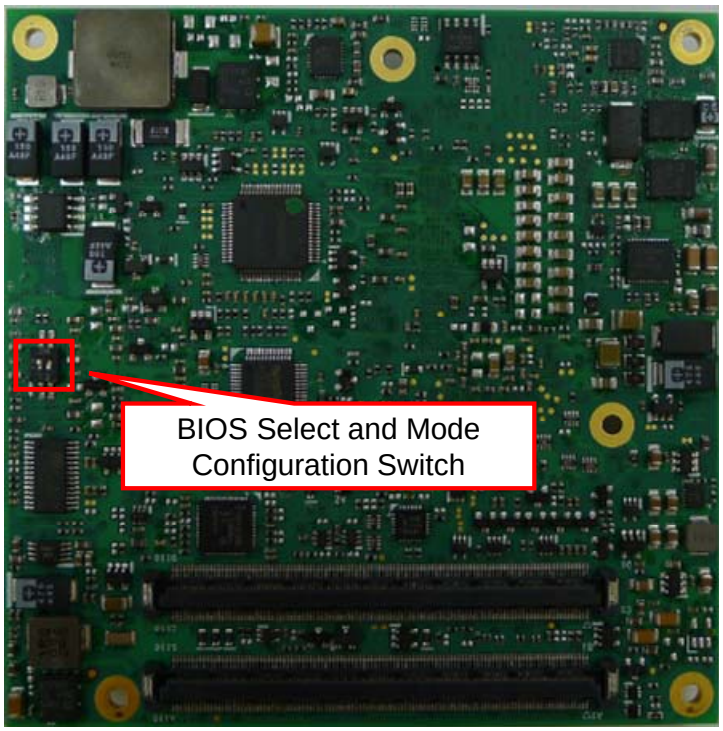
To perform a hardware reset of BIOS default settings, perform the following steps:

1. Shut down the system.
2. Press the BIOS Setup Defaults RESET Button continuously and boot up the system. You can release the button when the BIOS prompt screen appears
3. The BIOS prompt screen will display a confirmation that BIOS defaults have been reset and request that you reboot the system.



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4.6. BIOS Select and Mode Configuration Switch



The module has two BIOS chips and BIOS operation can be configured to "PICMG" and dual-BIOS "Failsafe" modes using the BIOS Select and Mode Configuration Switch, Pin 2.

Setting the module to PICMG mode will configure the BIOS chips on the module as SPI0 and SPI1. In PICMG mode, a BIOS chip cannot be placed in the SPI0 slot on the carrier.

In dual-BIOS Failsafe mode, both BIOS chips on the module are configured as SPI1. Only one of the two is connected to the SPI bus at any given time. In case of failure of the primary SPI1 BIOS, the system will reboot and switch to the secondary SPI1 BIOS on the module. In Failsafe mode, the SPI0 BIOS socket on the carrier can be populated.

In either mode, BIOS Select and Mode Configuration Switch, Pin 1 is used to select whether to boot from SPI0 or SPI1.

Mode	Pin 1	Pin 2
Boot from SPI0 (default)	On	—
Boot from SPI1	Off	—
Set BIOS to PICMG mode	—	On
Set BIOS to Failsafe BIOS mode (default)	—	Off

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5. Smart Embedded Management Agent (SEMA)

The onboard microcontroller (BMC) implements power sequencing and Smart Embedded Management Agent (SEMA) functionality. The microcontroller communicates via the System Management Bus with the CPU/chipset. The following functions are implemented:

- Total operating hours counter. Counts the number of hours the module has been run in minutes.
- On-time minutes counter. Counts the seconds since last system start.
- Temperature monitoring of CPU and board temperature. Minimum and maximum temperature values of CPU and board are stored in flash.
- Power cycles counter
- Boot counter. Counts the number of boot attempts.
- Watchdog Timer (Type-II). Set/Reset/Disable Watchdog Timer. Features auto-reload at power-up.
- System Restart Cause. Power loss/BIOS Fail/Watchdog/Internal Reset/External Reset
- Fail-safe BIOS support. In case of a boot failure, hardware signals tells external logic to boot from fail-safe BIOS.
- Flash area. 1kB Flash area for customer data
- 128 Bytes Protected Flash area. Keys, IDs, etc. can be stored in a write- and clear-protectable region.
- Board Identify. Vendor/Board/Serial number/Production Date
- Main-current & voltage. Monitors drawn current and main voltages

For a detailed description of SEMA features and functionality, please refer to SEMA Technical Manual and SEMA Software Manual, downloadable at: http://www.adlinktech.com/sema/.

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5.1. Board Specific SEMA Functions

5.1.1. Voltages

The BMC of the cExpress-BL implements a voltage monitor and samples several onboard voltages. The voltages can be read by calling the SEMA function “Get Voltages”. The function returns a 16-bit value divided into high-byte (MSB) and low-byte (LSB).

ADC Channel	Voltage Name	Voltage Formula [V]
0	+V1.5S	(MSB<<8 + LSB) x 3.3 / 1024
1	+VCORE	(MSB<<8 + LSB) x 3.3 / 1024
2	+V1.05S	(MSB<<8 + LSB) x 3.3 / 1024
3	+V3.3A	(MSB<<8 + LSB) x 1.100 x 3.3 / 1024
4	+VDDQ (V1.35 ~ V1.5)	(MSB<<8 + LSB) x 3.3 / 1024
5	+V5A_DUAL	(MSB<<8 + LSB) x 1.833 x 3.3 / 1024
6	+VIN	(MSB<<8 + LSB) x 6.000 x 3.3 / 1024
7	(MAIN CURRENT)	Use Main Current Function

5.1.2. Main Current

The BMC of the cExpress-BL implements a current monitor. The current can be read by calling the SEMA function “Get Main Current”. The function returns four 16-bit values divided in high-byte (MSB) and low-byte (LSB). These 4 values represent the last 4 currents drawn by the board. The values are sampled every 250ms. The order of the 4 values is NOT in chronological order. Access by the BMC may increase the drawn current of the whole system. In this case, there are still 3 samples not influenced by the read access.

Main Current = (MSB_n<<8 + LSB_n) x 8.06mA

5.1.3. BMC Status

This register shows the status of BMC controlled signals on the cExpress-BL.

Status Bit	Signal
0	WDT_OUT
1	LVDS_VDDEN
2	LVDS_BKLTEN
3	BIOS_MODE
4	POSTWDT_DISn
5	SEL_BIOS
6	BIOS_DIS0n
7	BIOS_DIS1n

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5.1.4. Exception Codes

In case of an error, the BMC drives a blinking code on the blue Status LED (LED1). The same error code is also reported by the BMC Flags register. The Exception Code is not stored in the Flash Storage and is cleared when the power is removed. Therefore, a “Clear Exception Code” command is not needed or supported.

Exception Code	Error Message
0	NOERROR
2	NO_SUSCLK
3	NO_SLP_S5
4	NO_SLP_S4
5	NO_SLP_S3
6	BIOS_FAIL
7	RESET_FAIL
8	POWER_FAIL
9	LOW_VIN
11	VCORE
12	+P1V05_S
13	+P3V3_A
14	+VDDQ
15	+P5V_A
16	+P12V
18	CRITICAL_TEMP
19	NO_CB_PWROK
20	NO_SYS_GD
21	NO_VCORE_GD
22	NO_XDP_PIN47

5.1.5. BMC Flags

The BMC Flags register returns the last detected Exception Code since power-up and shows the BIOS in use and the power mode.

Bit	Description
[0 ~ 4]	Exception Code
[6]	0 = AT mode 1 = ATX mode
[7]	0 = Standard BIOS 1 = Fail-safe BIOS.

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6. System Resources

6.1. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
(4GB-2MB)	FFE00000 – FFFFFFFF	2 MB	High BIOS Area
(4GB-18MB) – (4GB-17MB-1)	FEE00000 – FEEFFFFF	1 MB	MSI Interrupts
(4GB-20MB) – (4GB-19MB-1)	FEC00000 – FECFFFFF	1 MB	APIC Configuration Space
15MB – 16MB	F00000 – FFFFFF	1 MB	ISA Hole
1MB -15MB	100000 - EFFFFF	14MB	Main Memory
0K –1MB	00000 – FFFFFF	1MB	DOS Compatibility Memory

6.2. Direct Memory Access Channels

Channel Number	Data Width	System Resource
0	8-bits	Generic
1	8-bits	Generic
2	8-bits	Generic
3	8-bits	Generic
4		Reserved - cascade channel
5	16-bits	Generic
6	16-bits	Generic
7	16-bits	Generic

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6.3. I/O Map

Hex Range	Device
000-01F	Reserved
020-02D and 030-03F	Interrupt controller 1, 8259 equivalent
02E-02F	LPC SIO () configuration index/data registers
040-05F	Timer, 8254-2 equivalent
060, 062, 064, 066, 068-06F	8742 equivalent (keyboard)
061, 063, 065, 067	NMI control and status
070-07F	Real Time Clock Controller(bit 7 -NMI mask)
080-090	LPC or PCIe
092	Reset (Bit 0)/ Fast Gate A20 (Bit 1)
091， 93-9F	Reserved
0A0-0B1 and 0B4-0BF	Interrupt controller 2, 8259 equivalent
0B2 and 0B3	APM control and status port respectively
0C0-0DF	Reserved
0E0-0EF	Available
0F0	Co-processor error register
0F1-0FF	N/A
100-169	N/A
170-177	Sata Controller
178-1EF	N/A
1F0-1F7	Sata Controller
1F8-2DF	N/A
2E0 -2F7	Serial Port 3/4
2F8-2FF	Serial Port 2
300-36F	Available
376	Sata Controller
378-37F	Available
380-3AF	Available
3B0-3BB and 3BF	Mono/VGA mode video
3BC-3BE	Reserved for parallel port
3C0-3DF	VGA registers
3E0-3EF	Available

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Hex Range	Device
3F0-3F7	Available
3F8-3FF	Serial port 1
4D0	Master PIC Edge/Level Trigger register
4D1	Slave PIC Edge/Level Trigger register
CF8-CFB	PCI configuration address register (32 bit I/O only)
CF9	Reset Control register (8 bit I/O)
CFC-CFF	PCI configuration data register
F040	Smbus base address for SB.
1C00	GPIO Base Address for SB
1800	PM (ACPI) Base Address for SB
1860	Alias for ICH TCO base address.
0A00~0AFF	Reserved for SIO functions base address (ex: PME /GPIO etc)

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6.4. Interrupt Request (IRQ) Lines

PIC Mode

IRQ#	Typical Intterupt Resource	Connected to Pin	Available
0	Counter 0	N/A	No
1	Keyboard controller	N/A	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 2 (COM2)	IRQ3 via SERIRQ / PIRQ	Note (1)
4	Serial Port 1 (COM1)	IRQ4 via SERIRQ / PIRQ	Note (1)
5	Parallel Port 2 (LPT2)	IRQ5 via SERIRQ / PIRQ	Note (1)
6	Generic	IRQ6 via SERIRQ / PIRQ	No
7	Generic	IRQ7 via SERIRQ / PIRQ	Note (1)
8	Real-time clock	N/A	No
9	Generic	N/A	Note (1)
10	Serial Port 3 (COM3)	IRQ10 via SERIRQ / PIRQ	Note (1)
11	Serial Port 4 (COM4)	IRQ11 via SERIRQ / PIRQ	Note (1)
12	PS/2 Mouse	IRQ12 via SERIRQ / PIRQ	Note (1)
13	GSPI, UART, I2C, SDIO	N/A	Note (1)
14	gpio	PIRQ	Note (1)
15	gpio	PIRQ	Note (1)

Note (1): These IRQs can be used for PCI devices when onboard device is disabled.

APIC Mode

IRQ#	Typical Intterupt Resource	Connected to Pin	Available
0	Counter 0	N/A	No
1	Keyboard controller	N/A	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 2 (COM2)	IRQ3 via SERIRQ / PIRQ	Note (1)
4	Serial Port 1 (COM1	IRQ4 via SERIRQ / PIRQ	Note (1)
5	N/A	N/A	Note (1)
6	N/A	N/A	Note (1)
7	N/A	N/A	Note (1)
8	Real-time clock	N/A	No
9	N/A	IRQ9 via SERIRQ / PIRQ	Note (1)
10	Serial Port 3 (COM3)	IRQ10 via SERIRQ / PIRQ	Note (1)

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IRQ#	Typical Intterupt Resource	Connected to Pin	Available
11	Serial Port 4 (COM4)	IRQ11 via SERIRQ / PIRQ	Note (1)
12	PS/2 Mouse	IRQ12 via SERIRQ / PIRQ	Note (1)
13	Math Processor	N/A	Note (1)
14	Primary IDE controller	IRQ14 via SERIRQ / PIRQ	Note (1)
15	Secondary IDE controller	IRQ15 via SERIRQ / PIRQ	Note (1)
16	N/A	P.E.G Root Port,Intel HDA, PCIE Port 0/1/2/3/4/5/6, EHCI Conterller #2 , I.G.D ,XHCI Controller	Note (1)
17	N/A	PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port,	Note (1)
18	N/A	PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port, SMBus Controller, EHCI Controller #2	Note (1)
19	N/A	PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port,	Note (1)
20	N/A	Gbe Controller	Note (1)
21	N/A		Note (1)
22	N/A	Intel HDA	Note (1)
23	N/A	EHCI Controller #1	Note (1)

Note (1): These IRQs can be used for PCI devices when onboard device is disabled.

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6.5. PCI Configuration Space Map

Bus Number	Device Number	Function Number	Routing	Description
00h	00h	00h	N/A	Intel host Bridge
00h	02h	00h	Internal	Intel I.G.D
00h	03h	00h	Internal	HD Audio Device
00h	13h	00h	Internal	Instel Smart Sound Technology Controller
00h	14h	00h	Internal	xHCI Controller
00h	15h	00h	Internal	Intel Serial I/O DMA Controller
00h	15h	01h	Internal	Intel Serial I/O I2C Controller #0
00h	15h	02h	Internal	Intel Serial I/O I2C Controller #1
00h	15h	03h	Internal	Intel Serial I/O GSPI Controller #0
00h	15h	04h	Internal	Intel Serial I/O GSPI Controller #1
00h	15h	05h	Internal	Intel Serial I/O UART Controller #0
00h	15h	06h	Internal	Intel Serial I/O UART Controller #1
00h	16h	00h	Internal	Intel Management Engine Interface #1
00h	16h	01h	Internal	Intel Management Engine Interface #2
00h	17h	00h	Internal	SDIO Controller
00h	19h	00h	Internal	Gigabit Etherent Controller
00h	1Bh	00h	Internal	High Definition Audio controller
00h	1Ch	00h	Internal	Intel PCI Express Root port 1
00h	1Ch	01h	Internal	Intel PCI Express Root port 2
00h	1Ch	02h	Internal	Intel PCI Express Root port 3
00h	1Ch	03h	Internal	Intel PCI Express Root port 4
00h	1Ch	04h	Internal	Intel PCI Express Root port 5
00h	1Ch	05h	Internal	Intel PCI Express Root port 6
00h	1Dh	00h	Internal	Intel USB EHCI Controller #1
00h	1Fh	00h	N/A	Intel LPC Interface Bridge
00h	1Fh	02h	Internal	SATA Host Controller #1
00h	1Fh	03h	Internal	SMBus Controller
00h	1Fh	06h	Internal	Thermal Controller

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6.6. PCI Interrupt Routing Map

INT Line	P.E.G Root Port	Audio Controller	xHCI Controller	ME Controller #1	ME Controller #2	IDE-R	KT	GbE Controller	HAD Controller
Int0	INTA:16	INTH:23	INTA:16	INTA:16				INTE:20	INTG:22
Int1	INTB:17			INTD:19					
Int2	INTC:18			INTC:18					
Int3	INTD:19			INTB:17					

INT Line	PCIE port1	PCIE port 2	PCIE port 3	PCIE port 4	PCIE port5 (GbE)	PCIE port6 (SATA)	EHCI #1	EHCI #2
Int0	INTA:16	INTB:17	INTC:18	INTD:19	INTA:16	INTB:17	INTH:23	INTA:16
Int1	INTB:17	INTC:18	INTD:19	INTA:16	INTB:17	INTC:18	INTD:19	INTF:21
Int2	INTC:18	INTD:19	INTA:16	INTB:17	INTC:18	INTD:19	INTA:16	INTC:18
Int3	INTD:19	INTA:16	INTB:17	INTC:18	INTD:19	INTA:16	INTC:18	INTD:19

INT Line	LPC Controller	SATA Controller #1	SMBus Controller	SATA Controller #2	Thermal Subsystem	SDIO Controller #1	Intel Smart Sound Tech. Controller
Int0	INTF:21					INTG:22	INTH:23
Int1	INTD:19	INTD:19		INTD:19			
Int2	INTC:18		INTC:18		INTC:18		
Int3	INTA:16						

6.7. SMBus Address Table

Device	Address
DIMM A	A0h
DIMM B	A4h
BMC	50h
Extend GPIO	40h

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7. BIOS Setup

7.1. Menu Structure

This section presents the six primary menus of the BIOS Setup Utility. Use the following table as a quick reference for the contents of the BIOS Setup Utility. The subsections in this section describe the submenus and setting options for each menu item. The default setting options are presented in **bold**, and the function of each setting is described in the right hand column of the respective table.

Main	Advanced	Security	Boot	Save & Exit
- System Information	- CPU ▶	- Password Description ▶	- Boot Configuration ▶	- Reset Options ▶
- Processor Information	- Memory ▶	- Secure Boot Menu ▶	- CSM Configuration ▶	- Save Options ▶
- VGA Firmware Version	- Graphics ▶			
- Memory Information	- SATA ▶			
- SOC Information	- USB ▶			
- System Management ▶	- Network ▶			
- System Date	- PCI ▶			
- System Time	- Super IO ▶			
	- ACPI and Power Management ▶			
	- Sound ▶			
	- Serial Port Console ▶			
	- ACPI Thermal ▶			
	- Miscellaneous ▶			

Notes:

▶ indicates a submenu

Gray text indicates info only

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7.2. Main

The Main Menu provides read-only information about your system and also allows you to set the System Date and Time. Refer to the tables below the screen shot of this menu for details of the submenus and settings.

7.2.1. Main > System Information

Feature	Options	Description
BIOS Version	Info only	ADLINK BIOS version.
Build Date and Time	Info only	ADLINK date the BIOS was build.

7.2.2. Main > Processor Information

Feature	Options	Description
CPU Brand String	Info only	Display CPU Brand Name.
Frequency	Info only	Display CPU Frequency.
Number of Processors	Info only	Display number of Processors.
GT Info	Info only	Display GT info of Intel Graphics.
IGFX VBIOS Version	Info only	Display VBIOS Version.
Total Memory	Info only	Display installed memory size.

7.2.3. Main > PCH Information

Feature	Options	Description
PCH SKU	Info only	Display PCH SKU.
ME FW Version	Info only	Display version of ME.
ME Firmware SKU	Info only	Display ME Firmware Kit SKU number.
System Management	Submenu	

7.2.4. Main >System Management > System Management

Feature	Options	Description
System Management	Info only	
Version	Info only	Display version.

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7.2.5. Main >System Management > Board Information

Board Information	Info only	
SEMA Firmware	Read only	Display SEMA Firmware.
Build Date	Read only	Display SEMA firmware build date.
SEMA Boot loader	Read only	Display SEMA boot loader.
Build Date	Read only	Display SEMA boot loader build date.
Hardware Version	Read only	Display SEMA hardware Version.
Serial Number	Read only	Display SEMA serial Number.
Manufacturing Date	Read only	Display SEMA manufacturing date.
Last Repair Date	Read only	Display SEMA last repair date.
MAC ID	Read only	Display SEMA MAC ID.

1.1.6 System Management > Temperatures and Fan Speed

Feature	Options	Description
Temperatures and Fan	Info only	
CPU Temperature	Info only	
Current	Read only	Display CPU current temperature.
Startup	Read only	Display CPU startup temperature.
Min	Read only	Display CPU min temperature.
Max	Read only	Display CPU max temperature.
Board Temperatures	Info only	
Current	Read only	Display board current temperature.
Startup	Read only	Display board startup temperature.
Min	Read only	Display board min temperature.
Max	Read only	Display board max temperature.
CPU Fan Speed	Read only	Display CPU fan speed.
System Fan Speed	Read only	Display system fan speed.

7.2.6. System Management > Power Consumption

Feature	Options	Description
Power Consumption	Info only	
Current Input Current	Read only	Display input current.
Current Input Power	Read only	Display input power.
V1.50	Read only	Display actual voltage of the V1.50.
CPU-VCORE	Read only	Display actual voltage of the CPU-VCORE.
V1.05	Read only	Display actual voltage of the V1.05.

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Feature	Options	Description
V3.30	Read only	Display actual voltage of the V3.30.
VMEM	Read only	Display actual voltage of the VMEM.
V5.00	Read only	Display actual voltage of the V5.00.
VIN	Read only	Display actual voltage of the VIN.
AIN7	Read only	Display actual voltage of the AIN7.

7.2.7. System Management > Runtime Statistics

Feature	Options	Description
Runtime Statistics	Info only	
Total Runtime	Read only	The returned value specifies the total time in minutes the system is running in S0 state.
Current Runtime	Read only	The returned value specifies the time in seconds the system is running in S0 state. This counter is cleared when the system is removed from the external power supply.
Power Cycles	Read only	The returned value specifies the number of times the external power supply has been shut down
Boot Cycles	Read only	The Bootcounter is increased after a HW- or SW-Reset or after a successful power-up.
Boot Reason	Read only	The boot reason is the event which causes the reboot of the system.

1.1.9 System Management > Flags

Feature	Options	Description
Flags	Info only	
BMC Flags	Read only	
BIOS Select	Read only	Display the selection of current BIOS ROM.
ATX/AT-Mode	Read only	Display ATX/AT-Mode.
Exception Code	Read only	System exception reason.

7.2.8. System Management > Power Up

Feature	Options	Description
Power Up	Info only	
Power Up watchdog Note: F12 disables the Power Up Watchdog.	Enabled Disabled	The Power-Up Watchdog resets the system after a certain amount of time after power-up.
ECO Mode	Disable Enable	Reduces the power consumption of the system.
Power-up Mode ATTENTION: The Power-Up Mode only has effect, if the module is in ATX-Mode.	Turn on Remain off Last State	Turn On:The machine starts automatically when the power supply is turned on.Remain Off:To start the machine the power button has to be pressed.

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7.2.9. System Management > LVDS Backlight

Feature	Options	Description
LVDS Backlight	Info only	
LVDS Backlight Bright	255	The value range starts by 0 and ends by 255.

7.2.10. System Management > Smart Fan

Feature	Options	Description
Smart Fan	Info only	
CPU Smart FanTemperature Source	CPU Sensor System Sensor	Select CPU smart fan source.
CPU Fan Mode	AUTO (Smart Fan) Fan Off Fan On	Select CPU Fan Mode.
CPU Trigger Point 1	Read only	
Trigger Temperature	15	Specifies the temperature threshold at which the BMC turnn on CPU fan with specific PWM level.
PWM Level	30	Select PWM level.
CPU Trigger Point 2	Read only	
Trigger Temperature	60	Specifies the temperature threshold at which the BMC turnn on CPU fan with specific PWM level.
PWM Level	40	Select PWM level.
CPU Trigger Point 3	Read only	
Trigger Temperature	70	Specifies the temperature threshold at which the BMC turnn on CPU fan with specific PWM level.
PWM Level	63	Select PWM level.
CPU Trigger Point 4	Read only	
Trigger Temperature	80	Specifies the temperature threshold at which the BMC turnn on CPU fan with specific PWM level.
PWM Level	100	Select PWM level.

7.2.11. Main > System Date and Time

Feature	Options	Description
System Date	Weekday, MM / DD / YYYY	Requires the alpha-numeric entry of the day of the week, day of the month, calendar month, and all 4 digits of the year, indicating the century and year (Fri XX/XX/20XX)
System Time	HH / MM / SS	Presented as a 24-hour clock setting in hours, minutes, and seconds

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7.3. Advanced

This menu contains the settings for most of the user interfaces in the system.

7.3.1. Advanced > CPU

Feature	Options	Description
CPU	Info only	Manufacturer, model, speed
CPU Signature	Info only	Display CPU Signature.
Microcode Patch	Info only	Display Microcode Patch.
Max CPU speed	Info only	Display Max CPU speed.
Min CPU speed	Info only	Display Min CPU speed.
CPU Speed	Info only	Display CPU Speed.
Processor Cores	Info only	Display Processor Cores.
Intel HT Technology	Info only	Display Intel HT Technology support or not.
Intel VT-x Technology	Info only	Display Intel VT-x Technology support or not.
VT-d Capability	Info only	Display VT-d Capability support or not.
Intel SMX Technology	Info only	Display Intel SMX Technology support or not.
64-bit	Info only	Display 64-bit support or not.
L1 Data Cache	Info only	Display cache info.
L1 Code Cache	Info only	Display cache info.
L2 Cache	Info only	Display cache info.
L3 Cache	Inf o only	Display cache info.
Limit CPUID Maximum	Disabled Enabled	When Enabled, the processor will limit the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When Disabled, the processor will return the actual maximum CPUID input value
Execute Disable Bit	Disabled Enabled	Enable / Disable the Execute Disable Bit (XD) of the processor. With the XD bit set to enabled certain classes of malicious buffer overflow attacks can be prevented when combined with a supporting OS.
Intel Virtualization Technology	Disabled Enabled	Enable / Disable support for the Intel virtualization technology.
VT-d	Disabled Enabled	Check to enable VT-d function on MCH.
CPU Processor Power Managemnt (PPM)	Info only	
EIST	Disabled Enabled	Disabled: No SpeedStep, stick to CPU ratio Enabled: CPU speed is controlled by the operating system.
Turbo Mode	Disabled Enabled	Enable / Disable turbo mode.
CPU C3 Report	Disabled Enabled	Enable / Disable CPU C3 report to OS.
CPU C6 Report	Disabled Enabled	Enable / Disable CPU C6 report to OS.

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Feature	Options	Description
CPU C7 Report	Disabled CPU C7 CPU C7S	Enable / Disable CPU C7 report to OS.
C1 State auto undemotion	Disabled Enabled	Un-demotion from Demoted C1
C3 State auto undemotion	Disabled Enabled	Un-demotion from Demoted C3
ACPI T State	Disabled Enabled	Enable / Disable ACPI T state support.
CPU DTS	Disabled Enabled	Enable / Disable CPU DTS.

7.3.2. Advanced > Memory

Feature	Options	Description
Memory RC Version	Info only	Display Memory Reference Code Version.
Memory Frequency	Info only	Display Memory Frequency.
Total Memory	Info only	Display Total Memory.
Memory Voltage	Info only	Display Memory Voltage.
DIMM#0/1	Info only	Display DIMM#0/1.
CAS Latency (tCL)	Info only	Display CAS Latency (tCL).
Minimum delay time	Info only	Display Minimum delay time.
CAS to RAS (tRCDmin)	Info only	Display CAS to RAS (tRCDmin).
Row Precharge (tRPmin)	Info only	Display Row Precharge (tRPmin).
Active to Precharge (tRASmin)	Info only	Display Active to Precharge (tRASmin).
XMP Profile 1	Info only	Display XMP Profile 1 support or not.
XMP Profile 2	Info only	Display XMP Profile 2 support or not.
SPD Write Protect	Enabled Disabled	Enable:Writes to SMBus slave addresses A0h - AEh are disabled.
Memory Frequency Limiter	Auto 1333 1600	Maximum Memory Frequency Selections in Mhz.
Max TOLUD	Dynamic	Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.
MRC Fast Boot	Enabled Disabled	Enable / Disable MRC fast boot.
Memory Remap	Enabled Disabled	Enable / Disable e memory remap above 4G.

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7.3.3. Advanced > Graphics

Feature	Options	Description
Graphics Configuration	Info only	
IGFX VBIOS Version	Info only	Display VBIOS Version.
IGfx Frequency	Info only	Display IGfx Frequency.
Graphics Turbo IMON Current	Number entry field	Graphics turbo IMON current values supported (14-31).
Primary Display	Auto IGFX PEG PCIE	Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx.
Primary PCIE	Auto PCIE1 PCIE2 PCIE3 PCIE4 PCIE5 PCIE6 PCIE7	Select PCIE0/PCIE1/PCIE2/PCIE3/PCIE4/PCIE5/PCIE6/PCIE7 Graphics device should be Primary PCIE.
Internal Graphics	Auto Disable Enable	Keep IGD enabled based on the setup options.
Aperture Size	128MB 256MB 512MB	Select the Aperture Size.
DVMT Pre-Allocated	XXM	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.
DVMT Total Gfx Mem	XXXM	Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device.
Gfx Low Power Mode	Enabled Disabled	This option is applicable for SFF only.
EDP to LVDS Bridge Configuration	Info only	
Data format and Color Depth	Vesa 24 bpp JEIDA 24 bpp JEIDA/vesa 18 bpp	Data format and Color Depth select
LVDS Output Mode	Single LVDS bus Dual LVDS bus	Single/Dual mode select
Vsync Polarity	Active High Active Low	Vsync Polarity select
LVDS Backlight Mode	BMC Mode GTT Mode	Select LVDS Backlight control function.
GTT LVDS Backlight Control	0% 20% 40% 60% 80% 100%	Actual backlight value in percent of the maximum setting.

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Feature	Options	Description
DDI function choose	Display Port HDMI	Select DDI function choose to display port or HDMI.
Primary IGFX Boot Display	VBIOS Default	Select the Video Device which will be activated during POST
LCD Panel Type	VBIOS Default 640X480 800X600 1024X768 1280X1024 1400X1050 1600X1200 1366X768 1680X1050 1920X1200 1440X900 1600X900 1024X768 LVDS2 1280X800 1920X1080 2048X1536	Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.
Active LFP	No LVDS Edp Port-A	Select the Active LFP Configuration.
Panel Scaling	Auto Off Force Scaling	Select the LCD panel scaling option used by the Internal Graphics Device.
GT – Power Management Control	Info only	
GT Info	Info only	Display GT info of Intel Graphics.
RC6 (Render Standby)	Enabled Disabled	Check to enable render standby support.
GT OverClocking Support	Enabled Disabled	Enable / Disable GT OverClocking Support.
GT OverClocking Frequency	XX	Overclocked RP0 Frequency (MLC Clk) in multiples of 50 MHz
GT OverClocking Voltage	XX	Extra voltage needed above the original RP0 voltage - The unit is 1/256 volt

7.3.4. Advanced > SATA

Feature	Options	Description
SATA Controller(s)	Enabled Disabled	Enable / Disable SATA Device.
SATA Mode Selection	AHCI RAID	Determines how SATA controller(s) operate.
Aggressive LPM Support	Enabled Disabled	Enable PCH to aggressively enter link power state.
SATA Controller Speed	Gen1 Gen2 Gen3	Indicates the maximum speed the SATA controller can support.

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Feature	Options	Description
SATA Port Configuration	Submenu	
Software Feature Mask Configuration	Info only	
RAID0	Enabled Disabled	Enable / Disable RAID0 feature.
RAID1	Enabled Disabled	Enable / Disable RAID1 feature.
RAID10	Enabled Disabled	Enable / Disable RAID10 feature.
RAID5	Enabled Disabled	Enable / Disable RAID5 feature.
Intel Rapid Recovery Technology	Enabled Disabled	Enable / Disable Intel Rapid Recovery Technology.
OROM UI and BANNER	Enabled Disabled	If enabled, then the OROM UI is shown. Otherwise, no OROM banner or information will be displayed if all disks and RAID volumes are Normal.
HDD Unlock	Enabled Disabled	If enabled, indicates that the HDD password unlock in the OS is enabled.
LED Locate	Enabled Disabled	If enabled, indicates that the LED/SGPIO hardware is attached and ping to locate feature is enabled on the OS.
IRRT Only on ESATA	Enabled Disabled	If enabled, then only IRRT volumes can span internal and eSATA drives. If disabled, then any RAID volume can span internal and eSATA drives.
Smart Response Technology	Enabled Disabled	Enable / Disable Smart Response Technology.
OROM UI Delay	2 Seconds 4 Seconds 6 Seconds 8 Seconds	If enabled, indicates the delay of the OROM UI Splash Screen in a normal status.

7.3.4.1. Advanced > SATA > SATA Port Configuration

Feature	Options	Description
SATA Port Configuration	Info only	
Port X	Disabled Enabled	Enable / Disable SATA Port.
Hot Plug	Disabled Enabled	Designates this port as Hot Pluggable.
Mechanical Presence	Disabled Enabled	Controls reporting if this port has an Mechanical Presence Switch.\n\nNote: Requires hardware support.
External SATA	Disabled Enabled	External SATA Support.
SATA Device Type	Hard Disk Drive Sold State Drive	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.
Spin up Device	Disabled Enabled	On an edge detect from 0 to 1, the PCH starts a COMRESET initialization sequence to the device.

7.3.5. Advanced > USB

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Feature	Options	Description
USB Module Version	Info only	
USB Devices	Info only	X Drive, X Keyboards, X Mouse, X Hubs
Legacy USB Support	Enabled Disabled Auto	Enables legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications and setup.
XHCI Hand-off	Enabled Disabled	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by the XHCI OS driver.
EHCI Hand-off	Enabled Disabled	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by the EHCI OS driver.
USB Mass Storage Driver Support	Enabled Disabled	Enable/Disable USB Mass Storage Driver Support.
PCH USB Configuration	Submenu	
USB hardware delays and time-outs:	Info only	
USB transfer time-out	1 sec 5 sec 10 sec 20 sec	The time-out value for Control, Bulk, and Interrupt transfers
Device reset time-out	10 sec 20 sec 30 sec 40 sec	USB mass storage device Start Unit command time-out.
Device power-up delay	Auto Manual	Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.
Mass Storage Devices	Info only	List current USB max stroge device.

7.3.5.1. Advanced > USB > PCH USB Configuration

Feature	Options	Description
USB Precondition	Disable Enable	Precondition work on USB host controller and root ports for faster enumeration.
XHCI Mode	Smart Auto Auto Enable Disable Manial	Mode of operation of xHCI controller.
XHCI Idle L1	Enabled Disabled	Enable or disable XHCI Idle L1.\n XhcildleL1 can be set to disable for LPT-LP Ax stepping to workaround USB3 hot plug will fail after 1 hot plug removal.
BTCG	Disable Enable	Enable / Disable trunk clock gating.
USB Ports Per-Port Disable Control	Disable Enable	Control each of the USB ports (0~13) disabling.

7.3.6. Advanced > Network

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Feature	Options	Description
Network Stack	Info only	
Network Stack	Enabled **Disabled**	Enable/Disable UEFI network stack.
PCH LAN Controller	**Enabled** Disabled	Enable / Disable onboard NIC.
Wake on LAN	Enabled **Disabled**	Enable / Disable integrated LAN to wake the system. (The Wake On LAN cannot be disabled if ME is on at Sx state.
AMT Configuration	Info only	
Intel AMT	Enabled **Disabled**	Enable/Disable Intel (R) Active Management Technology BIOS Extension.
BIOS Hotkey Pressed	Enabled **Disabled**	Enable/Disable BIOS hotkey press.
MEBx Selection Screen	Enabled **Disabled**	Enable/Disable MEBx selection screen.
Hide Un-Configure ME Confirmation	Enabled **Disabled**	Hide Un-Configure ME without password Confirmation Prompt.
MEBx Debug Message Output	Enabled **Disabled**	Enable MEBx debug message output.
Un-Configure ME	Enabled **Disabled**	Un-Configure ME without password.
Amt Wait Timer	0	Set timer to wait before sending ASF_GET_BOOT_OPTIONS.
Disable ME	Enabled **Disabled**	Set ME to Soft Temporary Disabled.
ASF	**Enabled** Disabled	Enable/Disable Alert Specification Format.
Activate Remote Assistance Process	Enabled **Disabled**	Trigger CIRA boot.
USB Configure	**Enabled** Disabled	Enable/Disable USB Configure function.
PET Progress	**Enabled** Disabled	User can Enable/Disable PET Events progress to recieve PET events or not.
AMT CIRA Timeout	0	OEM defined timeout for MPS connection to be established. 0 - use the default timeout value of 60 seconds. 255 - MEBX waits until the connection succeeds.
Watchdog	Enabled **Disabled**	Enable/Disable WatchDog Timer.
OS Timer		Set OS watchdog timer.
BIOS Timer		Set BIOS watchdog timer.

7.3.7. Advanced > PCI and PCIe

Feature	Options	Description
PCI Common Settings	Info only	
PCI Latency Timer	**32 PCI Bus Clocks** 64 PCI Bus Clocks 96 PCI Bus Clocks 128 PCI Bus Clocks	Select the PCI latency defined in PCI Bus clock cycles

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Feature	Options	Description
	160 PCI Bus Clocks 192 PCI Bus Clocks 224 PCI Bus Clocks 248 PCI Bus Clocks	
VGA Palette Snoop	Disabled Enabled	Allow PCI cards that do not contain their own VGA color palette to access the video core's palette
PERR# Generation	Disabled Enabled	Enables or Disables PCI Device to Generate PERR#.
SERR# Generation	Disabled Enabled	Enables / Disables PCI Device to Generate SERR#.
PCI Express Settings		
Relaxed Ordering	Disabled Enabled	Enables / Disables PCI Express Device Relaxed Ordering.
Extended Tag	Disabled Enabled	If ENABLED allows Device to use 8-bit Tag field as a requester.
No Snoop	Disabled Enabled	Enables / Disables PCI Express Snoop option
Maximum Payload	Auto 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Select Maximum Payload size or let BIOS decide (Auto)
Maximum Read Request	Auto 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value.
ASPM Support Warning Enabling ASPM may cause some PCI-E devices to fail	Disable Auto Force L0S	Set the ASPM Level: Force L0s - Force all links to L0s State : AUTO - BIOS auto configure : DISABLE - Disables ASPM.
Extended Synch	Enabled Disabled	If enabled the generation of PCI Express synchronization patterns is allowed
Link Training Retry	Disable 2 3 5	Defines number of Retry Attempts software will take to retrain the link if previous training attempt was unsuccessful.
Link Training Timeout (uS)	100	Defines number of Microseconds software will wait before polling 'Link Training' bit in Link Status register. Value range from 10 to 10000 uS.
Unpopulated Links	Keep Link ON Disable	In order to save power, software will disable unpopulated PCI Express links, if this option set to 'Disable Link'.
Restore PCIE Registers	Enabled Disabled	On non-PCI Express aware OS's (Pre Windows Vista) some devices may not be correctly reinitialized after S3. Enabling this restors PCI Express device configurations on S3 resume. Warning: Enabling this may cause issues with other hardware after S3 resume.
PCH-PCIe Configuration	Submenu	

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7.3.7.1. Advanced > PCI and PCIe > PCH-PCIe Configuration

Feature	Options	Description
PCH-PCIe Configuration	Info only	
PCI Express Clock Gating	Disable Enable	Enable / Disable PCI Express Clock Gating for each root port.
DMI Link ASPM Control	Disable Enable	The control of Active State Power Management on both NB side and SB side of the DMI Link.
DMI Link Extended Synch Control	Disable Enable	The control of Extended Synch on SB side of the DMI Link.
PCIE Root Port Function Swapping	Disable Enable	Enable / Disable PCI Express PCI Express Root Port Function Swapping.
Subtractive Decode	Disable Enable	Enable / Disable PCI Express Subtractive Decode.
PCIE Ports 1-4 Configuration	4x1 Port 1X2 2X1 Port 2X2 Port 1X4 Port	To configure PCI-E Port 1-4 of PCH. [4X1] : Port 1-4 (x1) and Port 8 (x1) [1x2 2x1]: Port 1 (x2), Port 2 (disabled), Ports 3 and Port 4 (x1) [2x2] : Port 1-2 (x2) and Port 3-4 (x2) / [1x4]:Port 1 (x4), Ports 2-4 (disable)
PCI Express Root Port 1~4	Submenu	Configure PCI Express Root Port 1~4 setting.
PCIE Port 5 is assigned to LAN	Info only	

Advanced > PCI and PCIe > PCH-PCIe Configuration >PCI Express Root Port

Feature	Options	Description
PCI Express Root Port	Disable Enable	Control the PCI Express Root Port.
ASPM Support	Disabled L0s L1 L0sL1 Auto	Set the ASPM Level: Force L0s - Force all links to L0s State : AUTO - BIOS auto configure : DISABLE - Disables ASPM
L1 Substates	Disabled L1.1 L1.2 L1.1 & L1.2	PCI Express L1 Substates settings.
URR	Disable Enable	Enable / Disable PCI Express Unsupported Request Reporting.
FER	Disable Enable	Enable / Disable PCI Express Device Fatal Error Reporting.
NFER	Disable Enable	Enable / Disable PCI Express Device Non-Fatal Error Reporting.
CER	Disable Enable	Enable / Disable PCI Express Device Correctable Error Reporting.
CTO	Disable Enable	Enable / Disable PCI Express Completion Timer TO.
SEFE	Disable Enable	Enable / Disable Root PCI Express System Error on Fatal Error.

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Feature	Options	Description
SENFE	Disable Enable	Enable / Disable Root PCI Express System Error on Non-Fatal Error.
SECE	Disable Enable	Enable / Disable Root PCI Express System Error on Correctable Error.
PME SCI	Disable Enable	Enable / Disable PCI Express PME SCI.
Hot Plug	Disable Enable	Enable / Disable PCI Express Hot Plug.
PCIe Speed	Auto Gen1 Gen2	Select PCI Express port speed.
Detect Non-Compiance	Disable Enable	Detect Non-Compliance PCI Express Device. If enable, it will take more time at POST time.
Extra Bus Reserved	0	Extra Bus Reserved (0-7) for bridges behind this Root Bridge.
Reseved Memory	10	Reserved Memory Range for this Root Bridge.
Prefetchable Memory	10	Prefetchable Memory Range for this Root Bridge.
Reserved I/O	4	Reserved I/O (4K/8K/12K/16K/.../48K) Range for this Root Bridge.
PCIE LTR	Disable Enable	PCIE Latency Reporting Enable/Disable.
PCIE LTR Lock	Disable Enable	PCIE LTR Configuration Lock.
Snoop Latency Ocerrid	Disable Manual Auto	Snoop Latency Ocerride for PCH PCIE.
Non Snoop Latency Ocerrid	Disable Manual Auto	Non Snoop Latency Ocerride for PCH PCIE.

7.3.8. Advanced > Super IO

Feature	Options	Description
Super IO Chip	Info only	
W83627DHG Super IO Configuration	Info only	
Serial Port 1 Configuration Serial Port	Enabled Disabled	Enable / Disable Serial Port (COM).
Device Settings	IO=3F8h; IRQ=4	Fixed configuration of serial port.
Change Settings	Auto IO=3F8h; IRQ=4 IO=3F8h; IRQ=3,4,5,6,7,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,10,11,12	Select an optimal setting for super IO device.

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Feature	Options	Description
Serial Port 2 Configuration		
Serial Port	Enabled Disabled	Enable / Disable Serial Port (COM).
Device Settings	IO=2F8h; IRQ=4	Fixed configuration of serial port.
Change Settings	Auto IO=2F8h; IRQ=3 IO=3F8h; IRQ=3,4,5,6,7,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,10,11,12	Select an optimal setting for super IO device.
	Standard Serial Port Mode IrDA Active pulse 1.6 uS IrDA Active pulse 3/16 bit time ASKIR Mode	
N5104D Super IO Configuration	Info only	
Serial Port 1 Configuration		
Serial Port	Enabled Disabled	Enable / Disable Serial Port (COM).
Device Settings	IO=240h; IRQ=10	Fixed configuration of serial port.
Change Settings	Auto IO=240h; IRQ=10 IO=240h; IRQ=10,11,12 IO=248h; IRQ=10,11,12 IO=250h; IRQ=10,11,12 IO=258h; IRQ=10,11,12	Select an optimal setting for super IO device.
Device Mode	RS232 Mode RS485 Mode	
Serial Port 2 Configuration		
Serial Port	Enabled Disabled	Enable / Disable Serial Port (COM).
Device Settings	IO=248h; IRQ=11	Fixed configuration of serial port.
Change Settings	Auto IO=248h; IRQ=11 IO=240h; IRQ=10,11,12 IO=248h; IRQ=10,11,12 IO=250h; IRQ=10,11,12 IO=258h; IRQ=10,11,12	Select an optimal setting for super IO device.
Device Mode	RS232 Mode RS485 Mode	

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7.3.9. Advanced > ACPI and Power Management

Feature	Options	Description
ACPI and Power Management	Info only	
Enable ACPI Auto Configuration	Enabled Disabled	Enables or Disables BIOS ACPI Auto Configuration.
Enable Hibernation	Enabled Disabled	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
Emulation AT/ATX	Emulation AT ATX	Select Emulation AT or ATX function. If this option set to [Emulation AT], BIOS will report no suspend functions to ACPI OS. In windows XP, it will make OS show shutdown message during system shutdown.
ACPI Sleep State	Suspend Disabled S1 only (CPU Stop Clock) S3 only (Suspend to RAM) Both S1 and S3 available for os to choose from	Select ACPI sleep state the system will enter when the SUSPEND button is pressed.

7.3.10. Advanced > Sound

Feature	Options	Description
Sound	Info only	
Azalia	Disable Enable Auto	Control Detection of the Azalia device. Disabled = Azalia will be unconditionally disabled . Enabled = Azalia will be unconditionally Enabled. Auto = Azalia will be enabled if present, disabled other.
Azalia Docking Support	Enabled Disabled	Enable / Disable Azalia Docking Support of Audio Controller.
Azalia PME	Enabled Disabled	Enable / Disable Power Management capability of Audio Controller.

7.3.11. Advanced > Serial Port Console

Feature	Options	Description
Serial Port Console	Info only	
COM1	Info only	
Console Redirection	Enabled Disabled	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	
COM2	Info only	
Console Redirection	Enabled Disabled	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	
COM3	Info only	
Console Redirection	Enabled Disabled	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	

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Feature	Options	Description
COM4	Info only	
Console Redirection	Enabled Disabled	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	

7.3.11.1. Advanced > Serial Port Console > Console Redirection

Feature	Options	Description
Console Redirection Settings	Info only	
Terminal Type	VT100 VT100+ VT-UTF8 ANSI	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 115200	Selects serial port transmission speed.
Data Bits	7 8	Select Data Bits.
Parity	None Even Odd Mark Space	Select Parity.
Stop Bits	1 2	Select number of stop bits.
Flow Control	None Hardware RTS/CTS	Select flow control.
VT-UTF8 Combo Key Support	Disable Enable	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.
Recorder Mode	Disable Enable	With this mode enabled only text will be sent. This is to capture Terminal data.
Resolution 100x31	Disable Enable	Enables or disables extended terminal resolution
Legacy OS Redirection	80x24 80x25	On Legacy OS, the Number of Rows and Columns supported redirection
Putty KeyPad	VT100 LINUX XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS Post	Always Enable BootLoader	The Settings specify if BootLoader is selected than Legacy console redirection is disabled before booting to Legacy OS. Default value is Always Enable which means Legaacy console Redirection is enabled for Legacy OS.

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7.3.12. Advanced > ICC Configuration

Feature	Options	Description
Turn off unused PCI/PCIe clocks	Disabled Enable	Disabled: all clocks turned on. Enabled: clocks for empty PCI/PCIe slots will be turned off to save power. Platform must be powered off for changes to take effect.
Clock Manipulation	Info only	
ICC Overclocking Lib	Info only	
Clock2	Submenu*	
CLKRUN# Logic	Enabled Disabled	Enable the CLKRUN# logic to stop the PCI clock.

*Note: This submenu is “view only” in standard BIOS. The options can be accessed by customer request if neccessary.

7.3.12.1. Advanced > ICC Configuration > Clock2

Feature	Options	Description
Clock2	info only	Requested SSC mode. Changes will not be applied unless 'Accept changes' is pressed.
BCLK, DMI, PEG, PCIe, PCI33, SATA, USB3	info only	
Maximum supported frequency	info only	
Minimum supported frequency	info only	
Current frequency	info only	
Supported SSC modes	info only	
Current SSC mode	info only	
New SSC Mode:	Down Center Up	Requested SSC mode. Changes will not be applied unless 'Accept changes' is pressed.
Maximum supported SSC %	info only	
"Current SSC %"	info only	
New SSC spread percent [0.01%]	value	Requested SSC percent in 0.01% increments. Changes will not be applied unless 'Accept changes' is pressed.
Apply settings immediately	Apply item	Changes will be applied immediately, but forgotten after reboot. This mode of making changes is more likely to cause platform instability and spontaneous restart.
Apply settings permanently after reboot	Apply item	Changes will be applied permanently, starting after the next reboot. Use it to provide changes that are verified and safe.

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7.3.13. Advanced > Thermal

Feature	Options	Description
Thermal	Info only	
Automatic Thermal Reporting	Enabled Disabled	Configure _CRT, _PSV and _AC0 automatically based on values recommended in BWG's Thermal Reporting for Thermal Management settings. Set to Disabled for manual conmfiguration.
Critical Trip Point	Disable 85 C 95C	This value controls the temperature of the ACPI Critical Trip Point - the point in which the OS will shut the system off. NOTE: 100C is the Plan Of Record (POR) for all Intel mobile processors.
Active Trip Point	Disable 40 C 50 C 60 C 70 C BMC Default	This value controls the temperature of the ACPI Active Trip Point - the point in which the OS will turn the processor fan on Active Trip Point Fan Speed.
Passive Trip Point	Disable 80 C 90 C	This value controls the temperature of the ACPI Passive Trip Point - the point in which the OS will begin throttling the processor.
Passive TC1 Value	1	This value sets the TC1 value for the ACPI Passive Cooling Formula. Range 1 – 16.
Passive TC2 Value	5	This value value sets the TC2 value for the ACPI Passive Cooling Formula. Range 1 - 16
Passive TSP Value	10	This item sets the TSP value for the ACPI Passive Cooling Formula. It represents in tenths of a second how often the OS will read the temperature when passive cooling is enabled. Range 2 – 32.
Watchdog ACPI Even Shutdown	Disable Enable	Enable / Disable Watchdog ACPI Even Shutdown.

7.3.14. Advanced > Miscellaneous

Feature	Options	Description
High Precision Timer	Enabled Disabled	Enable/Disable the High Precision Event Timer.
Security		
BIOS Security Configuration	Submenu	
Trusted Computing	Submenu	
GPI with interrupt	Enabled Disabled	GPI with interrupt Enabled/Disabled
Intel TXT(LT) Configuration	Enabled Disabled	Enables or Disables the High Precision Event Timer.

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7.3.14.1. Advanced > Miscellaneous > BIOS Security Configuration

Feature	Options	Description
SMI Lock	**Enabled** Disabled	Enable or Disable the SMI Lock
BIOS Lock	Enabled **Disabled**	Enable or Disable the BIOS lock enable (BLE) bit
GPIO Lock	Enabled **Disabled**	Enable or Disable the GPIO lockdown
BIOS Interface Lock	**Enabled** Disabled	Enable or Disable the BIOS interface lockdown
RTC RAM Lock	Enabled **Disabled**	Enable or Disable bytes 38h-2Fh in the upper and lower 128-byte bank of the RTC RAM lockdown

7.3.14.2. Advanced > Miscellaneous > Trusted Computing

Feature	Options	Description
Security Device Support	Enabled **Disabled**	Enables or Disables BIOS support for security device. When disabled OS wil not show Security Device. TCG EFI protocol and INT1A interface will not be available

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7.4. Boot

The Boot Menu allows control of Boot features

7.4.1. Boot > Boot Configuration

Feature	Options	Description
Boot Configuration	Info only	
Setup Prompt Timeout	1	Enable / Disable the onboard SATA controllers.
Bootup NumLock State	On	Select SATA controller mode.
Quiet Boot	Disabled Enabled	Enable / Disable the PATA port. In fact this enables or disables the SATA channel on which the onboard SATA to PATA converter is attached. When set to enabled the system boot will be delayed for the time specified in PATA Port Detection Timeout if no PATA device is connected. Auto: Scan for PATA device and enable per default.
Fast Boot	Disabled Enabled	Define the maximum time to wait for drive detection on PATA port.
Boot Option Priorities	Info only	
CSM Configuration	Submenu	CSM configuration Enable/Disable, Option ROM execution settings, etc.

7.4.2. Boot > CSM Configuration

Feature	Options	Description
CSM Support	Enable Disable	Enable/Disable CSM Support
CSM16 Module Version	Info Only	
GateA20 Active	Upon Request Always	UPON Request – GA20 can be disabled using BIOS servives. Alreadys – do not allow disabling GA20; this option is useful when any RT code is executed above 1 MB.
Option ROM Messages	Force BIOS Keep current	Set display mode for Option ROM
Boot Option filter	UEFI and Legacy Legacy only UEFI only	This option controls what devices system can to boot.
Network	Do not launch Legacy UEFI	Controls the execution of UEFI and Legacy PXE OpROM.
Storage	Do not launch UEFI Legacy	Controls the execution of UEFI and Legacy Storage OpROM.
Video	Do not launch UEFI Legacy	Controls the execution of UEFI and Legacy Video OpROM.
Other PCI devices	UEFI Legacy	For PCI devices other than Network, Mass storage or Video defines which OpROM to launch.

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7.5. Security

7.5.1. Security > Password Description

Feature	Options	Description
Administrator Password	Enter password	
User Password	Enter password	
HDD Security Configuration:	Info only	
Px: xxxxxxxx	Info only	

7.6. Save & Exit

7.6.1. Save and Exit > Reset Options

Feature	Options	Description
Save Changes and Reset	Save changes and reset the system.	Save Changes and Reset
Discard Changes and Reset	Reset the system without saving any changes.	Discard Changes and Reset

7.6.2. Save and Exit > Save Options

Feature	Options	Description
Save Changes		Save Changes done so far to any of the setup options.
Discard Changes		Discard Changes done so far to any of the setup options.
Restore Defaults		Restore/Load Default values for all the setup options.
Save as User Defaults		Save the changes done so far as User Defaults.
Restore User Defaults		Restore the User Defaults to all the setup options.

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8. BIOS Checkpoints, Beep Codes

This section of this document lists checkpoints and beep codes generated by AMI Aptio BIOS. The checkpoints defined in this document are inherent to the AMIBIOS generic core, and do not include any chipset or board specific checkpoint definitions.

Checkpoints and Beep Codes Definition

A checkpoint is either a byte or word value output to I/O port 80h. The BIOS outputs checkpoints throughout bootblock and Power-On Self Test (POST) to indicate the task the system is currently executing. Checkpoints are very useful for debugging problems that occur during the preboot process.

Beep codes are used by the BIOS to indicate a serious or fatal error. They are used when an error occurs before the system video has been initialized, and generated by the system board speaker.

Aptio Boot Flow

While performing the functions of the traditional BIOS, Aptio 5.x core follows the firmware model described by the Intel Platform Innovation Framework for EFI ("the Framework"). The Framework refers the following "boot phases", which may apply to various status code & checkpoint descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization[1]
- Driver Execution Environment (DXE) – main hardware initialization[2]
- Boot Device Selection (BDS) – system setup, pre-OS user interface & selecting a bootable device (CD/DVD, HDD, USB, Network, Shell, …)

Viewing BIOS Checkpoints

Viewing all checkpoints generated by the BIOS requires a checkpoint card, also referred to as a POST Card or POST Diagnostic Card. These are PCI add-in cards that show the value of I/O port 80h on a LED display.

Some computers display checkpoints in the bottom right corner of the screen during POST. This display method is limited, since it only displays checkpoints that occur after the video card has been activated.

Keep in mind that not all computers using AMI Aptio BIOS enable this feature. In most cases, a checkpoint card is the best tool for viewing AMI Aptio BIOS checkpoints.

[1]Analogous to "bootblock" functionality of legacy BIOS
[2]Analogous to "POST" functionality in legacy BIOS

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8.1. Status Code Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

8.2. Standard Status Codes

8.2.1. SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization

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SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

8.2.2. SEC Beep Codes

None

8.2.3. PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection

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Status Code	Description
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error

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Status Code	Description
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

8.2.4. PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

8.2.5. DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)

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Status Code	Description
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect

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Status Code	Description
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM

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Status Code	Description
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

8.2.6. DXE Beep Codes

# of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

8.2.7. ACPI/ASL Checkpoint

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

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8.3. OEM-Reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

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9. Mechanical Information

9.1. Board-to-Board Connectors

To allow for different stacking heights, the receptacles for COM Express carrier boards are available in two heights: 5 mm and 8 mm. When 5 mm receptacles are chosen, the carrier board should be free of components.

Tyco 3-1827253-6

Foxconn QT002206-2131-3H

- 220-pin board-to-board connector with 0.5mm for a stacking height of 5 mm.
- This connector can be used with 5 mm through-hole standoffs (SMT type).



Tyco 3-6318491-6

Foxconn QT002206-4141-3H

- 220-pin board-to-board connector with 0.5mm for a stacking height of 8 mm.
- This connector can be used with 8 mm through-hole standoffs (SMT type).



Common Specifications

- Current capacity: 0.5A per pin
- Rated voltage: 50 VAC
- Insulation resistance: 100M or greater @ 500 VDC
- Temperature rating: -40°C ~ 85°C
- UL certification (ECBT2.E28476)
- Copper alloy (contacts)
- Housing: thermo-plastic molded compound (L.C.P.)

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9.2. Thermal Solution

9.2.1. Heat Spreaders

The function of the heat spreader is to ensure an identical mechanical profile for all COM Express modules. By using a heat spreader, the thermal solution that is built on top of the module is compatible with all COM Express modules.

9.2.2. Heat Sinks

A heat sink can be used as a thermal solution for a specific COM Express module and can have a fan or be fanless, depending on the thermal requirements.

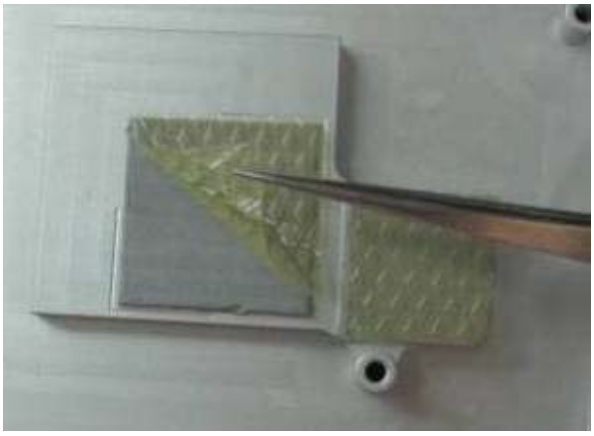
9.2.3. Installation

Install a heat spreader or heat sink using the following instructions.

Step 1: Before mounting the heatsink, install the required memory modules onto the SODIMM socket(s) on the COM Express module.



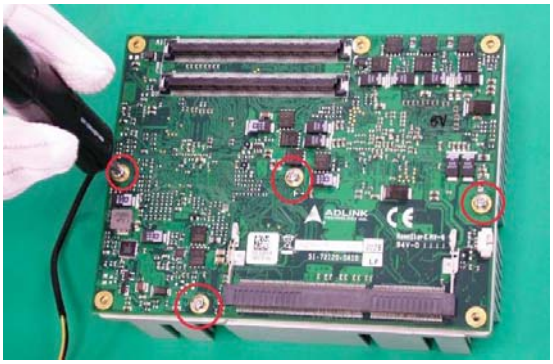
Step 2: Remove the protective membranes from the thermal pads.



Step 3: Assemble the heatsink onto the COM Express module.

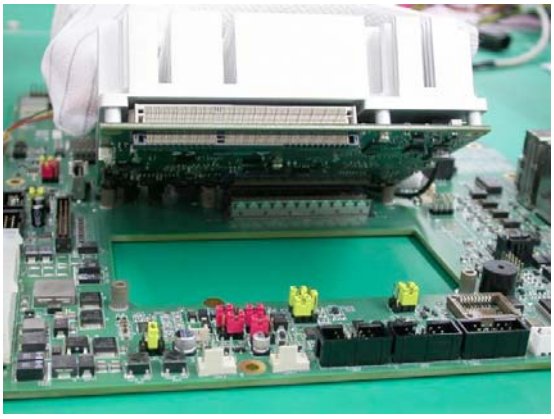
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Step 4: Use the four M2.5, L=6mm screws provided to fasten the heatsink to the module.



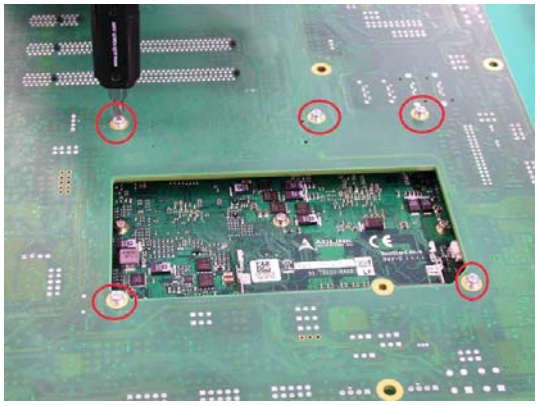


Step 5: Place the COM Express module and heatsink assembly onto the connectors on the carrier board as shown.



Then press down on the module until it is firmly seated on the carrier board.

Step 6: Use the five M2.5, L=16mm screws provided to secure the COM Express module to the carrier board from the solder side.





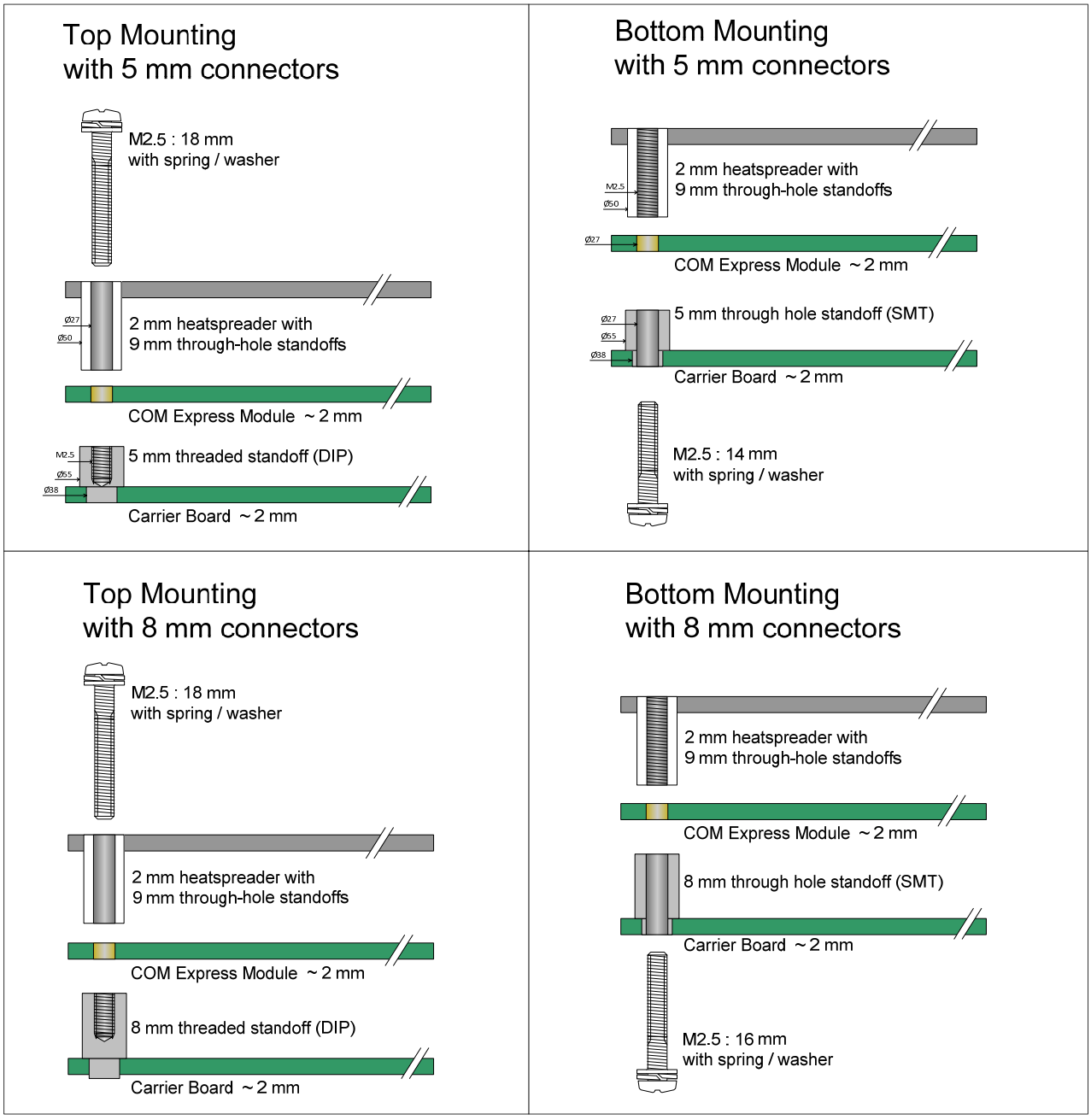
Step 7: If you are installing a heatsink with a fan, plug the fan connector into the carrier board as shown.



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9.3. Mounting Methods

There are several standard ways to mount the COM Express module with a thermal solution onto a carrier board. In addition to the choice of 5 mm or 8mm board-to-board connectors, there is the choice of Top and Bottom mounting. In Top mounting, the threaded standoffs are on the carrier board and the thermal solution is equipped with through-hole standoffs. In Bottom mounting, the threaded standoffs are on the thermal solution and the carrier board has through-hole standoffs.



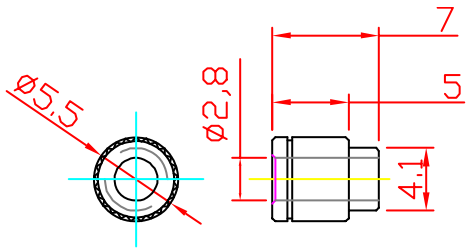
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9.4. Standoff Types

The standoffs available for Top and Bottom mounting methods are shown below. Note that threaded standoffs are DIP type and through-hole standoffs are SMT type. Other types not listed are available upon request.

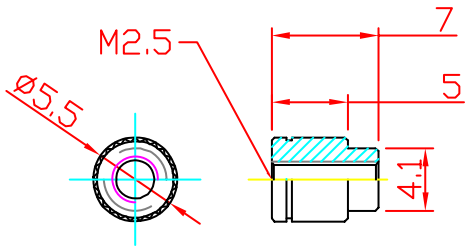
5mm through-hole standoff (SMT type)

P/N: 33-72000-0050



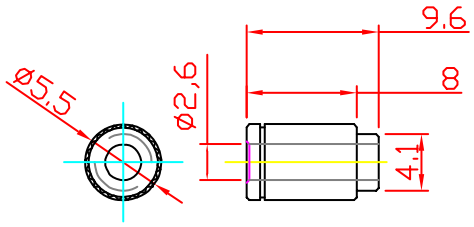
5mm threaded standoff (DIP type)

P/N: 33-72016-0050



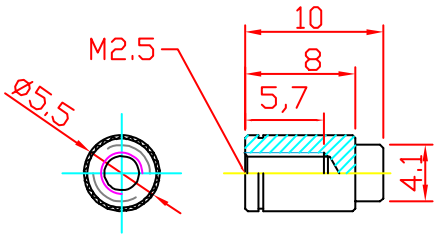
8mm through-hole standoff (SMT type)

P/N: 33-72000-0080



8mm threaded standoff (DIP type)

P/N: 33-72015-0050



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Safety Instructions

Read and follow all instructions marked on the product and in the documentation before you operate your system. Retain all safety and operating instructions for future use.

- Please read these safety instructions carefully.
- Please keep this User‘s Manual for later reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment, turn off the power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources.
  - Keep equipment away from high heat or high humidity.
  - Keep equipment properly ventilated (do not block or cover ventilation openings).
  - Make sure to use recommended voltage and power source settings.
  - Always install and operate equipment near an easily accessible electrical socket-outlet.
  - Secure the power cord (do not place any object on/over the power cord).
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings.
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.
- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

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Getting Service

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