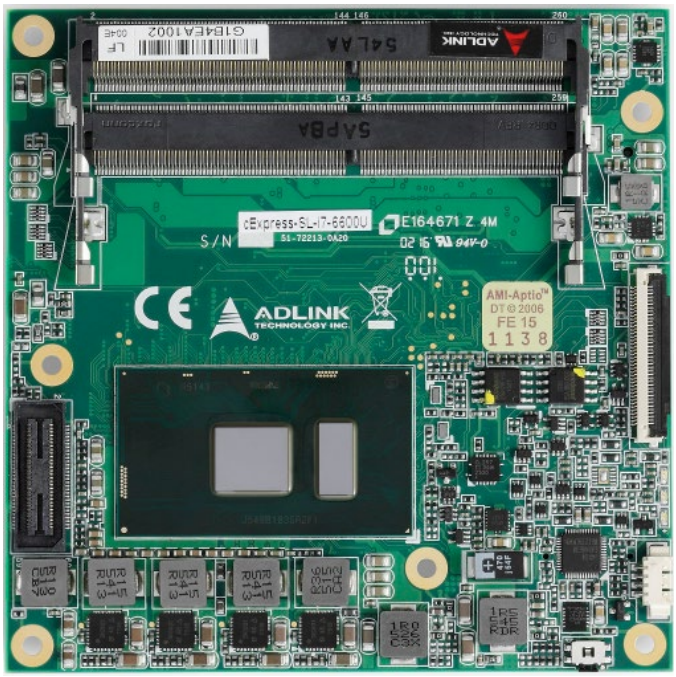
# COM Express®

## cExpress-SL

## User's Manual



Manual Revision: Rev. 1.3

Revision Date: December 4, 2024

Part Number: 50M-1J063-1030

ADLINK TECHNOLOGY INC.

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# Revision History

| Revision | Description | Date | By |
|---|---|---|---|
| 1.0 | Initial release | 2016-04-15 | JC |
| 1.1 | Correct functional diagram | 2016-04-27 | JC |
| 1.2 | Update AB/CD signal descriptions | 2016-07-20 | Alex |
| 1.3 | BIOS Setup updated | 2024-12-04 | AL |

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# Preface

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# 1. Introduction

The cExpress-SL is a COM Express® COM.0 R2.1 Type 6 Compact size module featuring the 64-bit 6th Generation Intel® Core™ i7/i5/i3 and Intel® Celeron® Ultra-Low TDP processors (formerly “Skylake-U”) with CPU, memory controller, graphics processor and I/O hub on a single chip. Leveraging the benefits provided by the 6th generation Intel® Core™ and Celeron™ System-on-Chip, the cExpress-SL is specifically designed for customers who need optimum processing and graphics performance with suitable power consumption using Intel’s Configurable TDP in a long product life solution. The cExpress-SL’s Intel® processors support Intel® Hyper-Threading Technology (up to 2 cores, 4 threads) and up to 32 GB of non-ECC DDR4 dual-channel memory at 1866/2133 MHz in dual stacked SODIMM sockets to provide excellent overall performance.

Integrated Intel® Generation 9 Low Power Graphics includes features such as OpenGL 4.4/4.3, DirectX 11.3/11, Intel® Clear Video HD Technology, Advanced Scheduler 2.0, 1.0, XPDM support, and DirectX Video Acceleration (DXVA2) support for AVC/VC1/MPEG2/HEVC/VP8/JPEG hardware decode and AVC/MPEG2/HEVC/VP8/JPEG hardware encode. Graphics outputs include dual-channel 18/24-bit LVDS (eDP by build option) and two DDI ports supporting HDMI/DVI/DisplayPort. The cExpress-SL is specifically designed for customers with high-performance processing graphics requirements who want to outsource the custom core logic of their systems for reduced development time.

The cExpress-SL features a single onboard Gigabit Ethernet port, up to six PCIe Gen3/2 ports (build option), four USB 3.0 ports, four USB 2.0 ports, and up to three SATA 6Gb/s ports. Support is provided for SMBus and I²C. The module is equipped with SPI AMI EFI BIOS with CMOS backup, supporting embedded features such as remote console, CMOS backup, hardware monitor, and watchdog timer.

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# 2. Specifications

## 2.1. Core System

- **CPU**: 6th Generation Intel® Core™ and Celeron® processor SoC (formerly "Skylake-U")
  - Intel® Core™ i7-6600U 2.6 GHz (3.4 GHz Turbo), 15W (cTDP support) (2C/GT2)
  - Intel® Core™ i5-6300U 2.4 GHz (3.0 GHz Turbo), 15W (cTDP support) (2C/GT2)
  - Intel® Core™ i3-6100U 2.3 GHz (no Turbo), 15W (cTDP support) (2C/GT2)
  - Intel® Celeron® 3955U 2.0 GHz (no Turbo), 15W (2C/GT1)

  Note: Core™ i7 and i5 GT3e SKUs are supported on a project basis only. Please contact your local sales representative.

  Supporting: Intel® VT, Intel® TXT, Intel® SSE4.2, Intel® HT Technology, Intel® 64 Architecture, Execute Disable Bit, Intel® Turbo Boost Technology 2.0, Intel® AVX2, Intel® AES-NI, PCLMULQDQ Instruction, Intel® Device Protection Technology with Intel® Secure Key, Intel® TSXNI

  **Note:** Availability of features may vary between processor SKUs.
- **L3 Cache:** 4MB for Core™ i7, 3MB for Core™ i5 and Core™ i3, 2MB for Celeron®
- **Memory:** Dual channel non-ECC 1866/2133 MHz DDR4 memory up to 32 GB in dual SODIMM socket
- **BIOS:** AMI EFI with CMOS backup in 16MB SPI BIOS with Intel® AMT 11.0 support (AMT supported on i7/i5 SKUs only)
- **Platform Controller Hub:** Integrated PCH-LP (i7/i5/i3: Premium PCH-LP, Celeron: Base PCH-LP)

## 2.2. Expansion Busses

- 5x PCI Express x1 Gen3/2 (AB): Lanes 0/1/2/3/4, supports x4, x2, x1 configuration (Core™i7/i5/i3: Gen3, Celeron®: Gen2)
  (Up to 6x PCI Express x1 Gen3/2 support by build option, in place of GbE)
- LPC bus, SMBus (system), $I^2C$ (user)

## 2.3. Video

- **Integrated on Processor:** Intel® Generation 9 Low Power Graphics core architecture
- **GPU Feature Support:**
  - 3 independent and simultaneous display combinations of DisplayPort/HDMI/LVDS monitors (eDP by build option in place of LVDS)
  - Encode/transcode HD content
  - Playback of high definition content including Blu-ray Disc
  - Playback of Blu-ray disc S3D content using HDMI (1.4a spec compliant with 3D)
  - DirectX Video Acceleration (DXVA2) support for accelerated video processing
  - AVC/VC1/MPEG2/HEVC/VP8/JPEG HW decode
  - AVC/MPEG2/HEVC/VP8/JPEG HW encode
  - Advanced Scheduler 2.0, 1.0, XPDM support
  - DirectX 11.3, OpenGL 4.4, OpenGL ES 2.0 and OpenCL 2.0
  - Multi Display Support: 3 independent displays

  **Note:** Availability of features may vary between operating systems.

- **Display Types**
  - Single/dual channel 18/24-bit LVDS via eDP-to-LVDS chip, supports DE mode and H/V-Sync mode display

    (eDP 4 lanes available as build option in place of LVDS)

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- 2x Digital Display Ports
  DDI1 supports DisplayPort/HDMI/DVI
  DDI2 supports DisplayPort/HDMI/DVI

**Note:** Supports HDMI 1.4, DP 1.2 and eDP 1.3.

## 2.4. Audio

- **Integrated:** Intel® HD Audio integrated on SoC
- **Codec:** Realtek ALC886 on Express-BASE6 Reference Carrier Board

## 2.5. LAN

- **Integrated:** MAC integrated on SoC
- **Intel PHY:** Intel® Ethernet Controller i219LM
- **Interface:** 10/100/1000 GbE connection

## 2.6. Multi I/O and Storage

- **I/O Hub:** Integrated on SOC
- **USB:** 4x USB 3.0 ports (USB0,1,2,3) and 4x USB 2.0 ports (USB4,5,6,7). All USB support by XHCI controller.

  Note: No native XHCI drivers are included with Windows 7.
- **SATA:** Up to 3x SATA 6Gb/s ports (i7/i5/i3 support port 0/1/2, Celeron supports ports 0/1 only)
- **GPIO:** 4 GPO and 4 GPI

## 2.7. Serial I/O on Module

- **Chipset:** Nuvoton NCT5104D
- **Ports:** 2x UARTs Rx/Tx only, the bit rate can support up to 115.2k bps
- **Console Redirection:** selectable in BIOS, supported during BIOS POST

| COM Port | Description | IRQ | Address | Console redirection support |
|---|---|---|---|---|
| COM 1 | Supported by module (SER0, A98/A99) via NCT5104D | 7 | 0x240 | Yes |
| COM 2 | Supported by module (SER1, A101/A102) via NCT5104D | 5 | 0x248 | Yes |
| COM 3 | Supported by Super I/O (W83627DHG) on carrier board | 4 | 0x3F8 | Yes |
| COM 4 | Supported by Super I/O (W83627DHG) on carrier board | 3 | 0x2F8 | Yes |

## 2.8. Trusted Platform Module (TPM)

- **Chipset:** Atmel AT97SC3204
- **Type:** TPM 1.2/2.0 (TPM 2.0 under development)

## 2.9. SEMA Board Controller

- **Type:** ADLINK Smart Embedded Management Agent (SEMA)
- **Functions:**
  - Voltage/Current monitoring
  - Power sequence debug support

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- AT/ATX mode control
- Logistics and forensic information
- Flat panel control
- General purpose I2C
- Failsafe BIOS (dual BIOS )
- Watchdog timer and fan control

## 2.10. Debug

- 40-pin flat cable connector to be used with DB-40 debug module
  Supports: BIOS POST code LED, BMC access, SPI BIOS flashing, power testpoints, debug LEDs
- 60-pin XDP header for ICE debug of CPU/chipset

## 2.11. Power Specifications

- **Power Modes:** AT and ATX mode (AT mode startup controlled by SEMA Board Controller)
- **Standard Voltage Input:** ATX = 12V±5% / 5Vsb ±5% or AT = 12V±5%
- **Wide Voltage Input:** ATX = 5~20 V / 5Vsb ±5% or AT = 5 ~20V
- **Power Management:** ACPI 5.0 compliant, Smart Battery support
- **Power States:** supports C1-C6, S0, S3, S4, S5 (Wake-on-USB S3/S4, WoL S3/S4/S5)
- **ECO mode:** supports deep S5 for 5Vsb power saving

## 2.12. Operating Temperatures

- **Standard Operating Temperature:** 0°C to +60°C (Wide Voltage Input)
  Storage Temperature: -20°C to +70°C
- **Extreme Rugged™ Operating Temperature (optional):** -40°C to +85°C (Standard Voltage Input)
  Storage Temperature: -40°C to +85°C

## 2.13. Environmental

- **Humidity:** 5-90% RH operating, non-condensing
  5-95% RH storage (and operating with conformal coating).
- **Shock and Vibration:** IEC 60068-2-64 and IEC-60068-2-27
  MIL-STD-202F, Method 213B, Table 213-I, Condition A and Method 214A, Table 214-I, Condition D
- **HALT:** Thermal Stress, Vibration Stress, Thermal Shock and Combined Test

## 2.14. Specification Compliance

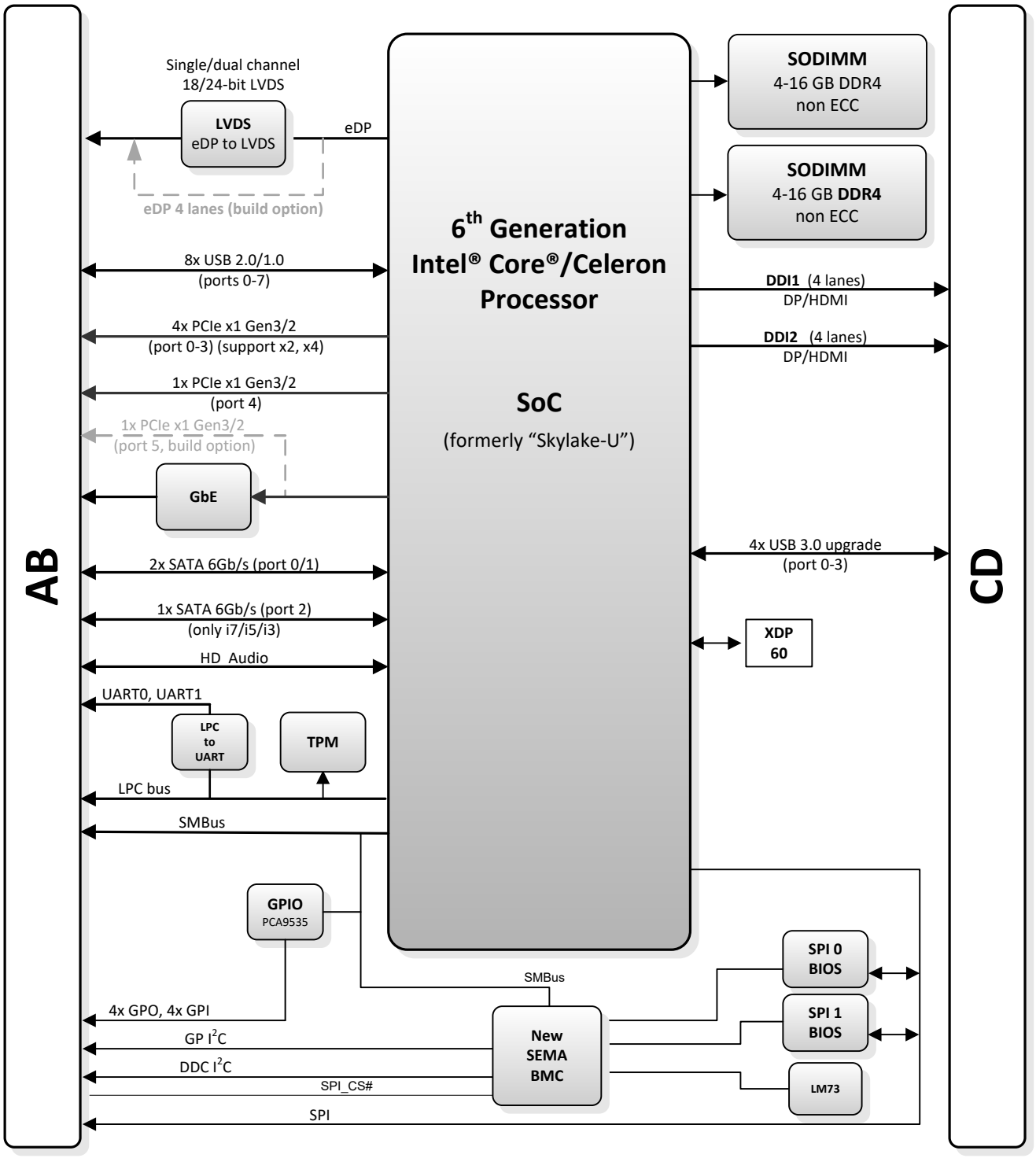
- PICMG COM.0: Rev 2.1 Type 6, Compact size 95 x 95 mm

## 2.15. Operating Systems

- **Standard Support:** Windows 10/8.1 (64-bit), Windows 7 (32/64-bit), Linux (32/64-bit), VxWorks (64-bit)
- **Extended Support (BSP):** Windows Embedded Standard 7 (WES7), Linux, VxWorks

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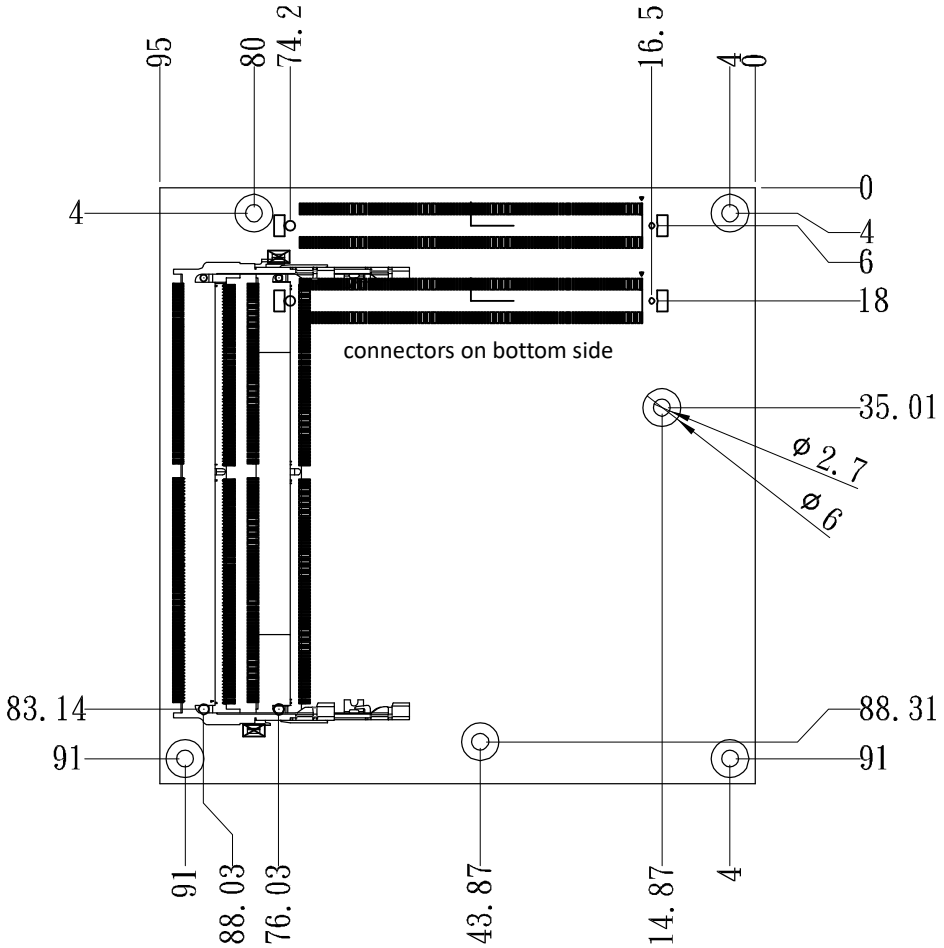
## 2.16. Functional Diagram



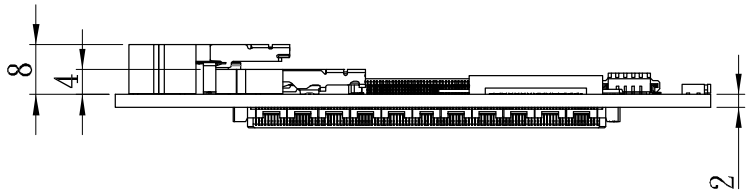

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## 2.17. Mechanical Drawing

Top View




Side View




All Ø tolerances ± 0.10 mm
Other tolerances ± 0.25 mm

Dimensions: mm

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# 3. Pinouts and Signal Descriptions

## 3.1. AB/CD Pin Definitions

The cExpress-SL is a Type 6 module supporting USB 3.0 upgrade signals and DDI channels on the CD connector

All pins in the COM Express specification are described, including those not supported on the cExpress-SL. Those not supported on the cExpress-SL module are ~~crossed out~~.

| | Row A | | Row B | | Row C | | Row D |
|---|---|---|---|---|---|---|---|
| **Pin** | **Name** | **Pin** | **Name** | **Pin** | **Name** | **Pin** | **Name** |
| **A1** | GND (FIXED) | **B1** | GND (FIXED) | **C1** | GND FIXED) | **D1** | GND FIXED) |
| **A2** | GBE0_MDI3- | **B2** | GBE0_ACT# | **C2** | GND | **D2** | GND |
| **A3** | GBE0_MDI3+ | **B3** | LPC_FRAME# | **C3** | USB_SSRX0- | **D3** | USB_SSTX0- |
| **A4** | GBE0_LINK100# | **B4** | LPC_AD0 | **C4** | USB_SSRX0+ | **D4** | USB_SSTX0+ |
| **A5** | GBE0_LINK1000# | **B5** | LPC_AD1 | **C5** | GND | **D5** | GND |
| **A6** | GBE0_MDI2- | **B6** | LPC_AD2 | **C6** | USB_SSRX1- | **D6** | USB_SSTX1- |
| **A7** | GBE0_MDI2+ | **B7** | LPC_AD3 | **C7** | USB_SSRX1+ | **D7** | USB_SSTX1+ |
| **A8** | GBE0_LINK# | **B8** | LPC_DRQ0# | **C8** | GND | **D8** | GND |
| **A9** | GBE0_MDI1- | **B9** | LPC_DRQ1# | **C9** | USB_SSRX2- | **D9** | USB_SSTX2- |
| **A10** | GBE0_MDI1+ | **B10** | LPC_CLK | **C10** | USB_SSRX2+ | **D10** | USB_SSTX2+ |
| **A11** | GND (FIXED) | **B11** | GND (FIXED) | **C11** | GND (FIXED) | **D11** | GND (FIXED) |
| **A12** | GBE0_MDI0- | **B12** | PWRBTN# | **C12** | USB_SSRX3- | **D12** | USB_SSTX3- |
| **A13** | GBE0_MDI0+ | **B13** | SMB_CK | **C13** | USB_SSRX3+ | **D13** | USB_SSTX3+ |
| **A14** | ~~GBE0_CTREF~~ | **B14** | SMB_DAT | **C14** | GND | **D14** | GND |
| **A15** | SUS_S3# | **B15** | SMB_ALERT# | **C15** | ~~DDI1_PAIR6+~~ | **D15** | DDI1_CTRLCLK_AUX+ |
| **A16** | SATA0_TX+ | **B16** | SATA1_TX+ | **C16** | ~~DDI1_PAIR6-~~ | **D16** | DDI1_CTRLDATA_AUX- |
| **A17** | SATA0_TX- | **B17** | SATA1_TX- | **C17** | RSVD | **D17** | RSVD |
| **A18** | SUS_S4# | **B18** | SUS_STAT# | **C18** | RSVD | **D18** | RSVD |
| **A19** | SATA0_RX+ | **B19** | SATA1_RX+ | **C19** | ~~PCIE_RX6+~~ | **D19** | ~~PCIE_TX6+~~ |
| **A20** | SATA0_RX- | **B20** | SATA1_RX- | **C20** | ~~PCIE_RX6-~~ | **D20** | ~~PCIE_TX6-~~ |
| **A21** | GND (FIXED) | **B21** | GND (FIXED) | **C21** | GND (FIXED) | **D21** | GND (FIXED) |
| **A22** | SATA2_TX+ | **B22** | ~~SATA3_TX+~~ | **C22** | ~~PCIE_RX7+~~ | **D22** | ~~PCIE_TX7+~~ |
| **A23** | SATA2_TX- | **B23** | ~~SATA3_TX-~~ | **C23** | ~~PCIE_RX7-~~ | **D23** | ~~PCIE_TX7-~~ |
| **A24** | SUS_S5# | **B24** | PWR_OK | **C24** | DDI1_HPD | **D24** | RSVD |
| **A25** | SATA2_RX+ | **B25** | ~~SATA3_RX+~~ | **C25** | ~~DDI1_PAIR4+~~ | **D25** | RSVD |
| **A26** | SATA2_RX- | **B26** | ~~SATA3_RX-~~ | **C26** | ~~DDI1_PAIR4-~~ | **D26** | DDI1_PAIR0+ |
| **A27** | BATLOW# | **B27** | WDT | **C27** | RSVD | **D27** | DDI1_PAIR0- |
| **A28** | (S)ATA_ACT# | **B28** | AC/HDA_SDIN2 | **C28** | RSVD | **D28** | RSVD |
| **A29** | AC/HDA_SYNC | **B29** | AC/HDA_SDIN1 | **C29** | ~~DDI1_PAIR5+~~ | **D29** | DDI1_PAIR1+ |
| **A30** | AC/HDA_RST# | **B30** | AC/HDA_SDIN0 | **C30** | ~~DDI1_PAIR5-~~ | **D30** | DDI1_PAIR1- |
| **A31** | GND (FIXED) | **B31** | GND (FIXED) | **C31** | GND (FIXED) | **D31** | GND (FIXED) |
| **A32** | AC/HDA_BITCLK | **B32** | SPKR | **C32** | DDI2_CTRLCLK_AUX+ | **D32** | DDI1_PAIR2+ |
| **A33** | AC/HDA_SDOUT | **B33** | I2C_CK | **C33** | DDI2_CTRLDATA_AUX- | **D33** | DDI1_PAIR2- |
| **A34** | BIOS_DIS0# | **B34** | I2C_DAT | **C34** | DDI2_DDC_AUX_SEL | **D34** | DDI1_DDC_AUX_SEL |
| **A35** | THRMTRIP# | **B35** | THRM# | **C35** | RSVD | **D35** | RSVD |

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| Row A | | Row B | | Row C | | Row D | |
|---|---|---|---|---|---|---|---|
| **Pin** | **Name** | **Pin** | **Name** | **Pin** | **Name** | **Pin** | **Name** |
| **A36** | USB6- | **B36** | USB7- | **C36** | ~~DDI3_CTRLCLK_AUX+~~ | **D36** | DDI1_PAIR3+ |
| **A37** | USB6+ | **B37** | USB7+ | **C37** | ~~DDI3_CTRLDATA_AUX-~~ | **D37** | DDI1_PAIR3- |
| **A38** | USB_6_7_OC# | **B38** | USB_4_5_OC# | **C38** | ~~DDI3_DDC_AUX_SEL~~ | **D38** | RSVD |
| **A39** | USB4- | **B39** | USB5- | **C39** | ~~DDI3_PAIR0+~~ | **D39** | DDI2_PAIR0+ |
| **A40** | USB4+ | **B40** | USB5+ | **C40** | ~~DDI3_PAIR0-~~ | **D40** | DDI2_PAIR0- |
| **A41** | GND (FIXED) | **B41** | GND (FIXED) | **C41** | GND (FIXED) | **D41** | GND (FIXED) |
| **A42** | USB2- | **B42** | USB3- | **C42** | ~~DDI3_PAIR1+~~ | **D42** | DDI2_PAIR1+ |
| **A43** | USB2+ | **B43** | USB3+ | **C43** | ~~DDI3_PAIR1-~~ | **D43** | DDI2_PAIR1- |
| **A44** | USB_2_3_OC# | **B44** | USB_0_1_OC# | **C44** | ~~DDI3_HPD~~ | **D44** | DDI2_HPD |
| **A45** | USB0- | **B45** | USB1- | **C45** | RSVD | **D45** | RSVD |
| **A46** | USB0+ | **B46** | USB1+ | **C46** | ~~DDI3_PAIR2+~~ | **D46** | DDI2_PAIR2+ |
| **A47** | VCC_RTC | **B47** | EXCD1_PERST# | **C47** | ~~DDI3_PAIR2-~~ | **D47** | DDI2_PAIR2- |
| **A48** | EXCD0_PERST# | **B48** | EXCD1_CPPE# | **C48** | RSVD | **D48** | RSVD |
| **A49** | EXCD0_CPPE# | **B49** | SYS_RESET# | **C49** | ~~DDI3_PAIR3+~~ | **D49** | DDI2_PAIR3+ |
| **A50** | LPC_SERIRQ | **B50** | CB_RESET# | **C50** | ~~DDI3_PAIR3-~~ | **D50** | DDI2_PAIR3- |
| **A51** | GND (FIXED) | **B51** | GND (FIXED) | **C51** | GND (FIXED) | **D51** | GND (FIXED) |
| **A52** | ~~PCIE_TX5+~~ | **B52** | ~~PCIE_RX5+~~ | **C52** | ~~PEG_RX0+~~ | **D52** | ~~PEG_TX0+~~ |
| **A53** | ~~PCIE_TX5-~~ | **B53** | ~~PCIE_RX5-~~ | **C53** | ~~PEG_RX0-~~ | **D53** | ~~PEG_TX0-~~ |
| **A54** | GPI0 | **B54** | GPO1 | **C54** | TYPE0# | **D54** | PEG_LANE_RV# |
| **A55** | PCIE_TX4+ | **B55** | PCIE_RX4+ | **C55** | ~~PEG_RX1+~~ | **D55** | ~~PEG_TX1+~~ |
| **A56** | PCIE_TX4- | **B56** | PCIE_RX4- | **C56** | ~~PEG_RX1-~~ | **D56** | ~~PEG_TX1-~~ |
| **A57** | GND | **B57** | GPO2 | **C57** | TYPE1# | **D57** | TYPE2# |
| **A58** | PCIE_TX3+ | **B58** | PCIE_RX3+ | **C58** | ~~PEG_RX2+~~ | **D58** | ~~PEG_TX2+~~ |
| **A59** | PCIE_TX3- | **B59** | PCIE_RX3- | **C59** | ~~PEG_RX2-~~ | **D59** | ~~PEG_TX2-~~ |
| **A60** | GND (FIXED) | **B60** | GND (FIXED) | **C60** | GND (FIXED) | **D60** | GND (FIXED) |
| **A61** | PCIE_TX2+ | **B61** | PCIE_RX2+ | **C61** | ~~PEG_RX3+~~ | **D61** | ~~PEG_TX3+~~ |
| **A62** | PCIE_TX2- | **B62** | PCIE_RX2- | **C62** | ~~PEG_RX3-~~ | **D62** | ~~PEG_TX3-~~ |
| **A63** | GPI1 | **B63** | GPO3 | **C63** | RSVD | **D63** | RSVD |
| **A64** | PCIE_TX1+ | **B64** | PCIE_RX1+ | **C64** | RSVD | **D64** | RSVD |
| **A65** | PCIE_TX1- | **B65** | PCIE_RX1- | **C65** | ~~PEG_RX4+~~ | **D65** | ~~PEG_TX4+~~ |
| **A66** | GND | **B66** | WAKE0# | **C66** | ~~PEG_RX4-~~ | **D66** | ~~PEG_TX4-~~ |
| **A67** | GPI2 | **B67** | WAKE1# | **C67** | RSVD | **D67** | GND |
| **A68** | PCIE_TX0+ | **B68** | PCIE_RX0+ | **C68** | ~~PEG_RX5+~~ | **D68** | ~~PEG_TX5+~~ |
| **A69** | PCIE_TX0- | **B69** | PCIE_RX0- | **C69** | ~~PEG_RX5-~~ | **D69** | ~~PEG_TX5-~~ |
| **A70** | GND (FIXED) | **B70** | GND (FIXED) | **C70** | GND (FIXED) | **D70** | GND (FIXED) |
| **A71** | LVDS_A0+ (eDP_TX2+)* | **B71** | LVDS_B0+ | **C71** | ~~PEG_RX6+~~ | **D71** | ~~PEG_TX6+~~ |
| **A72** | LVDS_A0- (eDP_TX2+)* | **B72** | LVDS_B0- | **C72** | ~~PEG_RX6-~~ | **D72** | ~~PEG_TX6-~~ |
| **A73** | LVDS_A1+ (eDP_TX1+ )* | **B73** | LVDS_B1+ | **C73** | GND | **D73** | GND |
| **A74** | LVDS_A1- (eDP_TX1- )* | **B74** | LVDS_B1- | **C74** | ~~PEG_RX7+~~ | **D74** | ~~PEG_TX7+~~ |
| **A75** | LVDS_A2+ (eDP_TX0+ )* | **B75** | LVDS_B2+ | **C75** | ~~PEG_RX7-~~ | **D75** | ~~PEG_TX7-~~ |
| **A76** | LVDS_A2- (eDP_TX0- )* | **B76** | LVDS_B2- | **C76** | GND | **D76** | GND |
| **A77** | LVDS_VDD_EN (eDP_VDD_EN)* | **B77** | LVDS_B3+ | **C77** | RSVD | **D77** | RSVD |
| **A78** | LVDS_A3+ | **B78** | LVDS_B3- | **C78** | ~~PEG_RX8+~~ | **D78** | ~~PEG_TX8+~~ |
| **A79** | LVDS_A3- | **B79** | LVDS_BKLT_EN (eDP_BKLT_EN)* | **C79** | ~~PEG_RX8-~~ | **D79** | ~~PEG_TX8-~~ |

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| | Row A | | Row B | | Row C | | Row D |
|---|---|---|---|---|---|---|---|
| **Pin** | **Name** | **Pin** | **Name** | **Pin** | **Name** | **Pin** | **Name** |
| **A80** | GND (FIXED) | **B80** | GND (FIXED) | **C80** | GND (FIXED) | **D80** | GND (FIXED) |
| **A81** | LVDS_A_CK+ (eDP_TX3+) | **B81** | LVDS_B_CK+ | **C81** | ~~PEG_RX9+~~ | **D81** | ~~PEG_TX9+~~ |
| **A82** | LVDS_A_CK- (eDP_TX3-) | **B82** | LVDS_B_CK- | **C82** | ~~PEG_RX9-~~ | **D82** | ~~PEG_TX9-~~ |
| **A83** | LVDS_I2C_CK /eDP_AUX+ * | **B83** | LVDS_BKLT_CTRL /eDP_BKLT_CTRL * | **C83** | RSVD | **D83** | RSVD |
| **A84** | LVDS_I2C_DAT /eDP_AUX- * | **B84** | VCC_5V_SBY | **C84** | GND | **D84** | GND |
| **A85** | GPI3 | **B85** | VCC_5V_SBY | **C85** | ~~PEG_RX10+~~ | **D85** | ~~PEG_TX10+~~ |
| **A86** | RSVD | **B86** | VCC_5V_SBY | **C86** | ~~PEG_RX10-~~ | **D86** | ~~PEG_TX10-~~ |
| **A87** | RSVD /eDP_HPD * | **B87** | VCC_5V_SBY | **C87** | GND | **D87** | GND |
| **A88** | PCIE0_CK_REF+ | **B88** | BIOS_DIS1# | **C88** | ~~PEG_RX11+~~ | **D88** | ~~PEG_TX11+~~ |
| **A89** | PCIE0_CK_REF- | **B89** | ~~VGA_RED~~ | **C89** | ~~PEG_RX11-~~ | **D89** | ~~PEG_TX11-~~ |
| **A90** | GND (FIXED) | **B90** | GND (FIXED) | **C90** | GND (FIXED) | **D90** | GND (FIXED) |
| **A91** | SPI_POWER | **B91** | ~~VGA_GRN~~ | **C91** | ~~PEG_RX12+~~ | **D91** | ~~PEG_TX12+~~ |
| **A92** | SPI_MISO | **B92** | ~~VGA_BLU~~ | **C92** | ~~PEG_RX12-~~ | **D92** | ~~PEG_TX12-~~ |
| **A93** | GPO0 | **B93** | ~~VGA_HSYNC~~ | **C93** | GND | **D93** | GND |
| **A94** | SPI_CLK | **B94** | ~~VGA_VSYNC~~ | **C94** | ~~PEG_RX13+~~ | **D94** | ~~PEG_TX13+~~ |
| **A95** | SPI_MOSI | **B95** | ~~VGA_I2C_CK~~ | **C95** | ~~PEG_RX13-~~ | **D95** | ~~PEG_TX13-~~ |
| **A96** | TPM_PP | **B96** | ~~VGA_I2C_DAT~~ | **C96** | GND | **D96** | GND |
| **A97** | TYPE10# | **B97** | SPI_CS# | **C97** | RSVD | **D97** | RSVD |
| **A98** | SER0_TX | **B98** | RSVD | **C98** | ~~PEG_RX14+~~ | **D98** | ~~PEG_TX14+~~ |
| **A99** | SER0_RX | **B99** | RSVD | **C99** | ~~PEG_RX14-~~ | **D99** | ~~PEG_TX14-~~ |
| **A100** | GND (FIXED) | **B100** | GND (FIXED) | **C100** | GND (FIXED) | **D100** | GND (FIXED) |
| **A101** | SER1_TX | **B101** | FAN_PWMOUT | **C101** | ~~PEG_RX15+~~ | **D101** | ~~PEG_TX15+~~ |
| **A102** | SER1_RX | **B102** | FAN_TACHIN | **C102** | ~~PEG_RX15-~~ | **D102** | ~~PEG_TX15-~~ |
| **A103** | LID# | **B103** | SLEEP# | **C103** | GND | **D103** | GND |
| **A104** | VCC_12V | **B104** | VCC_12V | **C104** | VCC_12V | **D104** | VCC_12V |
| **A105** | VCC_12V | **B105** | VCC_12V | **C105** | VCC_12V | **D105** | VCC_12V |
| **A106** | VCC_12V | **B106** | VCC_12V | **C106** | VCC_12V | **D106** | VCC_12V |
| **A107** | VCC_12V | **B107** | VCC_12V | **C107** | VCC_12V | **D107** | VCC_12V |
| **A108** | VCC_12V | **B108** | VCC_12V | **C108** | VCC_12V | **D108** | VCC_12V |
| **A109** | VCC_12V | **B109** | VCC_12V | **C109** | VCC_12V | **D109** | VCC_12V |
| **A110** | GND (FIXED) | **B110** | GND (FIXED) | **C110** | GND (FIXED) | **D110** | GND (FIXED) |

**Notes:**

(1) eDP is available as a build option in place of LVDS.
(2) Celeron SKU supports two SATA ports only
(3) PCIe port 5 is available by build option in place of GbE

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## 3.2. Signal Description Terminology

The following terms are used in the COM Express AB/CD Signal Descriptions below.

| | |
|---|---|
| I | Input to the Module |
| O | Output from the Module |
| I/O | Bi-directional input/output signal |
| OD | Open drain output |
| I 3.3V | Input 3.3V tolerant |
| I 5V | Input 5V tolerant |
| O 3.3V | Output 3.3V signal level |
| O 5V | Output 5V signal level |
| I/O 3.3V | Bi-directional signal 3.3V tolerant |
| I/O 5V | Bi-directional signal 5V tolerant |
| I/O 3.3Vsb | Input 3.3V tolerant active in standby state |
| P | Power Input/Output |
| REF | Reference voltage output that may be sourced from a module power plane. |
| PDS | Pull-down strap. This is an output pin on the module that is either tied to GND or not connected. The signal is used to indicate the PICMG module type to the Carrier Board. |
| PU | ADLINK implemented pull-up resistor on module |
| PD | ADLINK implemented pull-down resistor on module |

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## 3.3. AB Signal Descriptions

### 3.3.1. Audio Signals

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| AC_RST# / HDA_RST# | A30 | Reset output to codec, active low. | O 3.3VSB | | |
| AC_SYNC / HDA_SYNC | A29 | Sample-synchronization signal to the codec(s). | O 3.3V | | |
| AC_BITCLK / HDA_BITCLK | A32 | Serial data clock generated by the external codec(s). | I/O 3.3V | | |
| AC _SDOUT / HDA_SDOUT | A33 | Serial TDM data output to the codec. | O 3.3V | | |
| AC _SDIN[2:0] HDA_SDIN[2:0] | B28<br>B29<br>B30 | Serial TDM data inputs from up to 3 codecs. | I/O 3.3VSB | | No AC/HDA_SDIN 2 (B28) support on this platform |

### 3.3.2. Analog VGA (no VGA support)

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| VGA_RED | B89 | Red for monitor.<br>Analog DAC output, designed to drive a 37.5-Ohm equivalent load. | O Analog | | Not supported |
| VGA_GRN | B91 | Green for monitor<br>Analog DAC output, designed to drive a 37.5-Ohm equivalent load. | O Analog | | Not supported |
| VGA_BLU | B92 | Blue for monitor.<br>Analog DAC output, designed to drive a 37.5-Ohm equivalent load. | O Analog | | Not supported |
| VGA_HSYNC | B93 | Horizontal sync output to VGA monitor | O 3.3V | | Not supported |
| VGA_VSYNC | B94 | Vertical sync output to VGA monitor | O 3.3V | | Not supported |
| VGA_I2C_CK | B95 | DDC clock line (I²C port dedicated to identify VGA monitor capabilities) | I/O OD 3.3V | | Not supported |
| VGA_I2C_DAT | B96 | DDC data line. | I/O OD 3.3V | | Not supported |

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### 3.3.3. LVDS/eDP

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| LVDS_A0+<br>LVDS_A0-<br>LVDS_A1+<br>LVDS_A1-<br>LVDS_A2+<br>LVDS_A2- -<br>LVDS_A3+<br>LVDS_A3- | A71<br>A72<br>A73<br>A74<br>A75<br>A76<br>A78<br>A79 | LVDS Channel A differential pairs | O LVDS | | LVDS is default. (through eDP to LVDS bridge)<br><br>**Note:** eDP support is a build option |
| LVDS_A_CK+<br>LVDS_A_CK- | A81<br>A82 | LVDS Channel A differential clock | O LVDS | | |
| LVDS_B0+<br>LVDS_B0-<br>LVDS_B1+<br>LVDS_B1-<br>LVDS_B2+<br>LVDS_B2-<br>LVDS_B3+<br>LVDS_B3- | B71<br>B72<br>B73<br>B74<br>B75<br>B76<br>B77<br>B78 | LVDS Channel B differential pairs | O LVDS | | |
| LVDS_B_CK+<br>LVDS_B_CK- | B81<br>B82 | LVDS Channel B differential clock | O LVDS | | |
| LVDS_VDD_EN | A77 | LVDS panel power enable | O 3.3V | | |
| LVDS_BKLT_EN | B79 | LVDS panel backlight enable | O 3.3V | | |
| LVDS_BKLT_CTRL | B83 | LVDS panel backlight brightness control | O 3.3V | PD 100K | ePD to LVDS requirement |
| LVDS_I2C_CK | A83 | DDC lines used for flat panel detection and control. | O 3.3V | PU 2k2 3.3V | |
| LVDS_I2C_DAT | A84 | DDC lines used for flat panel detection and control. | I/O 3.3V | PU 2k2 3.3V | |

**eDP Build Option Signal Descriptions**

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| eDP_TX2+<br>eDP_TX2-<br>eDP_TX1+<br>eDP_TX1-<br>eDP_TX0+<br>eDP_TX0-- | A71<br>A72<br>A73<br>A74<br>A75<br>A76 | eDP differential pairs | O PCIE | | AC coupled off module |
| eDP_TX3+<br>eDP_TX3-- | A81<br>A82 | eDP differential pairs | O PCIE | | AC coupled off module |
| eDP_VDD_EN | A77 | eDP power enable | O 3.3V | | |
| eDP_BKLT_EN | B79 | eDP backlight enable | O 3.3V | | |
| eDP_BKLT_CTRL | B83 | eDP backlight brightness control | O 3.3V | PD 100K | |
| eDP_AUX+ | A83 | eDP AUX+ | I/O PCIE | | AC coupled off module |
| eDP_AUX- | A84 | eDP AUX- | I/O PCIE | | AC coupled off module |
| eDP_HPD | A87 | Detection of Hot Plug / Unplug and notification of the link layer | I 3.3V | PD 100K | |

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### 3.3.4. Gigabit Ethernet

| Gigabit Ethernet | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| GBE0_MDI0+<br>GBE0_MDI0-<br>GBE0_MDI1+<br>GBE0_MDI1-<br>GBE0_MDI2+<br>GBE0_MDI2-<br>GBE0_MDI3+<br>GBE0_MDI3- | A13<br>A12<br>A10<br>A9<br>A7<br>A6<br>A3<br>A2 | Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following:<br>1000BASE-T / 100BASE-TX / 10BASE-T<br>MDI[0]+/- B1_DA+/- TX+/- TX+/-<br>MDI[1]+/- B1_DB+/- RX+/- RX+/-<br>MDI[2]+/- B1_DC+/-<br>MDI[3]+/- B1_DD+/- | I/O Analog | | Twisted pair signals for external transformer. |
| GBE0_ACT# | B2 | Gigabit Ethernet Controller 0 activity indicator, active low. | O 3.3VSB | | |
| GBE0_LINK# | A8 | Gigabit Ethernet Controller 0 link indicator, active low. | O 3.3VSB | | |
| GBE0_LINK100# | A4 | Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low. | O 3.3VSB | | |
| GBE0_LINK1000# | A5 | Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low. | O 3.3VSB | | |
| GBE0_CTREF | A14 | Reference voltage for Carrier Board Ethernet channel 1 and 2 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be 250 mA or less. | GND min 3.3V max | | No support on this product |

### 3.3.5. Serial ATA

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| SATA0_TX+<br>SATA0_TX- | A16<br>A17 | Serial ATA channel 0, Transmit Output differential pair. | O SATA | | AC coupled on Module |
| SATA0_RX+<br>SATA0_RX- | A19<br>A20 | Serial ATA channel 0, Receive Input differential pair. | I SATA | | AC coupled on Module |
| SATA1_TX+<br>SATA1_TX- | B16<br>B17 | Serial ATA channel 1, Transmit Output differential pair. | O SATA | | AC coupled on Module |
| SATA1_RX+<br>SATA1_RX- | B19<br>B20 | Serial ATA channel 1, Receive Input differential pair. | I SATA | | AC coupled on Module |
| SATA2_TX+<br>SATA2_TX- | A22<br>A23 | Serial ATA channel 2, Transmit Output differential pair. | O SATA | | AC coupled on Module |
| SATA2_RX+<br>SATA2_RX- | A25<br>A26 | Serial ATA channel 2, Receive Input differential pair. | I SATA | | AC coupled on Module |
| SATA3_TX+<br>SATA3_TX- | B22<br>B23 | Serial ATA channel 3, Transmit Output differential pair. | O SATA | | Not supported |
| SATA3_RX+<br>SATA3_RX- | B25<br>B26 | Serial ATA channel 3, Receive Input differential pair. | I SATA | | Not supported |
| (S)ATA_ACT# | A28 | ATA (parallel and serial) or SAS activity indicator, active low. | O 3.3V | PU 10K 3.3V | |

**Note:** Core i7/i5/i3 support three SATA ports, Celeron support two SATA ports

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### 3.3.6. PCI Express

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| PCIE_TX0+<br>PCIE_TX0- | A68<br>A69 | PCI Express channel 0, Transmit Output differential pair. | O PCIE | | AC coupled on Module |
| PCIE_RX0+<br>PCIE_RX0- | B68<br>B69 | PCI Express channel 0, Receive Input differential pair. | I PCIE | | AC coupled off Module |
| PCIE_TX1+<br>PCIE_TX1- | A64<br>A65 | PCI Express channel 1, Transmit Output differential pair. | O PCIE | | AC coupled on Module |
| PCIE_RX1+<br>PCIE_RX1- | B64<br>B65 | PCI Express channel 1, Receive Input differential pair. | I PCIE | | AC coupled off Module |
| PCIE_TX2+<br>PCIE_TX2- | A61<br>A62 | PCI Express channel 2, Transmit Output differential pair. | O PCIE | | AC coupled on Module |
| PCIE_RX2+<br>PCIE_RX2- | B61<br>B62 | PCI Express channel 2, Receive Input differential pair. | I PCIE | | AC coupled off Module |
| PCIE_TX3+<br>PCIE_TX3- | A58<br>A59 | PCI Express channel 3, Transmit Output differential pair. | O PCIE | | AC coupled on Module |
| PCIE_RX3+<br>PCIE_RX3- | B58<br>B59 | PCI Express channel 3, Receive Input differential pair. | I PCIE | | AC coupled off Module |
| PCIE_TX4+<br>PCIE_TX4- | A55<br>A56 | PCI Express channel 4, Transmit Output differential pair. | O PCIE | | AC coupled on Module |
| PCIE_RX4+<br>PCIE_RX4- | B55<br>B56 | PCI Express channel 4, Receive Input differential pair. | I PCIE | | AC coupled off Module |
| PCIE_TX5+<br>PCIE_TX5- | A52<br>A53 | PCI Express channel 5, Transmit Output differential pair. | O PCIE | | PCIe port 5 is used by LAN by default. build option supports PCIe port5 |
| PCIE_RX5+<br>PCIE_RX5- | B52<br>B53 | PCI Express channel 5, Receive Input differential pair. | I PCIE | | PCIe port 5 is used by LAN by default. build option supports PCIe port5 |
| PCIE_CLK_REF+<br>PCIE_CLK_REF- | A88<br>A89 | PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes. | O PCIE | | |

### 3.3.7. Express Card

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| EXCD0_CPPE#<br>EXCD1_CPPE# | A49<br>B48 | PCI ExpressCard: PCI Express capable card request | I 3.3V | PU 10k 3.3V | |
| EXCD0_PERST#<br>EXCD1_PERST# | A48<br>B47 | PCI ExpressCard: reset | O 3.3V | | |

### 3.3.8. LPC Bus

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| LPC_AD[0:3] | B4-B7 | LPC multiplexed address, command and data bus | I/O 3.3VSB | | Skylake platform uses standby power for LPC bus |
| LPC_FRAME# | B3 | LPC frame indicates the start of an LPC cycle | O 3.3VSB | | Skylake platform uses standby power for LPC bus |

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| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| LPC_DRQ0#<br>LPC_DRQ1# | B8<br>B9 | LPC serial DMA request | I 3.3V | | NC.<br>No support on Skylake-U platform |
| LPC_SERIRQ | A50 | LPC serial interrupt | I/O OD 3.3VSB | PU 8k2 3.3V | Skylake platform uses standby power for LPC bus |
| LPC_CLK | B10 | LPC clock output - 33MHz nominal | O 3.3VSB | | Skylake platform uses standby power for LPC bus<br>The LPC_CLK frequency is 24MHz |

### 3.3.9. USB

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| USB0+<br>USB0- | A46<br>A45 | USB differential data pairs for Port 0 | I/O 3.3VSB | | USB 1.1/ 2.0 compliant |
| USB1+<br>USB1- | B46<br>B45 | USB differential data pairs for Port 1 | I/O 3.3VSB | | USB 1.1/ 2.0 compliant |
| USB2+<br>USB2- | A43<br>A42 | USB differential data pairs for Port 1 | I/O 3.3VSB | | USB 1.1/ 2.0 compliant |
| USB3+<br>USB3- | B43<br>B42 | USB differential data pairs for Port 2 | I/O 3.3VSB | | USB 1.1/ 2.0 compliant |
| USB4+<br>USB4- | A40<br>A39 | USB differential data pairs for Port 3 | I/O 3.3VSB | | USB 1.1/ 2.0 compliant |
| USB5+<br>USB5- | B40<br>B39 | USB differential data pairs for Port 4 | I/O 3.3VSB | | USB 1.1/ 2.0 compliant |
| USB6+<br>USB6- | A37<br>A36 | USB differential data pairs for Port 5 | I/O 3.3VSB | | USB 1.1/ 2.0 compliant |
| USB7+<br>USB7- | B37<br>B37 | USB differential data pairs for Port 6 | I/O 3.3VSB | | USB 1.1/ 2.0 compliant |
| USB_0_1_OC# | B44 | USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. | I 3.3VSB | PU 10k 3.3VSB | Do not pull high on carrier |
| USB_2_3_OC# | A44 | USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. . | I 3.3VSB | PU 10k 3.3VSB | Do not pull high on carrier |
| USB_4_5_OC# | B38 | USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. | I 3.3VSB | PU 10k 3.3VSB | Do not pull high on carrier |
| USB_6_7_OC# | A38 | USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. | I 3.3VSB | PU 10k 3.3VSB | Do not pull high on carrier |

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### 3.3.10. USB Root Segmentation

All USB from XHCI controller.

### 3.3.11. SPI (BIOS only)

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| SPI_CS# | B97 | Chip select for Carrier Board SPI BIOS Flash. | O 3.3VSB | PU 10K 3.3VSB | |
| SPI_MISO | A92 | Data in to module from carrier board SPI BIOS flash. | I 3.3VSB | | |
| SPI_MOSI | A95 | Data out from module to carrier board SPI BIOS flash. | O 3.3VSB | | |
| SPI_CLK | A94 | Clock from module to carrier board SPI BIOS flash. | O 3.3VSB | | |
| SPI_POWER | A91 | Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V.<br>The Module shall provide a minimum of 100mA on SPI_POWER.<br>Carriers shall use less than 100mA of SPI_POWER.<br>SPI_POWER shall only be used to power SPI devices on the Carrier | O P 3.3VSB | | |
| BIOS_DIS0# | A34 | Selection strap to determine the BIOS boot device. | I | PU 10K 3.3VSB | Carrier shall pull to GND or leave no-connect. |
| BIOS_DIS1# | B88 | Selection strap to determine the BIOS boot device. | I | PU 10K 3.3VSB | Carrier shall pull to GND or leave no-connect |

### 3.3.12. Miscellaneous

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| SPKR | B32 | Output for audio enunciator, the “speaker” in PC-AT systems | O 3.3V | PU 10K 3.3V | |
| WDT | B27 | Output indicating that a watchdog time-out event has occurred. | O 3.3V | | |
| THRM# | B35 | Input from off-module temp sensor indicating an over-temp situation. | I 3.3V | | |
| THERMTRIP# | A35 | Active low output indicating that the CPU has entered thermal shutdown. | O 3.3VSB | | |
| FAN_PWMOUT | B101 | Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan’s RPM. | O OD 3.3V | PU 2.2K 3.3V | PD shall be on the carrier board |
| FAN_TACHIN11 | B102 | Fan tachometer input for a fan with a two pulse output. | I OD 3.3V | PU 10k 3.3V | |
| TPM_PP | A96 | Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM. | I 3.3V | PD 1k 3.3V | PD is only placed when TPM is installed on module |

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### 3.3.13. SMBus

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| SMB_CK | B13 | System Management Bus bidirectional clock line. Power sourced through 5V standby rail and main power rails. | I/O OD 3.3VSB | PU 8k2 3.3VSB | |
| SMB_DAT# | B14 | System Management Bus bidirectional data line. Power sourced through 5V standby rail and main power rails. | I/O OD 3.3VSB | PU 8k2 3.3VSB | |
| SMB_ALERT# | B15 | System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 5V standby rail and main power rails. | I 3.3VSB | PU 10k 3.3VSB | |

### 3.3.14. I2C Bus

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| I2C_CK | B33 | General purpose I²C port clock output/input | I/O OD 3.3VSB | PU 2k2 3.3VSB | Sourced from SEMA BMC by default (Braswell SoC by build option) |
| I2C_DAT | B34 | General purpose I²C port data I/O line | I/O OD 3.3VSB | PU 2k2 3.3VSB | Sourced from SEMA BMC by default (Braswell SoC by build option) |

### 3.3.15. General Purpose I/O (GPIO)

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| GPO[0] | A93 | General purpose output pins. | O 3.3V | PU 10K 3.3V | After hardware RESET output low |
| GPO[1] | B54 | General purpose output pins. | O 3.3V | PU 10K 3.3V | After hardware RESET output low |
| GPO[2] | B57 | General purpose output pins. | O 3.3V | PU 10K 3.3V | After hardware RESET output low |
| GPO[3] | B63 | General purpose output pins. | O 3.3V | PU 10K 3.3V | After hardware RESET output low |
| GPI[0] | A54 | General purpose input pins. Pulled high internally on the module. | I 3.3V | PU 10K 3.3V | |
| GPI[1] | A63 | General purpose input pins. Pulled high internally on the module. | I 3.3V | PU 10K 3.3V | |
| GPI[2] | A67 | General purpose input pins. Pulled high internally on the module. | I 3.3V | PU 10K 3.3V | |
| GPI[3] | A85 | General purpose input pins. Pulled high internally on the module. | I 3.3V | PU 10K 3.3V | |

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### 3.3.16. Serial Interface Signals

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| SER0_TX | A98 | General purpose serial port transmitter (TTL level output) | O CMOS | | Power rail tolerance 5V/12V<br>PD shall be on the carrier board |
| SER0_RX | A99 | General purpose serial port receiver (TTL level input) | I CMOS | | Power rail tolerance 5V/12V |
| SER1_TX | A101 | General purpose serial port transmitter (TTL level output) | O CMOS | | Power rail tolerance 5V/12V<br>PD shall be on the carrier board |
| SER1_RX | A102 | General purpose serial port receiver (TTL level input) | I CMOS | | Power rail tolerance 5V/12V |

### 3.3.17. Power and System Management

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| PWRBTN# | B12 | Power button to bring system out of S5 (soft off), active on falling edge. | I 3.3VSB | PU 10k 3.3VSB | |
| SYS_RESET# | B49 | Reset button input. Active low request for module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. | I 3.3VSB | PU 10k 3.3VSB | |
| CB_RESET# | B50 | Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software. | O 3.3VSB | | |
| PWR_OK | B24 | Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow carrier based FPGAs or other configurable devices time to be programmed. | I 3.3V | PU 1k 3.3VSB | |
| SUS_STAT# | B18 | Indicates imminent suspend operation; used to notify LPC devices. | O 3.3VSB | | |
| SUS_S3# | A15 | Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as “PS_ON”) may be used to enable the non-standby power on a typical ATX power supply. | O 3.3VSB | | |
| SUS_S4# | A18 | Indicates system is in Suspend to Disk state. Active low output. | O 3.3VSB | | |
| SUS_S5# | A24 | Indicates system is in Soft Off state. | O 3.3VSB | | |
| WAKE0# | B66 | PCI Express wake up signal. | I 3.3VSB | PU 10k 3.3VSB | |
| WAKE1# | B67 | General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity. | I 3.3VSB | PU 10k 3.3VSB | Not supported. Connected to WAKE0# |
| BATLOW# | A27 | Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event. | I 3.3VSB | PU 10k 3.3VSB | |
| LID# | A103 | LID button. Low active signal used by the ACPI operating system for a LID switch. | I OD 3.3VSB | PU 10k 3.3VSB | Emulated on GPIO (BIOS) |
| SLEEP# | B103 | Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again. | I OD 3.3VSB | PU 10K 3.3VSB | Emulated on GPIO (BIOS) |

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### 3.3.18. Power and Ground

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| VCC_12V | A104-A109<br>B104-B109 | Primary power input: +12V nominal (5 ~ 20V wide input).<br>All available VCC_12V pins on the connector(s) shall be used. | P | | 5~20 V |
| VCC_5V_SBY | B84-B87 | Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design. | P | | 5Vsb ±5% |
| VCC_RTC | A47 | Real-time clock circuit-power input. Nominally +3.0V. | P | | |
| GND | A1, A11, A21, A31, A41, A51, A57, A66, A80, A90, A96, A100, A110, B1, B11, B21 ,B31, B41, B51, B60, B70, B80, B90, B100, B110 | Ground - DC power and signal and AC signal return path. | P | | |

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## 3.4. CD Signal Descriptions

### 3.4.1. USB 3.0 extension

| Signal | Pin | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| USB_SSRX0-<br>USB_SSRX0+ | C3<br>C4 | Additional Receive signal differential pairs for the SuperSpeed USB data path on USB0 | I PCIE | | AC coupled off Module |
| USB_SSTX0-<br>USB_SSTX0+ | D3<br>D4 | Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB0 | O PCIE | | AC coupled on Module |
| USB_SSRX1-<br>USB_SSRX1+ | C6<br>C7 | Additional Receive signal differential pairs for the SuperSpeed USB data path on USB1 | I PCIE | | AC coupled off Module |
| USB_SSTX1-<br>USB_SSTX1+ | D6<br>D7 | Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB1 | O PCIE | | AC coupled on Module |
| USB_SSRX2-<br>USB_SSRX2+ | C9<br>C10 | Additional Receive signal differential pairs for the SuperSpeed USB data path on USB2 | I PCIE | | AC coupled off Module |
| USB_SSTX2-<br>USB_SSTX2+ | D9<br>D10 | Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB2 | O PCIE | | AC coupled on Module |
| USB_SSRX3-<br>USB_SSRX3+ | C12<br>C13 | Additional Receive signal differential pairs for the SuperSpeed USB data path on USB3 | I PCIE | | AC coupled off Module |
| USB_SSTX3-<br>USB_SSTX3+ | D12<br>D13 | Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB3 | O PCIE | | AC coupled on Module |

### 3.4.2. PCI Express x1

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| PCIE_TX6+<br>PCIE_TX6- | D19<br>D20 | PCI Express channel 6, Transmit Output differential pair. | O PCIE | | Not supported |
| PCIE_RX6+<br>PCIE_RX6- | C19<br>C20 | PCI Express channel 6, Receive Input differential pair. | I PCIE | | Not supported |
| PCIE_TX7+<br>PCIE_TX7- | D22<br>D23 | PCI Express channel 7, Transmit Output differential pair. | O PCIE | | Not supported |
| PCIE_RX7+<br>PCIE_RX7- | C22<br>C23 | PCI Express channel 7, Receive Input differential pair. | I PCIE | | Not supported |

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### 3.4.3. DDI Channels

**DDI 1**

| Signal | Pin | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| DDI1_PAIR0+<br>DDI1_PAIR0-<br>DDI1_PAIR1+<br>DDI1_PAIR1-<br>DDI1_PAIR2+<br>DDI1_PAIR2-<br>DDI1_PAIR3+<br>DDI1_PAIR3-<br>DDI1_PAIR4+<br>DDI1_PAIR4-<br>DDI1_PAIR5+<br>DDI1_PAIR5-<br>DDI1_PAIR6+<br>DDI1_PAIR6- | D26<br>D27<br>D29<br>D30<br>D32<br>D33<br>D36<br>D37<br>C25<br>C26<br>C29<br>C30<br>C15<br>C16 | Digital Display Interface1 differential pairs | O PCIE | | Pair 4 to Pair 6<br>Not supported |
| DDI1_HPD | C24 | Digital Display Interface Hot-Plug Detect | I PCIE | PD 100K | |
| DDI1_CTRLCLK_AUX+ | D15 | IF DDI1_DDC_AUX_SEL is floating | I/O PCIe | PD 100K | DP1_AUX+<br>AC coupled on Module |
| | | IF DDI1_DDC_AUX_SEL pulled high | I/O OD 3.3V | | HDMI1_CTRLCLK<br>PU 2.2k 3.3V |
| DDI1_CTRLDATA_AUX- | D16 | IF DDI1_DDC_AUX_SEL is floating | I/O PCIe | PU 100K 3.3V | DP1_AUX-<br>AC coupled on Module |
| | | IF DDI1_DDC_AUX_SEL pulled high | I/O OD 3.3V | | HDMI1_CTRLDATA<br>PU 2.2k 3.3V |
| DDI1_DDC_AUX_SEL | D34 | Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals. | I/O OD 3.3V | PD 1M | |

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**DDI 2**

| Signal | Pin | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| DDI2_PAIR0+<br>DDI2_PAIR0-<br>DDI2_PAIR1+<br>DDI2_PAIR1-<br>DDI2_PAIR2+<br>DDI2_PAIR2-<br>DDI2_PAIR3+<br>DDI2_PAIR3- | D39<br>D40<br>D42<br>D43<br>D46<br>D47<br>D49<br>D50 | Digital Display Interface2 differential pairs | | | |
| DDI2_HPD | D44 | | | PD<br>100K | |
| DDI2_CTRLCLK_AUX+ | C32 | IF DDI2_DDC_AUX_SEL is floating | I/O PCIe | PD<br>100K | DP2_AUX+<br>AC coupled on Module |
| | | IF DDI2_DDC_AUX_SEL pulled high | I/O OD 3.3V | | HDMI2_CTRLCLK<br>PU 2.2k 3.3V |
| DDI2_CTRLDATA_AUX- | C33 | IF DDI2_DDC_AUX_SEL is floating | I/O PCIe | PU<br>100K<br>3.3V | DP2_AUX-<br>AC coupled on Module |
| | | IF DDI2_DDC_AUX_SEL pulled high | I/O OD 3.3V | | HDMI2_CTRLDATA<br>PU 2.2k 3.3V |
| DDI2_DDC_AUX_SEL | C34 | Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals. | | PD 1M | |

**DDI 3** (no DDI3 support)

| Signal | Pin | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| DDI3_PAIR0+<br>DDI3_PAIR0-<br>DDI3_PAIR1+<br>DDI3_PAIR1-<br>DDI3_PAIR2+<br>DDI3_PAIR2-<br>DDI3_PAIR3+<br>DDI3_PAIR3- | C39<br>C40<br>C42<br>C43<br>C46<br>C47<br>C49<br>C50 | Digital Display Interface3 differential pairs | | | Not supported |
| DDI3_HPD | C44 | | | PD<br>100K | Not supported |
| DDI3_CTRLCLK_AUX+ | C36 | IF DDI3_DDC_AUX_SEL is floating | I/O PCIe | | Not supported |
| | | IF DDI3_DDC_AUX_SEL pulled high | I/O OD 3.3V | | Not supported |
| DDI3_CTRLDATA_AUX- | C37 | IF DDI3_DDC_AUX_SEL is floating | I/O PCIe | | Not supported |
| | | IF DDI3_DDC_AUX_SEL pulled high | I/O OD 3.3V | | Not supported |
| DDI3_DDC_AUX_SEL | C38 | Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals. | | PD 1M | Not supported |

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### 3.4.4. DDI to DP/HDMI/SDVO Mapping

| Pin | Pin Name | DP | HDMI \ DVI |
|---|---|---|---|
| D26 | DDI1_PAIR0+ | DP1_LANE0+ | TMDS1_DATA2+ |
| D27 | DDI1_PAIR0- | DP1_LANE0- | TMDS1_DATA2- |
| D29 | DDI1_PAIR1+ | DP1_LANE1+ | TMDS1_DATA1+ |
| D30 | DDI1_PAIR1- | DP1_LANE1- | TMDS1_DATA1- |
| D32 | DDI1_PAIR2+ | DP1_LANE2+ | TMDS1_DATA0+ |
| D33 | DDI1_PAIR2- | DP1_LANE2- | TMDS1_DATA0- |
| D36 | DDI1_PAIR3+ | DP1_LANE3+ | TMDS1_CLK+ |
| D37 | DDI1_PAIR3- | DP1_LANE3- | TMDS1_CLK- |
| C25 | DDI1_PAIR4+ | Not supported | Not supported |
| C26 | DDI1_PAIR4- | Not supported | Not supported |
| C29 | DDI1_PAIR5+ | Not supported | Not supported |
| C30 | DDI1_PAIR5- | Not supported | Not supported |
| C15 | DDI1_PAIR6+ | Not supported | Not supported |
| C16 | DDI1_PAIR6- | Not supported | Not supported |
| C24 | DDI1_HPD | DP1_HPD | HDMI1_HPD |
| D15 | DDI1_CTRLCLK_AUX+ | DP1_AUX+ | HMDI1_CTRLCLK |
| D16 | DDI1_CTRLDATA_AUX- | DP1_AUX- | HMDI1_CTRLDATA |
| D34 | DDI1_DDC_AUX_SEL | | |
| D39 | DDI2_PAIR0+ | DP2_LANE0+ | TMDS2_DATA2+ |
| D40 | DDI2_PAIR0- | DP2_LANE0- | TMDS2_DATA2- |
| D42 | DDI2_PAIR1+ | DP2_LANE1+ | TMDS2_DATA1+ |
| D43 | DDI2_PAIR1- | DP2_LANE1- | TMDS2_DATA1- |
| D46 | DDI2_PAIR2+ | DP2_LANE2+ | TMDS2_DATA0+ |
| D47 | DDI2_PAIR2- | DP2_LANE2- | TMDS2_DATA0- |
| D49 | DDI2_PAIR3+ | DP2_LANE3+ | TMDS2_CLK+ |
| D50 | DDI2_PAIR3- | DP2_LANE3- | TMDS2_CLK- |
| D44 | DDI2_HPD | DP2_HPD | HDMI2_HPD |
| C32 | DDI2_CTRLCLK_AUX+ | DP2_AUX+ | HDMI2_CTRLCLK |
| C33 | DDI2_CTRLDATA_AUX- | DP2_AUX- | HDMI2_CTRLDATA |
| C34 | DDI2_DDC_AUX_SEL | | |

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### 3.4.5. PCI Express Graphics x16 (no PEG support)

| Signal | Pin | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| PEG_RX0+<br>PEG_RX0-<br>PEG_RX1+<br>PEG_RX1-<br>PEG_RX2+<br>PEG_RX2-<br>PEG_RX3+<br>PEG_RX3-<br>PEG_RX4+<br>PEG_RX4-<br>PEG_RX5+<br>PEG_RX5-<br>PEG_RX6+<br>PEG_RX6-<br>PEG_RX7+<br>PEG_RX7-<br>PEG_RX8+<br>PEG_RX8-<br>PEG_RX9+<br>PEG_RX9-<br>PEG_RX10+<br>PEG_RX10-<br>PEG_RX11+<br>PEG_RX11-<br>PEG_RX12+<br>PEG_RX12-<br>PEG_RX13+<br>PEG_RX13-<br>PEG_RX14+<br>PEG_RX14-<br>PEG_RX15+<br>PEG_RX15 | C52<br>C53<br>C55<br>C56<br>C58<br>C59<br>C61<br>C62<br>C65<br>C66<br>C68<br>C69<br>C71<br>C72<br>C74<br>C75<br>C78<br>C79<br>C81<br>C82<br>C85<br>C86<br>C88<br>C89<br>C91<br>C92<br>C94<br>C95<br>C98<br>C99<br>C101<br>C102 | PCI Express Graphics transmit differential pairs. | I PCIE | | Not supported |
| PEG_TX0+<br>PEG_TX0-<br>PEG_TX1+<br>PEG_TX1-<br>PEG_TX2+<br>PEG_TX2-<br>PEG_TX3+<br>PEG_TX3-<br>PEG_TX4+<br>PEG_TX4-<br>PEG_TX5+<br>PEG_TX5-<br>PEG_TX6+<br>PEG_TX6-<br>PEG_TX7+<br>PEG_TX7-<br>PEG_TX8+<br>PEG_TX8-<br>PEG_TX9+<br>PEG_TX9-<br>PEG_TX10+<br>PEG_TX10-<br>PEG_TX11+<br>PEG_TX11-<br>PEG_TX12+<br>PEG_TX12-<br>PEG_TX13+<br>PEG_TX13-<br>PEG_TX14+<br>PEG_TX14- | D52<br>D53<br>D55<br>D56<br>D58<br>D57<br>D61<br>D62<br>D65<br>D66<br>D68<br>D69<br>D71<br>D72<br>D74<br>D75<br>D78<br>D79<br>D81<br>D82<br>D85<br>D86<br>D88<br>D89<br>D91<br>D92<br>D94<br>D95<br>D98<br>D99 | PCI Express Graphics receive differential pairs. | O PCIE | | Not supported |

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| Signal | Pin | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| PEG_TX15+<br>PEG_TX15- | D101<br>D102 | | | | |
| PEG_LANE_RV# | D54 | PCI Express Graphics lane reversal input strap.<br>Pull low on the Carrier board to reverse lane order. | I 1.05V | | Not supported |

### 3.4.6. Module Type Definition

| Signal | Pin # | Description | I/O | Comment |
|---|---|---|---|---|
| TYPE0#<br>TYPE1#<br>TYPE2# | C54<br>C57<br>D57 | The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pinout Type 1, these pins are don't care (X).<br>TYPE2# TYPE1# TYPE0#<br>X X X Pinout Type 1<br>NC NC NC Pinout Type 2<br>NC NC GND Pinout Type 3 (no IDE)<br>NC GND NC Pinout Type 4 (no PCI)<br>NC GND GND Pinout Type 5 (no IDE, no PCI)<br>**GND NC NC Pinout Type 6 (no IDE, no PCI)**<br>The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED. | | Type 6 |

### 3.4.7. Power and Ground

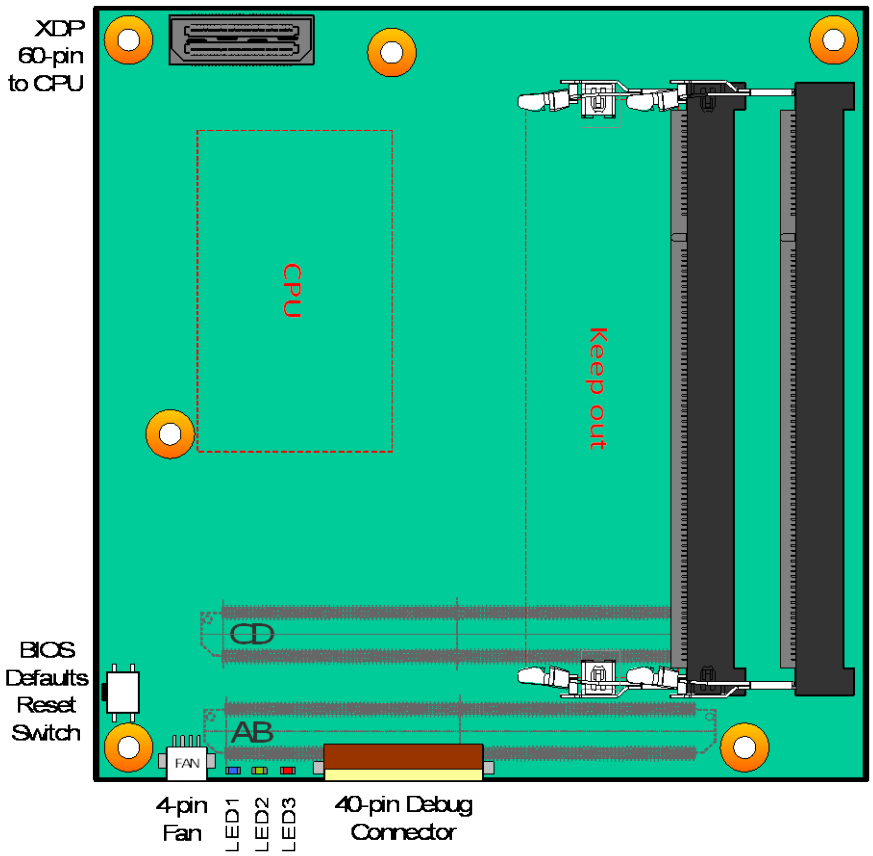
| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---|---|---|---|---|---|
| VCC_12V | C104-C109<br>D104-D109 | Primary power input: +12V nominal (5 ~ 20V wide input).<br>All available VCC_12V pins on the connector(s) shall be used. | P | | 5~20 V |
| GND | C1, C11, C21, C31, C41, C51, C60, C70, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D11, D21, D31, D41, D51, D60, D67, D70, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110 | Ground - DC power and signal and AC signal return path.<br>All available GND connector pins shall be used and tied to carrier board GND plane. | P | | |

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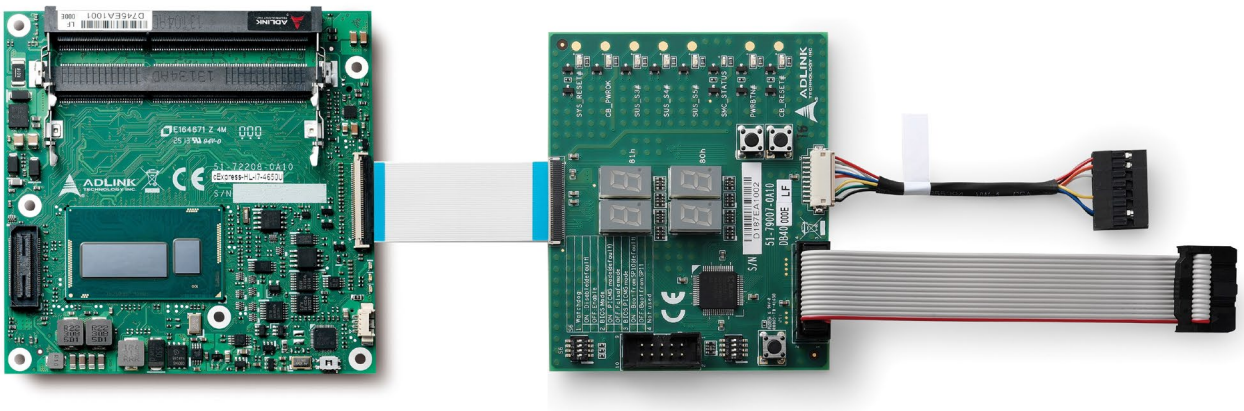
# 4. Connector Pinouts on Module

This chapter describes connectors and pinouts, LEDs and switches that are used on the module but are not included in the PICMG standard specification

## 4.1. Connector, Switch and LED Locations



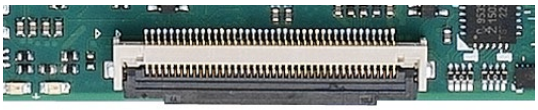

➢ **cExpress-SL and the DB40 Debug Module**



For illustration purposes only

## 4.2. 40-pin Debug Connector

- **FPC Connector Type:** FCI 59GF Flex 10042867
- **Pin Orientation**



1 40

- **40-pin Debug Connector Pin Definition on the COM Express Module**

| Pin | Interface | Signal | Remark |
|---|---|---|---|
| 1 | SPI Program interface | VCC_SPI_IN | SPI Power Input from flash tool to module. HW need add MOS FET to switch SPI power for SPI ROM |
| 2 | | GND | |
| 3 | | SPI_BIOS_CS0# | |
| 4 | | SPI_BIOS_CS1# | |
| 5 | | SPI_BIOS_MISO | |
| 6 | | SPI_BIOS_MOSI | |
| 7 | | SPI_BIOS_CLK | |
| 8 | LPC Bus | 3V3_LPC | System power 3.3V provide from COM module |
| 9 | | GND | |
| 10 | | BIOS_DIS0 | |
| 11 | | RST# | |
| 12 | | CLK33_LPC | |
| 13 | | LPC_FRAME# | |
| 14 | | LPC_AD3 | |
| 15 | | LPC_AD2 | |
| 16 | | LPC_AD1 | always power 3.3V provide from COM module |
| 17 | | LPC_AD0 | |
| 18 | BMC Program interface | 3.3V_BMC | always power 3.3V provide from COM module |
| 19 | | 3.3V_BMC | always power 3.3V provide from COM module |
| 20 | | GND | |

| Pin | Interface | Signal | Remark |
|---|---|---|---|
| 21 | BMC Program interface (continued) | TXD6 | |
| 22 | | RXD6 | |
| 23 | | FUMD0 | |
| 24 | | RESET_IN# | |
| 25 | | DATA | |
| 26 | | CLK | |
| 27 | | OCD0A | Include a jumper to connect OCD0A via 1K0 pull-up to 3.3V_BMC |
| 28 | | OCD0B | Include a jumper to connect OCD0A via 1K0 pull-up to 3.3V_BMC |
| 29 | Test points | PWRBTN# | |
| 30 | | SYS_RESET# | |
| 31 | | CB_RESET# | |
| 32 | | CB_PWROK | |
| 33 | | SUS_S3# | |
| 34 | | SUS_S4# | |
| 35 | | SUS_S5# | |
| 36 | BMC Debug signals | POSTWDT_DIS# | Connect to Jumper for Debug |
| 37 | | SEL_BIOS | Connect to Jumper for Debug |
| 38 | | BIOS_MODE | Connect to Jumper for Debug |
| 39 | | BMC_STATUS | |
| 40 | Reserved | | |

**Note:** The pin definition on the debug module is the inverse of that on the COM Express module.

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## 4.3. Status LEDs

To facilitate easier maintenance, status LED's are mounted on the board.



LED1 LED2 LED3

➢ **LED Descriptions**

| Name | Color | Connection | Function |
|---|---|---|---|
| LED1 | Blue | BMC output | Power Sequence Status Code (BMC)<br>Power Changes, RESET<br><br>(see 5.1.4 Exception Codes below) |
| LED2 | Green | Power Source 3Vcc | S0 LED ON<br>S3/S4/S5 LED OFF<br>ECO mode LED OFF |
| LED3 | Red | BMC output<br><br>and same signal as WDT (B27) on BtB connector | Module power up WD LED = LED OFF<br>Watchdog counting WD LED = Keep Last State<br>Watchdog timed out WD LED = LED ON<br>Watchdog RESET WD LED = LED ON<br>Rebooted after WD RESET WD LED = LED ON<br>Rebooted after PWRBTN WD LED = LED OFF<br>Rebooted after RESET BTN WD LED = LED OFF<br><br>Note: only a RESET not initiated by the BMC can clear the WD LED (user action) |

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## 4.4. XDP Debug header

The debug port is a connection into a target-system environment that provides access to JTAG, run control, system control, and observation resources. The XDP target system connector is a Samtec™ 60-pin BSH-030-01 series connector.

| Pin | XDP Signal | Target Signal | I/O | Device |
|---|---|---|---|---|
| 1 | GND | GND | NA | |
| 3 | OBSFN_A0 | PREQ# | I/O | Processor |
| 5 | OBSFN_A1 | PRDY# | I/O | Processor |
| 7 | GND | GND | NA | |
| 9 | OBSDATA_A0 | CFG[0][2] | I/O | Processor |
| 11 | OBSDATA_A1 | CFG[1][2] | I/O | Processor |
| 13 | GND | GND | NA | |
| 15 | OBSDATA_A2 | CFG[2][2] | I/O | Processor |
| 17 | OBSDATA_A3 | CFG[3][2] | I/O | Processor |
| 19 | GND | GND | NA | |
| 21 | OBSFN_B0 | BPM#[0][1] | I/O | Processor |
| 23 | OBSFN_B1 | BPM#[1][1] | I/O | Processor |
| 25 | GND | GND | NA | |
| 27 | OBSDATA_B0 | CFG[4][2] | I/O | Processor |
| 29 | OBSDATA_B1 | CFG[5][2] | I/O | Processor |
| 31 | GND | GND | NA | |
| 33 | OBSDATA_B2 | CFG[6][2] | I/O | Processor |
| 35 | OBSDATA_B3 | CFG[7][2] | I/O | Processor |
| 37 | GND | GND | NA | |
| 39 | HOOK0 | PWRGOOD | I | System |
| 41 | HOOK11 | BP_PWRGD_RST# | O | System |
| 43 | VCC_OBS_AB | VCCIO_OUT | I | System |
| 45 | HOOK2 | PWR_DEBUG | O | Processor |
| 47 | HOOK3 | PCH_SYS_PWROK | O | System |
| 49 | GND | GND | NA | |
| 51 | SDA1 | SDA | I/O | System |
| 53 | SCL1 | SCL | I/O | System |
| 55 | TCK1 | Open | NA | |
| 57 | TCK0 | TCK | O | Processor |
| 59 | GND | GND | NA | |

| Pin | XDP Signal | Target Signal | I/O | Device |
|---|---|---|---|---|
| 2 | GND | GND | NA | |
| 4 | OBSFN_C0 | CFG[17][2] | I | Processor |
| 6 | OBSFN_C1 | CFG[16][2] | I | Processor |
| 8 | GND | GND | NA | |
| 10 | OBSDATA_C0 | CFG[8][2] | I/O | Processor |
| 12 | OBSDATA_C1 | CFG[9][2] | I/O | Processor |
| 14 | GND | GND | NA | |
| 16 | OBSDATA_C2 | CFG[10][2] | I/O | Processor |
| 18 | OBSDATA_C3 | CFG[11][2] | I/O | Processor |
| 20 | GND | GND | NA | |
| 22 | OBSFN_D0 | CFG[19][2] | I/O | Processor |
| 24 | OBSFN_D1 | CFG[18][2] | I/O | Processor |
| 26 | GND | GND | NA | |
| 28 | OBSDATA_D0 | CFG[12][2] | I | Processor |
| 30 | OBSDATA_D1 | CFG[13][2] | I | Processor |
| 32 | GND | GND | NA | |
| 34 | OBSDATA_D2 | CFG[14][2] | I/O | Processor |
| 36 | OBSDATA_D3 | CFG[15][2] | I/O | Processor |
| 38 | GND | GND | NA | |
| 40 | ITPCLK/HOOK4 | Open | NA | |
| 42 | ITPCLK#/HOOK5 | Open | NA | |
| 44 | VCC_OBS_CD | VCCIO_OUT | I | System |
| 46 | HOOK6/RESET# | PLTRSTIN# | I | System |
| 48 | HOOK7/DBR# | DBR# | O | System |
| 50 | GND | GND | NA | |
| 52 | TDO | TDO | I | Processor |
| 54 | TRSTn | TRST# | O | Processor |
| 56 | TDI | TDI | O | Processor |
| 58 | TMS | TMS | O | Processor |
| 60 | GND | GND (or XDP_PRESENT# if required) | NA | |

**Notes:**

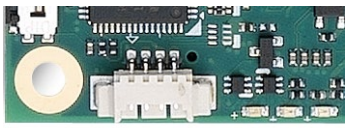
1. These signals are optional, can be left as OPEN/No-Connect if debug by Intel will not be needed.
2. These CFG signals can be left as Open/No Connect if not used as a strapping signal and top side probe will be used to debug processor.

Refer to the "Shark Bay, Denlow and Broadwell U/Y Platforms Debug Port Design Guide", Document Number: 479493, Revision: 2.0

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## 4.5. Fan Connector

- **Connector Type:** JVE 24W1125A-04M00
- Pin Orientation



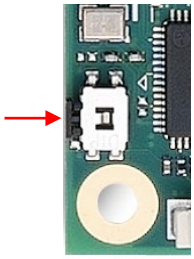
1 2 3 4

- **Pin Assignment:**

| Name | Signal | Description |
|---|---|---|
| 1 | BMC_FAN_OUT | FAN_PWMOUT |
| 2 | BMC_FAN_PWM_IN | FAN_TACHIN |
| 3 | GND | Ground |
| 4 | P5V_S | 5V |

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## 4.6. BIOS Setup Defaults Reset Button



To perform a hardware reset of BIOS default settings, perform the following steps:

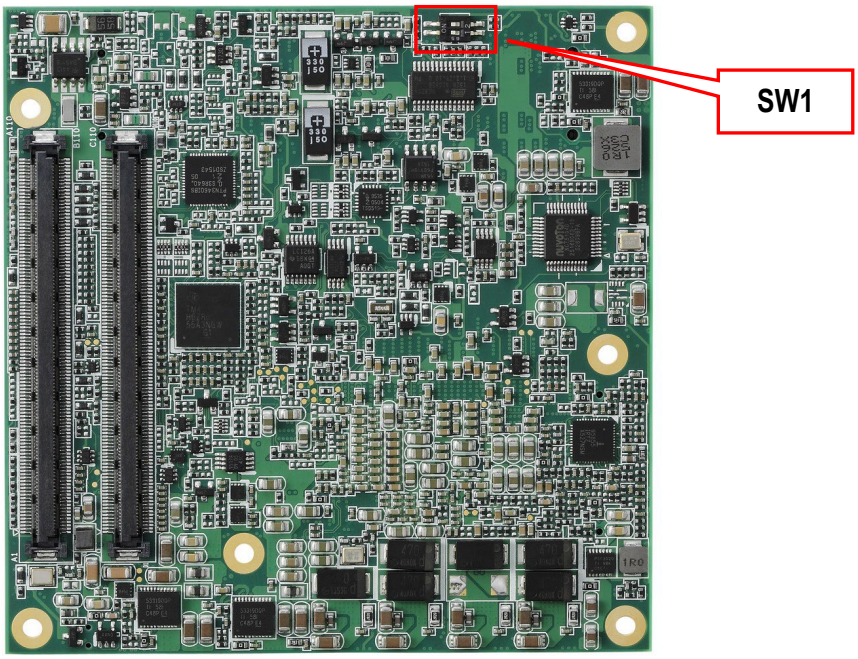
1. Shut down the system.
2. Press the BIOS Setup Defaults RESET Button continuously and boot up the system. You can release the button when the BIOS prompt screen appears
3. The BIOS prompt screen will display a confirmation that BIOS defaults have been reset and request that you reboot the system.




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## 4.7. Switch Settings

➢ **Switch Locations**




➢ **SW1: BIOS Select and Mode Configuration Switch**

The module has two BIOS chips and BIOS operation can be configured to "PICMG" and dual-BIOS "Failsafe" modes using SW1, Pin 2.

Setting the module to PICMG mode will configure the BIOS chips on the module as SPI0 and SPI1. In PICMG mode, a BIOS chip cannot be placed in the SPI0 slot on the carrier.

In dual-BIOS Failsafe mode, both BIOS chips on the module are configured as SPI1. Only one of the two is connected to the SPI bus at any given time. In case of failure of the primary SPI1 BIOS, the system will reboot and switch to the secondary SPI1 BIOS on the module. In Failsafe mode, the SPI0 BIOS socket on the carrier can be populated.

In either mode, SW1 Pin 1 is used to select whether to boot from SPI0 or SPI1.

| Mode | Pin 1 | Pin 2 |
|---|---|---|
| Boot from SPI0 (default) | On | — |
| Boot from SPI1 | Off | — |
| Set BIOS to PICMG mode | — | On |
| Set BIOS to Failsafe BIOS mode (default) | — | Off |

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# 5. Smart Embedded Management Agent (SEMA)

The onboard microcontroller (BMC) implements power sequencing and Smart Embedded Management Agent (SEMA) functionality. The microcontroller communicates via the System Management Bus with the CPU/chipset. The following functions are implemented:

- Total operating hours counter. Counts the number of hours the module has been run in minutes.
- On-time minutes counter. Counts the seconds since last system start.
- Temperature monitoring of CPU and board temperature. Minimum and maximum temperature values of CPU and board are stored in flash.
- Power cycles counter
- Boot counter. Counts the number of boot attempts.
- Watchdog Timer. Set/Reset/Disable Watchdog Timer. Features auto-reload at power-up.
- System Restart Cause. Power loss/BIOS Fail/Watchdog/Internal Reset/External Reset
- Fail-safe BIOS support. In case of a boot failure, hardware signals tells external logic to boot from fail-safe BIOS.
- Flash area. 1kB Flash area for customer data
- 2K Bytes Protected Flash area. Keys, IDs, etc. can be stored in a write- and clear-protectable region.
- Board Identify. Vendor/Board/Serial number/Production Date
- Main-current & voltage. Monitors drawn current and main voltages

For a detailed description of SEMA features and functionality, please refer to **SEMA Technical Manual** and **SEMA Software Manual**, downloadable at: **http://www.adlinktech.com/sema/**.

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## 5.1. Board Specific SEMA Functions

### 5.1.1. Voltages

The BMC of the cExpress-SL implements a voltage monitor and samples several onboard voltages. The voltages can be read by calling the SEMA function “Get Voltages”. The function returns a 16-bit value divided into high-byte (MSB) and low-byte (LSB).

| ADC Channel | Voltage Name | Voltage Formula [V] |
|---|---|---|
| 0 | VCC_CORE | (MSB<<8 + LSB) x 3.3 / 1024 |
| 1 | VCC_GT | (MSB<<8 + LSB) x 3.3 / 1024 |
| 2 | 1V0_A | (MSB<<8 + LSB) x 3.3 / 1024 |
| 3 | VDDQ | (MSB<<8 + LSB) x 3.3 / 1024 |
| 4 | VRTC | (MSB<<8 + LSB) x 3.3 / 1024 |
| 5 | V3P3S | (MSB<<8 + LSB) x 1.100 x 3.3 / 1024 |
| 6 | V3P3A | (MSB<<8 + LSB) x 1.100 x 3.3 / 1024 |
| 7 | V5_S | (MSB<<8 + LSB) x 1.826 x 3.3 / 1024 |
| 8 | 0V6_VTT | (MSB<<8 + LSB) x 3.3 / 1024 |
| 9 | 1V0_VCCIO | (MSB<<8 + LSB) x 3.3 / 1024 |
| 10 | 1V0_VCCSTG | (MSB<<8 + LSB) x 3.3 / 1024 |
| 11 | VCCSA | (MSB<<8 + LSB) x 3.3 / 1024 |
| 12 | 1v8_A | (MSB<<8 + LSB) x 3.3 / 1024 |
| 13 | V5VSB | (MSB<<8 + LSB) x 1.826 x 3.3 / 1024 |
| 14 | V12 | (MSB<<8 + LSB) x 6.000 x 3.3 / 1024 |
| 15 | (MAIN CURRENT) | Use Main Current Function |

### 5.1.2. Main Current

The BMC of the cExpress-SL implements a current monitor. The current can be read by calling the SEMA function “Get Main Current”. The function returns four 16-bit values divided in high-byte (MSB) and low-byte (LSB). These 4 values represent the last 4 currents drawn by the board. The values are sampled every 250ms. The order of the 4 values is NOT in chronological order. Access by the BMC may increase the drawn current of the whole system. In this case, there are still 3 samples not influenced by the read access.

Main Current = (MSB_n<<8 + LSB_n) x 8.06mA

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### 5.1.3. BMC Status

This register shows the status of BMC controlled signals on the cExpress-SL.

| Status Bit | Signal |
|---|---|
| 0 | WDT_OUT |
| 1 | LVDS_VDDEN |
| 2 | LVDS_BKLTEN |
| 3 | BIOS_MODE |
| 4 | POSTWDT_DISn |
| 5 | SEL_BIOS |
| 6 | BIOS_DIS0n |
| 7 | BIOS_DIS1n |

### 5.1.4. Exception Codes

In case of an error, the BMC drives a blinking code on the blue Status LED (LED1). The same error code is also reported by the BMC Flags register. The Exception Code is not stored in the Flash Storage and is cleared when the power is removed. Therefore, a “Clear Exception Code” command is not needed or supported.

| Exception Code | Error Message |
|---|---|
| 0 | NOERROR |
| 2 | NO_SUSCLK |
| 3 | NO_SLP_S5 |
| 4 | NO_SLP_S4 |
| 5 | NO_SLP_S3 |
| 6 | NO_CB_PWRGD |
| 7 | BIOS_FAIL |
| 8 | RESET_FAIL |
| 9 | RESETIN_FAIL |
| 10 | CRITICAL_TEMP |
| 11 | POWER_FAIL |
| 12 | VOLTAGE_FAIL |
| 13 | NO_SYS_GD |
| 14 | NO_3V3_A_PGD |
| 15 | NO_VDDQ_PG |
| 16 | NO_P_5V_3V3_S0_PG |
| 17 | NO_1V0_A_PG |
| 18 | NO_VCORE_PG |

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### 5.1.5. BMC Flags

The BMC Flags register returns the last detected Exception Code since power-up and shows the BIOS in use and the power mode.

| Bit | Description |
|---|---|
| [ 0 ~ 4 ] | Exception Code |
| [ 6 ] | 0 = AT mode<br>1 = ATX mode |
| [ 7 ] | 0 = Standard BIOS<br>1 = Fail-safe BIOS. |

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# 6. System Resources

## 6.1. System Memory Map

| Address Range (decimal) | Address Range (hex) | Size | Description |
|---|---|---|---|
| (4GB-2MB) | FFE00000 – FFFFFFFF | 16 MB | High BIOS Area |
| (4GB-18MB) – (4GB-17MB-1) | FEE00000 – FEEFFFFF | 1 MB | MSI Interrupts |
| (4GB-20MB) – (4GB-19MB-1) | FEC00000 – FECFFFFF | 1 MB | APIC Configuration Space |
| 15MB – 16MB | F00000 – FFFFFF | 1 MB | ISA Hole |
| 1MB -15MB | 100000 - EFFFFF | 14MB | Main Memory |
| 0K –1MB | 00000 – FFFFFF | 1MB | DOS Compatibility Memory |

## 6.2. Direct Memory Access Channels

| Channel Number | Data Width | System Resource |
|---|---|---|
| 0 | 8-bits | Generic |
| 1 | 8-bits | Generic |
| 2 | 8-bits | Generic |
| 3 | 8-bits | Generic |
| 4 | | Reserved - cascade channel |
| 5 | 16-bits | Generic |
| 6 | 16-bits | Generic |
| 7 | 16-bits | Generic |

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## 6.3. I/O Map

| Hex Range | Device |
|---|---|
| 000-01F | Reserved |
| 020-02D and 030-03F | Interrupt controller 1, 8259 equivalent |
| 02E-02F | LPC SIO () configuration index/data registers |
| 040-05F | Timer, 8254-2 equivalent |
| 060, 062, 064, 066, 068-06F | 8742 equivalent (keyboard) |
| 061, 063, 065, 067 | NMI control and status |
| 070-07F | Real Time Clock Controller( bit 7 -NMI mask) |
| 080-090 | LPC or PCIe |
| 092 | Reset (Bit 0)/ Fast Gate A20 (Bit 1) |
| 091， 93-9F | Reserved |
| 0A0-0B1 and 0B4-0BF | Interrupt controller 2, 8259 equivalent |
| 0B2 and 0B3 | APM control and status port respectively |
| 0C0-0DF | Reserved |
| 0E0-0EF | Available |
| 0F0 | Co-processor error register |
| 0F1-0FF | N/A |
| 100-169 | N/A |
| 170-177 | Sata Controller |
| 178-1EF | N/A |
| 1F0-1F7 | Sata Controller |
| 1F8-2DF | N/A |
| 240 -24F | Serial Port 1/2 |
| 2F8-2FF | Serial Port 3 |
| 300-36F | Available |
| 376 | Sata Controller |
| 378-37F | Available |
| 380-3AF | Available |
| 3B0-3BB and 3BF | Mono/VGA mode video |
| 3BC-3BE | Reserved for parallel port |
| 3C0-3DF | VGA registers |
| 3E0-3EF | Available |

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| Hex Range | Device |
|---|---|
| 3F0-3F7 | Available |
| 3F8-3FF | Serial port 4 |
| 4D0 | Master PIC Edge/Level Trigger register |
| 4D1 | Slave PIC Edge/Level Trigger register |
| CF8-CFB | PCI configuration address register (32 bit I/O only) |
| CF9 | Reset Control register (8 bit I/O) |
| CFC-CFF | PCI configuration data register |
| F040 | Smbus base address for SB. |
| 1C00 | GPIO Base Address for SB |
| 1800 | PM (ACPI) Base Address for SB |
| 1860 | Alias for ICH TCO base address. |
| 0A00~0AFF | Reserved for SIO functions base address (ex: PME /GPIO etc) |

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## 6.4. Interrupt Request (IRQ) Lines

**PIC Mode**

| IRQ# | Typical Intterupt Resource | Connected to Pin | Available |
|---|---|---|---|
| 0 | Counter 0 | N/A | No |
| 1 | Keyboard controller | N/A | No |
| 2 | Cascade interrupt from slave PIC | N/A | No |
| 3 | Serial Port 4 (COM4) | IRQ3 via SERIRQ / PIRQ | Note (1) |
| 4 | Serial Port 3 (COM3) | IRQ4 via SERIRQ / PIRQ | Note (1) |
| 5 | Serial Port 2 (COM2) | IRQ5 via SERIRQ / PIRQ | Note (1) |
| 6 | Generic | IRQ6 via SERIRQ / PIRQ | No |
| 7 | Serial Port 1 (COM1) | IRQ7 via SERIRQ / PIRQ | Note (1) |
| 8 | Real-time clock | N/A | No |
| 9 | Generic | N/A | Note (1) |
| 10 | Generic | IRQ10 via SERIRQ / PIRQ | Note (1) |
| 11 | Generic | IRQ11 via SERIRQ / PIRQ | Note (1) |
| 12 | PS/2 Mouse | IRQ12 via SERIRQ / PIRQ | Note (1) |
| 13 | GSPI, UART, I2C, SDIO | N/A | Note (1) |
| 14 | Gpio | PIRQ | Note (1) |
| 15 | Gpio | PIRQ | Note (1) |

**Note (1):** These IRQs can be used for PCI devices when onboard device is disabled.

**APIC Mode**

| IRQ# | Typical Intterupt Resource | Connected to Pin | Available |
|---|---|---|---|
| 0 | Counter 0 | N/A | No |
| 1 | Keyboard controller | N/A | No |
| 2 | Cascade interrupt from slave PIC | N/A | No |
| 3 | Serial Port 4 (COM4) | IRQ3 via SERIRQ / PIRQ | Note (1) |
| 4 | Serial Port 3 (COM3) | IRQ4 via SERIRQ / PIRQ | Note (1) |
| 5 | Serial Port 2 (COM2) | N/A | Note (1) |
| 6 | N/A | N/A | Note (1) |
| 7 | Serial Port 1 (COM1) | N/A | Note (1) |
| 8 | Real-time clock | N/A | No |
| 9 | N/A | IRQ9 via SERIRQ / PIRQ | Note (1) |
| 10 | N/A | IRQ10 via SERIRQ / PIRQ | Note (1) |

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| IRQ# | Typical Intterupt Resource | Connected to Pin | Available |
|---|---|---|---|
| 11 | N/A | IRQ11 via SERIRQ / PIRQ | Note (1) |
| 12 | PS/2 Mouse | IRQ12 via SERIRQ / PIRQ | Note (1) |
| 13 | Math Processor | N/A | Note (1) |
| 14 | Primary IDE controller | IRQ14 via SERIRQ / PIRQ | Note (1) |
| 15 | Secondary IDE controller | IRQ15 via SERIRQ / PIRQ | Note (1) |
| 16 | N/A | P.E.G Root Port,Intel HDA, PCIE Port 0/1/2/3/4/5/6, EHCI Conterller #2 , I.G.D ,XHCI Controller | Note (1) |
| 17 | N/A | PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port, | Note (1) |
| 18 | N/A | PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port, SMBus Controller, EHCI Controller #2 | Note (1) |
| 19 | N/A | PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port, | Note (1) |
| 20 | N/A | Gbe Controller | Note (1) |
| 21 | N/A | | Note (1) |
| 22 | N/A | Intel HDA | Note (1) |
| 23 | N/A | EHCI Controller #1 | Note (1) |

**Note (1):** These IRQs can be used for PCI devices when onboard device is disabled.

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## 6.5. PCI Configuration Space Map

| Bus Number | Device Number | Function Number | Routing | Description |
|---|---|---|---|---|
| 00h | 00h | 00h | N/A | Intel host Bridge |
| 00h | 02h | 00h | Internal | Intel I.G.D |
| 00h | 08h | 00h | Internal | Gaussian Mixture Models Controller |
| 00h | 14h | 00h | Internal | xHCI Controller |
| 00h | 16h | 00h | Internal | Intel Management Engine Interface #1 |
| 00h | 17h | 00h | Internal | AHCI Controller |
| 00h | 1Ch | 00h | Internal | Intel PCI Express Root port 1 |
| 00h | 1Ch | 01h | Internal | Intel PCI Express Root port 2 |
| 00h | 1Ch | 02h | Internal | Intel PCI Express Root port 3 |
| 00h | 1Ch | 03h | Internal | Intel PCI Express Root port 4 |
| 00h | 1Ch | 04h | Internal | Intel PCI Express Root port 5 |
| 00h | 1Ch | 05h | Internal | Intel PCI Express Root port 6 |
| 00h | 1Fh | 00h | N/A | Intel LPC Interface Bridge |
| 00h | 1Fh | 02h | Internal | PMC Controller |
| 00h | 1Fh | 03h | Internal | HD Audio Controller |
| 00h | 1Fh | 04h | Internal | SMBus Controller |
| 00h | 1Fh | 06h | Internal | Gigabit Etherent Controller |

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## 6.6. PCI Interrupt Routing Map

| INT Line | P.E.G Root Port | Audio Controller | xHCI Controller | ME Controller #1 | ME Controller #2 | IDE-R | KT | GbE Controller | HAD Controller |
|---|---|---|---|---|---|---|---|---|---|
| Int0 | INTA:16 | INTA:16 | INTA:16 | INTA:16 | | | | INTA:16 | |
| Int1 | INTB:17 | | | INTD:19 | | | | | |
| Int2 | INTC:18 | | | INTC:18 | | | | | |
| Int3 | INTD:19 | | | INTB:17 | | | | | |

| INT Line | PCIE port1 | PCIE port 2 | PCIE port 3 | PCIE port 4 | PCIE port5 |
|---|---|---|---|---|---|
| Int0 | INTA:16 | INTB:17 | INTC:18 | INTD:19 | INTA:16 |
| Int1 | INTB:17 | INTC:18 | INTD:19 | INTA:16 | INTB:17 |
| Int2 | INTC:18 | INTD:19 | INTA:16 | INTB:17 | INTC:18 |
| Int3 | INTD:19 | INTA:16 | INTB:17 | INTC:18 | INTC:19 |

| INT Line | LPC Controller | SATA Controller #1 | SMBus Controller | SATA Controller #2 |
|---|---|---|---|---|
| Int0 | INTA:16 | INTA:16 | INTA:16 | |
| Int1 | INTB:17 | | | |
| Int2 | INTC:18 | | | |
| Int3 | INTD:19 | | | |

## 6.7. SMBus Address Table

| Device | Address |
|---|---|
| DIMM A | A0h |
| DIMM B | A4h |
| BMC | 50h |
| Extend GPIO | 40h |

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# 7. BIOS Setup

## 7.1. Menu Structure

This section presents the six primary menus of the BIOS Setup Utility. Use the following table as a quick reference for the contents of the BIOS Setup Utility. The subsections in this section describe the submenus and setting options for each menu item. The default setting options are presented in **bold**, and the function of each setting is described in the right hand column of the respective table.

| Main | Advanced | Security | Boot | Save & Exit |
|---|---|---|---|---|
| - System Information | - CPU ▶ | - Password Description ▶ | - Boot Configuration ▶ | - Reset Options ▶ |
| - Processor Information | - Memory ▶ | - Secure Boot Menu ▶ | - CSM Configuration ▶ | - Save Options ▶ |
| - PCH Information | - Graphics ▶ | | | |
| - System Management ▶ | - SATA ▶ | | | |
| - System Date | - USB ▶ | | | |
| - System Time | - Network ▶ | | | |
| | - PCI and PCIe ▶ | | | |
| | - Super IO ▶ | | | |
| | - ACPI and Power Management ▶ | | | |
| | - Sound ▶ | | | |
| | - Serial Port Console ▶ | | | |
| | - ICC ▶ | | | |
| | - Thermal ▶ | | | |
| | - Miscellaneous ▶ | | | |

**Notes:**

▶ indicates a submenu

Gray text indicates info only

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## 7.2. Main

The Main Menu provides read-only information about your system and also allows you to set the System Date and Time. Refer to the tables below the screen shot of this menu for details of the submenus and settings.

### 7.2.1. System Information

| Feature | Options | Description |
|---|---|---|
| BIOS Version | Info only | ADLINK BIOS version. |
| Board Revision | Info only | Hardware revision. |
| Build Date and Time | Info only | ADLINK date the BIOS was build. |

### 7.2.2. Processor Information

| Feature | Options | Description |
|---|---|---|
| CPU Brand String | Info only | Display CPU Brand Name. |
| Frequency | Info only | Display CPU Frequency. |
| Processor ID | Info only | Display CPU ID. |
| Stepping | Info only | Display CPU Stepping. |
| Number of Processors | Info only | Display number of Processors. |
| GT Info | Info only | Display GT info of Intel Graphics. |
| IGFX VBIOS Version | Info only | Display VBIOS Version. |
| Total Memory | Info only | Display installed memory size. |

### 7.2.3. PCH Information

| Feature | Options | Description |
|---|---|---|
| PCH Name | Info only | Display PCH name. |
| PCH SKU | Info only | Display PCH SKU. |
| Stepping | Info only | Display PCH stepping. |
| ME FW Version | Info only | Display version of ME. |
| ME Firmware SKU | Info only | Display ME Firmware Kit SKU number. |
| System Management | Submenu | |

#### 7.2.3.1. PCH Information System Management

| Feature | Options | Description |
|---|---|---|
| System Management | Info only | |
| Version | Info only | Display version. |

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## 7.2.4. System Management

### 7.2.4.1. System Management > Board Information

| Board Information | Info only | Description |
|---|---|---|
| SMC Firmware | Read only | Display SMC Firmware. |
| Build Date | Read only | Display SMC firmware build date. |
| SMC Boot loader | Read only | Display SMC boot loader. |
| Build Date | Read only | Display SMC boot loader build date. |
| Hardware Version | Read only | Display SMC hardware Version. |
| Serial Number | Read only | Display SMC serial Number. |
| Manufacturing Date | Read only | Display SMC manufacturing date. |
| Last Repair Date | Read only | Display SMC last repair date. |
| MAC ID | Read only | Display SMC MAC ID |

### 7.2.4.2. System Management > Temperatures and Fan Speed

| Feature | Options | Description |
|---|---|---|
| Temperatures and Fan | Info only | |
| CPU Temperature | Info only | |
| Current | Read only | Display CPU current temperature. |
| Startup | Read only | Display CPU startup temperature. |
| Min | Read only | Display CPU min temperature. |
| Max | Read only | Display CPU max temperature. |
| Board Temperatures | Info only | |
| Current | Read only | Display board current temperature. |
| Startup | Read only | Display board startup temperature. |
| Min | Read only | Display board min temperature. |
| Max | Read only | Display board max temperature. |
| CPU Fan Speed | Read only | Display CPU fan speed. |
| System Fan Speed | Read only | Display system fan speed. |

### 7.2.4.3. System Management > Power Consumption

| Feature | Options | Description |
|---|---|---|
| Power Consumption | Info only | |
| Current Input Current | Read only | Display input current. |
| Current Input Power | Read only | Display input power. |
| V3.30 | Read only | Display actual voltage of the V3.30. |



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| Feature | Options | Description |
|---|---|---|
| V1.05 | Read only | Display actual voltage of the V1.05. |
| Vtt | Read only | Display actual voltage of the VTT. |
| V1.35 | Read only | Display actual voltage of the V1.35. |
| V5.00 | Read only | Display actual voltage of the V5.00. |
| V3.30 | Read only | Display actual voltage of the V3.30. |
| AIN7 | Read only | Display actual voltage of the AIN7. |

### 7.2.4.4. System Management > Runtime Statistics

| Feature | Options | Description |
|---|---|---|
| Runtime Statistics | Info only | |
| Total Runtime | Read only | The returned value specifies the total time in minutes the system is running in S0 state. |
| Current Runtime | Read only | The returned value specifies the time in seconds the system is running in S0 state.<br>This counter is cleared when the system is removed from the external power supply. |
| Power Cycles | Read only | The returned value specifies the number of times the external power supply has been shut down |
| Boot Cycles | Read only | The Bootcounter is increased after a HW- or SW-Reset or after a successful power-up. |
| Boot Reason | Read only | The boot reason is the event which causes the reboot of the system. |

### 7.2.4.5. System Management > Flags

| Feature | Options | Description |
|---|---|---|
| Flags | Info only | |
| BMC Flags | Read only | |
| BIOS Select | Read only | Display the selection of current BIOS ROM. |
| ATX/AT-Mode | Read only | Display ATX/AT-Mode. |
| Exception Code | Read only | System exception reason. |

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### 7.2.4.6. System Management > Power Up

| Feature | Options | Description |
|---|---|---|
| Power Up | Info only | |
| Power Up watchdog<br>Attention: F12 disables the Power Up Watchdog. | Enabled<br>**Disabled** | The Power-Up Watchdog resets the system after a certain amount of time after power-up. |
| ECO Mode | **Disabled**<br>Enable | Reduces the power consumption of the system. |
| Power-up Mode<br>Attention: The Power-Up Mode only has effect, if the module is in ATX-Mode. | Turn on<br>**Remain off**<br>Last State | Turn On: The machine starts automatically when the power supply is turned on.<br>Remain Off :To start the machine the power button has to be pressed.<br>Last State: when powered on during a power failure the system will automatically power on when power is restored |

### 7.2.4.7. System Management > LVDS Backlight

| Feature | Options | Description |
|---|---|---|
| LVDS Backlight | Info only | |
| LVDS Backlight Bright | 255 | The value range starts by 0 and ends by 255. |

### 7.2.4.8. System Management > Smart Fan

| Feature | Options | Description |
|---|---|---|
| Smart Fan | Info only | |
| CPU Smart FanTemperature Source | **CPU Sensor**<br>System Sensor | Select CPU smart fan source. |
| CPU Fan Mode | **AUTO (Smart Fan)**<br>Fan Off<br>Fan On | Select CPU Fan Mode. |
| CPU Trigger Point 1 | Read only | |
| Trigger Temperature | 15 | Specifies the temperature threshold at which the BMC turns on CPU fan with specific PWM level. |
| PWM Level | 30 | Select PWM level. |
| CPU Trigger Point 2 | Read only | |
| Trigger Temperature | 60 | Specifies the temperature threshold at which the BMC turns on CPU fan with specific PWM level. |
| PWM Level | 40 | Select PWM level. |
| CPU Trigger Point 3 | Read only | |
| Trigger Temperature | 70 | Specifies the temperature threshold at which the BMC turns on CPU fan with specific PWM level. |
| PWM Level | 63 | Select PWM level. |
| CPU Trigger Point 4 | Read only | |
| Trigger Temperature | 80 | Specifies the temperature threshold at which the BMC turns on CPU fan with specific PWM level. |
| PWM Level | 100 | Select PWM level. |

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### 7.2.5. System Date and Time

| Feature | Options | Description |
|---|---|---|
| System Date | Weekday, MM/DD/YYYY | Requires the alpha-numeric entry of the day of the week, day of the month, calendar month, and all 4 digits of the year, indicating the century and year (Fri XX/XX/20XX) |
| System Time | HH/MM/SS | Presented as a 24-hour clock setting in hours, minutes, and seconds |

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## 7.3. Advanced

This menu contains the settings for most of the user interfaces in the system

### 7.3.1. CPU

| Feature | Options | Description |
|---|---|---|
| CPU | Info only | Manufacturer, model, speed |
| CPU Signature | Info only | Display CPU Signature. |
| Processor Family | Info only | Display Processor Family. |
| Microcode Patch | Info only | Display Microcode Patch. |
| Max CPU speed | Info only | Display Max CPU speed. |
| Min CPU speed | Info only | Display Min CPU speed. |
| CPU Speed | Info only | Display CPU Speed. |
| Processor Cores | Info only | Display Processor Cores. |
| Intel HT Technology | Info only | Display Intel HT Technology support or not. |
| Intel VT-x Technology | Info only | Display Intel VT-x Technology support or not. |
| EIST Technology | Info only | Display EIST Technology support or not |
| CPU C3 state | Info only | Display CPU C3 state support or not |
| CPU C6 state | Info only | Display CPU C6 state support or not |
| CPU C7 state | Info only | Display CPU C7 state support or not |
| Intel SMX Technology | Info only | Display Intel SMX Technology support or not. |
| 64-bit | Info only | Display 64-bit support or not. |
| L1 Data Cache | Info only | Display cache info. |
| L1 Code Cache | Info only | Display cache info. |
| L2 Cache | Info only | Display cache info. |
| L3 Cache | Inf o only | Display cache info. |
| L4 Cache | Inf o only | Display cache info. |
| Hyper-threading | Disabled<br>**Enabled** | Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled only one thread per enabled core is enabled. |
| Active Processor Cores | **All**<br>1 | Number of cores to enable in each processor package. |
| VT-d | Disabled<br>**Enabled** | Check to enable VT-d function on MCH. |
| Intel Virtualization Technology | Disabled<br>**Enabled** | Enable/Disable support for the Intel virtualization technology. |
| Intel(R) SpeedStep(TM) | Disabled<br>**Enabled** | Allows more than two frequency ranges to be supported. |
| Turbo Mode | Disabled<br>**Enabled** | Enable/Disable turbo mode. |

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| Feature | Options | Description |
|---|---|---|
| Configurable TDP Boot Mode | **TDP Nominal**<br>TDP Down<br>Disabled | Configure TDP Mode as Nominal/Down/Disabled. Disabled option will set MSR to Nominal and MMIO to Zero. |
| Config TDP Lock | **Disabled**<br>Enabled | Configurable TDP Mode Lock sets the Lock bits on TURBO_ACTIVATION_RATIO and CONFIG_TDP_CONTROL.<br>Note: When CTDP Lock is enabled Custom ConfigTDP Count will be forced to 1 and Custom ConfigTDP Boot Index will be forced to 0. |
| CPU C state | Disabled<br>**Enabled** | Enable or disable CPU C states |
| C-State Auto Demotion | Disabled<br>C1<br>C3<br>**C1 and C3** | Configure C-State Auto Demotion |
| Package C State limit | **Auto**<br>C2<br>C3<br>C6<br>C7<br>Auto | Package C State limit |
| Intel TXT(LT) support | Disabled<br>**Enabled** | Enables or Disables Intel(R) TXT(LT) support. |
| | | |
| CPU DTS | Disabled<br>**Enabled** | Enable/Disable CPU DTS. |
| ACPI 3.0 T-state | **Disabled**<br>Enabled | Enable/Disable ACPI 3.0 T-States. |

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### 7.3.2. Memory

| Feature | Options | Description |
|---|---|---|
| Memory RC Version | Info only | Display Memory Reference Code Version. |
| Memory Frequency | Info only | Display Memory Frequency. |
| Total Memory | Info only | Display Total Memory. |
| VDD | Info only | Display Memory Voltage. |
| DIMM#0/1 | Info only | Display DIMM#0/1. |
| Memory Timings | Info only | Display Memory timings |
| XMP Profile 1 | Info only | Display XMP Profile 1 support or not. |
| XMP Profile 2 | Info only | Display XMP Profile 2 support or not. |
| I2C Write Protect Control | Active<br>**Write Protect** | I2C write protect control |
| SPD Write Protect | **Enabled**<br>Disabled | Enable:Writes to SMBus slave addresses A0h - AEh are disabled. |
| Maximum Memory Frequency | **Auto**<br>1067<br>1200<br>1333<br>1400<br>1600<br>1800<br>1867<br>2000<br>2133<br>2200<br>2400<br>2600<br>2800<br>2933<br>3000<br>3200 | Maximun Memory Frequency Selections in MHz |
| Max TOLUD | **Dynamic** | Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller. |

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### 7.3.3. Graphics

| Feature | Options | Description |
|---|---|---|
| Graphics Configuration | Info only | |
| IGFX VBIOS Version | Info only | Display VBIOS Version. |
| IGfx Frequency | Info only | Display IGfx Frequency. |
| Graphics Turbo IMON Current | Number entry field | Graphics turbo IMON current values supported (14-31). |
| Primary Display | **Auto**<br>IGFX<br>PEG<br>PCIE | Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx. |
| Primary PEG | **Auto**<br>PEG1<br>PEG2 | Select PEG0/PEG1/PEG2/PEG3 Graphics device should be Primary PEG. |
| Primary PCIE | **Auto**<br>PCIE1<br>PCIE2<br>PCIE3<br>PCIE4<br>PCIE5<br>PCIE6<br>PCIE7 | Select PCIE0/PCIE1/PCIE2/PCIE3/PCIE4/PCIE5/PCIE6/PCIE7 Graphics device should be Primary PCIE. |
| Internal Graphics | **Auto**<br>Disabled<br>Enable | Keep IGD enabled based on the setup options. |
| Aperture Size | 128MB<br>**256MB**<br>512MB<br>1024MB<br>2048MB<br>4096MB | Select the Aperture Size. |
| DVMT Pre-Allocated | **XXM** | Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device. |
| DVMT Total Gfx Mem | **XXXM** | Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device. |
| Gfx Low Power Mode | **Enabled**<br>Disabled | This option is applicable for SFF only. |
| EDP to LVDS Bridge Configuration | **Info only** | |
| Data Format and Color Depth | VESA 24 bpp<br>JEIDA 24 bpp<br>**JEIDA/VESA 18 bpp** | Data format and color depth select |
| LVDS Output Mode | **Single LVDS bus**<br>Dual LVDS bus | Single/Dual mode select |
| DE Polarity | **Active High**<br>Active Low | DE Polarity select |
| Vsync Polarity | **Active High** | Vsync Polarity select |

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| Feature | Options | Description |
|---|---|---|
| | Active Low | |
| Hsync Polarity | **Active High**<br>Active Low | Hsync Polarity select |
| LVDS Backlight Mode | **BMC Mode**<br>GTT Mode | Select LVDS Backlight control function. |
| GTT LVDS/eDP Backlight Control | 0%<br>20%<br>40%<br>60%<br>80%<br>**100%** | Actual backlight value in percent of the maximum setting. |
| DDI function choose | **Display Port**<br>HDMI | Select DDI function choose to display port or HDMI. |
| Primary IGFX Boot Display | **VBIOS Default** | Select the Video Device which will be activated during POS. |
| LCD Panel Type | **VBIOS Default**<br>640X480<br>800X600<br>1024X768<br>1280X1024<br>1400X1050<br>1600X1200<br>1366X768<br>1680X1050<br>1920X1200<br>1440X900<br>1600X900<br>1024X768 LVDS2<br>1280X800<br>1920X1080<br>2048X1536 | Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item. |
| Active LFP | No LVDS<br>**eDP Port-A** | Select the Active LFP Configuration. |
| Panel Scaling | **Auto**<br>Off<br>Force Scaling | Select the LCD panel scaling option used by the Internal Graphics Device. |

### 7.3.4. SATA

| Feature | Options | Description |
|---|---|---|
| SATA Controller(s) | **Enabled**<br>Disabled | Enable/Disable SATA Device. |
| SATA Mode Selection | **AHCI**<br>RAID | Determines how SATA controller(s) operate. |
| SATA Speed Selection | **Default**<br>Gen1<br>Gen2<br>Gen3 | Indicates the maximum speed the SATA controller can support. |
| SATA Test Mode | Enabled<br>**Disabled** | Test Mode Enable/Disable (Loop Back) |

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| Feature | Options | Description |
|---|---|---|
| Aggressive LPM Support | **Enabled**<br>Disabled | Enable PCH to aggressively enter link power state. |
| SATA Port Configuration | Submenu | |
| Software Feature Mask Configuration | Info only | |
| RAID0 | **Enabled**<br>Disabled | Enable/Disable RAID0 feature. |
| RAID1 | **Enabled**<br>Disabled | Enable/Disable RAID1 feature. |
| RAID5 | **Enabled**<br>Disabled | Enable/Disable RAID5 feature. |
| Intel Rapid Recovery Technology | **Enabled**<br>Disabled | Enable/Disable Intel Rapid Recovery Technology. |
| OROM UI and BANNER | **Enabled**<br>Disabled | If enabled, then the OROM UI is shown. Otherwise, no OROM banner or information will be displayed if all disks and RAID volumes are Normal. |
| HDD Unlock | **Enabled**<br>Disabled | If enabled, indicates that the HDD password unlock in the OS is enabled. |
| LED Locate | **Enabled**<br>Disabled | If enabled, indicates that the LED/SGPIO hardware is attached and ping to locate feature is enabled on the OS. |
| IRRT Only on ESATA | **Enabled**<br>Disabled | If enabled, then only IRRT volumes can span internal and eSATA drives. If disabled, then any RAID volume can span internal and eSATA drives. |
| Smart Response Technology | **Enabled**<br>Disabled | Enable/Disable Smart Response Technology. |
| OROM UI Delay | **Enabled**<br>Disabled | If enabled, indicates the delay of the OROM UI Splash Screen in a normal status. |
| RST Force Form | Enabled<br>**Disabled** | Enable/Disable Form for Intel Rapid Storage Technology. |

### 7.3.4.1. SATA > SATA Port Configuration

| Feature | Options | Description |
|---|---|---|
| SATA Port Configuration | Info only | |
| Port X | Disabled<br>**Enabled** | Enable/Disable SATA Port. |
| Hot Plug | Disabled<br>**Enabled** | Designates this port as Hot Pluggable. |
| External SATA | **Disabled**<br>Enabled | External SATA Support. |
| Spin up Device | **Disabled**<br>Enabled | On an edge detect from 0 to 1, the PCH starts a COMRESET initialization sequence to the device. |
| SATA Device Type | **Hard Disk Drive**<br>Solid State Drive | Identify the SATA port is connected to Solid State Drive or Hard Disk Drive. |
| Topology | **Unknown**<br>ISATA<br>Direct Connect<br>Flex<br>M2 | Identify the SATA Topology if it is Default, ISATA, Flex, DirectConnect or M2. |



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| Feature | Options | Description |
|---|---|---|
| Device Sleep | **Disabled**<br>Enabled | mSATA for RTD3 |
| SATA DEVSLEP Idle Timeout Configuration | **Disabled**<br>Enabled | Enable/Disable SATA DTIO Configuration |

### 7.3.5. USB

| Feature | Options | Description |
|---|---|---|
| USB Configuration | Submenu | |
| USB Module Version | Info only | |
| USB Devices | Info only | X Drive, X Keyboards, X Mouse, X Hubs |
| Legacy USB Support | **Enabled**<br>Disabled<br>Auto | Enables legacy USB support.<br>Auto option disables legacy support if no USB devices are connected.<br>Disable option will keep USB devices available only for EFI applications and setup. |
| XHCI Hand-off | **Enabled**<br>Disabled | This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by the XHCI OS driver. |
| USB Mass Storage Driver Support | **Enabled**<br>Disabled | Enable/Disable USB Mass Storage Driver Support. |
| Port 60/64 Emulation | Enabled<br>**Disabled** | Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes. |
| USB hardware delays and time-outs: | Info only | |
| USB transfer time-out | 1 sec<br>5 sec<br>10 sec<br>**20 sec** | The time-out value for Control, Bulk, and Interrupt transfers |
| Device reset time-out | 10 sec<br>**20 sec**<br>30 sec<br>40 sec | USB mass storage device Start Unit command time-out. |
| Device power-up delay | **Auto**<br>Manual | Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor. |
| Mass Storage Devices | Info only | List current USB max stroge device. |

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#### 7.3.5.1. USB > USB Configuration

| Feature | Options | Description |
|---|---|---|
| USB Precondition | **Disabled**<br>Enabled | Precondition work on USB host controller and root ports for faster enumeration. |
| XHCI Disable Compliance Mode | **FALSE**<br>TRUE | Options to disable Compliance Mode. Default is FALSE to not disable Compliance Mode. Set TRUE to disable Compliance Mode. |
| XDCI Support | **Disabled**<br>Enabled | Enable/Disable XDCI (USB OTG Device) |
| USB Port Disable Override | **Disabled**<br>Select Per-Pin | Selectively Enable/Disable the corresponding USB port from reporting a Device Connection to the controller. |

### 7.3.6. Network

| Feature | Options | Description |
|---|---|---|
| Network Stack | Info only | |
| Network Stack | Enabled<br>**Disabled** | Enable/Disable UEFI network stack. |
| PCH LAN Controller | **Enabled**<br>Disabled | Enable/Disable onboard NIC. |
| Wake on LAN | Enabled<br>**Disabled** | Enable/Disable integrated LAN to wake the system. (The Wake On LAN cannot be disabled if ME is on at Sx state. |
| AMT Configuration | Info only | |
| Intel AMT | Enabled<br>**Disabled** | Enable/Disable Intel (R) Active Management Technology BIOS Extension. |
| BIOS Hotkey Pressed | Enabled<br>**Disabled** | Enable/Disable BIOS hotkey press. |
| MEBx Selection Screen | Enabled<br>**Disabled** | Enable/Disable MEBx selection screen. |
| Hide Un-Configure ME Confirmation | Enabled<br>**Disabled** | Hide Un-Configure ME without password Confirmation Prompt. |
| MEBx Debug Message Output | Enabled<br>**Disabled** | Enable MEBx debug message output. |
| Un-Configure ME | Enabled<br>**Disabled** | Un-Configure ME without password. |
| AMT Wait Timer | 0 | Set timer to wait before sending ASF_GET_BOOT_OPTIONS. |
| ASF | **Enabled**<br>Disabled | Enable/Disable Alert Specification Format. |
| Activate Remote Assistance Process | Enabled<br>**Disabled** | Trigger CIRA boot. |
| USB Configure | **Enabled**<br>Disabled | Enable/Disable USB Configure function. |
| PET Progress | **Enabled**<br>Disabled | User can Enable/Disable PET Events progress to recieve PET events or not. |
| AMT CIRA Timeout | 0 | OEM defined timeout for MPS connection to be established. 0 - use the default timeout value of 60 seconds. 255 - MEBX waits until the connection succeeds. |
| Watchdog | Enabled<br>**Disabled** | Enable/Disable WatchDog Timer. |

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| Feature | Options | Description |
|---|---|---|
| OS Timer | | Set OS watchdog timer. |
| BIOS Timer | | Set BIOS watchdog timer. |

### 7.3.7. PCI and PCIe

| Feature | Options | Description |
|---|---|---|
| PCI Common Settings | Info only | |
| Native PCIE Enable | **Disabled**<br>Enabled | CI Express Native Support Enable/Disable. This feature is only available in Vista |
| PCIE Ports 1-4 Configuration | **4x1 Port**<br>1x2 2x1 Port<br>2x2 Port<br>1x4 Port | Configures PCI-E Port 1-4 of PCH.<br>[4X1]: Port 1-4 (x1) and Port 8 (x1)<br>[1x2 2x1]: Port 1 (x2), Port 2 (disabled), Ports 3 and Port 4 (x1)<br>[2x2]: Port 1-2 (x2) and Port 3-4 (x2)<br>[1x4]: Port 1 (x4), Ports 2-4 (disabled) |
| PCI Latency Timer | **32 PCI Bus Clocks**<br>64 PCI Bus Clocks<br>96 PCI Bus Clocks<br>128 PCI Bus Clocks<br>160 PCI Bus Clocks<br>192 PCI Bus Clocks<br>224 PCI Bus Clocks<br>248 PCI Bus Clocks | Value to be programmed into PCI Latency Timer Register. |
| PCI-X Latency Timer | 32 PCI Bus Clocks<br>**64 PCI Bus Clocks**<br>96 PCI Bus Clocks<br>128 PCI Bus Clocks<br>160 PCI Bus Clocks<br>192 PCI Bus Clocks<br>224 PCI Bus Clocks<br>248 PCI Bus Clocks | Value to be programmed into PCI Latency Timer Register. |
| VGA Palette Snoop | **Disabled**<br>Enabled | Allow PCI cards that do not contain their own VGA color palette to access the video core's palette |
| PERR# Generation | **Disabled**<br>Enabled | Enables or Disables PCI Device to Generate PERR#. |
| SERR# Generation | **Disabled**<br>Enabled | Enables/Disables PCI Device to Generate SERR#. |
| PCI Express Configuration | Submenu | |

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### 7.3.7.1. PCI and PCIe > PCI Express Configuration

| Feature | Options | Description |
|---|---|---|
| PEG Configuration | Info only | |
| PCI Express Clock Gating | Disabled<br>**Enable** | Enable/Disable PCI Express Clock Gating for each root port. |
| DMI Link ASPM Control | Disabled<br>**Enable** | ontrol of Active State Power Management on both NB side and SB side of the DMI Link. |
| Port8xh Decode | Disabled | Port8xh Decode |
| Compliance Test Mode | Disabled | Compliance Test Mode |
| PCI Express Gen3 EQ Lanes | Submenu | |
| PCI Express Root Port X | Submenu | |

#### PCI and PCIe > PCI Express Configuration > PCI Express Gen3 EQ Lanes

| Feature | Options | Description |
|---|---|---|
| Override SW EQ settings | **Disabled**<br>Enable | Override SW EQ settings |

#### PCI and PCIe > PCI Express Configuration > PCI Express Root Port X

| Feature | Options | Description |
|---|---|---|
| PCI Express Root Port | Disabled<br>**Enable** | Control the PCI Express Root Port. |
| Topology | Unknown<br>x1<br>x4<br>Sata Express<br>M2 | Identify the SATA Topology: Default, ISATA, Flex, DirectConnect or M2. |
| ASPM Support | **Disabled**<br>L0s<br>L1<br>L0sL1<br>Auto | Set the ASPM Level.<br>Force L0s - Force all links to L0s State<br>Auto - BIOS auto configure;<br>Disabled - Disables ASPM |
| L1 Substates | **Disabled**<br>Enable | PCI Express L1 Substates settings. |
| URR | **Disabled**<br>Enable | Enable/Disable PCI Express Unsupported Request Reporting. |
| FER | **Disabled**<br>Enable | Enable/Disable PCI Express Device Fatal Error Reporting. |
| NFER | **Disabled**<br>Enable | Enable/Disable PCI Express Device Non-Fatal Error Reporting. |
| CER | **Disabled**<br>Enable | Enable/Disable PCI Express Device Correctable Error Reporting. |
| CTO | **Disabled**<br>Enable | Enable/Disable PCI Express Completion Timer TO. |
| SEFE | **Disabled**<br>Enable | Enable/Disable Root PCI Express System Error on Fatal Error. |



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| Feature | Options | Description |
|---|---|---|
| SENFE | **Disabled**<br>Enable | Enable/Disable Root PCI Express System Error on Non-Fatal Error. |
| SECE | **Disabled**<br>Enable | Enable/Disable Root PCI Express System Error on Correctable Error. |
| PME SCI | Disabled<br>**Enable** | Enable/Disable PCI Express PME SCI. |
| Hot Plug | Disabled<br>**Enable** | Enable/Disable PCI Express Hot Plug. |
| PCIe Speed | **Auto**<br>Gen1<br>Gen2 | Select PCI Express port speed. |
| Transmitter Half Swing | **Disabled**<br>Enabled | Transmitter Half Swing Enable/Disable. |
| Detect Non-Compiance | **Disabled**<br>Enable | Detect Non-Compliance PCI Express Device. If enabled, it will take more time at POST time. |
| Extra Bus Reserved | **0** | Extra Bus Reserved (0-7) for bridges behind this Root Bridge. |
| Reseved Memory | **10** | Reserved Memory Range for this Root Bridge. |
| Prefetchable Memory | **10** | Prefetchable Memory Range for this Root Bridge. |
| Reserved I/O | **4** | Reserved I/O (4K/8K/12K/16K/.../48K) Range for this Root Bridge. |
| PCIE Cp | **2** | Gen3 Equalization settings for physical PCIe lane. |
| PCIE Cm | **6** | Gen3 Equalization settings for physical PCIe lane. |
| PCIE LTR | **Disabled**<br>Enable | PCIE Latency Reporting Enable/Disable. |
| PCIE LTR Lock | **Disabled**<br>Enable | PCIE LTR Configuration Lock. |
| PCIEx CLKREQ mapping Override | **Default**<br>No CLKREQ<br>Customer number | PCIE CLKREQ Override for default platform mapping |
| Snoop Latency Ocerrid | Disabled<br>Manual<br>**Auto** | Snoop Latency Ocerride for PCH PCIE. |
| Non Snoop Latency Ocerrid | Disabled<br>Manual<br>**Auto** | Non Snoop Latency Ocerride for PCH PCIE. |

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## 7.3.8. Super IO

| Feature | Options | Description |
|---|---|---|
| Super IO Chip | Info only | |
| W83627DHG Super IO Configuration | Info only | |
| Serial Port 1 Configuration<br>Serial Port | **Enabled**<br>Disabled | Enable/Disable Serial Port (COM). |
| Device Settings | IO=3F8h; IRQ=4 | Fixed configuration of serial port. |
| Change Settings | **Auto**<br>IO=3F8h; IRQ=4<br>IO=3F8h; IRQ=3,4,5,6,7,10,11,12<br>IO=2F8h; IRQ=3,4,5,6,7,10,11,12<br>IO=3E8h; IRQ=3,4,5,6,7,10,11,12<br>IO=2E8h; IRQ=3,4,5,6,7,10,11,12 | Select an optimal setting for Super IO device. |
| Serial Port 2 Configuration<br>Serial Port | **Enabled**<br>Disabled | Enable/Disable Serial Port (COM). |
| Device Settings | IO=2F8h; IRQ=3 | Fixed configuration of serial port. |
| Change Settings | **Auto**<br>IO=2F8h; IRQ=3<br>IO=3F8h; IRQ=3,4,5,6,7,10,11,12<br>IO=2F8h; IRQ=3,4,5,6,7,10,11,12<br>IO=3E8h; IRQ=3,4,5,6,7,10,11,12<br>IO=2E8h; IRQ=3,4,5,6,7,10,11,12 | Select an optimal setting for Super IO device. |
| Device Mode | **Standard Serial Port Mode**<br>IrDA Active pulse 1.6 uS<br>IrDA Active pulse 3/16 bit time<br>ASKIR Mode | |
| N5104D Super IO Configuration | Info only | |
| Serial Port 1 Configuration<br>Serial Port | **Enabled**<br>Disabled | Enable/Disable Serial Port (COM). |
| Device Settings | IO=240h; IRQ=7 | Fixed configuration of serial port. |
| Change Settings | **Auto**<br>IO=240h; IRQ=7<br>IO=240h; IRQ=3,4,5,6,7,10,11,12<br>IO=248h; IRQ=3,4,5,6,7,10,11,12<br>IO=250h; IRQ=3,4,5,6,7,10,11,12<br>IO=258h; IRQ=3,4,5,6,7,10,11,12 | Select an optimal setting for Super IO device. |

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| Feature | Options | Description |
|---|---|---|
| Serial Port 2 Configuration | | |
| Serial Port | **Enabled**<br>Disabled | Enable/Disable Serial Port (COM). |
| Device Settings | IO=248h; IRQ=5 | Fixed configuration of serial port. |
| Change Settings | **Auto**<br>IO=248h; IRQ=5<br>IO=240h; IRQ=3,4,5,6,7,10,11,12<br>IO=248h; IRQ=3,4,5,6,7,10,11,12<br>IO=250h; IRQ=3,4,5,6,7,10,11,12<br>IO=258h; IRQ=3,4,5,6,7,10,11,12 | Select an optimal setting for Super IO device. |

### 7.3.9. ACPI and Power Management

| Feature | Options | Description |
|---|---|---|
| ACPI and Power Management | Info only | |
| Enable ACPI Auto Configuration | Enabled<br>**Disabled** | Enables or Disables BIOS ACPI Auto Configuration. |
| Enable Hibernation | **Enabled**<br>Disabled | Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS. |
| ACPI Sleep State | **S3 only** | Select ACPI sleep state the system will enter when the SUSPEND button is pressed. |
| Lock Legacy Resources | Enabled<br>**Disabled** | Enables or Disables Lock of Legacy Resources |
| ACPI Low Power S0 Idle | Enabled<br>**Disabled** | Enable or Disable ACPI Low Power S0 Idle Support. |
| Emulation AT/ATX | Emulation AT<br>**ATX** | Select Emulation AT or ATX function. If this option set to [Emulation AT], BIOS will report no suspend functions to ACPI OS. In windows XP, it will make OS show shutdown message during system shutdown. |

### 7.3.10. Sound

| Feature | Options | Description |
|---|---|---|
| Sound | Info only | |
| HD Audio | Disabled<br>Enabled<br>**Auto** | Control Detection of the HD-Audio device.<br>Disabled: HDA will be unconditionally disabled.<br>Enabled: HDA will be unconditionally enabled.<br>Auto: HDA will be enabled if present, disabled other. |

### 7.3.11. Serial Port Console

| Feature | Options | Description |
|---|---|---|
| Serial Port Console | Info only | |
| COM1 | Info only | |
| Console Redirection | Enabled<br>**Disabled** | Console Redirection Enable or Disable. |

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| Feature | Options | Description |
|---|---|---|
| Console Redirection Settings | Submenu | |
| COM2 | Info only | |
| Console Redirection | Enabled<br>**Disabled** | Console Redirection Enable or Disable. |
| Console Redirection Settings | Submenu | |
| COM3 | Info only | |
| Console Redirection | Enabled<br>**Disabled** | Console Redirection Enable or Disable. |
| Console Redirection Settings | Submenu | |
| COM4 | Info only | |
| Console Redirection | Enabled<br>**Disabled** | Console Redirection Enable or Disable. |
| Console Redirection Settings | Submenu | |

### 7.3.11.1. Serial Port Console > Console Redirection Settings

| Feature | Options | Description |
|---|---|---|
| Console Redirection Settings | Info only | |
| Terminal Type | VT100<br>VT100+<br>VT-UTF8<br>**ANSI** | Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes. |
| Bits per second | 9600<br>19200<br>38400<br>57600<br>**115200** | Selects serial port transmission speed. |
| Data Bits | 7<br>**8** | Select Data Bits. |
| Parity | **None**<br>Even<br>Odd<br>Mark<br>Space | Select Parity. |
| Stop Bits | 1<br>**2** | Select number of stop bits. |
| Flow Control | **None**<br>Hardware RTS/CTS | Select flow control. |
| VT-UTF8 Combo Key Support | Disabled<br>**Enable** | Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals. |
| Recorder Mode | **Disabled**<br>Enable | With this mode enabled only text will be sent. This is to capture Terminal data. |
| Resolution 100x31 | **Disabled**<br>Enable | Enables or disables extended terminal resolution |
| Legacy OS Redirection | **80x24** | On Legacy OS, the Number of Rows and Columns supported redirection |



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| Feature | Options | Description |
|---|---|---|
| | 80x25 | |
| Putty KeyPad | **VT100**<br>LINUX<br>XTERMR6<br>SCO<br>ESCN<br>VT400 | Select FunctionKey and KeyPad on Putty. |
| Redirection After BIOS Post | **Always Enabled**<br>BootLoader | The Settings specify if BootLoader is selected than Legacy console redirection is disabled before booting to Legacy OS. Default value is Always Enable which means Legaacy console Redirection is enabled for Legacy OS. |

### 7.3.11.2. ICC Configuration

| Feature | Options | Description |
|---|---|---|
| ICC Information | Info only | |
| ICC PLL Shutdown | Disabled<br>**Enabled** | This option controls the programming of the ICC PLL shutdown flow. When enabled,this ICC PM register will be programmed on every non-Sx boot. |

**Note1:** The item is view only in standard BIOS default, the options can be opened by customer request if neccessary.

## 7.3.12. Thermal

| Feature | Options | Description |
|---|---|---|
| Thermal | Info only | |
| Active Trip Point | Disabled<br>40 C<br>50 C<br>60 C<br>70 C<br>**BMC Default** | This value controls the temperature of the ACPI Active Trip Point - the point in which the OS will turn the processor fan on Active Trip Point Fan Speed. |
| Passive Trip Point | **Disabled**<br>80 C<br>90 C | This value controls the temperature of the ACPI Passive Trip Point - the point in which the OS will begin throttling the processor. |
| Critical Trip Point | **Disabled**<br>85 C<br>95 C | This value controls the temperature of the ACPI Critical Trip Point - the point in which the OS will shut the system off.<br>NOTE: 100C is the Plan Of Record (POR) for all Intel mobile processors. |
| Watchdog ACPI Even Shutdown | **Disabled**<br>Enable | Enable/Disable Watchdog ACPI Even Shutdown. |

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## 7.3.13. Miscellaneous

| Feature | Options | Description |
|---|---|---|
| Trusted Computing | Submenu | |
| NVME Configuration | Submenu | |

### 7.3.13.1. Miscellaneous > Trusted Computing

| Feature | Options | Description |
|---|---|---|
| Security Device Support | **Enabled**<br>Disabled | Enables or Disables BIOS support for security device.<br>When disabled OS wil not show Security Device. TCG EFI protocol and INT1A interface will not be available |
| TPM State | **Enabled**<br>Disabled | Enable/Disable Security Device. NOTE: Your Computer will reboot during restart in order to change State of the Device. |
| Pending operation | **None**<br>TPM Clear | Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device. |
| Device Start | TPM 1.2<br>TPM 2.0<br>**Auto** | TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated |

### 7.3.13.2. Miscellaneous > NVME Configuration

| Feature | Options | Description |
|---|---|---|
| NVME controller and Drive information | Info Only | |

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## 7.4. Boot

### 7.4.1. Boot Configuration

| Feature | Options | Description |
|---|---|---|
| Fast Boot | **Enabled**<br>Disabled | Enables or disables booting with the initialization of a minimal set of devices required to launch the active boot option. Has no effect on BBS options. |
| SATA Support | **Last Boot HDD Only**<br>All Sata Devices | |
| VGA Support | Auto<br>**EFI Driver** | If set to Auto, only the legacy OpRom will be installed with a Legacy OS, and the logo will **not** be displayed during the boot process. The EFI driver will still be installed with an EFI OS. |
| USB Support | Disabled<br>**Full Initial**<br>Partial Initial | If disabled, all USB devices will not be available until after the OS boots. If set to partial initial, USB mass storage and specific USB ports/devices will not be available before the OS boots. If enabled, all USB devices will be available during both POST and in the OS. |
| PS2 Devices Support | **Enabled**<br>Disabled | If disabled, PS2 devices will be skipped. |
| Netowrtk Stack Driver Support | Enabled<br>**Disabled** | If disabled, the Network Stack Driver will be skipped. |
| Redirection Support | Enabled<br>**Disabled** | If disabled, the redirection function will be disabled. |
| New Boot Option Policy | Default<br>**Place First**<br>Place Last | Controls the placement of newly detected UEFI boot options. |

#### 7.4.1.1. CSM Configuration

| Feature | Options | Description |
|---|---|---|
| CSM Support | **Enabled**<br>Disable | This option controls if CSM will be launched. |
| CSM16 Module Version | Info only | |
| GateA20 Active | **Upon Request**<br>Always | UPON REQUEST - GA20 can be disabled using BIOS services. ALWAYS - do not allow disabling GA20; this option is useful when any RT code is executed above 1MB. |
| Option ROM Messages | **Force BIOS**<br>Keep Current | Set display mode for Option ROM. |
| INT19 Trap Response | **Immediate**<br>Postponed | BIOS reaction on INT19 trapping by Option ROM |
| Boot Option filter | **UEFI and Legacy**<br>Legacy only<br>UEFI only | This option controls what devices system can to boot. |
| Option ROM execution | Info only | |
| Network | **Do not launch**<br>Legacy only<br>UEFI only | Controls the execution of UEFI and Legacy PXE OpROM. |
| Storage | Do not launch<br>UEFI only | Controls the execution of UEFI and Legacy Storage OpROM. |

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| | | |
|---|---|---|
| | **Legacy only** | |
| Video | Do not launch<br>UEFI only<br>**Legacy only** | Controls the execution of UEFI and Legacy Video OpROM. |
| Other PCI devices | UEFI OpROM<br>Legacy OpROM | For PCI devices other than Network, Mass storage or Video defines which OpROM to launch. |

## 7.5. Security

### 7.5.1. Password Description

| Feature | Options | Description |
|---|---|---|
| Administrator Password | Enter password | |
| User Password | Enter password | |
| HDD Security Configuration: | Info only | |
| Px: xxxxxxxx | Info only | |

## 7.6. Save & Exit

### 7.6.1. Reset Options

| Feature | Options | Description |
|---|---|---|
| Save Changes and Reset | Save changes and reset the system. | Save Changes and Reset |
| Discard Changes and Reset | Reset the system without saving any changes. | Discard Changes and Reset |

### 7.6.2. Save Options

| Feature | Options | Description |
|---|---|---|
| Save Changes | | Save Changes done so far to any of the setup options. |
| Discard Changes | | Discard Changes done so far to any of the setup options. |
| Restore Defaults | | Restore/Load Default values for all the setup options. |
| Save as User Defaults | | Save the changes done so far as User Defaults. |
| Restore User Defaults | | Restore the User Defaults to all the setup options. |

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# 8. BIOS Checkpoints, Beep Codes

This section of this document lists checkpoints and beep codes generated by AMI Aptio BIOS. The checkpoints defined in this document are inherent to the AMIBIOS generic core, and do not include any chipset or board specific checkpoint definitions.

**Checkpoints and Beep Codes Definition**

A checkpoint is either a byte or word value output to I/O port 80h. The BIOS outputs checkpoints throughout bootblock and Power-On Self Test (POST) to indicate the task the system is currently executing. Checkpoints are very useful for debugging problems that occur during the preboot process.

Beep codes are used by the BIOS to indicate a serious or fatal error. They are used when an error occurs before the system video has been initialized, and generated by the system board speaker.

**Aptio Boot Flow**

While performing the functions of the traditional BIOS, Aptio 5.x core follows the firmware model described by the Intel Platform Innovation Framework for EFI ("the Framework"). The Framework refers the following "boot phases", which may apply to various status code & checkpoint descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization[1]
- Driver Execution Environment (DXE) – main hardware initialization[2]
- Boot Device Selection (BDS) – system setup, pre-OS user interface & selecting a bootable device (CD/DVD, HDD, USB, Network, Shell, …)

**Viewing BIOS Checkpoints**

Viewing all checkpoints generated by the BIOS requires a checkpoint card, also referred to as a POST Card or POST Diagnostic Card. These are PCI add-in cards that show the value of I/O port 80h on a LED display.

Some computers display checkpoints in the bottom right corner of the screen during POST. This display method is limited, since it only displays checkpoints that occur after the video card has been activated.

Keep in mind that not all computers using AMI Aptio BIOS enable this feature. In most cases, a checkpoint card is the best tool for viewing AMI Aptio BIOS checkpoints.

[1]Analogous to "bootblock" functionality of legacy BIOS
[2]Analogous to "POST" functionality in legacy BIOS

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## 8.1. Status Code Ranges

| Status Code Range | Description |
|---|---|
| 0x01 – 0x0B | SEC execution |
| 0x0C – 0x0F | SEC errors |
| 0x10 – 0x2F | PEI execution up to and including memory detection |
| 0x30 – 0x4F | PEI execution after memory detection |
| 0x50 – 0x5F | PEI errors |
| 0x60 – 0x8F | DXE execution up to BDS |
| 0x90 – 0xCF | BDS execution |
| 0xD0 – 0xDF | DXE errors |
| 0xE0 – 0xE8 | S3 Resume (PEI) |
| 0xE9 – 0xEF | S3 Resume errors (PEI) |
| 0xF0 – 0xF8 | Recovery (PEI) |
| 0xF9 – 0xFF | Recovery errors (PEI) |

## 8.2. Standard Status Codes

### 8.2.1. SEC Phase

| Status Code | Description |
|---|---|
| 0x00 | Not used |
| **Progress Codes** | |
| 0x01 | Power on. Reset type detection (soft/hard). |
| 0x02 | AP initialization before microcode loading |
| 0x03 | North Bridge initialization before microcode loading |
| 0x04 | South Bridge initialization before microcode loading |
| 0x05 | OEM initialization before microcode loading |
| 0x06 | Microcode loading |
| 0x07 | AP initialization after microcode loading |
| 0x08 | North Bridge initialization after microcode loading |
| 0x09 | South Bridge initialization after microcode loading |
| 0x0A | OEM initialization after microcode loading |
| 0x0B | Cache initialization |

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| SEC Error Codes | |
|---|---|
| 0x0C – 0x0D | Reserved for future AMI SEC error codes |
| 0x0E | Microcode not found |
| 0x0F | Microcode not loaded |

### 8.2.2. SEC Beep Codes

None

### 8.2.3. PEI Phase

| Status Code | Description |
|---|---|
| **Progress Codes** | |
| 0x10 | PEI Core is started |
| 0x11 | Pre-memory CPU initialization is started |
| 0x12 | Pre-memory CPU initialization (CPU module specific) |
| 0x13 | Pre-memory CPU initialization (CPU module specific) |
| 0x14 | Pre-memory CPU initialization (CPU module specific) |
| 0x15 | Pre-memory North Bridge initialization is started |
| 0x16 | Pre-Memory North Bridge initialization (North Bridge module specific) |
| 0x17 | Pre-Memory North Bridge initialization (North Bridge module specific) |
| 0x18 | Pre-Memory North Bridge initialization (North Bridge module specific) |
| 0x19 | Pre-memory South Bridge initialization is started |
| 0x1A | Pre-memory South Bridge initialization (South Bridge module specific) |
| 0x1B | Pre-memory South Bridge initialization (South Bridge module specific) |
| 0x1C | Pre-memory South Bridge initialization (South Bridge module specific) |
| 0x1D – 0x2A | OEM pre-memory initialization codes |
| 0x2B | Memory initialization. Serial Presence Detect (SPD) data reading |
| 0x2C | Memory initialization. Memory presence detection |
| 0x2D | Memory initialization. Programming memory timing information |
| 0x2E | Memory initialization. Configuring memory |
| 0x2F | Memory initialization (other). |
| 0x30 | Reserved for ASL (see ASL Status Codes section below) |
| 0x31 | Memory Installed |
| 0x32 | CPU post-memory initialization is started |
| 0x33 | CPU post-memory initialization. Cache initialization |
| 0x34 | CPU post-memory initialization. Application Processor(s) (AP) initialization |
| 0x35 | CPU post-memory initialization. Boot Strap Processor (BSP) selection |

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| Status Code | Description |
|---|---|
| 0x36 | CPU post-memory initialization. System Management Mode (SMM) initialization |
| 0x37 | Post-Memory North Bridge initialization is started |
| 0x38 | Post-Memory North Bridge initialization (North Bridge module specific) |
| 0x39 | Post-Memory North Bridge initialization (North Bridge module specific) |
| 0x3A | Post-Memory North Bridge initialization (North Bridge module specific) |
| 0x3B | Post-Memory South Bridge initialization is started |
| 0x3C | Post-Memory South Bridge initialization (South Bridge module specific) |
| 0x3D | Post-Memory South Bridge initialization (South Bridge module specific) |
| 0x3E | Post-Memory South Bridge initialization (South Bridge module specific) |
| 0x3F-0x4E | OEM post memory initialization codes |
| 0x4F | DXE IPL is started |
| **PEI Error Codes** | |
| 0x50 | Memory initialization error. Invalid memory type or incompatible memory speed |
| 0x51 | Memory initialization error. SPD reading has failed |
| 0x52 | Memory initialization error. Invalid memory size or memory modules do not match. |
| 0x53 | Memory initialization error. No usable memory detected |
| 0x54 | Unspecified memory initialization error. |
| 0x55 | Memory not installed |
| 0x56 | Invalid CPU type or Speed |
| 0x57 | CPU mismatch |
| 0x58 | CPU self test failed or possible CPU cache error |
| 0x59 | CPU micro-code is not found or micro-code update is failed |
| 0x5A | Internal CPU error |
| 0x5B | reset PPI is not available |
| 0x5C-0x5F | Reserved for future AMI error codes |
| **S3 Resume Progress Codes** | |
| 0xE0 | S3 Resume is stared (S3 Resume PPI is called by the DXE IPL) |
| 0xE1 | S3 Boot Script execution |
| 0xE2 | Video repost |
| 0xE3 | OS S3 wake vector call |
| 0xE4-0xE7 | Reserved for future AMI progress codes |
| **S3 Resume Error Codes** | |
| 0xE8 | S3 Resume Failed |
| 0xE9 | S3 Resume PPI not Found |
| 0xEA | S3 Resume Boot Script Error |

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| Status Code | Description |
|---|---|
| 0xEB | S3 OS Wake Error |
| 0xEC-0xEF | Reserved for future AMI error codes |
| **Recovery Progress Codes** | |
| 0xF0 | Recovery condition triggered by firmware (Auto recovery) |
| 0xF1 | Recovery condition triggered by user (Forced recovery) |
| 0xF2 | Recovery process started |
| 0xF3 | Recovery firmware image is found |
| 0xF4 | Recovery firmware image is loaded |
| 0xF5-0xF7 | Reserved for future AMI progress codes |
| **Recovery Error Codes** | |
| 0xF8 | Recovery PPI is not available |
| 0xF9 | Recovery capsule is not found |
| 0xFA | Invalid recovery capsule |
| 0xFB – 0xFF | Reserved for future AMI error codes |

### 8.2.4. PEI Beep Codes

| # of Beeps | Description |
|---|---|
| 1 | Memory not Installed |
| 1 | Memory was installed twice (InstallPeiMemory routine in PEI Core called twice) |
| 2 | Recovery started |
| 3 | DXEIPL was not found |
| 3 | DXE Core Firmware Volume was not found |
| 4 | Recovery failed |
| 4 | S3 Resume failed |
| 7 | Reset PPI is not available |

### 8.2.5. DXE Status Codes

| Status Code | Description |
|---|---|
| 0x60 | DXE Core is started |
| 0x61 | NVRAM initialization |
| 0x62 | Installation of the South Bridge Runtime Services |
| 0x63 | CPU DXE initialization is started |
| 0x64 | CPU DXE initialization (CPU module specific) |
| 0x65 | CPU DXE initialization (CPU module specific) |

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| Status Code | Description |
|---|---|
| 0x66 | CPU DXE initialization (CPU module specific) |
| 0x67 | CPU DXE initialization (CPU module specific) |
| 0x68 | PCI host bridge initialization |
| 0x69 | North Bridge DXE initialization is started |
| 0x6A | North Bridge DXE SMM initialization is started |
| 0x6B | North Bridge DXE initialization (North Bridge module specific) |
| 0x6C | North Bridge DXE initialization (North Bridge module specific) |
| 0x6D | North Bridge DXE initialization (North Bridge module specific) |
| 0x6E | North Bridge DXE initialization (North Bridge module specific) |
| 0x6F | North Bridge DXE initialization (North Bridge module specific) |
| 0x70 | South Bridge DXE initialization is started |
| 0x71 | South Bridge DXE SMM initialization is started |
| 0x72 | South Bridge devices initialization |
| 0x73 | South Bridge DXE Initialization (South Bridge module specific) |
| 0x74 | South Bridge DXE Initialization (South Bridge module specific) |
| 0x75 | South Bridge DXE Initialization (South Bridge module specific) |
| 0x76 | South Bridge DXE Initialization (South Bridge module specific) |
| 0x77 | South Bridge DXE Initialization (South Bridge module specific) |
| 0x78 | ACPI module initialization |
| 0x79 | CSM initialization |
| 0x7A – 0x7F | Reserved for future AMI DXE codes |
| 0x80 – 0x8F | OEM DXE initialization codes |
| 0x90 | Boot Device Selection (BDS) phase is started |
| 0x91 | Driver connecting is started |
| 0x92 | PCI Bus initialization is started |
| 0x93 | PCI Bus Hot Plug Controller Initialization |
| 0x94 | PCI Bus Enumeration |
| 0x95 | PCI Bus Request Resources |
| 0x96 | PCI Bus Assign Resources |
| 0x97 | Console Output devices connect |
| 0x98 | Console input devices connect |
| 0x99 | Super IO Initialization |
| 0x9A | USB initialization is started |
| 0x9B | USB Reset |
| 0x9C | USB Detect |

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| Status Code | Description |
|---|---|
| 0x9D | USB Enable |
| 0x9E – 0x9F | Reserved for future AMI codes |
| 0xA0 | IDE initialization is started |
| 0xA1 | IDE Reset |
| 0xA2 | IDE Detect |
| 0xA3 | IDE Enable |
| 0xA4 | SCSI initialization is started |
| 0xA5 | SCSI Reset |
| 0xA6 | SCSI Detect |
| 0xA7 | SCSI Enable |
| 0xA8 | Setup Verifying Password |
| 0xA9 | Start of Setup |
| 0xAA | Reserved for ASL (see ASL Status Codes section below) |
| 0xAB | Setup Input Wait |
| 0xAC | Reserved for ASL (see ASL Status Codes section below) |
| 0xAD | Ready To Boot event |
| 0xAE | Legacy Boot event |
| 0xAF | Exit Boot Services event |
| 0xB0 | Runtime Set Virtual Address MAP Begin |
| 0xB1 | Runtime Set Virtual Address MAP End |
| 0xB2 | Legacy Option ROM Initialization |
| 0xB3 | System Reset |
| 0xB4 | USB hot plug |
| 0xB5 | PCI bus hot plug |
| 0xB6 | Clean-up of NVRAM |
| 0xB7 | Configuration Reset (reset of NVRAM settings) |
| 0xB8 – 0xBF | Reserved for future AMI codes |
| 0xC0 – 0xCF | OEM BDS initialization codes |
| **DXE Error Codes** | |
| 0xD0 | CPU initialization error |
| 0xD1 | North Bridge initialization error |
| 0xD2 | South Bridge initialization error |
| 0xD3 | Some of the Architectural Protocols are not available |
| 0xD4 | PCI resource allocation error. Out of Resources |
| 0xD5 | No Space for Legacy Option ROM |

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| Status Code | Description |
|---|---|
| 0xD6 | No Console Output Devices are found |
| 0xD7 | No Console Input Devices are found |
| 0xD8 | Invalid password |
| 0xD9 | Error loading Boot Option (LoadImage returned error) |
| 0xDA | Boot Option is failed (StartImage returned error) |
| 0xDB | Flash update is failed |
| 0xDC | Reset protocol is not available |

### 8.2.6. DXE Beep Codes

| # of Beeps | Description |
|---|---|
| 1 | Invalid password |
| 4 | Some of the Architectural Protocols are not available |
| 5 | No Console Output Devices are found |
| 5 | No Console Input Devices are found |
| 6 | Flash update is failed |
| 7 | Reset protocol is not available |
| 8 | Platform PCI resource requirements cannot be met |

### 8.2.7. ACPI/ASL Checkpoint

| Status Code | Description |
|---|---|
| 0x01 | System is entering S1 sleep state |
| 0x02 | System is entering S2 sleep state |
| 0x03 | System is entering S3 sleep state |
| 0x04 | System is entering S4 sleep state |
| 0x05 | System is entering S5 sleep state |
| 0x10 | System is waking up from the S1 sleep state |
| 0x20 | System is waking up from the S2 sleep state |
| 0x30 | System is waking up from the S3 sleep state |
| 0x40 | System is waking up from the S4 sleep state |
| 0xAC | System has transitioned into ACPI mode. Interrupt controller is in PIC mode. |
| 0xAA | System has transitioned into ACPI mode. Interrupt controller is in APIC mode. |

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## 8.3. OEM-Reserved Checkpoint Ranges

| Status Code | Description |
|---|---|
| 0x05 | OEM SEC initialization before microcode loading |
| 0x0A | OEM SEC initialization after microcode loading |
| 0x1D – 0x2A | OEM pre-memory initialization codes |
| 0x3F – 0x4E | OEM PEI post memory initialization codes |
| 0x80 – 0x8F | OEM DXE initialization codes |
| 0xC0 – 0xCF | OEM BDS initialization codes |

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# 9. Mechanical Information

## 9.1. Board-to-Board Connectors

To allow for different stacking heights, the receptacles for COM Express carrier boards are available in two heights: 5 mm and 8 mm. When 5 mm receptacles are chosen, the carrier board should be free of components.

**Tyco 3-1827253-6**

**Foxconn QT002206-2131-3H**

- 220-pin board-to-board connector with 0.5mm for a stacking height of 5 mm.
- This connector can be used with 5 mm through-hole standoffs (SMT type).



**Tyco 3-6318491-6**

**Foxconn QT002206-4141-3H**

- 220-pin board-to-board connector with 0.5mm for a stacking height of 8 mm.
- This connector can be used with 8 mm through-hole standoffs (SMT type).



**Common Specifications**

- Current capacity: 0.5A per pin
- Rated voltage: 50 VAC
- Insulation resistance: 100M or greater @ 500 VDC
- Temperature rating: -40°C ~ 85°C
- UL certification (ECBT2.E28476)
- Copper alloy (contacts)
- Housing: thermo-plastic molded compound (L.C.P.)

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## 9.2. Thermal Solution

### 9.2.1. Heat Spreaders

The function of the heat spreader is to ensure an identical mechanical profile for all COM Express modules. By using a heat spreader, the thermal solution that is built on top of the module is compatible with all COM Express modules.

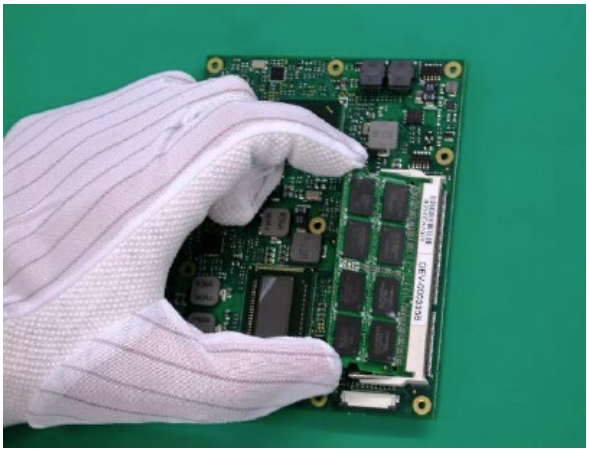
### 9.2.2. Heat Sinks

A heat sink can be used as a thermal solution for a specific COM Express module and can have a fan or be fanless, depending on the thermal requirements.

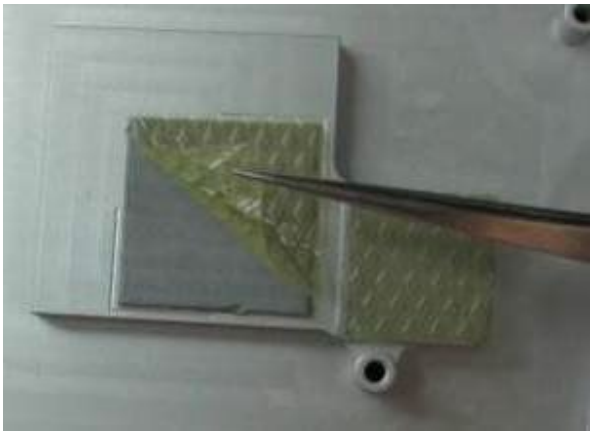
### 9.2.3. Installation

Install a heat spreader or heat sink using the following instructions.

Step 1: Before mounting the heatsink, install the required memory modules onto the SODIMM socket(s) on the COM Express module.



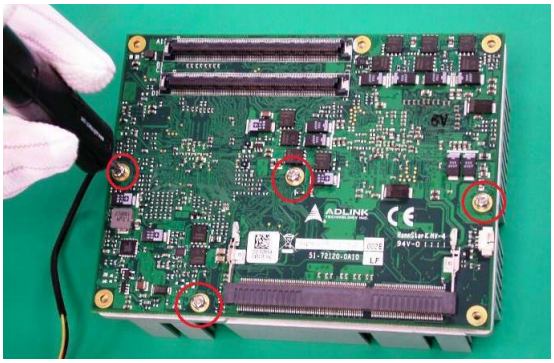
Step 2: Remove the protective membranes from the thermal pads.



Step 3: Assemble the heatsink onto the COM Express module.

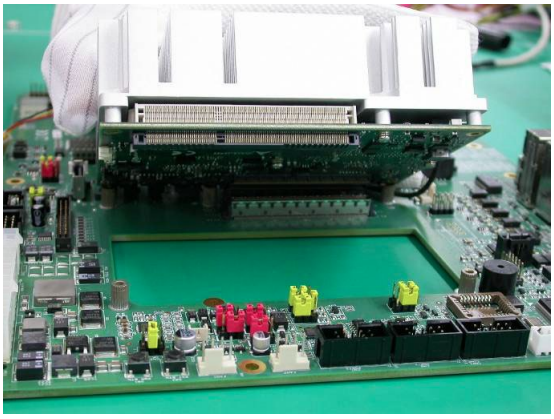
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Step 4: Use the four M2.5, L=6mm screws provided to fasten the heatsink to the module.



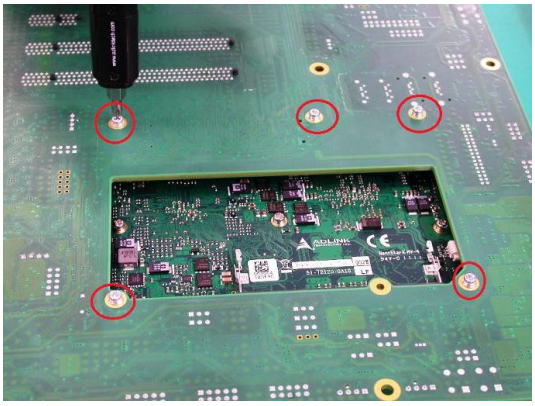


Step 5: Place the COM Express module and heatsink assembly onto the connectors on the carrier board as shown.



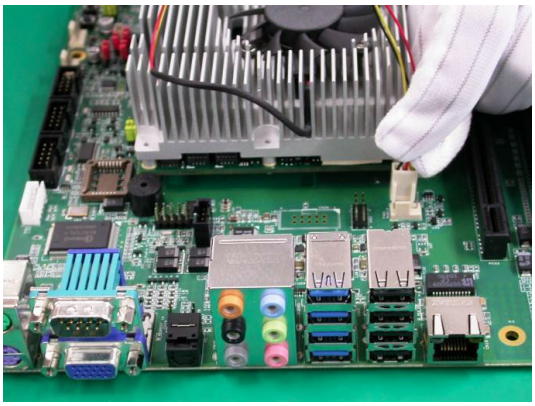
Then press down on the module until it is firmly seated on the carrier board.

Step 6: Use the five M2.5, L=16mm screws provided to secure the COM Express module to the carrier board from the solder side.





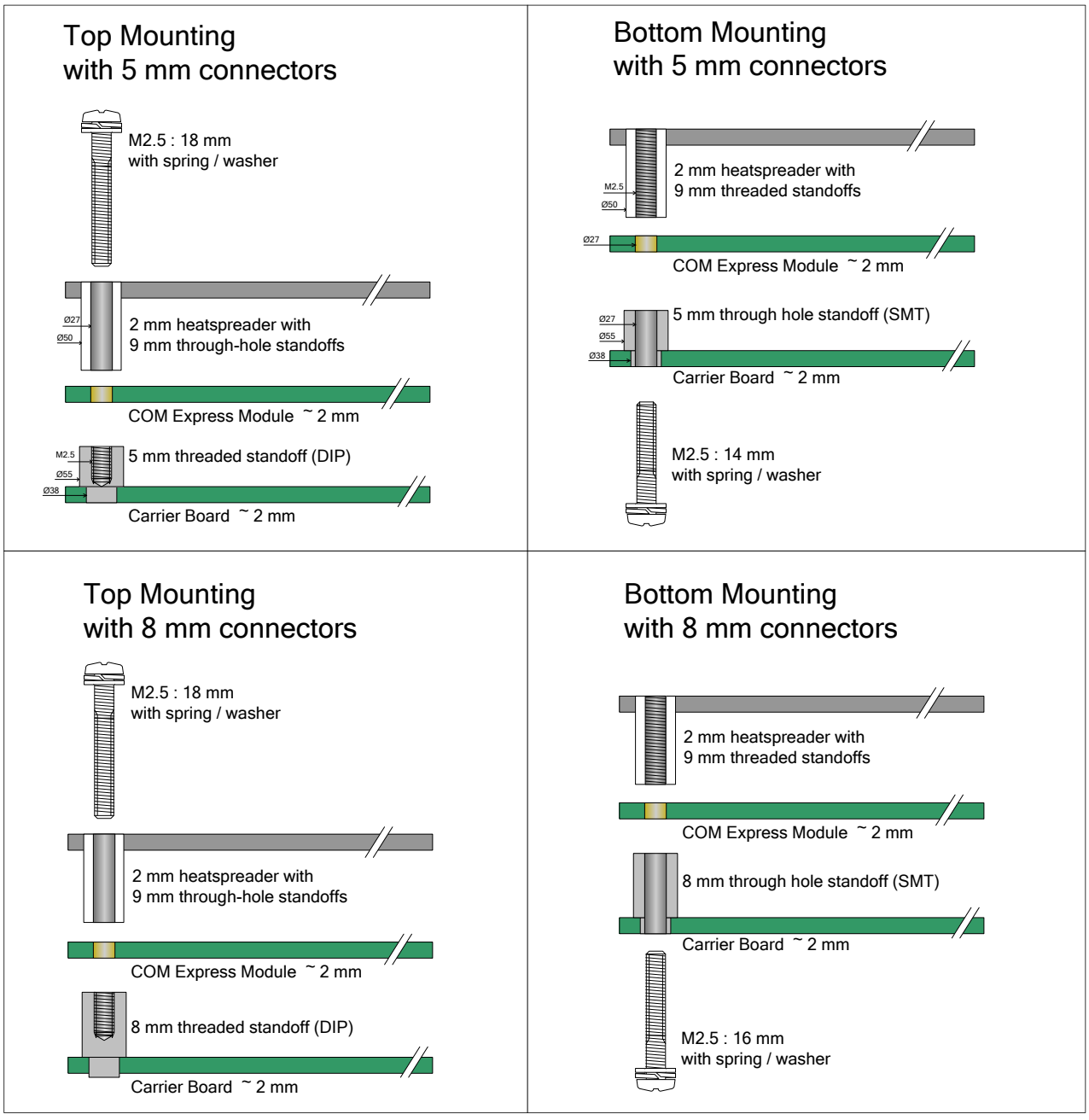
Step 7: If you are installing a heatsink with a fan, plug the fan connector into the carrier board as shown.



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## 9.3. Mounting Methods

There are several standard ways to mount the COM Express module with a thermal solution onto a carrier board. In addition to the choice of 5 mm or 8mm board-to-board connectors, there is the choice of Top and Bottom mounting. In Top mounting, the threaded standoffs are on the carrier board and the thermal solution is equipped with through-hole standoffs. In Bottom mounting, the threaded standoffs are on the thermal solution and the carrier board has through-hole standoffs.



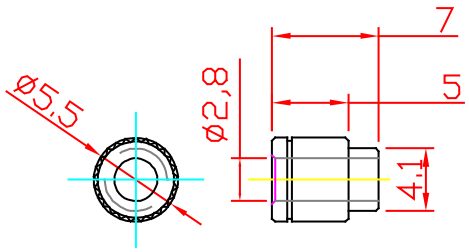

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## 9.4. Standoff Types

The standoffs available for Top and Bottom mounting methods are shown below. Note that threaded standoffs are DIP type and through-hole standoffs are SMT type. Other types not listed are available upon request.

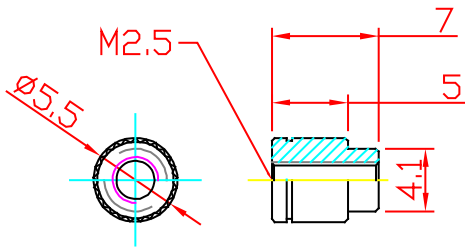
**5mm through-hole standoff (SMT type)**

**P/N: 33-72000-0050**



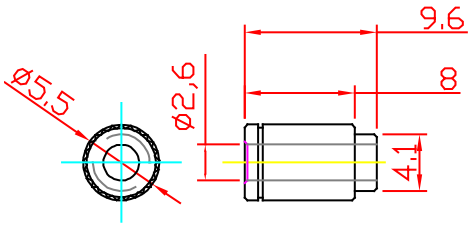

**5mm threaded standoff (DIP type)**

**P/N: 33-72016-0050**



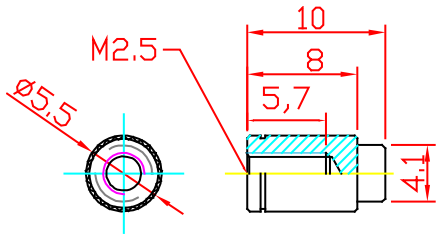

**8mm through-hole standoff (SMT type)**

**P/N: 33-72000-0080**




**8mm threaded standoff (DIP type)**

**P/N: 33-72015-0050**




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# Safety Instructions

Read and follow all instructions marked on the product and in the documentation before you operate your system. Retain all safety and operating instructions for future use.

- Please read these safety instructions carefully.
- Please keep this User's Manual for later reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment, turn off the power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources.
  - Keep equipment away from high heat or high humidity.
  - Keep equipment properly ventilated (do not block or cover ventilation openings).
  - Make sure to use recommended voltage and power source settings.
  - Always install and operate equipment near an easily accessible electrical socket-outlet.
  - Secure the power cord (do not place any object on/over the power cord).
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings.
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.
- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

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