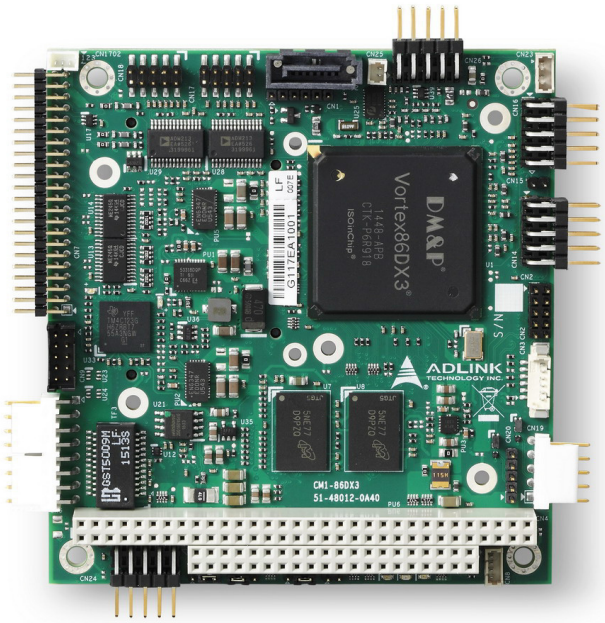
CM1-86DX3

Technical Reference

PC/104 Single Board Computer with Vortex86-DX3 SoC



Manual Rev.:	2.6
Revision Date:	December 30, 2024
Part Number:	50M-48012-2060

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Preface

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Revision History

Revision	Reason for Change	Date
1.0	Initial Release	Oct/15
2.0	Added VGA DDC interface to Chapter 3; revised CFast information; added CFast pinout Chapter 3; transposed CN14 and CN16 headers for COM1 and COM2; added cooling airflow specifications; added Getting Started section to chapter 1; added Component Features section to chapter 2; restructured the format of this manual to four chapters	Jul/16
2.1	Added Appendix B, System Resources; updated Ordering Information in Table 1-1	Jan/18
2.2	Revised RS485/422 mode signals in Table 3-1; changed positions of labels for jumper headers in Figure 2-5; added Prop 65 warning and Battery labels to Preface	Jul/18
2.3	Removed SPI flash support; add heat sink installation	2020-04-24
2.4	Add French safety warnings	2021-02-04
2.5	Update specifications	2022-07-12
2.6	Update heat sink installation	2024-12-30

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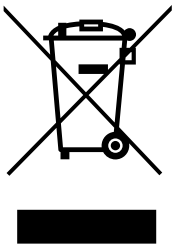
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Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

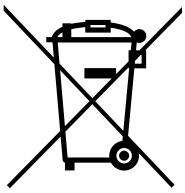
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Battery Labels (for products with battery)









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WARNING: This product can expose you to chemicals including acrylamide, arsenic, benzene, cadmium, Tris(1,3-dichloro-2-propyl)phosphate (TDCPP), 1,4-Dioxane, formaldehyde, lead, DEHP, styrene, DINP, BBP, PVC, and vinyl materials, which are known to the State of California to cause cancer, and acrylamide, benzene, cadmium, lead, mercury, phthalates, toluene, DEHP, DIDP, DnHP, DBP, BBP, PVC, and vinyl materials, which are known to the State of California to cause birth defects or other reproductive harm. For more information go to www.P65Warnings.ca.gov**.**

AVERTISSEMENT: *Ce produit peut vous exposer à des produits chimiques tels que l'acrylamide, l'arsenic, le benzène, le cadmium, le phosphate de tris (1,3-dichloro-2-propyle) (TDCPP), le 1,4-dioxane, le formaldéhyde, le plomb, le DEHP, le styrène, le DINP , BBP, PVC et matériaux en vinyle, qui sont connus dans l'État de Californie pour causer le cancer, et acrylamide, benzène, cadmium, plomb, mercure, phtalates, toluène, DEHP, DIDP, DnHP, DBP, BBP, PVC et vinyle matériaux, qui sont connus de l'État de Californie pour causer des anomalies congénitales ou d'autres troubles de la reproduction. Pour plus d'informations, visitez le site www.P65Warnings.ca.gov.*

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Conventions

The following conventions may be used throughout this manual, denoting special levels of information.



This information adds clarity or specifics to text and illustrations.



MISE EN GARDE

This information indicates the possibility of ***minor*** physical injury, component damage, data loss, and/or program corruption.

*Ces informations indiquent la possibilité de blessures physiques **mineures**, de dommages aux composants, de perte de données et / ou de corruption de programme.*



ATTENTION

This information warns of possible ***serious*** physical injury, component damage, data loss, and/or program corruption.

*Ces informations mettent en garde contre d'éventuelles blessures physiques **graves**, des dommages aux composants, une perte de données et / ou une corruption du programme.*

Important Safety Instructions

For user safety, please read and follow all **Instructions**, **WARNINGs**, **CAUTIONs,** and **NOTEs** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,

If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

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1 Product Overview

1.1 Description

The CM1-86DX3 is a PC/104 Single Board Computer (SBC) based on DMP's Vortex86-DX3 single chip solution, featuring exceptionally high integration and an optimum performance-to-power ratio. The board supports all peripherals needed for an embedded PC on a small 3.55" by 3.77" printed circuit board.

The Vortex86-DX3 chip integrates a powerful yet efficient CPU with graphics, memory, and I/O controller hubs to form a complete PC, with all the standard peripheral connections onboard.

The board provides two Ethernet ports (1x Gbps and 1x 100Mbps), two RS232 serial ports, two RS232/RS422/RS485 serial ports, and two USB 2.0 ports to handle the communication with external devices. A first generation optional SATA interface allows the connection of SSD or CD drives. In addition, an optional CFast card can be used as a boot drive.



The use of external disk drives (HDD/SSD) as boot devices is not recommended.

System expansion is provided over the PC/104 connector.

The CM1-86DX3 is powered by a 5V-only supply and runs DOS, Windows XP/7 and Linux operating systems.

Regarding ACPI: The Vortex 86DX3 SoC does not offer full ACPI support and requires external power management design (standby power design, for example) to simulate power-down functionality. Without full ACPI support, CM1-86DX3 running Window 7 or Linux will not have soft-off functionality. For Windows, users must turn off the system manually at the end of the shutdown process, when the cursor stops blinking.

1.2 About this Manual

This manual presents the supported features of the CM1-86DX3 Single Board Computer (SBC). After reviewing this document you should understand the following features of the CM1-86DX3.

- Board Features
- Functional Block Diagram
- Major Component (IC) Locations and Descriptions
- Header, Connector, and Socket Locations and Descriptions
- Specifications
- Interface Signal Definitions
- Board Utilities

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1.3 Features

SoC ▶ DMP Vortex86-DX3 @ max. 1GHz ▷ X86 Dual-Core Microprocessor ▷ Floating point unit support ▷ Embedded I/D L1 Cache (16K each) ▷ Embedded Unified L2 Cache (512K 4-way) ▷ DDR3 Interface ▷ GPU Control Unit (VGA, 2D Graphics, UMA Architecture) ▷ Embedded 2MB Flash (BIOS storage)	**Main Memory** ▶ 2GB DDR3 Soldered Memory (non-ECC) **Expansion** ▶ 1x 16-bit PC/104 with full DMA capability
Interfaces ▶ 1x Ethernet 1Gbps ▶ 1x Ethernet 100Mbps ▶ 1x SATA 1.5 Gb/s ▶ 1x CFast ▶ PS/2 Keyboard/Mouse ▶ 2x USB 2.0 ports ▶ 2x RS485/RS422/RS232 ▶ 2x RS232 ▶ 1x TTL/VGA	▶ MISC signals: external power button, speaker (5V), external reset button, external battery connector ▶ 1x 8bit GPIO-Port, usable as TTL-UART ▶ 1x, 5V Power Input



Other configurations are possible. Please contact your local ADLINK Technology representative to discuss requirements.

1.4 Ordering Information

Table 1-1: CM1-86DX3 Models

Model Number	Description
CM1-86DX3	PC/104 with Vortex 86DX3, 2GB soldered DDR3, 10/100 Ethernet, GbE, CFast socket, TTL LCD and VGA display

Table 1-2: Cable Sets and Accessories

Model Number	Description
CM1-86DX3-X-01	Adapter Cable Set
CM1-86DX3-TM-20_A5	CM1-86DX3-TM-20_A5 passive heatsink for -40°C to +85°C operating range, with airflow requirements
CM1-86DX3-TM-10_A5	CM1-86DX3-TM-10_A5 passive heatsink for 0°C to +60°C operating range.

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1.5 Block Diagram

Figure 1-1 provides a functional representation of the CM1-86DX3.

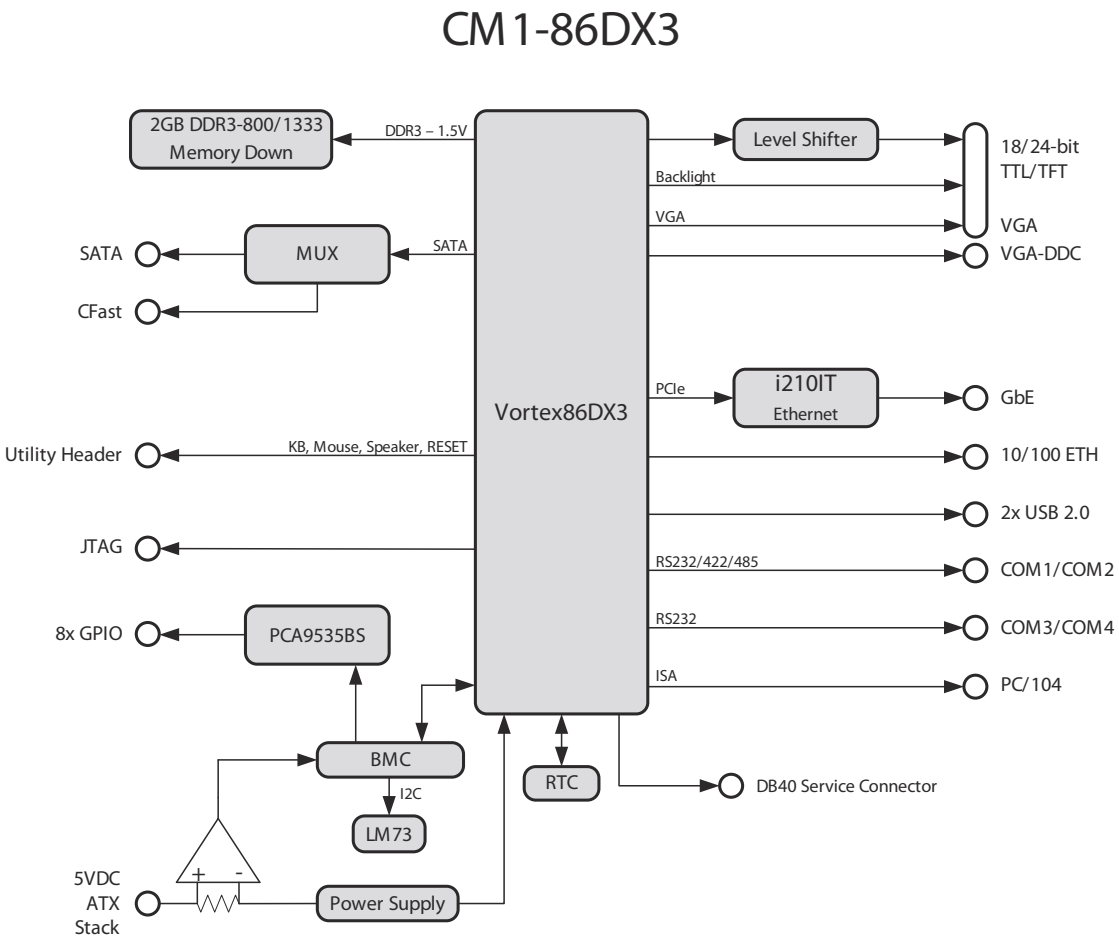


Figure 1-1: Functional Block Diagram

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1.6 Specifications

1.6.1 Physical

Table 1-3 provides the physical dimensions of the module.

Table 1-3: Weight and Footprint Dimensions

Item	Dimension	
Weight	0.12 kg (0.25 lbs)	Overall height is measured from the upper board surface to the highest permanent component (PC/104 bus connector) on the upper board surface. This measurement does not include the heatsink, which can vary. The heatsink could increase this dimension.
Height (overall)	11.05 mm (0.435 inches)	
Board thickness	2.362 mm (0.093 inches)	
Width	90.17 mm (3.55 inches)	
Length	95.86 mm (3.77 inches)	

1.6.2 Mechanical

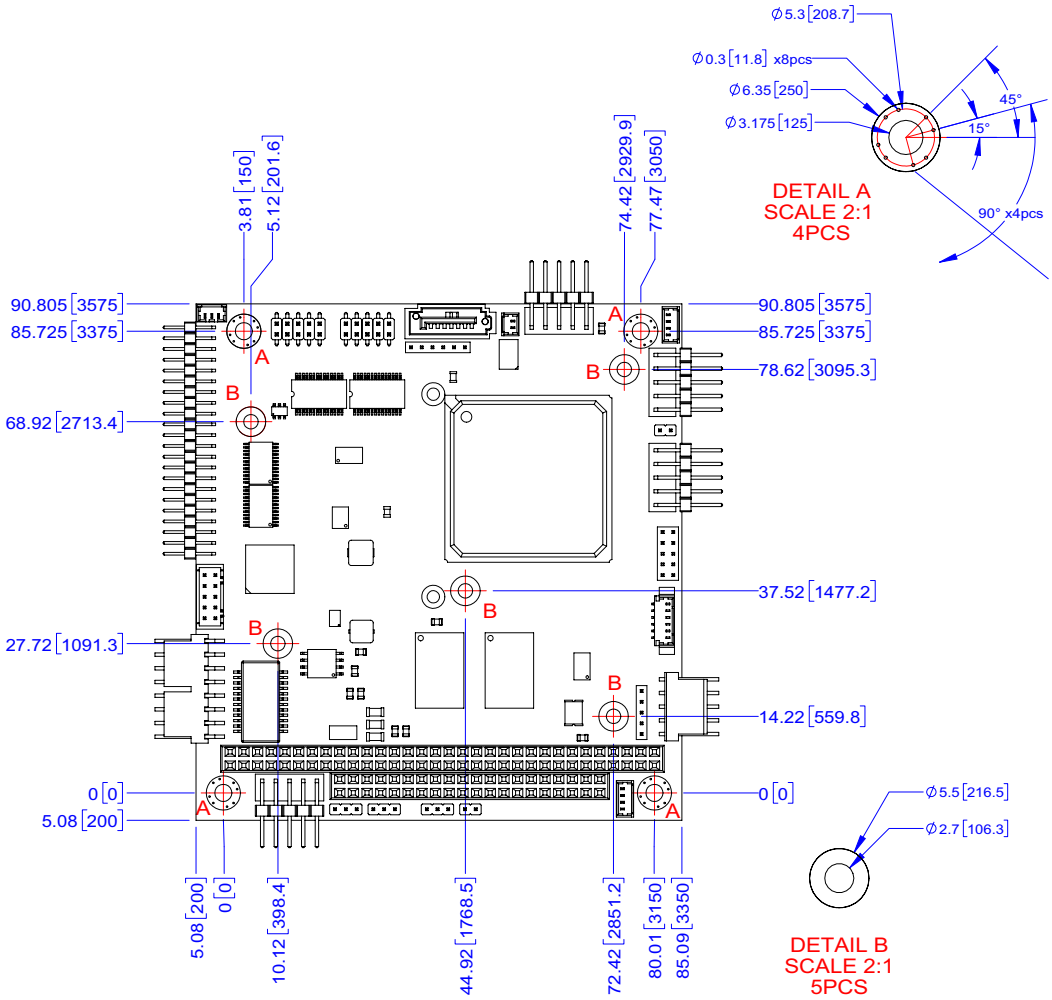


Figure 1-2: Mechanical Overview (Top Side)

NOTE:

All dimensions are given in inches and millimeters. Pin 1 is shown as a solid, black square on headers and connectors.

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1.6.3 Electrical

Table 1-4 specifies the electrical characteristics of the module.

Table 1-4: Electrical Specifications

Parameter	Value
Voltage Input	
Modes	▶ AT, only
Standard	▶ +5V DC +/-5%, =/- 50mV ripple
RTC	▶ 3.0V, 2.0V to 3.3V (battery), +/-30mV ripple
Power States	▶ S3, S4, S5 (S3 and S4 not supported by Windows 7)

1.6.4 Power

Table 1-5 provides the power consumption values of the CM1-86DX3.

Table 1-5: Power Supply Requirements

Parameter	Board Characteristics
Input Type	Regulated DC voltage
Typical Idle Current and Power	1.04A (5.20W) @ 5V
Typical Operating Current and Power	1.25A (6.25W) @ 5V

Operating configurations:

- ▶ Idle operating configuration includes a 1024x768 display, Windows 7, 2GB DDR3 memory, SATA HDD, 4.60 watts power supply
- ▶ Typical operating configuration is the same as the Idle configuration

1.6.5 Environmental

Table 1-6 provides the most efficient operating and storage condition ranges required for this module.

Table 1-6: Environmental Requirements

Parameter	Conditions
Temperature	
Operating	-40° C to +85° C (-40° F to +185° F) NOTE: this temperature range requires the CM1-86DX3-TM-20 passive heatsink with specified airflow.
Storage	–55° C to +85° C (–67° F to +185° F)
Humidity	
Operating	5% to 90% relative humidity, non-condensing
Non-operating	5% to 95% relative humidity, non-condensing

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Table 1-7 provides shock and vibration tests performed on the board.

Table 1-7: Shock and Vibration

Parameter	Result
Shock Test	MIL-STD-202F, Method 213B, Table 213-I, Condition A
Random Vibration Test	MIL-STD-202F, Method 214A, Table 214-I, Condition D

Table 1-8 presents the average times between system failures.

Table 1-8: Mean Time Between Failures

Parameter	Value
MTBF at 25°C	200,000 hrs (according to Bellcore calculation)

1.6.6 Thermal/Cooling Requirements

The CM1-86DX3 is designed to operate at its maximum CPU speed and requires a thermal solution to cool the CPU. ADLINK offers a heat spreader and a passive heatsink (separate order numbers) for cooling. The heatsink can be used for module evaluation. If a custom heatsink is used, it is recommended to connect it to the ADLINK heat spreader. This facilitates future module upgrades without the need to re-design the custom heatsink. Refer to Figure 1-3 for heatsink dimension and mounting information. See Figures 1-4 and 1-5 for airflow requirements.

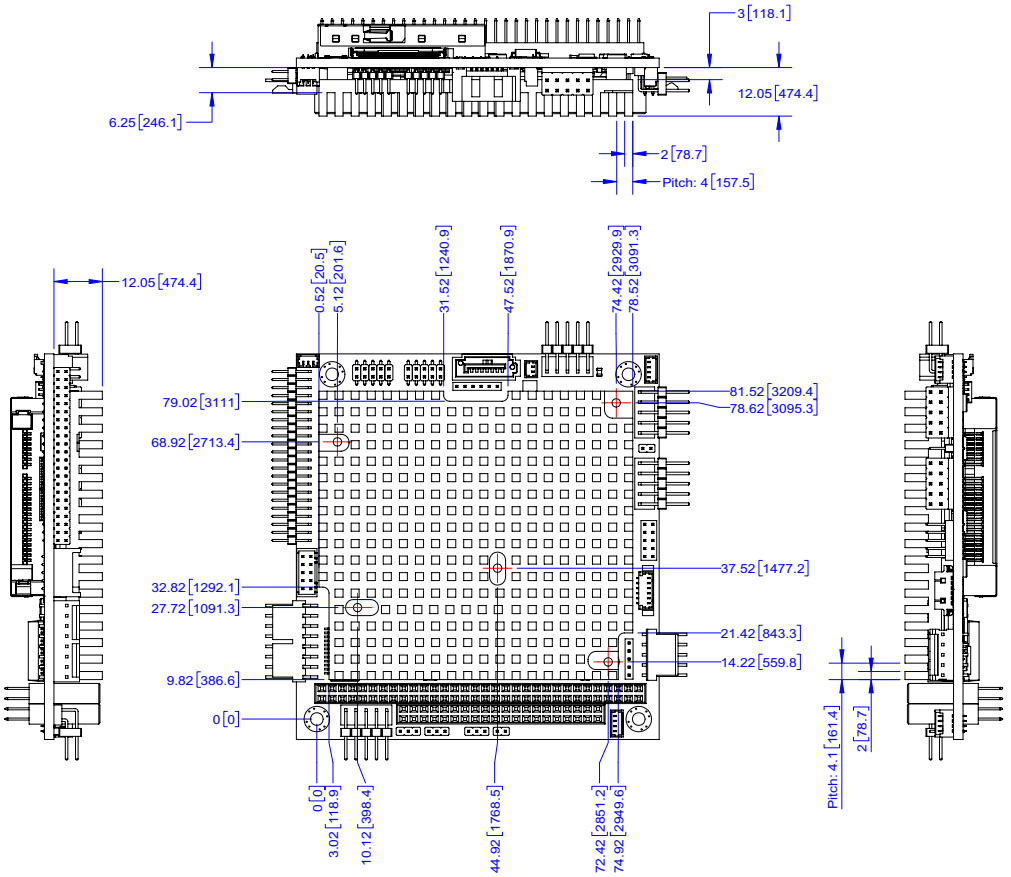


Figure 1-3: Heatsink mounting dimensions (top side)

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Figure 1-4 provides airflow versus temperature ratios with regard to four different airflow directions. See Figure 1-5 for an illustration of the four airflow directions.

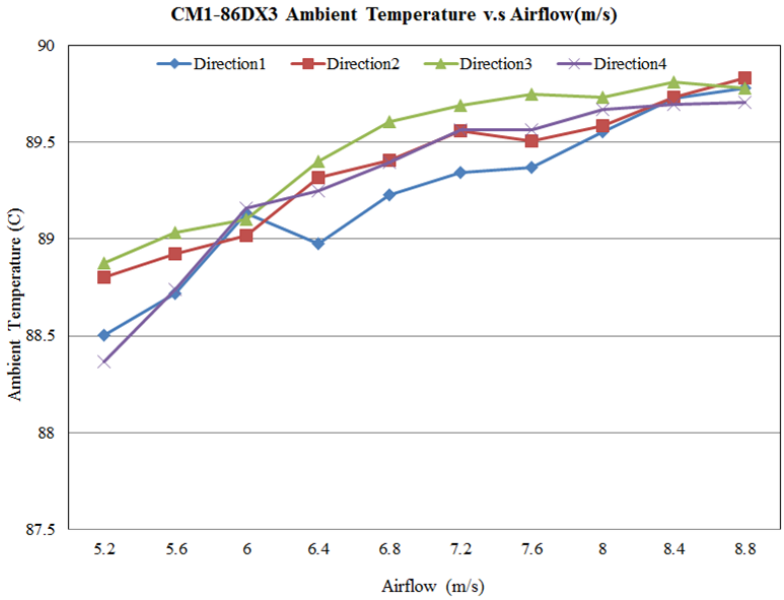


Figure 1-4: Temperature vs Airflow Chart

Figure 1-5 presents four separate directions of airflow across the fins of the passive heatsink. Refer to Figure 1-4 for required airflow ratios with regard to each of the airflow directions.

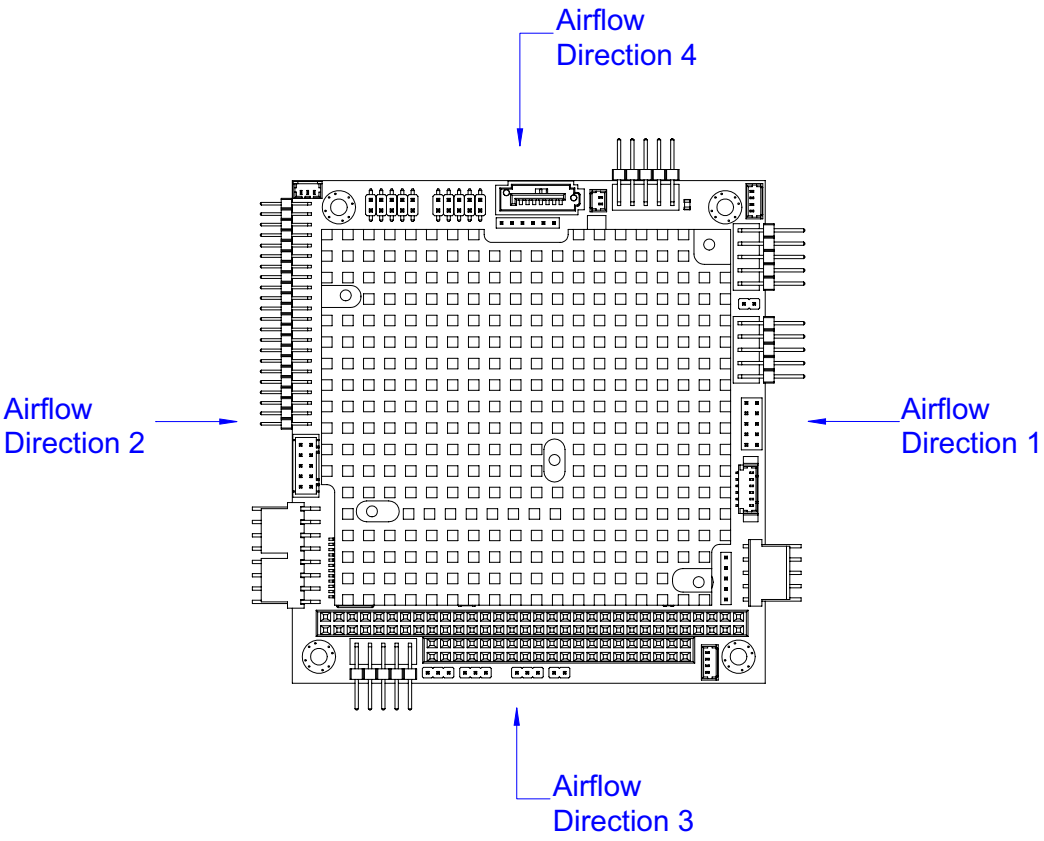


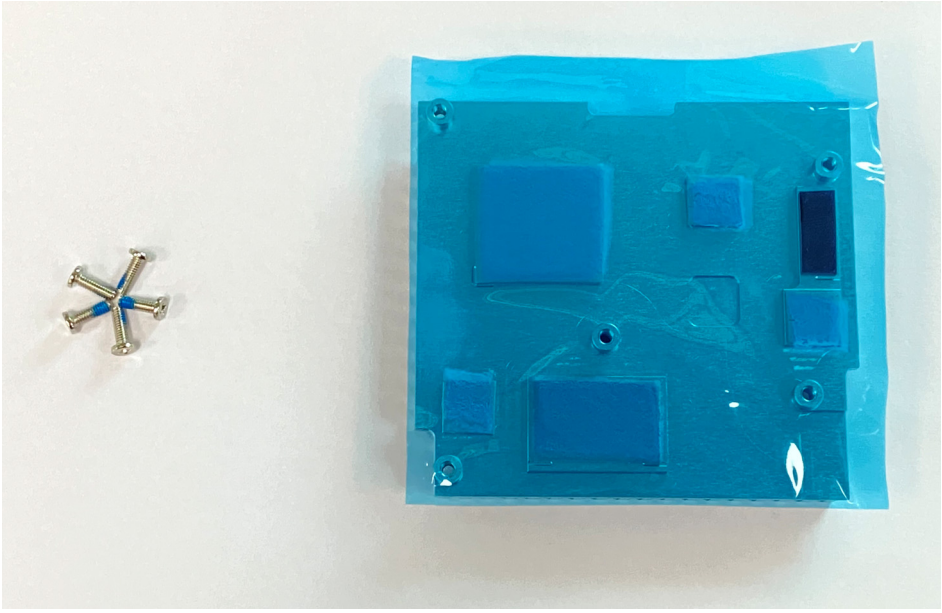
Figure 1-5: Airflow Directions with CM1-86DX3-TM Heatsink

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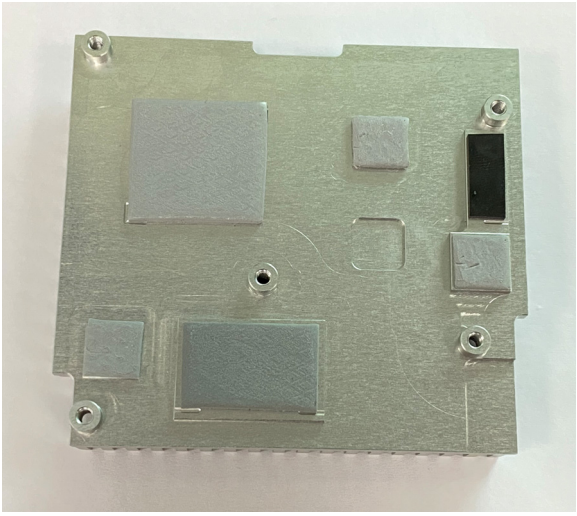
1.7 Heat Sink Installation

Follow the steps below to mount the passive heat sink to the top side of the board. The heat sink features thermal pads to draw heat away from the SoC, SDRAM, BMC controller, and other components.

1. Locate the heat sink kit in the package, including five M2.5 I-head L7.5 mounting screws.

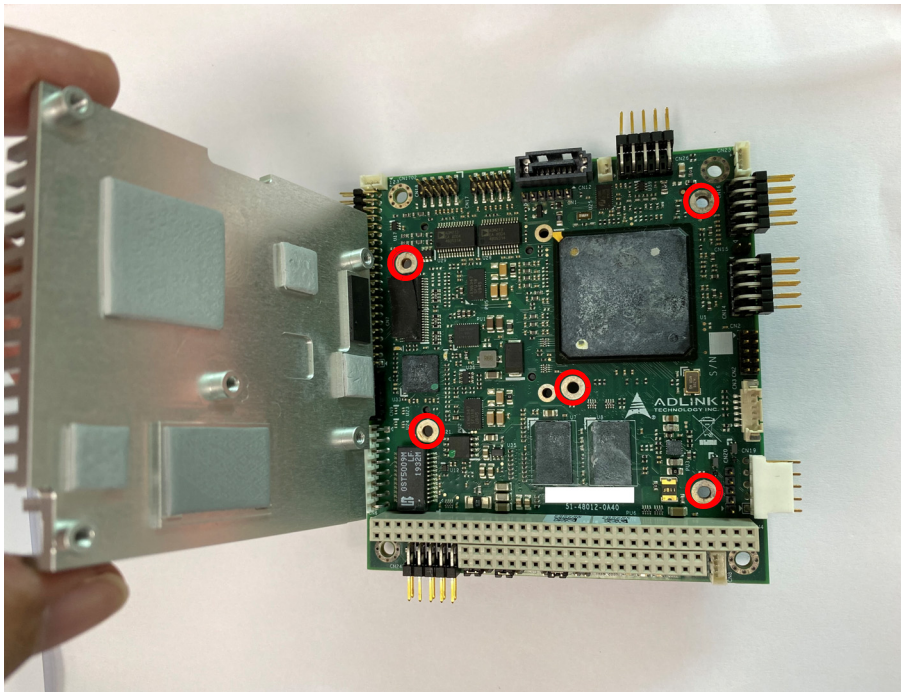


2. Remove the blue film protecting the thermal pads on the heat sink.

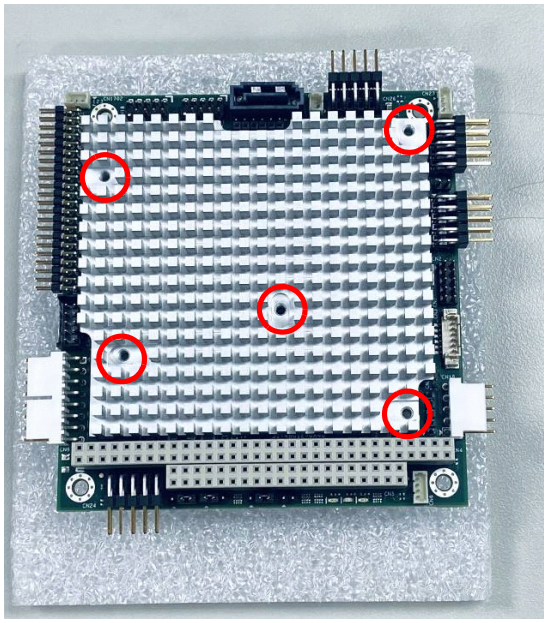


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3. Align the heat sink with the board as shown below. The five mounting holes on the board are circled in red.



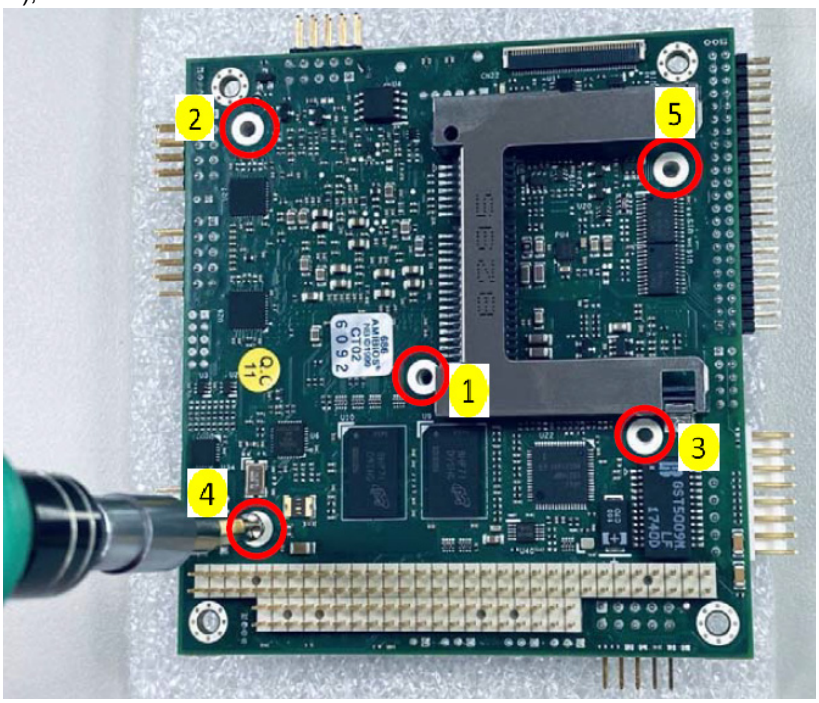
4. Place the heat sink over the board so that the five mounting holes on the heat sink are aligned with mounting holes on the board.



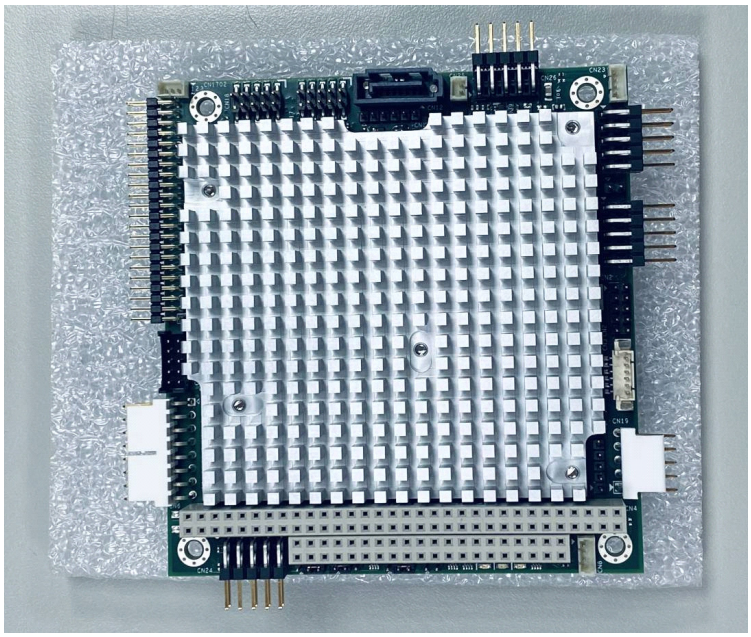
5. Apply light pressure on the heat sink to ensure the thermal pads are in contact with the components on the board

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6. Flip the board and heat sink assembly over. Secure the heat sink to the board with five M2.5 screws by tightening them sequentially, applying a torque of 0.36 N.m (3.67 kgf.cm), as shown below.



7. The heat sink installation is now complete.



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1.8 Getting Started

This section provides the most efficient way to setup and power on your CM1-86DX3 SBC. Select a clean flat, anti-static work surface for setup and operation, large enough to include any external peripherals and optional devices.



Be sure to observe ESD prevention measures. Make sure you are always at the same potential as the module.

Assurez-vous de respecter les mesures de prévention des décharges électrostatiques. Assurez-vous que vous êtes toujours au même potentiel que le module.



Never connect or disconnect peripherals like HDDs while the power supply is connected and switched on.

Ne connectez ou ne déconnectez jamais des périphériques tels que des disques durs lorsque l'alimentation est connectée et sous tension.

Use the cable set provided by ADLINK Technology to connect the CM1-86DX3 to a VGA monitor. Connect a USB keyboard and mouse. Use the SATA cable to connect the SSD. Make sure that the pins match their counterparts correctly and are not twisted. If you plan to use additional peripherals, connect them to the appropriate headers.

Connect a 5 volt power supply to the power connector and switch on the power.



The 5 amps value is the minimum you should have for the standard peripherals mentioned. For additional peripherals, make sure enough power is available. The system will not work if there is not enough supply current for all your devices.

The display shows the BIOS messages. If you want to change the standard BIOS settings, press the <DEL> key to enter the BIOS setup menus. See Chapter 4 for setup details.

If you need to load the BIOS default values, they can be automatically loaded at boot time.

The CM1-86DX3 boots from CD drives, USB sticks, hard disks, or CFast . Provided that any of these is connected and contains a valid operating system image, the display then shows the boot screen of your operating system.

The CM1-86DX3 needs adequate cooling measures depending on the desired operating temperature range. Using the board without cooling could damage the board permanently.

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2 Hardware

This chapter describes the major integrated circuits (ICs) and interface connectors and headers on the module. The third section of this chapter further describes the major ICs including the manufacturers' model numbers.

2.1 Major IC Definitions and Locations

Table 2-1 describes the major ICs on the CM1-86DX3, including a brief description of each IC. Figures 2-1 and 2-2 show the locations of the major ICs.

Table 2-1: Major Component Descriptions and Functions

Chip Type	Mfg.	Model	Description	Function
CPU (U1)	DMP Electronics, Inc.	Vortex86-DX3	Vortex x86 6.5W, 32-bit SoC (System on Chip)	Integrates Processor Core, Graphics and Memory Controller Hub, and I/O Hub
DDR3L SDRAM (U7 and U8 - on top side) [see Figure 2-1]	Micron	MT41K256M16	On-board DDR3L, 1.35V, 4Gb, 32Mx16x8, non-ECC, un-buffered System Memory	Provides high-speed data transfer
DDR3L SDRAM (U9 and U10 - on bottom side) [see Figure 2-2]	Micron	MT41K256M16	On-board DDR3L, 1.35V, 4Gb, 32Mx16x8, non-ECC, un-buffered System Memory	Provides high-speed data transfer
Ethernet EEPROM (U21)	Winbond	W25Q16DVSSIG	Three-Wire Serial EEPROM for Gigabit Ethernet Controller	Provides storage for MAC addresses, serial numbers, and pre-boot configuration data
Ethernet Controller (U22)	Intel	WGI210IT SLIXT	Single-port Gigabit Ethernet controller	Integrates GbE MAC, PHY, and SGMII/SerDes to enable 10T/100TX/1000T Ethernet signals using the PCIe x1 bus
RS-485/422/232 Transceiver (U26 and U27 - on bottom side) [see Figure 2-2])	EXAR	SP339EER1-L	RS-485/422/232 Transceiver for COM1 and COM2	Transmits and receives RS-485/422/232 signals for COM1 and COM2
RS-232 Transceiver (U28 and U29 - on top side) [see Figure 2-1]	Analog Devices	ADM213EARSZH6ZRB	RS-232 Transceiver for COM3 and COM4	Transmits and receives RS-232 signals for COM3 and COM4

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Table 2-1: Major Component Descriptions and Functions (Continued)

Chip Type	Mfg.	Model	Description	Function
BMC (U33) [**Optional**]	Texas Instruments	TM4C123GH6ZRBT7	Microcontroller	Provides logistics and forensic information, flat panel control, I2C bus control, user flash, Watchdog Timer and fan control
Gb Ethernet Transformer (TF2 - on bottom side) [see Figure 2-2]	BOTHHAND	GST5009M	Gigabit Ethernet Magnetics	Provides electrical isolation for Gigabit Ethernet controller
Fast Ethernet Transformer (TF3 - on top side) [see Figure 2-1]	BOTHHAND	GST5009M	Fast Ethernet Magnetics	Provides electrical isolation for Fast Ethernet controller in SoC

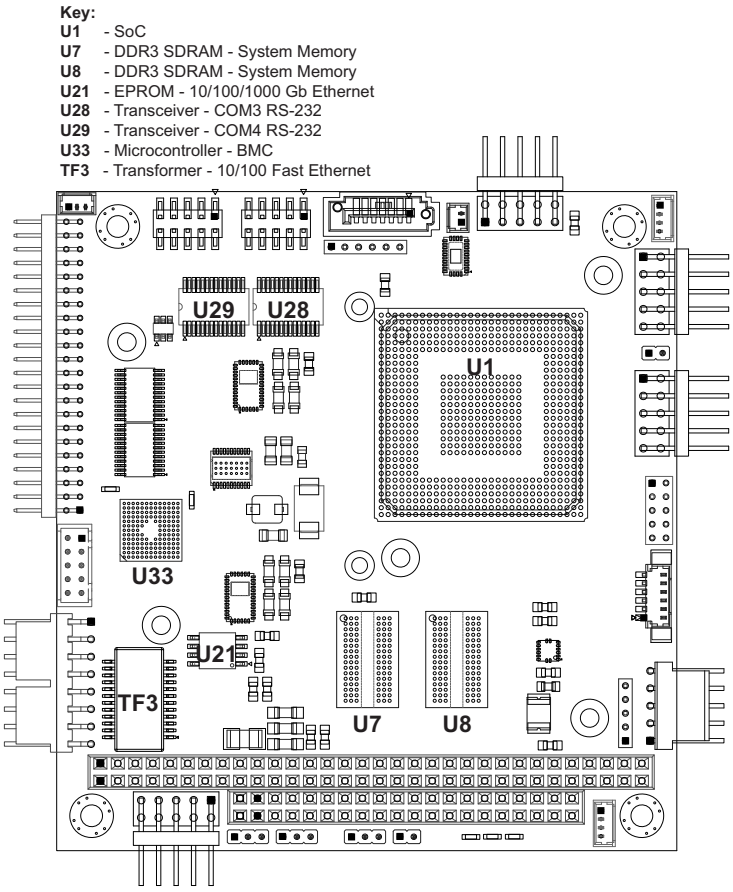


Figure 2-1: Component Locations (Top Side)

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Key:

U9 - DDR3 SDRAM - System Memory
U10 - DDR3 SDRAM - System Memory
U22 - Controller - 10/100/1000 Gb Ethernet
U26 - Transceiver - COM1 RS-485/422/232
U27 - Transceiver - COM2 RS-485/422/232
TF2 - Transformer - 10/100/1000 Gb Ethernet

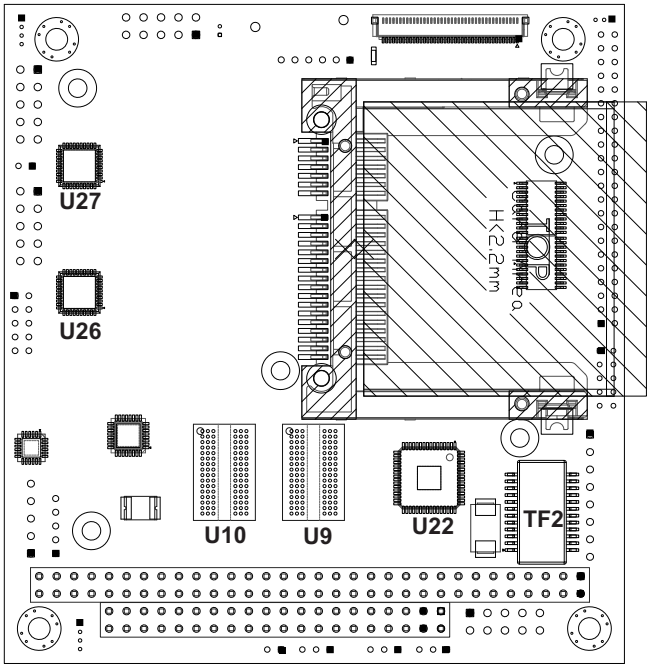


Figure 2-2: Component Locations (Bottom Side)

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2.2 Header, Connector, and Socket Definitions

Table 2-2 describes the headers, connectors, and sockets shown in Figures 2-3 and 2-4.

Table 2-2: Header, Connector, and Socket Descriptions

Jack/Plug #	Access	Description
CN2 – GPIO (User)	Top	10-pin, 0.079" (2mm) header for User defined GPIO signals [TEKA, HM205CB1N-191-00]
CN3 – JTAG	Top	6-pin, 0.049" (1.25mm) crimp-style connector for factory use, only [WIN WIN, JS-1147V-06]
CN4 – PC/104 (A/B)	Top/ Bottom	64-pin, 0.100" (2.54mm) connector for PC/104 (ISA) bus [EPT, 962-60322-12]
CN5 – PC/104 (C/D)	Top/ Bottom	40-pin, 0.100" (2.54mm) connector for PC/104 (ISA) bus [EPT, 962-60202-12]
CN6 – 10/100 Ethernet	Top	8-pin, 0.100" (2.54mm), right-angle header for Fast (10baseT/100baseTX) Ethernet interface [MOLEX, 22-12-2084]
CN7 – Video	Top	44-pin, 0.079" (2mm), right-angle header for TTL/VGA interface [21N22050-44D10B-01G-4]
CN8 – LED - 10/100/1000 Ethernet	Top	4-pin, 0.049" (1.25mm) header for Gigabit Ethernet external LED [REGO, 830-1251-04STD-3.2-6T]
CN9 – 10/100/1000 Ethernet	Top	10-pin, 0.079" (2mm) header for 10/100/1000BaseT Gigabit Ethernet port [HIROSE, DF11-10DP-2DSA]
CN12 – SATA [**Optional**]	Top	7-pin, 0.050" (1.27mm), standard, right-angle connector for Generation 1 Serial ATA signals [MOLEX, 67800-5005]
CN13 – CFast [**Optional**]	Bottom	24-pin, 0.050" (1.27mm), standard, right-angle, push push socket with 8.35mm height for SATA-based CFast cards [REGO, 821101-1100190]
CN14 – Serial 2 (COM2)	Top	10-pin, 0.100" (2.54mm), right-angle header for Serial 2 RS485/ 422/232 signals [TEKA, HR205A1BB-NS-H0]
CN15 – Oops! Jumper	Top	2-pin, 0.079" (2mm) header for overriding current BIOS settings. Refer to Chapter 4. [JIH, 21N12050-02S10B-01G-4]
CN16 – Serial 1 (COM1)	Top	10-pin, 0.100" (2.54mm), right-angle header for Serial 1, RS-485/422/232 signals [TEKA, HR205A1BB-NS-H0]
CN17 – Serial 3 (COM3)	Top	10-pin, 0.079" (2mm), straight header for Serial 3, RS-232 signals [ASTRON, 27-24051-205-2G-TR1-R]
CN18 – Serial 4 (COM4)	Top	10-pin, 0.079" (2mm), straight header for Serial 4, RS-232 signals [ASTRON, 27-24051-205-2G-TR1-R]
CN19 – USB0	Top	5-pin, 0.100" (2.54mm), right-angle header for USB0 interface [AMP, 3-641216-5]
CN20 – USB1	Top	5-pin, 0.079" (2mm), straight header for USB1 interface [SAMTEC, TMM-105-03-LM-S]
CN22 – Debug, DB40	Bottom	40-pin, 0.196" (0.50mm) FPC/FFC, DB40 debug connector [FCI, 10042867-40MB10ELF]
CN23 – Fan	Top	4-pin, 0.049" (1.25mm) wire-to-board friction lock blade header for system fan signals [REGO, 830-1251-04STD-3.2-6T]

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Table 2-2: Header, Connector, and Socket Descriptions (Continued)

Jack/Plug #	Access	Description
CN24 – Power	Top	10-pin, 0.100" (2.54mm), right-angle header for Power connection [TEKA, HR205A1BB-NS-H0]
CN25 – Battery	Top	2-pin, 0.049" (1.25mm) header for external battery [REGO, 830-1251-02STD-3.2-6T]
CN26 – Utility	Top	10-pin, 0.100" (2.54mm), right-angle header for Utility interface [TEKA, HR205A1BB-NS-H0]
CN27 – Power Button	Top	2-pin, 0.079" (2mm) header for external power button [JIH, 21N12050-02S10B-01G-4]
CN1702 – VGA DDC	Top	3-pin, 0.049" (1.25mm) header for VGA Display Data Channel [REGO, 830-1251-02STD-3.2-6T]
LED1 – LAN 10/100 Duplex	Top	Indicates Duplex activity of fast Ethernet interface (Green) [LIGITEK, LG-192G-CT]
LED2 – LAN 10/100 LNK_ACT	Top	Indicates link and traffic of fast Ethernet interface (Yellow) [EVERLIGHT, 19-21UYC/S530-A3/TR8]
LED3 – CFAST_ACT	Bottom	Indicates activity of CFast memory card interface (Yellow) [EVERLIGHT, 19-21UYC/S530-A3/TR8]
LED4 – BMC_STATUS	Top	Indicates system-error blink codes (Blue) [LIGITEK, LG-192DBK-CT/T]
LED5 – WDTOUT	Top	Indicates triggered watchdog timer (Red) [LIGITEK, LG-192HRF-CT]
LED6 – +5V_LED	Top	Indicates power on (Green) [LIGITEK, LG-192G-CT]

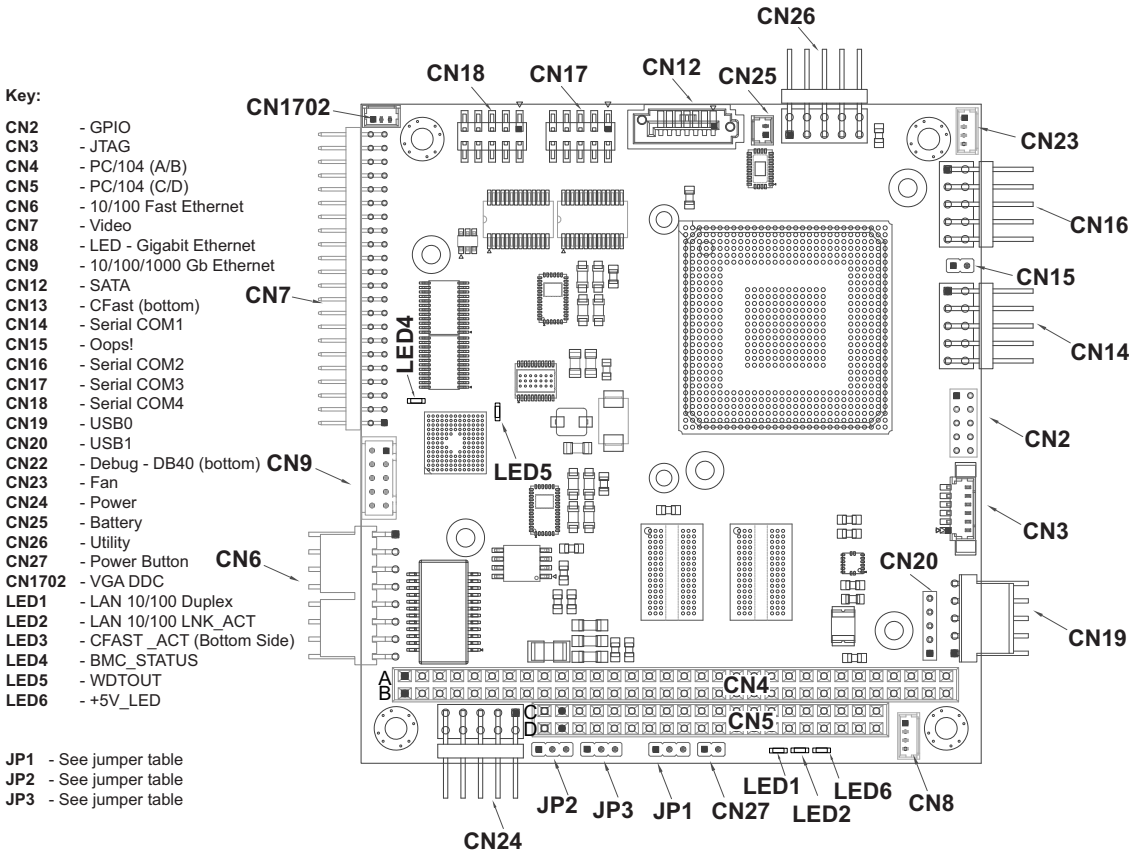


Figure 2-3: Header, Connector, and Socket Locations (Top Side)

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Key:
CN13 - CFast
CN22 - Debug - DB40
CN4 - PC/104 (A/B)
CN5 - PC/104 (C/D)
LED3 - CFAST_ACT

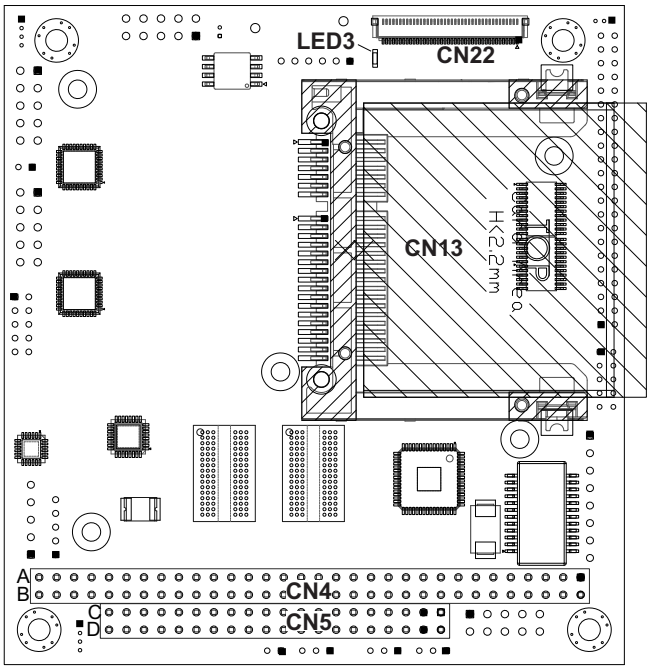


Figure 2-4: Header and Socket Locations (Bottom Side)

NOTE:

Pin 1 is shown as a solid, black square on headers and connectors.

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2.3 Jumper Header Definitions

Table 2-3 describes the jumper headers shown in Figure 2-5. All jumper headers provide 0.079" (2mm) pitch.

Table 2-3: Jumper Settings

Jumper Header	Jumper on Pins 1-2	Jumper on Pins 2-3
JP1 – TFT Interface Voltage Select	+1.8 Volts	+3.3 Volts **(Default)**
JP2 – Backlight Voltage Select	+5 Volts	+12 Volts **(Default)**
JP3 – TFT Supply Voltage Select	+3.3 Volts **(Default)**	+5 Volts

Note: Remove all jumpers to set 18-bit LCD interface.

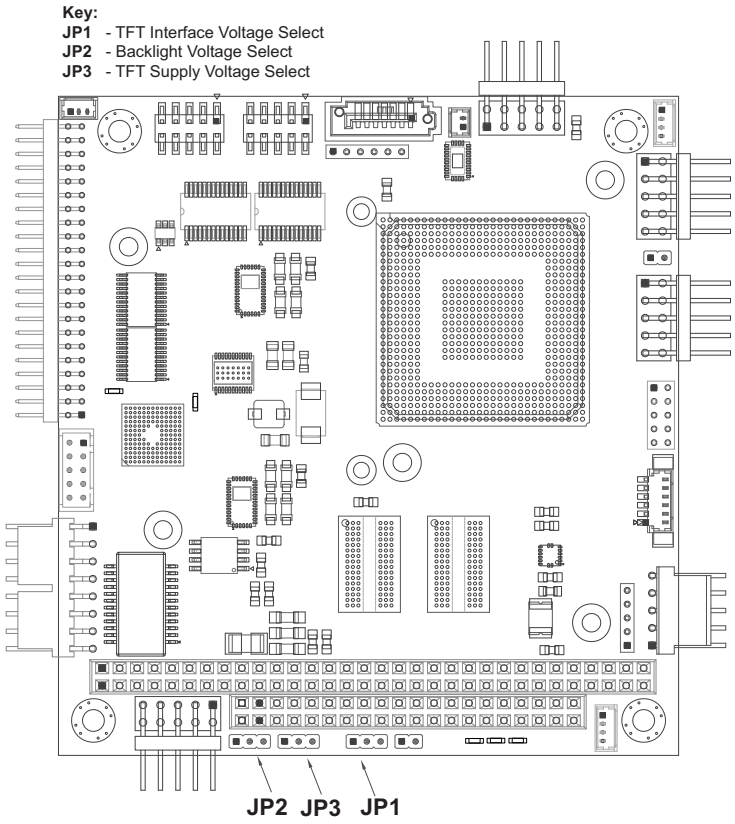


Figure 2-5: Jumper Header Locations (Top Side)

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2.4 Component Features

This section further describes the supported features of the CM1-86DX3 major, on-board hardware components.

2.4.1 CPU

The CM1-86DX3 features the DMP Electronics Vortex, Vortex86-DX3 system-on-chip (SoC). The Vortex86-DX3 is a high-performance and fully static, 32-bit x86 processor with the compatibility of Windows-based, Linux, and most popular 32-bit RTOS. The SoC integrates Processor Core, Northbridge, and Southbridge functions within a single 581-pin BGA package, providing an optimal solution for embedded system and communications products such as thin client, NAST router, home gateway, access point, and tablet applications.

2.4.2 SDRAM

The CM1-86DX3 employs one channel of 64-bit DDR3L on-board memory. Four SDRAM memory chips provide up to 16Gb of low-voltage non-ECC, unbuffered system memory. Refer to the MT41K SDRAM data sheet on the Micron web site.

The following total DRAM capacities are supported:

- 256M x 16 x 2 = 1 GB (optional)
- 256M x 16 x 4 = 2 GB (standard)

2.4.4 LAN Controller

The Intel I210IT provides a single-port controller that supports GbE functionality using the high-speed PCIe standard, v2.1 (2.5GT/s). The I210IT features an integrated PHY, which enables 1000BASE-T implementations such as rack-mounted or pedestal servers in add-on NIC or LAN-on-Motherboard (LOM) designs. Other implementations include blade servers such as LOMs or mezzanine cards as well as embedded applications such as switch add-on cards and network appliances. Refer to the Intel I210IT Ethernet Controller data sheet on the Intel web site.



Due to Vortex86-DX3 SoC performance limitation, Intel I210I Gigabit Ethernet will not be able to reach full bandwidth. Reliable average speed is around 550-600Mbps in full duplex mode.

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2.4.3 CFast Card Slot

The CFast slot (CN13) provides the standard, push-push interface for CFast memory cards. LED3 provides indication of CFast activity. See Chapter 3 for the signal definitions of the CFast interface. Figure 2-6 provides the dimension and mechanical specifications of the CFast card connector.

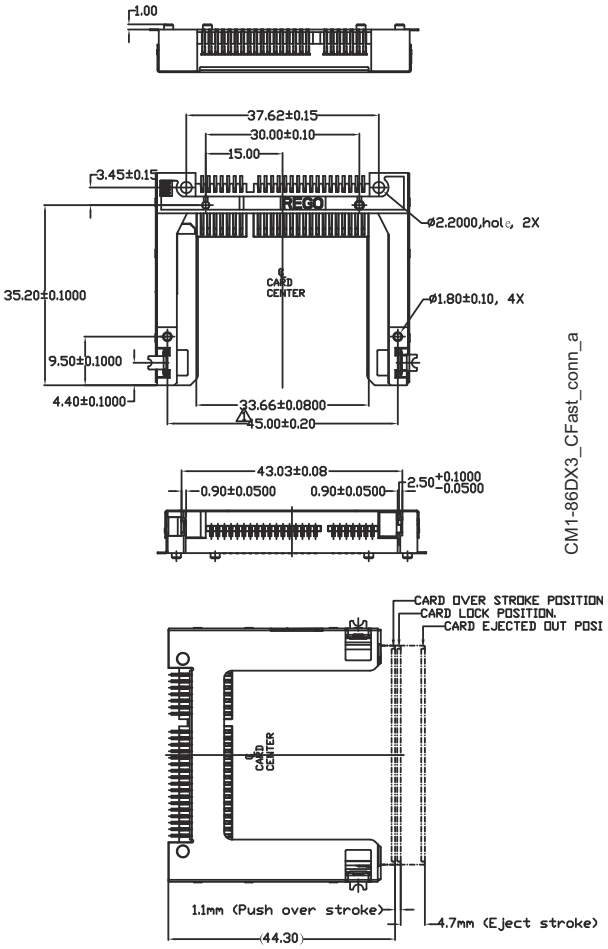


Figure 2-6: CFast Slot

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3 Interfaces

This chapter provides descriptions and signal definitions only of the non-standard interfaces on the board. Descriptions and signal definitions of standard interfaces such as PC/104 and SATA can be found in their respective specification data sheets. If certain signals of standard interfaces have been modified or disconnected, those interfaces will be described in this chapter.

NOTE:

The tables in this chapter define pin sequence using the method in the following example: A 10-pin header with two rows of pins, using odd/even numbering, where pin 2 is directly across from pin 1, is noted as **10 pins, 2 rows, odd/even pin sequence (1, 2)**. Consecutive numbering is noted, for example, as **24 pins, 2 rows, consecutive pin sequence (1, 13)**, where pin 13 is directly across from pin 1. Refer to Figure 2-3 and Figure 2-4 for pin-1 locations.

3.1 Serial Interfaces

Table 3-1 provides the signals for serial interfaces 1 & 2. Table 3-2 provides the signals for the serial interfaces 3 & 4. Both interfaces use 10-pin, right-angle headers with 2 rows, odd/even sequence (1, 2), and 0.100" (2.54mm) pitch.

NOTE:

Serial Ports 1 and 2 provide RS-485/422 functions as well as RS-232 functionality. Only pins 1 and 3 provide RS-485/422/232 signals. Pins 5 and 7 provide only RS-422/232 signals.

To change the mode from RS-232 to RS-485 or RS-422, use the settings in the Advanced>Serial Port menu of the BIOS Setup Utility, described in Chapter 4.

In Table 3-1, pins 1, 3, 5, and 7 include secondary signals assigned for RS-485/422 modes.

Serial Ports 3 and 4, described in Table 3-2, provide only RS-232 functions.

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Table 3-1: Serial Port 1 (CN16) & Port 2 (CN14) Interface Pin Signals

Pin #	Signal	DB9 #	Description
1	DCD* TX-/RX-	1	Data Carrier Detect – Indicates external serial device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input is driven by DTR as part of the DTR/DSR handshake. If in RS-422 mode, this pin is TX- (Data Negative). If in RS-485 mode, this pin is TX-/RX- (Data Negative).
2	DSR*	6	Data Set Ready – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR for overall readiness.
3	RXD TX+/RX+	2	Receive Data – Serial port receive data input is typically held at a logic 1 (mark) when no data is being transmitted, and is held “Off” for a brief interval after an “On” to “Off” transition on the RTS line to allow the transmission to complete. If in RS-422 mode, this pin is TX+ (Data Positive). If in RS-485 mode, this pin is TX+/RX+ (Data Positive).
4	RTS*	7	Request To Send – Indicates serial port is ready to transmit data. Used as hardware handshake with CTS for low level flow control.
5	TXD RX+	3	Transmit Data – Serial port transmit data output is typically held to a logic 1 when no data is being sent. Typically, a logic 0 (On) must be present on RTS, CTS, DSR, and DTR before data can be transmitted on this line. If in RS-422 mode, this pin is RX+ (Data Positive).
6	CTS*	8	Clear To Send – Indicates external serial device is ready to receive data. Used as hardware handshake with RTS for low level flow control.
7	DTR* RX-	4	Data Terminal Ready – Indicates serial port is powered, initialized, and ready. Used as hardware handshake with DSR for overall readiness. If in RS-422 mode, this pin is RX- (Data Negative).
8	RI*	9	Ring Indicator – Indicates external serial device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
9	GND	5	Ground
10	Key/NC	NC	Key Pin/Not connected

Note: The shaded table cells denote power or ground. The * symbol indicates the signal is Active Low.

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Table 3-2: Serial Port 3 (CN17) & Port 4 (CN18) Interface Pin Signals

Pin #	Signal	DB9 #	Description
1	DCD*	1	Data Carrier Detect – Indicates external serial device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input is driven by DTR as part of the DTR/DSR handshake.
2	DSR*	6	Data Set Ready – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR for overall readiness.
3	RXD	2	Receive Data – Serial port receive data input is typically held at a logic 1 (mark) when no data is being transmitted, and is held “Off” for a brief interval after an “On” to “Off” transition on the RTS line to allow the transmission to complete.
4	RTS*	7	Request To Send – Indicates serial port is ready to transmit data. Used as hardware handshake with CTS for low level flow control.
5	TXD	3	Transmit Data – Serial port transmit data output is typically held to a logic 1 when no data is being sent. Typically, a logic 0 (On) must be present on RTS, CTS, DSR, and DTR before data can be transmitted on this line.
6	CTS*	8	Clear To Send – Indicates external serial device is ready to receive data. Used as hardware handshake with RTS for low level flow control.
7	DTR*	4	Data Terminal Ready – Indicates serial port is powered, initialized, and ready. Used as hardware handshake with DSR for overall readiness.
8	RI*	9	Ring Indicator – Indicates external serial device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
9	GND	5	Ground
10	Key/NC	NC	Key Pin – Not connected

Note: The shaded table cells denote power or ground. The * symbol indicates the signal is Active Low.

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3.2 USB Interfaces

The CM1-86DX3 provides one root USB hub and two functional USB ports, supporting USB EHCI v2.0 and over-current detection.

Table 3-3 describes the pin signals of the USB0 interface, which uses a single-row, 5-pin, right-angle header with 0.100" (2.54mm) pitch.

Table 3-3: USB0 Interface Pin Signals (CN19)

Pin #	Signal	Description
1	USB0PWR	USB Power – VCC (+5V +/-5%) power goes to the port through an on-board fuse. Port is disabled if this input is low.
2	USB0N	USB0 Port Data Negative
3	USB0P	USB0 Port Data Positive
4	GND	USB0 Port ground
5	SHIELD	USB0 Port shield

Note: The shaded table cells denote power or ground.

Table 3-4 describes the pin signals of the USB1 interface, which uses a single-row, 5-pin, vertical header with 0.079" (2mm) pitch.

Table 3-4: USB1 Interface Pin Signals (CN20)

Pin #	Signal	Description
1	USB1PWR	USB Power – VCC (+5V +/-5%) power goes to the port through an on-board fuse. Port is disabled if this input is low.
2	USB1N	USB1 Port Data Negative
3	USB1P	USB1 Port Data Positive
4	GND	USB1 Port ground
5	SHIELD	USB1 Port shield

Note: The shaded table cells denote power or ground.

3.3 Utility Interface

The Utility interface provides various utility and I/O signals on the module and consists of a 10-pin, 0.1" (2.54mm) pitch header. The Vortex CPU drives the signals on the Utility interface, and Table 3-5 provides the signal definitions.

- PS/2 Keyboard and PS/2 Mouse
- Battery
- Reset Switch
- Speaker

3.3.1 Keyboard

The signal lines for a PS/2 keyboard are provided from the Vortex CPU to the Utility interface.

3.3.2 Mouse

The signal lines for a PS/2 mouse are provided from the Vortex CPU to the Utility interface.

3.3.3 Battery

An external battery input connection is provided through the Utility interface to support a battery backup for the CMOS RAM and the RTC (Real Time Clock).

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3.3.4 Reset Switch

An external reset switch provides the reset signal through the Utility interface to a reset circuit, which drives the Vortex CPU.

3.3.5 Speaker

The speaker signal provides sufficient signal strength to drive a 1W 8 Ω “Beep” speaker through the Utility interface at an audible level. The speaker signal is driven from an on-board amplifier and the Vortex CPU.

Table 3-5 describes the pin signals of the Utility interface, which uses a 10-pin, right-angle header with 2 rows, odd/even sequence (1, 2), and 0.100" (2.54mm) pitch.

Table 3-5: Utility Interface Pin Signals (CN26)

Pin #	Signal	Description
1	SPKR	Speaker Output
2	GND	Ground
3	RST_BTN_IN*	External Reset Switch signal
4	MSDATA	Mouse Data input
5	KBDATA	Keyboard Data input
6	KBCLK	Keyboard Clock input
7	GND	Ground
8	+VCC UTIL	Keyboard /Mouse power (+5V) output
9	VBATV_EX	Real time battery voltage (3.6V Type/ 4.0V Max) input
10	MSCLK	Mouse Clock input

Note: The shaded table cells denote power or ground. The * symbol indicates the signal is Active Low.

3.4 Fast Ethernet Interface

Table 3-6 describes the pin signals of the Fast Ethernet interface, which uses a single-row, 8-pin header with 0.100" (2.54mm) pitch.

Table 3-6: Fast Ethernet Interface Pin Signals (CN6)

Pin #	Signal	Description
1	LAN100_TX_P	Analog Twisted Pair Ethernet Transmit Differential Pair – These pins transmit the serial bit stream through the isolation transformer.
2	LAN100_TX_N	
3	LAN100_RX_P	Analog Twisted Pair Ethernet Receive Differential Pair – These pins receive the serial bit stream through the isolation transformer.
6	LAN100_RX_N	
4	ETH_PE	Connected through two 75 ohm resistors in series to center tap of isolation transformer and then to ground through common 1k PF capacitor.
5	ETH_PE	
7	ETH_PE	Connected through two 75 ohm resistors in series to center tap of isolation transformer and then to ground through common 1k PF capacitor.
8	ETH_PE	

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3.5 Gigabit Ethernet Interface

Table 3-7 describes the pin signals of the Gigabit Ethernet header which consists of 10 right-angle pins, two rows, odd/even (1,2) pin sequence, and 0.079" (2mm) pitch.

Table 3-7: Gigabit Ethernet Interface Pin Signals (CN9)

Pin #	Signal	Description
1	ETH-PE	Connected through two 75 ohm resistors in series to center tap of isolation transformer and then to ground through common 1k PF capacitor.
2	ETH-PE	
3	ETH1_TRD0_P	Media Dependent Interface 0 +/-
4	ETH1_TRD0_N	
5	ETH1_TRD1_P	Media Dependent Interface 1 +/-
6	ETH1_TRD1_N	
7	ETH1_TRD2_P	Media Dependent Interface 2 +/-
8	ETH1_TRD2_N	
9	ETH1_TRD3_P	Media Dependent Interface 3 +/-
10	ETH1_TRD3_N	

Note: The shaded table cells denote ground.

3.6 Gigabit Ethernet External LED Interface

Table 3-8 defines the signals of the external LED that indicates Gigabit Ethernet links and activity using a single row of 4 pins with 0.049" (1.25mm) pitch.

Table 3-8: Gigabit Ethernet External LED Pin Signals (CN8)

Pin #	Signal	Description
1	+V3P3	+3.3 volts Power
2	ETH1_LINK_ACT*	Indicates link connectivity or transfer data activity
3	ETH1_LED_100*	Indicates link activity at 100 Mbps
4	ETH1_LED_1000*	Indicates link activity at 1000 Mbps

Note: The shaded table cell denotes power. The * symbol indicates the signal is Active Low.

3.7 Video (TFT/VGA) Interface

Table 3-9 describes the pin signals of the Video interface, which uses a 44-pin, right-angle header with 2 rows, odd/even sequence (1, 2), and 0.079" (2mm) pitch.

Table 3-9: Video Interface Pin Signals (CN7)

Pin #	Signal	Description
1	FP1_CLK	TFT Shift Clock – This clock signal provides the timing for transferring digital pixel data.
2	FP1_DE	TFT Data Enable – This signal indicates valid data on any of the FP [23:0] lines.
3	FP1_HSYNC	TFT Line Pulse – This signal is the digital monitor equivalent of HSYNC.
4	FP1_VSYNC	TFT Frame Marker – This signal is the TFT monitor equivalent of VSYNC.
5	GND1	Ground 1
6	GND2	Ground 2
7	NC	Not connected (FP0 = Flat Panel Data 0)
8	NC	Not connected (FP1 = Flat Panel Data 1)
9	FP2	Flat Panel Data 2 – data output, Blue0 (18-bit)

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Table 3-9: Video Interface Pin Signals (CN7) (Continued)

Pin #	Signal	Description
10	FP3	Flat Panel Data 3 – data output, Blue1 (18-bit)
11	FP4	Flat Panel Data 4 – data output, Blue2 (18-bit)
12	FP5	Flat Panel Data 5 – data output, Blue3 (18-bit)
13	FP6	Flat Panel Data 6 – data output, Blue4 (18-bit)
14	FP7	Flat Panel Data 7 – data output, Blue5 (18-bit)
15	NC	Not connected (FP8 = Flat Panel Data 8)
16	NC	Not connected (FP9 = Flat Panel Data 9)
17	FP10	Flat Panel Data 10 – data output, Green0 (18-bit)
18	FP11	Flat Panel Data 11 – data output, Green1 (18-bit)
19	FP12	Flat Panel Data 12 – data output, Green2 (18-bit)
20	FP13	Flat Panel Data 13 – data output, Green3 (18-bit)
21	FP14	Flat Panel Data 14 – data output, Green4 (18-bit)
22	FP15	Flat Panel Data 15 – data output, Green5 (18-bit)
23	NC	Not connected (FP16 = Flat Panel Data 16)
24	NC	Not connected (FP17 = Flat Panel Data 17)
25	FP18	Flat Panel Data 18 – data output, Red0 (18-bit)
26	FP19	Flat Panel Data 19 – data output, Red1 (18-bit)
27	FP20	Flat Panel Data 20 – data output, Red2 (18-bit)
28	FP21	Flat Panel Data 21 – data output, Red3 (18-bit)
29	FP22	Flat Panel Data 22 – data output, Red4 (18-bit)
30	FP23	Flat Panel Data 23 – data output, Red5 (18-bit)
31	VDD_EN_CN	TFT Power Enable
32	BKLT_EN_R	TFT Backlight Enable
33	+VCC_TFT_CN	Panel Voltage (+3.3 or +5 volts ±5%) depending on setting of JP3
34	+VCC_BKL_CN	Backlight Voltage (+5 or +12 volts ±5%) depending on setting of JP2
35	GND3	Ground 3
36	GND4	Ground 4
37	CON_HSYNC	Horizontal Sync – This signal is used for the digital horizontal sync output to the CRT. Also used (with VSYNC) to signal power management state information to the CRT per the VESA™ DPMS™ standard.
38	CON_VSYNC	Vertical Sync – This signal is used for the digital vertical sync output to the CRT. Also used (with HSYNC) to signal power management state information to the CRT per the VESA™ DPMS™ standard.
39	AGNDR	Analog Ground for Red
40	VGA_RED	Red – This pin provides the Red analog output to the CRT.
41	AGNDG	Analog Ground for Green
42	VGA_GREEN	Green – This pin provides the Green analog output to the CRT.
43	AGNDB	Analog Ground for Blue
44	VGA_BLUE	Blue – This pin provides the Blue analog output to the CRT.

Note: The shaded table cells denote power or ground.

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3.8 VGA DDC (Display Data Channel)

The VGA DDC interface provides digital communication of display modes between the display and a graphics adapter for plug-and-play performance, enabling the computer host to adjust monitor parameters such as brightness and contrast.

Table 3-10 describes the signals for the VGA DDC interface, which provides a single row, 3-pin header with 0.049" (1.25mm) pitch.

Table 3-10: VGA DDC Signals (CN1702)

Pin #	Signal	Description
1	VGA_DDC_CLK	Display Data Channel clock
2	NC	Not Connected
5	VGA_DDC_DAT	Display Data Channel data

3.9 Power Interface

The CM1-86DX3 requires one +5 volt DC power source. If the +5VDC power drops below ~4.65V, a low voltage reset is triggered, resetting the system.

The power input header (CN24) supplies the following voltages and ground directly to the module:

- 5.0VDC +/- 5% @ 1.35 Amps

Table 3-11 describes the pin signals of the Power interface, which uses a 10-pin, right-angle header with 2 rows, odd/even sequence (1, 2), and 0.100" (2.54mm) pitch.

Table 3-11: Power Interface Pin Signal (CN24)

Pin	Signal	Descriptions
1	+5V	+5 Volts
2	GND	Ground
3	+5V	+5 Volts
4	GND	Ground
5	NC	Not Connected
6	GND	Ground
7	+12V	+12 volts routed to PC/104
8	GND	Ground
9	+5V	+5 Volts
10	GND	Ground

Note: The shaded table cells denote power or ground.

3.10 Battery Interface

Table 3-12 lists the pin signals of the External Battery Input header for backup RTC (Real Time Clock), which uses 2 pins with 0.049" (1.25mm) pitch.

Table 3-12: External Battery Input Header (CN25)

Pin #	Signal	Description
1	VBAT_EXT	+3.0 volts DC
2	GND	Ground

Note: The shaded table cells denote power or ground. The RTC has an expected current draw of ~5µA at room temperature (25°C). A 3-volt model (CR1225) battery is recommended. The battery is used only when power is not applied to the board.

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3.11 Power Button Interface

Table 3-13 lists the pin signals of the External Power Button header, which uses 2 pins with 0.079" (2mm) pitch.

Table 3-13: External Power Button Header (CN27)

Pin #	Signal	Description
1	PWRBTN#	+3.3 volts for power button
2	GND	Ground

Note: The shaded table cells denote power or ground.

3.12 CFast Mass Storage Socket

The optional CFast socket supports Generation 1 SATA signals with transfer speeds of 1.5 GB/s and is compatible with versions 1.1 and 2.0 CFast cards. This 24-pin female socket provides 7 data pins and 17 power pins for CFast Type II mass storage cards.

Table 3-14 lists the pin signals of the CFast Card socket, which uses 24 right-angle pins with 0.050" (1.27mm) pitch.

Table 3-14: CFast Mass Storage Socket (CN13)

Pin #	Signal	Description
S1	SGND	Ground
S2	CFAST_C_TX_P	SATA HOST Signal Pair
S3	CFAST_C_TX_N	SATA HOST Signal Pair
S4	SGND	Ground
S5	CFAST_C_RX_N	SATA HOST Signal Pair
S6	CFAST_C_RX_P	SATA HOST Signal Pair
S7	SGND	Ground
Key		
PC1	NC	Not Connected
PC2	GND	Ground
PC3	NC	Not Connected
PC4	NC	Not Connected
PC5	NC	Not Connected
PC6	NC	Not Connected
PC7	GND	Ground
PC8	CFAST_ACT#	Card Activity LED
PC9	NC	Not Connected
PC10	NC	Not Connected
PC11	NC	Not Connected
PC12	NC	Not Connected
PC13	PWR1	+3.3V
PC14	PWR2	+3.3V
PC15	PGND	Power / Ground
PC16	PGND	Power / Ground
PC17	NC	Not Connected

Note: The shaded table cells denote power or ground.

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4 Utilities

4.1 BIOS Setup

The CM1-86DX3 features an AMI BIOS. The default settings provide a “ready to run” system, even without a BIOS setup backup battery.

The BIOS is located in flash memory and can be easily updated with software under DOS.

All setup changes of the BIOS are stored in the CMOS RAM.

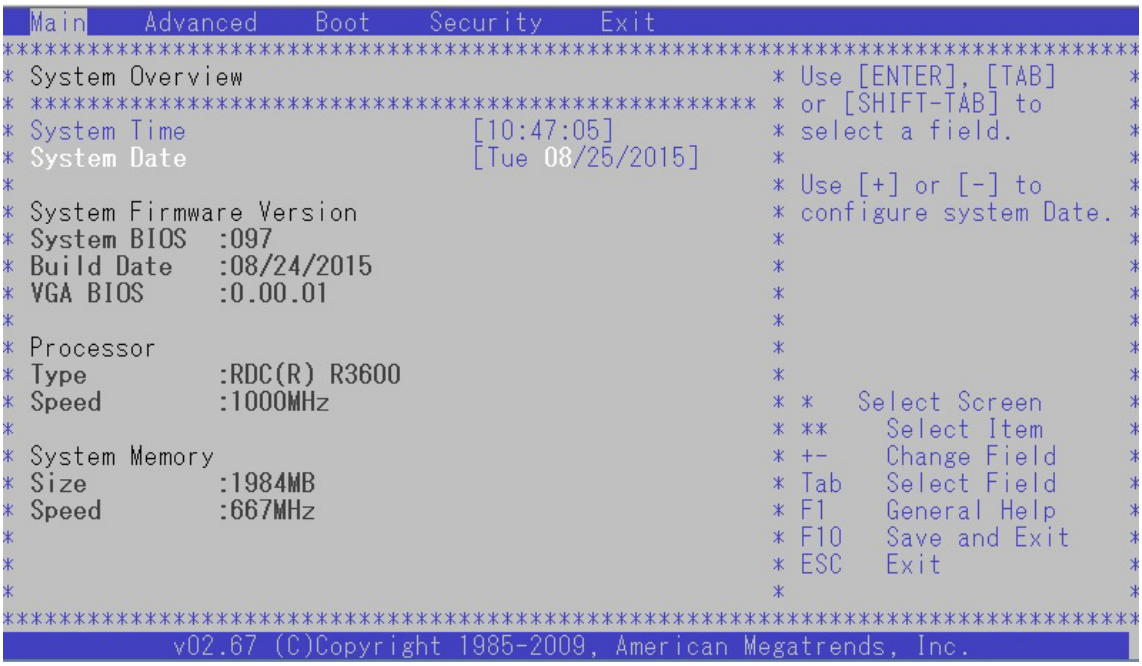
The soldered battery will provide power to store that information for over two years without board activation.

4.1.1 Configuring the BIOS

- Pressing <DEL> during power up starts the BIOS setup utility.
- Pressing <F11> during power up starts the boot menu.

4.1.2 Main screen of the BIOS

The main screen of the BIOS SETUP UTILITY gives you a quick overview of the BIOS version, the clock speed, installed memory, memory speed, date and time. The date and time can be configured by the user.



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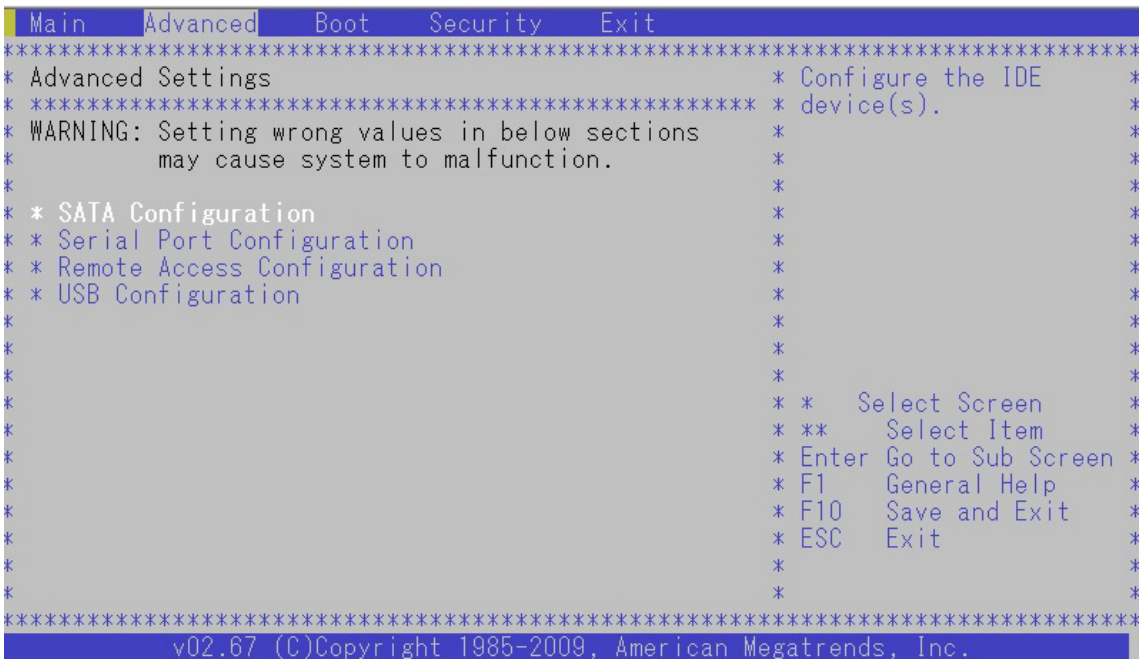
4.1.3 Advanced Settings screen

The main screen of “Advanced Settings” provides configuration settings for the IDE interface, serial port, remote access, and USB port. Refer to the following illustrations for visual reference. A description of the selected setting appears in the right column of the active screen.

CAUTION:
MISE EN GARDE

The use of inappropriate values on any of the following advanced settings below may cause the system to malfunction.

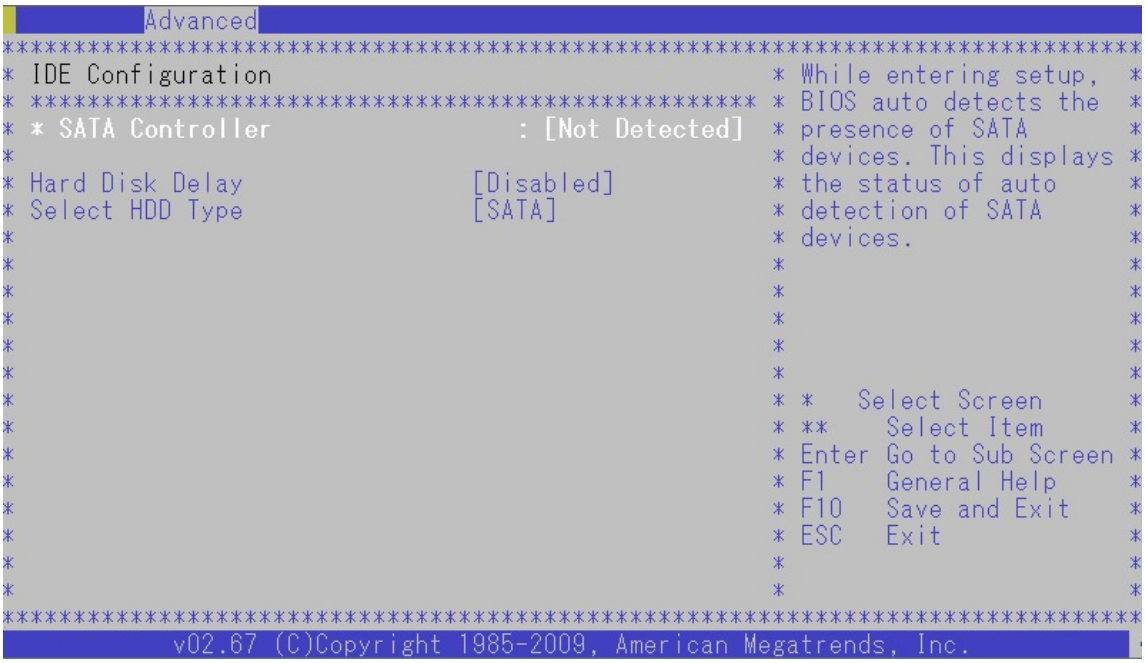
L'utilisation de valeurs inappropriées sur l'un des paramètres avancés suivants ci-dessous peut entraîner un dysfonctionnement du système.



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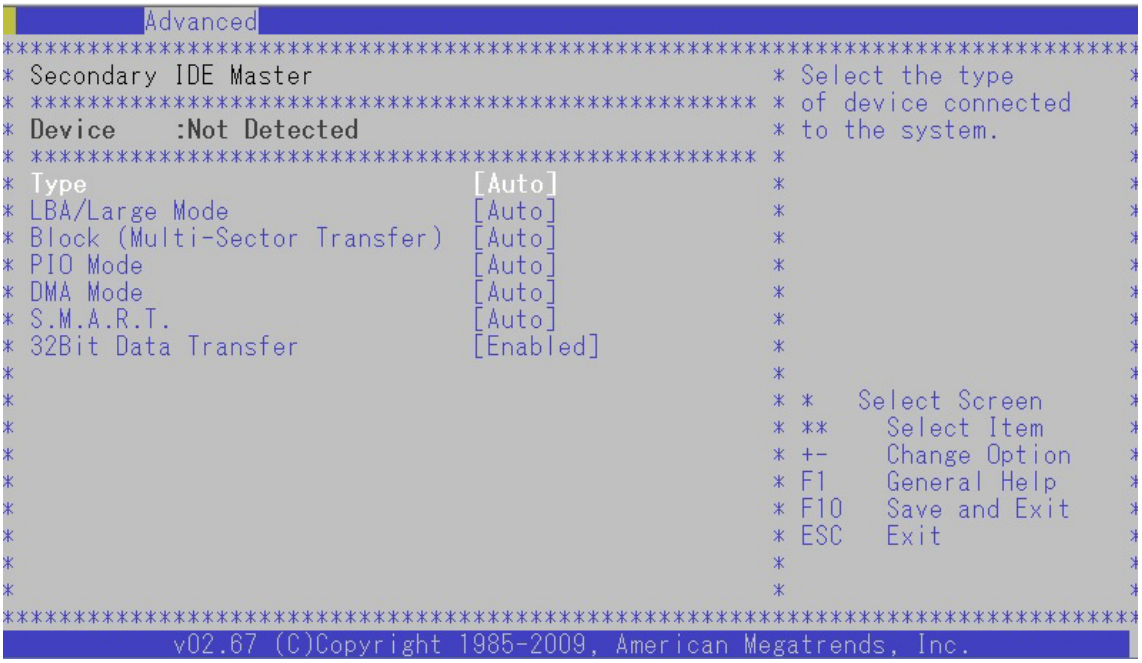
Advanced > IDE Configuration

These settings allow you to configure the features of the integrated IDE controllers.



Advanced > IDE Master

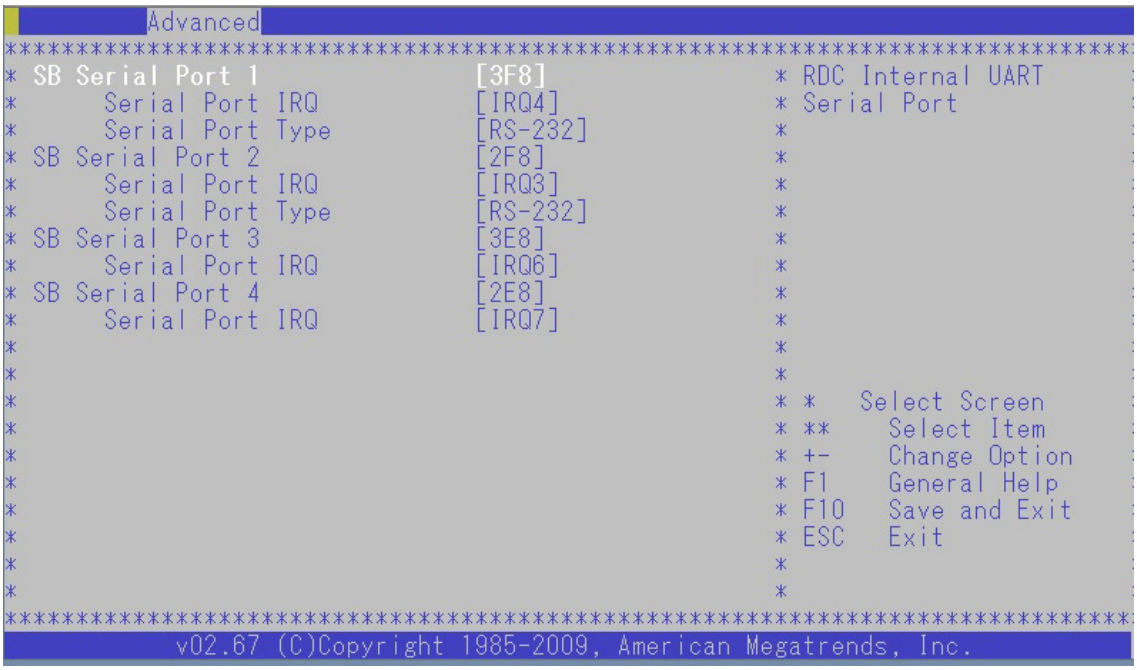
This setting provides options for IDE slave and master drives.



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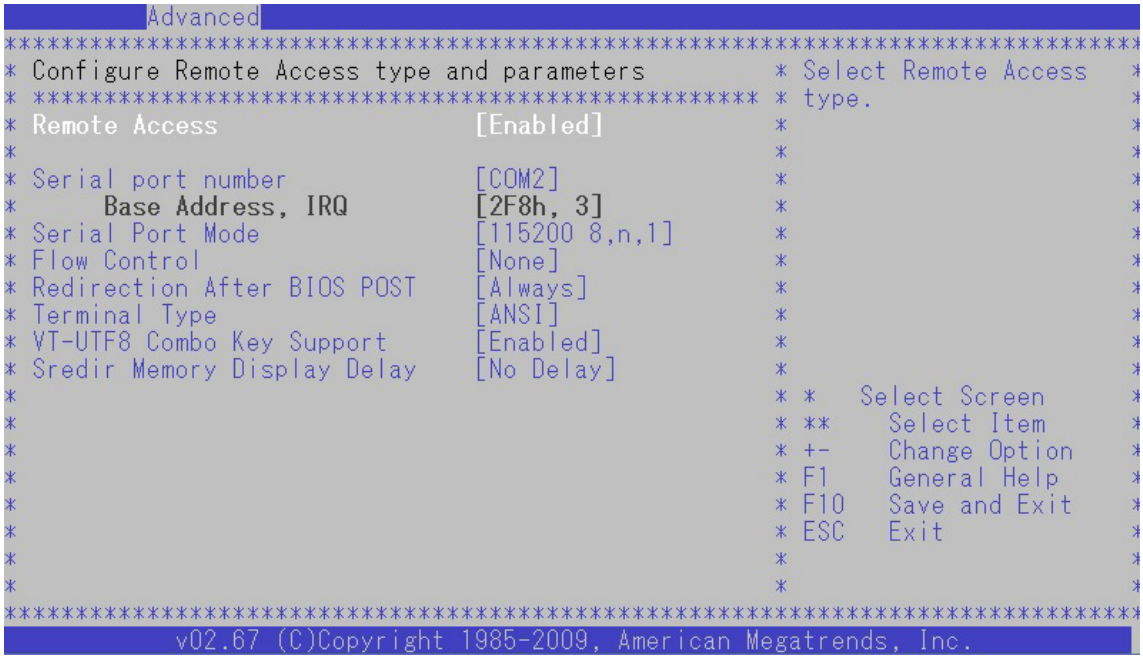
Advanced > Serial Port

These settings allow you to specify the base I/O port address, Interrupt Request address, and Port Type mode (if applicable) of specific serial ports.



Advanced > Remote Access

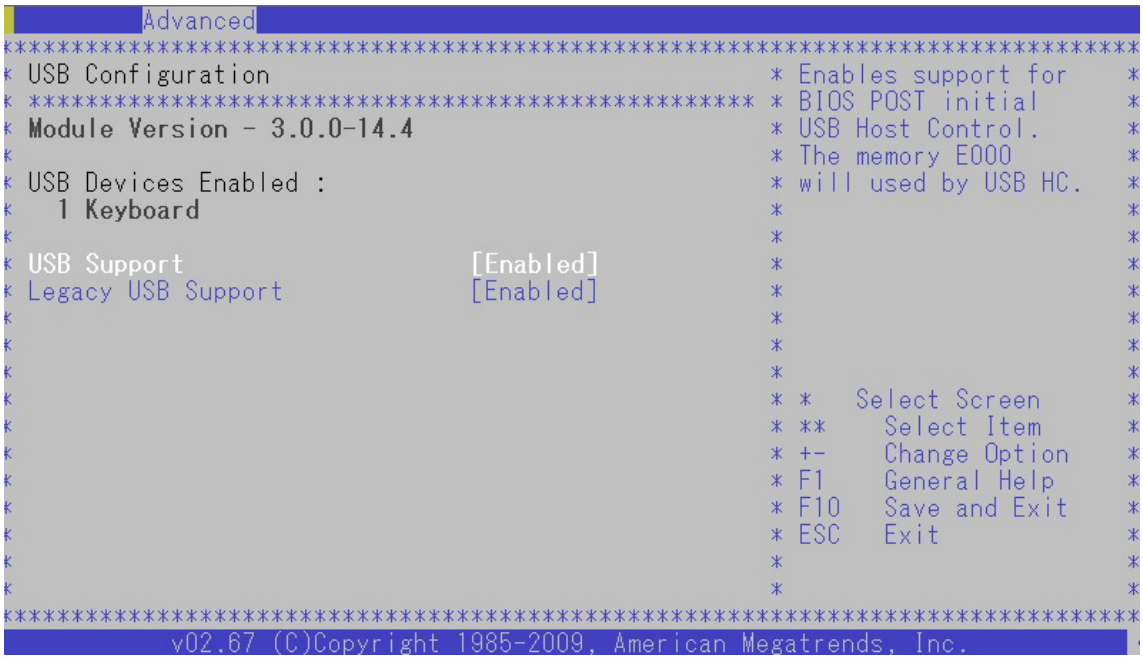
Remote Access allows you to enter the BIOS Setup through a serial terminal or PC.



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Advanced > USB Port

The USB Support settings allow you to select options for enabling or disabling on-board USB ports. The Legacy USB support settings allow a USB mouse and keyboard to control the system even if no USB drivers are loaded on the system.

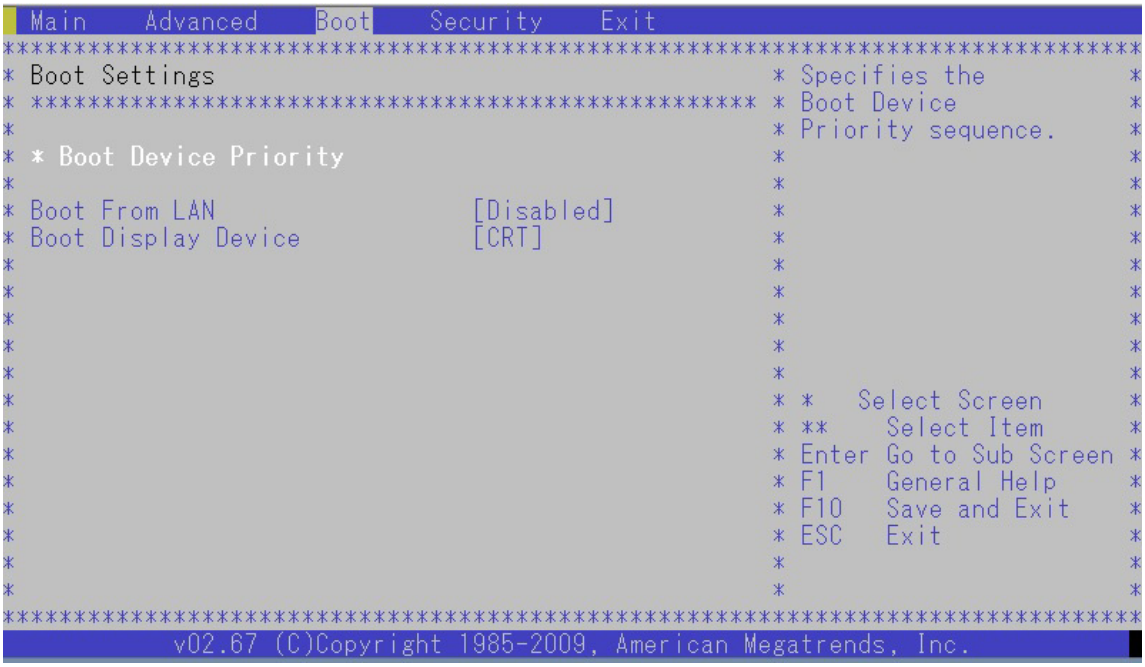


4.1.4 Boot screen

If more than one drive is attached to the CM1-86DX3, you can select from the first “Boot Settings” screen the boot order in which the drives are scanned for a bootable OS image.

Boot Settings

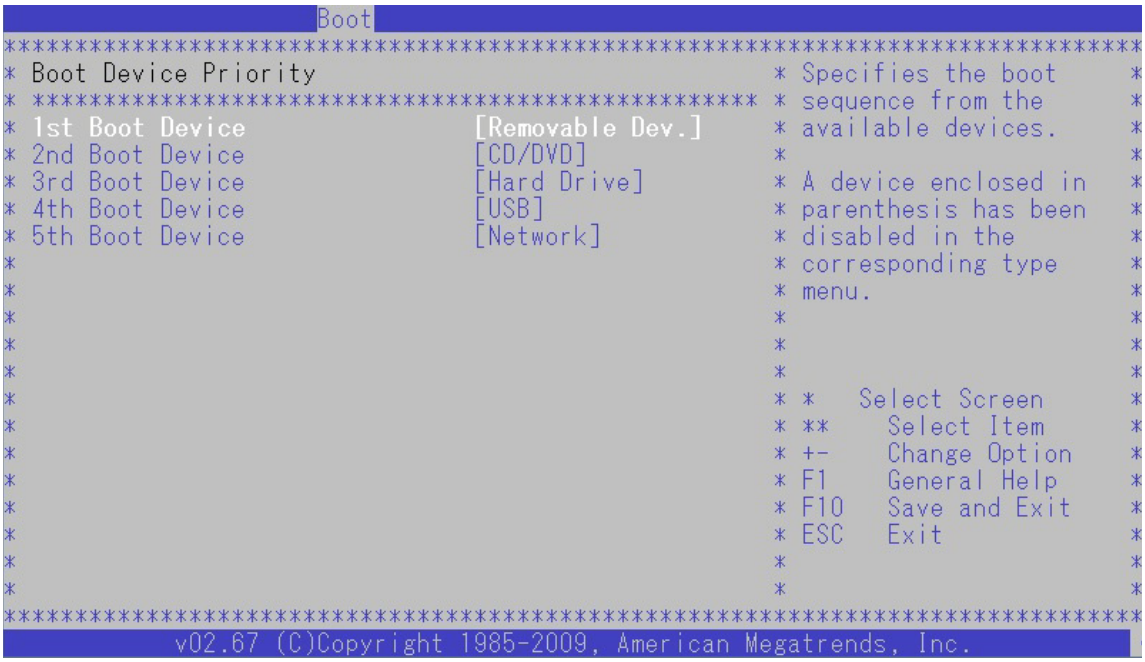
The Boot From LAN setting allows you to enable LAN PXE boot. The Boot Display Device setting allows you to choose CRT or LCD as the display source.



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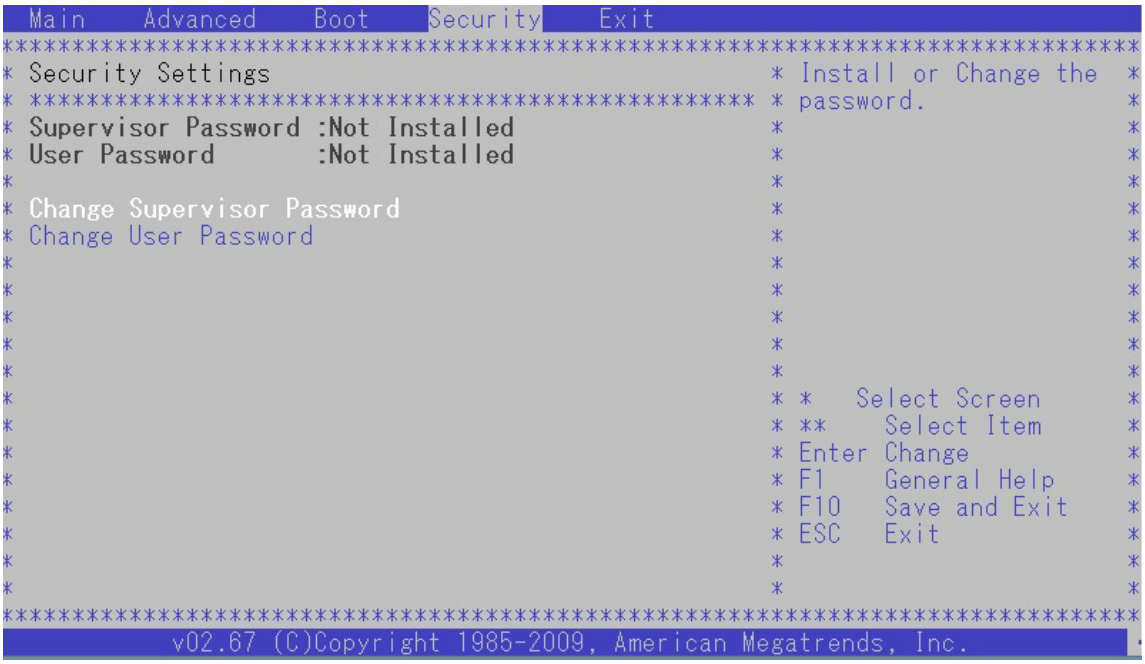
Boot > Boot Device Priority

These settings allow you to specify the order in which the system checks for the device from which to boot.



4.1.5 Security screen

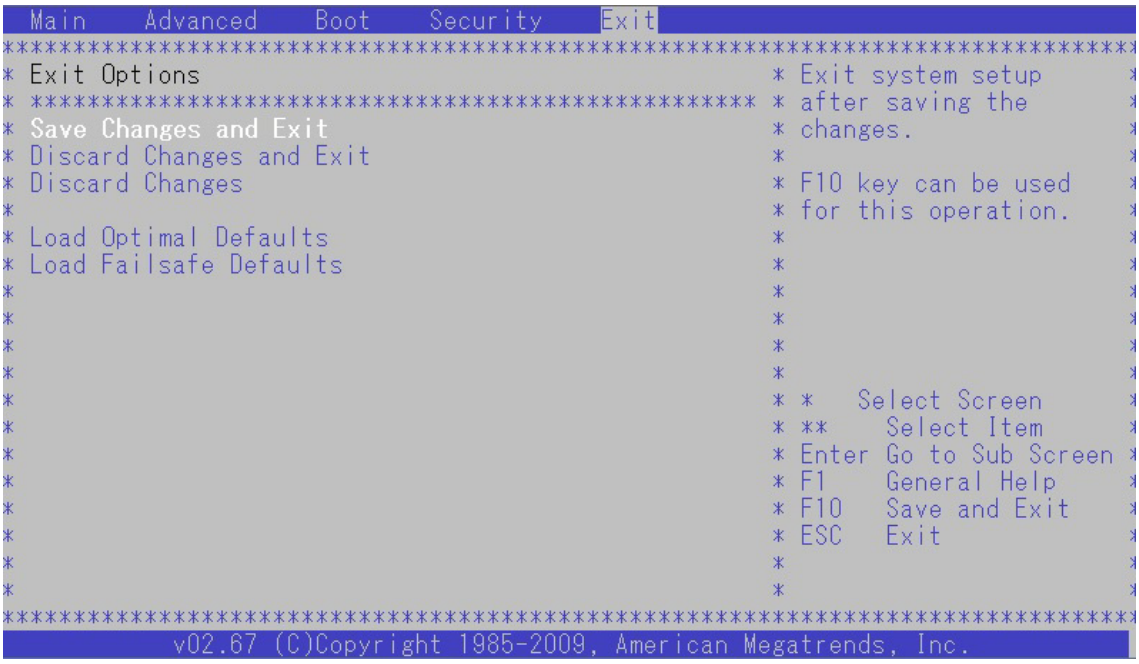
This screen allows you to set a Supervisor or a User password. If you want to use both passwords, the Supervisor password must be set first.



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4.1.6 Exit screen

The settings in the Exit screen allow you to exit the BIOS Setup utility while saving or discarding certain defaults or changes.



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4.2 SEMA Functions

Under the management of the BMC chip (Board Management Controller), the SEMA utility (Smart Embedded Management Agent) provides system control and failure protection—counting, monitoring, and measuring hardware and software events, from which the SoC can trigger corrective commands. The optional SEMA Cloud utility not only controls local events on the module but system client events on the Internet of Things (IoT.) Refer to the following bullets for a list of SEMA functions.

- Total operating hours counter
  Counts the time the module has been run in minutes.
- On-time minutes counter
  Counts the seconds since last system start.
- Monitoring of Board temperature
  Minimum and maximum temperature values of the board are stored in flash.
- Power monitor
  Reads the current drawn by the board and reports the nominal operating voltage.
- Power cycles counter
- Boot counter
  Boot counter is increased after a HW- or SW-Reset or after a successful power-up.
- Watchdog Timer
  Set / Reset / Disable Watchdog Timer.
- System Restart Cause
  Power loss / Watchdog / External Reset.
- Flash area
  1kB Flash area for customer data
- Protected Flash area
  128 Bytes for Keys, ID's, etc. can be stored in a write- and clear-protectable region.
- Board Identify
  Vendor / Board / Serial number

The SEMA Tools are available for Windows and Linux. SEMA functionality can also be used in applications. Refer to the SEMA software manual and technical manual on the ADLINK web site for more information.



If a failure occurs while updating the BMC firmware through the SEMA command line, restart the system and repeat the update to resolve the failure.

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4.2.1 Board Specific SEMA functions

Voltages

The BMC of the CM1-86DX3 implements a Voltage Monitor and samples several Onboard Voltages. The Voltages can be read by calling the SEMA function, “Get Voltages”. The function returns a 16-bit value divided in Hi-Byte (MSB) and Lo-Byte (LSB).

Table 4-1: SEMA Monitored Voltages

ADC Channel	Voltage Name	Voltage Formula [V]
0	VCC_CORE	(MSB<<8 + LSB) x 3.3 / 1024
1	V1P2	(MSB<<8 + LSB) x 3.3 / 1024
2	VTT	(MSB<<8 + LSB) x 3.3 / 1024
3	VDDQ	(MSB<<8 + LSB) x 3.3 / 1024
4	V1P8	(MSB<<8 + LSB) x 3.3 / 1024
5	V3P3	(MSB<<8 + LSB) x 1.1 x 3.3 / 1024
6	VCC	(MSB<<8 + LSB) x 1.83 x 3.3 / 1024
7	V12	(MSB<<8 + LSB) x 6.0 x 3.3 / 1024
8	MAINCURRENT	Use Main Current Function

Main Current

The BMC of the CM1-86DX3 implements a Current Monitor. The current can be read by calling the SEMA function “Get Main Current”. The function returns four 16-bit values divided in Hi-Byte (MSB) and Lo-Byte (LSB). These four values represent the last four currents drawn by the board. The values are sampled every 250ms. The order of the four values is NOT in relationship to time. The access to the BMC may increase the drawn current of the whole system. In this case, you still have three samples without the influence of the read access.

Main Current = (MSB_n<<8 + LSB_n) * 8.06mA

TS#-Events

TS# is activated by a temperature sensor when a device reaches its critical temperature and released when the device is back in its normal temperature range. This counter gives the user information about temperature or cooling issues. This counter is cleared when the system is removed from power. The CM1-86DX3 only monitors the board temperature and does not support TS#-Events.

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Exception Blink Codes

In the case of an error, the BMC shows a blink code on the STATUS-LED. This error code is also reported by the BMC Flags register. The Exception Code is not stored in the Flash storage and is cleared when the power is removed. Therefore, the “Clear Exception Code”-Command is not supported.

Table 4-2: Blink Codes

Exception Blink Code	Error Message
0	NOERROR
2	NO_VCORE_POK_3P3
3	NO_V1P2_POK_3P3
4	NO_VDDQ_POK_3P3
5	NO_V1P8_POK_3P3
6	NO_V3P3_POK_3P3
7	CRITICAL_TEMP
8	POWER_FAIL
9	VOLTAGE_FAIL
10	NO_BUF_PLT_RST_L

BMC Flags

The BMC Flags register returns the last detected exception code since power up.

4.3 Real Time Clock (RTC)

The CM1-86DX3 contains a Real Time (time of day) Clock (RTC), which can be backed up with an external Lithium Battery. The CM1-86DX3 will function without a battery in those environments which prohibit batteries. The CM1-86DX3 will also continue to operate after the battery life has been exceeded. Under these conditions all setup information is restored from the onboard flash memory during POST along with the default date and time information.



Some operating systems require a valid default date and time to function.

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4.4 User GPIO Interface

Table 4-3 describes the pin signals of the GPIO interface, which uses a 10-pin header with 2 rows, odd/even sequence (1, 2), and 0.079" (2mm) pitch.

Table 4-3: User GPIO Interface Pin Signals (CN2)

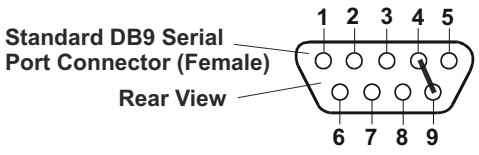
Pin #	Signal	Description
1	GPIO0	User defined
2	GPIO1	User defined
3	GPIO2	User defined
4	GPIO3	User defined
5	GPIO4	User defined
6	GPIO5	User defined
7	GPIO6	User defined
8	GPIO7	User defined
9	GND	Ground
10	GND	Ground

Note: The shaded table cells denote ground.

4.5 Oops! Jumper (BIOS Recovery)

The Oops! jumper is provided in the event you have selected BIOS settings that prevent you from booting the system. By using the Oops! Jumper you can stop the current BIOS settings in the CMOS from being loaded, allowing you to proceed, using the default settings. Install a jumper on the CN15, 2-pin header or connect the DTR pin to the RI pin on Serial port 1 (COM 1) prior to boot up to prevent the present BIOS settings from loading. After booting with the Oops! Jumper in place, remove the Oops! Jumper and go into the BIOS Setup Utility. Change the desired BIOS settings, or select the default settings, and save changes before rebooting the system.

To convert a standard DB9 connector to an Oops! Jumper, short together the DTR (4) and RI (9) pins on the rear of the connector as shown in the following figure on the Serial Port 1 DB9 connector.



CM1-86DX3_Oopsjump_

4.6 Serial Console

The CM1-86DX3 BIOS supports the serial console (or console redirection) feature. These I/O functions are provided by an ANSI-compatible serial terminal, or the equivalent terminal emulation software running on another system. This can be very useful when setting up the BIOS on a production line for systems that are not connected to a keyboard and display.

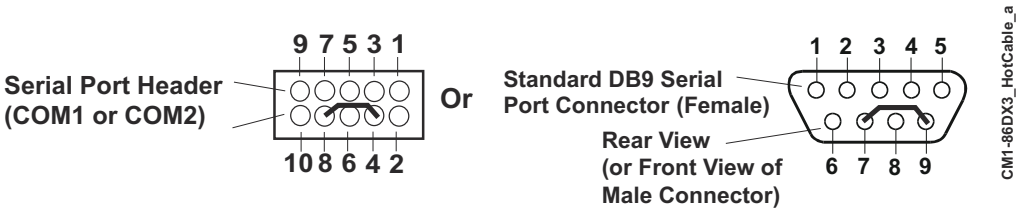
4.7 Serial Console BIOS Setup

The serial console (console redirection) feature is implemented by connecting a standard null-modem cable or a modified serial cable (or “Hot Cable”) from either serial port COM1 or COM2 (CN14 or CN16) to the serial terminal or a PC with communications software. The BIOS Setup Utility controls the serial console settings on the CM1-86DX3. Refer to the BIOS Setup for the serial console option settings using a serial terminal or PC with communications software.

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4.8 Hot (Serial) Cable

To convert a standard serial cable to a Hot Cable, certain pins must be shorted together at the Serial port header or at the DB9 connector. Short together the RTS (4) and RI (8) pins on either the COM1 or COM2 (CN14 or CN16) header. As an alternate, you can short the equivalent pins (pins 7 and 9) on the back of the respective DB9 connector as shown in the following figure.



4.9 Watchdog Timer

The Watchdog Timer (WDT) restarts the system if an error or mishap occurs, allowing the system to recover from the mishap, even though the error condition may still exist. Possible problems include failure to boot properly, loss of control by the application software, failure of an interface device, unexpected conditions on the bus, or other hardware or software malfunctions.

The WDT is used through the SEMA during normal system operation. The following SEMA features provide support for the WDT.

- ADLINK SEMA provides an API for the WDT. The API tickles (resets) the WDT before the timer expires, otherwise the system will be reset.
- Watchdog Code examples – ADLINK has provided source code examples in the CM1-86DX3 SEMA, illustrating how to control the WDT. The code examples can be easily copied to your environment to compile and test, or to make any desired changes before compiling. Refer to the SEMA Programming Guide by downloading the SEMA Utility from the CM1-86DX3 web page.

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Appendix A System Resources

This appendix provides system resource specifications for the CM1-86DX3 including Memory addresses, IO addresses, PCI configuration registers, IO registers, and system interrupts.

A.1 Memory Address Map

The SoC supports 4 GBytes of addressable memory space and 64 KBytes of addressable I/O space. In order to be compatible with a PC/AT system, the lower 1 MBytes of this addressable memory is divided into regions which can be individually controlled with programmable attributes such as disable, read/write, write only, or read only.

Figure 2 represents the SoC memory address map. It shows the main memory regions defined and supported by the SoC. At the highest level, the address space is divided into two main conceptual regions. One is the 0-1-Mbyte DOS Compatibility region, and the other is the 1-Mbyte to 4-GByte Extended Memory region.

DOS Compatibility Region

The first region of memory is called the DOS Compatibility Region and it was defined for early PCs.This area is divided into the following address regions:

- 0-640 KByte DOS Area
- 640-768 KByte Video Buffer Area
- 768-896 KByte in 16 KByte section (total of 8 section)-Expansion Area
- 896-960 KByte in 16 KByte section (total of 4 section)-Expansion System BIOS Area
- 960 KByte-1Mbyte Memory (BIOS Area)-System BIOS Area

DOS Area (00000-9FFFFFh)

The DOS area (0000H-9FFFFh) is 640 KBytes in Size. It is mapped to the main memory controlled by the SoC.

Video Buffer Area (A0000-BFFFFh)

The 128 KByte graphics adapter memory region is normally mapped to a video device on the PCI bus (Typically VGA controller). This area is controlled by the A/B Page control Register. It can be mapped to either the main DRAM or the PCI bus for both read and write commands.

ISA Expansion Area (C0000–DFFFFh)

This 128-KByte ISA Expansion region is divided into eight 16-KByte segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through the PCI bridge to ISA space. Memory that is disabled is not remapped.

Extended System BIOS (E0000–EFFFFh)

This 64-KByte area is divided into four 16-KByte segments. Each segment can be assigned independent read and write attributes so it can be mapped either to the main DRAM or to the PCI bus. Typically, this area is used for RAM or ROM. Memory that is disabled is not remapped.

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System BIOS Area (F0000–FFFFFh)

This area is a single 64-KByte segment that can be assigned read and write attributes. It is by default (after reset) read/write disabled and cycles are forwarded to the PCI bus. By manipulating the read/write attributes, the SoC can “shadow” BIOS into main memory. Memory that is disabled is not remapped.

Extended Memory Region

This memory region covers 10_0000h (1 Mbyte) to FFFF_FFFFh (4 GBytes minus 1) address range and is divided into the following regions:

- DRAM memory from 1 Mbyte to the top of memory
- PCI Memory space from the top of memory to 4 GBytes
- High BIOS area from 4 GBytes to 4 GBytes minus 16 MBytes

Main DRAM Address Range (0010_0000h to Top of Main Memory)

The address range from 1 Mbyte to the top of main memory is mapped to the main memory address range controlled by the SoC. All accesses to addresses within this range are forwarded to the main memory.

PCI Memory Address Range (Top of Main Memory to 4 GBytes)

The address range from the top of main DRAM to 4 GBytes is normally mapped to PCI. The PMC forwards all accesses within this address range to PCI.

High BIOS Area (FF00_0000–FFFF_FFFFh)

The top 16 MBytes of the Extended Memory Region is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The CPU begins execution from the High BIOS after reset. This region is mapped to the PCI so that the upper subset of this region is aliased to 16 MBytes minus 256 KBytes range. The actual address space required for the BIOS is less than 2 MBytes. However, the minimum CPU MTRR range for this region is 2 MBytes. Thus, the full 2 MBytes must be considered.

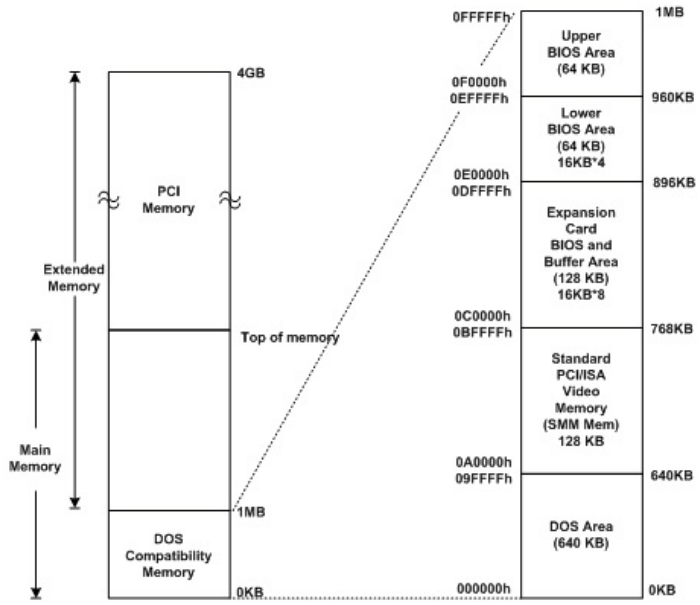


Figure B-2: Memory Address Map

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A.2 I/O Address Map

The SoC positively decodes accesses to all internal registers, including PCI configuration registers (CF8h and CFCh), PC/AT Compatible IO registers (8237, 8254 & 8259), and all re-locatable IO space registers (UART).

Table A-1: Fixed IO Ranges in the CPU

Device	IO Address	Comment
DMA 8237-1	0000h – 000Fh	
PIC 8259-1	0020h – 0021h	
Indirect Access Registers (6117D configuration port)	0022h – 0023h	
Timer Counter 8254	0040h –0043h	
Keyboard / Mouse data port	0060h	
Port B + NMI control port	0061h	
8051 download 4k address counter	0062h – 0063h	
Keyboard/ Mouse status/ command port	0064h	
WatchDog0 reload counter	0065h	
CMOS RAM port	0070h – 0071h	
MTBF control register	0072h – 0075h	
DMA page register	0080h – 008Fh	
System control register	0092h	
PIC 8259-2	00A0h – 00A1h	
WatchDog1 control counter	00A8h – 00ADh	
WatchDog1 reload counter	00AEh	
DMA 8237-2	00C0h – 00DFh	
DOS 4G Page access	00E0h – 00EFh	
IDE 1(IRQ 15)	0170h – 0177h	
COM4 (IRQ 11)	02E8h – 02EFh	
COM2 (IRQ 3)	02F8h – 02EFh	
COM3 (IRQ 10)	03E8h – 03EFh	
IDE1 ATAPI device control write only register	03F6h	
COM1 (IRQ 4)	03F8h – 03FFh	
DMA High page register	0480h – 048Fh	
Instruction counter register	0490h – 0499h	
Instruction counter register	0490h – 0499h	
8259 Edge / level control register	04D0h – 04D1h	
PCI configuration port	0CF8h – 0CFFh	
PCA9535 GPIO Controller	40h	On I2C Bus



The following table shows the variable IO decode ranges. They are set using base address registers (BARs) or other similar means. Plug-and-play (PnP) software (PCI/ACPI) can use their configuration mechanisms to set and adjust these values.

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Table A-2: Variable IO Address Ranges Decoded by PCI Devices in the IO Fabric

Device	Size / Bytes	Comment
ACPI Power Management (PCU)	128	ACPI BASE ADDRESS: PCI[B:0,D:7,F:0] + F8h
I2C	16	I2C BASE ADDRESS: PCI[B:0,D:7,F:0] + D4h



MISE EN GARDE

Variable IO ranges should not be set to conflict with other IO ranges. There will be unpredictable results if the configuration software allows conflicts to occur. Hardware does not check for conflicts.

Les plages d'E/S variables ne doivent pas être définies pour entrer en conflit avec d'autres plages d'E/S. Il y aura des résultats imprévisibles si le logiciel de configuration permet à des conflits de se produire. Le matériel ne recherche pas les conflits.

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A.3 PCI Configuration Registers

Devices and functions can be accessed by the PCI Configuration Registers.

Table A-3: PCI Configuration Registers

Address Range (hex)	Description
0CFB – 0CF8	PCI Configuration Address Register
0CFF – 0CFC	PCI Configuration Data Register

Table A-4: PCI CONFIG_ADDRESS Register Mapping (IO Port CF8h)

Field	CONFIG_ADDRESS Bits
Enable PCI Configuration Space Mapping	31
Reserved	30:24
Bus Number	23:16
Device Number	15:11
Function Number	10:08
Register / Offset Number	07:02



Bit 31 of CONFIG_ADDRESS must be set for a configuration cycle to be generated.

Table A-5: PCI Devices and Functions

Bus#	Device#	Function#	Device ID	Description	Function
0	0	0	6023h	Host bridge	
0	1	0	1031h	PCI-to-PCI bridge(PCI Express)	
0	2	0	1031h	PCI-to-PCI bridge(PCI Express)	
0	7	0	6035	ISA bridge	
0	7	1	6035h	ISA bridge	
0	8	0	6040h	Ethernet controller	
0	A	0	6060h	USB OHCI	
0	A	1	6061h	USB2 EHCI	
0	C	0	1012h	IDE controller	
0	D	0	2015	VGA controller	
1	0	0	1533h	Intel Ethernet controller	

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A.4 IO Register Maps

A.4.1 CMOS Memory and RTC Registers

The RTC internal registers and RAM are organized as two banks of 128 bytes each, called the standard and extended banks. The first 14 bytes of the standard bank contain the RTC time and date information along with four registers A-D, that are used for configuration of the RTC. The extended bank contains a full 128 bytes of battery backed SRAM. All data movement between the host CPU and the RTC is done through register mapped standard I/O space.



It is not possible to disable the extended bank.



Registers reg_RTC_IR_type and reg_RTC_TR_type are used for data movement to and from the standard bank.

Table A-6: RTC IO Registers Alias Locations

Register	Original IO location
reg_RTC_IR_type	70h
reg_RTC_TR_type	71h

Table A-7: RTC Indexed Registers

Start	End	Name
00h	00h	Seconds
01h	01h	Seconds Alarm
02h	02h	Minutes
03h	03h	Minutes Alarm
04h	04h	Hours
05h	05h	Hours Alarm
06h	06h	Day of Week
07h	07h	Day of Month
08h	08h	Month
09h	09h	Year
0Ah	0Ah	Register A
0Bh	0Bh	Register B
0Ch	0Ch	Register C
0Dh	0Dh	Register D
0Eh	7Fh	114 Bytes of User RAM
09h	09h	Year
0Ah	0Ah	Register A
0Bh	0Bh	Register B
0Ch	0Ch	Register C
0Dh	0Dh	Register D
0Eh	7Fh	114 Bytes of User RAM

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A.5 Interrupts

A.5.1 SERIRQ Interrupt Mapping

Below the SERIRQ Interrupt Mapping is shown:

Table A-8: SERRIRQ Interrupt Mapping

Data Frame#	Interrupt	Comment
1	IRQ0	System Timer
2	IRQ1	Keyboard Controller
3	IRQ2	Cascade for IRQ8~15
4	IRQ3	Serial port 2
5	IRQ4	Serial port 1
6	IRQ5	Ethernet 10/100M LAN
7	IRQ6	USB
8	IRQ7	USB / Multimedia Device
9	IRQ8	Real Timer Clock
10	IRQ9	ACPI
11	IRQ10	PCIe0 / Serial Port 3
12	IRQ11	PCIe1 / Serial Port 4
13	IRQ12	Mouse
14	IRQ13	Math Coprocessor
15	IRQ14	Hard Disk Controller #1
16	IRQ15	Hard Disk Controller #2

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Appendix B Technical Support

Ask an Expert: http://askanexpert.adlinktech.com

ADLINK Technology, Inc.
No. 66, Huaya 1st Rd., Guishan District
Taoyuan City 333411, Taiwan
Tel: +886-3-216-5088
Fax: +886-3-328-5706
Email: service@adlinktech.com

Ampro ADLINK Technology, Inc.
6450 Via Del Oro, San Jose, CA 95119-1208, USA
Tel: +1-408-360-0200
Toll Free: +1-800-966-5200 (USA only)
Fax: +1-408-600-1189
Email: info@adlinktech.com

ADLINK Technology (China) Co., Ltd.
300 Fang Chun Rd., Zhangjiang Hi-Tech Park
Pudong New Area, Shanghai, 201203 China
Tel: +86-21-5132-8988
Fax: +86-21-5132-3588
Email: market@adlinktech.com

ADLINK Technology GmbH
Hans-Thoma-Strasse 8-10
D-68163 Mannheim, Germany
Tel: +49-621-43214-0
Fax: +49-621 43214-30
Email: emea@adlinktech.com

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