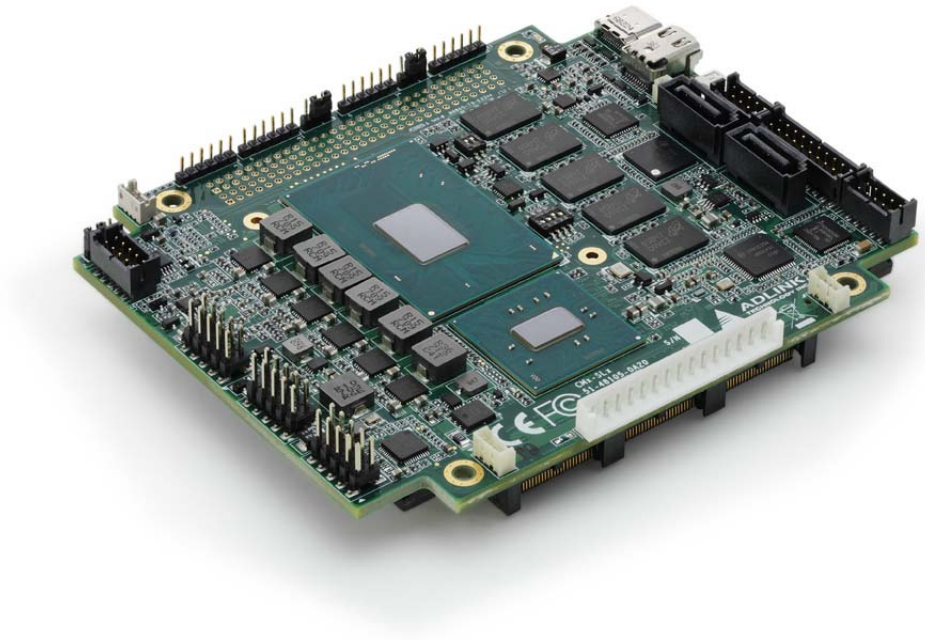
CMx-SLx

Technical Reference

PCI/104-Express Single Board Computer
with 6th Generation Intel® Core™ Processor



Manual Rev.:	1.4
Revision Date:	January 25, 2022
Part Number:	50M-00063-1040

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Preface

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Revision History

Revision	Date	Description of Change(s)
1.00	2017-07-17	Initial Release
1.1	2018-04-20	Added heat spreader installation section to Chapter 1; re-ordered pin sequence in Table 3-4 on page 31; re-labelled signals in Table 3-3 on page 31 to USB0 and USB1; added BMC thermal pad to the heat spreader photos in Chapter 1; added notes concerning +5V-only power to Power Interface (J24) on page 37
1.2	2020-04-08	Correct specifications, Ethernet connector pin definitions (H11)
1.3	2021-02-03	Add French safety warnings
1.4	2022-01-25	Update CPU, memory, SSD specs

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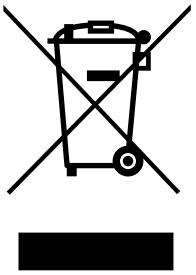
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Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

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Conventions

The following conventions may be used throughout this manual, denoting special levels of information.



This information adds clarity or specifics to text and illustrations.



MISE EN GARDE

This information indicates the possibility of ***minor*** physical injury, component damage, data loss, and/or program corruption.

*Ces informations indiquent la possibilité de blessures physiques **mineures**, de dommages aux composants, de perte de données et / ou de corruption de programme.*



ATTENTION

This information warns of possible ***serious*** physical injury, component damage, data loss, and/or program corruption.

*Ces informations mettent en garde contre d'éventuelles blessures physiques **graves**, des dommages aux composants, une perte de données et / ou une corruption du programme.*

Important Safety Instructions

For user safety, please read and follow all **Instructions**, **WARNINGs**, **CAUTIONs,** and **NOTEs** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

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Table of Contents

Preface ii

1 Product Overview 1
- 1.1 Description 1
- 1.2 About this Manual 1
- 1.3 Features 2
- 1.4 Ordering Information 5
- 1.5 Block Diagram 6
- 1.6 Specifications 7
  - 1.6.1 Physical 7
  - 1.6.2 Mechanical 7
  - 1.6.3 Electrical 8
  - 1.6.4 Power 8
  - 1.6.5 Environmental 9
  - 1.6.6 Thermal/Cooling Requirements 10
- 1.7 Getting Started 13

2 Hardware 17
- 2.1 Major IC Definitions and Locations 17
- 2.2 Header and Connector Definitions and Locations 21
- 2.3 Jumper Header Definitions 25
- 2.4 Component Features 26
  - 2.4.1 CPU 26
  - 2.4.2 PCH 26
  - 2.4.3 SDRAM 26
  - 2.4.4 Gigabit Ethernet PHY Transceiver (I219 - Supporting GLAN1) 26
  - 2.4.5 Gigabit Ethernet Controller (I210 - Supporting GLAN2) 27
  - 2.4.6 SSD (Solid State Drive) 27
  - 2.4.7 BMC 27
  - 2.4.8 LM73 Temperature Sensor 27
  - 2.4.9 PTN3460I eDP-to-LVDS Converter 27
  - 2.4.10 SMBus Slave Addresses 28
- 2.5 Standard Connectors 28
  - 2.5.1 Micro HDMI (J8) 28
  - 2.5.2 Mini DisplayPort (J17) 29
  - 2.5.3 USB Type-C (J28) 30

3 Interfaces 31
- 3.1 Serial Interfaces (H16 and J18) 31
- 3.2 USB 2.0 Interface (H15 and J25) 33
- 3.3 Ethernet (H11 and J14) 34
- 3.4 Video (J8 [Micro HDMI], J17 [Mini DisplayPort], and J23 [LVDS]) 35
- 3.5 Power Interface (J24) 37

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3.6 User GPIO Interface (J26 and J27) 38
3.7 I2C / SMBus Interface (J31) 38
3.8 Utility Interface (J21) 39
3.8.1 Power Button 39
3.8.2 Reset Switch 39
3.8.3 Speaker 39
3.9 System Fan (J22) 40
3.10 Battery (J12) 40
3.11 External LEDs - Ethernet (J2 and J3) 41

4 Utilities 43
4.1 BIOS Setup 43
4.1.1 Menu Structure 43
4.1.2 Starting the BIOS Setup Utility 44
4.1.3 Main Menu 44
4.1.4 Advanced Menu 49
4.1.5 Boot Menu 68
4.1.6 Security Menu 69
4.1.7 Save & Exit Menu 70
4.2 BIOS Checkpoints, Beep Codes 71
4.2.1 Checkpoints and Beep Codes Definition 71
4.2.2 Aptio Boot Flow 71
4.2.3 Viewing BIOS Checkpoints 71
4.2.4 Status Code Ranges 72
4.2.5 Standard Status Codes 72
4.3 SEMA Functions 79
4.3.1 Board Specific SEMA functions 80
4.4 Real Time Clock (RTC) 81
4.5 Oops! Jumper (BIOS Recovery) 82
4.6 Serial Console 82
4.7 Serial Console BIOS Setup 82
4.8 Hot (Serial) Cable 82
4.9 Watchdog Timer 83

Appendix A System Resource.....85

Appendix B Technical Support.....89

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1 Product Overview

1.1 Description

The CMx-SLx is a PCI/104-Express Type 1 Single Board Computer (SBC) featuring the 64-bit 6th Generation Intel® Core™ i3 and Intel® Xeon® E3 processor (formerly “Skylake-H”), supported by the Intel® CM236 Chipset. The CMx-SLx is specifically designed for customers who need high-level processing and graphics performance in a long product life solution.

The CMx-SLx Intel processor supports Intel Hyper-Threading Technology and up to 16GB of soldered ECC DDR4 memory at 1866/2133 to achieve optimum overall performance.

Integrated Intel® Generation 9 Graphics includes features such as OpenGL 5.x, OpenCL 2.x, DirectX 2015, DirectX 12, Intel® Clear Video HD Technology, Advanced Scheduler 2.0, 1.0, XPDM support, and DirectX Video Acceleration (DXVA) support for full HEVC/VP8/VP9/AVC/MPEG2 hardware codec. Graphics outputs include single-channel 18/24-bit LVDS (eDP x4 lanes optional) and three DDI ports supporting HDMI/DVI/DisplayPort. The CMx-SLx is specifically designed for customers with high-performance processing graphics requirements who want to outsource the custom core logic of their systems for reduced development time.

The CMx-SLx features one mini DisplayPort (DDI1), one micro HDMI port (DDI2), and one single channel 18/24-bit LVDS port (eDP), two Gigabit Ethernet ports, four USB 2.0 ports, two COM ports, eight GPIOs (from BMC), two SATA 6Gb/s ports, and one onboard SATA SLC SSD up to 32GB capacity. The module is equipped with an SPI AMI EFI BIOS with CMOS backup, supporting embedded features such as fail safe BIOS, remote console, CMOS backup, hardware monitor, and watchdog timer.

The CMx-SLx is capable of working in the temperature ranges of 0°C to 60°C (standard) and -40°C to 85°C (extended).

1.2 About this Manual

This manual presents the supported features of the CMx-SLx Single Board Computer (SBC). After reviewing this document you should understand the following features of the CMx-SLx.

- Board Features
- Functional Block Diagram
- Major Component (IC) Locations and Descriptions
- Header, Connector, and Socket Locations and Descriptions
- Specifications
- Interface Signal Definitions
- Board Utilities

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1.3 Features

- CPU
  - 6th Gen Intel® Core™ i3 and Intel® Xeon® E3 processor (formerly “Skylake-H”)
    - Intel® Core™ i3-6102E 1.9GHz (no Turbo), 25W (2C/GT2)
    - Intel® Core™ i3-6100E 2.7GHz (no Turbo), 35W (2C/GT2)
    - Intel® Xeon® E3-1505L v5 2.0/2.8GHz (Turbo), 25W (4C/GT2)
  - DMI (Direct Media Interface) with 8 GT/s point-to-point interface to the chipset
  - Enhanced Intel SpeedStep® Technology (EIST)
  - Hyper-Threading Technology
  - Up to 3MB on-die L2 cache
  - 3D graphics engine
  - Dual-channel DDR4 memory controller (only one channel connected on board)
- Chipset
  - Intel CM236 PCH with ECC memory support
  - Gen3 PCIe support
  - 8 GT/s transfer rate
  - Sensor-enhanced
  - ECC memory support
- Memory
  - Up to 16GB of ECC DDR4 soldered, on-board memory
  - Eight non-ECC and one ECC, unbuffered SDRAM chips
  - Single-channel, 1866/2133MHz
  - Double Data Rate interface
  - 64-bit data bus
  - Non-ECC option
- BIOS
  - AMI EFI BIOS with CMOS backup of 8MB
  - SPI interface
  - Intel AMT 11.0 support for Xeon processors
  - SEMA fail-safe
- Expansion Buses
  - PCI bus version 2.3 at 33MHz
  - PCIe bus version 2.0 at 100MHz
- SATA Interface
  - Two SATA 6Gb/s ports from the CM236 PCH
  - eSATA capable
  - Up to 6Gb/second data transfer rate
  - Independent DMA operation
  - Native Command Queuing
  - Auto Activate for DMA
  - Hot Plug features
  - Two standard SATA 6Gb/s connectors
  - One SATA 3Gb/s port dedicated for the onboard SSD

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- Serial Interface
  - Two buffered serial ports (COM1-2) with full handshaking
  - Two 10-pin headers
  - 16550-equivalent controllers with 16-byte FIFO modes
  - Full-duplex buffering and full status reporting
  - Full modem capability
  - Programmable word length, stop bits, and parity
  - Programmable baud-rate generator
- USB 2.0 Interface
  - Two root USB 2.0 hubs
  - Up to six USB 2.0 ports
  - USB bootable devices
  - USB Keyboard and Mouse
  - USB v2.0 EHCI and v1.1 UHCI
  - Over-current detection status
  - Wake on USB at S3/S4
- USB 3.1 Interface
  - 1x USB 3.1 Gen1 (5Gbps) host port
  - 24-pin Type C connector
  - Battery charging support
- Ethernet Interface
  - Two fully independent Gigabit Ethernet ports
  - Integrated LEDs on each port (Link/Activity and Speed)
  - One Intel i210 IT controller chip and one i219 LM PHY transceiver chip
  - Two 10-pin headers for Gigabit Ethernet user interface
  - Two headers for GLAN LED signals
  - IEEE 802.3 10/100BaseT and 10/100/1000BaseT compatible physical layers
  - Auto-negotiation for speed, duplex mode, and flow control
  - Full-duplex or half-duplex mode
    - Full-duplex mode supports transmit and receive frames simultaneously
    - Supports IEEE 802.3x Flow control in full-duplex mode
    - Half-duplex mode supports enhanced proprietary collision reduction mode
- Video Interfaces (LVDS, DisplayPort, HDMI, and PEG)
  - LVDS flat panel outputs
    - Single channel capability
    - Resolutions up to 1280x720 at 60Hz
    - Pixel clock rates of up to 112MHz
    - Pixel color depths of 18 and 24 bits
  - DisplayPort
    - Resolutions up to 4096x2304 pixels at 60Hz
    - Pixel clock rates up to 605MHz
    - AC-3 Dolby Digital
    - Silent Stream Audio up to 192khz sampling rate

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- HDMI outputs
  - Resolutions up to 4096x2304 pixels at 30Hz
  - Pixel clock rates up to 605MHz
  - AC-3 Dolby Digital
  - Silent Stream Audio up to 192khz sampling rate
- PCI Express graphics (PEG)
  - External high-performance PCI Express graphics card support
  - General-purpose PCI Express device support
  - Transfer rate up to 8GT/s
  - Theoretical bandwidth of up to 15.8GB/s
  - PCIe Gen3 compliance

- GPIO Interface
  - Two 6-pin interface headers
  - Total of eight GPIO ports
  - Sample code by request
- Utility Interface
  - Power Button
  - Reset Switch
  - Speaker
- Miscellaneous
  - Real Time Clock (RTC) with external replaceable battery
  - Battery-free boot
  - Oops! Jumper support
  - Serial Console support
  - Watchdog Timer
  - Logo Screen (Splash)
  - SSD (Solid State Drive)
  - Hardware Monitor (voltage and temperature)



Other configurations are possible. Please contact your local ADLINK Technology representative to discuss requirements.

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1.4 Ordering Information

Table 1-1: CMx-SLx Models

Model Number	Description
CM4-SL2-6102E-8G-8G	PCI/104-Express Type 1 SBC, Intel® Core™ i3-6102E (max. 1.9GHz), 8GB DDR4 ECC, 8GB SLC SATA-SSD, 0°C to +60°C
CM4-SL2-6102E-8G-8G-ETT	PCI/104-Express Type 1 SBC, Intel® Core™ i3-6102E (max. 1.9GHz), 8GB DDR4 ECC, 8GB SLC SATA-SSD, -40°C to +85°C
CM4-SL2-6102E-8G-8G-CC	PCI/104-Express Type 1 SBC, Intel® Core™ i3-6102E (max. 1.9GHz), 8GB DDR4 ECC, 8GB SLC SATA-SSD, 0°C to +60°C, conformal coating “Humiseal 1B73”
CM4-SL2-6102E-8G-8G-ETT-CC	PCI/104-Express Type 1 SBC, Intel® Core™ i3-6102E (max. 1.9GHz), 8GB DDR4 ECC, 8GB SLC SATA-SSD, -40°C to +85°C, conformal coating “Humiseal 1B73”
CM4-SL2-6100E-16G-32G	PCI/104-Express Type 1 SBC, Intel Core i3-6100E (2.7GHz), CM236 chipset, 16G DDR4-ECC, 32G SLC SATA-SSD, 0°C to + 60°C
CM4-SL4-1505L-16G-32G	PCI/104-Express Type 1 SBC, Intel ® Xeon® E3-1505L v5 (2.0GHz), CM236 chipset, 16G DDR4-ECC, 32G SLC SATA-SSD, 0°C to + 60°C

Table 1-2: Cable Sets and Accessories

Model Number	Description
CMx-SLx-X-10	CMx-SLx Cable Kit
CMx-SLx-TM-00	CMx-SLx Heat Spreader
CMx-SLx-TM-10	CMx-SLx Passive Heat Sink (0°C to +60°C)
CMx-SLx-TM-20	CMx-SLx Active Heat Sink for i3-6102E CPU 25W CPU (-40°C to +85°C)

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1.5 Block Diagram

Figure 1-1 provides a functional representation of the CMx-SLx.

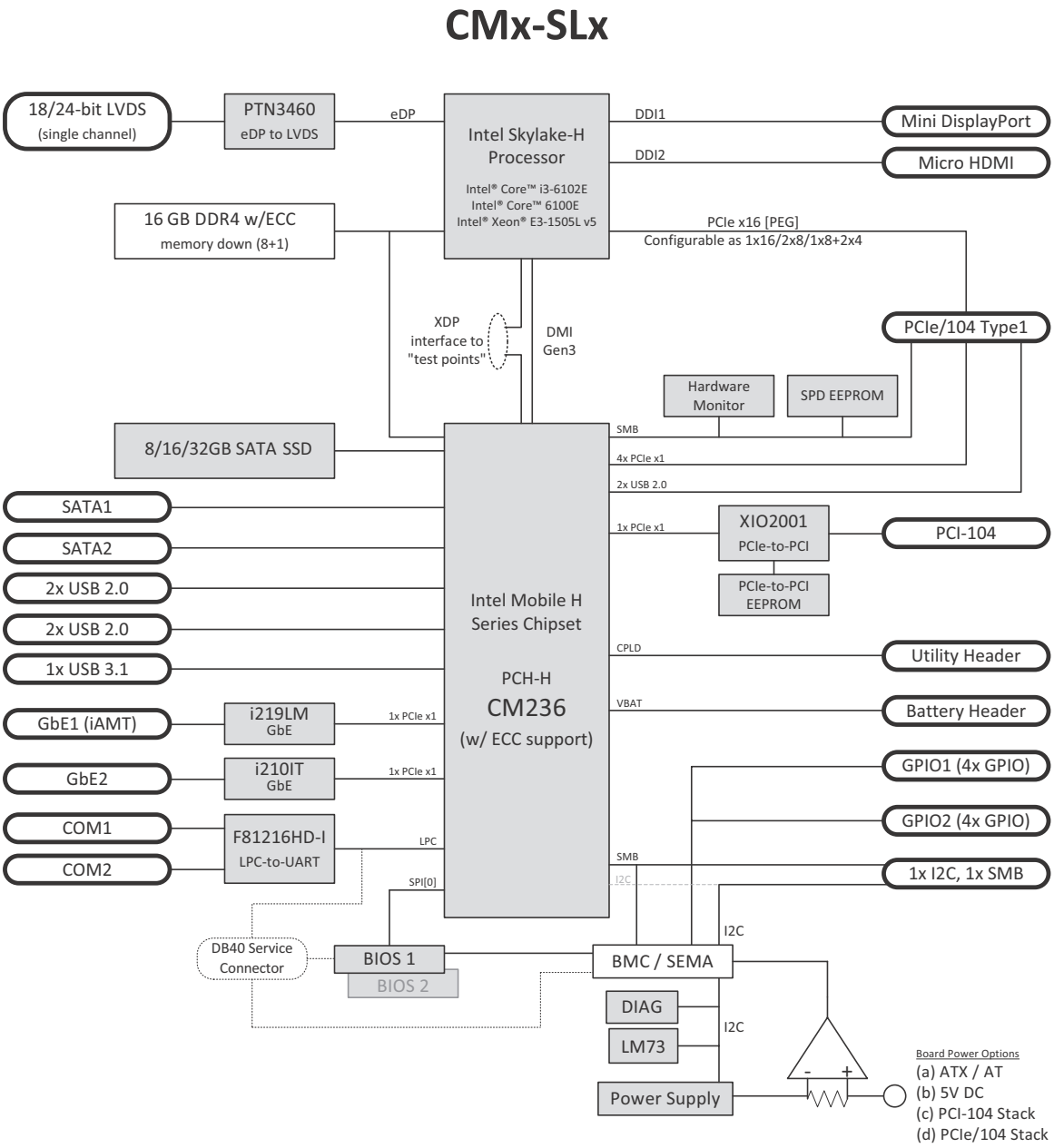


Figure 1-1: Functional Block Diagram

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1.6 Specifications

1.6.1 Physical

Table 1-3 provides the physical dimensions of the module.

Table 1-3: Weight and Footprint Dimensions

Item	Dimension	
Weight	0.12 kg (0.25 lbs)	Overall height is measured from the upper board surface to the highest permanent component (GLAN1 header) on the upper board surface. This measurement does not include the heatsink, which can vary. The heatsink could increase this dimension.
Height (overall)	9.35 mm (0.370) inches)	
Board thickness	2.50 mm (0.098 inches)	
Width	95.89 mm (3.78 inches)	
Length	117.40 mm (4.62 inches)	

1.6.2 Mechanical

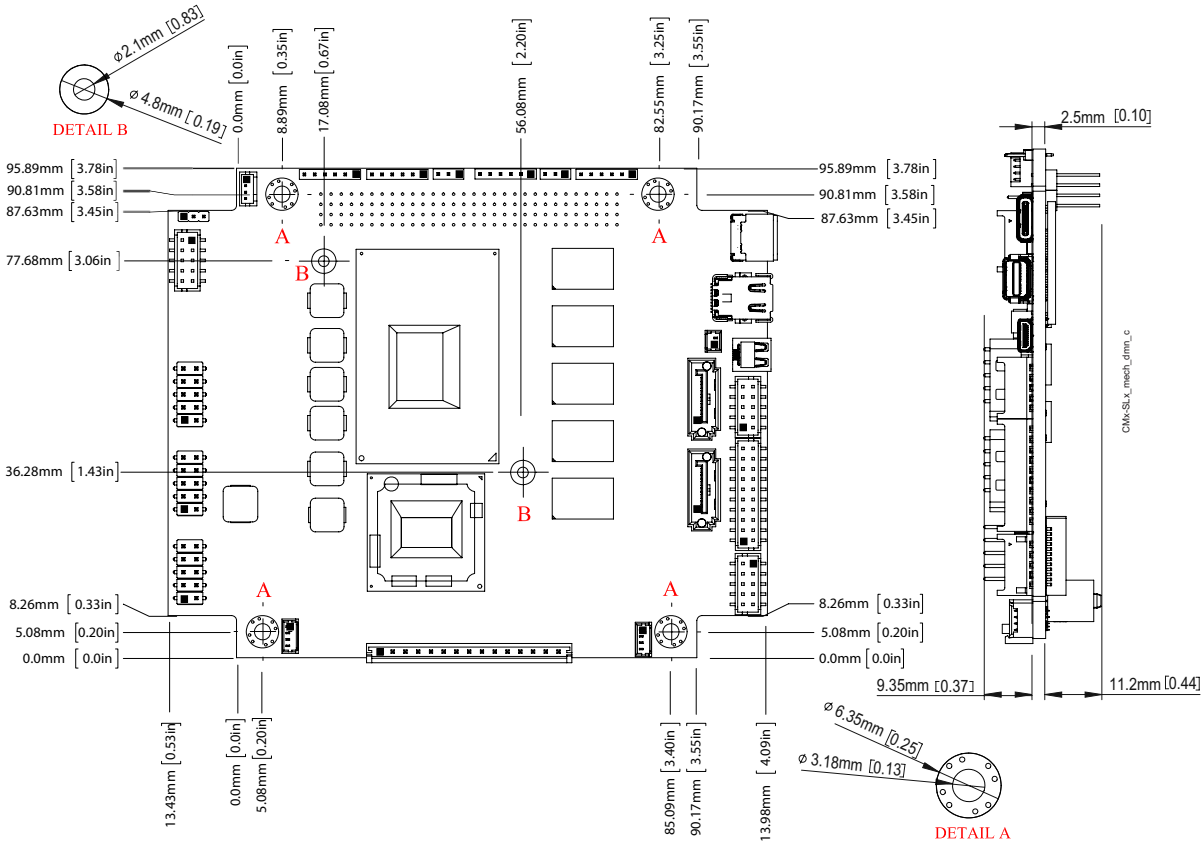


Figure 1-2: Mechanical Overview (Top Side)

NOTE:

All dimensions are given in inches and millimeters. Pin 1 is shown as a solid, black square on headers and connectors.

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1.6.3 Electrical

Table 1-4 specifies the electrical characteristics of the module.

Table 1-4: Electrical Specifications

Parameter	Value
Voltage Input	
Input Modes	▶ ATX and AT (AT mode startup controlled by SEMA and BMC)
Standard Inputs	▶ ATX = 5V±5% / 5Vsb ±5% ▶ AT = 5V±5% ▶ PCIe/104 Power Module = 5V±5% NOTE: If the power supply also provides 3.3VDC and 12VDC to the board, only the 5-volt signals are routed to the I/O interfaces on the board. The 12-volt signals are routed to the PCIe/104, PCI-104, and LVDS interfaces. The 3.3-volt signals are routed to the PCI-104 interface.
RTC	▶ 3.0V, 2.0V to 3.3V (battery), +/-30mV ripple
Power States (for all Standard Inputs)	▶ C1-C6, S0, S3, S4, S5 (Wake-on-USB S3/S4, Wake-on-LAN S3/S4/S5)
Power Management	▶ ACPI 4.0 compliant

1.6.4 Power

Table 1-5 provides the power consumption values of the CMx-SLx.

.

Table 1-5: Power Supply Requirements

Parameters	24W, Core i3-6102E SoC
Input Type	Regulated DC voltage
Typical Idle Current and Power (EIST enabled; 3TB HDD; Windows 10 Enterprise Operating System)	2.15A (10.75W) @ 5V
Typical Operating Mode Current and Power (EIST enabled; 3TB HDD; Windows 10 Enterprise Operating System)	5.26A (26.30W) @ 5V
Maximum Operating Mode Current and Power (EIST disabled; 3TB HDD; Windows 10 Enterprise Operating System; Intel TAT tool v5.0.1026)	6.69A (33.45W) @ 5V
System S3 mode (3TB HDD; Windows 10 Enterprise Operating System)	0.22A (1.10W) @ 5VSB
System S4 mode (3TB HDD; Windows 10 Enterprise Operating System)	0.175A (0.875W) @ 5VSB
System S5 mode with ECO enabled (3TB HDD; Windows 10 Enterprise Operating System)	0.012A (0.06W) @ 5VSB

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1.6.5 Environmental

Table 1-6 provides the most efficient operating and storage condition ranges required for this module.

Table 1-6: Environmental Requirements

Parameter	Conditions
Temperature	
Operating	-40°C to +85°C (-40°F to +185°F) NOTE: this temperature range requires the CMx-SLx-TM-20 active heatsink with specified airflow.
Storage	–55°C to +85°C (–67°F to +185°F)
Humidity	
Operating	5% to 90% relative humidity, non-condensing
Non-operating	5% to 95% relative humidity, non-condensing

Table 1-7 provides results for shock and vibration tests performed on the board.

Table 1-7: Shock and Vibration

Parameter	Result
Shock Test	50G peak-to-peak, 11ms duration, MIL-STD-202G, Method 213B
Random Vibration Test	Operating 11.96Grms, 50-2000Hz, each axis, MIL-STD-202G, Method 214A

Table 1-8 presents the average times between system failures.

Table 1-8: Mean Time Between Failures

Parameter	Value
MTBF at 40°C	309,759 hrs (according to MIL calculation)
MTBF at 85°C	71,063 hrs (according to MIL calculation)

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1.6.6 Thermal/Cooling Requirements

The CMx-SLx is designed to operate at its maximum CPU speed and requires a thermal solution to cool the CPU. ADLINK offers an active heatsink, a heat spreader, and a passive heatsink (separate order numbers) for cooling. The heatsinks can be used for module evaluation. If a custom heatsink is used, it is recommended to connect it to the ADLINK heat spreader. This facilitates future module upgrades without the need to re-design the custom heatsink. Refer to Figure 1-3 for active heatsink dimensions. See Figure 1-4 for passive heatsink and heat spreader dimensions. Figure 1-6 provides airflow specifications. See “Getting Started” on page 13 for installation instructions.

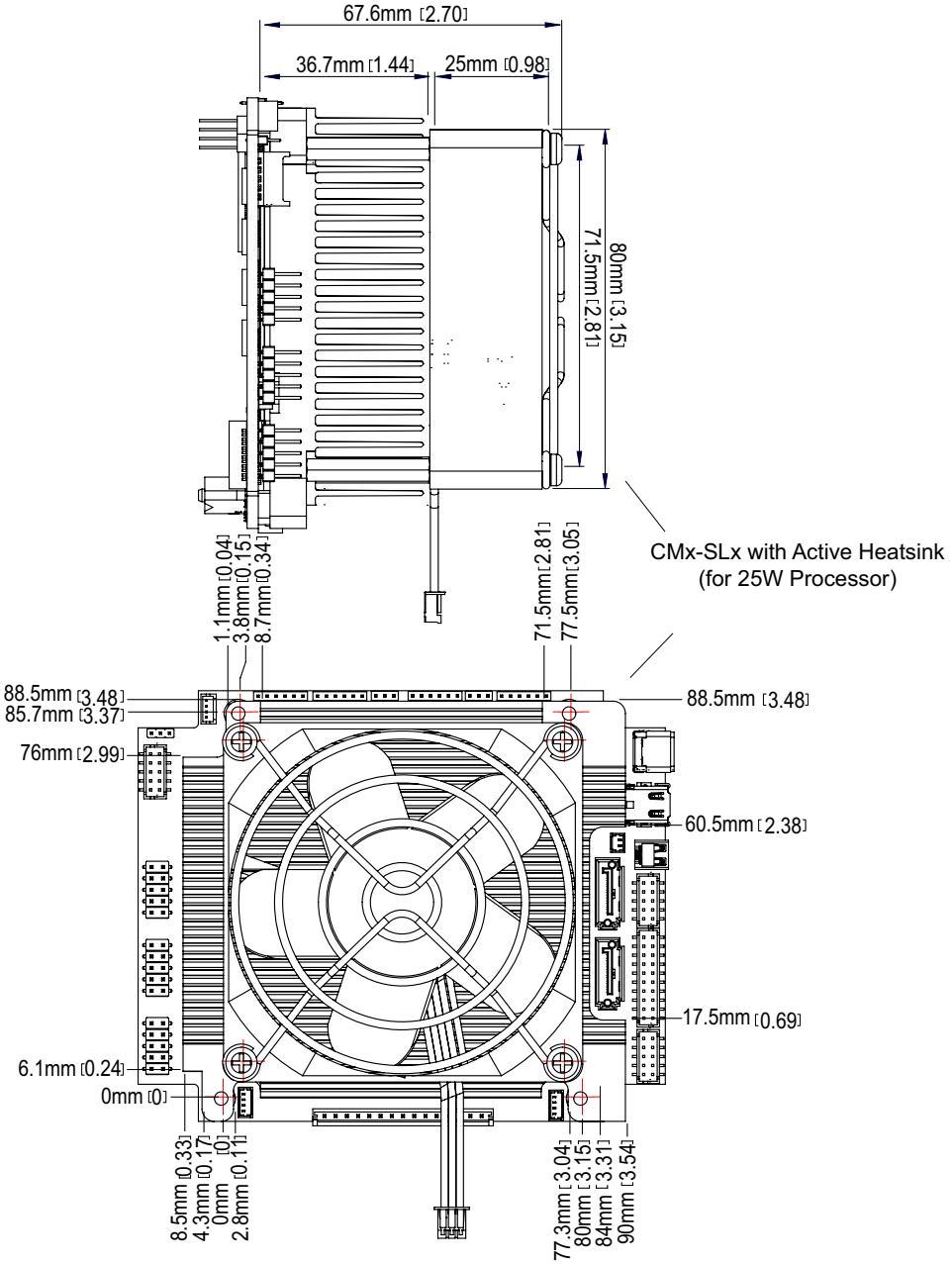


Figure 1-3: Active heatsink mounting dimensions (top side)

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Figure 1-4 provides dimensions and mounting orientations of the passive heatsink and the heat spreader.

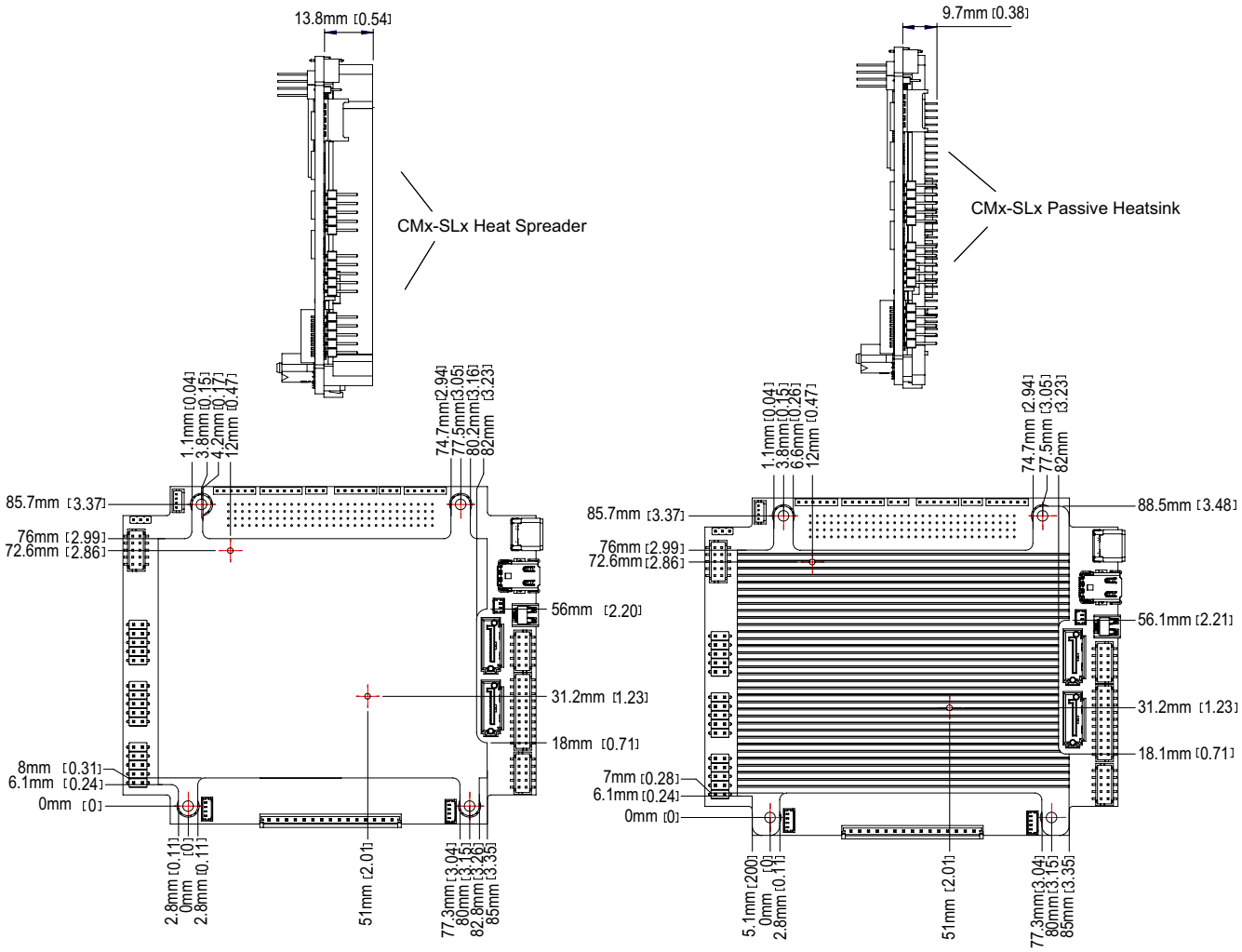


Figure 1-4: Passive Heatsink and Heat Spreader mounting dimensions (top side)

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Figure 1-5 provides airflow versus ambient temperature ratios with regard to one airflow direction. See Figure 1-6 for an illustration of the airflow direction.

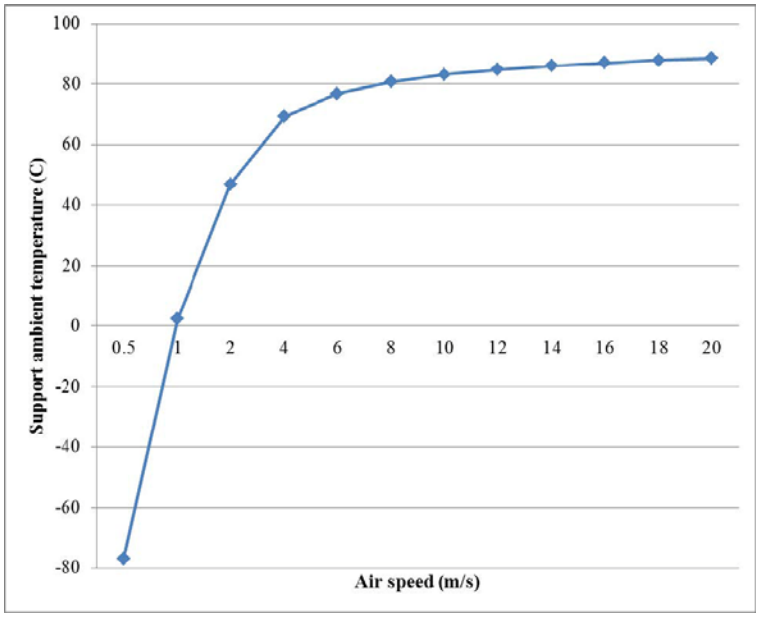


Figure 1-5: Temperature vs Airflow Chart

Figure 1-6 presents direction of airflow across the fins of the passive heatsink. Refer to Figure 1-5 for required airflow with regard to ambient temperature.

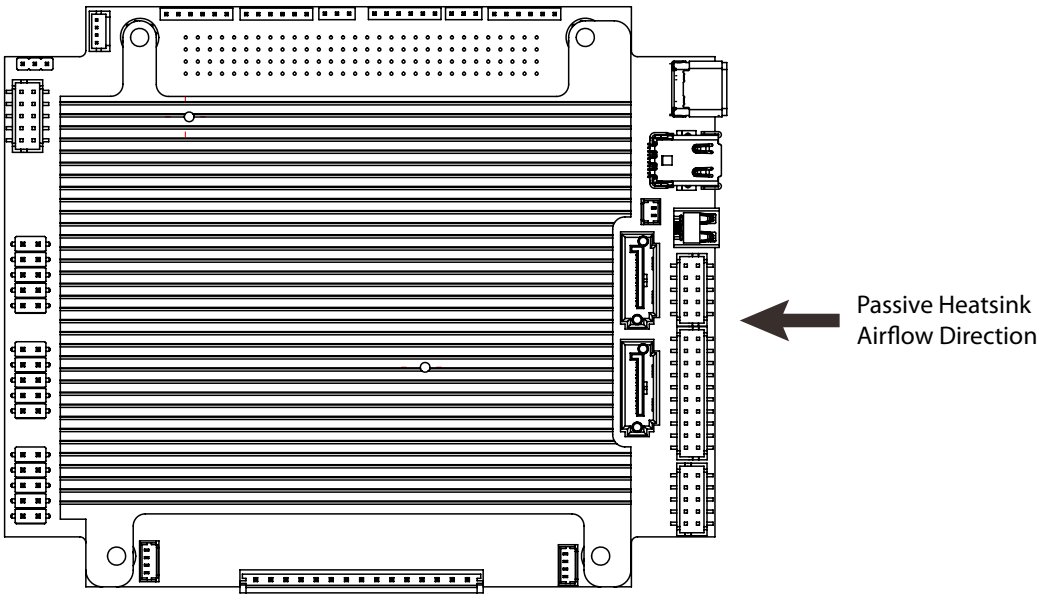


Figure 1-6: Airflow Directions with CMx-SLx-TM-10 Heatsink

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1.7 Getting Started

This section provides the most efficient way to setup and power on your CMx-SLx SBC. Select a clean flat, anti-static work surface for setup and operation, large enough to include any external peripherals and optional devices.

CAUTION:
MISE EN GARDE

Be sure to observe ESD prevention measures. Make sure you are always at the same potential as the module.

Assurez-vous de respecter les mesures de prévention des décharges électrostatiques. Assurez-vous que vous êtes toujours au même potentiel que le module.

CAUTION:
MISE EN GARDE

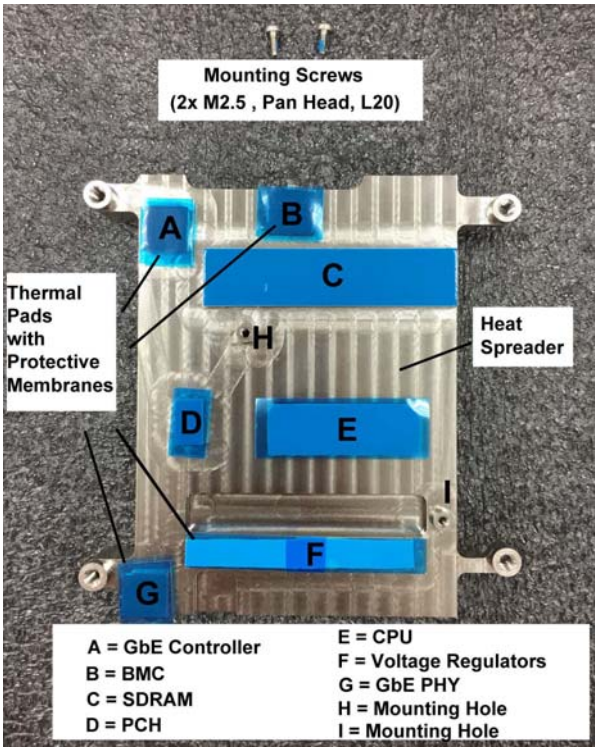
Never connect or disconnect peripherals like HDDs while the power supply is connected and switched on.

Ne connectez ou ne déconnectez jamais des périphériques tels que des disques durs lorsque l'alimentation est connectée et sous tension.

Use the following steps to mount the heat spreader to the top side of the board, covering the CPU, PCH, SDRAM, Ethernet PHY, Ethernet controller, BMC, and voltage regulators with the respective thermal pads on the heat spreader. The heat spreader provides a neutral plane for mounting a custom heat sink.

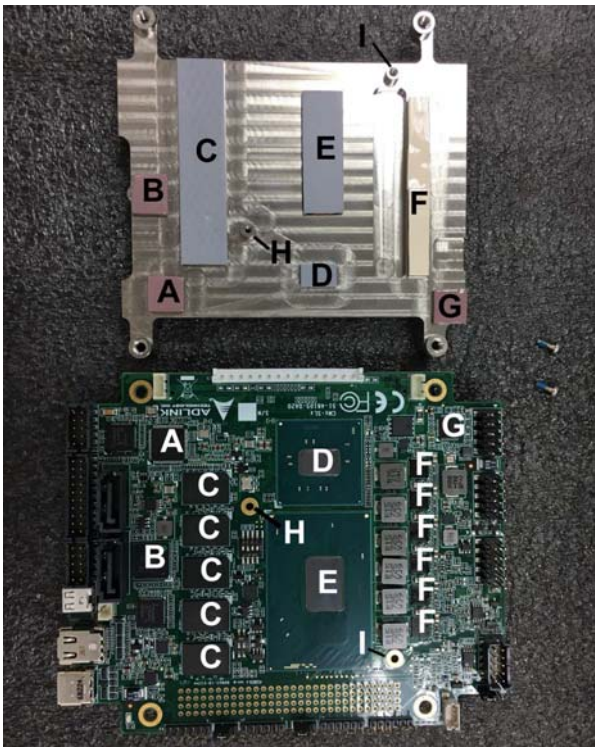
NOTE:

If the passive or active heatsink is required instead of the heat spreader, use the same mounting procedure used for the heat spreader, as described in the following steps. See “Thermal/Cooling Requirements” on page 10 for cooling solution requirements.



1. Remove the blue protective membranes from the thermal pads on the heat spreader.

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2. Align the thermal pads on the heat spreader with their respective components on the board.

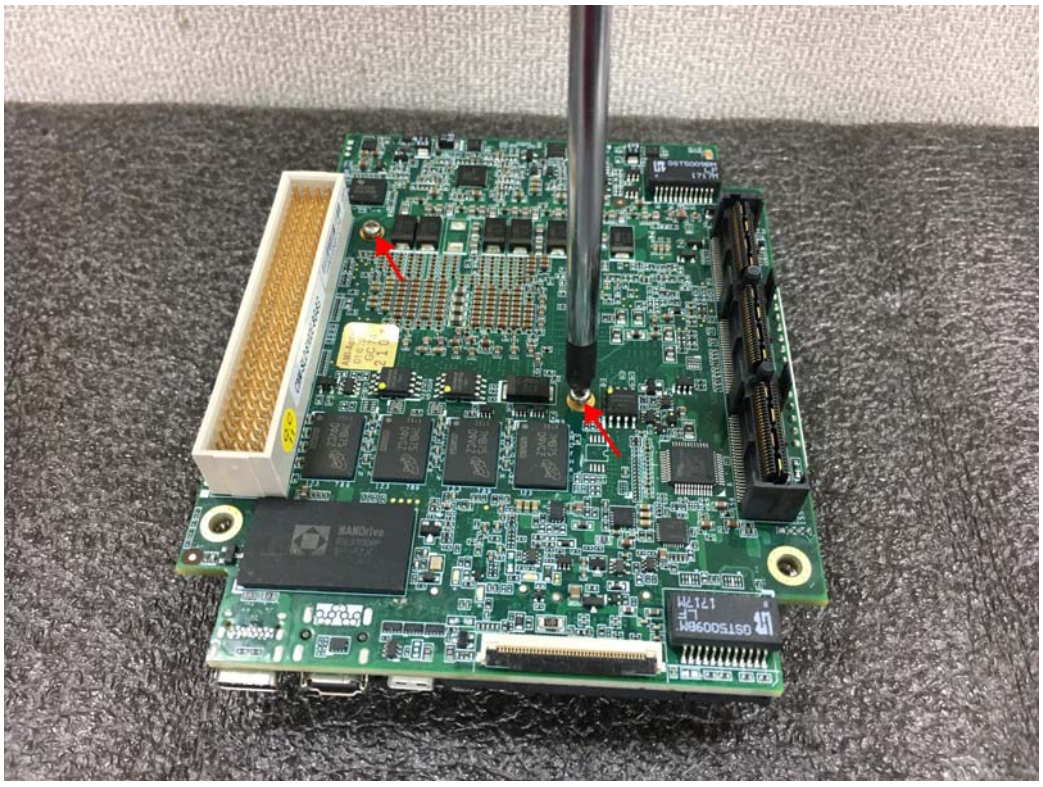


3. Turn over the heat spreader so that the two mounting holes line up with the corresponding holes on the board, and the thermal pads line up with their respective components on the board.

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4. Place the heat spreader on top of the board ensuring that the thermal pads entirely cover and adhere to their respective components on the board.



5. Turn over the assembly so that the board lays on top of the heat spreader and the heat spreader lays on the work surface. 6. Install two M2.5, pan head, L20 mounting screws at 2kgf. cm torque in the two mounting holes on the board. See the two red arrows in the photo above for locations of the mounting holes.

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NOTE:

The passive and active heatsinks mount on top of the board (without the heat spreader) using the same installation steps for the heat spreader, provided above.

Use the cable set provided by ADLINK Technology to connect the CMx-SLx to an LCD monitor. Connect either PS/2 or USB keyboard or mouse, respectively. Use the SATA cable to connect the hard disk. Make sure that the pins match their counterparts correctly and are not twisted. If you plan to use additional peripherals, connect them to the appropriate headers.

Connect a 5-volt, 5 amps power supply to the power connector and switch on the power.

NOTE:

The 5 amps value is the minimum you should have for the standard peripherals mentioned. For additional peripherals, make sure enough power is available. The system will not work if there is not enough supply current for all your devices.

The display shows the BIOS messages. If you want to change the standard BIOS settings, press the <DEL> key to enter the BIOS setup menus. See Chapter 4 for setup details.

If you need to load the BIOS default values, they can be automatically loaded at boot time.

The CMx-SLx boots from CD drives, USB flash drives, hard disks, or microSD cards. If the media is connected and contains a valid operating system image, the display then shows the boot screen of your operating system.

The CMx-SLx needs adequate cooling measures depending on the desired operating temperature range. Using the board without cooling could damage the board permanently.

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2 Hardware

This chapter describes the major integrated circuits (ICs) and interface connectors and headers on the module. The third and fourth sections of this chapter further describe the major ICs (including the manufacturers' model numbers) and the standard interface connectors on the board.

2.1 Major IC Definitions and Locations

Table 2-1 describes the major ICs on the CMx-SLx, including a brief description of each IC. Figures 2-1 and 2-2 show the locations of the major ICs.

Table 2-1: Major Component Descriptions and Functions

Chip Type	Mfg.	Model	Description	Function
CPU (CPU1)	Intel	Core™ i3-6102E, 1.9GHz (25W tuned to 17W) Core™ i3-6100E, 2.7GHz (35W) Xeon® E3-1505L v5, 2.0GHz (25W)	Central Processing Unit with 2 execution cores and up to 3MB L2 cache	Integrates Processor Core and Graphics Memory Controller Hub
Gigabit Ethernet PHY Transceiver (LU1)	Intel	WGI219LM SLKJ3	Single-port Gigabit Ethernet PHY Transceiver for GLAN1 interface	Provides a standard IEEE 802.3 Ethernet interface for Ethernet transfer rates up to 1000 Mb/s
Chipset (PCH1)]	Intel	CM236	I/O Hub for common user interfaces	Provides Southbridge interfaces and off loads some Northbridge functions from the CPU
DDR4 SDRAM (U3, U5, U7, U9, [and U11 to enable ECC])	Micron Hynix	N/A	On-board DDR4, memory module	Provides high-speed data transfer
DDR4 SDRAM (U4, U6, U8, U10 - all on bottom side [see Figure 2-2])	Micron Hynix	N/A	On-board DDR4, memory module	Provides high-speed data transfer
Ethernet EEPROM (U20)	Winbond	W25Q16DVSSIG	Three-Wire Serial EEPROM for Gigabit Ethernet Controller	Provides storage for MAC addresses, serial numbers, and pre-boot configuration data
Gigabit Ethernet Controller (U21 on bottom side; see Figure 2-2)	Intel	WGI210IT SLJXT	Single-port Gigabit Ethernet controller for GLAN2 interface	Integrates GbE MAC, PHY, and SGMII/SerDes to enable 10T/100TX/1000T Ethernet signals using the PCIe x1 bus

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Table 2-1: Major Component Descriptions and Functions (Continued)

Chip Type	Mfg.	Model	Description	Function
Embedded DisplayPort-to-LVDS Converter (U22)	NXP	PTN3460	Embedded DisplayPort (eDP) to LVDS bridge device that enables connectivity between an embedded DisplayPort (eDP) source and an LVDS display panel.	Processes the incoming embedded DisplayPort (eDP) stream, performs eDP to LVDS protocol conversion, and transmits processed stream in LVDS format.
LPC-to-UART Controller (U26)	Fintek	F81216AU-I	Serial communication controller	Provides 4 UART ports through the LPC bus
RS-232 Transceiver (U27)	Texas Instruments	TRS3253EIRSMR	Transceiver for Serial 1 RS-232 signals	Transmits and receives RS-232 signals for COM1
RS-232 Transceiver (U28)	Texas Instruments	TRS3253EIRSMR	Transceiver for Serial 2 RS-232 signals	Transmits and receives RS-232 signals for COM2
Solid State Drive [SSD] - SATA (U29) - on bottom side [see Figure 2-2])	Greenliant	8GB: GLS85LS1008P 32GB GLS85LS1032P	Industrial-grade soldered solid-state storage module	Provides solid state storage through SATA 6Gb/s port
HDMI Level Shifter (U38)	NXP	PTN3360DBS	HDMI level-shift IC for HDMI video	Converts HDMI differential input from the PCH to TMDS differential output for the HDMI interface
BMC (U46)	Texas Instruments	TM4C123BH6ZRBT7R	Microcontroller	Provides logistics and forensic information, flat panel control, I2C bus control, user flash, Watchdog Timer and fan control
Temperature Sensor - CPU (U47 on bottom side; see Figure 2-2)	Texas Instruments	LM73	Digital-output temperature sensor	Measures its own temperature and the temperature of the CPU thermal diode and provides temperature correction with fan speed control.

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Table 2-1: Major Component Descriptions and Functions (Continued)

Chip Type	Mfg.	Model	Description	Function
SPI Flash (U50 and U52)	Macronix	MX25L12835FM2I-10GRT	Serial Peripheral Interface Flash Memory chip (for firmware)	Stores BIOS 0 and BIOS 1 in Flash Memory
EEPROM, PCIe-to-PCI Bridge (U57 - on bottom side [see Figure 2-2])	Atmel	AT24C08D	Two-Wire Serial EEPROM for PCIe-to-PCI Bridge	Stores PCIe-to-PCI bridge configuration data
PCIe-to-PCI Bridge (U58)	Texas Instruments	XIO2001	PCIe-to-PCI interface	Migrates legacy PCI interfaces
Gb Ethernet Transformer (TF3 - on bottom side) [see Figure 2-2]	BOTHHAND	GST5009M	Gigabit Ethernet Magnetics	Provides electrical isolation for Gigabit Ethernet PHY transceiver (GLAN1)
Gb Ethernet Transformer (TF2 - on bottom side) [see Figure 2-2]	BOTHHAND	GST5009M	Gigabit Ethernet Magnetics	Provides electrical isolation for Gigabit Ethernet controller (GLAN2)

Key:
CPU1 - CPU
LU1 - Ethernet PHY Transceiver
PCH1 - PCH
U3 - DDR4 SDRAM
U5 - DDR4 SDRAM
U7 - DDR4 SDRAM
U9 - DDR4 SDRAM
U11 - DDR4 SDRAM (ECC)
U21 - Gigabit Ethernet Controller
U22 - DisplayPort-to-LVDS Converter
U38 - HDMI Level Shifter
U46 - BMC
U47 - Temerature Sensor
U57 - PCIe-to-PCI Bridge EEPROM

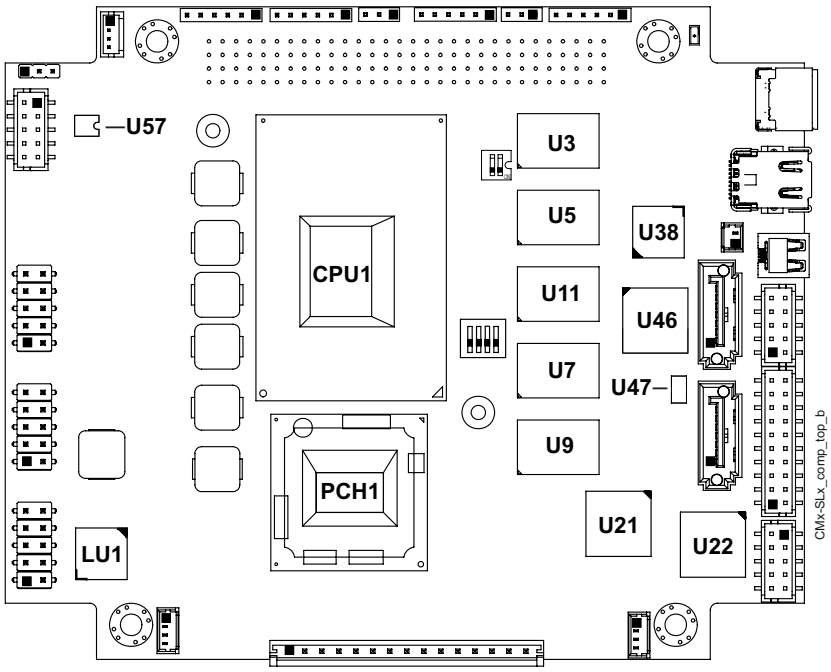


Figure 2-1: Component Locations (Top Side)

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Key:
U4 - DDR4 SDRAM
U6 - DDR4 SDRAM
U8 - DDR4 SDRAM
U10 - DDR4 SDRAM
U20 - Gigabit Ethernet EEPROM
U26 - LPC-to-UART Controller
U27 - RS-232 Transceiver (COM1)
U28 - RS-232 Transceiver (COM2)
U29 - SSD (Solid State Drive)
U50 - BIOS1
U52 - BIOS2
U58 - PCIe-to-PCI Bridge
TF2 - GbE 2 Transformer
TF3 - GbE 1 Transformer

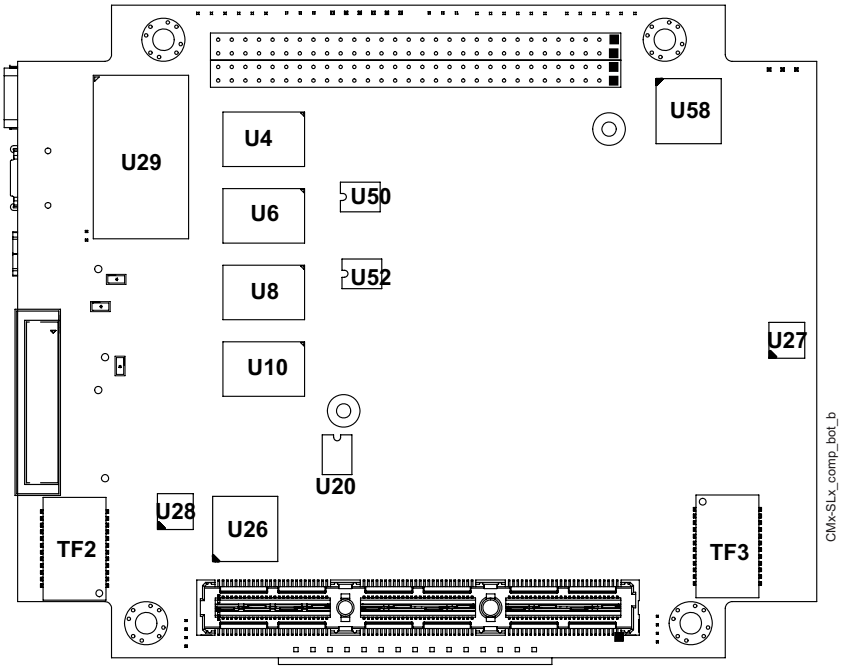


Figure 2-2: Component Locations (Bottom Side)

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2.2 Header and Connector Definitions and Locations

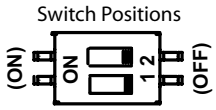
Table 2-2 describes the headers, connectors, and sockets shown in Figures 2-3 and 2-4.

Table 2-2: Header and Connector Descriptions

Header/Connector #	Access	Description
H11 – GLAN1	Top	10-pin, 0.100" (2.54mm) header for Gigabit Ethernet port 1 (JIH JVE, 21N22564-10M00B-01G-6-C-02)
H15 – USB (0-1)	Top	10-pin, 0.100" (2.54mm) header for USB 2.0 ports 0-1 (JIH JVE, 21N22564-10M00B-01G-6-C-02)
H16 – COM1	Top	10-pin, 0.100" (2.54mm) header for serial port 1 (JIH JVE, 21N22564-10M00B-01G-6-C-02)
J2 – LED - GLAN1	Top	4-pin, 0.049" (1.25mm) shrouded, single-row header for Gigabit Ethernet port 1 LED (REGO, 830-1251-02STD-3.2-6T)
J3 – LED - GLAN2	Top	4-pin, 0.049" (1.25mm) shrouded, single-row header for Gigabit Ethernet port 2 LED (REGO, 830-1251-02STD-3.2-6T)
J6 – PCIe/104	Bottom	156-pin, 0.025" (0.64mm) standard PCI Express connector for SMBus, USB 2.0, PCIe x1, and PCI interfaces (SAMTEC, ASP-129646-03)
J7 – PCI-104	Bottom	60-pin, 0.079" (2mm) standard PCI-104, male connector for PCI interfaces (EPT, 264-17302)
J8 – HDMI (Micro)	Top	19-pin, 0.016" (0.04mm), standard micro-connector for HDMI Type D video port (MOLEX, 46765-0001)
J10 – SATA0	Top	7-pin, 0.050" (1.27mm) standard connector for SATA 6Gb/s port 0 (WIN WIN, WATF-07DBLBA1UW)
J12 – Battery	Top	2-pin, 0.049" (1.25mm) shrouded header for power from external battery (REGO, 830-1251-02STD-3.2-6T)
J13 – SATA1	Top	7-pin, 0.050" (1.27mm) standard connector for SATA 6Gb/s port 1 (WIN WIN, WATF-07DBLBA1UW)
J14 – GLAN2	Top	10-pin, 0.079" (2mm) shrouded header for Gigabit Ethernet port 2 (CST, CSI-2221-102R)
J17 – DisplayPort (MIni)	Top	20-pin, right-angle Thunderbolt connector for Mini DisplayPort interface (FOXCONN, 3VT11207-N730-7H)
J18 – COM2	Top	10-pin, 0.079" (2mm) shrouded header for serial port 2 (CST, CSI-2221-102R)
J21 – Utility	Top	6-pin, 0.079" (2mm) single-row header for Power Button, Reset Switch, and Speaker (SAMTEC, TMM-106-03-L-S)
J22 – Fan	Top	4-pin, 0.049" (1.25mm) single-row, shrouded header for power to external fan (HIROSE, DF13-4P-1.25DSA)
J23 – LVDS	Top	20-pin, 0.079" (2mm) shrouded header for LVDS video port (CST, CSI-2221-202R)
J24 – Power	Top	15-pin, 0.100" (2.54mm) shrouded, straight header for supplying external power to the board (JST, B15B-EH-A/LF)

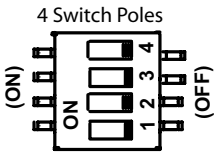
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Table 2-2: Header and Connector Descriptions (Continued)

Header/Connector #	Access	Description
J25 – USB 2-3	Top	10-pin, 0.079" (2mm) shrouded header for USB 2.0 ports 2-3 (CST, CSI-2221-102R)
J26 – GPIO1, (ports 5-8)	Top	6-pin, 0.079" (2mm) single-row header for GPIO1, ports 5-8 (SAMTEC, TMM-106-03-L-S)
J27 – GPIO2 (ports 1-4)	Top	6-pin, 0.079" (2mm) single-row header for GPIO2, ports 1-4 (SAMTEC, TMM-106-03-L-S)
J28 – USB Type-C	Top	24-pin, standard female right-angle connector for USB 3.1 host function (FOXCONN, UT11113-11604-7)
J29 – DB40 Debug	Bottom	40-pin, DB40 Front-Flip connector for debug card (Molex, 502790-4091)
J30 – Fan Voltage Select (see Table 2-3 for settings)	Top	3-pin, 0.079" (2mm) single-row jumper header for setting the fan interface voltage (JIH21N1250-03S10B-01G-4/2.8-G)
J31 – I2C / SMBus	Top	6-pin, 0.079" (2mm) single-row header for I2C and SMBus interfaces (SAMTEC, TMM-106-03-L-S)
JP1 – LVDS Voltage Select	Top	3-pin, 0.079" (2mm) single-row jumper header for setting the LVDS interface voltage (JIH21N1250-03S10B-01G-4/2.8-G)
JP2 – PCI-104 Voltage Select	Top	3-pin, 0.079" (2mm) single-row jumper header for setting the PCI-104 interface voltage (JIH21N1250-03S10B-01G-4/2.8-G)
LED1 – BMC Status	Bottom	Indicates system-error blink codes (Blue) [LIGITEK, LG-192DBK-CT/T]
LED2 – +3V3 Standby Power On	Bottom	Indicates standby power on (Green) [LIGITEK, LG-192G-CT]
LED3 – Watchdog Status	Bottom	Indicates triggered watchdog timer (Red) [LIGITEK, LG-192HRF-CT]
LED4 – +5V Power On	Top	Indicates +5V power on (Green) [LIGITEK, LG-192G-CT]
SW1 – PCIe x16 Lane Configuration Switch	Top	2-pole dip switch for selecting CPU PCIe x16 lane configurations (WIN WIN, DHN-02-T-V-T/R) Switch Positions = Lane Configurations 1-OFF, 2-OFF = 1x16 [Default] 1-OFF, 2-ON = 2x8 1-ON, 2-OFF = Reserved 1-ON, 2-ON = 1x8, 2x4 

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Table 2-2: Header and Connector Descriptions (Continued)

Header/Connector #	Access	Description
SW2 – BIOS Reset Configuration Switch	Top	4-pole dip switch for configuring BIOS reset (DIPTRONICS, DHNF-04-T-Q-T/R) Pole 1 - CPU_BIOS_Default ▶ OFF= User settings active [default] ▶ ON = Resets BIOS user settings Pole 2 - BIO_ Mode ▶ OFF = Failsafe BIOS [default] ▶ ON = Normal BIOS Pole 3 - SEL_BIOS ▶ OFF = BIOS 1 active ▶ ON = BIOS 0 active [default] Pole 4 - POSTWDT_DIS# ▶ OFF = Watchdog timer disabled [default] ▶ ON = Watchdog timer active 

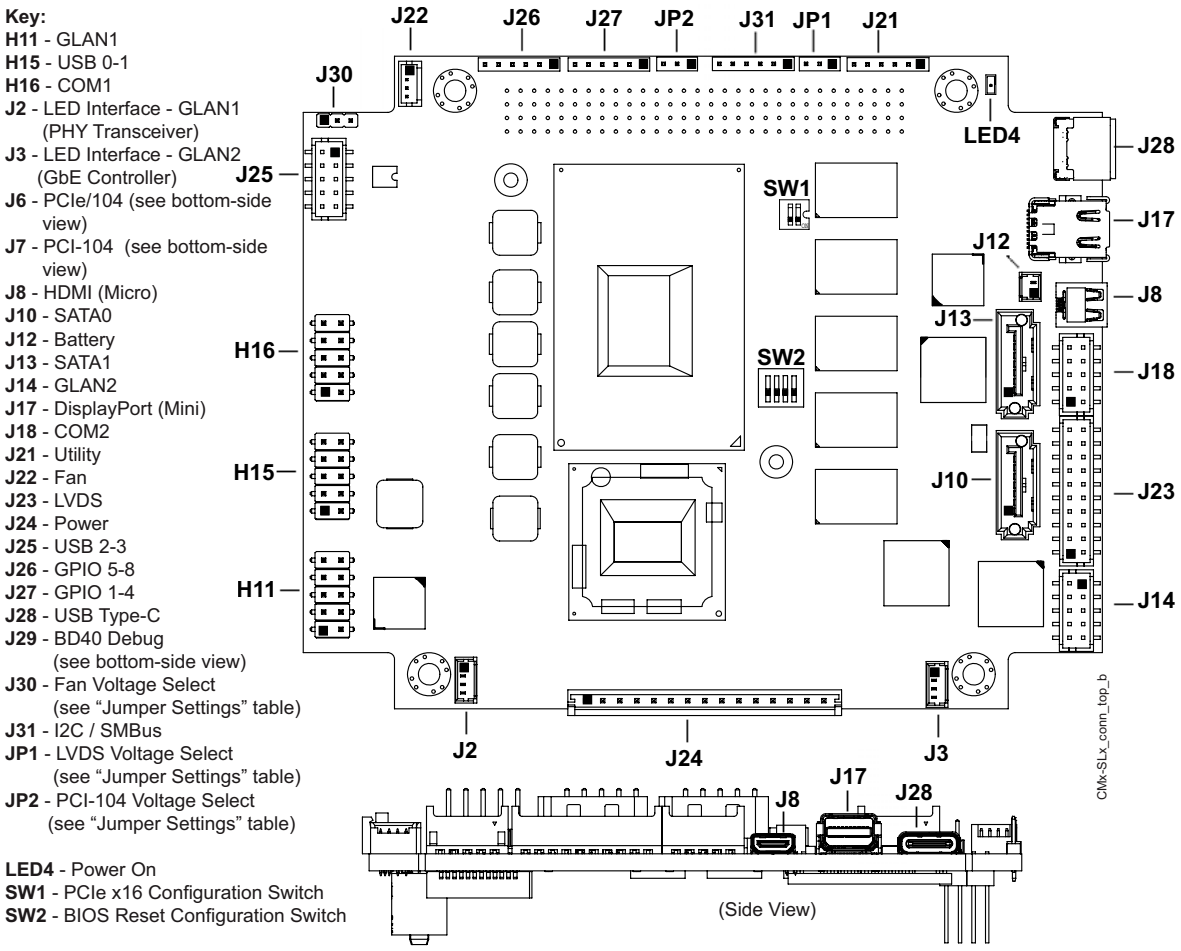


Figure 2-3: Header and Connector Locations (Top Side)

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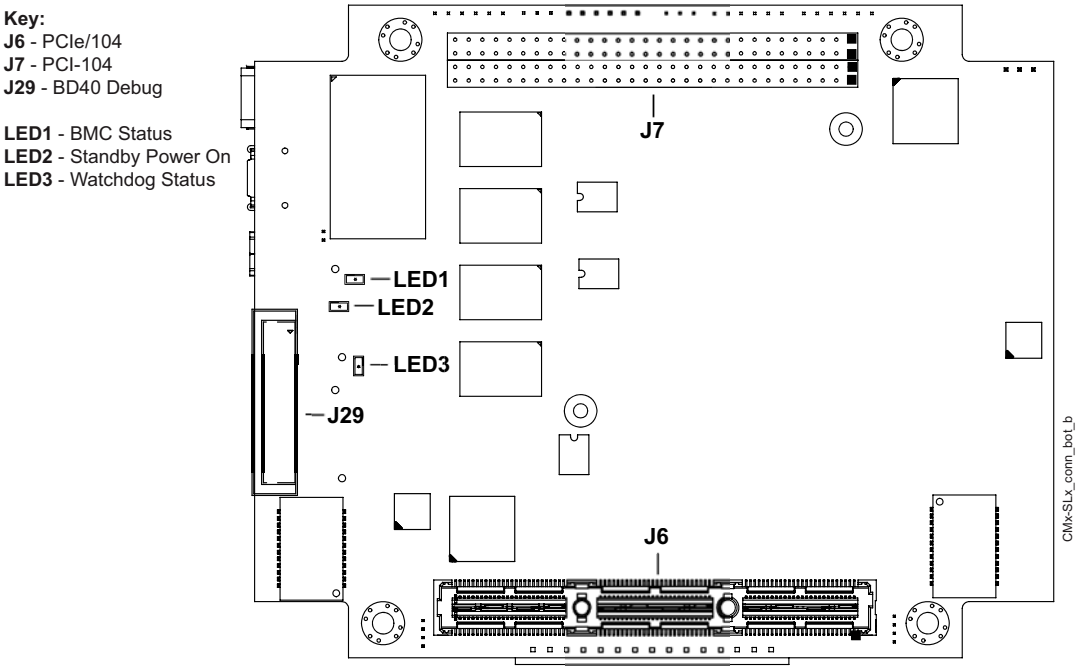


Figure 2-4: Header and Connector Locations (Bottom Side)

NOTE:

Pin 1 is shown as a larger, black square on headers and connectors.

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2.3 Jumper Header Definitions

Table 2-3 describes the jumper headers shown in Figure 2-5. All jumper headers provide 0.079" (2mm) pitch.

Table 2-3: Jumper Settings

Jumper Header	Jumper on Pins 1-2	Jumper on Pins 2-3
J30 – Fan Voltage	Enable +5V (1-2)	Enable +12V (2-3) **(Default)**
JP1 – LVDS Voltage Selection (JIH JVE, 27S1001-OPS35-01G-B)	Enable +3.3V (1-2) **(Default)**	Enable +5V (2-3)
JP2 – PCI-104 Voltage Selection (JIH JVE, 27S1001-OPS35-01G-B)	Enable +3.3V (1-2) **(Default)**	Enable +5V (2-3)

Note: Remove all jumpers to set 18-bit LCD interface.

Key:
J30 - Fan Voltage Select
JP1 - LVDS Voltage Select
JP2 - PCI-104 Voltage Select

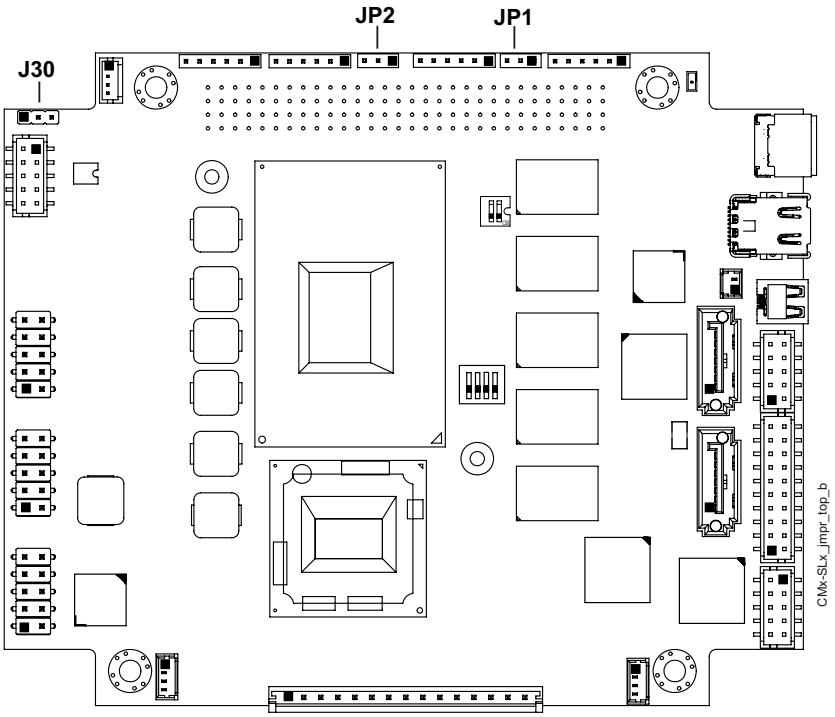


Figure 2-5: Jumper Header Locations (Top Side)

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2.4 Component Features

This section further describes the supported features of the CMx-SLx major, on-board hardware components.

2.4.1 CPU

The CMx-SLx features the 6th Generation Intel® Core™ i3 and Intel® Xeon® E3 processor. The CPU integrates a high-performance 64-bit, x86 Processor Core with Memory Controller and GEN 9 graphics engine. This single chip—based on Intel 64 Architecture and built on 14-nm process technology—provides two execution cores and a Gen 3 Direct Media Interface (DMI) for high-speed connectivity to the Chipset. The CPU also supports Intel Hyper-Threading Technology and up to 16GB of DDR4 SDRAM memory at 1866MHz for high overall performance. Refer to the 6th Generation Intel Processor Data Sheet for H-Platforms on the Intel website for more information.

2.4.4 Chipset

The Intel® CM236 Chipset functions as the IO hub, controlling the DMI and system clock on the CPU and delivering IO interfaces at transfer rates of 8 GT/s. The CM236 supports Gen 3 PCIe connectivity with new technologies such as Intel Rapid Storage Technology 14, Context Sensing SDK, and Platform Trust Technology 3.0. Refer to the CM236 data sheet at the Intel website.

2.4.2 SDRAM

The CMx-SLx employs one 1866/2133MHz memory channel with one rank of eight system memory chips (and one additional chip for ECC). The board provides up to 16GB of extended memory using 16Gb DDR4 SDRAM chips. The CPU features Intel FMA (Fast Memory Access) technology, providing Just-in-Time Scheduling for issuing concurrent requests, Command Overlap for issuing multiple overlapping commands, and Out-of-Order Scheduling to re-order requests made to the same open page.

2.4.5 Gigabit Ethernet PHY Transceiver (I219 - Supporting GLAN1)

The Intel I219 provides a dedicated Physical Layer (PHY) interconnect between the Media Access Controller (MAC) on the Chipset and the first Gb Ethernet interface (GLAN1) on the CMx-SLx. The PHY circuitry provides a standard IEEE 802.3 Ethernet interface for 10BASE-T, 100BASE-TX, and 1000BASE-T applications (802.3, 802.3U, and 802.3ab). The I219 allows for less power consumption during periods of low data activity with the support for the Energy Efficient Ethernet (EEE) 802.az specification. Communication between the I219 and the Chipset occurs through PCIe and SMBus interfaces. The PCIe interface is used for all link speeds when the system is in an active state, and the SMBus interface is used only when the system is in a low power state. For remote, out-of-band system management, the I219 supports Intel Active Management Technology (AMT) 11.0. Refer to the Intel Ethernet Connection I219 data sheet on the Intel web site for more information.

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2.4.6 Gigabit Ethernet Controller (I210 - Supporting GLAN2)

The second Gb Ethernet interface (GLAN2) originates from the Intel I210 Controller, which provides a single-port controller that supports GbE functionality using the high-speed PCIe standard, v2.1 (2.5GT/s). The I210 features a fully-integrated Media Access Control (MAC) and a Physical Layer (PHY), which enable 1000BASE-T implementations such as rack-mounted or pedestal servers in add-on NIC or LAN-on-Motherboard (LOM) designs. Other implementations include blade servers such as LOMs or mezzanine cards as well as embedded applications such as switch add-on cards and network appliances. Additionally, the I210 integrates an SGMII/SerDes port, which allows MAC-to-MAC blade server connections or MAC-to-external PHY connections. Refer to the Intel I210 Ethernet Controller data sheet on the Intel web site.

2.4.7 SSD (Solid State Drive)

The CMx-SLx provides an on-board, 8GB SSD for user storage. The SSD communicates with the Chipset through the SATA 3Gb/s port and is user-accessible through the BIOS Boot menu and the OS interface. For more information, refer to the GLS85LS1008P/GLS85LS1032P SSD data sheet on the Greenliant website.

2.4.3 BMC

The Board Management Controller (BMC) is a micro-controller chip that transmits and receives data to and from the SEMA, BIOS, and debug utilities—monitoring system performance, behavior, and diagnostics at transfer speeds up to 3.33Mbps at 400KHz. The BMC queries components on the board for data related to temperature, power-supply voltage and current, power sequencing, logistics and forensics, flat panel control, I2C bus control, user flash, Watchdog Timer, and fan control. Refer to the Texas Instruments web site for more information on the TM4C123GH6ZRB micro-controller.

2.4.4 LM73 Temperature Sensor

The temperature sensor operates over a wide temperature range (-40°C to +150°C) with a 14-bit mode maximum resolution. Programmed to the BMC and controlled through the SEMA user interface, the temperature sensor monitors system temperatures and issues alerts, time outs, resets, and shutdowns, protecting the system as it approaches temperature limits. For more information on the LM73 Temperature Sensor, refer to the data sheet on the Texas Instruments website.

2.4.5 PTN3460I eDP-to-LVDS Converter

The PTN3460I supports single-bus or dual-bus LVDS signalling with color depths of 18 bits per pixel or 24 bits per pixel and pixel clock frequency up to 112MHz. LVDS data packing can be done either in VESA or JEIDA formats. Also, the DP AUX interface transports I2C-over-AUX commands and supports EDID-DDC communication with an LVDS panel. To support panels without EDID ROM, the PTN3460 can emulate EDID ROM behavior, avoiding specific changes in system video BIOS. Find more details on the NXP website.

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2.4.6 SMBus Slave Addresses

Table 2-8 lists the corresponding slave addresses of the devices on the SMBus.

Table 2-8: SMBus Slave Addresses

Address (HEX)	Function	Device
(50)	BIOS / SEMA	BMC
(92)	Temperature Sensor	LM73
(C0)	eDP-to-LVDS Converter	PTN3460I
(C8)	GbE PHY	I219
APR	PCIe Connector	PCIe Connector

2.5 Standard Connectors

The section describes the industry-standard connectors on the board.

2.5.1 Micro HDMI (J8)

The Micro HDMI connector (J8) provides the standard interface for IO connection to and from an HDMI audiovisual device. Figure 2-6 provides schematic and mechanical presentations of the micro HDMI connector.

CAUTION:
MISE EN GARDE

Make sure the width of the mating connector does not conflict with the width of the mini DisplayPort mating connector.

Assurez-vous que la largeur du connecteur correspondant n'est pas en conflit avec la largeur du connecteur correspondant mini DisplayPort.

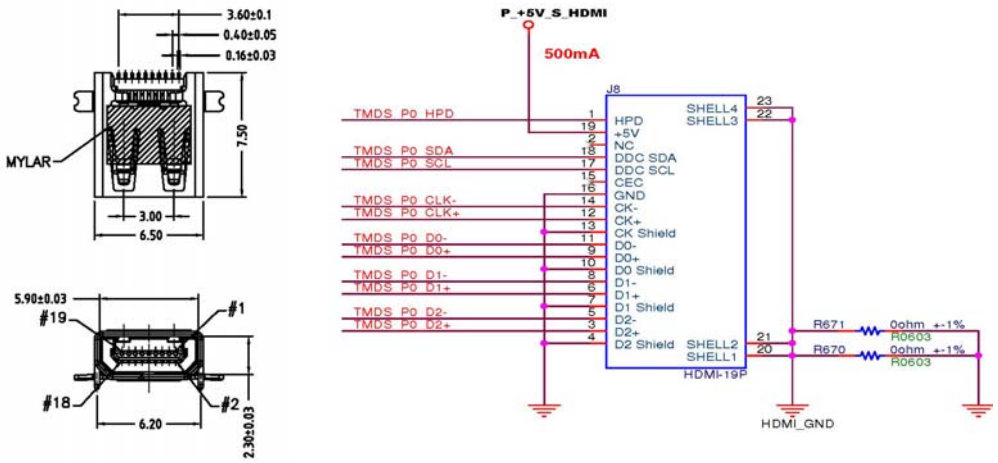


Figure 2-6: Micro HDMI connector

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2.5.2 Mini DisplayPort (J17)

The Mini DisplayPort connector (J17) provides the standard interface to drive IO connection to and from a DisplayPort audiovisual device. Figure 2-7 provides schematic and mechanical presentations of the Mini DisplayPort connector.

CAUTION:
MISE EN GARDE

Make sure the width of the mating connector does not conflict with the widths of the micro HDMI and USB Type-C mating connectors.

Assurez-vous que la largeur du connecteur d'accouplement n'est pas en conflit avec les largeurs des connecteurs d'accouplement micro HDMI et USB Type-C.

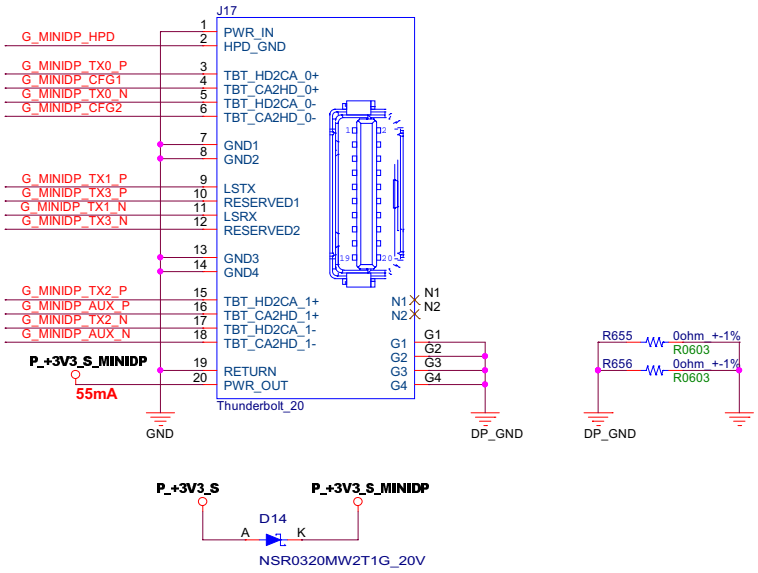


Figure 2-7: Mini DisplayPort connector

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2.5.3 USB Type-C (J28)

The USB Type-C connector (J28) provides a standard USB Type-C interface for super-speed USB 3.1 host and device signals. Figure 2-8 provides schematic and mechanical presentations of the USB Type-C connector.

CAUTION:
MISE EN GARDE

Make sure the width of the mating connector does not conflict with the width of the mini DisplayPort mating connector.

Assurez-vous que la largeur du connecteur correspondant n'est pas en conflit avec la largeur du connecteur correspondant mini DisplayPort.

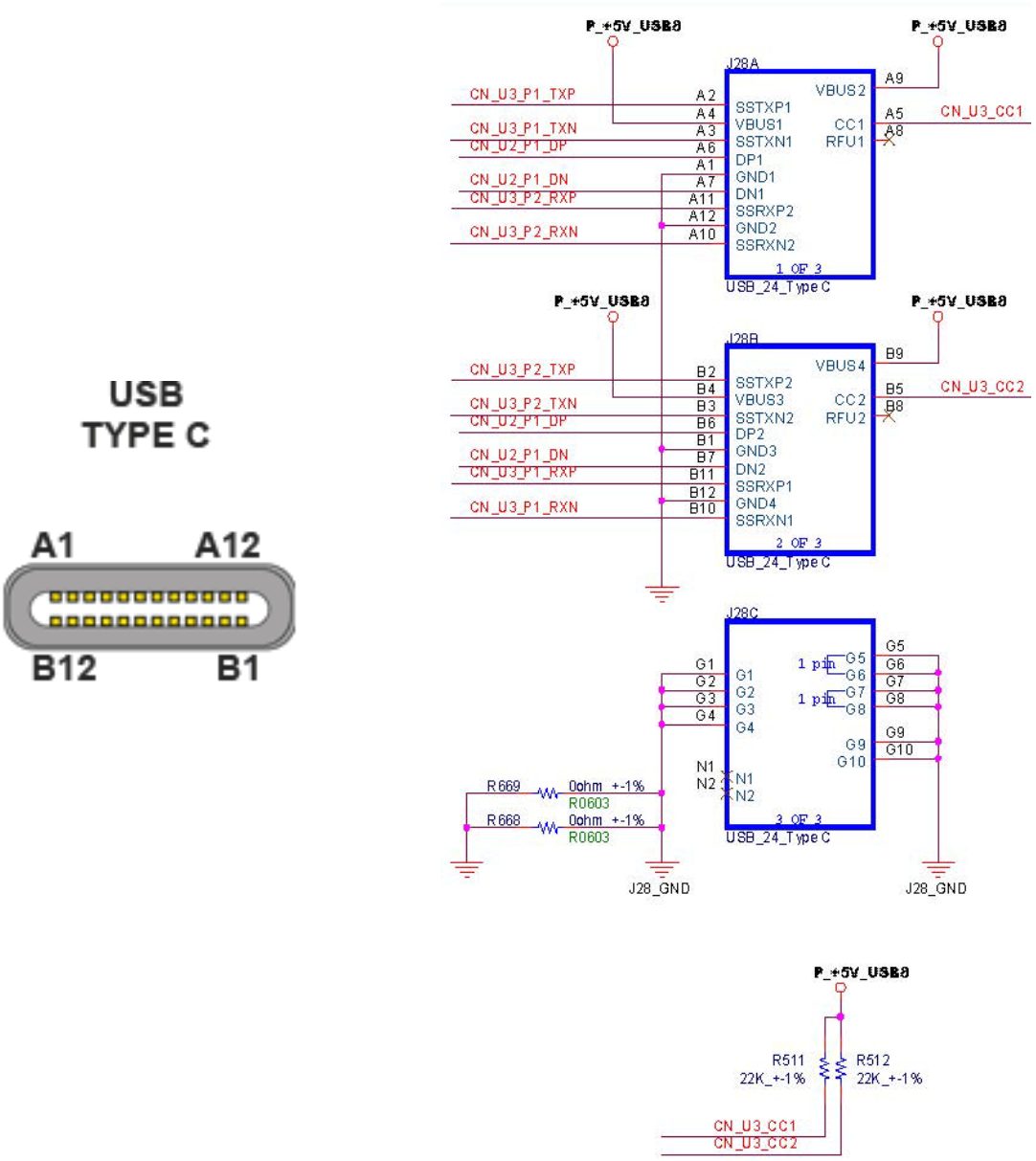


Figure 2-8: USB Type-C connector

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3 Interfaces

This chapter provides descriptions and signal definitions only of the non-standard interfaces on the board. Descriptions and signal definitions of standard interfaces such as PCI-104 and SATA can be found in their respective specification data sheets. If certain signals of standard interfaces have been modified or disconnected, those interfaces will be described in this chapter.



The tables in this chapter define pin sequence using the method in the following example: A 10-pin header with two rows of pins, using odd/even numbering, where pin 2 is directly across from pin 1, is noted as **10 pins, 2 rows, odd/even pin sequence (1, 2)**. Consecutive numbering is noted, for example, as **24 pins, 2 rows, consecutive pin sequence (1, 13)**, where pin 13 is directly across from pin 1. Refer to Figure 2-3 and Figure 2-4 for pin-1 locations.

3.1 Serial Interfaces (H16 and J18)

Table 3-1 provides the signals for serial port 1 interface. Table 3-2 provides the signals for serial port 2 interface. Serial port 1 uses a 10-pin, vertical header with 2 rows, odd/even sequence (1, 2), and 0.100" (2.54mm) pitch. Serial port 2 uses a 10-pin, vertical header with 2 rows, odd/even sequence (1, 2), and 0.079" (2.00mm) pitch.

Table 3-1: Serial Port 1 (COM1) Signals (H16)

Pin #	Signal	DB9 #	Description
1	S1_DSR#	6	COM1 Data Set Ready – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR for overall readiness.
2	S1_DCD#	1	COM1 Data Carrier Detect – Indicates external serial device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input is driven by DTR as part of the DTR/DSR handshake.
3	S1_RTS#	7	COM1 Request To Send – Indicates serial port is ready to transmit data. Used as hardware handshake with CTS for low level flow control.
4	S1_RXD	2	COM1 Receive Data – Serial port receive data input is typically held at a logic 1 (mark) when no data is being transmitted, and is held “Off” for a brief interval after an “On” to “Off” transition on the RTS line to allow the transmission to complete.
5	S1_CTS#	8	COM1 Clear To Send – Indicates external serial device is ready to receive data. Used as hardware handshake with RTS for low level flow control.
6	S1_TXD	3	COM1 Transmit Data – Serial port transmit data output is typically held to a logic 1 when no data is being sent. Typically, a logic 0 (On) must be present on RTS, CTS, DSR, and DTR before data can be transmitted on this line.
7	S1_RI#	9	COM1 Ring Indicator – Indicates external serial device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
8	S1_DTR#	4	COM1 Data Terminal Ready – Indicates serial port is powered, initialized, and ready. Used as hardware handshake with DSR for overall readiness.

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Table 3-1: Serial Port 1 (COM1) Signals (H16) (Continued)

Pin #	Signal	DB9 #	Description
9	COMPORT_RST#		COM1 reset
10	GND	10	COM1 Ground

Note: The shaded table cell denotes ground. The # symbol indicates the signal is Active Low.

Table 3-2: Serial Port 2 (COM2) Signal (J18)

Pin #	Signal	DB9 #	Description
1	GND	10	COM2 Ground
2	GND	5	COM2 Ground
3	S2_DTR#	4	COM2 Data Terminal Ready – Indicates serial port is powered, initialized, and ready. Used as hardware handshake with DSR for overall readiness.
4	S2_RI#	9	COM2 Ring Indicator – Indicates external serial device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
5	S2_TXD	3	COM2 Transmit Data – Serial port transmit data output is typically held to a logic 1 when no data is being sent. Typically, a logic 0 (On) must be present on RTS, CTS, DSR, and DTR before data can be transmitted on this line.
6	S2_CTS#	8	COM2 Clear To Send – Indicates external serial device is ready to receive data. Used as hardware handshake with RTS for low level flow control.
7	S2_RXD	2	COM2 Receive Data – Serial port receive data input is typically held at a logic 1 (mark) when no data is being transmitted, and is held “Off” for a brief interval after an “On” to “Off” transition on the RTS line to allow the transmission to complete.
8	S2_RTS#	7	COM2 Request To Send – Indicates serial port is ready to transmit data. Used as hardware handshake with CTS for low level flow control.
9	S2_DCD#	1	COM2 Data Carrier Detect – Indicates external serial device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input is driven by DTR as part of the DTR/DSR handshake.
10	S2_DSR#	6	COM2 Data Set Ready – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR for overall readiness.

Note: The shaded table cells denote ground. The # symbol indicates the signal is Active Low.

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3.2 USB 2.0 Interface (H15 and J25)

The CMx-SLx contains two root USB hubs and six functional USB ports. Four of the six USB ports are routed through two 10-pin headers (H15 and J25), and the other two ports are routed through the PCIe/104 interface connector. The PCH provides the USB function including the following features:

- Supports USB v.2.0 EHCI and USB v.1.1 UHCI
- Provides over-current detection status
- Provides a fuse on board for over-current protection



The standard USB 3.1 host interface is described in the USB Type-C (J28) section of Chapter 2.

Table 3-3 describes the pin signals of the USB0 and USB1 header which consists of 10 pins, in two rows, with odd/even (1, 2) pin sequence, and 0.100" (2.54mm) pitch.

Table 3-3: USB0 and USB1 Interface Pin Signals (H15)

Pin #	Signal	Description
1	USB-PWR_1	USB1 Power – VCC (+5V +/-5%) power goes to the port through an on-board fuse. Port is disabled if this input is low.
2	USB-PWR_0	USB0 Power – VCC (+5V +/-5%) power goes to the port through an on-board fuse. Port is disabled if this input is low.
3	CONN_USB1_N	USB1 Port Data Negative
4	CONN_USB0_N	USB0 Port Data Negative
5	CONN_USB1_P	USB1 Port Data Positive
6	CONN_USB0_P	USB0 Port Data Positive
7	USB_GND1	USB1 Ground
8	USB_GND0	USB0 Ground
9	USB_GND1	USB1 Ground
10	USB_GND0	USB0 Ground

Note: The shaded table cells denote power or ground.

Table 3-4 describes the pin signals of the USB2 and USB3 header, which consists of 10 pins in two rows, with odd/even (1, 2) pin sequence, and 0.079" (2mm) pitch.

Table 3-4: USB2 and USB3 Interface Pin Signals (J25)

Pin #	Signal	Description
1	USB_GND2	USB2 Ground
2	USB_GND3	USB3 Ground
3	USB_GND2	USB2 Ground
4	USB_GND3	USB3 Ground
5	CONN_USB2_P	USB2 Port Data Positive
6	CONN_USB3_P	USB3 Port Data Positive
7	CONN_USB2_N	USB2 Port Data Negative
8	CONN_USB3_N	USB3 Port Data Negative
9	USB-PWR_2	USB2 Power – VCC (+5V +/-5%) power goes to the port through an on-board fuse. Port is disabled if this input is low.
10	USB-PWR_3	USB3 Power – VCC (+5V +/-5%) power goes to the port through an on-board fuse. Port is disabled if this input is low.

Note: The shaded table cells denote power or ground.

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3.3 Ethernet (H11 and J14)

The CMx-SLx supports two Gigabit Ethernet interfaces. The first Ethernet interface originates from the WGI219LM PHY transceiver, which occupies one PCI Express lane and supports the internal MAC (Media Access Controller) in the PCH. The second Ethernet interface is implemented through the WGI210AT Ethernet controller, which occupies one PCI Express lane and generates its own Gigabit Ethernet signals. The Ethernet function supports multi-speed operation at 10/100/1000 Mbps and operates in full-duplex at all supported speeds or half duplex at 10/100 Mbps while adhering to the IEEE 802.3x flow control specification. The Ethernet interface offers the following features:

- Full duplex support at 10 Mbps, 100 Mbps, or 1000 Mbps
- Half duplex support at 10 Mbps and 100 Mbps
- In full duplex mode, the Ethernet controller adheres to the IEEE 802.3x Flow Control specification
- In half duplex mode, performance is enhanced by a proprietary collision reduction mechanism
- IEEE 802.3 compatible physical layer to wire transformer
- IEEE 802.3u Auto-Negotiation support
- Fast back-to-back transmission support with minimum interframe spacing (IFS)
- IEEE 802.3x auto-negotiation support for speed and duplex operation
- On-board magnetics (Ethernet isolation transformers)
- Intel Active Management Technology (AMT) 11.0 support

Table 3-5 describes the pin signals of the Ethernet GLAN1 interface, which consists of a two-row, 10-pin vertical header with odd/even (1,2) pin sequence, and 0.100" (2.54mm) pitch.

Table 3-5: GLAN1 Interface Signal Descriptions (H11)

Pin #	Signal	Description
1	MDI1-	Media Dependent Interface 1 +/-
2	MDI1+	
3	MDI2-	Media Dependent Interface 2 +/-
4	MDI2+	
5	MDI0-	Media Dependent Interface 0 +/-
6	MDI0+	
7	MDI3-	Media Dependent Interface 3 +/-
8	MDI3+	
9	GND	Ground
10	GND	

Note: The shaded table cells denote ground. The magnetics (isolation transformer, TF3) for the Ethernet connector is included on the CMx-SLx.

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Table 3-6 describes the pin signals of the Ethernet GLAN2 interface, which consists of a two-row, 10-pin vertical header with odd/even (1,2) pin sequence, and 0.079" (2mm) pitch.

Table 3-6: GLAN2 Interface Signal Descriptions (J14)

Pin #	Signal	Description
1	GND	Ground
2	GND	
3	MDI3+	Media Dependent Interface 3 +/-
4	MDI3-	
5	MDI0+	Media Dependent Interface 0 +/-
6	MDI0-	
7	MDI2+	Media Dependent Interface 2 +/-
8	MDI2-	
9	MDI1+	Media Dependent Interface 1 +/-
10	MDI1-	

Note: The shaded table cells denote ground. The magnetics (isolation transformer, TF2) for the Ethernet connector is included on the CMx-SLx.

3.4 Video (J8 [Micro HDMI], J17 [Mini DisplayPort], and J23 [LVDS])

The Core i3-6102E CPU provides an integrated 2D/3D graphics engine, which supports video decode such as MPEG2, VC-1, and AVC/H.264 (main, baseline at L3 and High-profile level 4.0/4.1) as well as video encode such as MPEG2, AVC/H.264 (baseline at L3), and VGA. The CPU supports LVDS, DisplayPort, and HDMI display ports, permitting simultaneous, independent operation of two displays. The CPU provides PCIe x16 Graphics signals to the PCIe/104 connector for an external high-performance PCI Express Graphics card or other general purpose PCI Express devices. The video interface features are listed in the following bullets. Refer to Table 3-7 for the LVDS signal definitions. The HDMI and DisplayPort interfaces are standard connectors, and those signals are defined in Chapter 2. The PEG signals are part of the standard PCIe/104 interface and are not defined in this manual.

Mini DisplayPort:

- Supports resolutions of up to 4096x2304 @ 60 Hz
- Provides Main, Auxiliary, and Hot-Plug Detect signals
- Supports DisplayPort 1.2 specification
- Supports two DisplayPort interfaces

LVDS:

- Supports a maximum resolution of 1400x1050 at 60Hz (pixel clock rate up to 112MHz)
- Supports minimum pixel clock rate of 25MHz
- Supports a single channel interface through a 20-pin header
- Supports pixel color depths of 18 and 24 bits

Micro HDMI:

- Supports resolutions up to 3840x2160 pixels at 30Hz
- Supports pixel clock rates from 25MHz to 340MHz
- Supports DVD-Audio and Audio Return channel
- Provides one 19-pin, standard HDMI micro connector

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PEG (PCI Express Graphics):

- Supports external high-performance PCI Express graphics cards
- Supports general-purpose PCI Express devices
- Supports theoretical bandwidth of up to 8GT/s
- Provides PCIe Gen3 compliance

Table 3-7 lists the pin signals of the LVDS video header, which provides 20 pins, 2 rows, odd/even pin sequence (1, 2) with 0.079" (2mm) pitch.

Table 3-7: LVDS Video Interface Pin Signals (J23)

Pin #	Signal	Description
1	+12V_ATX	+12 volts for flat panel and backlight
2	VCC_LVDS_CONN	JP3 determines LVDS voltage (+3.3V or +5V)
3	GND	Ground
4	GND	Ground
5	LVDSA_CLK_P	LVDS A Clock Positive
6	LVDSA_CLK_N	LVDS A Clock Negative
7	LVDSA_DAT3_P	LVDS A DATA Positive Line 3
8	LVDSA_DAT3_N	LVDS A DATA Negative Line 3
9	LVDSA_DAT2_P	LVDS A DATA Positive Line 2
10	LVDSA_DAT2_N	LVDS A DATA Negative Line 2
11	LVDSA_DAT1_P	LVDS A DATA Positive Line 1
12	LVDSA_DAT1_N	LVDS A DATA Negative Line 1
13	LVDSA_DAT0_P	LVDS A DATA Positive Line 0
14	LVDSA_DAT0_N	LVDS A DATA Negative Line 0
15	LBKLT_CTL	Panel Backlight Control
16	LVDD_EN	Enable Panel Power
17	LDDC_CLK	Display Data Channel Clock
18	LDDC_DATA	Display Data Channel Data
19	LBKLT_EN	Enable Backlight Inverter
20	NC	Not Connected

Note: The shaded table cells denote power or ground.

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3.5 Power Interface (J24)

The CMx-SLx requires one +5 volt DC power source and provides a shrouded, 15-pin single-row, vertical header with 0.100" (2.54mm) pitch. If the +5VDC power drops below ~4.65V, a low voltage reset is triggered, resetting the system.

The power input header (J24) supplies the following voltage and ground directly to the module:

- 5.0VDC +/- 5%



-5V is not supported on the PCIe/104 connector.

The voltages +5V, +12V, and -12V are not generated by the onboard power supply but routed from the power supply connector. The maximum current is limited to 1.0A for each voltage.

If the CMx-SLx is supplied with only +5V, +12V will not be available, and devices that require +12V must be separately powered. PCI or PCIe devices on the PC/104 stack may not properly function with only +5V supplied to the CMx-SLx. Also, the system fan speed will decrease with only +5V supplied to the CMx-SLx.

Table 3-8: Power Interface Pin Signals (J24)

Pin	Signal	Descriptions
1	+5V_ATX	+5 Volts
2	GND	Ground
3	+5V_ATX	+5 Volts
4	GND	Ground
5	+5V_ATX	+5 Volts
6	+5V_ATX	+5 Volts
7	+5V_ATX_SBY	+5 Volts Standby
8	GND	Ground
9	ATX_PSON#	Power Supply On (turns on and off the power supply)
10	ATX_PWRGD	ATX Power Good (notifies the CPU that the voltage is in required range)
11	+3V3_ATX	+3.3 Volts (routed to PCI-104)
12	GND	Ground
13	+12V	+12 Volts (routed to PCIe/104, PCI-104, LVDS, and Fan interfaces)
14	GND	Ground
15	12V	12 Volts (routed to PCIe/104 and PCI-104 interfaces)

Note: The shaded table cells denote power or ground. The # symbol indicates the signal is Active Low.

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3.6 User GPIO Interface (J26 and J27)

The CMx-SLx provides GPIO pins for customer use, routing the signals from the BMC to the J26 and J27 headers. Example test applications and source codes are available on request.

For more information about the GPIO pin operation, refer to the BMC TM4C123BH6ZRBT7 data sheet at the Texas Instruments website.

Table 3-9 describes the pin signals of the GPIO1 interface, which provides a 6-pin, single-row header with 0.079" (2mm) pitch.

Table 3-9: User GPIO1 Interface Pin Signal Descriptions (J26)

Pin #	Signal	BMC Pin	Description
1	BMC_GPIO1	PJ0	User defined
2	BMC_GPIO2	PJ1	User defined
3	BMC_GPIO3	PJ2	User defined
4	BMC_GPIO4	PJ3	User defined
5	GND	N/A	Ground
6	GND	N/A	Ground

Note: The shaded table cells denote ground. All GPIO pins are in the Core Power Well of the PCH.

Table 3-10 describes the pin signals of the GPIO2 interface, which provides a 6-pin, single-row header with 0.079" (2mm) pitch.

Table 3-10: User GPIO2 Interface Pin Signal Descriptions (J27)

Pin #	Signal	BMC Pin	Description
1	BMC_GPIO5	PG6	User defined
2	BMC_GPIO6	PG7	User defined
3	BMC_GPIO7	PA0	User defined
4	BMC_GPIO8	PA1	User defined
5	GND	N/A	Ground
6	GND	N/A	Ground

Note: The shaded table cells denote ground. All GPIO pins are in the Core Power Well of the PCH.

3.7 I2C / SMBus Interface (J31)

Table 3-11 describes the pin signals of the I2C / SMBus interface, which provides a 6-pin, single-row header with 0.079" (2mm) pitch.

Table 3-11: I2C / SMBus Interface Pin Signal Descriptions (J31)

Pin #	Signal	Description
1	SMB_CLK	SMBus Clock (PCH)
2	SMB_DAT	SMBus Data (PCH)
3	GND	Ground
4	I2C_CLK	I2C Clock (PCH)
5	I2C_DAT	I2C Data (PCH)
6	GND	Ground

Note: The shaded table cells denote ground.

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3.8 Utility Interface (J21)

The Utility interface provides three I/O signals on the module and consists of a 6-pin, 0.079" (2mm), single-row header (J21). The CPU drives the Power Button and Speaker signals on the Utility interface. A separate Power Management microprocessor drives the Reset Switch signal. Table 3-12 provides the signal definitions.

- Power Button
- Reset Switch
- Speaker

3.8.1 Power Button

The Utility header provides a signal for an external Power Button through pins 1 and 2. The Power Button allows the user to shut down and power on the system. To shut down the system, press and hold the Power Button for four seconds. Press the Power Button for one second to power on the system.

3.8.2 Reset Switch

Pins 2 and 3 on the Utility header provide the signals for an external reset button, which allows the user to re-boot the system.

3.8.3 Speaker

The speaker signal provides sufficient signal strength to drive an external 1W 8 Ω "Beep" speaker at an audible level through pins 4 and 5 on the Utility header. The speaker signal is driven from an on-board amplifier and the CPU.

Table 3-12 describes the pin signals of the Utility interface, which provides a 5-pin, single-row header with 0.079" (2.00mm) pitch.

Table 3-12: Utility Interface Pin Signals (J21)

Pin #	Signal	Description
1	PWR_BTN#	External Power Button (Pins 1-2)
2	GND	Ground
3	RESET SW#	External Reset Switch signal (Pins 2-3)
4	5V	+5 Volts Power
5	SPKR_CONN	Speaker Output (Pins 4-5)
6	GND	Ground

Note: The shaded table cells denote power or ground. The # symbol indicates the signal is Active Low.

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3.9 System Fan (J22)

Table 3-13 lists the pin signals of the System Fan header, which provides a single row of 4 pins with 0.049" (1.25mm) pitch.

Table 3-13: System Fan Pin Signals (J22)

Pin #	Signal	Description
1	PWM_FAN_OUT	Fan power management
2	PWM_TACH_IN	Tachometer power management
3	GND	Ground
4	+V_FAN	+5.0 / +12 Volts DC +/- 5% (default is +12V - use J30 to select +5.0V)

Notes: Use the J30 fan voltage jumper header to select pin-4 voltage. The shaded table cells denote power or ground.



MISE EN GARDE

ADLINK recommends to use only a 2-wire fan, connected to pins 3-4, when implementing a 5V power supply. Use the J30 jumper header to change voltage setting to +5V.

ADLINK recommande d'utiliser uniquement un ventilateur à 2 fils, connecté aux broches 3-4, lors de la mise en œuvre d'une alimentation 5V. Utilisez l'en-tête du cavalier J30 pour changer le réglage de tension à + 5V.

3.10 Battery (J12)

Table 3-14 lists the pin signals of the External Battery Input header for backup RTC (Real Time Clock), which provides 2 pins with 0.049" (1.25mm) pitch.

Table 3-14: External Battery Input Header (J12)

Pin #	Signal	Description
1	+VBAT	+3.0 volts DC
2	GND	Ground

Note: The shaded table cells denote power or ground. The RTC has an expected current draw of 6μA at room temperature, with +3.0V. The battery is used only when power is not applied to the board.

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3.11 External LEDs - Ethernet (J2 and J3)

These two headers provide signals for two external LEDs that indicate Ethernet links and activity. Refer to the following two tables for signal definitions.

Table 3-15 defines the signals for the GLAN1 LED header that indicates Ethernet links and activity using a single row of 4 pins with 0.049" (1.25mm) pitch.

Table 3-15: GLAN1 External LED Signals (J2)

Pin #	Signal	Description
1	V3.3_CONN	+3.3 volts – Provides +3.3 volts to external LED (Pins 1-2 for Green LED)
2	GBE1_ACT_LED	Ethernet Activity
3	GBE1_LINK1000_LED	Gigabit Ethernet Link
4	GBE1_LINK100_LED	Fast Ethernet Link with +3.3 volts power (Pins 3-4 for Bi-Color LED)

Note: The shaded table cell denotes power. Configure Ethernet LEDs for Active Low operation.

Table 3-16 defines the signals for the GLAN2 LED header that indicates Ethernet links and activity using a single row of 4 pins with 0.049" (1.25mm) pitch.

Table 3-16: GLAN2 External LED Pin Signals (J3)

Pin #	Signal	Description
1	V3.3_CONN	+3.3 volts – Provides +3.3 volts to external LED (Pins 1-2 for Green LED)
2	GBE2_ACT_LED	Ethernet Activity
3	GBE2_LINK1000_LED	Gigabit Ethernet Link
4	GBE2_LINK100_LED	Fast Ethernet Link with +3.3 volts power (Pins 3-4 for Bi-Color LED)

Note: The shaded table cell denotes power. Configure Ethernet LEDs for Active Low operation.

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4 Utilities

This chapter provides information on how to read information from and configure the BIOS Setup utility, the SEMA utility, the Watchdog Timer utility, and the board temperature sensors on the CMx-SLx.

4.1 BIOS Setup

The CMx-SLx features an AMI BIOS. The default settings provide a “ready to run” system, even without a BIOS setup backup battery.

The BIOS is located in flash memory and can be easily updated with software under DOS.

All setup changes of the BIOS are stored in the CMOS RAM.

The soldered battery will provide power to store that information for over two years without board activation.

4.1.1 Menu Structure

This section presents the six primary menus of the BIOS Setup Utility. Use the following table as a quick reference for the contents of the BIOS Setup Utility. The subsections in this section describe the submenus and setting options for each menu item. The default setting options are presented in **bold**, and the function of each setting is described in the right hand column of the respective table.

Table 4-1: BIOS Setup Menu Overview

Main	Advanced	Security	Boot	Save & Exit
• BIOS Information • Processor Information • PCH Information • System ► Management • System Date • System Time	• CPU ► • Memory ► • Graphics ► • SATA ► • USB ► • Network ► • PCI and PCIe ► • Super IO► • ACPI and ► Power Management • Serial Port ► Console • ICC ► • Thermal ► • Miscellaneous ►	• Password ► Description • Secure Boot Menu►	• Boot Configuration► • CSM Configuration►	• Reset Options► • Save Options►

Note:
► indicates the item contains submenus

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4.1.2 Starting the BIOS Setup Utility

Use the following bullets to initiate start-up activity for the BIOS Setup Utility.

- Press <DEL> during power up to start the BIOS setup utility.
- Press <F11> during power up to start the Boot menu.
- Press <END> during power up to return BIOS settings to default.

4.1.3 Main Menu

The Main Menu provides read-only information about your system and also allows you to set the System Date and Time. Refer to the tables below for details of the submenus and settings.

Main > BIOS Information

Table 4-2: Main Menu > BIOS Information

Feature	Options	Description
BIOS Vendor	Info only	BIOS Vendor
Core Version	Info only	.Kernal code version
Compliancy	Info only	UEFI code support
Project version	Info only	ADLINK BIOS version
Build Date and Time	Info only	ADLINK date the BIOS was build
Access Level	Info only	Access Level

Main > Processor Information

Table 4-3: Main Menu > Processor Information

Feature	Options	Description
CPU Brand String	Info only	Display CPU Brand Name
Frequency	Info only	Display CPU Frequency
Processor ID	Info only	Display CPU ID
Stepping	Info only	Display CPU Stepping
Number of Processors	Info only	Display number of Processors
Microcode Revision	Info only	Display Microcode Revision
GT Info	Info only	Display GT info of Intel Graphics
IGFX VBIOS Version	Info only	Display VBIOS Version
Total Memory	Info only	Display installed memory size
Memory Frequency	Info only	Display Memory Frequency

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Main > PCH Information

Table 4-4: Main Menu > PCH Information

Feature	Options	Description
PCH Name	Info only	Display PCH name
PCH SKU	Info only	Display PCH SKU
Stepping	Info only	Display PCH stepping
LAN PHY Revision	Info only	Displays LAN PHY Revision
ME FW Version	Info only	Display version of ME
ME Firmware SKU	Info only	Display ME Firmware Kit SKU number
System Management ►	Submenu	

Main > PCH Information > System Management

Table 4-5: Main Menu > PCH Information > System Management

Feature	Options	Description
System Management	Info only	
Version	Info only	Display version.

Main > PCH Information > System Management > Board Information

Table 4-6: Main Menu > PCH Information > System Management > Board Information

Board Information	Info only	Description
SEMA Firmware	Read only	Display SMC Firmware.
Build Date	Read only	Display SMC firmware build date.
SEMA Boot loader	Read only	Display SMC boot loader.
Build Date	Read only	Display SMC boot loader build date.
Hardware Version	Read only	Display SMC hardware Version.
Serial Number	Read only	Display SMC serial Number.
Manufacturing Date	Read only	Display SMC manufacturing date.
Last Repair Date	Read only	Display SMC last repair date.
MAC ID	Read only	Display SMC MAC ID

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Main > PCH Information > System Management > Temperatures and Fan Speed

Table 4-7: Main Menu > PCH Information > System Management > Temperatures and Fan Speed

Feature	Options	Description
Temperatures and Fan	Info only	
CPU Temperature	Info only	
Current	Read only	Display CPU current temperature.
Startup	Read only	Display CPU startup temperature.
Min	Read only	Display CPU min temperature.
Max	Read only	Display CPU max temperature.
Board Temperatures	Info only	
Current	Read only	Display board current temperature.
Startup	Read only	Display board startup temperature.
Min	Read only	Display board min temperature.
Max	Read only	Display board max temperature.
CPU Fan Speed	Read only	Display CPU fan speed.

Main > PCH Information > System Management > Power Consumption

Table 4-8: Main Menu > PCH Information > System Management > Power Consumption

Feature	Options	Description
Power Consumption	Info only	
Current Input Current	Read only	Display input current.
Current Input Power	Read only	Display input power.
VCC_CORE	Read only	Display actual voltage of the VCC_CORE.
VCC_GT	Read only	Display actual voltage of the VCC_GT.
VCCSA	Read only	Display actual voltage of the VCCSA
0V95_VCCIO	Read only	Display actual voltage of the 0V95_VCCIO.
VDDQ	Read only	Display actual voltage of the VDDQ
1V0_A	Read only	Display actual voltage of the 1V0_A
1V0_VCCSTG	Read only	Display actual voltage of the 1V0_VCCSTG
V12_V	Read only	Display actual voltage of the V12_V
V5_ATX	Read only	Display actual voltage of the V5_ATX
V5VSB	Read only	Display actual voltage of the V5VSB
VRTC	Read only	Display actual voltage of the VRTC
V3P3A	Read only	Display actual voltage of the V3P3A
V3P3S	Read only	Display actual voltage of the V3P3S

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Main > PCH Information > System Management > Runtime Statistics

Table 4-9: Main Menu > PCH Information > System Management > Runtime Statistics

Feature	Options	Description
Runtime Statistics	Info only	
Total Runtime	Read only	The returned value specifies the total time in minutes the system is running in S0 state.
Current Runtime	Read only	The returned value specifies the time in seconds the system is running in S0 state. This counter is cleared when the system is removed from the external power supply.
Power Cycles	Read only	The returned value specifies the number of times the external power supply has been shut down
Boot Cycles	Read only	The Bootcounter is increased after a HW- or SW-Reset or after a successful power-up.
Boot Reason	Read only	The boot reason is the event which causes the reboot of the system.

Main > PCH Information > System Management > Flags

Table 4-10: Main Menu > PCH Information > System Management > Flags

Feature	Options	Description
Flags	Info only	
BMC Flags	Read only	
BIOS Select	Read only	Display the selection of current BIOS ROM.
ATX/AT-Mode	Read only	Display ATX/AT-Mode.
Exception Code	Read only	System exception reason.

Main > PCH Information > System Management > Power Up

Table 4-11: Main Menu > PCH Information > System Management > Power Up

Feature	Options	Description
Power Up	Info only	
Power Up watchdog Attention: F12 disables the Power Up Watchdog.	Enabled **Disabled**	The Power-Up Watchdog resets the system after a certain amount of time after power-up.
ECO Mode	**Disabled** Enable	Reduces the power consumption of the system.
BMC I2C Mode	**100Kbps** 400Kbps	BMC I2C Mode
Power-up Mode Attention: The Power-Up Mode only has effect, if the module is in ATX-Mode.	Turn on **Remain off** Last State	Turn On: The machine starts automatically when the power supply is turned on. Remain Off: To start the machine the power button has to be pressed. Last State: when powered on during a power failure the system will automatically power on when power is restored

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Main > PCH Information > System Management > LVDS Backlight

Table 4-12: Main Menu > PCH Information > System Management > LVDS Backlight

Feature	Options	Description
LVDS Backlight	Info only	
LVDS Backlight Bright	255	The value range starts at 0 and ends at 255 (0 = black [no backlight]; 255 = maximum brightness.)

Main > PCH Information > System Management > Smart Fan

Table 4-13: Main Menu > PCH Information > System Management > Smart Fan

Feature	Options	Description
Smart Fan	Info only	
CPU Smart Fan Temperature Source	**CPU Sensor** System Sensor	Select CPU smart fan source.
CPU Fan Mode	**AUTO (Smart Fan)** Fan Off Fan On	Select CPU Fan Mode.
CPU Trigger Point 1	Read only	
Trigger Temperature	15	Specifies the temperature threshold at which the BMC turns on CPU fan with specific PWM level. User can set the desired trigger threshold.
PWM Level	30	Select PWM level.
CPU Trigger Point 2	Read only	
Trigger Temperature	60	Specifies the temperature threshold at which the BMC turns on CPU fan with specific PWM level. User can set the desired trigger threshold.
PWM Level	40	Select PWM level.
CPU Trigger Point 3	Read only	
Trigger Temperature	70	Specifies the temperature threshold at which the BMC turns on CPU fan with specific PWM level. User can set the desired trigger threshold.
PWM Level	63	Select PWM level.
CPU Trigger Point 4	Read only	
Trigger Temperature	80	Specifies the temperature threshold at which the BMC turns on CPU fan with specific PWM level. User can set the desired trigger threshold.
PWM Level	100	Select PWM level.

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Main > System Date and Time

Table 4-14: Main Menu > System Date and Time

Feature	Options	Description
System Date	Weekday, MM/DD/YYYY	Requires the alpha-numeric entry of the day of the week, day of the month, calendar month, and all 4 digits of the year, indicating the century and year (Fri XX/XX/20XX)
System Time	HH/MM/SS	Presented as a 24-hour clock setting in hours, minutes, and seconds

4.1.4 Advanced Menu

This menu contains the settings for most of the user interfaces in the system.

Advanced > CPU

Table 4-15: Advanced Menu > CPU

Feature	Options	Description
CPU	Info only	Manufacturer, model, speed
CPU Signature	Info only	Display CPU Signature.
Microcode Revision	Info only	Display Microcode Patch.
Max CPU speed	Info only	Display Max CPU speed.
Min CPU speed	Info only	Display Min CPU speed.
CPU Speed	Info only	Display CPU Speed.
Processor Cores	Info only	Display Processor Cores.
Hyper Threading Technology	Info only	Display Hyper Threading Technology support or not.
Intel VT-x Technology	Info only	Display Intel VT-x Technology support or not.
Intel SMX Technology	Info only	Display Intel SMX Technology support or not.
64 bit	Info only	Display 64 bit support or not
EIST Technology	Info only	Display EIST Technology support or not
CPU C3 state	Info only	Display CPU C3 state support or not
CPU C6 state	Info only	Display CPU C6 state support or not
CPU C7 state	Info only	Display CPU C7 state support or not
L1 Data Cache	Info only	Display cache info.
L1 Code Cache	Info only	Display cache info.
L2 Cache	Info only	Display cache info.
L3 Cache	Info only	Display cache info.
L4 Cache	Info only	Display cache info.

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Table 4-15: Advanced Menu > CPU (Continued)

Feature	Options	Description
CPU Flex Ratio Override	**Disabled** Enabled	Enable/Disable CPU Flex Ratio Programming. If you want to enable this function, you must disable Turbo Mode. NOTE: If this setting is Enabled, the Custom Configurable TDP setting will be automatically hidden because these two settings will cause a system conflict if they are both enabled.
CPU Flex Ratio Settings	20	Non Turbo Range: 8 - 20. Turbo ratio: 21. If out of ratio range, maximum or minimum ratio is used. This sets the maximum ratio.
Hyper-threading	Disabled **Enabled**	Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled only one thread per enabled core is enabled.
VT-d	Disabled **Enabled**	Check to enable VT-d function on MCH.
Active Processor Cores	**ALL** 1 2 3	Number of cores to enable in each processor package.
Intel (VMX) Virtualization Technology	Disabled **Enabled**	Enable/Disable support for the Intel virtualization technology.
Intel(R) SpeedStep(TM)	Disabled **Enabled**	Allows more than two frequency ranges to be supported.
Intel(R) Speed Shift Technology	Disabled **Enabled**	Enable/Disable Intel(R) Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states."
Turbo Mode	Disabled **Enabled**	Enable/Disable turbo mode.
Configurable TDP Boot Mode	**TDP Nominal** TDP Down Disabled	Configure TDP Mode as Nominal/Down/Disabled. Disabled option will set MSR to Nominal and MMIO to Zero.
Config TDP Lock	**Disabled** Enabled	Configurable TDP Mode Lock sets the Lock bits on TURBO_ACTIVATION_RATIO and CONFIG_TDP _CONTROL. Note: When CTDP Lock is enabled Custom ConfigTDP Count will be forced to 1 and Custom ConfigTDP Boot Index will be forced to 0.
Custom Configurable TDP	**Disable** Enabled	Custom Configurable TDP setting. NOTE: If this setting is Enabled, the CPU Flex Ratio Override setting will be automatically hidden because these two settings will cause a system conflict if they are both enabled.

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Table 4-15: Advanced Menu > CPU (Continued)

Feature	Options	Description
Power Limit 1	10W 12W 15W 17W 20W 25W 30W **35W** 40W 20W 25W 30W 35W 40W	XE SKU: Any value can be programmed. Overclocking SKU: Value must be between Max and Min Power Limits (specified by PACKAGE_POWER_SKU_MSR). Other SKUs: This value must be between Min Power Limit and TDP Limit.
Power Limit 1 Time Window	**0** 1 2 3 4 5 6 7 8 10 12 14 16 20 24 28 32 40 48 56 64 80 96 112	Platform Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0 = default values. Indicates the time window over which Platform TDP value should be maintained.
CPU C state	Disabled **Enabled**	Enable or disable CPU C states
C-State Auto Demotion	Disabled C1 C3 **C1 and C3**	Configure C-State Auto Demotion

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Table 4-15: Advanced Menu > CPU (Continued)

Feature	Options	Description
Package C State limit	**Auto** CPU Default C10 C9 C8 C7S C7 C6 C3 C2 C0/C1	Package C State limit
Intel TXT(LT) support	**Disabled** Enabled	Enables or Disables Intel(R) TXT(LT) support.
CPU DTS	Disabled **Enabled**	Disabled: ACPI thermal management uses EC reported temperature values. Enabled: ACPI thermal management uses DTS SMM mechanism to obtain CPU temperature values. Out of Spec: ACPI Thermal Management uses EC reported temperature values and DTS SMM is used to handle Out of Spec condition.
ACPI T-states	**Disabled** Enabled	Enable/Disable ACPI T-States.

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Advanced > Memory

Table 4-16: Advanced Menu > Memory

Feature	Options	Description
Memory RC Version	Info only	Display Memory Reference Code Version
Memory Frequency	Info only	Display Memory Frequency
Total Memory	Info only	Display Total Memory
VDD	Info only	Display Memory Voltage
DIMM#0/1	Info only	Display DIMM#0/1
Memory Timings	Info only	Display Memory Timings
XMP Profile 1	Info only	Display XMP Profile 1 support or not
XMP Profile 2	Info only	Display XMP Profile 2 support or not
Maximum Memory Frequency	**Auto** 1067 1200 1333 1400 1600 1800 1867 2000 2133 2200 2400 2600 2800 2933 3000 3200	Maximun Memory Frequency Selections in MHz
Max TOLUD	**Dynamic** 1G 1.25G 1.5G 1.75G 2G 2.25G 2.5G 2.75G 3G 3.25G 3.5G	Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.

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Advanced > Graphics

Table 4-17: Advanced Menu > Graphics

Feature	Options	Description
Graphics Configuration	Info only	
Primary Display	**Auto** IGFX PCIE	Select which of IGFX//PCIE Graphics device should be Primary Display..
Primary PEG	**Auto** PEG1 PEG2	Select PEG0/PEG1/PEG2/PEG3 Graphics device should be Primary PEG.
Primary PCIE	**Auto** PCIE1 PCIE2 PCIE3 PCIE4 PCIE6	Select Auto/PCIE1/PCIE2/PCIE3/PCIE4/PCIE6 of D28:F0/F1/F2/F3/F4/F6
Internal Graphics	**Auto** Disabled Enable	Keep IGD enabled based on the setup options.
Aperture Size	128MB **256MB** 512MB 1024MB 2048MB 4096MB	Select the Aperture Size. Note: Above 4GB MMIO BIOS assignment is automatically enabled when selecting 2048MB aperture. To use this feature, please disable CSM Support.
DVMT Pre-Allocated	0M **32M** 64M 4M 8M 12M 16M 20M 24M	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.
DVMT Total Gfx Mem	**256M** 128M MAX	Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device.
Gfx Low Power Mode	**Enabled** Disabled	This option is applicable for SFF only.
EDP to LVDS Bridge Configuration	Info only	
Data Format and Color Depth	VESA 24 bpp JEIDA 24 bpp **JEIDA/VESA 18 bpp**	Data format and color depth select
LVDS Output Mode	**Single LVDS bus** Dual LVDS bus	Single/Dual mode select
DE Polarity	**Active High** Active Low	DE Polarity select
Vsync Polarity	**Active High** Active Low	Vsync Polarity select
Hsync Polarity	**Active High** Active Low	Hsync Polarity select
LVDS Backlight Mode	**BMC Mode** GTT Mode	Select LVDS Backlight control function.

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Table 4-17: Advanced Menu > Graphics (Continued)

Feature	Options	Description
GTT LVDS/eDP Backlight Control	0% 20% 40% 60% 80% **100%**	Actual backlight value in percent of the maximum setting.
Primary IGFX Boot Display	**VBIOS Default**	Select the Video Device which will be activated during POST.This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display.
LCD Panel Type	**VBIOS Default** 640X480 800X600 1024X768 1280X1024 1400X1050 1600X1200 1366X768 1680X1050 1920X1200 1440X900 1600X900 1024X768 1280X800 1920X1080 2048X1536	Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.
Active LFP	No LVDS **eDP Port-A**	Select the Active LFP Configuration.
Panel Scaling	**Auto** Off Force Scaling	Select the LCD panel scaling option used by the Internal Graphics Device.

Advanced > SATA

Table 4-18: Advanced Menu > SATA

Feature	Options	Description
SATA Controller(s)	**Enabled** Disabled	Enable/Disable SATA Device.
SATA Mode Selection	**AHCI** RAID	Determines how SATA controller(s) operate.
SATA Test Mode	Enabled **Disabled**	Test Mode Enable/Disable (Loop Back)
Software Feature Mask Configuration ►	Submenu	
Aggressive LPM Support	**Enabled** Disabled	Enable PCH to aggressively enter link power state.

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Table 4-18: Advanced Menu > SATA (Continued)

Feature	Options	Description
SATA Controller Speed	Default Gen1 **Gen2** Gen3	Indicates the maximum speed the SATA controller can support.
Serial ATA Port X Configuration ►	Submenu	

Advanced > SATA > SATA Port Configuration

Table 4-19: Advanced Menu > SATA > SATA Port Configuration

Feature	Options	Description
Serial ATA Port 0	Info only	
Software Preserve	Info only	
Port X	Disabled **Enabled**	Enable/Disable SATA Port.
Hot Plug	Disabled **Enabled**	Designates this port as Hot Pluggable.
External SATA	**Disabled** Enabled	External SATA Support.
Spin up Device	**Disabled** Enabled	If enabled for any of ports Staggered Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
SATA Device Type	**Hard Disk Drive** Solid State Drive	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.
Topology	**Unknown** ISATA Direct Connect Flex M2	Identify the SATA Topology if it is Default, ISATA, Flex, DirectConnect or M2.
Device Sleep	**Disabled** Enabled	mSATA for RTD3
SATA DEVSLEP Idle Timeout Configuration	**Disabled** Enabled	Enable/Disable SATA DTIO Configuration

Advanced > SATA > Software Feature Mask Configuration

Table 4-20: Advanced Menu > SATA > Software Feature Mask Configuration

Feature	Options	Description
RAID0	**Enabled** Disabled	Enable/Disable RAID0 feature
RAID1	**Enabled** Disabled	Enable/Disable RAID1 feature
RAID10	**Enabled** Disabled	Enable/Disable RAID10 feature.
RAID5	**Enabled** Disabled	Enable/Disable RAID5 feature.
Intel Rapid Recovery Technology	**Enabled** Disabled	Enable/Disable Intel Rapid Recovery Technology.

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Table 4-20: Advanced Menu > SATA > Software Feature Mask Configuration (Continued)

Feature	Options	Description
OROM UI and BANNER	**Enabled** Disabled	If enabled, then the OROM UI is shown. Otherwise, no OROM banner or information will be displayed if all disks and RAID volumes are Normal.
HDD Unlock	**Enabled** Disabled	If enabled, indicates that the HDD password unlock in the OS is enabled.
LED Locate	**Enabled** Disabled	If enabled, indicates that the LED/SGPIO hardware is attached and ping to locate feature is enabled on the OS.
IRRT Only on ESATA	**Enabled** Disabled	If enabled, then only IRRT volumes can span internal and eSATA drives. If disabled, then any RAID volume can span internal and eSATA drives.
Smart Response Technology	**Enabled** Disabled	Enable/Disable Smart Response Technology.
OROM UI Delay	**2 Seconds** **4 Seconds** **6 Seconds** **8 Seconds**	Select the delay time of the OROM UI Splash Screen in a normal status.
RST Force Form	Enabled **Disabled**	Enable/Disable Form for Intel Rapid Storage Technology.

Advanced > USB

Table 4-21: Advanced Menu > USB

Feature	Options	Description
USB Configuration ►	Submenu	
USB Module Version	Info only	
USB Devices	Info only	X Drive, X Keyboards, X Mouse, X Hubs
Legacy USB Support	**Enabled** Disabled Auto	Enables legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications and setup.
XHCI Hand-off	**Enabled** Disabled	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by the XHCI OS driver.
USB Mass Storage Driver Support	**Enabled** Disabled	Enable/Disable USB Mass Storage Driver Support.
Port 60/64 Emulation	Enabled **Disabled**	Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.
USB hardware delays and time-outs:	Info only	
USB transfer time-out	1 sec 5 sec 10 sec **20 sec**	The time-out value for Control, Bulk, and Interrupt transfers

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Table 4-21: Advanced Menu > USB (Continued)

Feature	Options	Description
Device reset time-out	10 sec **20 sec** 30 sec 40 sec	USB mass storage device Start Unit command time-out.
Device power-up delay	**Auto** Manual	Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.
Mass Storage Devices	Info only	List current USB max storage device.

Advanced > USB > USB Configuration

Table 4-22: Advanced Menu > USB > USB Configuration

Feature	Options	Description
USB Precondition	**Disabled** Enabled	Precondition work on USB host controller and root ports for faster enumeration.
XHCI Disable Compliance Mode	**FALSE** TRUE	Options to disable Compliance Mode. Default is FALSE to not disable Compliance Mode. Set TRUE to disable Compliance Mode.
XDCI Support	**Disabled** Enabled	Enable/Disable XDCI (USB OTG Device)
USB Port Disable Override	**Disabled** Select Per-Pin	Selectively Enable/Disable the corresponding USB port from reporting a Device Connection to the controller.

Advanced > Network

Table 4-23: Advanced Menu > Network

Feature	Options	Description
Network Stack	Info only	
Network Stack	Enabled **Disabled**	Enable/Disable UEFI network stack.
i219 lan controller	**Enabled** Disabled	Enable/Disable onboard NIC
i210 lan controller	**Enabled** Disabled	Enable/Disable i210 controller
Wake on LAN	Enabled **Disabled**	Enable/Disable integrated LAN to wake the system.
AMT Configuration	Info only	
AMT BIOS Feature	Enabled **Disabled**	When disabled AMT BIOS Features are no longer supported and user is no longer able to access MEBx Setup.Note:This option does not disable Manageability Features in FW.
MEBx Hotkey Pressed	Enabled **Disabled**	OEMFlag Bit 1:Enable automatic MEBx hotkey press.

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Table 4-23: Advanced Menu > Network (Continued)

Feature	Options	Description
MEBx Selection Screen	Enabled **Disabled**	OEMFlag Bit 2:Enable MEBx selection screen with 2 options: Press 1 to enter ME Configuration Screens Press 2 to initiate a remote connection Note: Network Access must be activated from MEBx Setup for this screen to be displayed.
Hide Un-Configure ME Confirmation	Enabled **Disabled**	OEMFlag Bit 6:Hide Unconfigure ME confirmation prompt when attempting ME unconfiguration.
MEBx Debug Message Output	Enabled **Disabled**	OEMFlag Bit 14:Enable OEM debug menu in MEBx.
Unconfigure ME	Enabled **Disabled**	OEMFlag Bit 6:Hide Unconfigure ME confirmation prompt when attempting ME unconfiguration.
ASF Support	**Enabled** Disabled	Enable/Disable Alert Specification Format.
Activate Remote Assistance Process	Enabled **Disabled**	Trigger CIRA boot Note: Network Access must be activated first from MEBx Setup.
USB Provisioning of AMT	**Enabled** Disabled	Enable/Disable USB Configure function.
PET Progress	**Enabled** Disabled	Enable/Disable PET Events progress to receive PET events.
CIRA Timeout	0	OEM defined timeout for MPS connection to be established. 0 - use the default timeout value of 60 seconds. 255 - MEBX waits until the connection succeeds.
Watchdog	Enabled **Disabled**	Enable/Disable WatchDog Timer.
OS Timer		Set OS watchdog timer.
BIOS Timer		Set BIOS watchdog timer.

Advanced > PCI and PCIe

Table 4-24: Advanced Menu > PCI and PCIe

Feature	Options	Description
PCI Common Settings	Info only	
PCI Latency Timer	**32 PCI Bus Clocks** 64 PCI Bus Clocks 96 PCI Bus Clocks 128 PCI Bus Clocks 160 PCI Bus Clocks 192 PCI Bus Clocks 224 PCI Bus Clocks 248 PCI Bus Clocks	Value to be programmed into PCI Latency Timer Register.

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Table 4-24: Advanced Menu > PCI and PCIe (Continued)

Feature	Options	Description
PCI-X Latency Timer	32 PCI Bus Clocks **64 PCI Bus Clocks** 96 PCI Bus Clocks 128 PCI Bus Clocks 160 PCI Bus Clocks 192 PCI Bus Clocks 224 PCI Bus Clocks 248 PCI Bus Clocks	Value to be programmed into PCI Latency Timer Register.
VGA Palette Snoop	**Disabled** Enabled	Allow PCI cards that do not contain their own VGA color palette to access the video core's palette
PERR# Generation	**Disabled** Enabled	Enables or Disables PCI Device to Generate PERR#.
SERR# Generation	**Disabled** Enabled	Enables/Disables PCI Device to Generate SERR#.
PCI Express Configuration ►	Submenu	

Advanced > PCI and PCIe > PCI Express Configuration

Table 4-25: Advanced Menu > PCI and PCIe > PCI Express Configuration

Feature	Options	Description
PEG Configuration	Info only	
PCI Express Clock Gating	Disabled **Enable**	Enable/Disable PCI Express Clock Gating for each root port.
Legacy IO Low Latency	**Disabled** Enabled	Set to enable low latency of legacy IO. Some systems require lower IO latency irrespective of power. This is a trade off between power and IO latency.
DMI Link ASPM Control	Disabled **Enable**	The control of Active State Power Management of the DMI Link.Auto is equal to POR setting.
Pcie Pll SSC	**Auto** 0.0% 0.1% 0.2% 0.3% 0.4% 0.5% 0.6% 0.7% 0.8% 0.9% 1.0% 1.1% 1.2% 1.3% 1.4% 1.5% 1.6% 1.7% 1.8% 1.9% 2.0%	Pcie Pll SSC percentage.AUTO - Keep hw default, no BIOS override. Range is 0.0%-2.0%.
Port8xh Decode	Disabled	PCI Express Port8xh Decode Enable/Disable.

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Table 4-25: Advanced Menu > PCI and PCIe > PCI Express Configuration (Continued)

Feature	Options	Description
Compliance Test Mode	Disabled	Enable when using Compliance Load Board.
PCI Express Gen3 EQ Lanes ►	Submenu	
PCI Express Root Port X ►	Submenu	

Advanced > PCI and PCIe > PCI Express Configuration > PCI Express Gen3 EQ Lanes

Table 4-26: Advanced Menu > PCI and PCIe > PCI Express Configuration > PCI Express Gen3 EQ Lanes

Feature	Options	Description
Override SW EQ settings	**Disabled** Enable	Override SW EQ settings

Advanced > PCI and PCIe > PCI Express Configuration > PCI Express Root Port X

Table 4-27: Advanced Menu > PCI and PCIe > PCI Express Configuration > PCI Express Root Port X

Feature	Options	Description
PCI Express Root Port	Disabled **Enable**	Control the PCI Express Root Port.
Topology	Unknown x1 x4 Sata Express M2	Identify the SATA Topology: Default, ISATA, Flex, DirectConnect or M2.
ASPM Support	Auto L0s L1 L0sL1 **Disabled**	Set the ASPM Level. Force L0s - Force all links to L0s State Auto - BIOS auto configure; Disabled - Disables ASPM
L1 Substates	Disabled L1.1 L1.2 **L1.1 & L1.2**	PCI Express L1 Substates settings.
Gen3 Eq Phase3 Method	Hardware Static Coeff **Software Search**	PCIe Gen3 Equalization Phase 3 Method
UPTP	**5**	Upstream Port Transmitter Preset.
DPTP	**7**	Downstream Port Transmitter Preset
ACS	Disable **Enable**	Enable/Disable Access Control Services Extended Capability.
URR	**Disabled** Enable	PCI Express Unsupported Request Reporting Enable/Disable.
FER	**Disabled** Enable	PCI Express Device Fatal Error Reporting Enable/ Disable.
NFER	**Disabled** Enable	PCI Express Device Non-Fatal Error Reporting Enable/Disable.
CER	**Disabled** Enable	PCI Express Device Correctable Error Reporting Enable/Disable.

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Table 4-27: Advanced Menu > PCI and PCIe > PCI Express Configuration > PCI Express Root Port X

Feature	Options	Description
CTO	**Disabled** Enable	PCI Express Completion Timer TO Enable/ Disable
SEFE	**Disabled** Enable	Root PCI Express System Error on Fatal Error Enable/Disable.
SENFE	**Disabled** Enable	Root PCI Express System Error on Non-Fatal Error Enable/Disable.
SECE	**Disabled** Enable	Root PCI Express System Error on Correctable Error Enable/Disable.
PME SCI	Disabled **Enable**	PCI Express PME SCI Enable/Disable.
Hot Plug	Disabled **Enable**	PCI Express Hot Plug Enable/Disable.
Advanced Error Reporting	Disable **Enable**	Advanced Error Reporting Enable/Disable.
PCIe Speed	**Auto** Gen1 Gen2 Gen3	Configure PCIe Speed.
Transmitter Half Swing	**Disabled** Enabled	Transmitter Half Swing Enable/Disable.
Detect Timeout	**0**	The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.
Extra Bus Reserved	**0**	Extra Bus Reserved (0-7) for bridges behind this Root Bridge.
Reserved Memory	**10**	Reserved Memory for this Root Bridge (1-20) MB.
Reserved I/O	**4**	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.
PCH PCIe LTR Configuration		
PCH PCIE1 LTR	**Disabled** Enable	PCH PCIE Latency Reporting Enable/Disable.
PCIE LTR Lock	**Disabled** Enabled	PCIE LTR Configuration Lock.
PCH PCIe CLKREQ# Configuration	Info only	
PCIE1 CLKREQ Mapping Override	**Default** No CLKREQ Custom number	PCIE CLKREQ Override for default platform mapping.
Snoop Latency Override	Disabled Manual **Auto**	Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Non Snoop Latency Override	Disabled Manual **Auto**	Non Snoop Latency Override for PCH PCIE. Disabled: Disable override.Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.

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Advanced > Super IO

Table 4-28: Advanced Menu > Super IO

Feature	Options	Description
Super IO Chip	Info only	
F81216 Super IO Configuration	Info only	
Serial Port 1 Configuration Serial Port Device Settings Change Settings	 **Enabled** Disabled IO=3F8h; IRQ=4 **Auto** IO=3F8h; IRQ=4 IO=3F8h; IRQ=3,4,5,6,7,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,10,11,12	 Enable/Disable Serial Port (COM). Fixed configuration of serial port. Select an optimal setting for Super IO device.
Serial Port 2 Configuration Serial Port Device Settings Change Settings	 **Enabled** Disabled IO=2F8h; IRQ=3 **Auto** IO=2F8h; IRQ=3 IO=3F8h; IRQ=3,4,5,6,7,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,10,11,12	 Enable/Disable Serial Port (COM). Fixed configuration of serial port. Select an optimal setting for Super IO device.

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Advanced > ACPI and Power Management

Table 4-29: Advanced Menu > ACPI and Power Management

Feature	Options	Description
ACPI and Power Management	Info only	
Enable ACPI Auto Configuration	Enabled **Disabled**	Enables or Disables BIOS ACPI Auto Configuration.
Enable Hibernation	**Enabled** Disabled	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	**S3 (Suspend to RAM)**	Select ACPI sleep state the system will enter when the SUSPEND button is pressed.
Lock Legacy Resources	Enabled **Disabled**	Enables or Disables Lock of Legacy Resources
ACPI Low Power S0 Idle	Enabled **Disabled**	This variable determines if we enable ACPI Lower Power S0 Idle Capability (Mutually exclusive with Smart connect).
Emulation AT/ATX	Emulation AT **ATX**	Select Emulation AT or ATX function. If this option set to [Emulation AT], BIOS will report no suspend functions to ACPI OS. In windows XP, it will make OS show shutdown message during system shutdown.

Advanced > Serial Port Console

Table 4-30: Advanced Menu > Serial Port Console

Feature	Options	Description
Serial Port Console	Info only	
COM0	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings ►	Submenu	
COM1	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	
COM2 ►	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings ►	Submenu	
COM3	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings ►	Submenu	

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Advanced > Serial Port Console > Console Redirection Settings

Table 4-31: Advanced Menu > Serial Port Console > Console Redirection Setting

Feature	Options	Description
Console Redirection Settings	Info only	
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed.
Data Bits	7 **8**	Select Data Bits.
Parity	**None** Even Odd Mark Space	Select Parity.
Stop Bits	1 **2**	Select number of stop bits.
Flow Control	**None** Hardware RTS/CTS	Select flow control.
VT-UTF8 Combo Key Support	Disabled **Enable**	Enable VT-UTF8 Combination Key Support for ANSI/ VT100 terminals.
Recorder Mode	**Disabled** Enable	With this mode enabled only text will be sent. This is to capture Terminal data.
Resolution 100x31	**Disabled** Enable	Enables or disables extended terminal resolution
Legacy OS Redirection	**80x24** 80x25	On Legacy OS, the Number of Rows and Columns supported redirection
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS Post	**Always Enabled** BootLoader	The Settings specify if BootLoader is selected than Legacy console redirection is disabled before booting to Legacy OS. Default value is Always Enable which means Legacy console Redirection is enabled for Legacy OS.

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Advanced > Serial Port Console >Legacy Console Redirection Settings

Table 4-32: Advanced Menu > Serial Port Console > Legacy Console Redirection Settings

Feature	Options	Description
Legacy Serial Redirection Port	**COM0** COM1 COM2 COM3	Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages.

Advanced > Serial Port Console >Console Redirection Settings

Table 4-33: Advanced Menu > Serial Port Console > Console Redirection Settings

Feature	Options	Description
Out-of-Band Mgmt Port	**COM0** COM1 COM2 COM3	Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.
Terminal	VT100 VT100+ **VT-UTF8** ANSI	
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Flow Control	**None** Hardware RTS/CTS Software Xon/Xoff	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
Data Bits	Info only	
Parity	Info only	
Stop Bits	Info only	

Advanced > ICC Configuration

Table 4-34: Advanced Menu > ICC Configuration

Feature	Options	Description
ICC Information	Info only	

Note: This is the only item in this menu available in the standard BIOS. Other options can be made available by customer request, if necessary.

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Advanced > Thermal

Table 4-35: Advanced Menu > Thermal

Feature	Options	Description
Thermal	Info only	
Active Trip Point	Disabled 40 C 50 C 60 C 70 C **BMC Default**	This value controls the temperature of the ACPI Active Trip Point - the point in which the OS will turn the processor fan on Active Trip Point Fan Speed.
Passive Trip Point	**Disabled** 80 C 90 C	This value controls the temperature of the ACPI Passive Trip Point - the point in which the OS will begin throttling the processor.
Critical Trip Point	**Disabled** 65 C 75 C 85 C	This value is the temperature threshold of the Critical Trip Point.
Watchdog ACPI Even Shutdown	**Disabled** Enable	Watchdog ACPI Even Shutdown Enable/Disable.

Advanced > Miscellaneous

Table 4-36: Advanced Menu > Miscellaneous

Feature	Options	Description
Trusted Computing ►	Submenu	
NVME Configuration ►	Submenu	

Advanced > Miscellaneous > Trusted Computing

Table 4-37: Advanced Menu > Miscellaneous > Trusted Computing

Feature	Options	Description
Security Device Support	**Enabled** Disabled	Enables or Disables BIOS support for security device. When disabled OS will not show Security Device. TCG EFI protocol and INT1A interface will not be available
TPM State	**Enabled** Disabled	Enable/Disable Security Device. NOTE: Your Computer will reboot during restart in order to change State of the Device.
Pending operation	**None** TPM Clear	Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.
Device Start	TPM 1.2 TPM 2.0 **Auto**	TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated

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Advanced > Miscellaneous > NVME Configuration

Table 4-38: Advanced Menu > Miscellaneous > NVME Configuration

Feature	Options	Description
NVME controller and Drive information	Info Only	

Advanced > AMI Graphics Output Protocol Policy (Video GOP show only)

Table 4-39: Advanced Menu > AMI Graphics Output Protocol Policy (Video GOP show only)

Feature	Options	Description
Intel(R) Graphics Controller	Info only	
Intel(R) GOP Driver	Info only	
Brightness String	**255**	Set GOP Brightness value
BIST Enable	**Disabled** Enable	Starts or stops the BIST on the integrated display panel

4.1.5 Boot Menu

Boot > Boot Configuration

Table 4-40: Boot Menu > Boot Configuration

Feature	Options	Description
Boot Configuration	Info only	
Setup Prompt Time Out	**1**	Enable/Disable the onboard SATA controllers.
Bootup NumLock State	**On**	Select SATA controller mode.
Quiet Boot	**Disabled** Enabled	Enable/Disable the PATA port. In fact this enables or disables the SATA channel on which the onboard SATA to PATA converter is attached. When set to enabled the system boot will be delayed for the time specified in PATA Port Detection Time out if no PATA device is connected. Auto: Scan for PATA device and enable per default.
CSM ►	Submenu	
Boot Option Priorities	Info only	
Fast Boot	Disable Enable	Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

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Boot > CSM Configuration

Table 4-41: Boot Menu > CSM Configuration

Feature	Options	Description
CSM Support	**Enabled** Disable	This option controls if CSM will be launched.
CSM16 Module Version	Info only	
GateA20 Active	**Upon Request** Always	UPON REQUEST: GA20 can be disabled using BIOS services. ALWAYS: do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.
Option ROM Messages	**Force BIOS** Keep Current	Set display mode for Option ROM.
INT19 Trap Response	**Immediate** Postponed	BIOS reaction on INT19 trapping by Option ROM
Boot Option filter	**UEFI and Legacy** Legacy only UEFI only	This option controls what devices system can to boot.
Option ROM execution	Info only	
Network	**Do not launch** Legacy only UEFI only	Controls the execution of UEFI and Legacy PXE OpROM.
Storage	Do not launch UEFI only **Legacy only**	Controls the execution of UEFI and Legacy Storage OpROM.
Video	Do not launch UEFI only **Legacy only**	Controls the execution of UEFI and Legacy Video OpROM.
Other PCI devices	UEFI OpROM Legacy OpROM	For PCI devices other than Network, Mass storage or Video defines which OpROM to launch.

4.1.6 Security Menu

Security > Password Description

Table 4-42: Security Menu > Password Description

Feature	Options
Administrator Password	Enter password
User Password	Enter password
HDD Security Configuration:	Info only
Px: xxxxxxxx	Info only

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4.1.7 Save & Exit Menu

Save & Exit > Reset Options

Table 4-43: Save & Exit Menu > Reset Options

Feature	Options	Description
Save Changes and Reset	Save changes and reset the system.	Save Changes and Reset
Discard Changes and Reset	Reset the system without saving any changes.	Discard Changes and Reset

Save & Exit > Save Options

Table 4-44: Save & Exit Menu > Save Options

Feature	Description
Save Changes	Save Changes done so far to any of the setup options.
Discard Changes	Discard Changes done so far to any of the setup options.
Restore Defaults	Restore/Load Default values for all the setup options.
Save as User Defaults	Save the changes done so far as User Defaults.
Restore User Defaults	Restore the User Defaults to all the setup options.

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4.2 BIOS Checkpoints, Beep Codes

This section lists checkpoints and beep codes generated by the AMI Aptio BIOS. The checkpoints defined in this document are inherent to the AMIBIOS generic core, and do not include any chipset or board specific checkpoint definitions.

4.2.1 Checkpoints and Beep Codes Definition

A checkpoint is either a byte or word value output to I/O port 80h. The BIOS outputs checkpoints throughout bootblock and Power-On Self Test (POST) to indicate the task the system is currently executing. Checkpoints are very useful for debugging problems that occur during the preboot process.

Beep codes are used by the BIOS to indicate a serious or fatal error. They are used when an error occurs before the system video has been initialized, and generated by the system speaker.

4.2.2 Aptio Boot Flow

While performing the functions of the traditional BIOS, Aptio 5.x core follows the firmware model described by the Intel Platform Innovation Framework for EFI (“the Framework”). The Framework refers the following “boot phases”, which may apply to various status code & checkpoint descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization[1]
- Driver Execution Environment (DXE) – main hardware initialization[2]
- Boot Device Selection (BDS) – system setup, pre-OS user interface & selecting a bootable device (CD/DVD, HDD, USB, Network, Shell, …)

4.2.3 Viewing BIOS Checkpoints

Viewing all checkpoints generated by the BIOS requires a checkpoint card, also referred to as a POST Card or POST Diagnostic Card. These are PCI add-in cards that show the value of I/O port 80h on a LED display.

Some computers display checkpoints in the bottom right corner of the screen during POST. This display method is limited, since it only displays checkpoints that occur after the video card has been activated.

Keep in mind that not all computers using AMI Aptio BIOS enable this feature. In most cases, a checkpoint card is the best tool for viewing AMI Aptio BIOS checkpoints.

[1]Analogous to “bootblock” functionality of legacy BIOS
[2]Analogous to “POST” functionality in legacy BIOS

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4.2.4 Status Code Ranges

Table 4-45: Status Code Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

4.2.5 Standard Status Codes

SEC Phase Status Codes

Table 4-46: Standard Status Codes (SEC Phase)

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization

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SEC Error Codes

Table 4-47: SEC Error Codes

SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

SEC Beep Codes

None

PEI Phase

Table 4-48: Standard Status Codes (PEI Phase)

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization

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Table 4-48: Standard Status Codes (PEI Phase) (Continued)

Status Code	Description
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	Reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes

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S3 Resume Error Codes

Table 4-49: S3 Resume Error Codes

Status Code	Description
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

PEI Beep Codes

Table 4-50: PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

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DXE Status Codes

Table 4-51: DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization

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Table 4-51: DXE Status Codes (Continued)

Status Code	Description
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM

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Table 4-51: DXE Status Codes (Continued)

Status Code	Description
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

DXE Beep Codes

Table 4-52: DXE Beep Codes

# of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

ACPI/ASL Checkpoint

Table 4-53: ACPI/ASL Checkpoint

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

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OEM-Reserved Checkpoint Ranges

Table 4-54: OEM-Reserved Check Point Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

4.3 SEMA Functions

Under the management of the BMC chip (Board Management Controller), the SEMA utility (Smart Embedded Management Agent) provides system control and failure protection—counting, monitoring, and measuring hardware and software events, from which the CPU can trigger corrective commands. The optional SEMA Cloud utility not only controls local events on the module but system client events on the Internet of Things (IoT.) Refer to the following bullets for a list of SEMA functions.

- Total operating hours counter
  Counts the time the module has been run in minutes.
- On-time minutes counter
  Counts the seconds since last system start.
- Monitoring of Board temperature
  Minimum and maximum temperature values of the board are stored in flash.
- Power monitor
  Reads the current drawn by the board and reports the nominal operating voltage.
- Power cycles counter
- Boot counter
  Boot counter is increased after a HW- or SW-Reset or after a successful power-up.
- Watchdog Timer
  Set / Reset / Disable Watchdog Timer.
- System Restart Cause
  Power loss / Watchdog / External Reset.
- Flash area
  1kB Flash area for customer data
- Protected Flash area
  128 Bytes for Keys, ID's, etc. can be stored in a write- and clear-protectable region.
- Board Identify
  Vendor / Board / Serial number

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The SEMA Tools are available for Windows and Linux. SEMA functionality can also be used in applications. Refer to the SEMA software manual and technical manual on the ADLINK web site for more information.



If a failure occurs while updating the BMC firmware through the SEMA command line, restart the system and repeat the update to resolve the failure.

4.3.1 Board Specific SEMA functions

Voltages

The BMC of the CMx-SLx implements a Voltage Monitor and samples several Onboard Voltages. The Voltages can be read by calling the SEMA function, “Get Voltages”. The function returns a 16-bit value divided in Hi-Byte (MSB) and Lo-Byte (LSB).

Table 4-55: SEMA Monitored Voltages

ADC Channel	Voltage Name	Voltage Formula [V]
0	VCC_CORE	(MSB<<8 + LSB) x 3.3 / 1024
1	V1P2	(MSB<<8 + LSB) x 3.3 / 1024
2	VTT	(MSB<<8 + LSB) x 3.3 / 1024
3	VDDQ	(MSB<<8 + LSB) x 3.3 / 1024
4	V1P8	(MSB<<8 + LSB) x 3.3 / 1024
5	V3P3	(MSB<<8 + LSB) x 1.1 x 3.3 / 1024
6	VCC	(MSB<<8 + LSB) x 1.83 x 3.3 / 1024
7	V12	(MSB<<8 + LSB) x 6.0 x 3.3 / 1024
8	MAINCURRENT	Use Main Current Function

Main Current

The BMC of the CMx-SLx implements a Current Monitor. The current can be read by calling the SEMA function “Get Main Current”. The function returns four 16-bit values divided in Hi-Byte (MSB) and Lo-Byte (LSB). These four values represent the last four currents drawn by the board. The values are sampled every 250ms. The order of the four values is NOT in relationship to time. The access to the BMC may increase the drawn current of the whole system. In this case, you still have three samples without the influence of the read access.

Main Current = (MSB_n<<8 + LSB_n) * 8.06mA

TS#-Events

TS# is activated by a temperature sensor when a device reaches its critical temperature and released when the device is back in its normal temperature range. This counter gives the user information about temperature or cooling issues. This counter is cleared when the system is removed from power. The CMx-SLx only monitors the board temperature and does not support TS#-Events.

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Exception Blink Codes

In the case of an error, the BMC shows a blink code on the STATUS-LED. This error code is also reported by the BMC Flags register. The Exception Code is not stored in the Flash storage and is cleared when the power is removed. Therefore, the “Clear Exception Code”-Command is not supported.

Table 4-56: Blink Codes

Exception Blink Code	Error Message
0	NOERROR
2	NO_VCORE_POK_3P3
3	NO_V1P2_POK_3P3
4	NO_VDDQ_POK_3P3
5	NO_V1P8_POK_3P3
6	NO_V3P3_POK_3P3
7	CRITICAL_TEMP
8	POWER_FAIL
9	VOLTAGE_FAIL
10	NO_BUF_PLT_RST_L

BMC Flags

The BMC Flags register returns the last detected exception code since power up.

4.4 Real Time Clock (RTC)

The CMx-SLx contains a Real Time (time of day) Clock (RTC), which can be backed up with an external Lithium Battery. The CMx-SLx will function without a battery in those environments which prohibit batteries. The CMx-SLx will also continue to operate after the battery life has been exceeded. Under these conditions all setup information is restored from the on-board flash memory during POST along with the default date and time information.



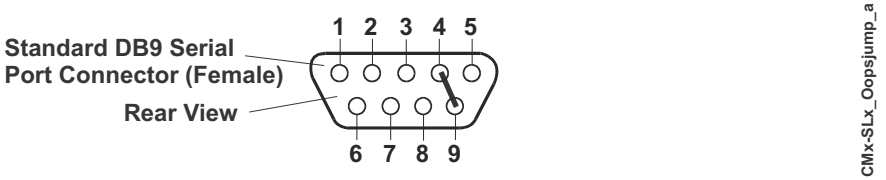
Some operating systems require a valid default date and time to function.

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4.5 Oops! Jumper (BIOS Recovery)

The Oops! jumper is provided in the event you have selected BIOS settings that prevent you from booting the system. By using the Oops! Jumper you can stop the current BIOS settings in the CMOS from being loaded, allowing you to proceed, using the default settings. Install a jumper on the CN15, 2-pin header or connect the DTR pin to the RI pin on Serial port 1 (COM 1) prior to boot up to prevent the present BIOS settings from loading. After booting with the Oops! Jumper in place, remove the Oops! Jumper and go into the BIOS Setup Utility. Change the desired BIOS settings, or select the default settings, and save changes before rebooting the system.

To convert a standard DB9 connector to an Oops! Jumper, short together the DTR (4) and RI (9) pins on the rear of the connector as shown in the following figure on the Serial Port 1 DB9 connector.



4.6 Serial Console

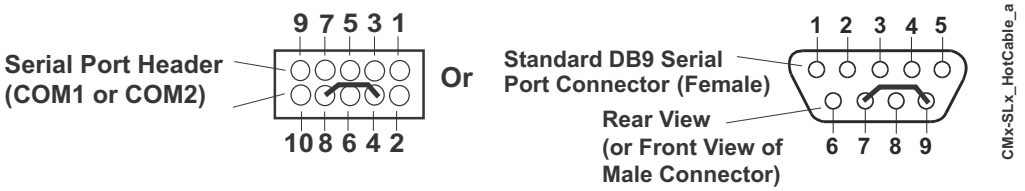
The CMx-SLx BIOS supports the serial console (or console redirection) feature. These I/O functions are provided by an ANSI-compatible serial terminal, or the equivalent terminal emulation software running on another system. This can be very useful when setting up the BIOS on a production line for systems that are not connected to a keyboard and display.

4.7 Serial Console BIOS Setup

The serial console (console redirection) feature is implemented by connecting a standard null-modem cable or a modified serial cable (or “Hot Cable”) from either serial port COM1 or COM2 (H16 or J18) to the serial terminal or a PC with communications software. The BIOS Setup Utility controls the serial console settings on the CMx-SLx. Refer to the BIOS Setup for the serial console option settings using a serial terminal or PC with communications software.

4.8 Hot (Serial) Cable

To convert a standard serial cable to a Hot Cable, certain pins must be shorted together at the Serial port header or at the DB9 connector. Short together the RTS (4) and RI (8) pins on either the COM1 or COM2 (H16 or J18) header. As an alternate, you can short the equivalent pins (pins 7 and 9) on the back of the respective DB9 connector as shown in the following figure.



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4.9 Watchdog Timer

The Watchdog Timer (WDT) restarts the system if an error or mishap occurs, allowing the system to recover from the mishap, even though the error condition may still exist. Possible problems include failure to boot properly, loss of control by the application software, failure of an interface device, unexpected conditions on the bus, or other hardware or software malfunctions.

The WDT is used through the SEMA during normal system operation. The following SEMA features provide support for the WDT.

- ADLINK SEMA provides an API for the WDT. The API tickles (resets) the WDT before the timer expires, otherwise the system will be reset.
- Watchdog Code examples – ADLINK has provided source code examples in the CMx-SLx SEMA, illustrating how to control the WDT. The code examples can be easily copied to your environment to compile and test, or to make any desired changes before compiling. Refer to the SEMA Programming Guide by downloading the SEMA Utility from the CMx-SLx web page.

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Appendix A System Resources

This appendix defines the system resources for the board including Interrupt Request Lines, Memory Map, I/O Address Map, PCI Configuration Space Map, and PCI Interrupt Routing Maps.

The interrupt request lines in PIC Mode are shown in Table A-1. Interrupt request lines for APIC mode are shown in Table A-2.

Table A-1: Interrupt Request Lines (PIC Mode)

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
0	Counter 0	N/A	No
1	Keyboard controller	IRQ1 via SERIRQ	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 2 (COM2)	IRQ3 via SERIRQ / PIRQ	Note (1)
4	Serial Port 1 (COM1)	IRQ4 via SERIRQ / PIRQ	Note (1)
5	Generic	IRQ5 via SERIRQ / PIRQ	Note (1)
6	Generic	IRQ6 via SERIRQ / PIRQ	No
7	Generic	IRQ7 via SERIRQ / PIRQ	Note (1)
8	Real-time clock	N/A	No
9	Generic	N/A	Note (1)
10	Generic	IRQ10 via SERIRQ / PIRQ	Note (1)
11	Generic	IRQ11 via SERIRQ / PIRQ	Note (1)
12	PS/2 Mouse	IRQ12 via SERIRQ / PIRQ	Note (1)
13	GSPI, UART, I2C, SDIO	N/A	Note (1)
14	Gpio	PIRQ	Note (1)
15	Gpio	PIRQ	Note (1)

Note (1): These IRQs can be used for PCI devices when onboard device is disabled.

Table A-2: Interrupt Request Lines (APIC Mode)

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
0	Counter 0	N/A	No
1	Keyboard controller	N/A	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 2 (COM2)	IRQ3 via SERIRQ / PIRQ	Note (1)
4	Serial Port 1 (COM1)	IRQ4 via SERIRQ / PIRQ	Note (1)
5	Generic	N/A	Note (1)
6	N/A	N/A	Note (1)
7	Generic	N/A	Note (1)
8	Real-time clock	N/A	No
9	N/A	IRQ9 via SERIRQ / PIRQ	Note (1)
10	N/A	IRQ10 via SERIRQ / PIRQ	Note (1)
11	N/A	IRQ11 via SERIRQ / PIRQ	Note (1)
12	Generic	IRQ12 via SERIRQ / PIRQ	Note (1)
13	Math Processor	N/A	Note (1)
14	Primary IDE controller	IRQ14 via SERIRQ / PIRQ	Note (1)
15	Secondary IDE controller	IRQ15 via SERIRQ / PIRQ	Note (1)
16	N/A	P.E.G Root Port, Intel HDA, PCIE Port 0/1/2/3/4/5/6,I.G.D ,XHCI Controller	Note (1)
17	N/A	PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port,	Note (1)

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Table A-2: Interrupt Request Lines (APIC Mode) (Continued)

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
18	N/A	PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port, SMBus Controller	Note (1)
19	N/A	PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port,	Note (1)
20	N/A	Gbe Controller	Note (1)
21	N/A		Note (1)
22	N/A	Intel HDA	Note (1)
23	N/A		Note (1)

The following table provides the common PC/AT memory allocations. These are DOS-level addresses. The OS typically hides these physical addresses by way of memory management.

Table A-3: Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
(4GB-2MB)	FFE00000 – FFFFFFFF	16 MB	High BIOS Area
(4GB-18MB) – (4GB-17MB-1)	FEE00000 – FEEFFFFF	1 MB	MSI Interrupts
(4GB-20MB) – (4GB-19MB-1)	FEC00000 – FECFFFFF	1 MB	APIC Configuration Space
15MB – 16MB	F00000 – FFFFFF	1 MB	ISA Hole
1MB -15MB	100000 - EFFFFF	14MB	Main Memory
0K –1MB	00000 – FFFFFF	1MB	DOS Compatibility Memory

Table A-4 shows the I/O address map. These are DOS-level addresses. The OS typically hides these physical addresses by way of memory management.

Table A-4: I/O Address Map

Hex Range	Device
20h – 21h	Interrupt Controller
24h – 25h	Interrupt Controller
28h – 29h	Interrupt Controller
2Ch – 2Dh	Interrupt Controller
02E-02F	LPC/eSPI
30h – 31h	Interrupt Controller
34h – 35h	Interrupt Controller
38h – 39h	Interrupt Controller
3Ch – 3Dh	Interrupt Controller
040	Timer/Counter
42h – 43h	Timer/Counter
4Eh – 4Fh	LPC/eSPI
50h	Timer/Counter
52h – 53h	Timer/Counter
60h	LPC/eSPI
61h	NMI Controller
62h	Microcontroller
63h	NMI Controller1
64h	Microcontroller

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Table A-4: I/O Address Map (Continued)

Hex Range	Device
65h	NMI Controller1
66h	Microcontroller
67h	NMI Controller1
70h	RTC Controller
71h	RTC Controller
72h	RTC Controller
73h	RTC Controller
74h	RTC Controller
75h	RTC Controller
76h – 77h	RTC Controller
80h	LPC/eSPI or PCIe
84h – 86h	Reserved
88h	Reserved
8Ch – 8Eh	Reserved
90h	(Alias to 80h)
092	Reset Generator
94h – 96h	(Aliases to 8xh)
98h	(Alias to 88h)
9Ch – 9Eh	(Alias to 8xh)
A0h – A1h	Interrupt Controller
A4h – A5h	Interrupt Controller
A8h – A9h	Interrupt Controller
ACh – ADh	Interrupt Controller
B0h – B1h	Interrupt Controller
B2h – B3h	Interrupt Controller
B4h – B5h	Interrupt Controller
B8h – B9h	Interrupt Controller
BCh – BDh	Interrupt Controller
200 – 207h	Gameport Low
208–20Fh	Gameport High
4D0h – 4D1h	Interrupt Controller
CF9h	Reset Generator

Table A-5 provides the PCI configuration space map.

Table A-5: PCI Configuration Space Map

Device: Functions #	Function Description
Bus 0: Device 31: Function 0	LPC Interface (eSPI Enable Strap = 0) eSPI Interface (eSPI Enable Strap = 1)
Bus 0: Device 31: Function 2	Memory Controller
Bus 0: Device 31: Function 3	Intel® High Definition Audio (Intel® HD Audio) (Audio, Voice, Speech)
Bus 0: Device 31: Function 4	SMBus Controller
Bus 0: Device 31: Function 6	GbE Controller
Bus 0: Device 28: Function 0	PCI Express Port 1
Bus 0: Device 28: Function 1	PCI Express Port 2

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Table A-5: PCI Configuration Space Map (Continued)

Device: Functions #	Function Description
Bus 0: Device 28: Function 2	PCI Express Port 3
Bus 0: Device 28: Function 3	PCI Express Port 4
Bus 0: Device 28: Function 5	PCI Express Port 6
Bus 0: Device 28: Function 6	PCI Express Port 7
Bus 0: Device 23: Function 0	SATA Controller
Bus 0: Device 22: Function 0	Intel® MEI #1
Bus 0: Device 20: Function 0	USB 3.0 xHCI Controller

Table A-6 provides the PCI interrupt routing map for the PEG Root Port and the Audio, xHCI, ME, and GbE controllers.

Table A-6: PCI Interrupt Routing Map (Controllers)

INT Line	P.E.G Root Port	Audio Controller	xHCI Controller	ME Controller #1	GbE Controller
Int0	INTA:16	INTA:16	INTA:16	INTA:16	INTA:16
Int1	INTB:17			INTD:19	
Int2	INTC:18			INTC:18	
Int3	INTD:19			INTB:17	

Table A-7 provides the PCI interrupt routing map for the five PCIe ports.

Table A-7: PCI Interrupt Routing Map (PCIe Ports)

INT Line	PCIE port1	PCIE port 2	PCIE port 3	PCIE port 4	PCIE port5
Int0	INTA:16	INTB:17	INTC:18	INTD:19	INTA:16
Int1	INTB:17	INTC:18	INTD:19	INTA:16	INTB:17
Int2	INTC:18	INTD:19	INTA:16	INTB:17	INTC:18
Int3	INTD:19	INTA:16	INTB:17	INTC:18	INTC:19

Table A-8 provides the PCI interrupt routing map for the LPC, SATA, and SMBus controllers.

Table A-8: PCI Interrupt Routing Map (LPS, SATA, and SMBus Controllers)

INT Line	LPC Controller	SATA Controller #1	SMBus Controller	SATA Controller #2
Int0	INTA:16	INTA:16	INTA:16	
Int1	INTB:17			
Int2	INTC:18			
Int3	INTD:19			

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