ADLINK TECHNOLOGY INC.

aTCA-6200

Dual Intel Xeon E5-2648L AdvancedTCA Processor Blade

User's manual



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Revision History

Revision	Release Date	Description of Change(s)
2.00	December 20, 2012	Initial release

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1 Overview

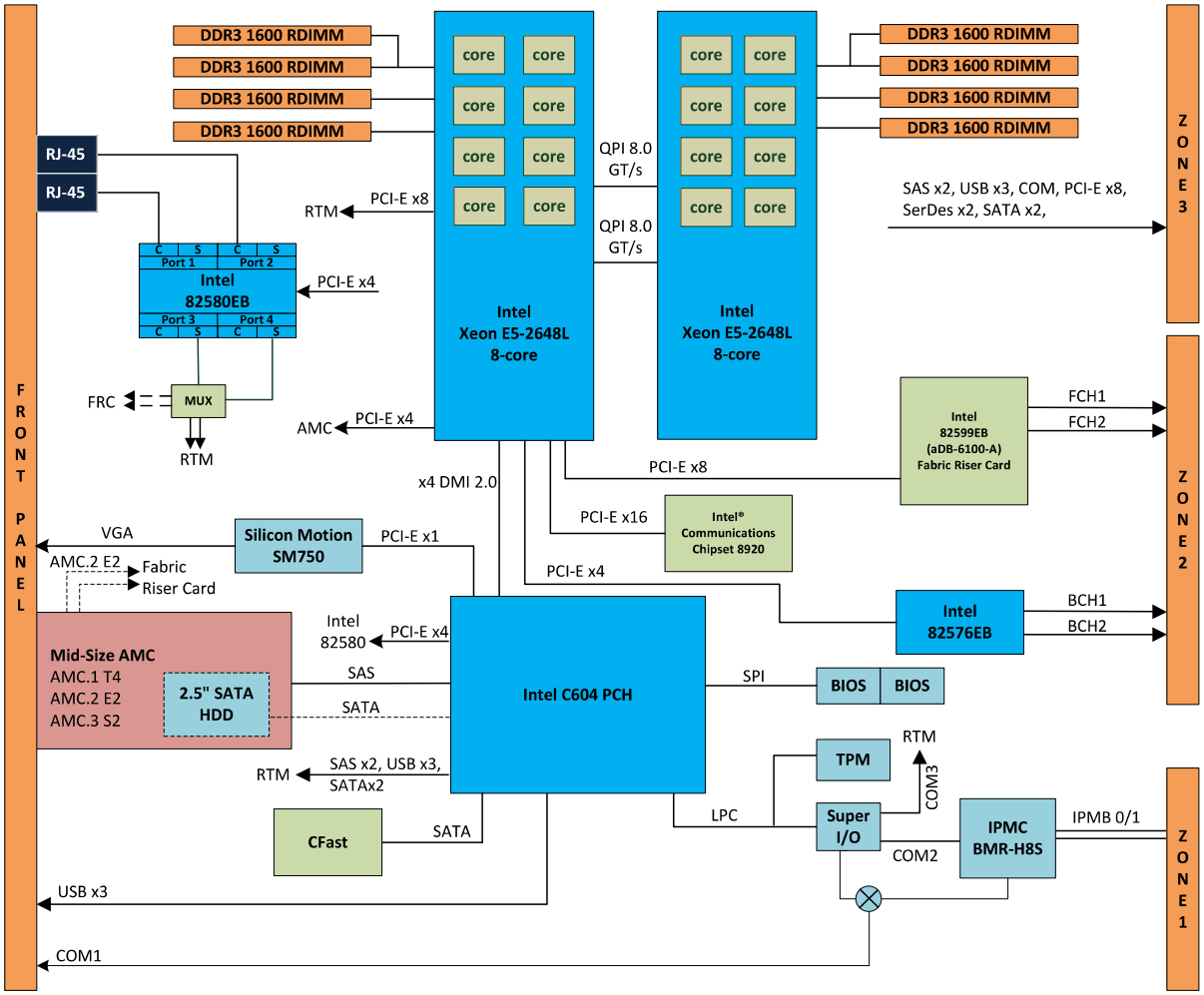
1.1 Introduction

The aTCA-6200 is a highly sophisticated AdvancedTCA processor blade supporting dual eight-core Intel® Xeon® processor E5-2648L, eight DDR3-1600 VLP RDIMMs up to 128 GB memory capacity and one single width, mid-size AMC bay. The aTCA-6200 delivers the computing power of 32 concurrent threads, massive I/O and memory capacity, and flexible connectivity for high-end telecom and media server applications requiring carrier-grade reliability and performance. More detailed features are outlined below and a functional block diagram is shown in the next section.

- Two eight-core Intel® Xeon® processor E5-2648L
- Server-class Intel® C604 PCH
- Intel® Communications Chipset 8920
- DDR3-1600 JEDEC standard VLP RDIMM (REG/ECC), up to 128 GB
- Onboard bootable SATA interface CFast card socket
- One Intel® 82580EB PCI-Express Gigabit Ethernet controller
- One Intel® 82576EB PCI-Express Gigabit Ethernet controller
- Intel® 82599EB PCI-Express 10Gigabit Ethernet (XAUI) controller
- Dual PICMG 3.1 option 9 Fabric Interface channels
- One single width, mid-size AMC bay supports AMC.0/1/2/3
- Failover system BIOS
- Analog RGB up to 1920x1440 resolution

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1.2 Block Diagram



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1.3 Package Contents

Before opening the product box, please check the shipping carton for any damage. If the shipping carton and contents are damaged, notify the dealer for a replacement. Retain the shipping carton and packing material for inspection by the dealer. Obtain authorization before returning any product to ADLINK.

Check that the following items are included in the package. If there are any missing items, contact your dealer:

- aTCA-6200 AdvancedTCA processor blade (CPU, RAM specifications may differ depending on options selected)
- RJ-45 to DB9 cable

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2 Specifications

2.1 aTCA-6200 Specifications

2.1.1 CPU/ Chipset/ Memory

CPU	Dual Eight-Core Intel® Xeon® Processor E5-2648L, (2.1GHz QPI 8.0GT/s, 20MB L2 cache, LGA2011 Socket)
Chipset	Intel® C604 PCH Intel® Communications Chipset 8920
Memory	Support Registered ECC DDR3-1600 VLP RDIMM Eight RDIMM sockets Up to 128GB

2.1.2 Standard and Interface

Standards	PICMG 3.0 R2.0 AdvancedTCA PICMG 3.1 AdvancedTCA Ethernet option 9
Networking	One Quad-Port Intel® 82580EB Gigabit Ethernet Controller One Dual-Port Intel® 82576EB Gigabit Ethernet Controller Dual 10/100/1000BASE-T RJ45 ports on face plate Dual GbE SerDes to RTM Dual 10/100/1000BASE-T Base Interface Channels Dual 10GBASE-BX4 Fabric Interface Channels via Intel® 82599EB 10G Ethernet Controller on aDB-6100-A riser card (option 9)
Display	Silicon Motion SM750 graphics controller Analog RGB up to 1920x1440 resolution
USB	Three USB 2.0 ports on front panel, three USB 2.0 ports to RTM
Serial	One RS-232 port (RJ-45) on front panel, One RS-232 port to RTM
Storage	Support AMC.3 SAS/SATA Onboard bootable CFast socket Onboard 2.5 inch SATA HDD mounting space (optional: shares the same space with AMC bay) Three SAS channels to RTM
Front panel I/O	1x VGA port (DB-15) 3x USB 2.0 port (Type-A) 1x RS-232 port (RJ45) 2x GbE ports (RJ45) 1x Single width, mid-size AMC slot LEDs: OOS, Media, User and Hotswap Recessed reset button
Rear I/O	PCI-E x8 from CPU1 1x COM port 3x USB 2.0 ports 2x SATA ports from C604 PCH 3x SAS ports from C604 PCH 2x GbE SerDes ports

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2.1.3 Software

BIOS	AMI® BIOS with 8Mbit flash memory
Supported OS	Microsoft® Windows® Server 2008 Microsoft® Windows® Server 2008 R2 RedHat Enterprise Linux Release 6.2 MontaVista Linux Carrier Grade Edition 5.1 Contact ADLINK for other OS availability

2.1.4 Mechanical & Environmental

Dimensions	322.25mm x 280mm x 30.48mm (H x D x W) - 6HP slot
Operating temperature	Standard: 0°C to 50°C NEBS short-term: 0°C to 55°C
Storage temperature	-40°C to 85°C
Humidity	5% to 90% non-condensing
Shock	15G peak-to-peak, 11ms duration, non-operation
Vibration	Non-operating: 1.88G rms, 5 to 500 Hz, each axis Operating: 0.5G rms. 5 to 500Hz, each axis
Compliance	CE, FCC Class A, CUL, NEBS Level 3 (design)

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2.2 Power Consumption

This section provides information on the power consumption of the aTCA-6200.

System configuration
(1) Memory: 8x ATP XL13N4E8GS-C-AD 8GB DDR3-1333 ECC REG
(2) Graphics: Silicon Motion SM750
(3) Power Supply: Sunpower SPS-600P-48
(4) Dual Eight-Core Xeon E5-2648L

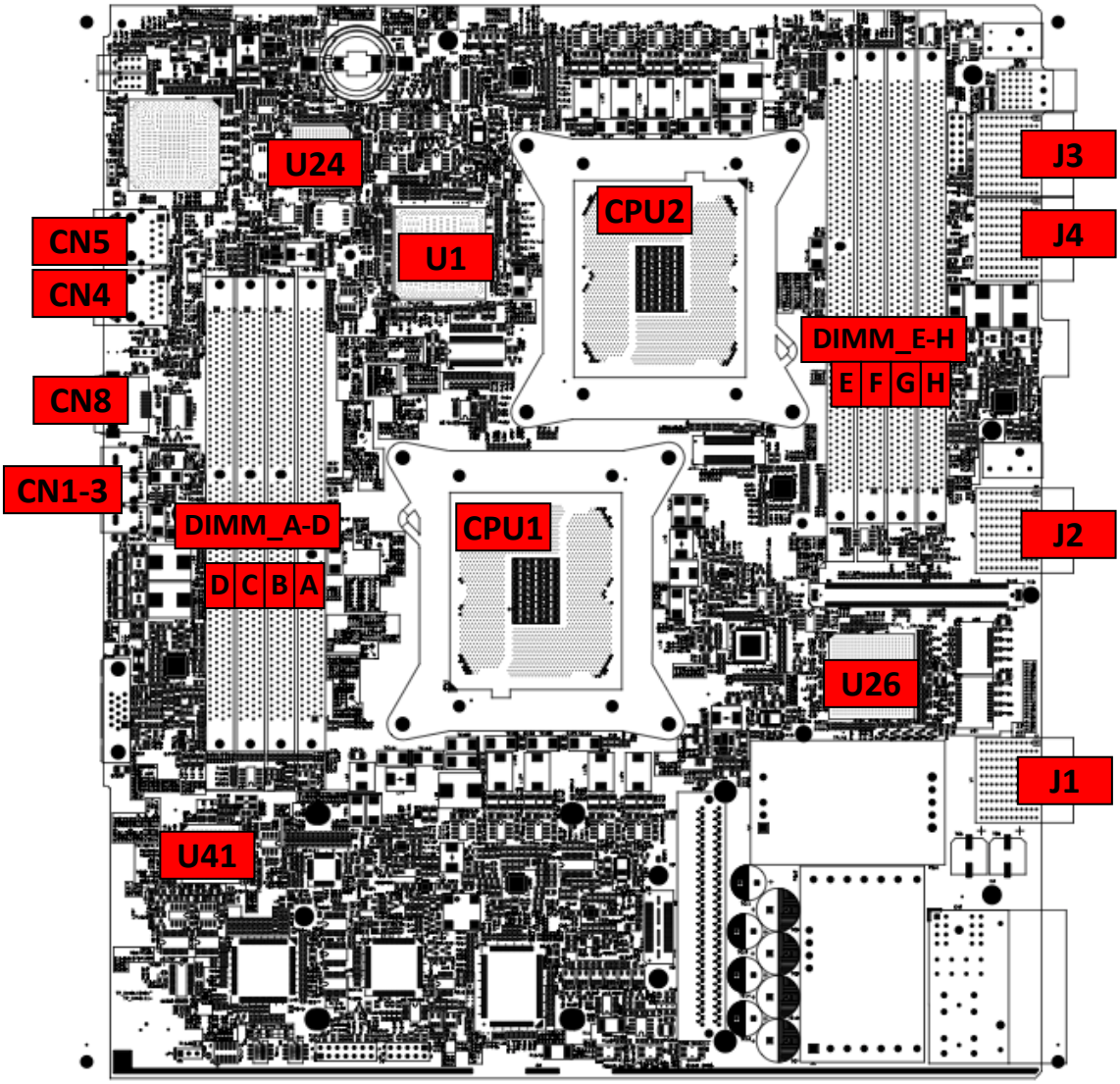
The following table describes power consumption with a 48V power rail under different OS and applications.

OS and Applications	aTCA-6200
DOS	123.36 W
Linux, Idle	111.36 W
Windows® Server 2008 R2, idle	70.08 W
Windows® Server 2008 R2, BurnIn Test, CPU 100% usage	167.04 W
Windows® Server 2008 R2, Power Thermal Utility, CPU 100% Usage	180.48 W

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2.3 Board Layout

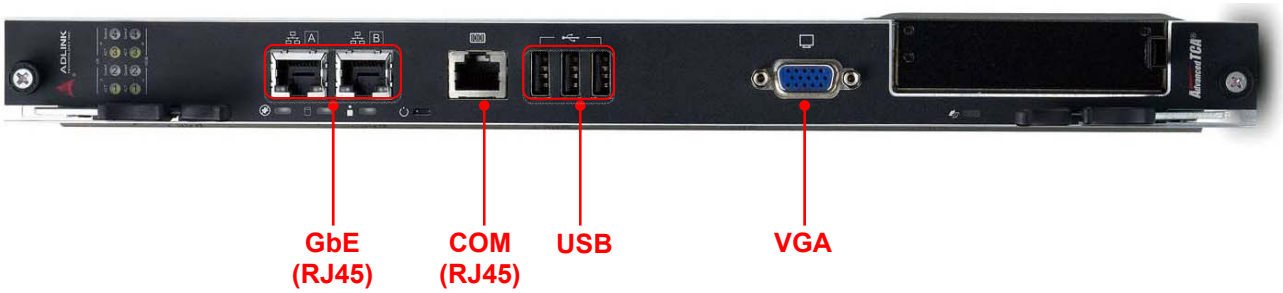
2.3.1 aTCA-6200 Board Layout



Location	Description	Location	Description
CN4	1GbE Ethernet ports	**DDR3_E-H**	DDR3-1600 DIMM E-H
CN5	1GbE Ethernet ports	**J1**	Base Interface
CN8	COM port	**J2**	Fabric Interface
CN10	DB-15 VGA connector	**J3-J4**	Zone 3 to RTM
CN1-3	USB ports	**U1**	Intel C604 PCH
CPU1	CPU1 Socket	**U24**	Intel 82580EB
CPU2	CPU2 Socket	**U26**	Intel 82576EB
DDR3_A-D	DDR3-1600 DIMM A-D	**U41**	Silicon Motion SM750

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aTCA-6200 Front Panel



Out of Service LED (Red)

Media LED (Green)

User LED (Amber)

Hot-swap LED (Blue)

Reset button

2.3.2 LED Definition

The following shows the LED in the front panel includes the Hot-swap LED, User LED, Media LED, and OOS LED.

2.3.2.1 Hot-swap LED

Hot-swap LED (Blue)	FRU State number	FRU State Name
Off	M0	FRU not installed
On	M1	FRU inactive
Long blink	M2	FRU activation request
Off	M3	FRU activation in process
Off	M4	FRU active
Short blink	M5	FRU deactivation request
Short blink	M6	FRU deactivation in process

2.3.2.2 OOS LED

Out of Service LED (Red)	State	Remark
Blink	During BIOS POST	FRU State M4
Off	BIOS POST OK	FRU State M4
On	After OS shutdown	FRU State M1

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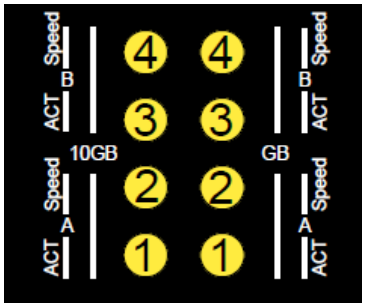
2.3.2.3 Media LED

Media LED (Green)	State	Remark
Blink	Accessing Disk I/O	
Off	Disk I/O idle	

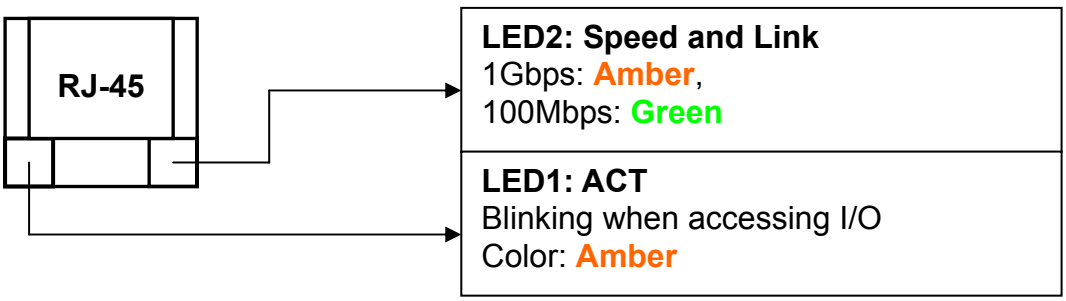
2.3.2.4 User LED

User LED (Amber)	State	Remark
On	Default On	This LED is reserved for customer applications and can be controlled via GPIO.

2.3.2.5 Base and Fabric Channel LED

BASE Channel and Fabric Channel LED		
Fabric 2 Speed and Link 1Gbps – OFF 10Gbps – ON (Amber)		BCH2 Speed and Link 100 Mbps: Green 1Gbps: Amber
Fabric 2 ACT (Amber) Blink when accessing Ethernet I/O		BCH2 ACT (Amber) Blink when accessing Ethernet I/O
Fabric 1 Speed and Link 1Gbps - OFF 10Gbps – ON (Amber)		BCH1 Speed and Link 100 Mbps: Green 1Gbps: Amber
Fabric 1 ACT (Amber) Blink when accessing Ethernet I/O		BCH1 ACT (Amber) Blink when accessing Ethernet I/O

2.3.2.6 GbE LED



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2.4 Compliance

The aTCA-6200 conforms to the following specifications:

- PICMG 3.0 R2.0 ECN0002 AdvancedTCA
- PICMG 3.1 Ethernet over AdvancedTCA option 9
- AMC.0 Advanced Mezzanine Card R2.0 single width, midsize
- AMC.1 PCI Express R1.0
- AMC.2 E2 / Type 4 (shares concurrent LAN3/4 from Intel 82580EB with 2x Serdes to RTM)
- AMC.3 Storage R1.0

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3 Functional Description

3.1 CPU, Memory and Chipset

3.1.1 CPU

The Intel Xeon E5-2648L processor implements several key technologies:

- Four channel Integrated Memory Controller supporting DDR3
- Integrated I/O with up to 40 lanes for PCI Express* Generation 3.0
- Two point-to-point link interface based on Intel® QuickPath Interconnect (Intel® QPI) up to 8.0GT/s
- 20 MB of shared cache
- Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3) and Streaming SIMD Extensions 4 (SSE4).

The Intel E5-2648L processor supports several advanced technologies:

- Execute Disable Bit
- Intel® 64 Technology
- Enhanced Intel SpeedStep® Technology
- Intel® Virtualization Technology (Intel® VT)
- Intel® Hyper-Threading Technology (Intel® HT Technology)

The Intel Xeon E5-2648L processor has a max. TDP of 70W and has an elevated case temperature specification. The elevated case temperatures are intended to meet the short-term thermal profile requirements of NEBS Level 3. The Intel Xeon E5-2648L processor is ideal for thermally constrained form factors in embedded servers, communications and storage markets.

Supported Processors, Maximum Power Dissipation

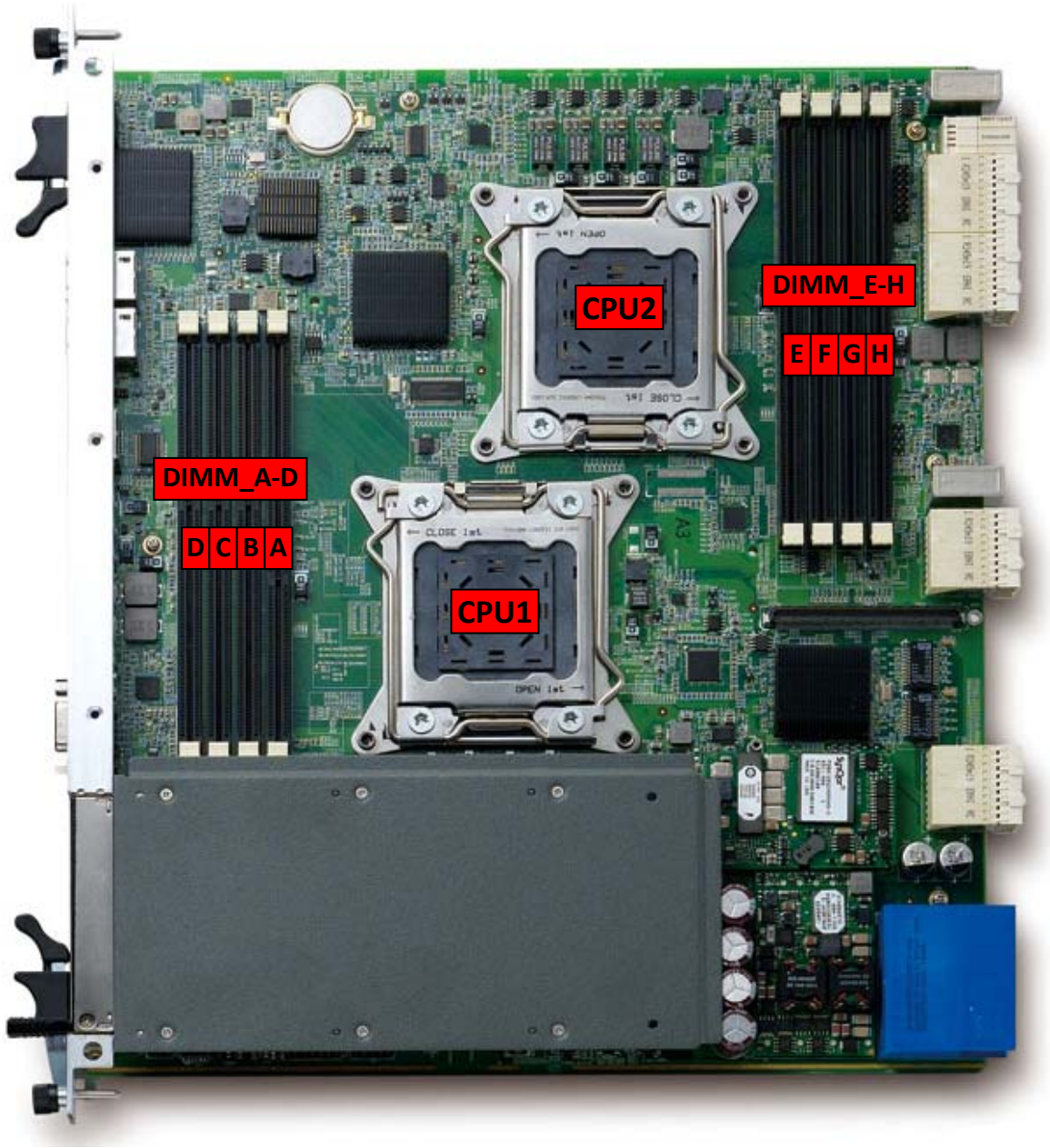
The following table describes the Intel E5-2648L processor supported by the aTCA-6200

Name	Intel® Xeon® processor E5-2648L
L2 cache	20MB
Clock	1.8GHz
QPI	8.0 GT/s
TDP	70W

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3.1.2 Memory

The aTCA-6200 supports DDR3-1600 RDIMM with eight DIMM sockets (A to D and E to H) up to 128GBytes. Socket A to D are controlled by integrated memory controller in CPU1 as well as socket E/F/G/H are controlled by integrated memory controller in CPU2. There are 3 memory channels from CPU1 for socket A/B/C/D while socket C/D share the same memory channel. The design logic also applies to socket E/F/G/H and socket G/H share the same memory channel.



Memory configuration changes are only permitted to be performed at the factory. Failure to comply with the above may result in damage to your board or improper operation.

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3.1.3 Intel® C604 PCH Overview

The Intel® C604 Chipset PCH provides a connection point between various I/O components and DMI based processors.
Functions and capabilities include:

- PCI Express Base Specification, Revision 2.0 support for up to eight ports with transfers up to 5 GT/s.
- PCI Local Bus Specification, Revision 2.3 support for 33 MHz PCI operations (supports up to four Req/Gnt pairs).
- ACPI Power Management Logic Support, Revision 4.0a Enhanced DMA controller, interrupt controller, and timer functions
- Integrated Serial Attached SCSI host controllers at transfer rate up to 3Gb/s on up to four ports.
- Integrated Serial ATA host controller switch independent DMA operation on up to six ports.
- USB host interface with two EHCI high-speed USB 2.0 Host controllers and 2 rate matching hubs provide support for support for up to fourteen USB 2.0 ports
- Integrated 10/100/1000 Gigabit Ethernet MAC with System Defense
- System Management Bus (SMBus) Specification, version 2.0 with additional support for I2C* devices
- Intel® High Definition Audio Supports
- Intel® Rapid Storage Technology enterprise (Intel® RSTe)
- Intel® Active Management Technology (Intel® AMT)
- Intel® Virtualization Technology for Directed I/O (Intel® VT-d)
- Intel® Trusted Execution Technology (Intel® TXT)
- Low Pin Count (LPC) interface Firmware Hub (FWH) interface
- Serial Peripheral Interface (SPI)
- Intel® Anti-Theft Technology (Intel® AT)
- JTAG Boundary Scan support

3.1.4 Intel® Communications Chipset 8920

The Intel® Communications Chipset 8920, enables workload consolidation across the control and data planes. Support for Intel® QuickAssist Acceleration Technology provides optimized packet and network capabilities by offloading cryptographic and compression workloads to the Intel® Communications Chipset 8920, freeing up CPU resources.

- PCI Express Gen2 x16 Uplink
- Support Intel® QuickAssist Technology

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3.1.5 Silicon Motion SM750 Graphics Controller

The aTCA-6200 provides an analog VGA port on the front panel powered by Silicon Motion SM750 2D graphics controller with the following features:

- PCI-Express x1 architecture
- 16MB integrated video DDR memory
- Low power consumption < 1.5W
- 300 MHz DAC supports up to 1920x1440 resolution
- 128-bit 2D graphic engine
- ROPs, BitBLT, transparent BLT, pattern BLT, Color expansion, and Line drawing
- YUV-16/32-bit RGB conversion
- Support 7 layers of display frames (2 hardware cursors, primary graphic, video, video alpha, alpha, and secondary graphic)
- Two 8-bit portsorone16-bitvideocaptureportsupportsITU601
- and ITU 656 specifications UV-16/32-bit RGB conversion
- ReduceOnTM Power Management Technology
- Quick-Rotation features allow for 90°, 180°, and 270° rotation of on-screen images

3.2 Peripherals

The following standard peripherals are available on the aTCA-6200 blad

3.2.1 Battery

The aTCA-6200 is equipped with a 3.0 V “coin cell” lithium battery for the RTC. To replace the battery, proceed as follows:

- Turn off power
- Remove the battery
- Place the new battery in the socket

Make sure that you insert the battery with the correct orientation. The positive pole must be on the top.

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. A suitable battery is the Panasonic CR2032.

Note: The user must be aware that the battery’s operational temperature range is less than that of the aTCA-6200’s storage temperature range. For exact temperature range information, refer to the battery manufacturer’s specifications.

Note: Care must be taken to ensure that the battery is correctly replaced. The battery should be replaced only with an identical or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer’s instructions. The typical life expectancy of a 225mAh battery

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(VARTA CR2032) is 4-5 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and standby (shutdown) time of the system in which it operates. To ensure that the lifetime of the battery has not been exceeded, it is recommended to change the battery after 3-4 years.

3.2.2 Reset

The aTCA-6200 is automatically reset by a precision voltage monitoring circuit that detects a drop in voltage below the acceptable operating limit of 4.85V for the 5V line and below 3.2V for the 3.3V line. Other reset sources include the Watchdog Timer, the face plate push-button switch and also the RESET signal from the IPMC. The aTCA-6200 responds to any of these sources by initializing local peripherals.

A reset will be generated by the following conditions:

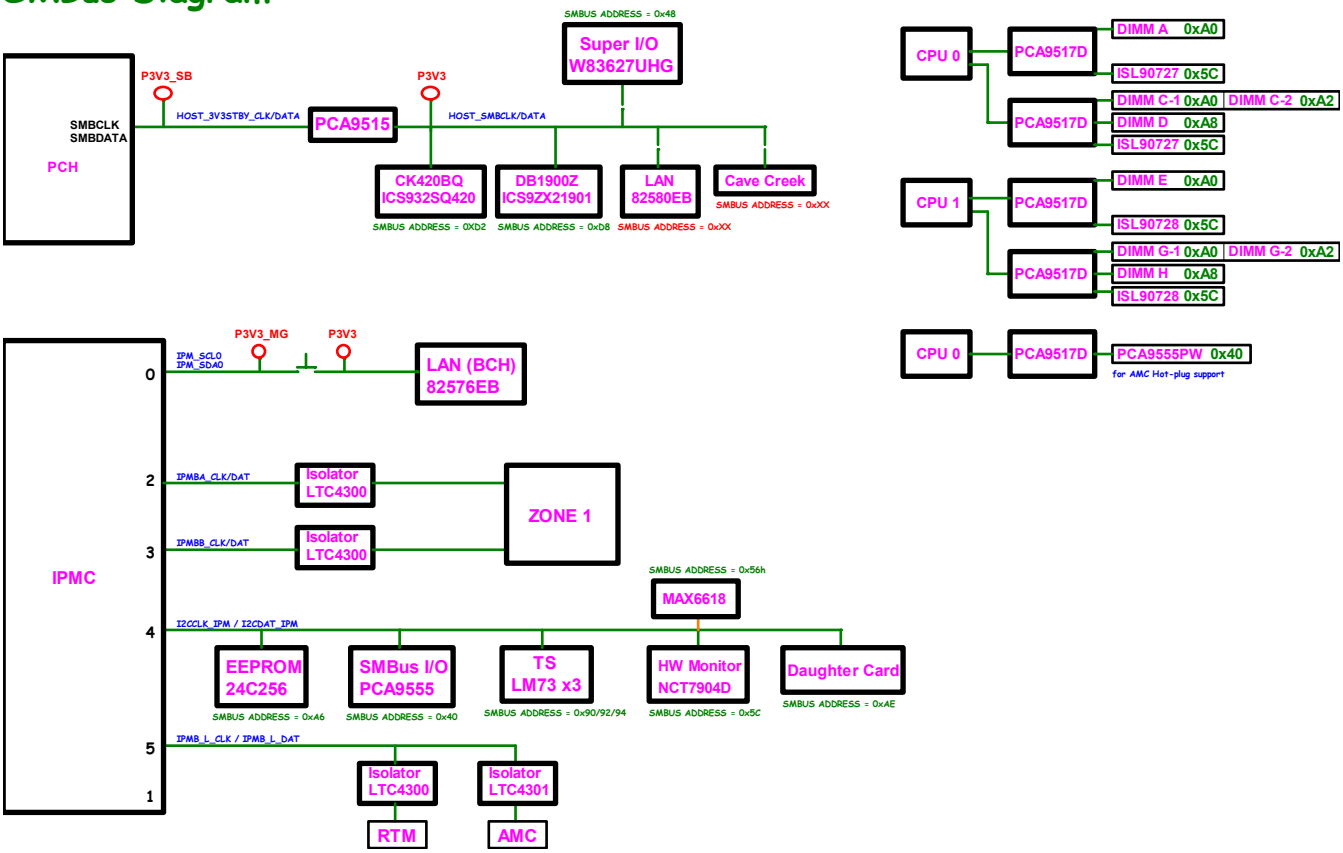
- Power failure, +5 V supply falls below 4.1 V (typ.) or +3.3 V supply falls below 2.93 V (typ.)
- Pushbutton ´RESET" pressed
- Watchdog time-out
- IPMI controller reset

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3.2.3 SMBus Devices

The aTCA-6200 provides a System Management Bus (SMBus) hosted by the C604 PCH as shown in the diagram below.

SMBus Diagram



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3.2.4 GPIO List

The following table summarizes GPIO usage on the C604 PCH

Name	Power Well	Default	Description	Name	Power Well	Default	Description
GPIO0	3.3V	GPI	IRQ_SSB_SCI_WHEA_N (PU)	**GPIO38**	3.3V	GPI	Unused (PU)
GPIO1	3.3V	GPI	Unused (PU)	**GPIO39**	3.3V	GPI	Unused (PU)
GPIO2	5V	GPI	TTL_ERR_N0	**GPIO40**	3.3V_SB	Native	Unused (PU)
GPIO3	5V	GPI	FM_ERR1_DLY_N	**GPIO41**	3.3V_SB	Native	USB1_OC-L (PU)
GPIO4	5V	GPI	FM_IBMC_SSB_SMI_LPC_N (PU)	**GPIO42**	3.3V_SB	Native	Unused (PU)
GPIO5	5V	GPI	IRQ_IBMC_SSB_NMI (PU)	**GPIO43**	3.3V_SB	Native	USB2_OC-L (PU)
GPIO6	3.3V	GPI	Unused (PU)	**GPIO44**	3.3V_SB	GPI	Unused (PU)
GPIO7	3.3V	GPI	Unused (PU)	**GPIO45**	3.3V_SB	GPI	Unused (PU)
GPIO8	3.3V_SB	GPO	IRQ_CATERR_DLY_BUF_N	**GPIO46**	3.3V_SB	GPI	Unused (PU)
GPIO9	3.3V_SB	Native	Unused (PU)	**GPIO47**	3.3V_SB	GPI	Unused (PU)
GPIO10	3.3V_SB	Native	Unused (PU)	**GPIO48**	3.3V	GPI	Unused (reserve PU)
GPIO11	3.3V_SB	Native	PU_SMB_ALERT_N (PU)	**GPIO49**	3.3V	GPI	Unused (PU)
GPIO12	3.3V_SB	Native	LOM_DEV_OFF_N (PU)	**GPIO50**	5V	Native	Unused (PU)
GPIO13	3.3V_SB	GPI	FM_IBMC_SSB_SCI_LPC_N (PU)	**GPIO51**	3.3V	Native	PU_SGPIO_GSX_DOUT (PU)
GPIO14	3.3V_SB	Native	Unused (PU)	**GPIO52**	5V	Native	Unused (PU)
GPIO15	3.3V_SB	GPO	SAS_SATA_RAID_KEY (PU)	**GPIO53**	3.3V	Native	Unused (PU)
GPIO16	3.3V	GPI	PU_SSB_GP16 (PU)	**GPIO54**	5V	Native	Unused (PU)
GPIO17	3.3V	GPI	Unused (PU)	**GPIO55**	3.3V	Native	FM_BIOS_RCVR_BOOT_N (PU)
GPIO18	3.3V	GPO	Unused (PU)	**GPIO56**	3.3V_SB	GPI	Unused (PU)
GPIO19	3.3V	GPI	FM_BIOS_SPI_WP_N	**GPIO57**	3.3V_SB	GPI	FM_ME_RCVR_N (PU)
GPIO20	3.3V	GPO	FM_SMI_ACTIVE_N (PU)	**GPIO58**	3.3V_SB	Native	PMBUS_CLK (PU)
GPIO21	3.3V	GPI	Unused (PU)	**GPIO59**	3.3V_SB	Native	USB0_OC-L (PU)
GPIO22	3.3V	GPI	Unused (PU)	**GPIO60**	3.3V_SB	Native	IRQ_SML0_ALERT_N (PU)
GPIO23	3.3V	Native	Unused (PU)	**GPIO61**	3.3V_SB	GPO	LPC_TPM_PD_N
GPIO24	3.3V_SB	GPO	FM_PBG_DYN_SKU_KEY (PU)	**GPIO62**	3.3V_SB	Native	CLK_33K_SUSCLK_PLD
GPIO25	3.3V_SB	GPO	SSB_GP25 (TP)	**GPIO63**	3.3V_SB	Native	FM_SLPS5_N
GPIO26	3.3V_SB	GPO	SSB_GP26 (TP)	**GPIO64**	3.3V	GPO	Unused (TP)
GPIO27	3.3V_SB	GPI	FP_PWR_LED_N (PU)	**GPIO65**	3.3V	GPO	Unused (TP)
GPIO28	3.3V_SB	GPO	PD_SSB_GP28 (PU)	**GPIO66**	3.3V	GPO	USR_LED
GPIO29	3.3V_SB	GPI	FM_THROTTLE_N (PU)	**GPIO67**	3.3V	GPO	Unused (TP)
GPIO30	3.3V_SB	Native	PU_SUS_WARN_N (PU)	**GPIO68**	3.3V	GPI	Unused (PU)
GPIO31	3.3V_SB	GPI	IRQ_SML1_PMBUS_ALERT_N (PU)	**GPIO69**	3.3V	GPI	Unused (PU)
GPIO32	3.3V	GPO	FM_MULTIPLE_PCI_MASTER_N (PU)	**GPIO70**	3.3V	Native	Unused (PU)
GPIO33	3.3V	GPO	Unused (TP)	**GPIO71**	3.3V	Native	Unused (PU)
GPIO34	3.3V	GPI	FM_VIDEO_DISABLE_N (PU)	**GPIO72**	3.3V_SB	Native	PU_BATLOW_N (PU)
GPIO35	3.3V	GPO	FM_NMI_EVENT_N (PU)	**GPIO73**	3.3V_SB	GPI	Unused (PU)
GPIO36	3.3V	GPI	TP_SSB_GP36 (PD)	**GPIO74**	3.3V_SB	Native	IBMC_THERMTRIP_N (PU)
GPIO37	3.3V	GPI	Unused (reserve PU)	**GPIO75**	3.3V_SB	Native	PMBUS_DATA (PU)

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3.3 IO Interfaces

3.3.1 USB

The aTCA-6200 supports six USB 2.0 ports:

- Three Type-A ports on front panel
- Three ports routed to RTM

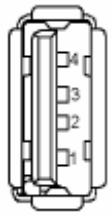
On the USB 2.0 front panel port, a USB cable with up to 5 meters in length can be used.

On the USB 2.0 Rear I/O ports, it is strongly recommended to use a cable below 3 meters in length for USB 2.0 devices.

The USB 2.0 ports are high-speed, full-speed, and low-speed capable. Hi-speed USB 2.0 allows data transfers of up to 480 Mb/s, 40 times faster than a full-speed USB (USB 1.1). One USB peripheral may be connected to each port.

Front Panel USB Connector (CN9-11)

Pin	USB 2.0 Signal Names
1	VCC
2	Data-
3	Data+
4	GND



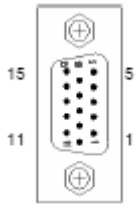
Note: The aTCA-6200 host interfaces can be used with maximum 500mA continuous load current as specified in the Universal Serial Bus Specification, Revision 2.0. Short circuit protection is provided. All the signal lines are EMI filtered.

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3.3.2 VGA Analog Interface

The DB-15 female connector CN10 is for analog display output.

Pin	Name	Pin	Name
1	RED	9	+5v
2	GREEN	10	GND
3	BLUE	11	NC
4	NC	12	DDC_DATA
5	GND	13	HSYNC
6	GND	14	VSYNC
7	GND	15	DDC_CLK
8	GND		



3.3.3 Ethernet Connection

The aTCA-6200 is equipped with one quad-port Intel® 82580EB Gigabit Ethernet Controller and one dual-port Intel® 82576EB Gigabit Ethernet Controller which provide six GbE ports in total. In default configuration, two ports (LAN 1/2) from Intel® 82580EB Gigabit Ethernet Controller are connected to the front panel RJ-45 ports. The other two ports (LAN3/4) are routed as GbE SerDes signals to Zone 3 RTM connectors or to the AMC port for AMC.2 E2 Support. Users can select the routing by changing the setting of switch SW11. Two GbE ports from Intel® 82576EB Gigabit Ethernet Controller are connected to Zone 2 Base Interface channel 1 and 2 (BCH1/BCH2).

The aDB-6100-A Fabric riser card provides the capability to support different configurations for Fabric Channels 1 and 2. An aDB-6100-A will be installed on the aTCA-6200 by default. An Intel 82599EB Ethernet controller on the riser card connects provides 10GbE links to Fabric Channels 1 and 2 (FCH1/FCH2).

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3.3.4 Serial Port

One PC-compatible serial RS-232 RJ-45 port is provided on the front panel with DIP switches SW9 and SW10 on the board that are used to set the COM port function (refer to section 3.3.5 for detailed switch settings). A complete set of handshaking and modem control signals are supported, with data transfer rates up to 115.2 kB/sec.

The Front Panel RS-232 RJ-45 connector pin-assignment fore different modes are listed below.

The pin assignment of front panel RS-232 RJ-45 connector for COM mode:

Pin	Signal Name	Function
1	DCD#	Data Carrier Detect
2	RTS#	Request to Send
3	DSR#	Data Set Ready
4	TXD	Transmit Data
5	RXD	Receive Data
6	GND	Ground
7	CTS#	Clear to Send
8	DTR#	Data Terminal Ready

The pin assignment of front panel RS-232 RJ-45 connector for IPMC debug mode:

Pin	Signal Name	Function
1	NC	No connected
2	NC	No connected
3	NC	No connected
4	DBG_TX	IPMC Transmit Data
5	DBG_RX	IPMC Receive Data
6	GND	Ground
7	NC	No connected
8	NC	No connected

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3.3.5 Switch Settings

3.3.5.1 Set Blade Operation Mode

Use Pin 2 of switch SW11 to set the Blade Operation Mode. Users can choose Normal Mode for operation with chassis or Standalone Mode for operation without chassis. Detailed settings are listed below.

Options	Pin1	Pin 2	Pin 3	Pin 4
Normal Mode	Off	Off	On	Off
Standalone Mode	Off	On	On	Off

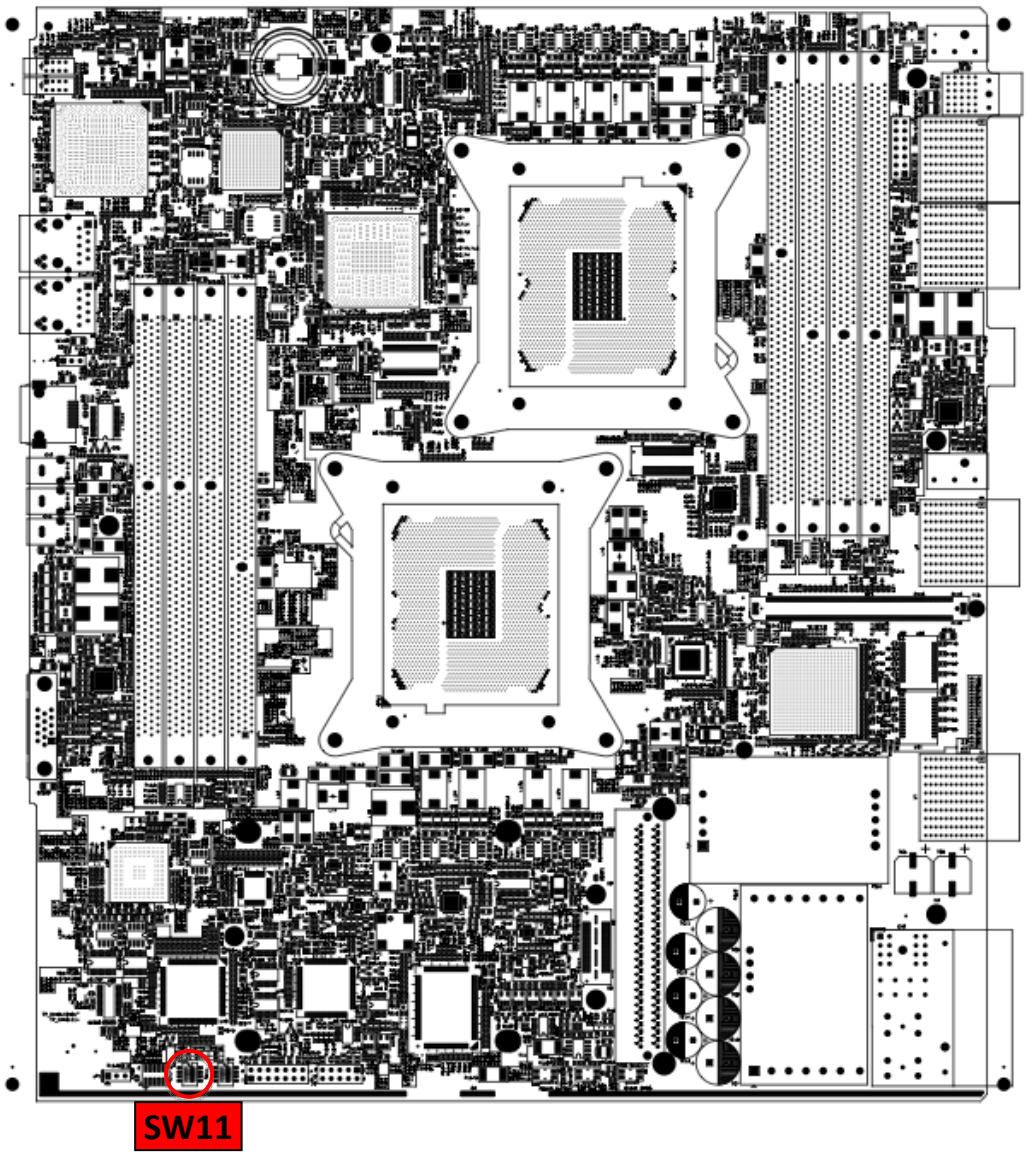
3.3.5.2 Select AMC.2 E2 Support

Use Pin 4 of switch SW11 to set the routing of LAN3/4 to Intel 82580EB to support AMC.2 E2 or to RTM. Detailed settings are listed below.

Options	Pin1	Pin 2	Pin 3	Pin 4
2x Serdes to RTM	Off	Off	On	Off
AMC.2 E2 Support	Off	Off	On	On

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Switch SW11 is located at the edge of PCB near the handle.

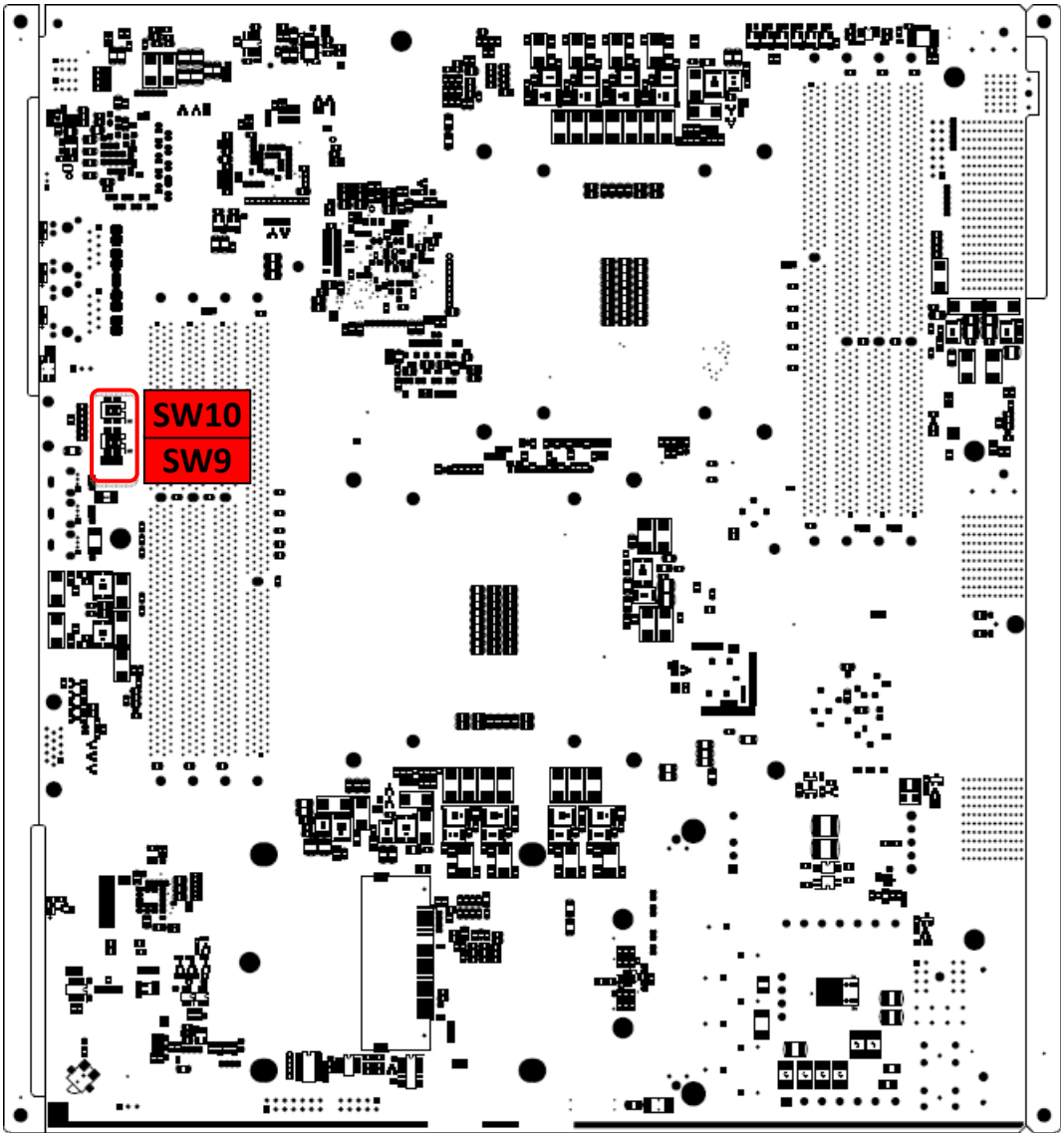


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3.3.5.3 Select Front Panel RJ-45 COM Port Mode

Use switches SW9 and SW10 located on the solder side of the aTCA-6200 to select the operating mode for front panel RJ-45 COM port. Users can choose RS-232 Mode for standard RS-232 COM port or IPMC Debug Mode which routes the front panel RJ-45 COM port to the IPMC.

Configuration	Switch	Pin 1	Pin 2	Pin 3	Pin 4
RS-232 Mode (default)	**SW9**	On	On	Off	Off
	SW10	On	Off	Off	Off
IPMC Debug Mode	**SW9**	Off	Off	On	On
	SW10	Off	On	On	On



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4 Hardware Platform Management

4.1 Platform Management Overview

The purpose of the hardware platform management system is to monitor, control, and assure proper operation of AdvancedTCA® Boards and other Shelf components. The hardware platform management system watches over the basic health of the system, reports anomalies, and takes corrective action when needed. The hardware platform management system can retrieve inventory information and sensor readings as well as receive event reports and failure notifications from Boards and other Intelligent FRUs. The hardware platform management system can also perform basic recovery operations such as power cycle or reset of managed entities.

The IPMI controller on aTCA-6200 supports an “intelligent” hardware management system, based on the Intelligent Platform Management Interface Specification. The hardware management system provides the ability to manage the power, cooling, and interconnect needs of intelligent devices; to monitor events; and to log events to a central repository.

4.2 IPMI Sensors

Following table shows all the sensors which aTCA-6200 supported.

Item	Sensor Name	Sensor Address	Description
(1)	Hot Swap	(0x0)	FRU Hotswap Sensor. Please refer to section 4.2.1
(2)	Hot Swap AMC 1	(0x1)	AMC#1 Hotswap Sensor. Please refer to section 4.2.1
(3)	RTM Hot Swap	(0x2)	RTM Hotswap Sensor. Please refer to section 4.2.1
(4)	Version change	(0x3)	Version Change Sensor. Please refer to section 4.2.4
(5)	IPMB Physical	(0x4)	Physical IPMB Sensor. Please refer to section 4.2.2
(6)	BMC Watchdog	(0x5)	Watchdog Timer Sensor. Please refer to section 4.2.3
(7)	+1.5V DDR-CPU	(0x6)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 1.65 Volts Upper Critical Threshold = 1.62 Volts Upper Non-Critical Threshold = 1.59 Volts Lower Non-Critical Threshold = 1.296 Volts Lower Critical Threshold = 1.242 Volts Lower Non-Recoverable Threshold = 1.215 Volts
(8)	+1.8V CPU0	(0x7)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 1.98 Volts Upper Critical Threshold = 1.944 Volts Upper Non-Critical Threshold = 1.908 Volts Lower Non-Critical Threshold = 1.692 Volts Lower Critical Threshold = 1.656 Volts Lower Non-Recoverable Threshold = 1.62 Volts
(9)	+1.5V DDR-CPU1	(0x8)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 1.65 Volts

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Item	Sensor Name	Sensor Address	Description
			Upper Critical Threshold = 1.62 Volts Upper Non-Critical Threshold = 1.59 Volts Lower Non-Critical Threshold = 1.296 Volts Lower Critical Threshold = 1.242 Volts Lower Non-Recoverable Threshold = 1.215 Volts
(10)	+1.8V CPU1	(0x9)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 1.98 Volts Upper Critical Threshold = 1.944 Volts Upper Non-Critical Threshold = 1.908 Volts Lower Non-Critical Threshold = 1.692 Volts Lower Critical Threshold = 1.656 Volts Lower Non-Recoverable Threshold = 1.62 Volts
(11)	+5.0V	(0xA)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 5.5 Volts Upper Critical Threshold = 5.4 Volts Upper Non-Critical Threshold = 5.3 Volts Lower Non-Critical Threshold = 4.7 Volts Lower Critical Threshold = 4.6 Volts Lower Non-Recoverable Threshold = 4.5 Volts
(12)	+3.3V	(0xB)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 3.63 Volts Upper Critical Threshold = 3.564 Volts Upper Non-Critical Threshold = 3.498 Volts Lower Non-Critical Threshold = 3.102 Volts Lower Critical Threshold = 3.036 Volts Lower Non-Recoverable Threshold = 2.97 Volts
(13)	+12V	(0xC)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 13.2 Volts Upper Critical Threshold = 12.96 Volts Upper Non-Critical Threshold = 12.72 Volts Lower Non-Critical Threshold = 11.28 Volts Lower Critical Threshold = 11.04 Volts Lower Non-Recoverable Threshold = 10.8 Volts
(14)	LM73 Temp PCH	(0xD)	Temperature Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 95 degrees C Upper Critical Threshold = 75 degrees C Upper Non-Critical Threshold = 60 degrees C Lower Non-Critical Threshold = 0 degrees C Lower Critical Threshold = -5 degrees C Lower Non-Recoverable Threshold = -10 degrees C
(15)	LM73 Temp PSU1	(0xE)	Temperature Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 95 degrees C Upper Critical Threshold = 75 degrees C Upper Non-Critical Threshold = 60 degrees C Lower Non-Critical Threshold = 0 degrees C Lower Critical Threshold = -5 degrees C Lower Non-Recoverable Threshold = -10 degrees C

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Item	Sensor Name	Sensor Address	Description
(16)	LM73 Temp 82580	(0xF)	Temperature Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 95 degrees C Upper Critical Threshold = 75 degrees C Upper Non-Critical Threshold = 60 degrees C Lower Non-Critical Threshold = 0 degrees C Lower Critical Threshold = -5 degrees C Lower Non-Recoverable Threshold = -10 degrees C
(17)	P0V75_DDR_VTT1	(0x10)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 0.825 Volts Upper Critical Threshold = 0.81 Volts Upper Non-Critical Threshold = 0.795 Volts Lower Non-Critical Threshold = 0.705 Volts Lower Critical Threshold = 0.69 Volts Lower Non-Recoverable Threshold = 0.675 Volts
(18)	P_VCCP1	(0x11)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 1.385 Volts Upper Critical Threshold = 1.365 Volts Upper Non-Critical Threshold = 1.35 Volts Lower Non-Critical Threshold = 0.6 Volts Lower Critical Threshold = 0.58 Volts Lower Non-Recoverable Threshold = 0.56 Volts
(19)	PVSA_CPU1	(0x12)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 1.232 Volts Upper Critical Threshold = 1.215 Volts Upper Non-Critical Threshold = 1.2 Volts Lower Non-Critical Threshold = 0.6 Volts Lower Critical Threshold = 0.582 Volts Lower Non-Recoverable Threshold = 0.565 Volts
(20)	PVTT_CPU1	(0x13)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 1.137 Volts Upper Critical Threshold = 1.117 Volts Upper Non-Critical Threshold = 1.095 Volts Lower Non-Critical Threshold = 1.005 Volts Lower Critical Threshold = 0.984 Volts Lower Non-Recoverable Threshold = 0.871 Volts
(21)	P0V75_DDR_VTT0	(0x14)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 0.825 Volts Upper Critical Threshold = 0.81 Volts Upper Non-Critical Threshold = 0.795 Volts Lower Non-Critical Threshold = 0.705 Volts Lower Critical Threshold = 0.69 Volts Lower Non-Recoverable Threshold = 0.675 Volts
(22)	P_VCCP0	(0x15)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 1.385 Volts Upper Critical Threshold = 1.365 Volts Upper Non-Critical Threshold = 1.35 Volts Lower Non-Critical Threshold = 0.6 Volts

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Item	Sensor Name	Sensor Address	Description
			Lower Critical Threshold = 0.58 Volts Lower Non-Recoverable Threshold = 0.56 Volts
(23)	PVSA_CPU0	(0x16)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 1.232 Volts Upper Critical Threshold = 1.215 Volts Upper Non-Critical Threshold = 1.2 Volts Lower Non-Critical Threshold = 0.6 Volts Lower Critical Threshold = 0.582 Volts Lower Non-Recoverable Threshold = 0.565 Volts
(24)	PVTT_CPU0	(0x17)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 1.137 Volts Upper Critical Threshold = 1.117 Volts Upper Non-Critical Threshold = 1.095 Volts Lower Non-Critical Threshold = 1.005 Volts Lower Critical Threshold = 0.984 Volts Lower Non-Recoverable Threshold = 0.871 Volts
(25)	P1V1_SSB	(0x18)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 1.21 Volts Upper Critical Threshold = 1.188 Volts Upper Non-Critical Threshold = 1.166 Volts Lower Non-Critical Threshold = 1.034 Volts Lower Critical Threshold = 1.012 Volts Lower Non-Recoverable Threshold = 0.99 Volts
(26)	P1V5_SSB	(0x19)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 1.65 Volts Upper Critical Threshold = 1.62 Volts Upper Non-Critical Threshold = 1.59 Volts Lower Non-Critical Threshold = 1.296 Volts Lower Critical Threshold = 1.242 Volts Lower Non-Recoverable Threshold = 1.215 Volts
(27)	P1V8_LAN_82576	(0x1A)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 1.98 Volts Upper Critical Threshold = 1.944 Volts Upper Non-Critical Threshold = 1.908 Volts Lower Non-Critical Threshold = 1.692 Volts Lower Critical Threshold = 1.656 Volts Lower Non-Recoverable Threshold = 1.62 Volts
(28)	P1V8_LAN_82580	(0x1B)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 1.98 Volts Upper Critical Threshold = 1.944 Volts Upper Non-Critical Threshold = 1.908 Volts Lower Non-Critical Threshold = 1.692 Volts Lower Critical Threshold = 1.656 Volts Lower Non-Recoverable Threshold = 1.62 Volts
(29)	P1V_LAN_82576	(0x1C)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 1.1 Volts Upper Critical Threshold = 1.08 Volts

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Item	Sensor Name	Sensor Address	Description
			Upper Non-Critical Threshold = 1.06 Volts Lower Non-Critical Threshold = 0.94 Volts Lower Critical Threshold = 0.92 Volts Lower Non-Recoverable Threshold = 0.9 Volts
(30)	P1V_LAN_82580	(0x1D)	Voltage Sensor. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 1.1 Volts Upper Critical Threshold = 1.08 Volts Upper Non-Critical Threshold = 1.06 Volts Lower Non-Critical Threshold = 0.94 Volts Lower Critical Threshold = 0.92 Volts Lower Non-Recoverable Threshold = 0.9 Volts
(31)	CPU0_Temp	(0x1E)	CPU Temperature. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 95 degrees C Upper Critical Threshold = 75 degrees C Upper Non-Critical Threshold = 60 degrees C Lower Non-Critical Threshold = 0 degrees C Lower Critical Threshold = -5 degrees C Lower Non-Recoverable Threshold = -10 degrees C
(32)	CPU1_Temp	(0x1F)	CPU Temperature. Please refer to section 4.2.5 Upper Non-Recoverable Threshold = 95 degrees C Upper Critical Threshold = 75 degrees C Upper Non-Critical Threshold = 60 degrees C Lower Non-Critical Threshold = 0 degrees C Lower Critical Threshold = -5 degrees C Lower Non-Recoverable Threshold = -10 degrees C

4.2.1 Get Sensor Reading (FRU Hotswap Sensor)

	Byte	Data field
Request data	1	Sensor Number (FFh = reserved)
Response data	1	Completion Code
	2	Sensor Reading. [7:0] - Not used. Write as 00h.
	3	Standard IPMI byte (See “Get Sensor Reading” in IPMI specification): [7] - 0b = All Event Messages disabled from this sensor [6] - 0b = sensor scanning disabled [5] - 1b = initial update in progress. This bit is set to indicate that a “Re-arm Sensor Events” or “Set Event Receiver” command has been used to request an update of the sensor status, and that update has not occurred yet. Software should use this bit to avoid getting an incorrect status while the first sensor update is in progress. This bit is only required if it is possible for the IPM Controller to receive and process a “Get Sensor Reading or Get Sensor Event Status” command for the sensor before the update has completed. This is most likely to be the case for sensors, such as fan RPM sensors,

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	Byte	Data field
		that may require seconds to accumulate the first reading after a re-arm. [4:0] – reserved. Ignore on read.
	4	Current State Mask [7] – 1b = FRU Operational State M7 - Communication Lost [6] – 1b = FRU Operational State M6 - FRU Deactivation In Progress [5] – 1b = FRU Operational State M5 - FRU Deactivation Request [4] – 1b = FRU Operational State M4 - FRU Active [3] – 1b = FRU Operational State M3 - FRU Activation in Progress [2] – 1b = FRU Operational State M2 - FRU Activation Request [1] – 1b = FRU Operational State M1 - FRU Inactive [0] – 1b = FRU Operational State M0 - FRU Not Installed
	(5)	[7:0] – Optional/Reserved. If provided, write as 80h (IPMI restriction). Ignore on read.

4.2.2 Get Sensor Reading (Physical IPMB-0 Sensor)

	Byte	Data field
Request data	1	Sensor Number (FFh = reserved)
Response data	1	Completion Code
	2	[7] – IPMB B Override State 0b = Override state, bus isolated 1b = Local Control state - IPM Controller determines state of bus. [6:4] = IPMB B Local Status 0h = No Failure. Bus enabled if no override in effect. 1h = Unable to drive clock HI 2h = Unable to drive data HI 3h = Unable to drive clock LO 4h = Unable to drive data LO 5h = Clock low timeout 6h = Under test (the IPM Controller is attempting to determine if it is causing a bus hang). 7h = Undiagnosed Communications Failure [3] – IPMB A Override State 0b = Override state, bus isolated 1b = Local Control state - IPM Controller determines state of bus. [2:0] = IPMB A Local Status 0h = No failure. Bus enabled if no override in effect. 1h = Unable to drive clock HI 2h = Unable to drive data HI 3h = Unable to drive clock LO 4h = Unable to drive data LO 5h = Clock low timeout 6h = Under test (the IPM Controller is attempting to determine if it is causing a bus hang). 7h = Undiagnosed Communications Failure
	3	Standard IPMI byte (see “Get Sensor Reading” in IPMI specification) [7] – 0b = All Event Messages disabled from this sensor

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	Byte	Data field
		[6] – 0b = Sensor scanning disabled [5] – 1b = Initial update in progress. This bit is set to indicate that a "Re-arm Sensor Events" or "Set Event Receiver" command has been used to request an update of the sensor status, and that update has not occurred yet. Software should use this bit to avoid getting an incorrect status while the first sensor update is in progress. This bit is only required if it is possible for the controller to receive and process a "Get Sensor Reading" or "Get Sensor Event Status" command for the sensor before the update has completed. This is most likely to be the case for sensors, such as fan RPM sensors, that may require seconds to accumulate the first reading after a re-arm. [4:0] – Reserved. Ignore on read.
	4	[7:4] – Reserved. Write as 0h, ignore on read [3] 1b = IPMB A enabled, IPMB-B enabled [2] 1b = IPMB A disabled, IPMB-B enabled [1] 1b = IPMB-A enabled, IPMB-B disabled [0] 1b = IPMB A disabled, IPMB-B disabled
	(5)	[7:0] – Optional/Reserved. If provided, write as 80h (IPMI restriction). Ignore on read.

4.2.3 Watchdog Timer Sensor

Sensor Type	Sensor Type Code	Sensor Specific Offset	Event
Watchdog 2	23h		This sensor is recommended for new IPMI v1.0 and later implementations.
		00h	Timer expired, status only (no action, no interrupt)
		01h	Hard Reset
		02h	Power Down
		03h	Power Cycle
		04h-07h	reserved
		08h	Timer interrupt
			The Event Data 2 field for this command can be used to provide an event extension code, with the following definition: 7:4 interrupt type 0h = none 1h = SMI 2h = NMI 3h = Messaging Interrupt Fh = unspecified all other = reserved 3:0 timer use at expiration: 0h = reserved 1h = BIOS FRB2 2h = BIOS/POST

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Sensor Type	Sensor Type Code	Sensor Specific Offset	Event
			3h = OS Load 4h = SMS/OS 5h = OEM Fh = unspecified all other = reserved

4.2.4 Version Change Sensor

Sensor Type	Sensor Type Code	Sensor Specific Offset	Event
Version Change	2Bh	00h	00h Hardware change detected with associated Entity. Informational. This offset does not imply whether the hardware change was successful or not. Only that a change occurred.
		01h	01h Firmware or software change detected with associated Entity.Informational. Success or failure not implied.
		02h	02h Hardware incompatibility detected with associated Entity.
		03h	03h Firmware or software incompatibility detected with associated Entity.
		04h	04h Entity is of an invalid or unsupported hardware version.
		05h	05h Entity contains an invalid or unsupported firmware or software version.
		06h	06h Hardware Change detected with associated Entity was successful. (deassertion event means unsuccessful').
		07h	07h Software or F/W Change detected with associated Entity was successful. (deassertion event means 'unsuccessful') *Event data 2 can be used for additional event information on the type of version change, with the following definition:* Event Data 2 7:0 Version change type 00h unspecified 01h management controller device ID (change in one or more fields from 'Get Device ID') 02h management controller firmware revision 03h management controller device revision 04h management controller manufacturer ID 05h management controller IPMI version 06h management controller auxiliary firmware ID 07h management controller firmware boot block 08h other management controller firmware

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			09h system firmware (EFI / BIOS) change 0Ah SMBIOS change 0Bh operating system change 0Ch operating system loader change 0Dh service or diagnostic partition change 0Eh management software agent change 0Fh management software application change 10h management software middleware change 11h programmable hardware change (e.g. FPGA) 12h board/FRU module change (change of a module plugged into associated entity) 13h board/FRU component change (addition or removal of a replaceable component on the board/FRU that is not tracked as a FRU) 14h board/FRU replaced with equivalent version 15h board/FRU replaced with newer version 16h board/FRU replaced with older version 17h board/FRU hardware configuration change (e.g. strap, jumper, cable change, etc.)

4.2.5 Get Sensor Reading Command

	Byte	Data field
Request data	1	Sensor Number (FFh = reserved)
Response data	1	Completion Code
	2	Sensor reading Byte 1: byte of reading. Ignore on read if sensor does not return an numeric (analog) reading.
	3	[7] - 0b = All Event Messages disabled from this sensor [6] - 0b = sensor scanning disabled [5] - 1b = reading/state unavailable (formerly “initial update in progress”). This bit is set to indicate that a ‘re-arm’ or ‘Set Event Receiver’ command has been used to request an update of the sensor status, and that update has not occurred yet. Software should use this bit to avoid getting an incorrect status while the first sensor update is in progress. This bit is only required if it is possible for the controller to receive and process a ‘Get Sensor Reading’ or ‘Get Sensor Event Status’ command for the sensor before the update has completed. This is most likely to be the case for sensors, such as fan RPM sensors, that may require seconds to accumulate the first reading after a re-arm. The bit is also used to indicate when a reading/state is unavailable because the management controller cannot obtain a valid reading or state for the monitored entity, typically because the entity is not present. For more in formation, please see *Section 16.4, Event Status, Even Conditions, and Present State* and *Section 16.6, Re-arming* on the PICMG specification 3.0. [4:0] - reserved. Ignore on read.
	4	For threshold-based sensors Present threshold comparison status

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	Byte	Data field
		[7:6] - reserved. Returned as 1b. Ignore on read. [5] - 1b = at or above (≥) upper non-recoverable threshold [4] - 1b = at or above (≥) upper critical threshold [3] - 1b = at or above (≥) upper non-critical threshold [2] - 1b = at or below (≤) lower non-recoverable threshold [1] - 1b = at or below (≤) lower critical threshold [0] - 1b = at or below (≤) lower non-critical threshold For discrete reading sensors [7] - 1b = state 7 asserted [6] - 1b = state 6 asserted [5] - 1b = state 5 asserted [4] - 1b = state 4 asserted [3] - 1b = state 3 asserted [2] - 1b = state 2 asserted [1] - 1b = state 1 asserted [0] - 1b = state 0 asserted
	(5)	For discrete reading sensors only. (Optional) (00h Otherwise) [7] - reserved. Returned as 1b. Ignore on read. [6] - 1b = state 14 asserted [5] - 1b = state 13 asserted [4] - 1b = state 12 asserted [3] - 1b = state 11 asserted [2] - 1b = state 10 asserted [1] - 1b = state 9 asserted [0] - 1b = state 8 asserted

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4.3 IPMI Commands

The following table presents all the commands which are supported by the aTCA-6200 in different interfaces and that are compatible with IPMI v1.5 and PICMG 3.0 R2.0 ECN001. There are two interfaces implemented with IPMI command support.

1. KCS: OpenIpmi
2. IPMB0: IPMBa & IPMBb

	KCS	IPMB0
IPMI commands		
IPM Device "Global" Commands		
Get Device ID	●	●
Cold Reset	●	●
Warm Reset	●	●
Get Self Test Results	●	●
Get Device GUID	●	●
IPMI Messaging Support Commands		
Set BMC Global Enables	●	●
Get BMC Global Enables	●	●
Clear Message Flags	●	●
Get Message Flags	●	●
Get Message	●	●
Send Message	●	●
Master Write-Read	●	●
BMC Watchdog Timer		
Reset Watchdog Timer	●	●
Set Watchdog Timer	●	●
Get Watchdog Timer	●	●
Event Commands		
Set Event Receiver	●	●
Get Event Receiver	●	●
Platform Event	●	●
Sensor Device Commands		
Get Device SDR Info	●	●
Get Device SDR	●	●
Reserve Device SDR Repository	●	●
Get Sensor Reading Factors	●	●
Set Sensor Hysteresis	●	●
Get Sensor Hysteresis	●	●
Set Sensor Threshold	●	●
Get Sensor Threshold	●	●
Set Sensor Event Enable	●	●
Get Sensor Event Enable	●	●
Rearm Sensor Events	●	●
Get Sensor Event Status	●	●
Get Sensor Reading	●	●

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FRU Device Commands		
Get FRU Inventory Area Info	●	●
Read FRU Data	●	●
Write FRU Data	●	●
PICMG Commands		
HPM.1 Upgrade Commands (HPM.1)		
Get target upgrade capabilities	●	●
Get component properties	●	●
Abort Firmware Upgrade	●	●
Initiate upgrade action	●	●
Upload firmware block	●	●
Finish firmware upload	●	●
Get upgrade status	●	●
Activate firmware	●	●
Query Self-test Results	●	●
Query Rollback status	●	●
Initiate Manual Rollback	●	●
AdvancedTCA		
Get PICMG Properties	●	●
Get Address Info	●	●
FRU Control	●	●
FRU Control Capabilities	●	●
Get FRU LED Properties	●	●
Get LED Color Capabilities	●	●
Set FRU LED State	●	●
Get FRU LED State	●	●
Set IPMB State		●
Set FRU Activation Policy	●	●
Get FRU Activation Policy	●	●
Set FRU Activation	●	●
Get Device Locator Record ID	●	●
Get Port State	●	●
Set Port State		●
Compute Power Properties		●
Set Power Level		●
Get Power Level	●	●
Bused Resource Control		●
Get IPMB Link Info	●	●
SET_CLOCK_STATE	●	●
GET_CLOCK_STATE	●	●
Get AMC-Port State		●
Set AMC-Port State		●

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5 Getting Started

The aTCA-6200 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

5.1 Safety Requirements

The following safety precautions must be observed when installing or operating the aTCA-6200. ADLINK assumes no responsibility for any damage resulting from failure to comply with these requirements.

Exercised due care when handling the board as the heat sink can get very hot. Do not touch the heat sink when installing or removing the board. The board should not be placed on any surface or in any form of storage container until the board and heat sink have cooled down to room temperature.

If your board type is not specifically qualified as being hot swap capable, switch off the AMC system power before installing the board in a free AMC slot. Failure to do so could endanger your life or health and may damage your board or system.

Certain AMC modules require bus master and/or Rear I/O capability. If you are in doubt whether such features are required for the board you intend to install, please check your specific board and/or system documentation to make sure that your system is provided with an appropriate free slot in which to insert the board.

This ATCA blade contains electrostatic sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

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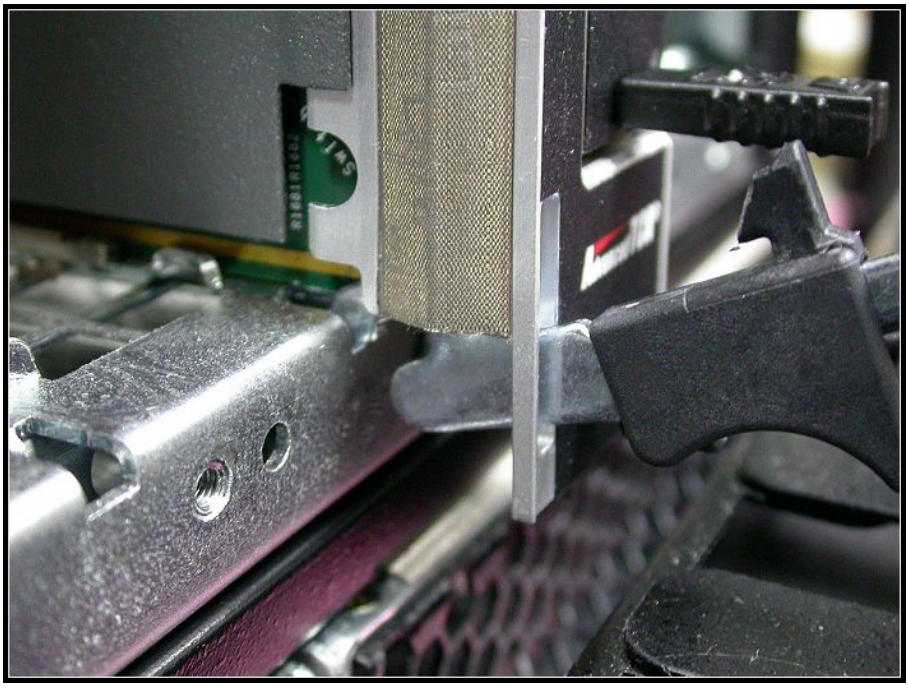
5.2 Installing and Removing the aTCA-6200 Blade

5.2.1 Installing the Blade

Follow the steps to install the aTCA-6200 blade to the chassis.

Step 1

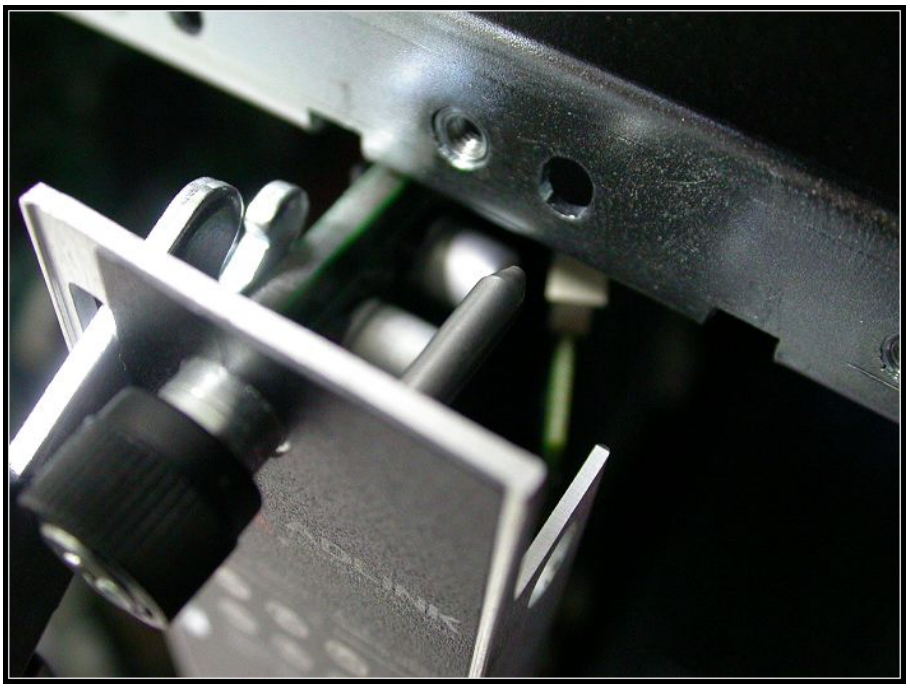
Carefully align the board edges with the chassis guide rails and push the blade inwards.



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Step 2

Check if the catch hooks and alignment pins at both ends of the module are correctly inserted into the proper openings. Push inwards on the handles until the blade is firmly seated in the chassis. (Do not force the handles if there is any abnormal resistance or it could damage the connectors and/or backplane.)

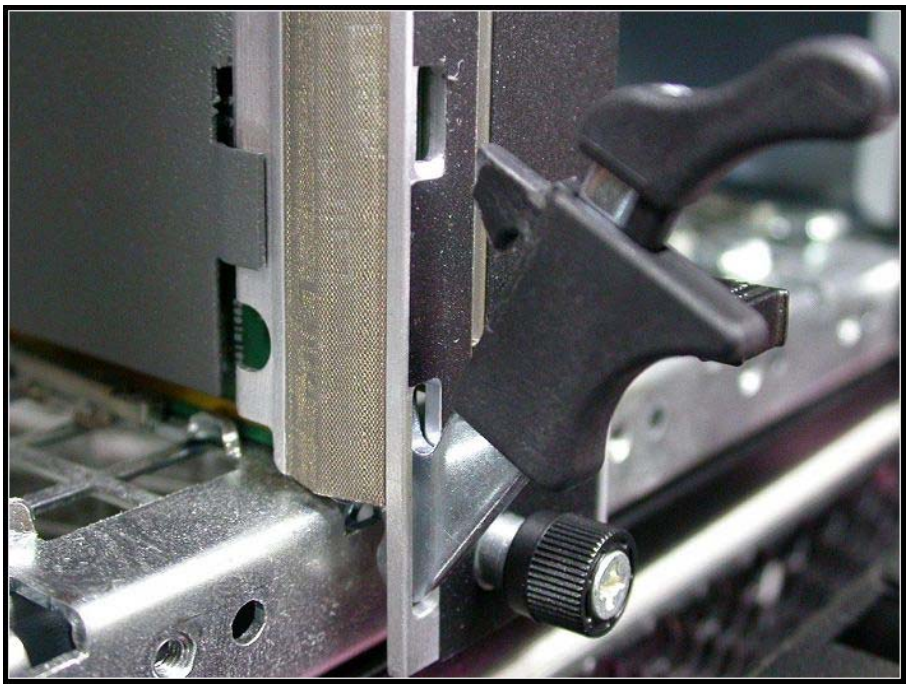


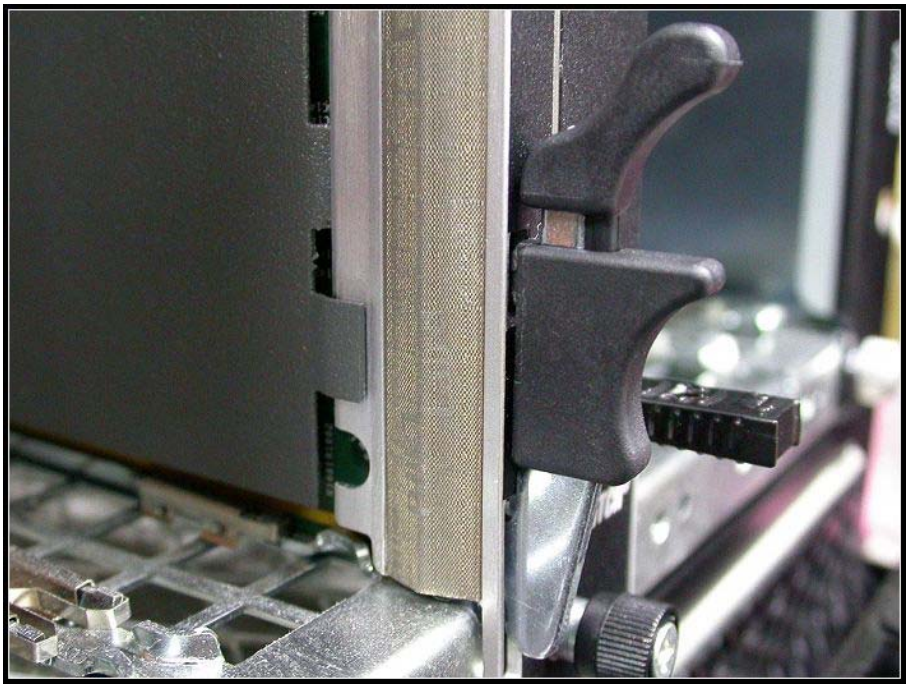


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Step 3

Push the ejector handles inwards until it is locked.





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Step 4

Lock both ends of the captive screws.



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5.2.2 Removing the Blade

Follow the steps to remove the aTCA-6200 blade from the chassis.

Step 1

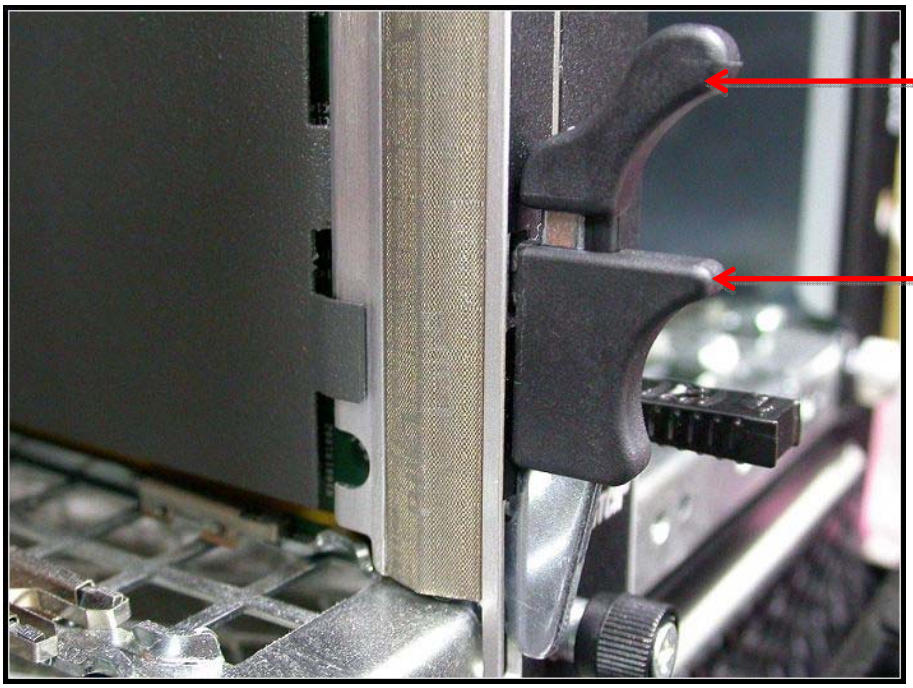
Unlock both ends of the captive screws.

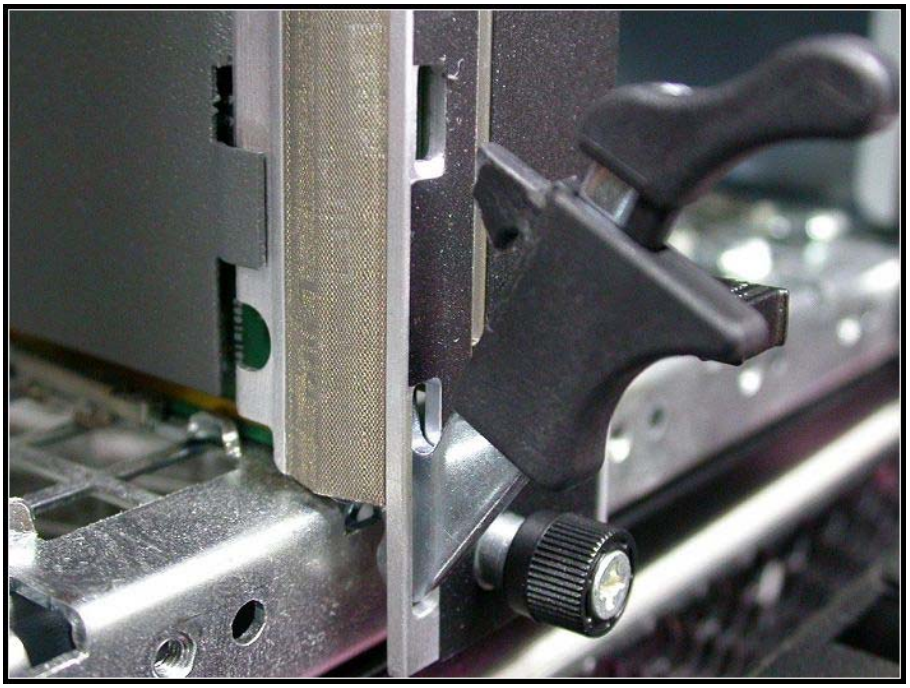


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Step 2

Pinch the lever and latch together then pull outwards to release the ejector handles at both ends.

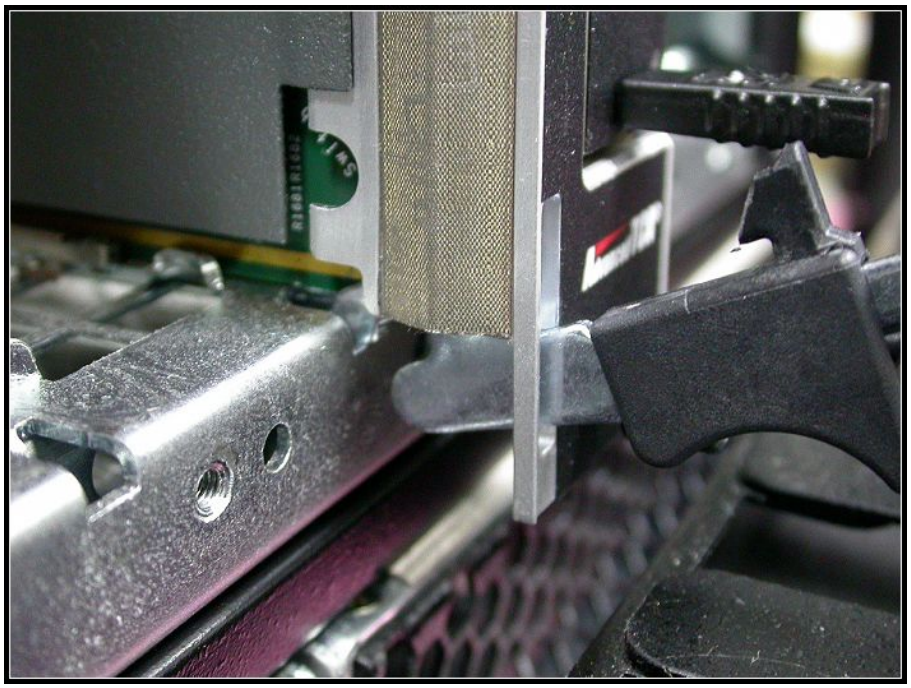




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Step 3

Pull the blade outwards from the chassis until it is removed.



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6 BIOS

This chapter outlines how to configure the BIOS setup items. A detailed description of each BIOS setup item in the following sections.

6.1 Entering the BIOS Setup Screen

To enter the setup screen, follow these steps:

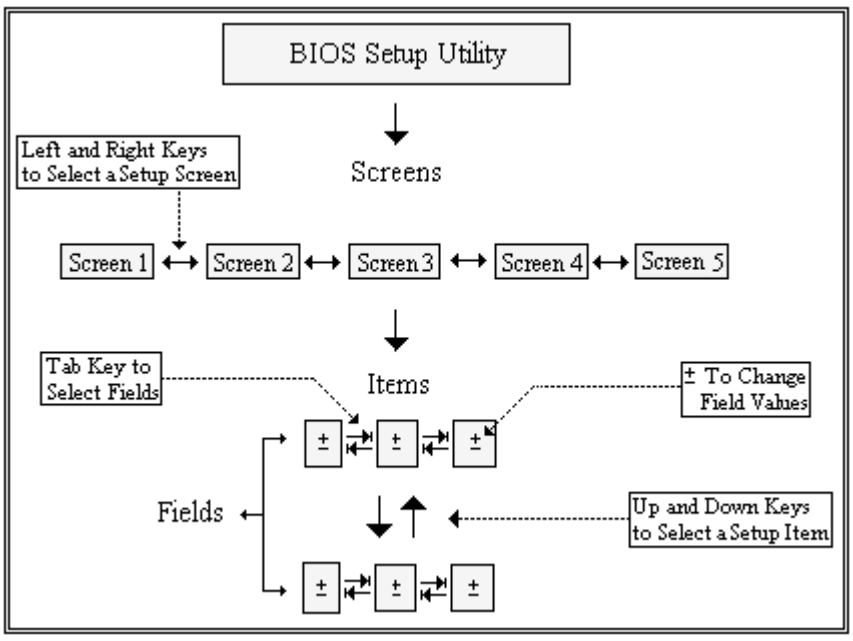
Step 1: Power on the aTCA-6200.
Step 2: Press the <S> key on a USB keyboard when you see the following text prompt on the boot up screen.

```
Version 2.14.1219. Copyright (C) 2011 American Megatrends, Inc.
BIOS Date: 10/22/2012 18:22:24 4.6.5.3 aTCA6200 REV:A1.2
Press <S> to enter setup.
```

Step 3: After pressing the <S> key, the Main BIOS setup menu will be displayed. You can access the other setup screens from the BIOS setup utility, such as CPU configuration, USB configuration, etc.

6.1.1 Navigation

The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process. These keys include <F1>, <F2>, <F3>, <F4>, <ESC>, <Enter>, <Arrow> keys, and so on.



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NOTE:	There is a hot key legend located in the right frame on most setup screens..
→←	Left/Right. The *Left and Right* < Arrow > keys allow you to select a setup screen.
↑↓	Up/Down The *Up and Down* < Arrow > keys allow you to select a setup item or sub-screen.
+-	Plus/Minus the *Plus and Minus* < Arrow > keys allow you to change the field value of a particular setup item. For example: Date and Time.
ESC	The < Esc > key allows you to discard any changes you have made and exit the Setup. Press the < Esc > key to exit the setup without saving your changes. Press the < Enter > key to discard changes and exit. You can also use the < Arrow > key to select *Cancel* and then press the < Enter > key to abort this function and return to the previous screen.
Enter	The < Enter > key allows you to display or change the setup option listed for a particular setup item. The < Enter > key can also allow you to display the setup sub-screens.

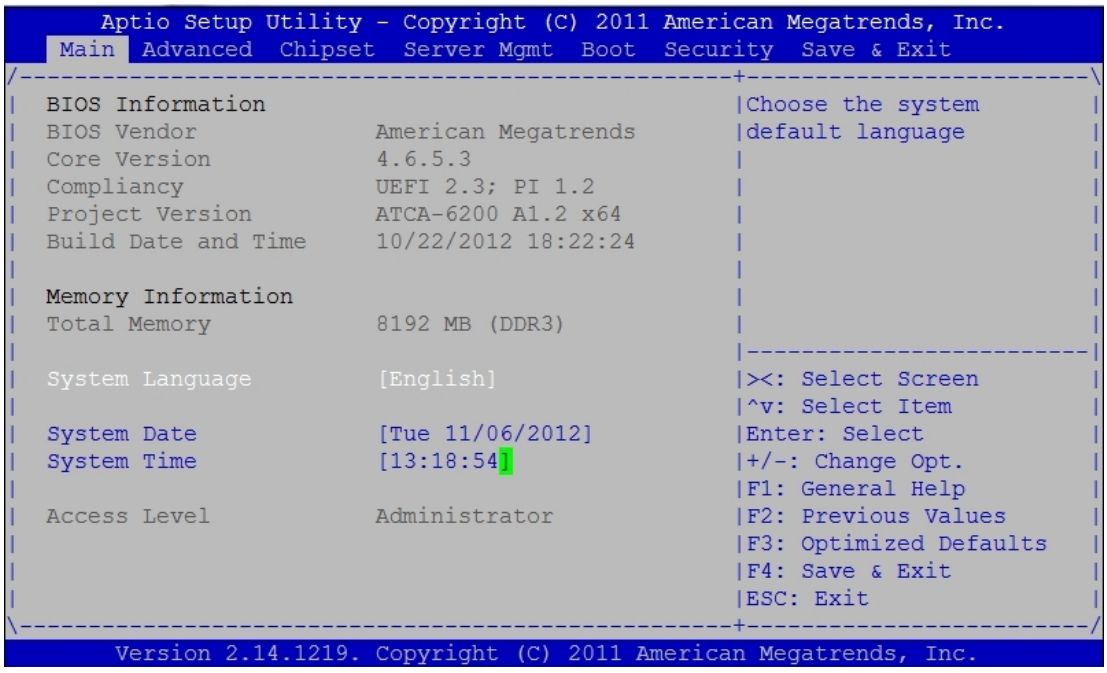
6.2 Main BIOS Setup Screen

The Main BIOS setup menu is the screen where you start navigation of the BIOS setting menus. You can always return to the Main setup screen by selecting the Main tab. Each BIOS setup menu option is described in the following sections.

There are two parts of the Main BIOS setup menu screen. The left part of the screen displays the available options. The user can configure the options in blue text. The selected option will appear highlighted in white text. Options in gray text are for information only

The upper right part of the screen displays the description of the selected option. The lower right part of the screen shows the navigation keys that user can use.

The Main setup screen is shown below.



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System Language

Currently, only “English” is supported on the aTCA-6200.

System Time/System Date

Use these two options to change system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values using the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.



The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

System & Board Information

The Main BIOS setup screen reports memory and board information.

BIOS Vendor

Reports the BIOS vendor of aTCA-6200’s BIOS. American Megatrend, Inc. is the BIOS vendor that aTCA-6200 is using.

Core Version

Shows which core version is used from AMI to develop the aTCA-6200’s BIOS.

Compliancy

Shows which version of EFI specification is compliant with the aTCA-6200’s BIOS.

BIOS Revision

Shows the revision of the aTCA-6200’s BIOS.

Build Date and Time

Shows the date and time that the aTCA-6200 BIOS was released.

Total Memory

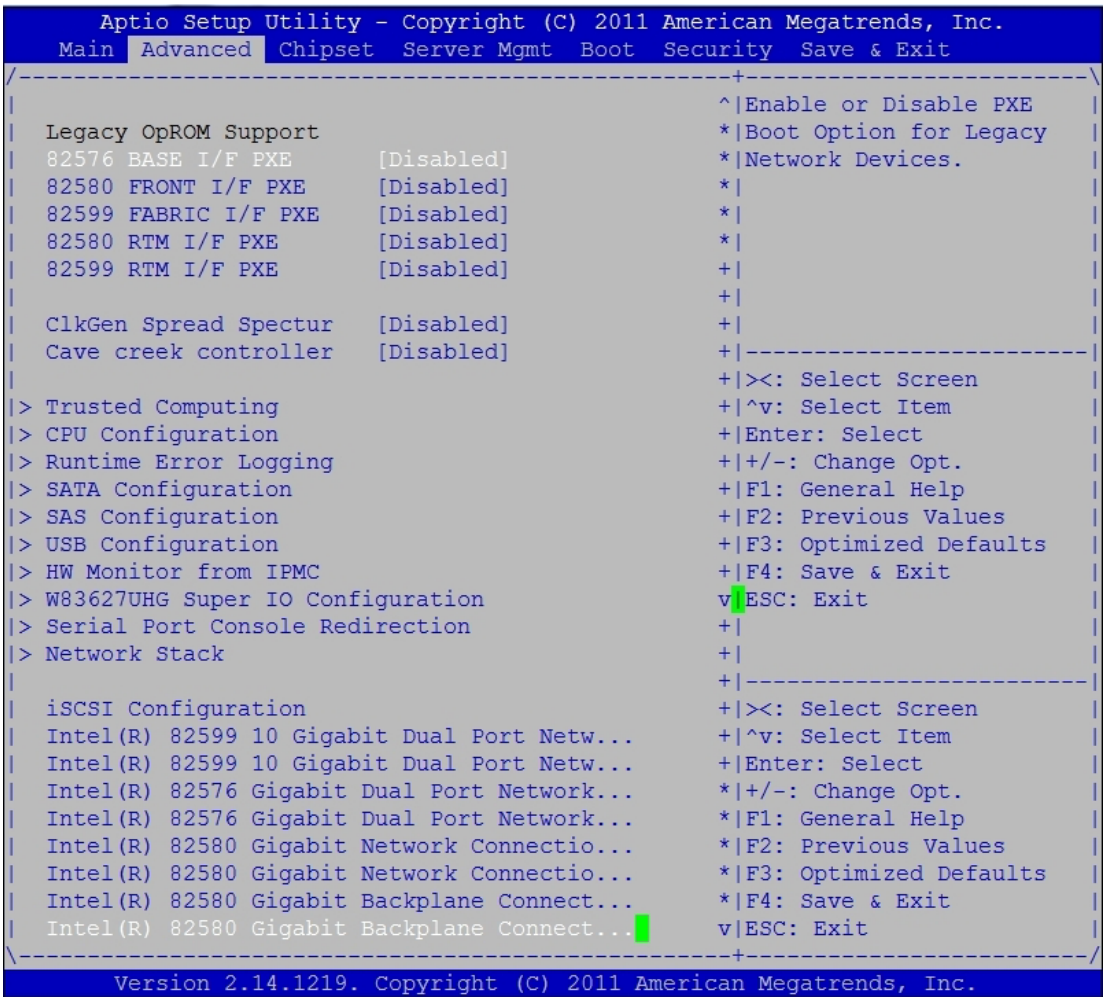
Shows the memory size of the aTCA-6200.

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6.3 Advanced Setup Screen

Select the ***Advanced*** tab from the setup screen to enter ***Advanced*** BIOS setup screen. You can select any of items in the left frame of the screen, such as CPU configuration, to go to the sub menu for that item. You can select an ***Advanced*** BIOS sub menu or option by highlighting it using the <Arrow> keys. The Advanced BIOS setup screen is shown below.

The sub menus are described in the following sections.



82576/82580/82599 PXE OpROM

These options can be configured to invoke Ethernet's PXE ROM on BASE/FRONT/RTM/FRABRIC interface. When it is set to disabled, system will boot without PXE ROM. Options: **Enabled/Disabled**.

ClkGen Spread Specturm

This option can enable or disable Clockgen spread specturm. Options: **Enabled/Disabled**.

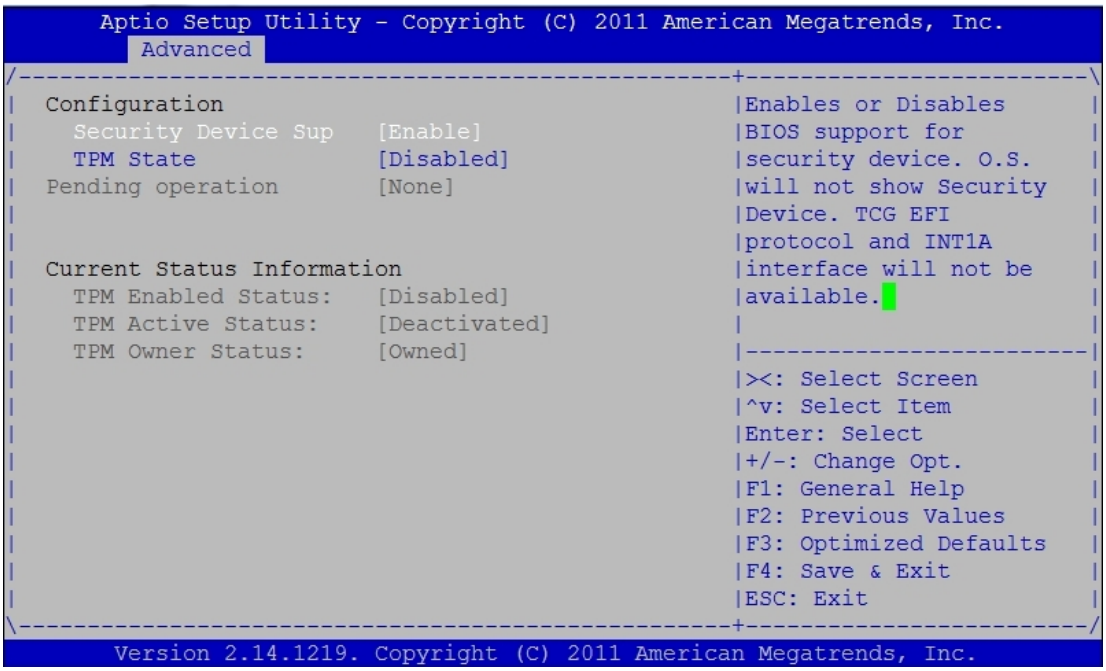
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Cave creek controller

This option can enable or disable cave creek devices. Options: **Enabled/Disabled**.

6.3.1 Trusted Computing

Trusted computing is an industry standard to make personal computers more secure through a dedicated hardware chip, called a Trusted Platform Module (TPM). This option allows enabling or disabling the TPM support.



Security Device Support

This item allows you to enables or disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available. Options: **Enabled/Disabled**.

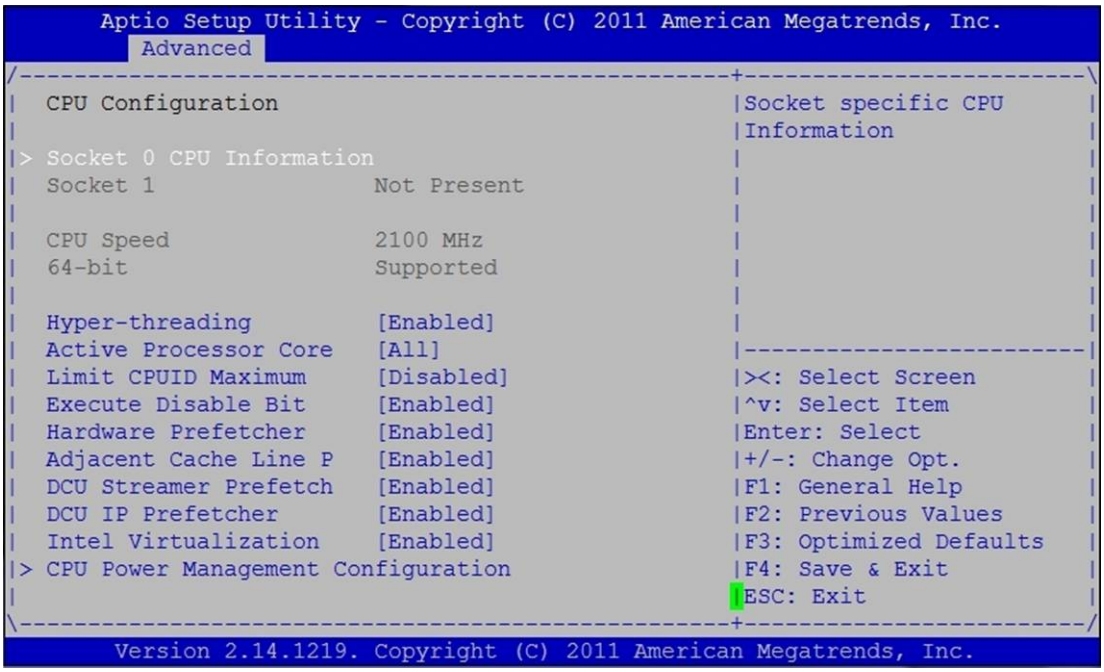
TPM State

This item allows you to enables or disables Security Device. NOTE: Your Computer will reboot during restart in order to change State of the Device. Options: **Enabled/Disabled**.

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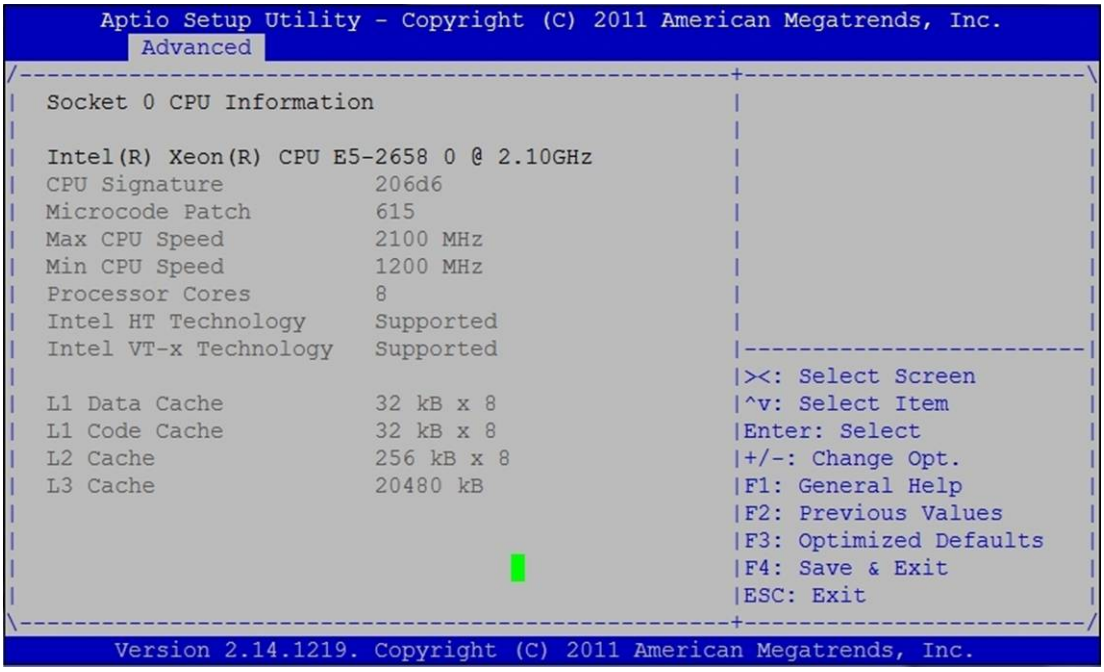
6.3.2 CPU Configuration

You can use this screen to select options for the CPU configuration settings. Use the up and down <Arrow> keys to select an item. Use the <+> and <-> keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the CPU configuration screen is shown below.



6.3.2.1 Socket 0/1 CPU Information

BIOS will show the information of detected CPU, like CPU speed and its supported feature. Detailed information will also be listed in each socket CPU information sub menu like below. User can select “Socket 0” or “Socket 1” information for more detailed understanding of what CPU is using on system.



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Hyper-threading

This item allows you to enable or disable the Hyper-Threading technology. Options: **Enabled/Disabled**.

Active Processor Core

This item allows you to select the number of cores to enable in each processor package. This BIOS setting is present only when a multi-core processor is installed.

Limit CPUID Maximum

When the computer is booted up, the operating system executes CPUID instruction to identify the processor and its capabilities. Before it can do so, it must first query the processor to find out the highest input value CPUID recognizes. This determines the kind of basic information CPUID can provide the operating system. This option allows you to circumvent problems with older operating systems that do not support Intel Pentium 4 processor with Hyper-Threading Technology.

When **Enabled**, the processor will limit the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When **Disabled**, the processor will return the actual maximum CPUID input value of the processor when queried. Options: **Enabled/Disabled**.

Execute Disable Bit

Intel's Execute Disable Bit functionality can help prevent certain classes of malicious buffer overflow attacks when combined with a supporting operating system. Execute Disable Bit allows the processor to classify areas in memory by where application code can execute and where it cannot. When a malicious worm attempts to insert code in the buffer, the processor disables code execution and prevents damage and worm propagation.

Hardware Prefetcher

This is used for reducing the waiting time of DRAM. The hardware prefetcher looks for streams of data and tries to predict what data will be needed next by the processor and proactively tries to fetch these data. Options: **Enabled/Disabled**.

Adjacent Cache Line P

It is opened for choose the optimal use of sequential memory access for performance purpose. Disable this setting for the application that requires high use of random memory access. Options: **Enabled/Disabled**.

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DCU Streamer Prefetch

There are two distinct hardware prefetchers on aTCA-6200. Data Cache Unit (DCU) streamer prefetcher and Data Cache Unit (DCU) IP-prefetcher. DCU streamer prefetchers detect multiple reads to a single cache line in a certain period of time and choose to load the following cache line to the L1 data caches.
This option allows user to enable or disable DCU streamer Prefetcher.

DCU IP Prefetcher

DCU IP Prefetcher looks for sequential load history to determine whether to prefetch the data to the L1 caches.

This option allows user to enable or disable DCU IP Prefetcher.

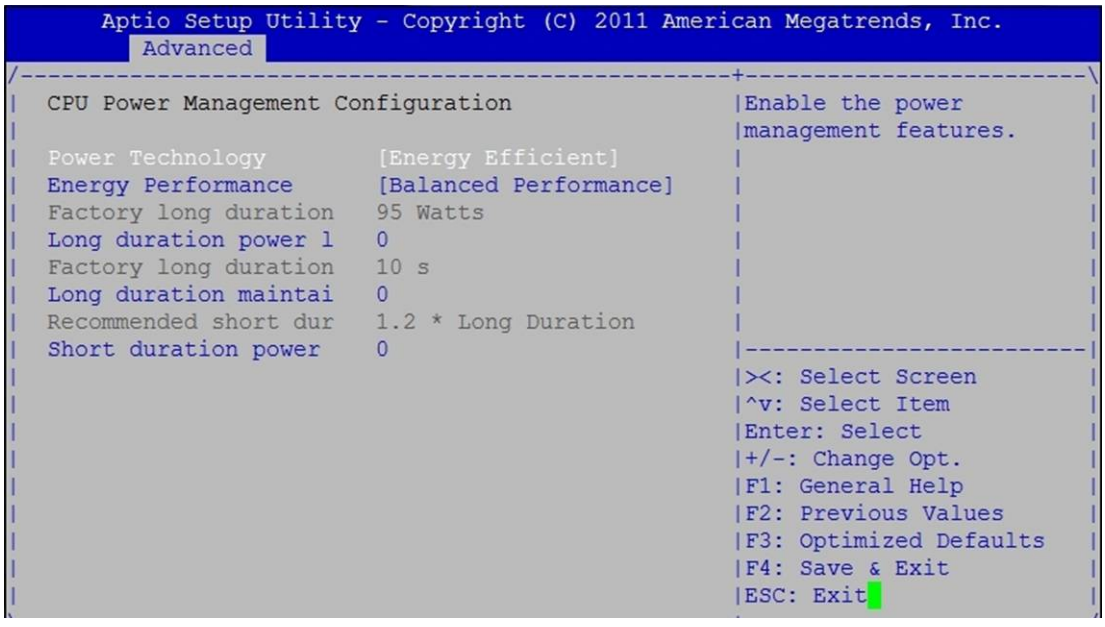
Intel Virtualization

Intel Virtualization Technology consists of components that support virtualization of platforms based on Intel processors, thereby enabling the running of multiple operating systems and applications in independent partitions. Each partition behaves like a virtual machine (VM) and provides isolation and protection across partitions.

Intel VT requires the use of a processor with Intel VT support. Additionally, a third-party VMM may also be required. Options: **Enabled/Disabled**.

6.3.2.2 CPU Power Management Configuration

CPU Power Management configuration opens some item for adjusting the load or timing to reduce the power consumption. User can go to this setup page to configure the best setting for the whole system.



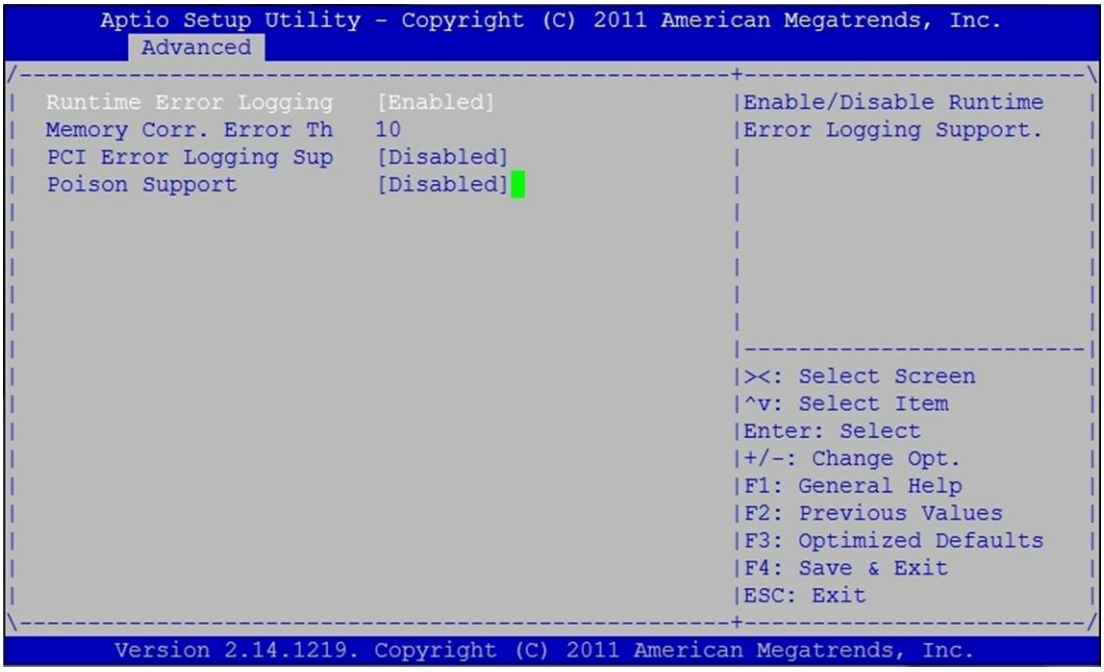
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Power Technology
This item enables the power management features.

Energy Performance
This item is designed for configuring the energy performance.

6.3.3 Runtime Error Logging

You can use this screen to specify options for the runtime error logging settings. Use the up and down <Arrow> keys to select an item. Use <+> and <-> keys to change the value of the selected option. The settings are described in the following pages. The screen is shown as below.



Runtime Error Logging

This option allows user to enable or disable runtime error logging.

Memory Corr. Error Th

This option is for setting memory correctable error threshold value.

PCI Error Logging Sup

This option is for enabling or disabling PCI error logging.

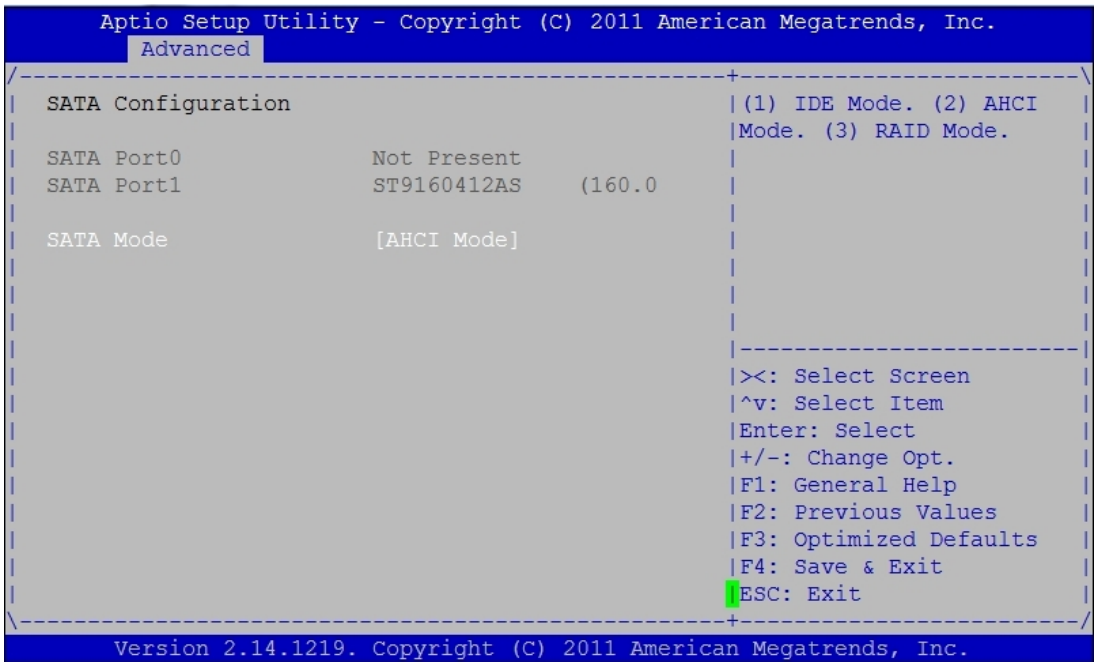
Poison Support

This option is for enabling or disabling Poison support. When poisioning is enabled, CPU doesn’t singal the uncorrectable error via MCERR but may signal CMCI if CMCI is enabled.

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6.3.4 SATA Configuration

You can use this screen to specify options for the SATA configuration settings. Use the up and down <Arrow> keys to select an item. Use <+> and <-> keys to change the value of the selected option. The settings are described in the following pages. The screen is shown as below.



SATA Mode

This option is designed for configuring SATA mode. It can be Disabled, IDE Mode and AHCI Mode.

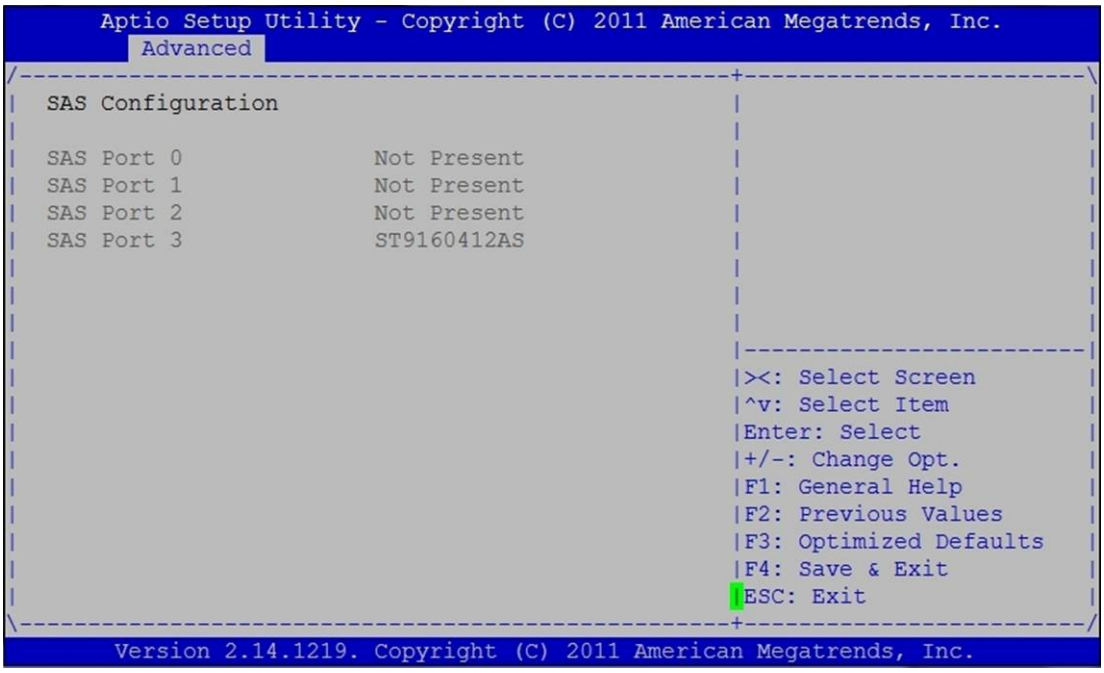
Aggressive Link Power

It allows enabling or disabling Aggressive Link Power for SATA.

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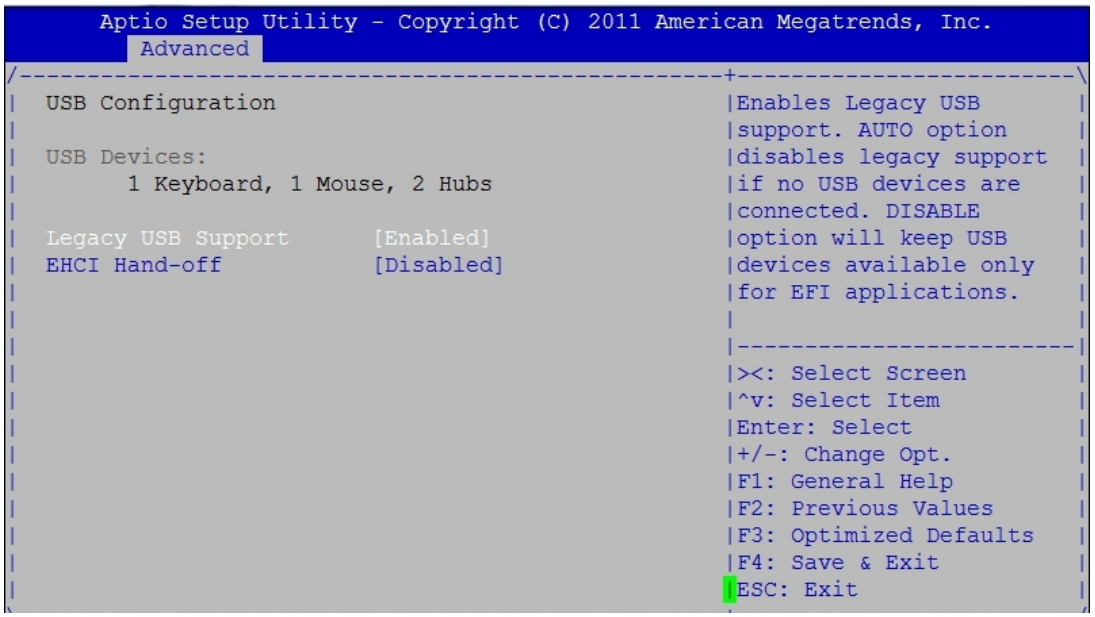
6.3.5 SAS Configuration

You can use this screen to view the current SAS configuration. The SAS device is shown dynamically when system boot. The SAS option will detect the existed drive and then show them on this setup screen. User can check the result of detection from this screen. The screen is shown as below.



6.3.6 USB Configuration

You can use this screen to specify options for the USB configuration settings. Use the up and down <Arrow> keys to select an item. Use <+> and <-> keys to change the value of the selected option. The settings are described in the following pages. The screen is shown as below.



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Legacy USB Support

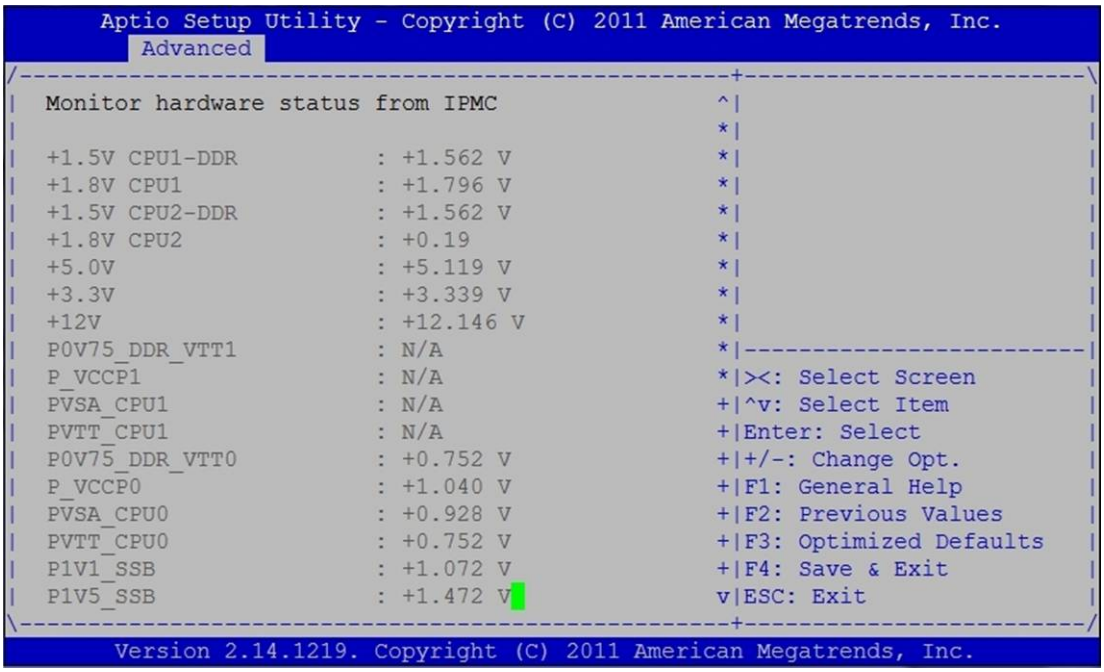
Legacy USB support refers to USB mouse and keyboard support. If this option is not enabled, any attached USB mouse or keyboard will not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or keyboard can control the system even there is no USB driver loaded on the system.

EHCI Hand-off

This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

6.3.7 HW Monitor from IPMC

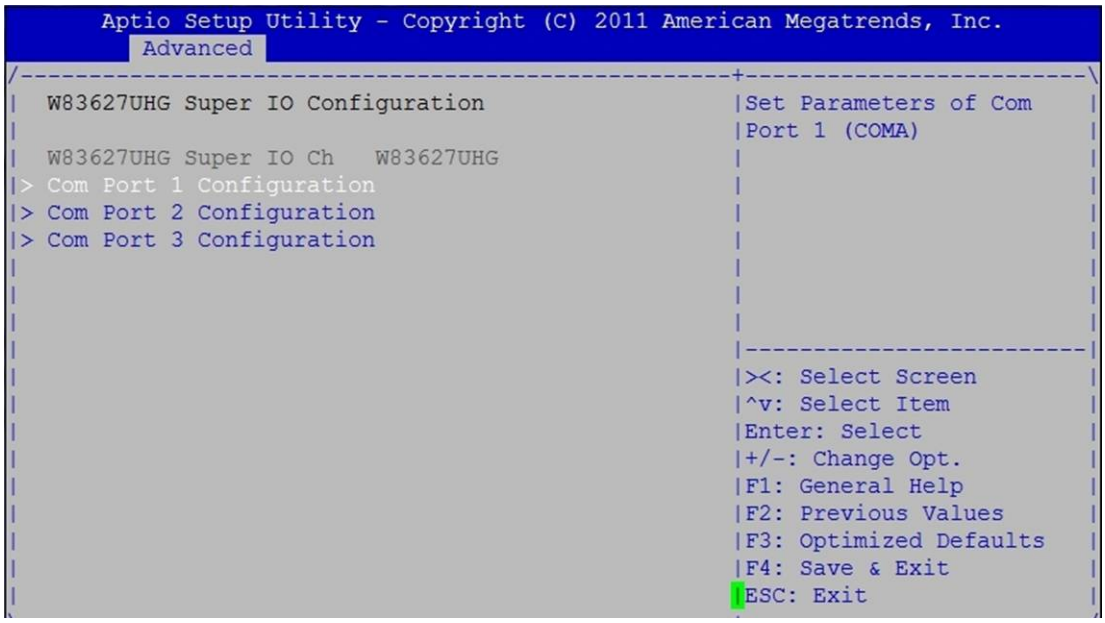
You can use this screen to check hardware status from IPMC. Use the up and down <Arrow> keys to move. The screen is shown as below.



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6.3.8 W83627UHG SIO Configuration

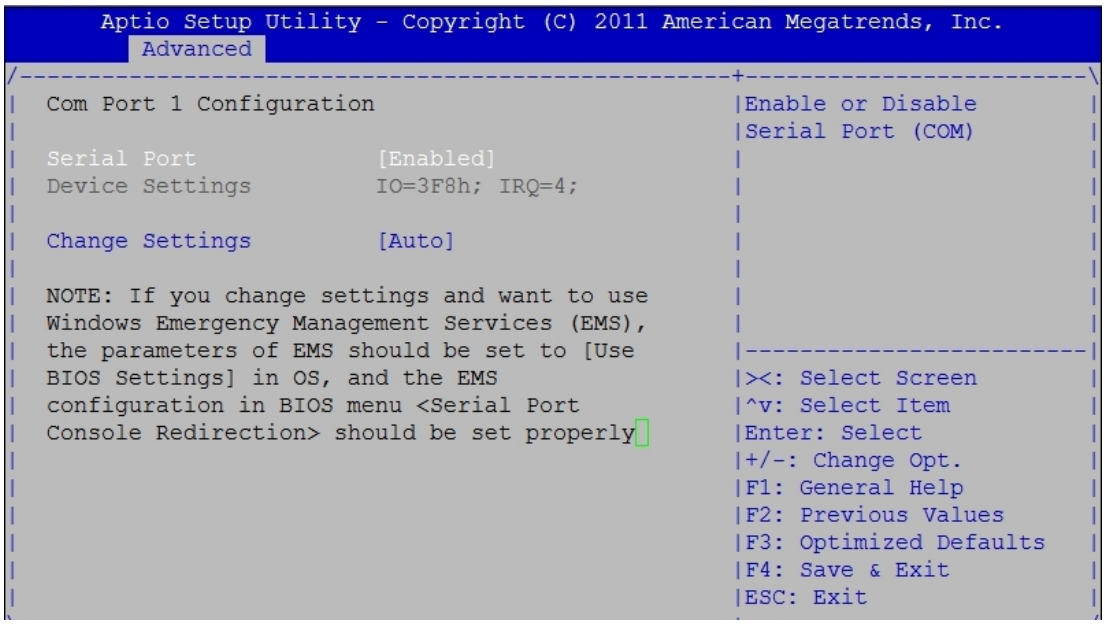
You can use this screen to specify options for the Super IO configuration settings. Use the up and down <Arrow> keys to select an item. Use <+> and <-> keys to change the value of the selected option. The settings are described in the following pages. The screen is shown as below.



Winbond W83627UHG is designed on aTCA-6200. When system boot, BIOS will detect superIO and show the name on this screen.

6.3.8.1 COM Port 1/2/3 Configuration

The settings on this setup screen can let users set parameters of com port 1/2/3, The screen is shown as below



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Serial Port

This item is designed for enabling/disabling the serial ports.

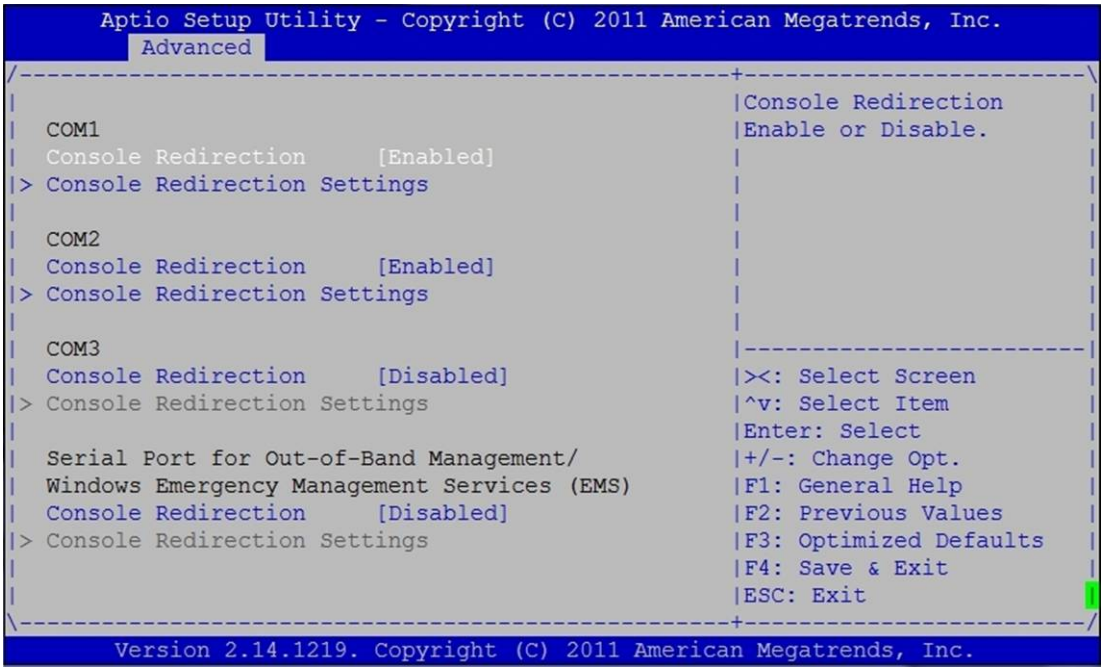
Change Settings

This item is designed for setting I/O and IRQ for the serial ports.

NOTE: If you change settings and want to use Windows Emergency Management Services (EMS), the parameters of EMS should be set to [Use BIOS Settings] in OS, and the EMS configuration in BIOS menu <Serial Port Console Redirection> should be set properly"

6.3.9 Serial Port Console Redirection

The settings on this setup screen specify how the host computer and the remote computer (which the user is using) exchange data. Both computers should have the same or compatible settings, like baud rate, terminal type, and so on.



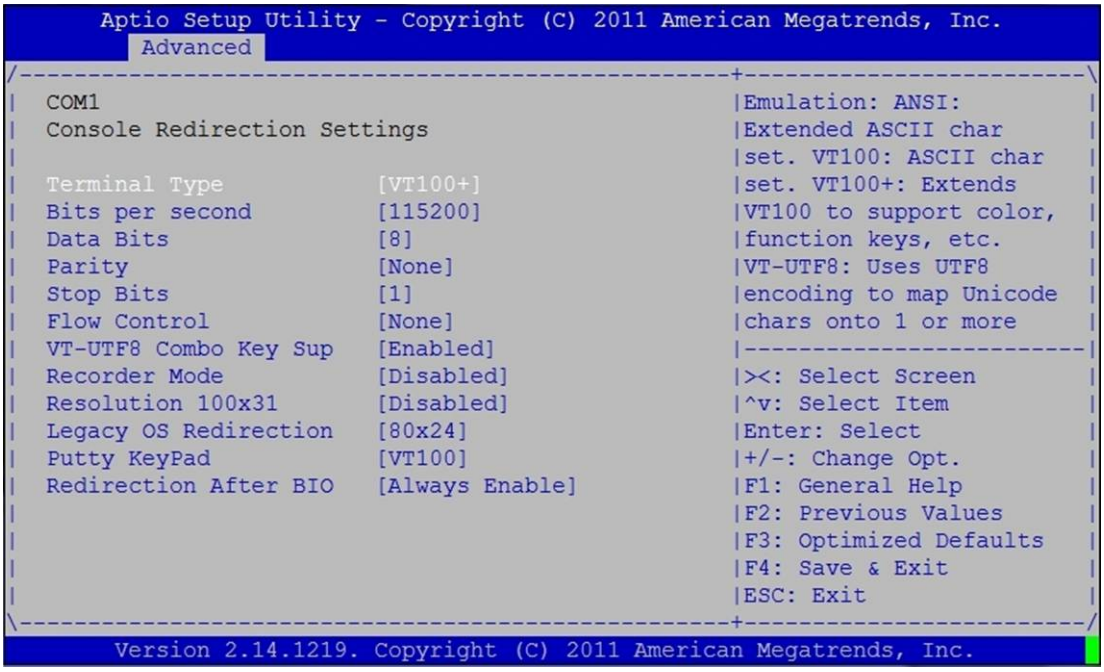
Console Redirection

This item is designed for enabling/disabling the serial ports redirection.

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6.3.9.1 Console Redirection settings (COM1/2/3)

When console redirection is set to enable, the below screen will be needed to set properly for communicating with other computer that is using terminal software to receive the message from aTCA-6200.



Terminal Type

Select the terminal type: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.".

Bits per second

Select the bits per second that you want serial port to use for console redirection.

Data Bits

This option allows to select the data bits you want the serial port to use for console redirection.

Parity

Set this option to select Parity for console redirection.

Stop Bits

Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may requires more than 1 stop bit.

Flow Control

Set this option to select Flow control for console redirection.

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VT-UTF8 Combo Key Sup

This option is used for enabling or disabling VT-UTF8 Combo key.

Recorder Mode

This option is used for enabling or disabling Recorder Mode.

Resolution 100x31

This option is used for enabling or disabling resolution 100x31 support.

Legacy OS Redirection

This option is used for configuring the legacy OS text format for proper display if system boots to legacy OS with console redirection enabled.

Putty KeyPad

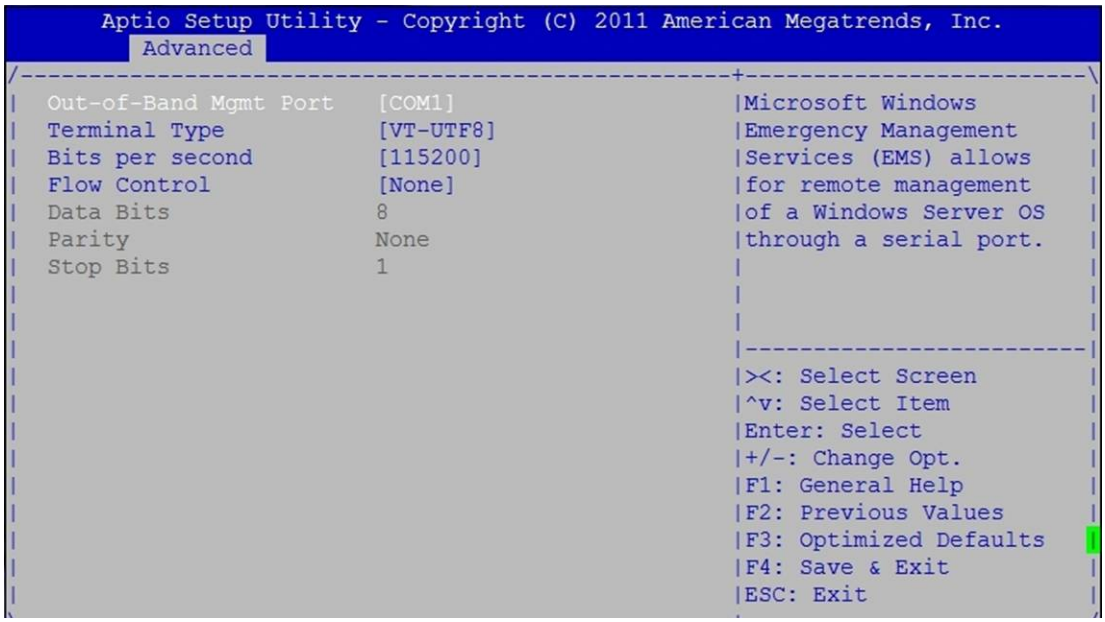
This option allows configuring the format of keypad when console redirection is enabled.

Redirection After BIOS

This option allows user to configure the console redirection mode via serial port after BIOS POST OK.

6.3.9.2 Console Redirection settings (EMS)

Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port. The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.



Out-of-Band Mgmt Port

Set this option to select which serial port will be used for EMS.

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Terminal Type
VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100.

Bits per second
Select the bits per second that you want serial port to use for console redirection.

Flow Control
Set this option to select Flow control for console redirection.

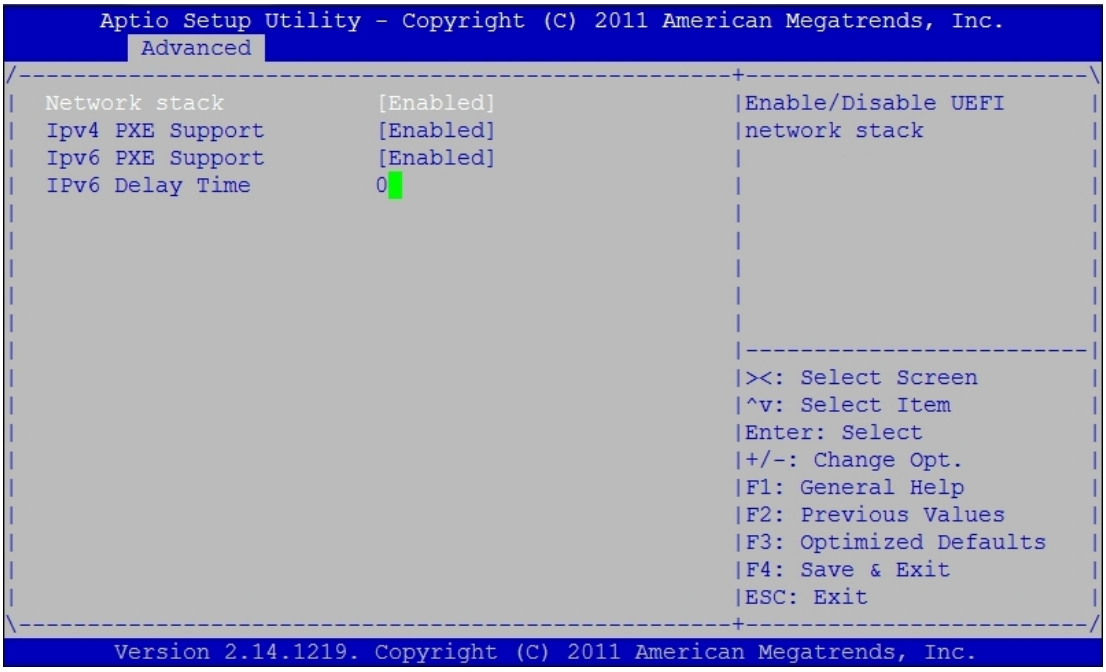
Data Bits
This option allows to select the data bits you want the serial port to use for console redirection.

Parity
Set this option to select Parity for console redirection.

Stop Bits
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may requires more than 1 stop bit.

6.3.10 Network Stack

You can use this screen to specify options for the Network Stack settings.
The screen is shown as below.



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Network Stack
This option is used for enabling or disabling UEFI network stack for onboard Ethernet.

Ipv4 PXE Support
This option is used for enable Ipv4 PXE boot support. If disabled IPV4 PXE boot option will not be created.

Ipv6 PXE Support
This option is used for enable Ipv6 PXE boot support. If disabled IPV4 PXE boot option will not be created.

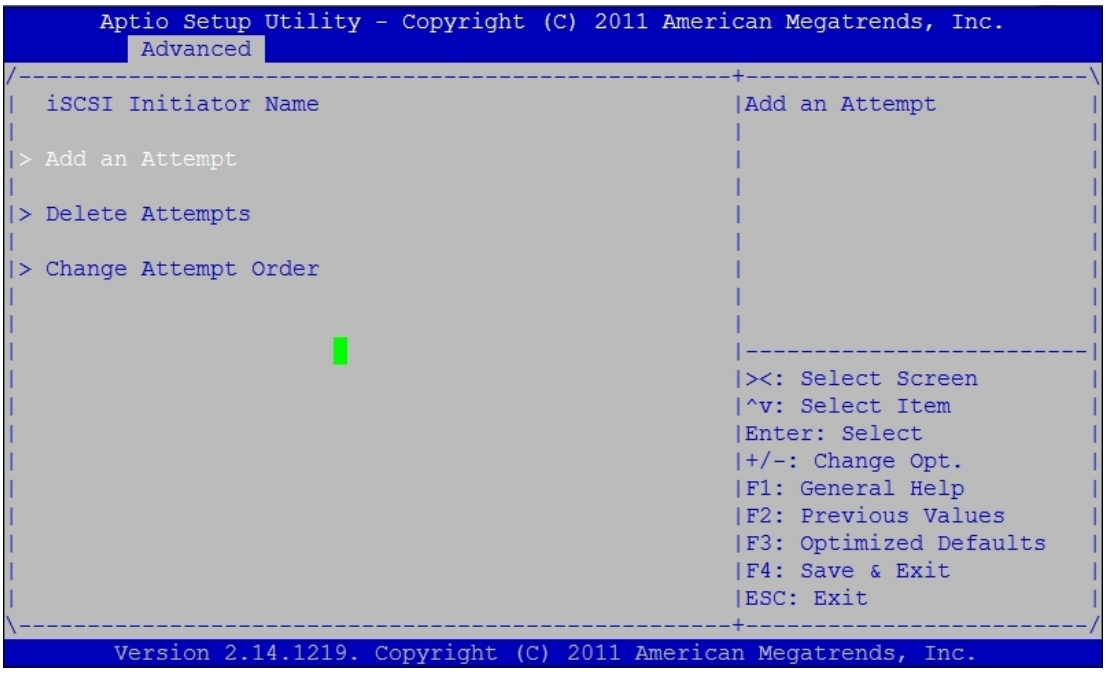
NOTE: The Network stack PXE boot supports EFI boot only.

IPv6 Delay Time
This option is used for set seconds of delay before IPv6 PXE boot.

6.3.11 iSCSI Configuration

You can use this screen to specify options for the iSCSI settings, The screen is shown as below.

NOTE: if you want to use iSCSI function, you have to enable Network Stack function first, and the iSCSI function provided here is for EFI boot only.



iSCSI Initiator Name

You can use this option to set iSCSI initiator name, only IQN format is accepted.

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Add an Attempt

You can use this option to add one iSCSI setting at a time, and BIOS can use these settings to connect iSCSI targets.

Delete Attempts

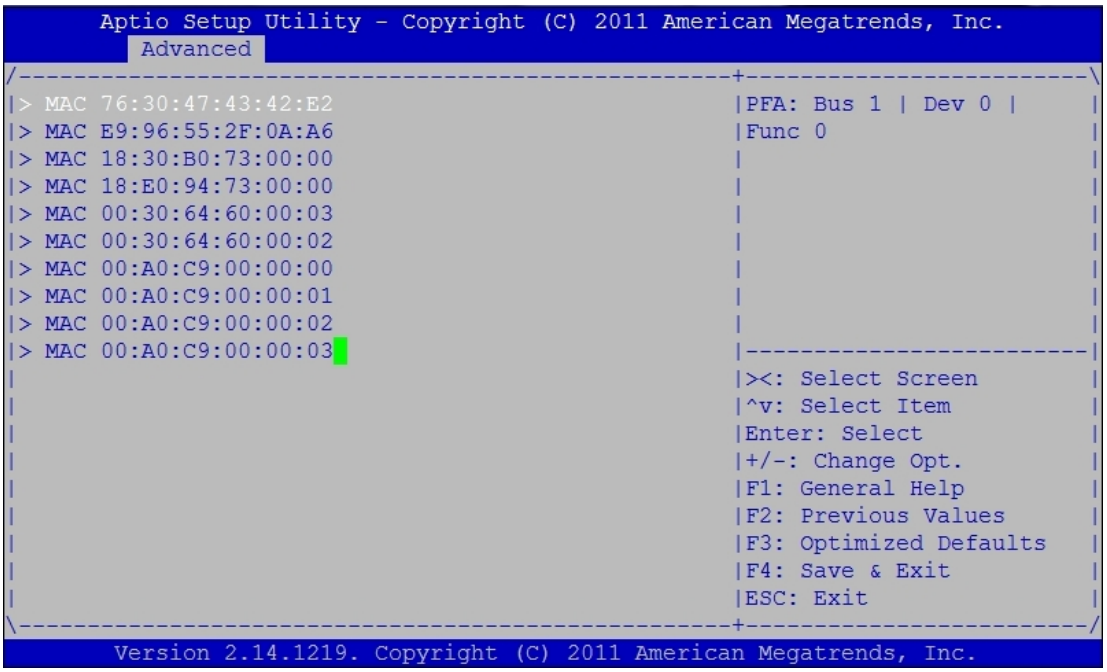
You can use this option to delete one or more iSCSI settings.

Change Attempt Order

You can use this option to change the order of iSCSI settings.

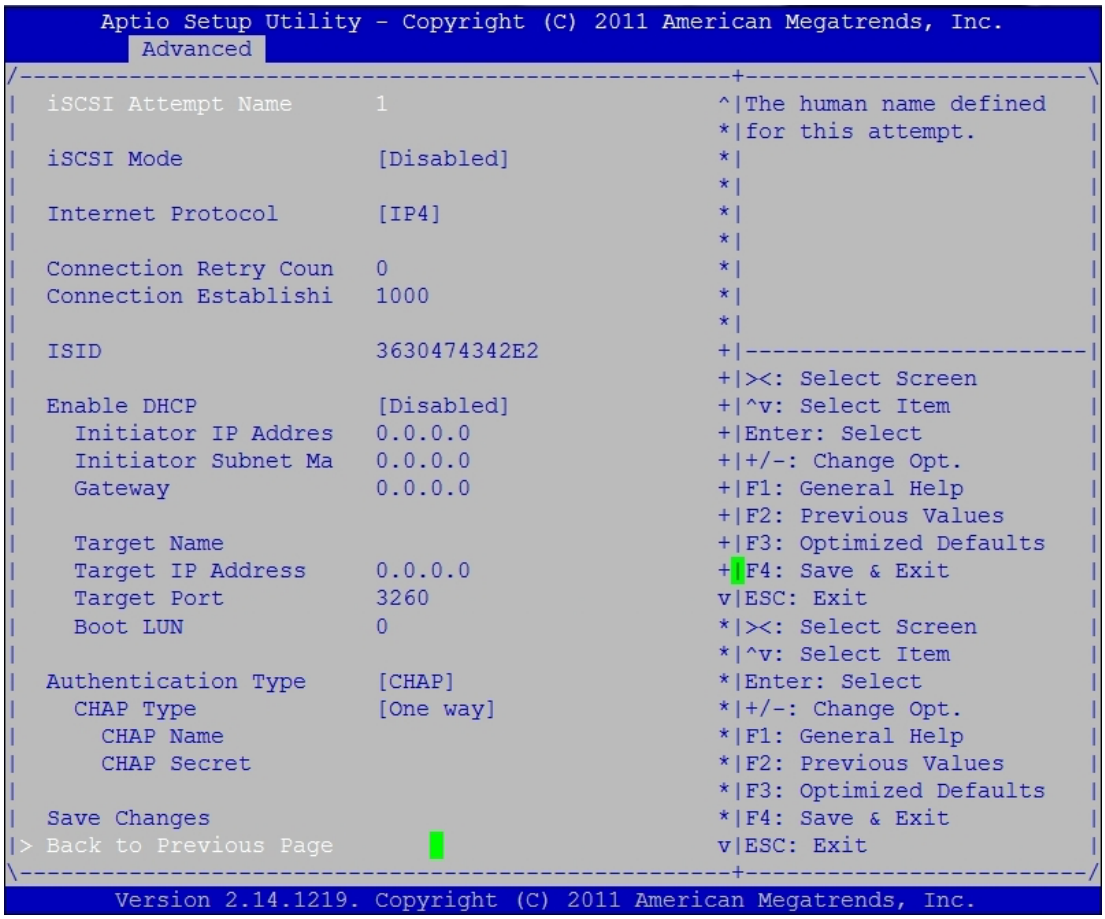
6.3.11.1 Add an Attempt

You can use this screen to select the Ethernet port that you want to configure. The screen is shown as below.



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After select the Ethernet port, you can set the iSCSI and other parameters. The screen is shown as below.



iSCSI Attempt Name

You can define the attempt name by this option.

iSCSI Mode

You can use this option to enable or disable iSCSI function for the corresponding port.

Internet Protocol

You can choose IPv4 or IPv6 protocol for the corresponding port.

Connection Retry Count

You can use this option to set retry number from 0 to 16, 0 means no retry.

Connection Establishment Time Out

You can use this option to set timeout value in milliseconds, the minimum value is 100 milliseconds and the maximum value is 20 seconds.

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ISID

This value is derived from MAC address, you can update it by input the last 3 bytes.

Enable DHCP

You can use this option to enable or disable DHCP in Initiator, if you disable it, then the IP address and other parameters should be setting properly.

Target Name

You can use this option to set iSCSI target name. Only iqn. format is accepted, this parameter should be the same with iSCSI target/server settings.

Authentication Type

You can use this option to choose authentication method, this parameter should be the same with iSCSI target/server settings.

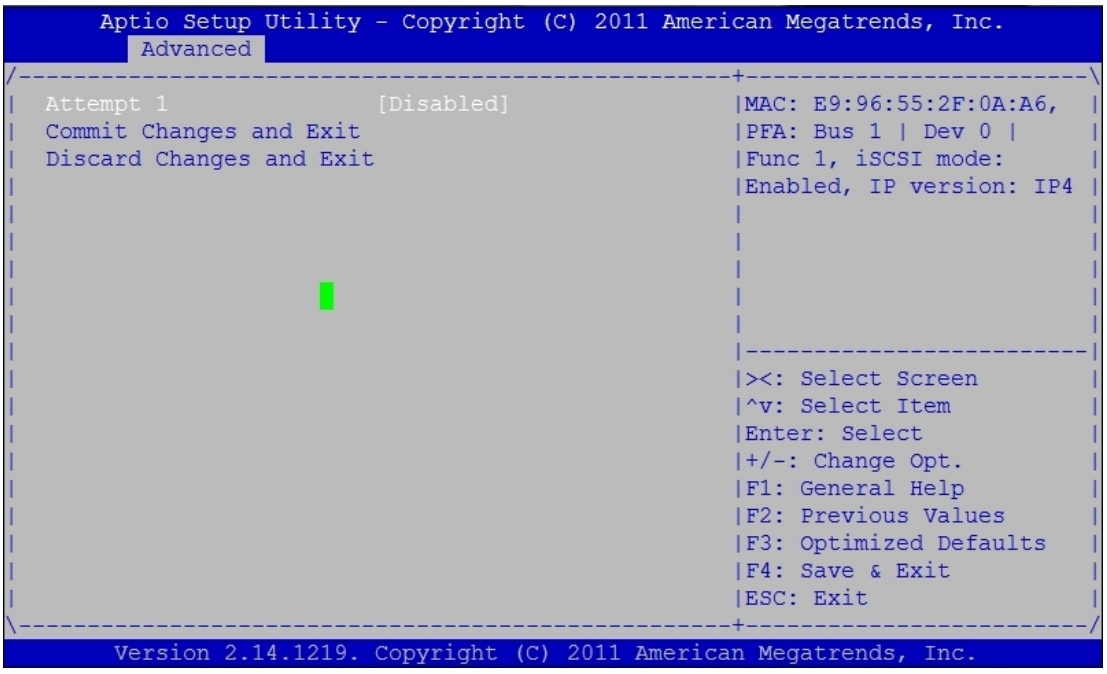
Save Changes

After parameters are set, you can save changes. Note: If you go to other pages without “save changes” in here, the parameters will not be saved.

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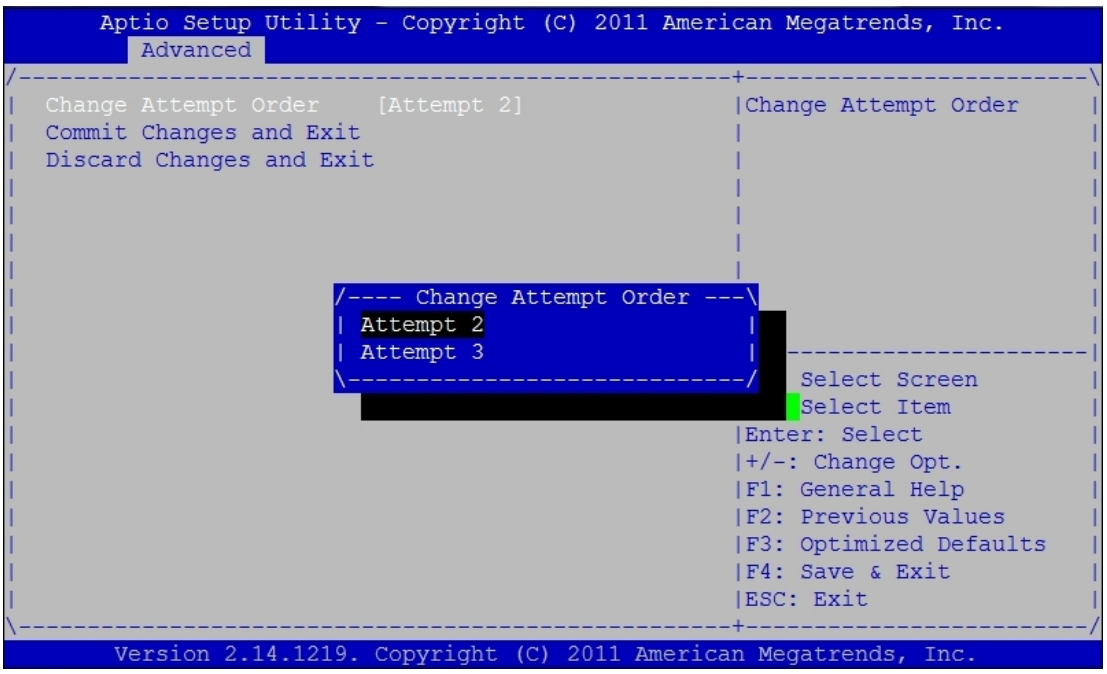
6.3.11.2 Delete Attempts

After add an attempt in previous page, you can delete it as well, The screen is shown as below. If you need to delete an attempt, set “enabled” in attempt that you want to delete, and select “Commit Changes and Exit”, then go back to previous page, you can check the attempt is deleted or not.



6.3.11.3 Change Attempt Order

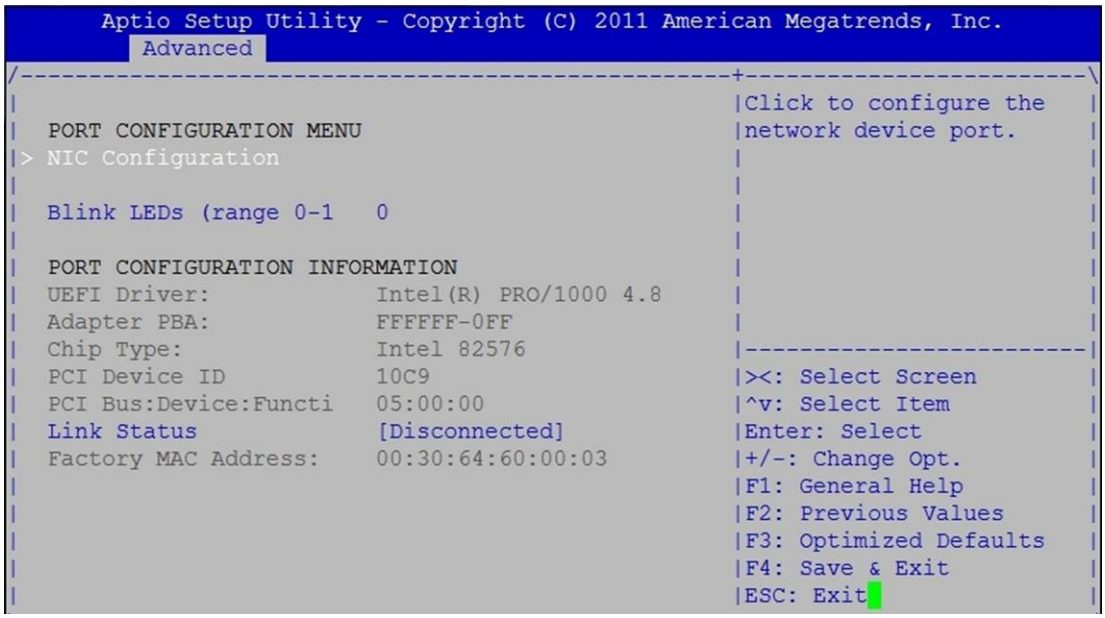
The function provided here is to let users change the order of attempts. The screen is shown as below.



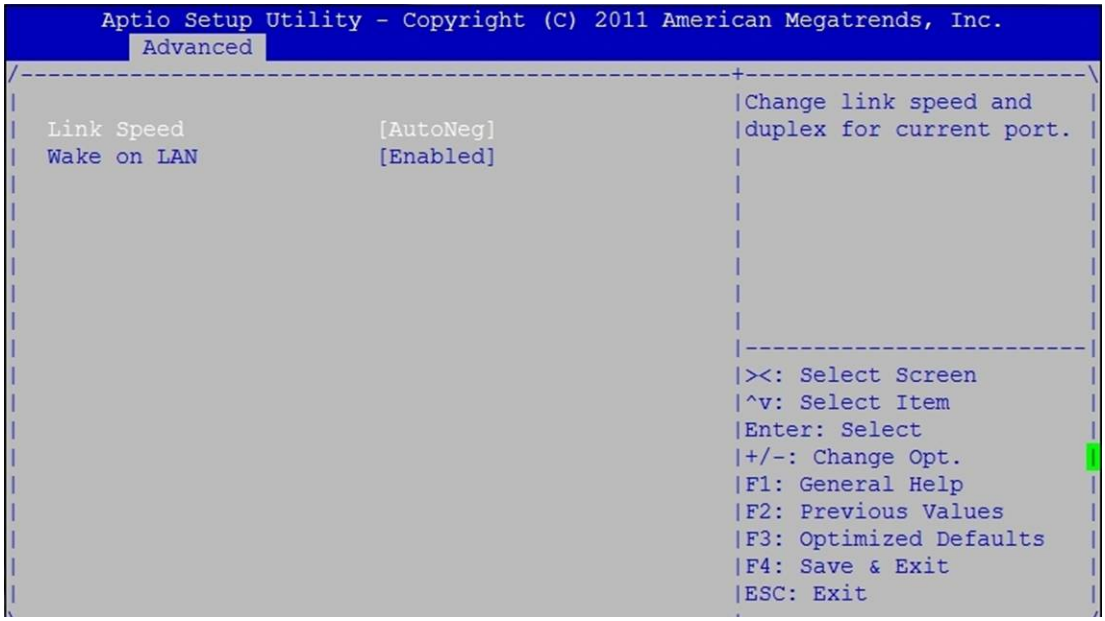
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6.3.12 Intel Ethernet Port Configuration

You can use this screen to view the Ethernet device information, like chip type, device ID, MAC address, and so on. The screen is shown as below.



6.3.12.1 NIC Configuration



Link Speed

This option allows user to change link speed and duplex for the current Ethernet port that user is configuring.

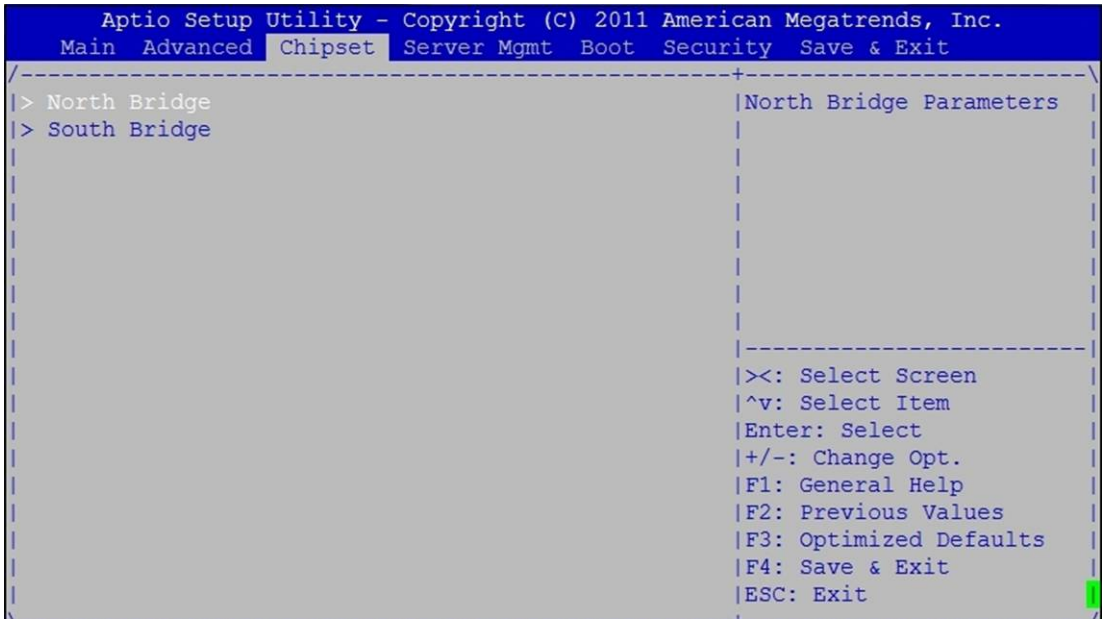
Wake on LAN

This option allows user to enable or disable wake the system with a magic packet.

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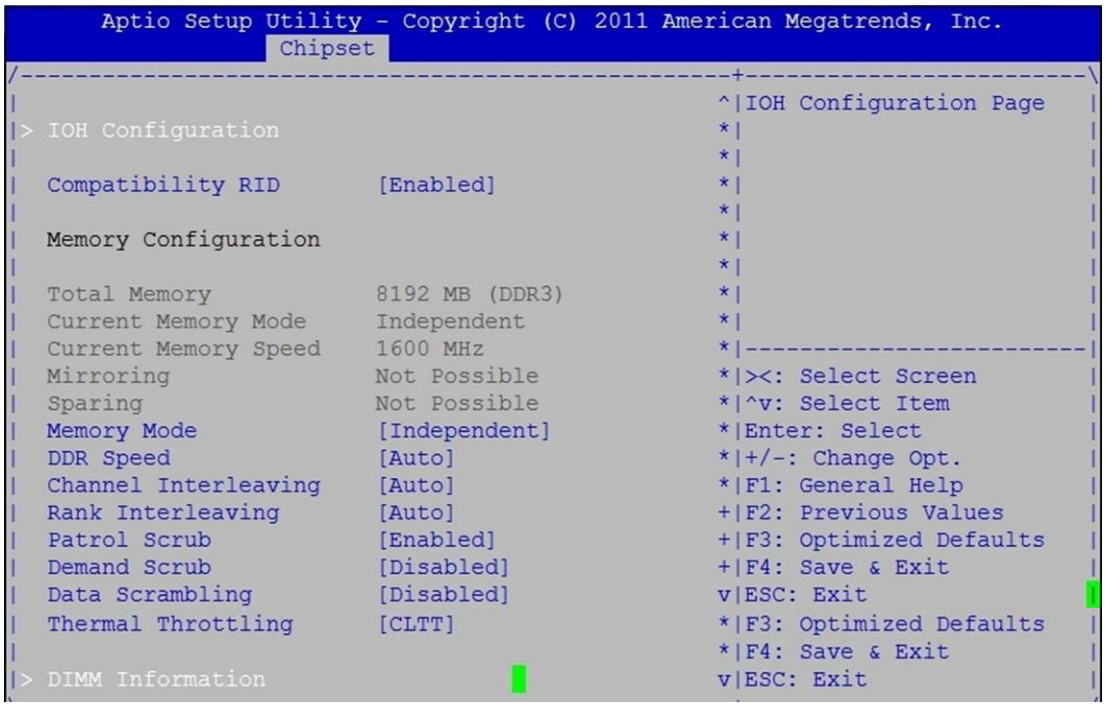
6.4 Chipset Setup Screen

Select Chipset tab from the setup screen to enter Chipset BIOS setup screen. You can select any of the items in the left frame of the screen to go to sub menu for that item. An example of Chipset BIOS setup screen is shown below.



6.4.1 North Bridge

You can use this screen to specify options for the North Bridge settings. Use the up and down <Arrow> keys to select an item. Use <+> and <-> keys to change the value of the selected option. The settings are described in the following pages. The screen is shown as below.



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Memory Configuration

In this setup screen, some memory information will be shown.

Memory Mode

This option is used for configuring the memory mode.

Patrol Scrub

This item is used for enabling or disabling patrol scrub.

Demand Scrub

This item is used for enabling or disabling Demand Scrubbing feature.

Data Scrambling

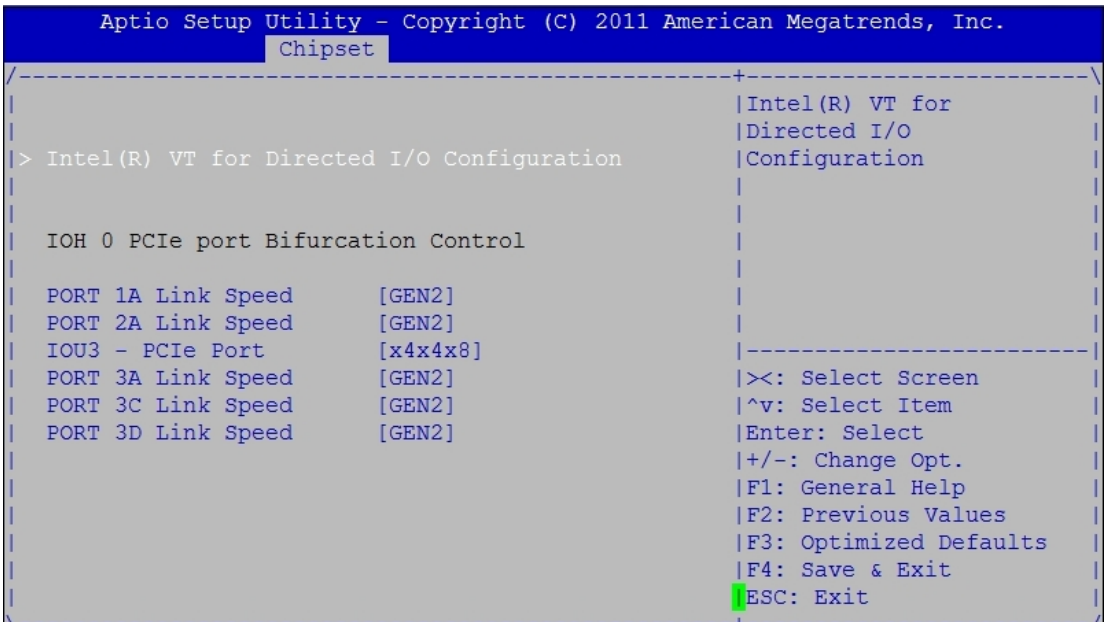
This item is used for enabling or disabling Data Scrambling.

Thermal Throttling

This item is used for close or open Loop Thermal Throttling.

6.4.1.1IOH Configuration

You can use this screen to configure PCIe port link speed and bifurcation. The screen is shown as below.



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PORT 1A Link Speed

Port 1A is designed to link onboard PCIe x8 Ethernet. This item is for configuring the link speed to x8 device.

PORT 2A Link Speed

Port 2A is designed to link onboard PCIe x16 device. This item is for configuring the link speed to x16 device.

IOU3 – PCIe Port

IOU3 can be configured to x4x4x4x4(if RTM has two x4 PCIe devices) or x4x4x8(if RTM has one x8 PCIe devices) or x8x4x4(if RTM has one x4 PCIe devices) or x8x8 or x16

PORT 3A Link Speed

Port 3A is designed to link onboard PCIe x8 Ethernet. It provides the link to RTM GbE ports. This item is for configuring the link speed to x8 device.

PORT 3C Link Speed

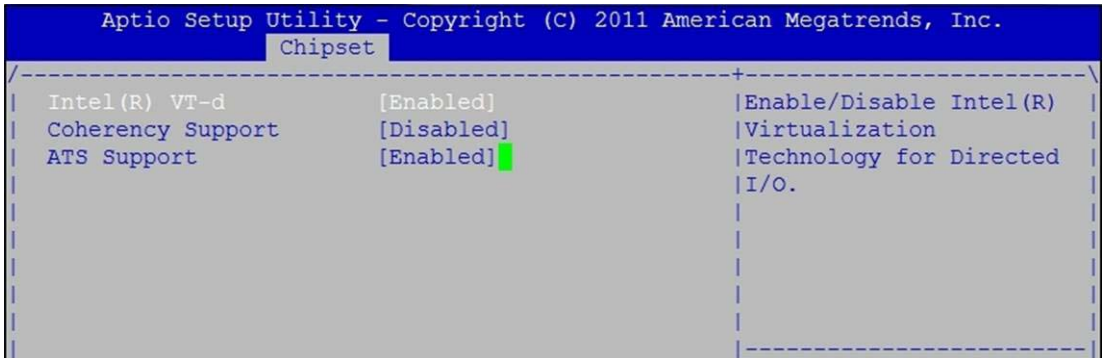
Port 3C is designed to link onboard PCIe x4/x8 Ethernet. It provides the link to RTM. This item is for configuring the link speed to x4/x8 device.

PORT 3D Link Speed

Port 3D is designed to link onboard PCIe x4 AMC device.

Intel VT for Directed I/O Configuration

You can use this screen to configure Intel Virtualization Technology parameters. The screen is shown as below.



Intel VT-d

This item allows user to enable or disable Intel® VT for Directed I/O (VT-d) which provides additional hardware support for managing I/O virtualization.

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Coherency Support

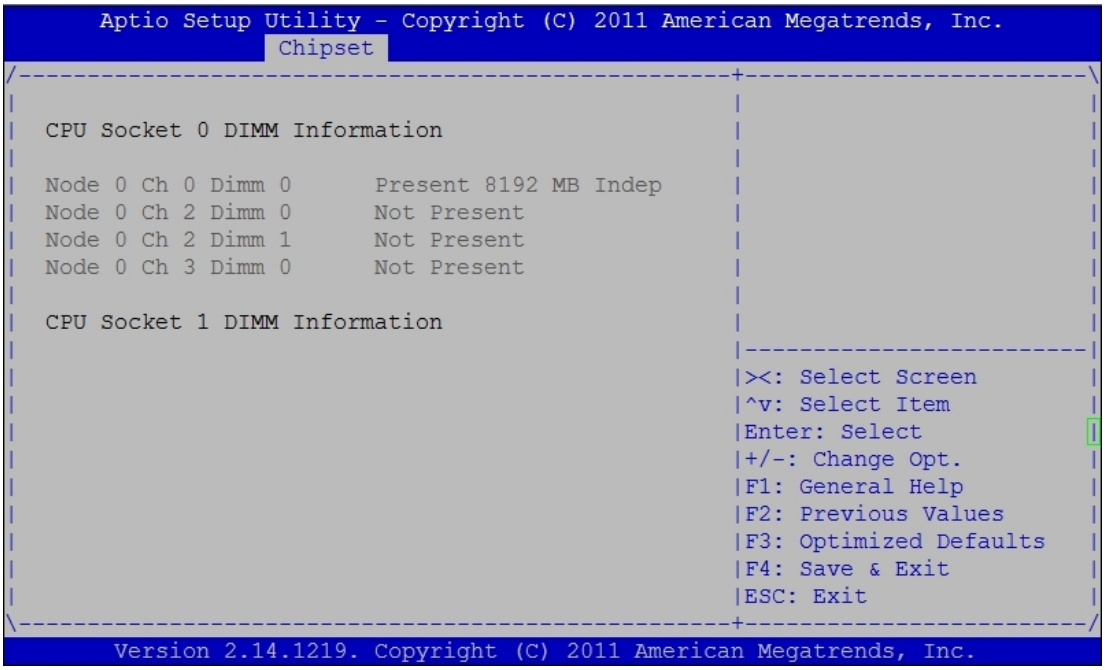
It allows user to enable or disable Non-Isoch VT-d Engine Coherency support.

ATS Support

It allows user to enable or disable Non-Isoch VT-d Engine Address Translation Services (ATS) support.

6.4.1.2 DIMM information

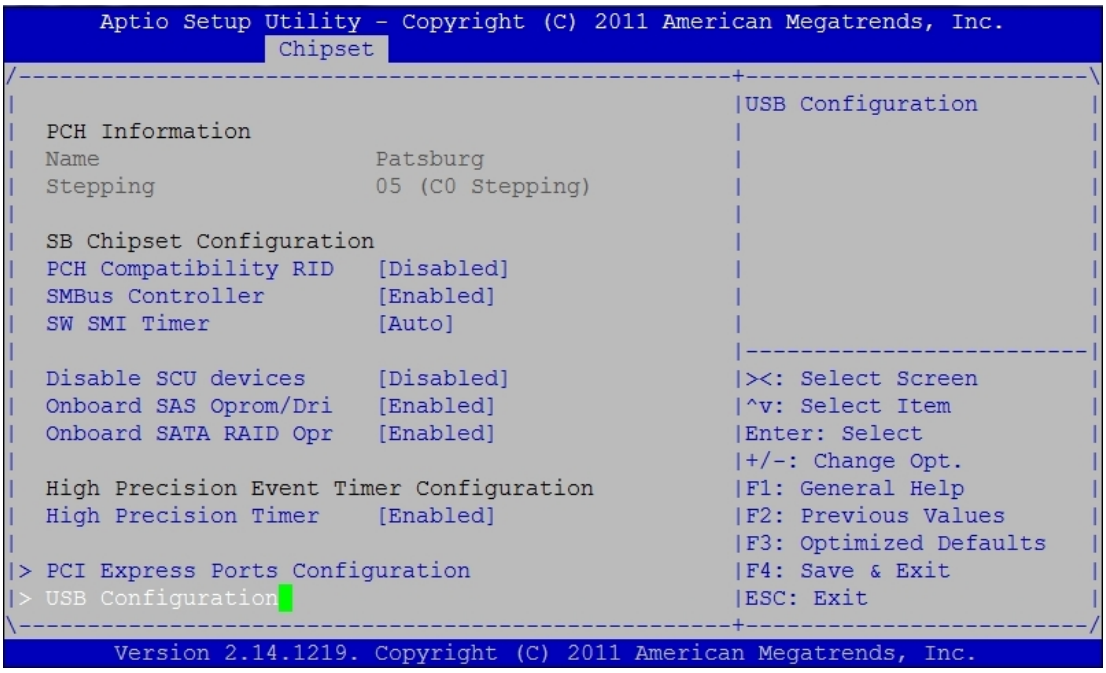
You can use this screen to check DIMM presence and Size information. The screen is shown as below.



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6.4.2 South Bridge

You can use this screen to specify options for the PCH configuration settings. Use the up and down <Arrow> keys to select an item. Use <+> and <-> keys to change the value of the selected option. The settings are described in the following pages. The screen is shown as below.



PCH Information

The PCH information will include the name and stepping of PCH that is designed on aTCA-6200.

PCH Compatibility RID

It is for setting the support for PCH compatibility revision ID (CRID) functionality.

SMBus Controller

This option allows enabling or disabling system's SMBus controller.

Periodic SMI

It allows user to enable or disable the periodic generation of a System management Interrupt (SMI).

Disable SCU devices

It is for enabling or disabling Patsburg SCU devices.

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Onboard SAS Oprom

This item allows user to enable or disable SAS option ROM.

Onboard SATA RAID Oprom

This item allows user to enable or disable SATA RAID option ROM.

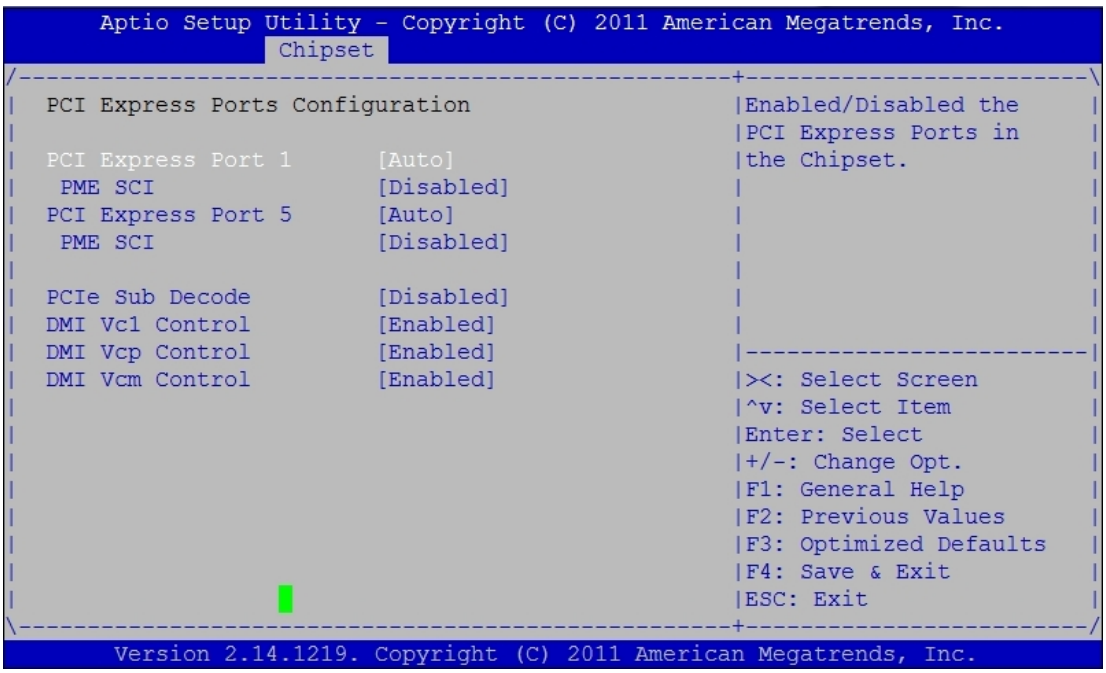
High Precision Timer

The High Precision Event Timer is a hardware timer used in personal computers. A High Precision Event Timer chip consists of a 64-bit main counter counting at least at 10MHz and a set of up to 256 comparators. HPET is programmed via a memory mapped I/O window that is discoverable via ACPI. The HPET circuit in modern PCs is integrated into the southbridge.

The HPET can produce periodic interrupts at a much higher resolution than the RTC.
This option allows user to enable or disable High Precision Event Timer.

6.4.2.1 PCI Express Ports Configuration

You can use this screen to specify options for the PCI Express Ports configuration settings. Use the up and down <Arrow> keys to select an item. Use <+> and <-> keys to change the value of the selected option. The settings are described in the following pages. The screen is shown as below.



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PCI Express Port

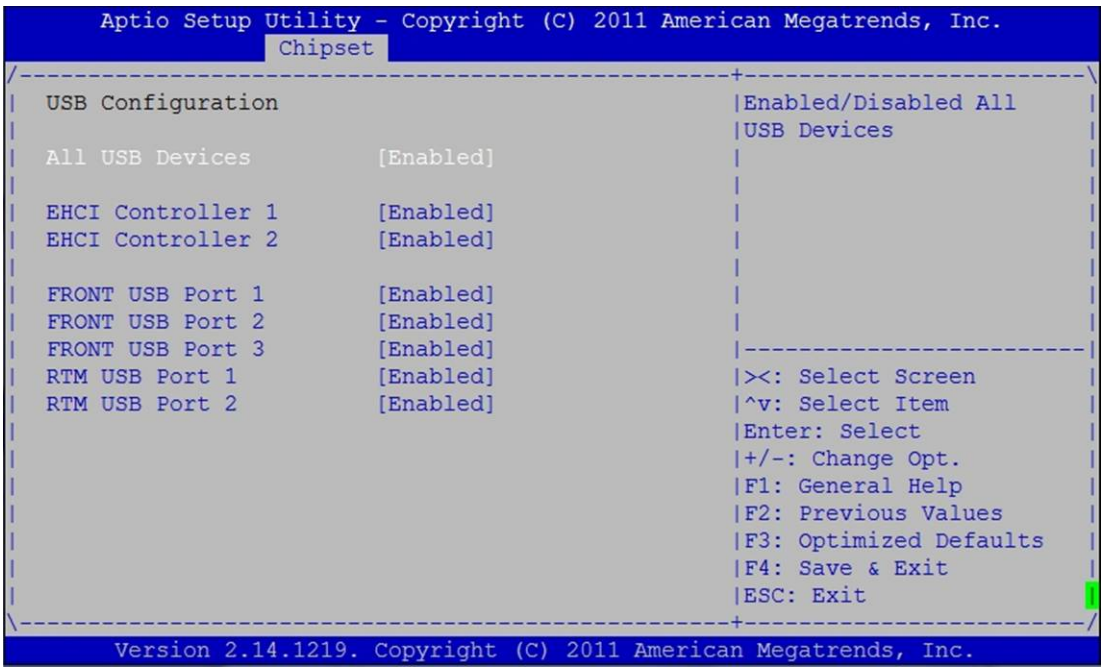
This item enables or disables the PCI Express Ports in the chipset.

PME SCI

This item enables or disables the PCI Express PME SCI.

6.4.2.2 USB Configuration

You can use this screen to specify options for the USB configuration settings. Use the up and down <Arrow> keys to select an item. Use <+> and <-> keys to change the value of the selected option. The settings are described in the following pages. The screen is shown as below.



All USB Devices

This item enables or disables all USB devices.

EHCI Controller 1

This item enables or disables USB 2.0 (EHCI) controller 1.

EHCI Controller 2

This item enables or disables USB 2.0 (EHCI) controller 2.

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FRONT USB Port 1

This item is to enable or disable front USB port 1. When it is disabled, the USB device plugged in the front USB port 1 won't work.

FRONT USB Port 2

This item is to enable or disable front USB port 2. When it is disabled, the USB device plugged in the front USB port 2 won't work.

FRONT USB Port 3

This item is to enable or disable front USB port 3. When it is disabled, the USB device plugged in the front USB port 3 won't work.

RTM USB Port 1

This item is to enable or disable RTM USB port 1. When it is disabled, the USB device plugged in the RTM USB port 1 won't work.

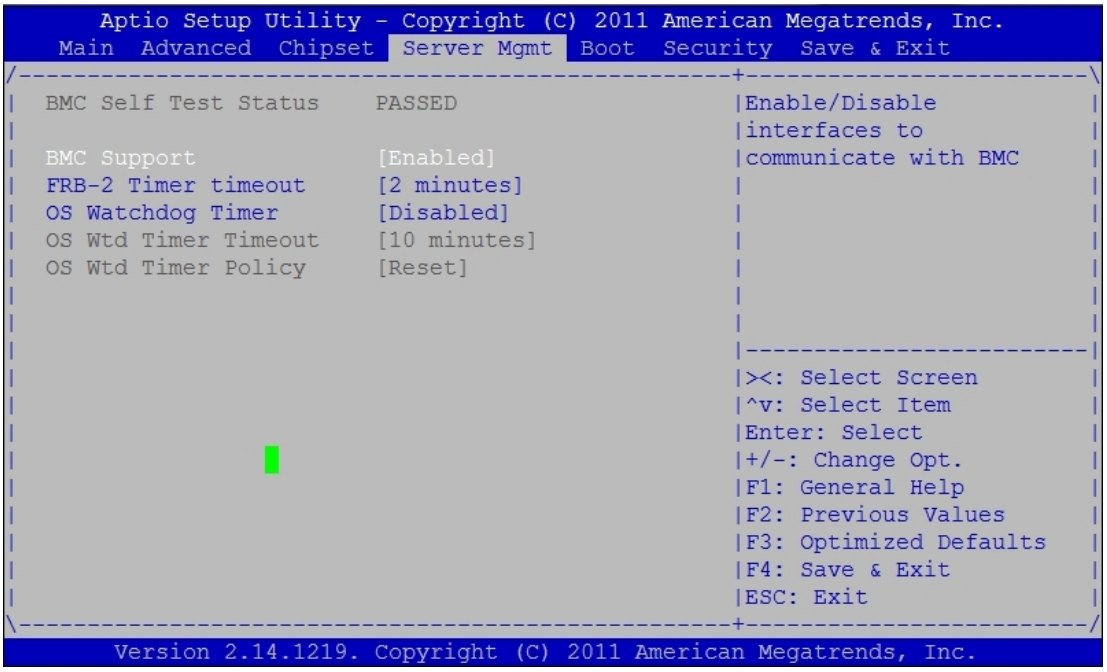
RTM USB Port 2

This item is to enable or disable RTM USB port 2. When it is disabled, the USB device plugged in the RTM USB port 2 won't work.

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6.5 Server Mgmt Setup Screen

You can use this screen to specify options for the Server Management settings. Use the up and down <Arrow> keys to select an item. Use <+> and <-> keys to change the value of the selected option. The settings are described in the following pages. The screen is shown as below.



BMC Support

It is for enabling or disabling the interface to communicate with BMC.

FRB-2 Timer timeout

It can select the value between 1 to 4 min for FRB-2 timer expiration value.

OS Watchdog Timer

If enabled, starts a BIOS timer which can only be shut off by Intel Management software after the OS loads.

OS WD Timer Timeout

If is for configuring the length of the OS boot watchdog timer. Not available if OS boot watchdog timer is disabled.

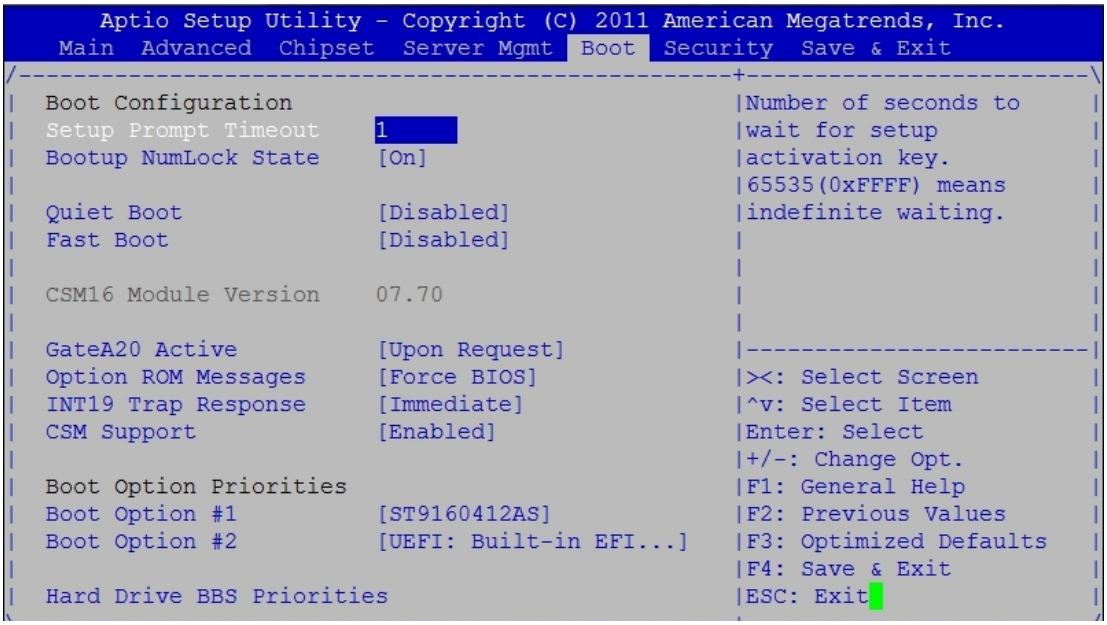
OS WD Timer Policy

If is for configuring how the system should respond if the OS boot Watchdog Timer expires. Not available if OS boot watchdog timer is disabled.

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6.6 Boot Setup Screen

You can use this screen to specify options for the Boot configuration settings. Use the up and down <Arrow> keys to select an item. Use the <+> and <-> keys to change the value of the selected option. The settings are described in the following pages. The screen is shown as the below.



Setup Prompt Timeout

It's the number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting. Use the <+> and <-> keys to change the value of this item.

Bootup NumLock State

The item let users to select the keyboard numLock state.

Quiet Boot

This item allows system BIOS to show the boot up splash logo. When it is set to "Enabled", the logo that in system BIOS will be shown during display outputs.

Fast Boot

This item allows system BIOS to boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

GateA20 Active

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Upon Request – GA20 can be disabled by using BIOS services. Always – do not allow disabling GA20. This option is useful when any RT code is executed above 1MB.

Option ROM Messages

Set this option to enable for allowing system to display PCI devices' option ROMs during system boot up.

INT19 Trap Response

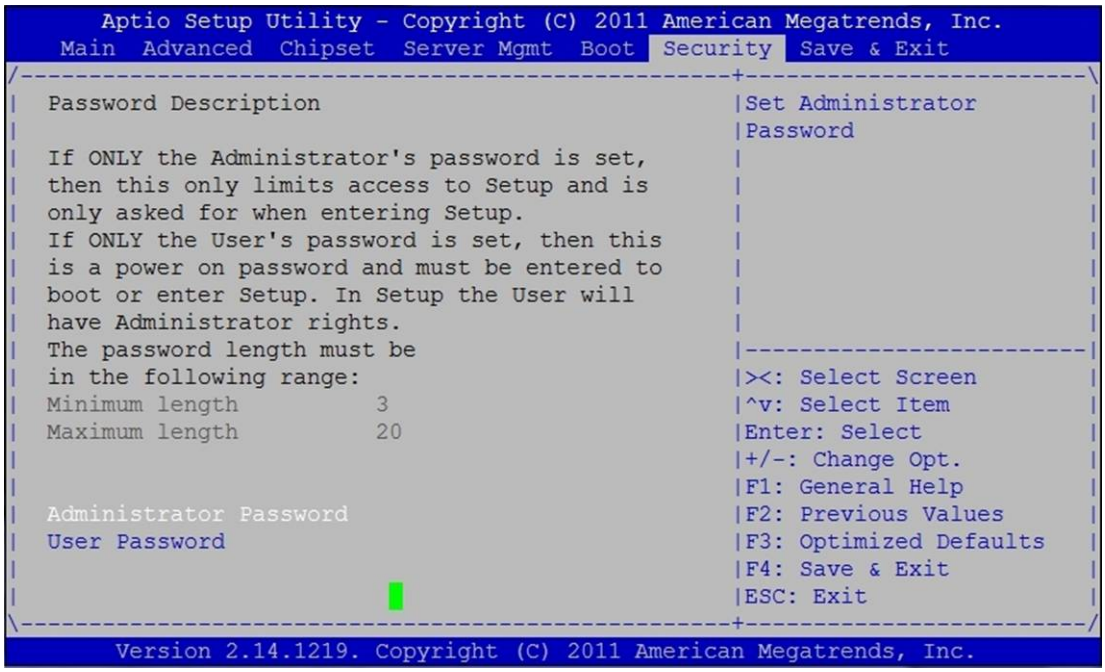
Interrupt 19 is the software interrupt that handles the boot disk function. When set to Enabled, this item allows the option ROMs to trap interrupt 19.

CSM Support

Set this option to Enable/Disable CSM Support. If Auto is selected, based on OS, CSM will be enabled/disabled automatically.

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6.7 Security Setup Screen



System BIOS provides two levels of password protection. They are Administrator password and User password. The system can be configured that all users must enter password every time the system boots or when setup utility is executed, using either Administrator password or User password.

The Administrator and User passwords activate two different levels of password security. If you select password support, you are prompted for 3 to 20 characters password. Type the password on the keyboard. The password doesn't appear on the screen when typed. Make sure you write it down. If you forget it, you must drain NVRAM and re-configure it.

Administrator Password

Use this option to set a password for administrator with full control of the BIOS setup utility.

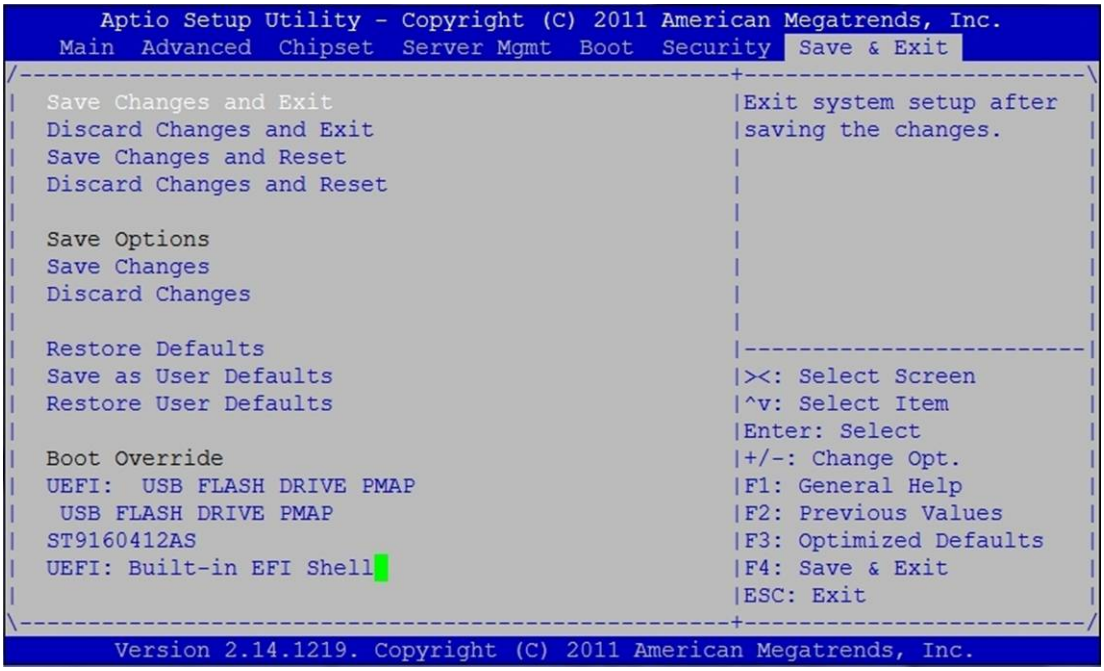
User Password

Use this option to set a password for user with limited access to the BIOS setup utility.

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6.8 Save & Exit Setup Screen

Select ***Save & Exit*** tab from setup utility to enter ***Save & Exit*** BIOS setup screen. You can select an item by highlighting it using the <Arrow> keys. The ***Save & Exit*** BIOS setup screen is shown below.



Save Changes and Exit

When you have completed the system configuration changes, select this option to leave setup utility and reboot the computer to let new system configuration parameters take effect. Select this item then press <Enter>. The prompt message will pop up and wait for use's confirmation.

Save Changes and Exit?
[OK] [Cancel]

Select OK then press <Enter> to save changes and exit. It will continue the boot up process if there is no need to reset the system.

Discard Changes and Exit

Select this option to quit setup without making any permanent changes to the system configuration. When selecting this item and then press <Enter>. The below message will be shown up and wait for the confirmation.

Discard Changes and Exit?
[OK] [Cancel]

Select OK and press <Enter> to discard changes and exit. It will keep booting the system to OS.

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Save Changes and Reset

It has the same function as Save Changes and Exit except resetting system. System will always be reset after selecting this item no matter what change is made,

Discard Changes and Reset

It has the same function as Discard Changes and Exit except resetting system. System will always be reset after selecting this item and will not save any configuration.

Save Changes

Save the changes done so far to any of setup options.

Discard Options

Discard the changes done so far to any of setup options.

Restore Defaults

Load BIOS built-in default value for all setup options.

Save as User Defaults

Save the changes done so far as user defaults.

Restore User Defaults

Restore the saved user default to all the setup options.

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7 Serial Over LAN

Serial Over LAN (SOL) is a remote management mechanism in which the IPMI controller redirects the serial console from the blade via an IPM Interface session over the network with RMCP+ protocol. The aTCA-6200 supports SOL on the Base Interface which is powered by the Intel® 82576 Gigabit Ethernet Controller. The SOL feature supports transmit/receive of serial console messages from a remote site with full console management ability. The aTCA-6200 supports 2 channels (channel 1/2) and 2 user IDs for SOL. You can refer to the following section for more detailed configuration.

Note: SOL does not support login of 2 users at the same time.

7.1 Preparation for SOL Connection

Prepare a remote client with Linux OS and connect it to the network.

7.2 Configuring the Remote Client

7.2.1 Installing the Ipmitool for Remote Client

You can download the latest ipmitool and document from the following website
http://ipmitool.sourceforge.net

Click on either the *bz or *gz version of ipmitool to download the bzipped or gzipped ipmitool source code tarball respectively.

To build the ipmitool, unzip and untar the downloaded ipmitool package, configure the ipmitool for your system, and then navigate to the created ipmitool directory.

Example using the gzipped tarball:

```
tar xvzf ipmitool*.tar.gz□cd ipmitool*
```

Run the following to configure ipmitool for your system:

```
./configure
```

Build the source code and install ipmitool:

```
make
make install
```

Now your remote client is ready to connect to the target aTCA-6200 blade.

Note: The install must be run with root permissions to overlay the existing ipmitool utility in /usr/local/bin.

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7.3 Configuring the Target aTCA-6200

7.3.1 BIOS Configuration

You can refer to section 6.3.9/6.3.10 to enable Serial Port Console Redirection

7.3.2 Linux GRUB Settings

Linux GRUB supports sending messages to the serial console. The following lines should be added to the top of the /boot/grub/grub.conf file.

```
default=1
timeout=5
serial --unit=1 --speed=115200 --word=8 --parity=no --stop=1
terminal --timeout=15 serial console
```

The following parameters need to be passed to each instance of the linux kernel. They should be added to the kernel line. It would be helpful if GRUB supported variable substitution so that the parameters only needed to be defined in one place.

```
console=tty0 console=ttyS1,115200n8
```

The example is below:

```
title SOL (2.6.18-128.el5)
root (hd0,0)
kernel /boot/vmlinuz-2.6.18-128.el5 ro root=LABEL=/ console=tty0
console=ttyS1,115200n8
initrd /boot/initrd-2.6.18-128.el5.img
```

7.3.3 Linux System Settings

Linux needs to be told to listen for logins on the serial port. This is done by adding the following line to /etc/inittab.
Add the following line to the init configuration file /etc/inittab.

s1:12345:respawn:/sbin/agetty –L ttyS1 115200 vt100

Now your target aTCA-6200 is ready for SOL connection.

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7.4 Establish SOL Connection

Execute the following command from your remote client to establish the SOL Connection
Command:

ipmitool -I lanplus -H <Target IPMC IP > -C < Cipher Suite Id > -U <User Name> -P <Passsword> sol activate

Note: Please refer to the following table for the Cipher Suite Id

ID	Characteristics	Cipher Suite	Authentication Algorithm	Integrity Algorithm(s)	Confidentiality Algorithm(s)
0	“straight password"	00h, 00h, 00h	RAKP-none	None	None
1	S	01h, 00h, 00h	RAKP-HMAC-SHA1	None	None
2	S, A	01h, 01h, 00h		HMAC-SHA1-96	None
3	S, A, E	01h, 01h, 01h			AES-CBC-128
4	S, A, E	01h, 01h, 02h			xRC4-128
5	S, A, E	01h, 01h, 03h			xRC4-40
6	S	02h, 00h, 00h	RAKP-HMAC-MD5	None	None
7	S, A	02h, 02h, 00h		HMAC-MD5-128	None
8	S, A, E	02h, 02h, 01h			AES-CBC-128
9	S, A, E	02h, 02h, 02h			xRC4-128
10	S, A, E	02h, 02h, 03h			xRC4-40
11	S, A	02h, 03h, 00h		MD5-128	None
12	S, A, E	02h, 03h, 01h			AES-CBC-128
13	S, A, E	02h, 03h, 02h			xRC4-128
14	S, A, E	02h, 03h, 03h			xRC4-40
80h-BFh	OEM specified	OEM specified	OEM specified	OEM specified	OEM specified
C0h-FFh	reserved	-	-	-	-

The default value of aTCA-6200 SOL parameters are listed in the table below

Parameter	Default Value
Channel 1 IP Address	192.168.100.100
Channel 2 IP Address	172.17.100.100
User ID	2
User Name	adlinkuser
Password	adlinkuser

Below are 2 samples to establish the SOL session via channel 1 with default user name and password:

Establish a non-nncrypted RMCP+ SOL session

./ipmitool -I lanplus -H 172.17.172.134 -C 0 -U "adlinkuser" -P "adlinkuser" sol activate

Establish an encrypted RMCP+ SOL session

./ipmitool -I lanplus -H 172.17.172.134 -C 3 -k gkey -U "adlinkuser" -P "adlinkuser" sol activate

For more detailed IPMI commands, please visit the following URL: http://ipmitool.sourceforge.net.

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8 Drivers

The drivers for aTCA-6200 are available on the ADLINK website. Please download them from the product page on the ADLINK web site:
http://www.adlinktech.com/PD/web/PD_detail.php?cKind=&pid=1110.

We recommend using the drivers provided on the ADLINK website to ensure optimum compatibility. Contact ADLINK to get support for drivers for other operating systems.

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Safety Instructions

1. Please read these safety instructions carefully.
2. Please keep this User‘s Manual for later reference.
3. One AC Inlets provided and service as Disconnect Devices, disconnect the equipment from both AC outlets use these AC Inlets before servicing or clearing. Use moisture sheet or cloth for cleaning.
4. For pluggable equipment, that the socket-outlet shall be installed near the equipment and shall be easily accessible.
5. Please keep this equipment from humidity.
6. Lay this equipment on a reliable surface when install. A drop or fall could cause injury.
7. Make sure the voltage of the power source when connect the equipment to the power outlet.
8. Place the power cord such a way that people can not step on it. Do not place anything over the power cord.
9. All cautions and warnings on the equipment should be noted.
10. If the equipment is not use for long time, disconnect the equipment from mains to avoid being damaged by transient overvoltage.
11. Never pour any liquid into openings; this could cause fire or electrical shock.
12. Never open the equipment. For safety reason, the equipment should only be opened by qualified service personnel.
13. If one of the following situations arises, get the equipment checked by a service personnel:
    a. The Power cord or plug is damaged.
    b. Liquid has penetrated into the equipment.
    c. The equipment has been exposed to moisture.
    d. The equipment has not work well or you can not get it work according to user‘s manual.
    e. The equipment has dropped and damaged.
    f. If the equipment has obvious sign of breakage.
14. The equipment can be operated at an ambient temperature of 55°C.
15. Lithium Battery provided (real time clock battery), contact ADLINK for replacing,

CAUTION – Risk of explosion if battery is replaced by an incorrect type. Dispose of used batteries according to the instructions”

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Getting Service

Contact us should you require any service or assistance.

ADLINK Technology, Inc.
Address: 9F, No.166 Jian Yi Road, Zhonghe District
New Taipei City 235, Taiwan
新北市中和區建一路 166 號 9 樓
Tel: +886-2-8226-5877
Fax: +886-2-8226-5717
Email: service@adlinktech.com

Ampro ADLINK Technology, Inc.
Address: 5215 Hellyer Avenue, #110, San Jose, CA 95138, USA
Tel: +1-408-360-0200
Toll Free: +1-800-966-5200 (USA only)
Fax: +1-408-360-0222
Email: info@adlinktech.com

ADLINK Technology (China) Co., Ltd.
Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203)
300 Fang Chun Rd., Zhangjiang Hi-Tech Park,
Pudong New Area, Shanghai, 201203 China
Tel: +86-21-5132-8988
Fax: +86-21-5132-3588
Email: market@adlinktech.com

ADLINK Technology Beijing
Address: 北京市海淀区上地东路 1 号盈创动力大厦 E 座 801 室(100085)
Rm. 801, Power Creative E, No. 1, B/D
Shang Di East Rd., Beijing, 100085 China
Tel: +86-10-5885-8666
Fax: +86-10-5885-8625
Email: market@adlinktech.com

ADLINK Technology Shenzhen
Address: 深圳市南山区科技园南区高新南七道 数字技术园 A1 栋 2 楼 C 区 (518057)
2F, C Block, Bldg. A1, Cyber-Tech Zone, Gao Xin Ave. Sec. 7,
High-Tech Industrial Park S., Shenzhen, 518054 China
Tel: +86-755-2643-4858
Fax: +86-755-2664-6353
Email: market@adlinktech.com

LiPPERT ADLINK Technology GmbH
Address: Hans-Thoma-Strasse 11, D-68163, Mannheim, Germany
Tel: +49-621-43214-0
Fax: +49-621 43214-30
Email: emea@adlinktech.com

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

ADLINK Technology, Inc. (French Liaison Office)
Address: 15 rue Emile Baudot, 91300 Massy CEDEX, France
Tel: +33 (0) 1 60 12 35 66
Fax: +33 (0) 1 60 12 35 66
Email: france@adlinktech.com

ADLINK Technology Japan Corporation
Address: 〒101-0045 東京都千代田区神田鍛冶町 3-7-4
神田 374 ビル 4F
KANDA374 Bldg. 4F, 3-7-4 Kanda Kajicho,
Chiyoda-ku, Tokyo 101-0045, Japan
Tel: +81-3-4455-3722
Fax: +81-3-5209-6013
Email: japan@adlinktech.com

ADLINK Technology, Inc. (Korean Liaison Office)
Address: 1675-12 8
8F Mointer B/D,1675-12, Seocho-Dong, Seocho-Gu,
Seoul 137-070, Korea
Tel: +82-2-2057-0565
Fax: +82-2-2057-0563
Email: korea@adlinktech.com

ADLINK Technology Singapore Pte. Ltd.
Address: 84 Genting Lane #07-02A, Cityneon Design Centre,
Singapore 349584
Tel: +65-6844-2261
Fax: +65-6844-2263
Email: singapore@adlinktech.com

ADLINK Technology Singapore Pte. Ltd. (Indian Liaison Office)
Address: 1st Floor, #50-56 (Between 16th/17th Cross) Margosa Plaza,
Margosa Main Road, Malleswaram, Bangalore-560055, India
Tel: +91-80-65605817, +91-80-42246107
Fax: +91-80-23464606
Email: india@adlinktech.com

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