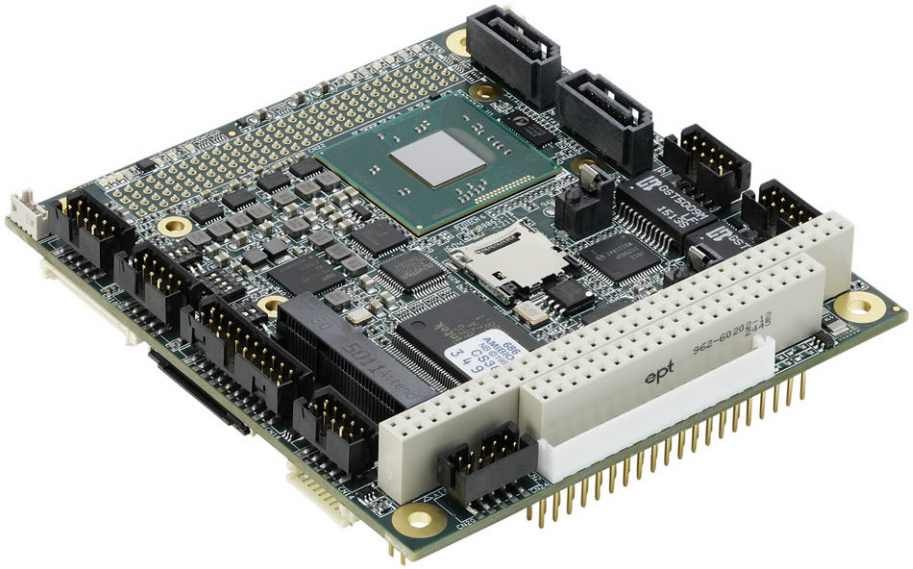
CMx-BTx
Technical Manual

PC/104-based Single Board Computer
with Intel Atom® E3800 Series Processors



Manual Rev.: 5.0

Revision Date: January 7, 2025

Part Number: 50M-95186-5000

Leading **EDGE COMPUTING**

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Preface

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Revision History

Revision	Reason for Change	Date
1.0	Initial Release	2015-05-08
2.0	Revised for new board layout	2015-08-27
3.0	Revised for new revision of the board; removed USB 3.0 functionality and added BAT1 interface	2016-02-12
4.0	Added note to Section 4.4.8, requiring a connected RTC battery for enabled ECO mode	2016-08-08
4.1	Added heat spreader installation procedure to Section 2.4; added requirements for SODIMM installation to Table 1-1; Updated BIOS setup section to new format and content in Chapter 4; updated Figure 2-2 to change CN17 from 10 to 9 pins; revised P/N of CN17 mating connector in Table 2-2; Added PM changes from review of rev 5.02; Removed SATA cable from cable set in Table 2-1	2017-11-16
4.2	Updated BMC exception blink codes in Table 4-2; moved BIOS Setup section to its own chapter; moved System Resources to their own chapter	2018-10-31
4.3	Remove description of unsupported RS485 functionality, add HD Audio (CN15) description	2020-11-16
4.4	Add French safety warnings	2021-02-04
4.5	Update support OS, BIOS info	2022-07-27
4.6	Update specifications, On-Board Power Supply description	2023-06-28
5.0	Revised for updated PCB	2025-01-07

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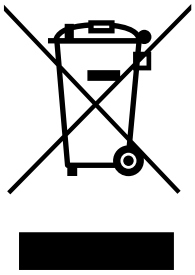
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Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

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WARNING: This product can expose you to chemicals including acrylamide, arsenic, benzene, cadmium, Tris(1,3-dichloro-2-propyl)phosphate (TDCPP), 1,4-Dioxane, formaldehyde, lead, DEHP, styrene, DINP, BBP, PVC, and vinyl materials, which are known to the State of California to cause cancer, and acrylamide, benzene, cadmium, lead, mercury, phthalates, toluene, DEHP, DIDP, DnHP, DBP, BBP, PVC, and vinyl materials, which are known to the State of California to cause birth defects or other reproductive harm. For more information go to www.P65Warnings.ca.gov**.**

AVERTISSEMENT: *Ce produit peut vous exposer à des produits chimiques tels que l'acrylamide, l'arsenic, le benzène, le cadmium, le phosphate de tris (1,3-dichloro-2-propyle) (TDCPP), le 1,4-dioxane, le formaldéhyde, le plomb, le DEHP, le styrène, le DINP , BBP, PVC et matériaux en vinyle, qui sont connus dans l'État de Californie pour causer le cancer, et acrylamide, benzène, cadmium, plomb, mercure, phtalates, toluène, DEHP, DIDP, DnHP, DBP, BBP, PVC et vinyle matériaux, qui sont connus de l'État de Californie pour causer des anomalies congénitales ou d'autres troubles de la reproduction. Pour plus d'informations, visitez le site www.P65Warnings.ca.gov.*

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Conventions

The following conventions may be used throughout this manual, denoting special levels of information.



This information adds clarity or specifics to text and illustrations.



MISE EN GARDE

This information indicates the possibility of ***minor*** physical injury, component damage, data loss, and/or program corruption.

*Ces informations indiquent la possibilité de blessures physiques **mineures**, de dommages aux composants, de perte de données et / ou de corruption de programme.*



ATTENTION

This information warns of possible ***serious*** physical injury, component damage, data loss, and/or program corruption.

*Ces informations mettent en garde contre d'éventuelles blessures physiques **graves**, des dommages aux composants, une perte de données et / ou une corruption du programme.*

Important Safety Instructions

For user safety, please read and follow all **Instructions**, **WARNINGs**, **CAUTIONs,** and **NOTEs** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

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1 Introduction

1.1 Overview

The CMx-BTx is a PC/104-based, Single Board Computer (SBC), fully compliant with the PCI-104 Specification, Version 1.1 and partially compliant with the PC/104 Specification, Version 2.6. PC/104 SBCs are very compact and highly integrated computers. This SBC features the 22nm Intel® Bay Trail SoC.

The board provides a DDR3L SODIMM socket, a PC/104 connector and/or a PCI-104 connector, up to four USB 2.0 ports (with one port routed to mini-PCIe slot), up to two Gigabit Ethernet ports, up to two SATA 3 Gb/s ports, one dedicated HD-Audio panel connector, one VGA port, one LVDS port, up to four COM ports, one mini-PCIe slot (shared with one USB 2.0 port).

The CMx-BTx can be run with only 5 volts and is capable of running operating systems like DOS, Windows 7/8.1/10 in either 32-bit or 64-bit configuration, Linux, VxWorks, and others.

Another feature included on the board is a secondary BIOS that enables the user to start the module even if the original BIOS is corrupted (see “SW4 BIOS Control Switch” on page 44).

1.2 Features

<table>
<tr>
<td>SoC
▶ Intel® Bay Trail I/M/D with integrated Graphics
▷ Bay Trail-I Premium (E3845)
▷ Bay Trail-I Med (E3825)
▷ Bay Trail-I Entry (E3815)</td>
<td>Main Memory
▶ Single channel 64bit 1067 MT/s and 1333 MT/s Non-ECC, unbuffered DDR3L SODIMM up to 4 GB
Expansion slots
▶ 1x mini-PCIe with mSATA and USB capability (3.3V I/O)
▶ 1x 16-bit PC/104 without DMA and no bus mastering capability
▶ 1x 32-bit PCI-104</td>
</tr>
<tr>
<td>Interfaces
▶ 2x Ethernet, 1GBit
▶ 2x SATA 3Gb/s
▶ 4x USB 2.0 (one routed to mini-PCIe slot)
▶ 4x RS232/422
▶ 5.1 channel HD-Audio (analog & SPDIF)
▶ 1x VGA</td>
<td>▶ 1x 18/24 Bit LVDS for displays
▶ 8x User GPIO
▶ System panel connector for power and reset button cable, watchdog out, speaker and HDD-LED</td>
</tr>
</table>



Other configurations are possible. Please contact your local ADLINK Technology representative to discuss requirements.

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1.3 Block Diagram

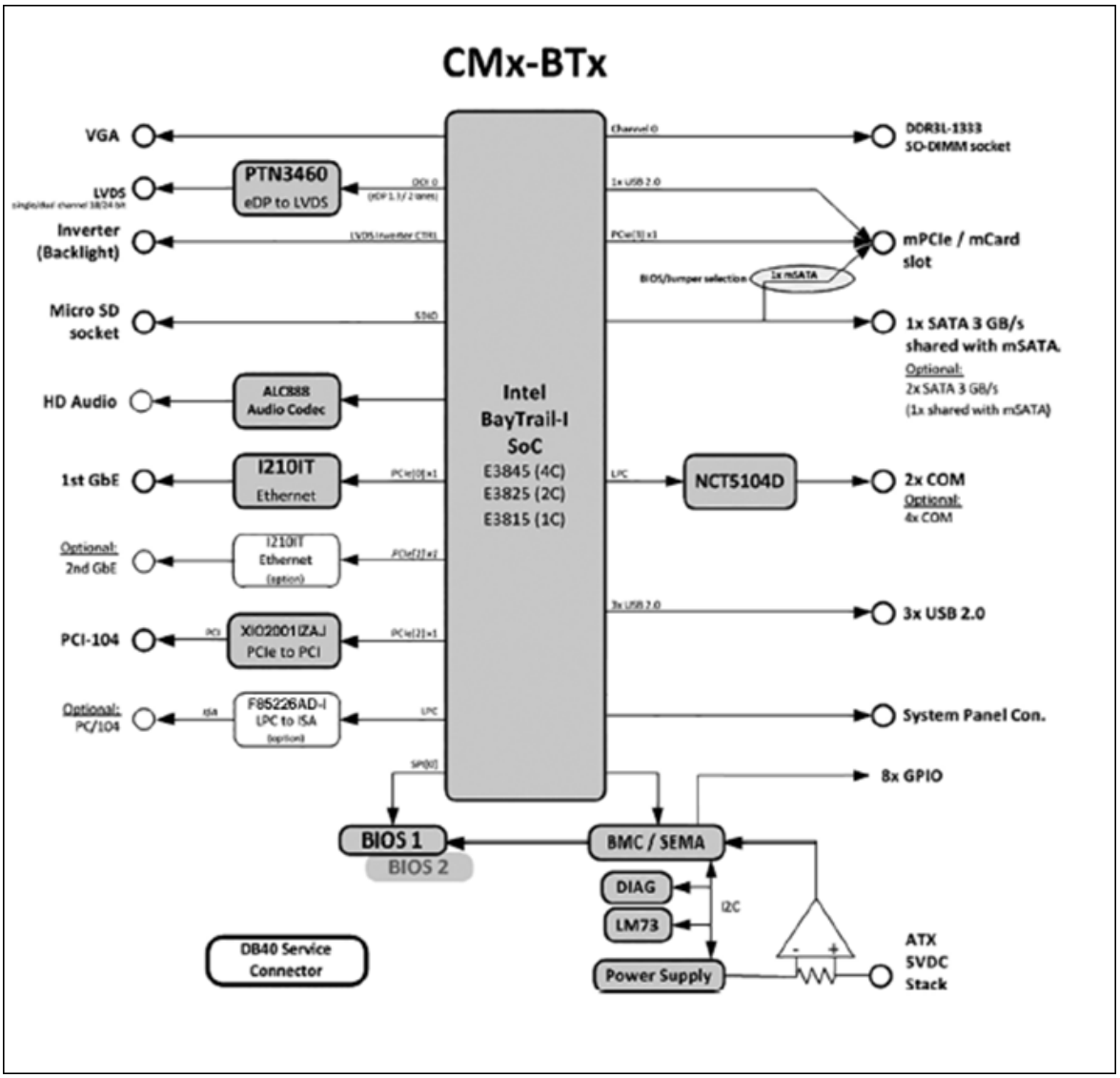


Figure 1-1: Functional Block Diagram

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1.4 Ordering Information

Table 1-1: CMx-BTx Models

Model Number	Description
CM1-BT1-E3815	PC/104, E3815, 1.46 GHz, Single Core, incl. heat spreader, 0°C to 60°C (memory not included; see Table 1-2 for DDR3L memory options)
CM2-BT2-E3825	PC/104-Plus, E3825, 1.33 GHz, Dual Core, incl. heat spreader, 0°C to 60°C (memory not included; see Table 1-2 for DDR3L memory options)
CM3-BT4-E3845	PCI-104, E3845, 1.91 GHz, Quad Core, incl. heat spreader, 0°C to 60°C (memory not included; see Table 1-2 for DDR3L memory options)
CM3-BT1-E3815	PCI-104, E3815, 1.46 GHz, Single Core, incl. heat spreader, 0°C to 60°C (memory not included; see Table 1-2 for DDR3L memory options)
CM1-BT1-E3815-ETT	PC/104, E3815, 1.46 GHz, Single Core, incl. heat spreader, -40°C to 85°C
CM2-BT2-E3825-ETT	PC/104-Plus, E3825, 1.33 GHz, Dual Core, incl. heat spreader, -40°C to 85°C
CM3-BT1-E3815-ETT	PCI-104, E3815, 1.46 GHz, Single Core, incl. heat spreader, -40°C to 85°C
CM3-BT4-E3845-ETT (supported with active heat sink, CMx-BTx-TM-20)	PCI-104, E3845, 1.91 GHz, Quad Core, incl. heat spreader, -40°C to 85°C

Table 1-2: CMx-BTx Cable Sets and Accessories

Ordering number	Description
CMx-BTx-X-10	Adapter Cable Set: ▶ Power ▶ 2x GBit-Ethernet ▶ 3x USB 2.0 ▶ 2x or 4x COM ▶ HD-Audio ▶ 1x System Panel ▶ External RTC Battery
CMx-BTx-TM-10	Passive, low-profile heat sink for CMx-BTx (see Table on page 5 for more details)
CMx-BTx-TM-20	Active, low-profile heat sink (with fan) for CMx-BTx (see Table on page 5 for more details)
DDR3L memory	Verified industrial grade 2GB and 4GB DDR3L SODIMM memory modules available

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1.5 Specifications

1.5.1 Electrical Specifications

Table 1-3: Electrical Specifications

Rise time:	< 10 ms
Supply voltage tolerance:	5VDC ±5 %
Inrush current:	3.5A at 5V in
Supply current:	3.5A

1.5.2 Environmental Specifications

Table 1-4: Operating Environmental Specifications

Temperature range:	-40°C … 85°C
Temperature change:	max. 10 Kelvin per 30 minutes
Humidity (relative):	10 % … 90 % (non condensing)
Pressure:	450 hPa … 1100 hPa

Table 1-5: Non-Operating/Transport Environmental Specifications

Temperature range:	-55°C … 85°C
Temperature change:	max. 10 Kelvin per 30 minutes
Humidity (relative):	5 % … 95 % (non condensing)
Pressure:	450 hPa … 1100 hPa

Table 1-6: HALT Parameters

Cold Temperature Step Stress:	The board remained operational during test down to -100°C, starting at 20°C and decreasing in 10°C increments with 15 minute dwells
Hot Temperature Step Stress:	The board remained operational during test up to 90°C, starting at 30°C and increasing in 10°C increments with 15 minute dwells
Rapid Thermal Transitions:	The board was subject to five rapid temperature cycles from -90°C to 85°C @ set transition rate of 60°C per minute
Vibration Step Stress:	The board was subject to vibration step stress with set points from 5 grams to 45 grams @ 20°C and vibration increasing by 5 grams with 15 minute dwells at each level of 2Hz to 5000Hz bandwidth
Combined Environment:	The board was subject to thermal cycles from -90°C to 85°C at an average rate of 60°C per minute combined with vibration at set points of 8, 16, 24, 32 and 40 grams from the first to the fifth thermal cycle and 10-minute dwells at each extreme temperature

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Table 1-7: Mean Time Between Failures

MTBF at 40°C	253981 Hrs
MTBF at 85°C	74186 Hrs

1.5.3 Mechanical Specifications

Table 1-8: Mechanical Specifications

Dimensions: (L x W)	90.6 mm x 95.2 mm
Height:	▶ 25mm with heat spreader
Weight:	▶ 172g with heat spreader
Mounting:	4 mounting holes
Heat spreader	pre-mounted



MISE EN GARDE

ADLINK strongly recommends plastic spacers instead of metal spacers for mounting the board. Metal spacers create the possibilities of short circuits with the components located around the mounting holes. This can damage the board.

ADLINK recommande fortement des entretoises en plastique au lieu d'entretoises métalliques pour le montage de la carte. Les entretoises métalliques créent des possibilités de courts-circuits avec les composants situés autour des trous de montage. Cela peut endommager la carte.

1.5.4 Heat Sink Specifications

Table 1-9: Cooling Requirements

Passive Heat Sink	• Supported by all CMx-BTx models in standard temperature range (0°C to 60°C) with 0.8m/s airflow. (Quad -core models start to throttle at 61°C.) • Supported by all CMx-BTx models (except for Quad-core models) in extended temperature range (-40°C to 85°C) with 0.8m/s airflow. (Dual-core models start to throttle at 87°C.)
Active Heat Sink	• Supported by all CMx-BTx models, including Quad-core models, in extended temperature range (-40°C to 85°C)

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2 Getting Started

2.1 Header and Connector Locations

Top Side

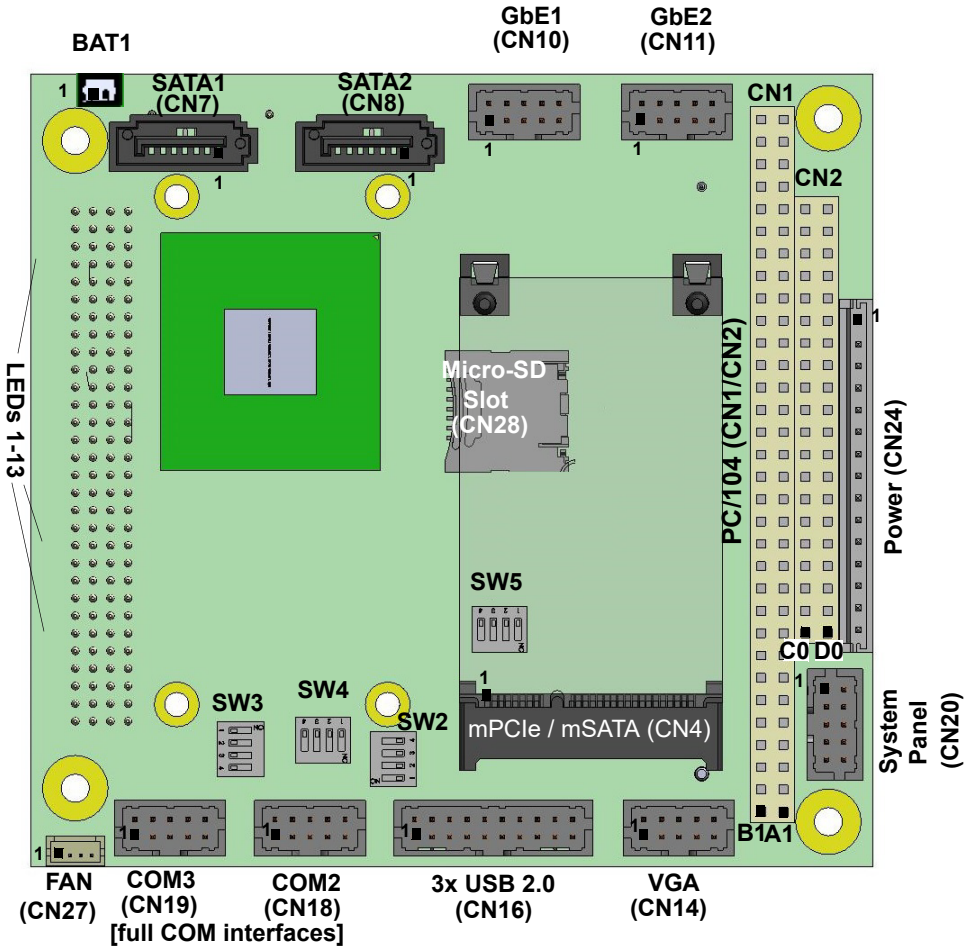


Figure 2-1: Header and Connector Locations (Top Side)

Table 2-1: Header, Connector, Socket, and Switch Definitions (Top Side)

Connector	Description	Mating Connector
BAT1	External battery header, 1*2 pins, 1.25mm pitch for power from external battery (SMP, W125-0210-310-Z)	Molex, 51021-0200 housing for 50058-8000 terminals
CN1/CN2	Standard PC/104 connector, female	Standard PC/104 connector, male
CN4	mini-PCIe socket, 1*52 pins, 0.08mm pitch (shared with mSATA)	8mm, 52-pin mini PCIe edge connector
CN7	Standard SATA connector for the 3Gb/s, SATA1 interface	Standard female SATA
CN8	Standard SATA connector for the 3Gb/s, SATA2 interface (Shared with mSATA)	Standard female SATA
CN10	Gigabit-Ethernet header, 2*5 pins, 2.0mm pitch for GbE1 interface (Molex, 87832-1014)	Molex, 51110-1051 crimp housing for 50394 crimp terminals

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Table 2-1: Header, Connector, Socket, and Switch Definitions (Top Side) **(Continued)**

Connector	Description	Mating Connector
CN11	Gigabit-Ethernet header, 2*5 pins, 2.0mm pitch for GbE2 interface (Molex, 87832-1014)	Molex, 51110-1051 crimp housing for 50394 crimp terminals
CN14	VGA header, 2*5 pins, 2mm pitch (Molex, 87832-1014)	Molex, 51110-1051 crimp housing for 50394 crimp terminals
CN16	USB 2.0 header, 2*10 pins, 2.0mm pitch (Molex, 87832-2014)	Molex, 51110-2051 crimp housing for 50394 crimp terminals
CN18	COM 2 header, 2*5 pins, 2.0mm pitch (Molex, 87832-1014)	Molex, 51110-1051 crimp housing for 50394 crimp terminals
CN19	COM 3 header, 2*5 pins, 2.0mm pitch (Molex, 87832-1014)	Molex, 51110-1051 crimp housing for 50394 crimp terminals
CN20	System panel header, 2*5 pins, 2.0mm pitch (Molex, 87832-1014)	Molex, 51110-1051 crimp housing for 50394 crimp terminals
CN24	ATX Power Input connector, 1*15 pins, 1.5mm pitch (JST, B15B-EH)	JST, EHR-15 with crimp contacts, SHE-001T-P0.6
CN27	FAN connector, 1*4 pins, 1.25mm pitch (Hirose, DF13-4P-1.25DSA)	Hirose, DF13-4S-1.25C with crimp contact DF13-2630SCFA (04)
CN28	Micro-SD card, push-pull (no ejection), hinge-type, standard, right-angle, 1.83mm, 8-pin slot	Micro-SD card
SW2	4-pin, 8.1mm, 25mA 24VDC dip switch for COM 0/1 termination	N/A
SW3	4-pin, 8.1mm, 25mA 24VDC dip switch for COM 2/3 termination	N/A
SW4	4-pin, 8.1mm, 25mA 24VDC dip switch for BIOS Settings	N/A
SW5	4-pin, 8.1mm, 25mA 24VDC dip switch for ISA device memory mapping of SMEMR# and SMEMW# compatibility. SW5 default: 1 and 2=>ON, 3 and 4=>OFF	N/A

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Bottom Side

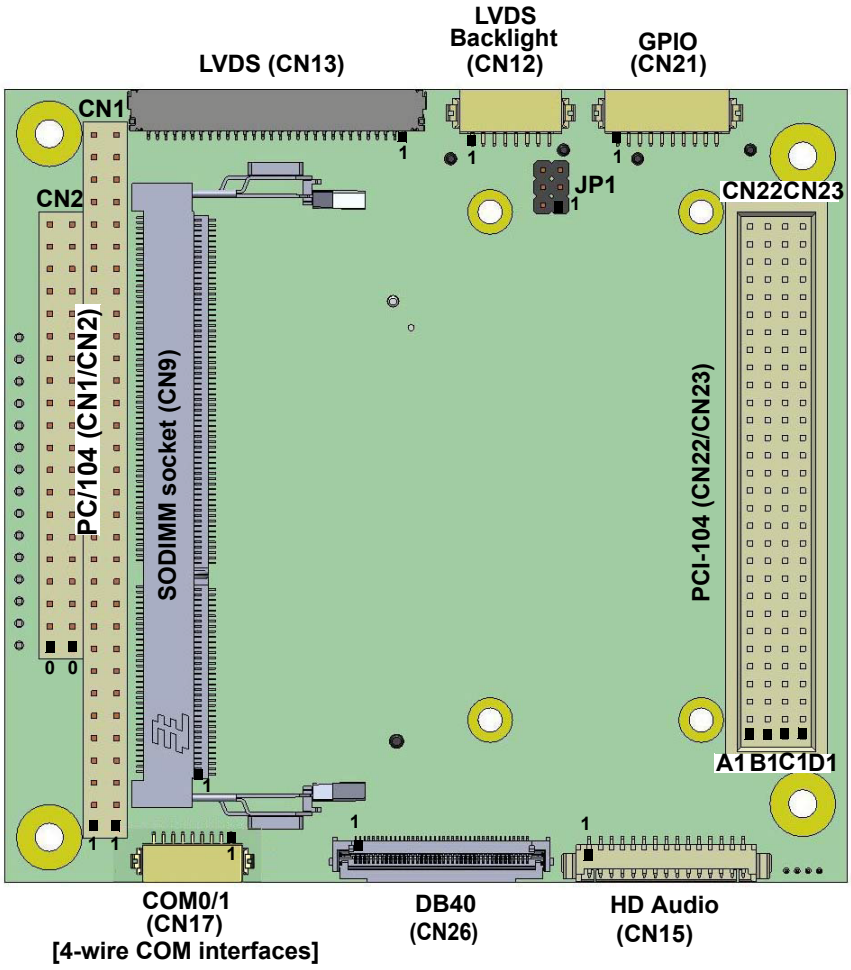


Figure 2-2: Header and Connector Locations (bottom side)

Table 2-2: Header and Connector Definitions (bottom side)

Connector	Description	Mating Connector
CN1/CN2	Standard PC/104 connector, male	Standard PC/104 connector, female
CN9	Standard DDR3L SODIMM socket	DDR3L memory module, non-buffered, non-ECC
CN12	LVDS Backlight connector, Hirose DF13, 1*8 pins, 1.25mm pitch (Hirose, DF13A-8P-1.25H)	Hirose, DF13-8S-1.25C with crimp contact DF13-2630 SCF
CN13	LVDS connector, Hirose DF19, 1*30 pins, 1.0mm pitch (Hirose, DF19G-30P-1H)	Hirose, DF19-30S-1C with crimp contact DF19A-3032 SCF A
CN15	HD Audio connector, Molex PicoBlade Header, 1*15 pins, 1.25mm pitch (Molex 53261-1571)	Molex PicoBlade female connector, (Molex 51021-1500)
CN17	COM0/1 connector, Hirose DF13, 1*9 pins, 1.25mm pitch (Hirose, DF13A9P-1.25H)	Hirose, DF13-9S-1.25C with crimp contact DF13-2630 SCF
CN21	User GPIO connector, Hirose DF13, 1*10 pins, 1.25mm pitch (Hirose, DF13A-10P-1.25H)	Hirose, DF13-10S-1.25C with crimp contact DF13-2630 SCF

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Table 2-2: Header and Connector Definitions (bottom side) (Continued)

Connector	Description	Mating Connector
CN22/CN23	Standard PCI-104 connector, male	Standard PC/104 connector, female
CN26	DB40 debug connector, FFC, 1*40 pins, 0.5mm pitch (Molex, 502790-4091)	FPC/FFC, 0.3mm thick (+/- 0.05mm) with 0.5mm pitch
JP1	LCD and Backlight voltage selection jumper block, 2*3 pins, 2.0mm pitch	2.0mm mini jumper

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2.2 Mechanical Dimensions

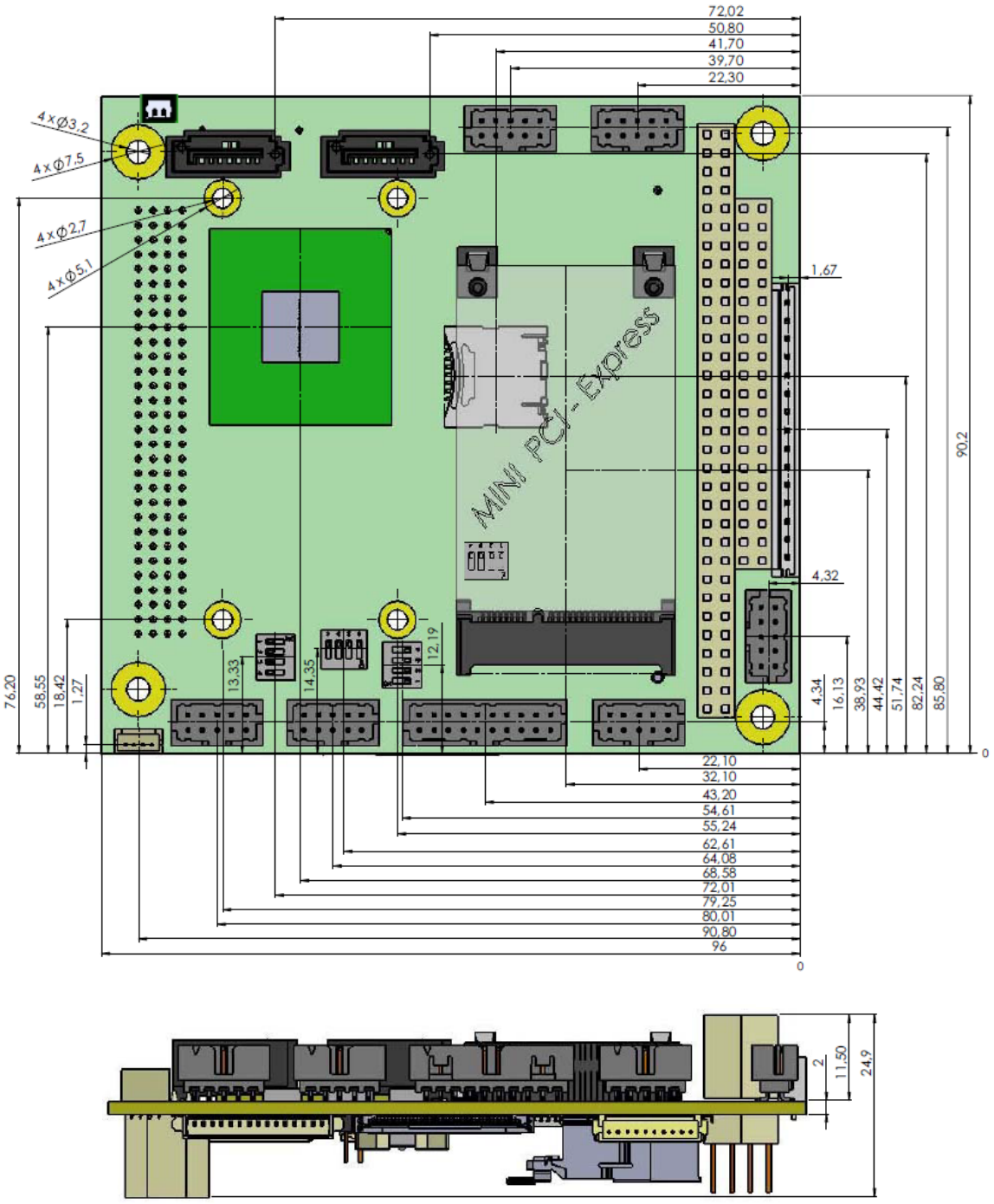


Figure 2-3: Mechanical Dimensions

NOTE:

Mechanical dimensions in Figure 2-3 shown in millimeters.

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2.3 LED Indicators

All LEDs are located on the top-side, board edge shown in Figure 2-1. See Figure 2-4 for LED locations and Table for LED function definitions.

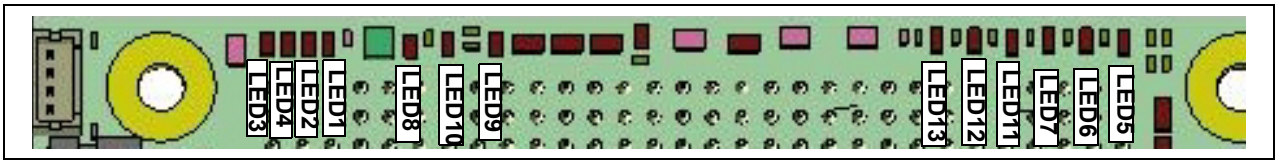


Figure 2-4: LED Locations

Table 2-3: LED Definitions

LED#	Color	Function
LED10	red	Watchdog indicator LED
LED1	green	HDD Activity indicator LED
LED8	blue	BMC Status indicator LED
LED4	green	mini-PCIe WPAN Connection indicator LED
LED3	green	mini-PCIe WLAN Connection indicator LED
LED2	green	mini-PCIe WWAN Connection indicator LED
LED7	yellow	Gbit Ethernet Speed = 1000 Mbit/s indicator on ETH1
LED6	yellow	Gbit Ethernet Activity indicator on ETH1
LED5	green	Gbit Ethernet Speed = 100 Mbit/s indicator on ETH1
LED9	green	Power Good indicator LED
LED13	yellow	Gbit Ethernet Speed = 1000 Mbit/s indicator on ETH2
LED12	yellow	Gbit Ethernet Activity indicator on ETH2
LED11	green	Gbit Ethernet Speed = 100 Mbit/s indicator on ETH2

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2.4 Hardware Setup

CAUTION:
MISE EN GARDE

Be sure to observe the EMC security measures. Make sure you are always at the same potential as the module.

Assurez-vous de respecter les mesures de sécurité CEM. Assurez-vous que vous êtes toujours au même potentiel que le module.

CAUTION:
MISE EN GARDE

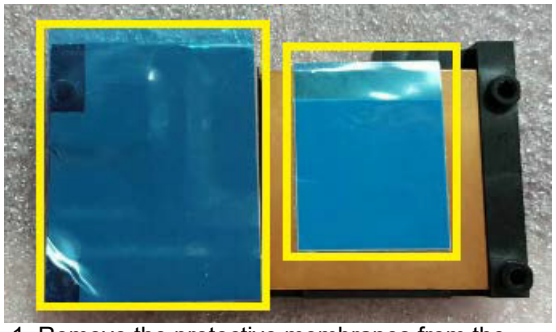
Never connect or disconnect peripherals like HDDs, PCI, and ISA boards while the board's power supply is connected and switched on.

Ne connectez ou ne déconnectez jamais des périphériques tels que des disques durs, des cartes PCI et ISA lorsque l'alimentation de la carte est connectée et sous tension.

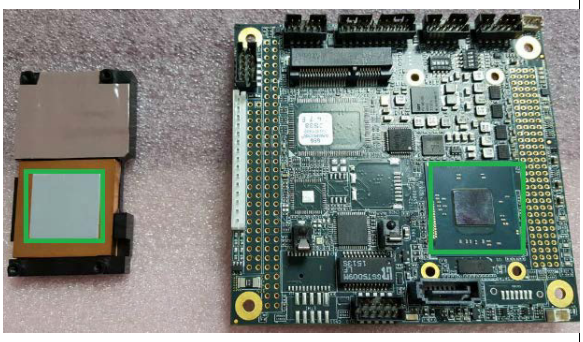
NOTE:

Refer to Table 1-2 on page 3 for a list of cables included in the optional cable set.

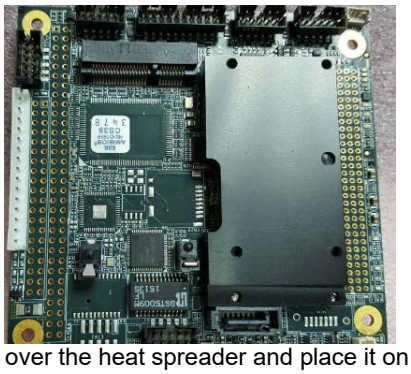
Use the following four steps to mount the heat spreader to the top side of the board, covering the CPU and voltage regulators with the thermal pads on the heat spreader. The heat spreader provides a neutral plane for mounting a custom heat sink.



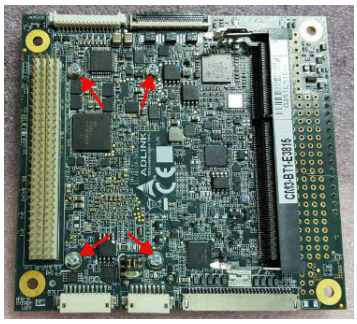
1. Remove the protective membranes from the thermal pads on the heat spreader.



2. Align the thermal pad on the heat spreader, designated for the CPU, with the CPU on the board.



3. Turn over the heat spreader and place it on top of the board so that the four mounting holes line up with the holes on the board and the thermal pads cover the CPU and voltage regulators on the board.



4. Turn over the board and install four M2.5, pan head, L8 mounting screws at 3kgf. cm torque in the four mounting holes on the board.

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Install up to 4GB of DDR3L SODIMM memory in the CN9 SODIMM socket.

Connect a USB keyboard and optionally a USB mouse to the appropriate headers on the board. Use a USB hub to expand the device connections, if necessary. Use the SATA cable to connect the hard disk. Make sure that the pins match their counterparts correctly and are not twisted. If you plan to use additional peripherals, connect them to the appropriate headers.

Connect a 5-volt, 3-amp power supply to the power connector and switch on the power.



The system will function with only 5V power input. Additional 12V input is only necessary if using an external LVDS panel.

The display shows the BIOS messages. If you want to change the standard BIOS settings, press the <DEL> key to enter the BIOS menu. See Chapter 4 for setup details.

If you need to load the BIOS default values, they can be automatically loaded at boot time. The CMx-BTx boots from SATA hard disk drives, CD drives, USB floppies, USB sticks, hard disks, or from a Micro SD card inserted in the optional Micro SD slot, if installed.

Provided that any of these is connected and contains a valid operating system image, the display then shows the boot screen of your operating system.

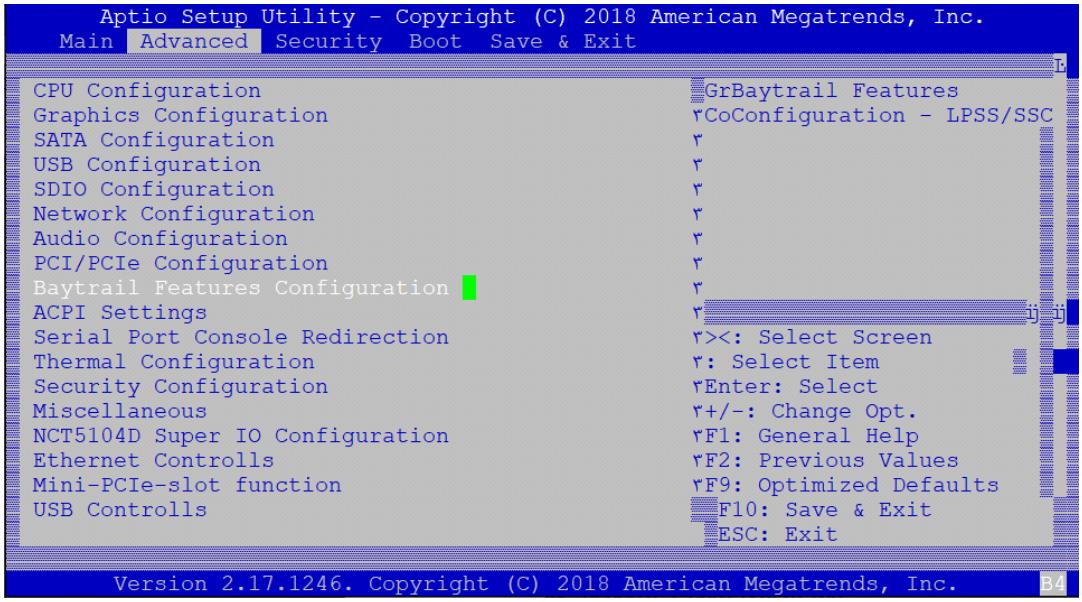
The CMx-BTx needs adequate cooling measures depending on the desired operating temperature range. Using the board without cooling could damage the board permanently. See Table 1-9 on page 5.

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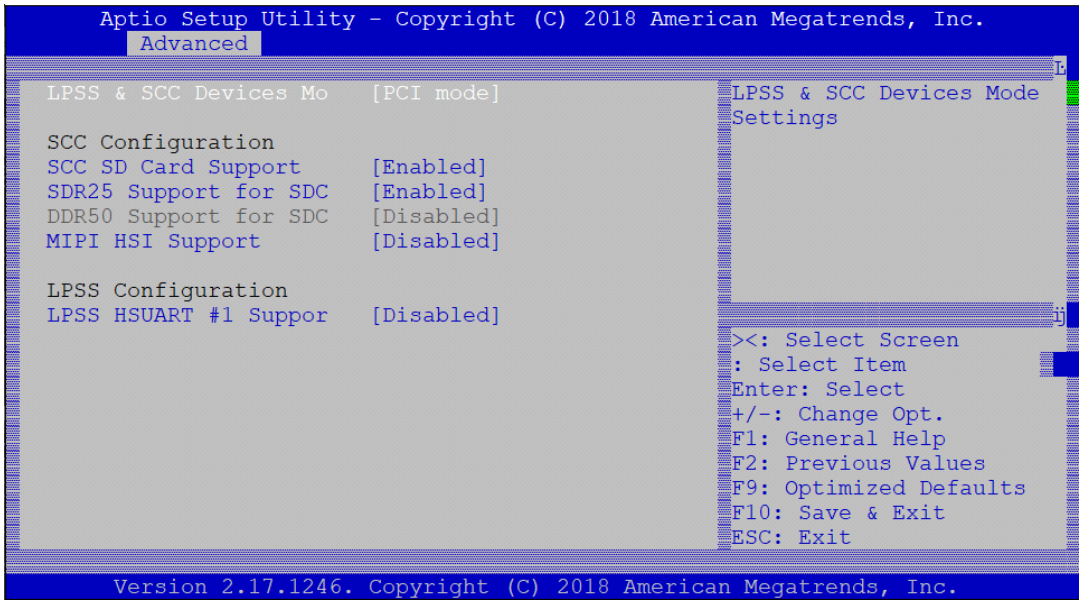
2.5 Windows 10 Installation

To install Windows 10 on the system, change the following settings in the BIOS. Refer to “BIOS Setup” on page 47 for information on how to enter BIOS setup.

"Advanced" >"BayTrail Features Configuration"

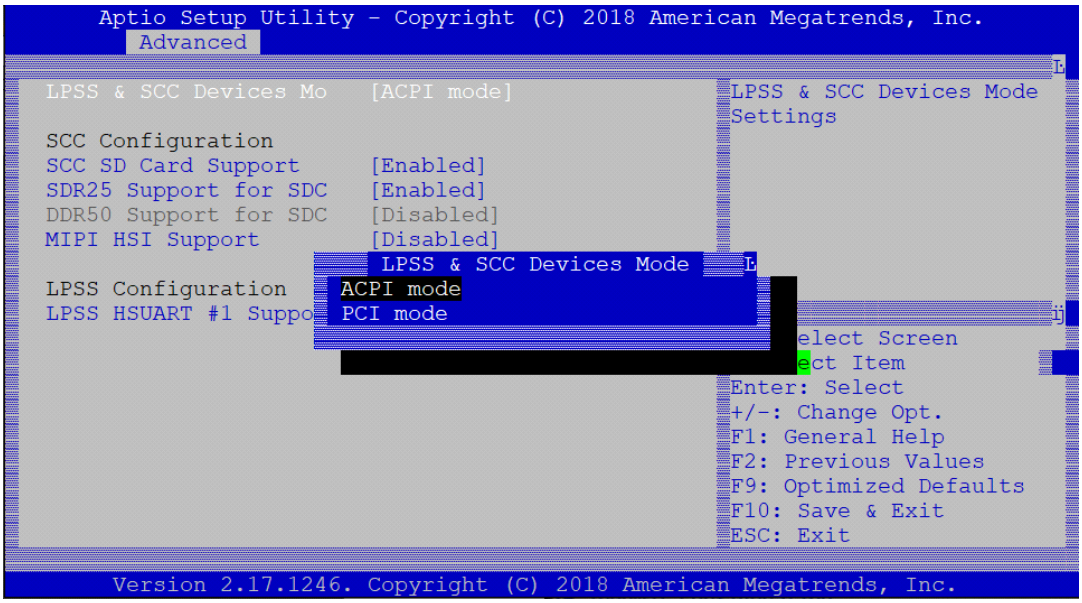


"LPSS & SCC Devices Mode"



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Set to **"ACPI mode"**



You can now perform a fresh installation of Windows 10 64-bit.

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3 Module Description

3.1 SoC (System on a Chip)

The Intel® Atom™ E3800 product series features an Intel® Architecture (IA) that integrates the next generation Intel processor core, graphics engine, memory controller, and I/O interfaces into a single SoC solution, which is based upon the Intel 22nm process technology.

3.1.1 Processor Core

- Up to four IA-compatible low power Intel® processor cores, one thread per core
- Two-wide instruction decode, out of order execution
- On-die, 32 KB 8-way L1 instruction cache and 24 KB 6-way L1 data cache per core
- On-die, 1 MB, 16-way L2 cache, shared per two cores
- 36-bit physical address, 48-bit linear address size support
- Supported C-states: C0, C1, C1E, C6C, C6
- Supports Intel® Virtualization Technology (Intel® VT-X)

3.1.2 Memory Controller

- Supports up to two channels of 64-bit data bus DDR3L-RS SDRAM (only one is supported on the CMx-BTx family of modules)
- Supports x16 DDR3L-RS SDRAM devices
- Supports DDR3L-RS with 1066 or 1333 MT/s data rates (type is bound to the specific SoC)
- Total memory bandwidth supported is 8.5 GB/s for 1066 MT/s single channel up to 21.3 GB/s for 1333 MT/s dual channel (not supported on the CMx-BTx family of boards)
- Supports different physical mappings of bank addresses to optimize performance
- Out-of-order request processing to increase performance
- Aggressive power management to reduce power consumption
- Proactive page closing policies to close unused pages

3.1.3 Graphics Engine

- Intel's 7^{th} generation (Gen 7) graphics and media encode/decode engine
- VED video decoder in addition to Gen 7 Media decoder
- Supports DX 11, OpenGL 3.0 (OGL 3.0), OpenCL 1.2 (OCL 1.2), OpenGLES 2.0 (OGLES 2.0)
- GPU shader is capable of up to 8 gigaflops
- 4x anti-aliasing
- Full HW acceleration for decode of H.264, MPEG2, MVC, VC-1, VP8, MJPEG
- Full HW acceleration for encode of H.264, MPEG2, MVC
- Supports 2.0 Stereoscopic 3D stretch
- Polyphase 8 tap scaling
- HD HQV
- Intel® Burst Technology
- Intel® Display Power Saving Technology (Intel® DPST) 6.0
- Intel® Display Refresh Rate Switching Technology (Intel® DRRS Technology)
- PSR (Panel self refresh)

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3.1.4 Image Signal Processor

- Integrated MIPI-CSI 2.0 interface (not supported on the CMx-BTx modules)

3.1.5 Power Management

- ACPI 5.0 support
- Processor states: C0 – C6
- Display device states: D0, D3
- Graphics device states: D0, D3
- System sleep states: S0, S3, S4, S5 (S4 and S5 are the same for this SoC)
- Dynamic I/O power reductions (disabling sense amps on input buffers, tri-stating output buffers)
- Conditional memory self-refresh during C2
- Active power-down of display links
- Downloadable power management firmware

3.1.6 PCI Express

On the CMx-BTx, the PCI Express bus is configured as four root ports, where each is configured as a x1 port (2.5 GT/s). The function of each port is shown in the table below:

Table 3-1: PCIe Port Functions

Root port#	Function/Description
Port 0	Gigabit Ethernet Channel 0 (ETH1)
Port 1	Gigabit Ethernet Channel 1 (ETH2)
Port 2	PCI Express to PCI Bridge for the PCI-104 Interface (XIO2001)
Port 3	mini-PCIe socket for PCI Express extension cards

Each of the four ports supports the WAKE function.

3.1.7 SATA Controller

- Up to two SATA 3 Gb/s ports
- Legacy IDE (including IRQ)/Native IDE/AHCI appearance to OS
- Partial/Slumber power management modes with wake
- Supports RunTime D3

3.1.8 USB xHCI Controller

- Supports USB 2.0/1.1
- Implements xHCI software host controller interface
- Four ports multiplexed with EHCI controller that are High Speed/Full Speed (HS/FS)

3.1.9 USB 2.0 EHCI Controller

- Internal Rate Matching Hub to support USB 1.1 to 2.0 devices
- Four Ports multiplexed with xHCI controller
- Enhanced EHCI descriptor caching

3.1.10 HD-Audio Controller

- Four In and four Out streams, where only three are used
- No wake on audio (modem) support

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3.1.11 Intel® Trusted Execution Engine (Intel® TXE)

Intel TXE system contains a security engine and additional hardware security features that enable a secure and robust platform. The security features include:

- Isolated execution environment for crypto operations (SKU-enabled)
- Supports secure boot – with customer programmable keys to secure code

NOTE:

The SoC requires TXE firmware in the PCU SPI flash image to function.

3.1.12 Platform Control Unit (PCU)

The SoC provides the following PCU HW blocks:

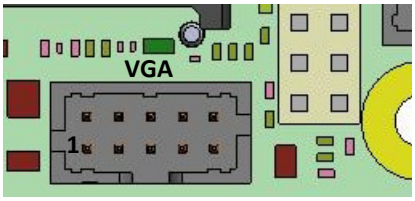
- SMBus
- SPI interface for flash only (boot FW and system configuration data)
- RTC, Interrupts, Timers, GPIOs, and LPC interface

3.2 VGA Interface

The CMx-BTx supports a VGA interface originating from the SoC and provides the signals through the CN14, 10-pin, 2.0mm header.

Table 3-2: VGA Header Signals (CN14)

Pin	Signal	Pin	Signal
1	Red	2	GND
3	Green	4	GND
5	Blue	6	VGA_DDC_CLK
7	HSYNC	8	VGA_DDC_DATA
9	VSYNC	10	GND



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3.3 LVDS Interface

The LVDS interface is connected to the DDI0 interface of the SoC, while the translation is made by a NXP PTN3460IBS (e)DisplayPort™ to LVDS converter.

The NXP PTN3460IBS supports the following features:

- 2-Lane Display Port receiver
- 2-Port LVDS output interface
- Max. Resolution up to 1920 x 1200 x 60 (RB), 18-bit color depth (24-bit color depth on smaller resolutions)
- Supports 2-lane digital input, with speeds up to 1.62/2.7Gbps
- Supports dual port, 6/8-bits LVDS output
- QFN-48 Pin package

The LVDS interface is accessible at connector CN13 (Bottom Side), which is a Hirose DF19-30 (1.0 mm pitch) with the following pin definitions:

Table 3-3: LVDS Signal Definitions (CN13)

Pin#	Interface	Signals	Comment
1	**Panel Power Supply**	+VCC_LCD_L_CN	Can be configured at the "CN_PANEL_VCC_SEL1" jumper block (JP1)
2		+VCC_LCD_L_CN	
3		GND	
4	**Power Supply/Shield**	GND	
5	**Data Channel A**	LA_DATA3_N_L	
6		LA_DATA3_P_L	
7		LA_CLK_N_L	
8		LA_CLK_P_L	
9		GND	
10		LA_DATA2_N_L	
11		LA_DATA2_P_L	
12		LA_DATA1_N_L	
13		LA_DATA1_P_L	
14		LA_DATA0_N_L	
15		LA_DATA0_P_L	
16	**Shield**	GND	

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Table 3-3: LVDS Signal Definitions (CN13) (Continued)

Pin#	Interface	Signals	Comment
17	**Data Channel B**	LB_DATA3_N_L	
18		LB_DATA3_P_L	
19		LB_CLK_N_L	
20		LB_CLK_P_L	
21		GND	
22		LB_DATA2_N_L	
23		LB_DATA2_P_L	
24		LB_DATA1_N_L	
25		LB_DATA1_P_L	
26		LB_DATA0_N_L	
27		LB_DATA0_P_L	
28	**Shield**	GND	
29	**DDC Channel**	LVDS_DDC_L_CLK	
30		LVDS_DDC_L_DATA	
31	**Case/Shield**	GND	
32		GND	
Connector			



3.4 LVDS Backlight

The backlight can be enabled/disabled from the BIOS setup. The backlight dimming source can be configured from the BIOS setup. These options originate from the SoC or from the BMC.

The connector (CN12) to which the backlight can be attached, is a Hirose DF13-8 with the following pin out:

Table 3-4: LVDS Backlight Signal Definitions (CN12)

Pin#	Signal	Comment
1	**+VCC_BLK**	Routed from JP1 as configured through the jumper setting on JP1 (5V or 12V, 12V = default)
2		
3		
4		
5	**LVDS_BKLT_CTRL**	PWM output for Backlight dimming (SoC | BMC)

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Table 3-4: LVDS Backlight Signal Definitions (CN12) (Continued)

Pin#	Signal	Comment
6	BKL_EN_OUT	Backlight enable signal; turns on simultaneously with the +VCC_LCD voltage
7	GND	
8	GND	
Connector		

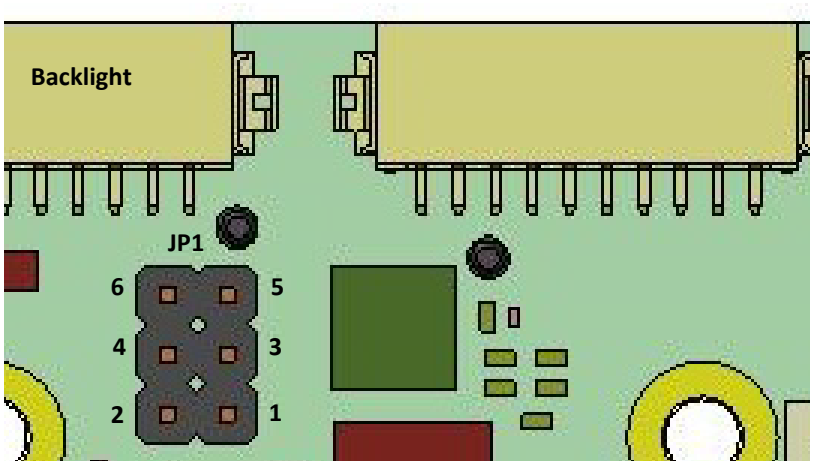


3.4.1 Selecting Panel and Backlight voltage

At the jumper block “CN_PANEL_VCC_SEL1” (JP1), both voltages can be configured using a 2mm jumpers.

Table 3-5: LVDS Backlight Voltage Select Signals (JP1)

Pin#	Signal	Pin#	Signal
1	+V3P3S (default)	2	+V12P0_ATX (default)
3	+VCC_LCD	4	+VCC_BKL
5	+V5P0_ATX	6	+V5P0_ATX



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3.5 Ethernet Controllers

Up to two Intel® I210IT Gigabit Ethernet controllers are supported with the following capabilities:

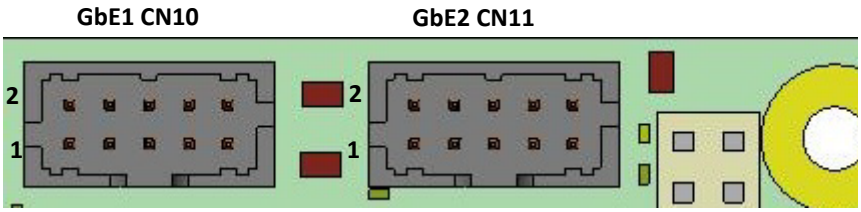
- PCIe v2.1 (2.5 GT/s) x1, with switching Voltage Regulator (iSVR)
- Integrated Non-Volatile Memory (iNVM)
- Platform Power Efficiency
  - IEEE 802.3az Energy Efficient Ethernet (EEE)
  - Proxy: ECMA-393 and Windows logo for proxy offload
  - Converged Platform Power Management (CPPM)/(DMAC, LTR, OBFF)
- Advanced Features:
  - -40°C to 85°C Industrial temperature
  - Audio-video bridging
    - IEEE 1588/802.1AS precision time synchronization
    - IEEE 802.1Qav traffic shaper (with software extensions)
  - Jumbo frames
  - Interrupt moderation, VLAN support, IP checksum offload
  - PCIe OBFF (Optimized Buffer Flush/Fill) for improved system power management
  - Four transmit and four receive queues
  - RSS and MSI-X to lower CPU utilization in multi-core systems
  - Advanced cable diagnostics, auto MDI-X
  - ECC – error correcting memory in packet buffers
  - Four Software Definable Pins (SDPs)
- Manageability:
  - NC-SI for greater bandwidth pass through
  - SMBus low-speed serial bus to pass network traffic
  - Flexible firmware architecture with secure Flash update
  - MCTP over SMBus/PCIe
  - OS2BMC/CEM (optionally enabled via external Flash)
  - PXE and iSCSI boot

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Each Ethernet interface is accessible through a 2*5, 2.0 mm pin header from Molex.

Table 3-6: Ethernet Signal Definitions (CN10/CN11)

Pin#	Signal	Pin#	Signal
1	MX1-	**2**	MX1+
3	MX2-	**4**	MX2+
5	n.c. (optional PE)	**6**	n.c.
7	MX3-	**8**	MX3+
9	MX4-	**10**	MX4+
Connector			



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3.6 USB Ports

The module supports up to four USB connections: three USB 2.0 High Speed ports, and one USB 2.0 High Speed port routed to the mini-PCIe socket.

The three USB 2.0 ports are combined on a 2*10 pin, 2.0 mm pitch header from Molex.

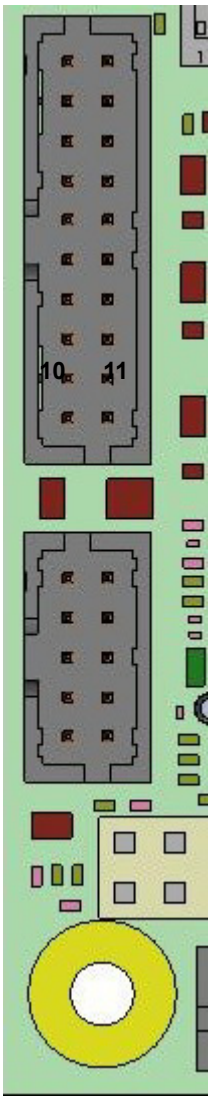
CAUTION:
MISE EN GARDE

It is not recommended to draw more than 2.0 A in total over all three USB ports, where each port is limited to approximately 680 mA. (Exception: On USB#0, 1000 mA is allowed.)

Il n'est pas recommandé de tirer plus de 2,0 A au total sur les trois ports USB, où chaque port est limité à environ 680 mA. (Exception: sur USB # 0, 1000 mA est autorisé.)

The signals of this header are defined in the following table.

Table 3-7: USB Signal Definitions (CN16)

Pin	Interface	Signals	CN16 Connector	Pin	Interface	Signals
1	USB #0	+VCC_USB0		20	USB #1 & #2	N.C.
2		USB3_P0_L_RXN		19		+VCC_USB1
3		USB3_P0_L_RXP		18		N.C.
4		GND		17		+VCC_USB2
5		USB3_P0_L_TXN		16		GND
6		USB3_P0_L_TXP		15		USB2_P2_L_DN
7		GND		14		USB2_P2_L_DP
8		USB2_P0_L_DN		13		GND
9		USB2_P0_L_DP		12		USB2_P1_L_DN
10		N.C.		11		USB2_P1_L_DP

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3.7 On-Board Power Supply

There are two resistor configuration options available for the CMx-BTx that can be selected at the time of build (available on A5 version only).

In the default configuration, the CMx-BTx devices can be run with only 5 volts. If a Standby mode is needed, the 5V Standby voltage has to be connected in addition to the 5V supply. In this configuration, externally generated PCI_3V3 should not be applied to the CMx-BTx.

The +12V supply is only needed for driving an LCD backlight.

All other voltages needed to run the module are generated on the module itself.

In an alternate configuration (contact ADLINK for further information), PCI_3V3 power is not generated on the module and instead can and should be powered externally by the stackable PCI-104 connector (available on A5 version only).

In both configurations, main +5V and LCD backlight +12V power can be supplied over the power connector, PCI-104 connector, or the PC/104 connector. 5V Standby power can be supplied over the power connector or the PCI-104 connector, but not the PC/104 connector.

The power connector is a JST-B15B-EH, 1.5 mm pitch single row connector. The cable kit provides an adapter cable to convert from this to a standard 20-pin ATX connector.

Table 3-8: Power Signal Definitions (CN24)

Pin#	Signal	Pin#	Signal
1	+V5P0_ATX	**2**	GND
3	+V5P0_ATX	**4**	GND
5	+V5P0_ATX	**6**	+V5P0ATX_SBY
7	GND	**8**	ATX_PSON#
9	ATX_PWRGD	**10**	+V3P3_ATX
11	GND	**12**	+V12P0_ATX
13	+V12P0_ATX	**14**	GND
15	-V12P0_ATX		
Connector			



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3.8 System Panel

The System Panel interface provides signals for external speakers, HDD LEDs, and power and reset buttons. The HDD-LED (K) on pin 7 includes a 680 Ohm series resistor for current limiting. The Anode of the LED should be connected to pin 2 (+V3P3S.)

For the speaker, ADLINK recommends speaker impedance at 8Ohm to 50Ohm and speaker power rating up to 1.0W.

The +V3P3S signal on pin 2 is fused with a slow-acting PTC-like, 750mA fuse. The same is true for the SPKR-OUT (+) signal on pin 3, but it is not recommended to draw more than 200mA from pin 3.

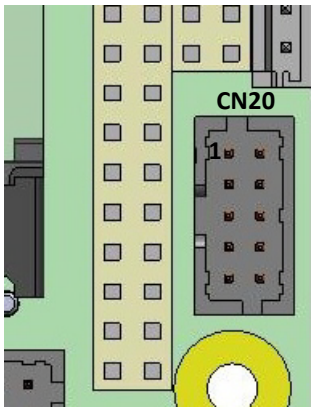
The cable set provided includes a cable for the system panel, which includes a power and reset button, while the other wires are open-end. The PMC_RSTBTN_IN# (reset) includes a 1k pull-up resistor to a switched 3.3V, while the PS_PWRBTN_IN# includes a 3k3 pull up to an always on 3.3V.



To connect an external RTC battery, use the system panel, open-end cable wires connected to pin 5 and pin 8 on CN20.

Table 3-9: System Panel Interface (CN20)

Pin	Signal	Pin	Signal
1	SPKR-IN (-)	2	+V3P3S
3	SPKR-OUT (+)	4	GND
5	+VCC_RTC_EXT	6	PS_PWRBTN_IN#
7	HDD-LED (K)	8	GND
9	WDTOUT	10	PMC_RSTBTN_IN#



The following table defines the pin assignments of the System Panel functions.

Table 3-10: System Panel Pin Assignments

Function	Related Pins
Power Button	4 and 6
Speaker	1 and 3
Reset	4 and 10
RTC-Battery	5 and 8
Watchdog-Out	8 and 9
HDD-LED	2 and 7

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3.9 Serial Ports

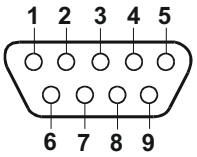
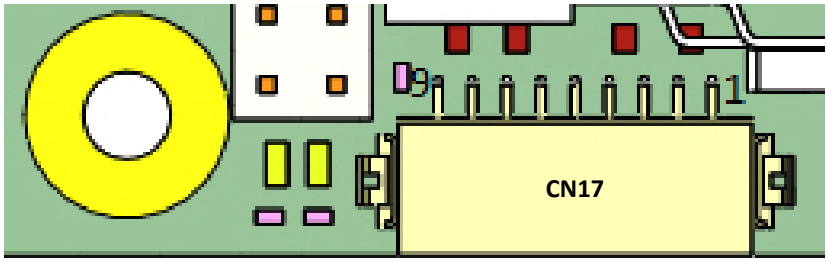
The CMx-BTx module provides up to four serial ports through an LPC-to-UART Bridge (NCT5104D from Nuvoton.) All four serial ports are capable of running as RS232 or RS422, and each supports the following features:

- 16650-compatible UART with 128-byte send/receive FIFO
- Programmable baud rate generator
- 5, 6, 7 or 8-bit characters
- Even, odd or no parity bit generation / detection
- 1, 1.5 or 2 stop-bit generation
- Loop-back controls for communications link fault isolation
- Break, parity, overrun, framing error simulation
- Speeds up to 115.2 kbaud in normal mode
- Up to 1.5 Mbaud in high speed mode (requires a custom BIOS, available on request)

The two COM ports COM2 and COM3 are fully implemented COM ports, supporting all nine defined signals, while the two COM ports COM0 and COM1 support only RXD, TXD and their corresponding handshake signals RTS# and CTS#.

The COM0 and COM1 are bundled on a Hirose DF13-9 connector (V) with the following pin out:

Table 3-11: COM0 and COM1 Serial Port Signal Definitions (CN17)

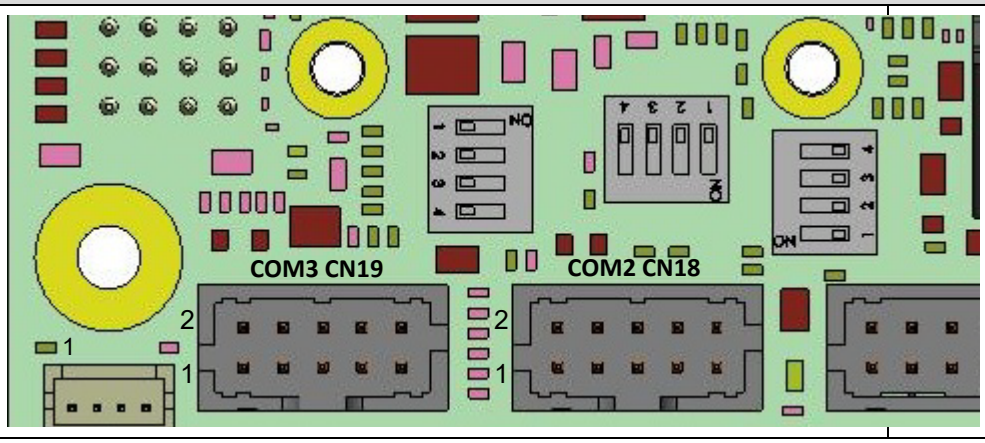
Pin#	RS232	RS422		DB9 - COM0	DB9 - COM1
1	COM0_RX	COM0_RX-		Pin 2	N/A
2	COM0_RTS#	COM0_TX+		Pin 7	N/A
3	COM0_TX	COM0_TX-		Pin 3	N/A
4	COM0_CTS#	COM0_RX+		Pin 8	N/A
5	GND	Not Used		Pin 5	Pin 5
6	COM1_RX	COM1_RX-		N/A	Pin 2
7	COM1_RTS#	COM1_TX+		N/A	Pin 7
8	COM1_TX	COM1_TX-		N/A	Pin 3
9	COM1_CTS#	COM1_RX+		N/A	Pin 8
				Standard DB9 	
Connector					
					

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Each of the COM2 and COM3 ports provides a Molex MilliGrid header with shroud and lock. The header pin signals are defined in the following table.

Table 3-12: COM2 and COM3 Serial Port Signal Definitions (CN18/CN19)

Pin#	RS232	DB9 Pin	Pin#	RS232	DB9 Pin
1	DCD#	1	**2**	DSR#	6
3	RXD	2	**4**	RTS#	7
5	TXD	3	**6**	CTS#	8
7	DTR#	4	**8**	RI#	9
9	GND	5	**10**	+V5P0S	Not connected
Connector					



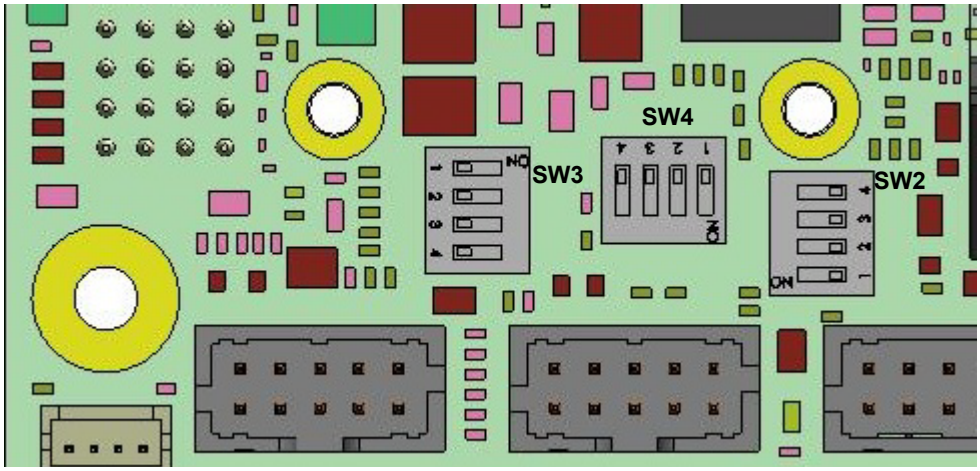
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3.10 Setting RS422 Termination

If the COM ports are used in RS422 modes, the termination resistors must be switched on. These are located at DIP-Switches SW2 and SW3 (SW4 is for BIOS configuration. See note.) The default setting is “OFF” (RS232-Mode) as illustrated in the following table.

Table 3-13: SW2 and SW3 RS422 Signal Definitions

Position	Position	Signal(s)	Function
1	**8**	SW2: COM0-TX SW3: COM2-TX	Pos. 1: TX-termination off Pos. 8: TX-termination on
2	**7**	SW2: COM0-RX SW3: COM2-RX	Pos. 2: RX-termination off Pos. 7: RX-termination on
3	**6**	SW2: COM1-TX SW3: COM3-TX	Pos. 3: TX-termination off Pos. 6: TX-termination on
4	**5**	SW2: COM1-RX SW3: COM3-RX	Pos. 4: RX-termination off Pos. 5: RX-termination on
DIP-Switches			



NOTE: The shaded table cells signify the default positions. Refer to Chapter 4 for the definition of the SW4 switch.

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3.11 Mini-PCIe Interface

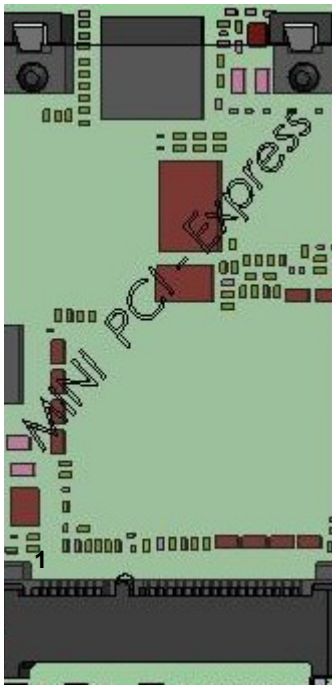
The Mini-PCIe interface, located on the top side of the module, provides expansion for PCIe, USB 2.0, and SSD devices as well as wireless applications. LEDs for WWAN, WLAN, and WPAN are implemented on the module, and the two disable lines for wireless expansion can be configured from the BIOS setup. Two modes can be configured from the BIOS setup for this socket:

- PCIe x1 mode
- mSATA mode, which shares the SATA interface with the SATA2 connector. When the socket is in mSATA mode, the SATA2 connector is disconnected from the SATA interface.

NOTE: Refer to Table 4-37 for Mini PCIe slot configuration settings.

The following table defines the Mini PCIe interface signals.

Table 3-14: Mini PCIe Signal Definitions (CN4)

Pin	Signal	Pin	Signal	Connector
1	MPCIE_WAKE# (3)	2	+V3P3S	
3	N. C.	4	GND	
5	N. C.	6	+V1P5S	
7	MPCIE_CLKREQ# (3)	8	N. C.	
9	GND	10	N. C.	
11	PCIE_CLK3_N-	12	N. C.	
13	PCIE_CLK3_P	14	N. C.	
15	GND	16	N. C.	
Mechanical Key				
17	N. C.	18	GND	
19	N. C.	20	DISABLE_RADIO1#	
21	GND	22	BUF_PLTRST#	
23	MINICARD_RX_N	24	+V3P3S	
25	MINICARD_RX_P	26	GND	
27	GND	28	+V1P5S	
29	GND	30	SMB_CLK	
31	MINICARD_TX_N	32	SMB_DATA	
33	MINICARD_TX_P	34	GND	
35	GND	36	USB2_P3_DN	
37	GND	38	USB2_P3_DP	
39	+V3P3S	40	GND	
41	+V3P3S	42	LED-W-WAN	
43	GND	44	LED-W-LAN	
45	N. C.	46	LED-W-PAN	
47	N. C.	48	+V1P5S	
49	N. C.	50	GND	
51	DISABLE_RADIO2#	52	+V3P3S	

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3.12 PCI-104 Bus Interface

The CMx-BTx modules use a PCIe-to-PCI Bridge from Texas Instruments -- XIO2001 -- to achieve PCI bus compatibility, providing full PCI Express and PCI local bus functionality and performance.

The following list presents the key features of the PCI-104 bus interface.

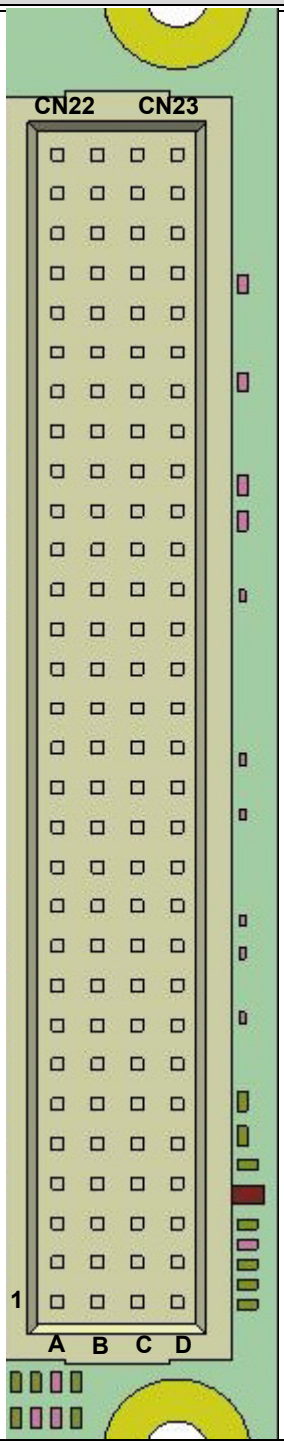
- Fully compliant with the PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0
- Fully compliant with the PCI Express Base Specification, Revision 2.0
- Fully compliant with the PCI Local Bus Specification, Revision 2.3
- Full x1 PCI Express throughput
- Capable of advanced error reporting
- Supports WAKE event and Beacon support
- Supports D1, D2, D3hot and D3cold
- Supports up to six external PCI Masters
- Advanced PCI Express Message Signaled Interrupt Generation for Serial IRQ Interrupts
- PCI Bus Interface 3.3V and 5.0V (25MHz or 33MHz only at 5.0V [solder jumper option]) Tolerance Options
- Active-State Link Power Management Saves Power When Packet Activity on the PCI Express Link is Idle, Using Both L0s and L1 States
- PCI-Express CLKREQ Support

The PCI-104 connector is located on the bottom side of the module, as shown in the drawing in the following table.

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The following table defines the signals of the PCI-104 interface.

Table 3-15: PCI-104 Signal Definitions (CN22 / CN23)

Pin	Row A	Row B	Row C	Row D	Connector
1	GND	+V5P0_SBY_	+V5P0_ATX	AD00	
2	+XPCI_VIO	AD02	AD01	+V5P0_ATX	
3	AD05	GND	AD04	AD03	
4	C/BE0#	AD07	GND	AD06	
5	GND	AD09	AD08	GND	
6	AD11	+XPCI_VIO	AD10	M66EN	
7	AD14	AD13	GND	AD12	
8	+V3P3_PCI	C/BE1#	AD15	+V3P3_PCI	
9	SERR#	GND	ATX_PSON#	PAR	
10	GND	PERR#	+V3P3_PCI	PME#	
11	STOP#	+V3P3_PCI	LOCK#	GND	
12	+V3P3_PCI	TRDY#	GND	DEVSEL#	
13	FRAME#	GND	IRDY#	+V3P3_PCI	
14	GND	AD16	+V3P3_PCI	C/BE2#	
15	AD18	+V3P3_PCI	AD17	GND	
16	AD21	AD20	GND	AD19	
17	+V3P3_PCI	AD23	AD22	+V3P3_PCI	
18	IDSEL0	GND	IDSEL1	IDSEL2	
19	AD24	C/BE3#	+XPCI_VIO	IDSEL3	
20	GND	AD26	AD25	GND	
21	AD29	+V5P0_ATX	AD28	AD27	
22	+V5P0_ATX	AD30	GND	AD31	
23	REQ0#	GND	REQ1#	+XPCI_VIO	
24	GND	REQ2#	+V5P0_ATX	GNT0#	
25	GNT1#	+XPCI_VIO	GNT2#	GND	
26	+V5P0_ATX	CLK0	GND	CLK1	
27	CLK2	+V5P0_ATX	CLK3	GND	
28	GND	INTD#	+V5P0_ATX	RST#	
29	+V12P0_ATX	INTA#	INTB#	INTC#	
30	-V12P0_ATX	REQ3#	GNT3#	GND	

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3.13 PC/104 Bus Interface

The PC/104 Bus Interface is implemented using a Fintek F85226FG LPC-to-ISA Bridge, capable of delivering a fully ISA, 16-bit compatible interface.

The Intel E3800 family of SoCs does not support the following features of the PC/104 interface:

- Bus Master Cycles
- DMA
- Memory Mapped transactions on the LPC bus
- IRQ0, Heartbeat Interrupt, which is generated off of the internal 8254 counter 0
- IRQ8, RTC interrupt can only be generated internally
- IRQ13, this Interrupt (floating point error) is not supported
- IRQ14, this Interrupt can only be generated by the SATA controller in Legacy mode
- ISA Enable (IE) bit is missing and therefore no automatic compensation for I/O address aliasing is available
- PnP

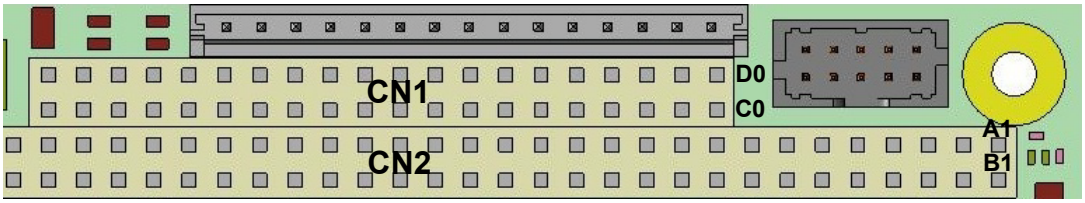
Table 3-16 defines the signals of the PC/104 connector.

Table 3-16: PC/104 Signal Definitions (CN1 / CN2)

Pin	Row D	Row C	Pin	Row A	Row B
			1	IOCHK#	GND
			2	D7	RSTDRV
			3	D6	+V5P0_ATX
			4	D5	IRQ9
			5	D4	N. C. (-5V)
			6	D3	DRQ2
			7	D2	-V12P0_ATX
			8	D1	0WS#
0	GND	GND	9	D0	+V12P0_ATX
1	MEMCS16#	SBHE#	10	IOCHRDY	KEY
2	IOCS16#	LA23	11	AEN	SMEMW#
3	IRQ10	LA22	12	A19	SMEMR#
4	IRQ11	LA21	13	A18	IOW#
5	IRQ12	LA20	14	A17	IOR#
6	IRQ15	LA19	15	A16	DACK3#
7	IRQ14	LA18	16	A15	DRQ3
8	DACK0#	LA17	17	A14	DACK1#
9	DRQ0	MEMR#	18	A13	DRQ1
10	DACK5#	MEMW#	19	A12	REFRESH#
11	DRQ5	SD8	20	A11	SYSCLK
12	DACK6#	SD9	21	A10	IRQ7
13	DRQ6	SD10	22	A9	IRQ6
14	DACK7#	SD11	23	A8	IRQ5
15	DRQ7	SD12	24	A7	IRQ4
16	+V5P0_ATX	SD13	25	A6	IRQ3
17	MASTER#	SD14	26	A5	DACK2#
18	GND	SD15	27	A4	TC
19	GND	KEY	28	A3	BALE

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Table 3-16: PC/104 Signal Definitions (CN1 / CN2) (Continued)

Pin	Row D	Row C	Pin	Row A	Row B
			29	A2	+V5P0_ATX
			30	A1	OSC
			31	A0	GND
			32	GND	GND
Connector					
					

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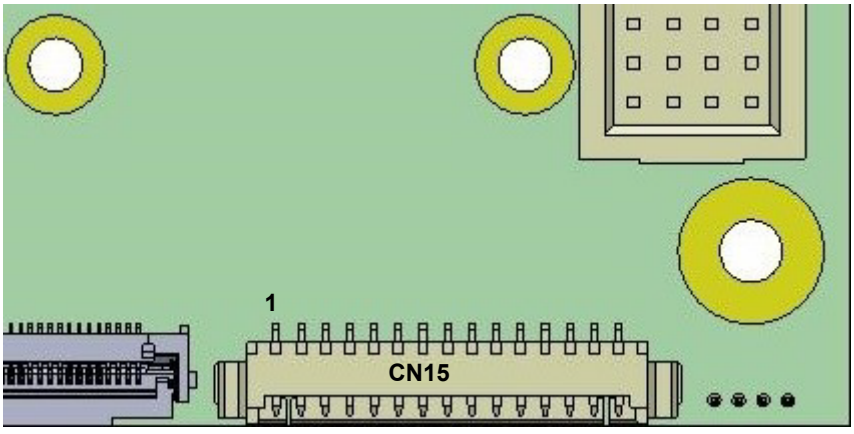
3.14 Audio Interface

The module provides an audio solution through a 5.1+2 channel HD audio codec and a fifteen pin, single-row header.

The signals of this header are defined in the following table.

Table 3-17: Audio Header Signal Definitions (CN15)

Pin	Signal	Function
1	FRONT_R	Front audio out, right channel
2	FRONT_L	Front audio out, left channel
3	SURR_R	Surround right channel
4	SURR_L	Surround left channel
5	LFE	Low Frequency output
6	CENTER	Center audio out
7	GND	Ground
8	LINE_IN_R	Stereo Line In right channel
9	LINE_IN_L	Stereo Line In left channel
10	MIC_R	Stereo Microphone In right channel
11	MIC_L	Stereo Microphone In left channel
12	GND	Ground
13	SPDIF_IN	Digital audio in
14	SPDIF_OUT	Digital audio out
15	GND	Ground
Connector		



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3.15 BMC Service Connector

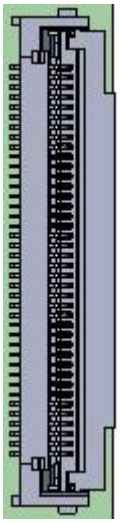
The BMC Service connector is a 40-pin, 0.5 mm pitch Front-Flip Connector. The additional DB40 Debug Card from ADLINK allows access to the following functions.

- BIOS POST codes
- BIOS Flash programming without powering up the module (required for flashing new BIOS versions)
- Power Supply and System Status Test Points
- Firmware update of the BMC
- BMC Debug Information
- SMBus interface of the module

The following table defines the signals of the BMC debug connector.

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Table 3-18: Service Debug Connector Signals (CN26)

Pin#	Interface	Signals	Connector
1	**NC**	RESVD	40  1
2	**BMC Debug**	BMC_STATUS	
3		BIOS_MODE	
4		SEL_BIOS	
5		POSTWD_DIS#	
6	**Test point**	SUS_S5#	
7		SUS_S4#	
8		SUS_S3#	
9		CB_PWROK	
10		CB_RESET#	
11		SYS_RESET#	
12		PWRBTN#	
13	**BMC programming**	BMC_TMS/SWDIO	
14		BMC_TCK/SWCLK	
15		CLK (SMBus)	
16		DATA (SMBus)	
17		RESET_IN#	
18		BMC_TDO/SWO	
19		BMC_TDI	
20		BMC_TX2	
21		GND	
22		+V3P3A	
23		+V3P3BMC	
24	**LPC Debug card**	LPC_AD0	
25		LPC_AD1	
26		LPC_AD2	
27		LPC_AD3	
28		LPC_FRAME#	
29		CLK33_LPC	
30		RST#	
31		BIOS_DIS0	
32		GND	
33		+V3P3S	
34	**SPI programming**	SPI_BIOS_CLK	
35		SPI_BIOS_MOSI	
36		SPI_BIOS_MISO	
37		SPI_BIOS_CS1#	
38		SPI_BIOS_CS0#	
39		GND	
40		+V3P3S_SPI_CN	

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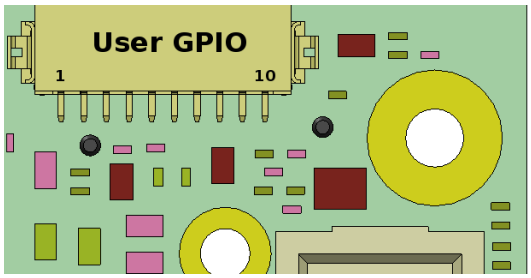
3.16 User GPIO Interface

The CMx-BTx offers eight user-accessible GPIOs, from SoC to BMC/SEMA to GPIO output. Need to use SEMA to use GPIO function.

For interface flexibility, these IOs run at 3.3V input but are 5.0V tolerant (5.0V input is the default support.) By changing the solder jumpers at R317/R318, the input voltage support can be changed to 3.3V or 5.0V permanently. However, 5.0V output voltage is not supported, and the maximum output voltage supported is 3.3V.

The GPIO interface supports a Hirose DF13-10 connector, and the following table defines the GPIO signals.

Table 3-19: GPIO Signal Definitions (CN21)

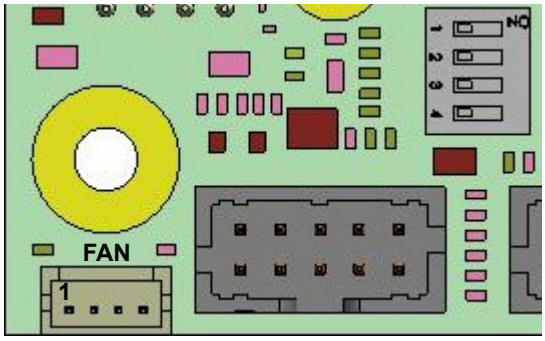
Pin	Signal	Connector
1	GPIO0	
2	GPIO1	
3	GPIO2	
4	GPIO3	
5	GPIO4	
6	GPIO5	
7	GPIO6	
8	GPIO7	
9	VCC_GPIO (5.0V input default)	
10	GND	

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3.17 Fan Interface

The module provides a system fan interface controlled by SEMA. The interface is located to the left of the COM3 header and consists of a Hirose DF13-4, 1.25 mm pitch 1*4 header.

Table 3-20: Fan Signal Definitions (CN27)

Pin	Signal	Connector
1	Speed (PWM out, 5V, 2k2 pull up included)	
2	Tacho (pull up 10k to3.3V included)	
3	GND	
4	+V5P0S (default) +V12P0ATX (on request)	

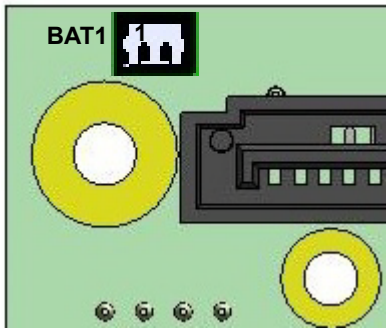
3.18 Battery Interface

The battery interface provides connection for an external battery to backup the RTC (real time clock). The interface is located next to the SATA1 connector and consists of an SMP, W125-0210-310-Z, 1.25 mm pitch 1*2 header.

NOTE:

The RTC has an expected current draw of 6µA at room temperature, with +3.0V. The battery is used only when power is not applied to the board.

Table 3-21: Battery Signal Definitions (BAT1)

Pin	Signal	Connector
1	V_BATT	
2	GND	

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4 Using the Module

This chapter defines the system management functions of the module including the SEMA system monitoring utility, BIOS control switch, temperature sensor function, and Real Time Clock.

4.1 SEMA Functions

The onboard micro controller provides SEMA (Smart Embedded Management Agent) functionality, which monitors and gathers hardware status and performance information from the system through the SMBus (System Management Bus). The following list highlights the SEMA functions available on the CMx-BTx.

- Total operating hours counter
  Counts the time the module has been run in minutes
- On-time minutes counter
  Counts the seconds since last system start
- Temperature monitoring of the board
  Stores minimum and maximum temperatures in the flash of the micro controller
- Automatic shut down on over temperature events
- Power monitor
  Reads the current drawn by the module and reports the nominal operating voltage
- Power cycles counter
- Boot counter
  Increases Boot count after a HW- or SW- Reset or after a successful power up
- Watchdog Timer
  Sets | Resets | Disables Watchdog Timer
- System restart cause
  Identifies Power loss | Watchdog event | External reset
- Flash area
  Provides 1 kByte Flash for customer data
- Protected Flash area
  Provides 128 Bytes Flash for Keys, IDs, etc. stored in a write- and clear-protectable region
- Board Identify
  Identifies Vendor | Board | Serial number

The SEMA tools are available for Windows, Linux, and VxWorks. SEMA functionality can also be used in applications. Refer to the SEMA software manual and technical manual on the ADLINK web site for more information.

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4.1.1 Board Specific SEMA Functions

Voltages

The BMC of the CMx-BTx implements a Voltage Monitor and samples several Onboard Voltages. The Voltages can be read out by calling the SEMA function <Get Voltages>. The function returns a 16-bit value divided in High-Byte (MSB) and Low-Byte (LSB).

The following table defines the voltages read out by the Voltage Monitor.

Table 4-1: BMC Readable Voltages

Channel#	Signal	Voltage Formula
0	+VCORE	(MSB<<8 + LSB) * 3.3 / 4096
1	+VNN (Graphics Core)	(MSB<<8 + LSB) * 3.3 / 4096
2	+VDDQ (Memory)	(MSB<<8 + LSB) * 3.3 / 4096
3	+V1P0A (Interfaces)	(MSB<<8 + LSB) * 3.3 / 4096
4	+V1P5S (HD Audio Interface)	(MSB<<8 + LSB) * 3.3 / 4096
5	+V3P3A	(MSB<<8 + LSB) * 1.100 * 3.3 / 4096
6	+V5P0_SBY	(MSB<<8 + LSB) * 1.2055 * 3.3 / 4096
7	+V5P0_ATX	(MSB<<8 + LSB) * 1.2055 * 3.3 / 4096
8	+V3P3_ATX	(MSB<<8 + LSB) * 1.100 * 3.3 / 4096
9	+V3P3_PCI	(MSB<<8 + LSB) * 1.100 * 3.3 / 4096
10	(MAINCURRENT)	Use Main Current Function

Main Current

The BMC of the CMx-BTx implements a Current Monitor, which allows the user to read the current by calling the SEMA function “Get Main Current”. The function returns four 16-bit values divided in Hi-Byte (MSB) and Lo-Byte (LSB). These four values represent the last four currents drawn by the board. The values are sampled every 250ms. The order of the four values is NOT in relationship to time. The access to the BMC may increase the drawn current of the whole system. In this case, you still have three samples without the influence of the read access.

Main Current = (MSB_n<<8 + LSB_n) * 2.014mA

TS# Events

TS# is activated by a temperature sensor when a device reaches its critical temperature and released when the device is back in its normal temperature range. This counter gives the user information about temperature or cooling issues. This counter is cleared when the system is removed from power. The CMx-BTx only monitors the board temperature.

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Exception Blink Codes

In the case of an error, the BMC shows a blink code on the blue STATUS LED (LED8). This error code is also reported by the BMC Flags register. The Exception Code is not stored in the Flash storage and is cleared when the power is removed. Therefore, the “Clear Exception Code” command is not supported.

Table 4-2: BMC Exception Blink Codes

Blink Code	Error Message	Description
2	NO_SUSCLK	No connection to Suspend Clock
3	NO_RSMRST	No Resume Well reset signal
4	NO_SLP_S4	No signal from CPU for S4 (suspend to disk) sleep control
5	NO_SLP_S3	No signal from CPU for S3 (suspend to RAM) sleep control
6	BIOS_FAIL	BIOS failure
7	RESET_FAIL	Reset failure
8	RESETIN_FAIL	Reset In failure
9	NO_ATX_PWRGD	No ATX Power Good signal
10	+VCC_S	No core voltage
11	+VNN_S	No GFX voltage
12	+VDDQ	No memory voltage
13	+V1P0A	No +V1P0A voltage
14	+V1P5S	No +V1P5S voltage
15	+V3P3A	No +V3P3A voltage
16	+5V_SBY	No stand-by voltage
17	+5V_ATX	No 5V main [AT/ATX] voltage
18	+V3P3_ATX	No 3.3V main [ATX] voltage
19	+V3P3_PCI	No +V3P3_PCI voltage
20	NO SYSTEM_S_PG	One or more S-voltages missing
21	NO_CORE_PWROK	Core power status failure
22	POWER_FAIL	Power failure
23	CRITICAL_TEMP	Critical temperature violation
24	PMIC_SDWN_FAIL	Power Management IC shutdown failure

BMC Flags

The BMC Flags Register returns the last detected exception code since power up.

4.1.2 Watchdog Timer

The BMC Watchdog activation is caused by under voltage protection. The Watchdog LED gets flashed after restart but only if the power supply reaches 4.2V.

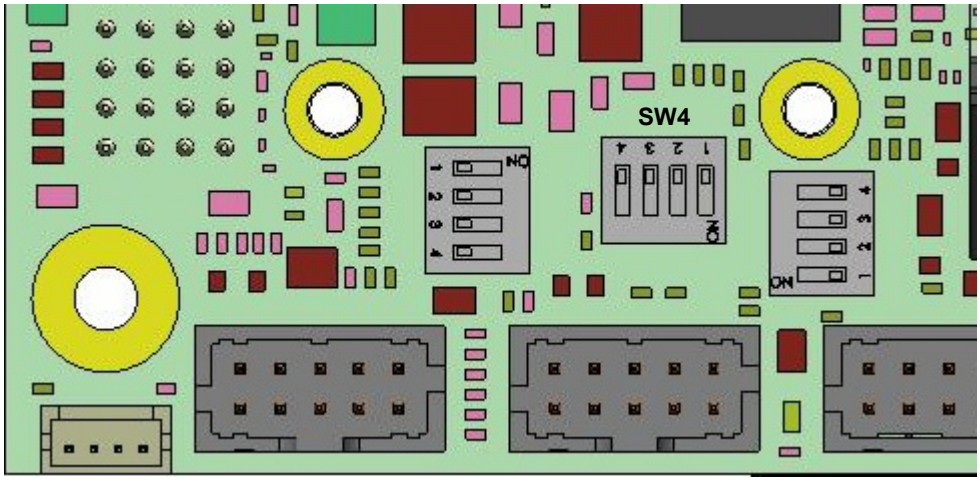
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4.2 SW4 BIOS Control Switch

Use the following table to configure the SW4 switch for controlling BIOS User Settings, Dual BIOS feature, Watchdog Timer activation, and LVDS 18/24-bit test mode. The default settings are indicated by the gray-shaded table cells under the “Position” columns.

Table 4-3: SW4 BIOS Control Signal Definitions

Position	Position	Signal(s)	Function
1	8	N/A	Not Used
2	7	CPU_BIOS_DEFAULT (position 2) GROUND (position 7)	Pos. 2: Retains User BIOS settings Pos. 7: Resets User BIOS settings
3	6	SEL_BIOS_SW (position 3) SEL_BIOS (position 6)	Pos. 3: Activates BIOS 1 Pos. 6: Activates BIOS 0
4	5	POSTWDT_DIS#_SW (position 4) POSTWDT_DIS# (position 5)	Pos. 4: Enables Watchdog Timer Pos. 5: Disables Watchdog Timer
DIP-Switches			



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4.3 Temperature Sensors

The CMx-BTx uses two different temperature sensors. The first is provided by the SoC, and the second is an LM73 which is connected to the BMC.

While the first one can only signal a catastrophic thermal situation within the SoC and cause a transition to S5, the second can be accessed through SEMA.

4.4 Real Time Clock (RTC)

The CMx-BTx contains a Real Time (time of day) Clock (RTC), which can be backed up with an external Lithium Battery. The CMx-BTx will function without a battery in those environments which prohibit batteries. The CMx-BTx will also continue to operate after the battery life has been exceeded. Under these conditions all setup information is restored from the on-board flash memory during POST along with the default date and time information.



To connect an external RTC battery, use the system panel, open-end cable wires connected to pin 5 and pin 8 on connector CN20.



Some operating systems require a valid default date and time to function.

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5 BIOS Setup

5.1 Menu Structure

This section presents the five primary menus of the BIOS Setup Utility. Use the following table as a quick reference for the contents of the BIOS Setup Utility. The subsections in this section describe the submenus and setting options for each menu item. The default setting options are presented in **bold**, and the function of each setting is described in the right hand column of the respective table.

Table 5-1: BIOS Setup Menu Overview

Main	Advanced	Boot	Security	Save & Exit
• BIOS Information • CPU Information • Memory Information • VGA Information • TXE Information • System Management ► • System Date • System Time	• CPU Configuration► • Graphics Configuration► • SATA Configuration► • USB Configuration► • SDIO Configuration► • Network Configuration► • Audio Configuration► • SPCI/PCIe Configuration► • Baytrail Features Configuration► • ACPI Settings► • Serial Port ► Console Redirection • Thermal Configuration► • Security Configuration► • Miscellaneous► • NCT5104D Super IO Configuration► • Ethernet Controls► • Mini-PCIe-slot function► • USB Controls►	• BootConfiguration► • CSM Parameters►	• Adminstrator Password • User Password	• Reset Options • Save Options

Notes:
► indicates a submenu
Gray text indicates info only

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5.2 Starting the BIOS Setup Utility

Use the following bullets to initiate start-up activity for the BIOS Setup Utility.

- Press <DEL> during power up to start the BIOS setup utility.
- Press <F11> during power up to start the Boot menu.
- Press <END> during power up to return BIOS settings to default.

5.3 Main Menu

The Main Menu provides read-only information about your system and also allows you to set the System Date and Time. Refer to the tables below for details of the submenus and settings.

5.3.1 Main > BIOS Information

Table 5-2: Main Menu > BIOS Information

Feature	Options	Description
BIOS Vender	Info only	BIOS source vendor
Core Version	Info Only	BIOS Core version
Compliancy	Info only	UEFI version
Project Version	Info only	ADLINK BIOS version
Build Date and Time	Info only	Date the BIOS was built

5.3.2 Main > CPU Information

Table 5-3: Main Menu > CPU Information

Feature	Options	Description
Microcode Patch	Info only	Display Microcode patch
BayTrail SoC	Info only	Display CPU steeping

5.3.3 Main > Memory Information

Table 5-4: Main Menu > Memory Information

Feature	Options	Description
Total Memory	Info only	Display total memory sizes

5.3.4 Main > VGA Information

Table 5-5: Main Menu > VGA Information

Feature	Options	Description
Intel (R) GOP Driver	Info only	Display Graphics FW version

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5.3.5 Main > TXE Information

Table 5-6: Main Menu > TXE Information

Feature	Options	Description
Sec RC Version	Info only	Display version of Sec RC
TXE FW Version	Info only	Display version of TXE

5.3.6 Main > System Management

Table 5-7: Main Menu > System Management

Board Information	Info only	
SMC Firmware	Read only	Display SMC firmware
Build Date	Read only	Display SMC firmware build date
SMC Boot loader	Read only	Display SMC boot loader
Build Date	Read only	Display SMC boot loader build date
Hardware Version	Read only	Display SMC hardware version
PCBA Revision	Read only	Display PCBA revision
Serial Number	Read only	Display SMC serial number
Manufacturing Date	Read only	Display SMC manufacturing date
Last Repair Date	Read only	Display SMC last repair date
MAC ID	Read only	Display SMC MAC ID
SEMA Features:	Read only	Display SEMA features

5.3.7 Main > System Management > Temperatures and Fan Speed

Table 5-8: Main Menu > System Management > Temperatures and Fan Speed

Feature	Options	Description
Temperatures and Fan	Info only	
• Board Temperatures	Info only	
• Current	Read only	Display current board temperature
• Startup	Read only	Display board startup temperature
• Min	Read only	Display board min. temperature
• Max	Read only	Display board max. temperature
• CPU Fan Speed	Read only	Display CPU fan speed
• System Fan Speed	Read only	Display system fan speed

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5.3.8 Main > System Management > Power Consumption

Table 5-9: Main Menu > System Management > Power Consumption

Feature	Options	Description
Power Consumption	Info only	
• Current Input Current	Read only	Display input current
• Current Input Power	Read only	Display input power
• GPU-Vcore	Read only	Display actual GPU-Vcore voltage
• GFX-Vcore	Read only	Display actual GFX-Vcore voltage
• V1.05	Read only	Display actual V1.05 voltage
• V1.35	Read only	Display actual V1.35 voltage
• V1.00	Read only	Display actual V1.00 voltage
• V3.30	Read only	Display actual V3.30 voltage
VIN	Read only	Display actual VIN voltage
• AIN7	Read only	Display actual AIN7 voltage

5.3.9 Main > System Management > Runtime Statistics

Table 5-10: Main Menu > System Management > Runtime Statistics

Feature	Options	Description
Runtime Statistics	Info only	
• Total Runtime	Read only	The returned value specifies the total time in minutes the system is running in S0 state.
• Current Runtime	Read only	The returned value specifies the time in seconds the system is running in S0 state. This counter is cleared when the system is removed from the external power supply.
• Power Cycles	Read only	The returned value specifies the number of times the external power supply has been shut down
• Boot Cycles	Read only	The Bootcounter is increased after a HW- or SW-Reset or after a successful power-up.
• Boot Reason	Read only	The boot reason is the event which causes the reboot of the system.

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5.3.10 Main > System Management > Flags

Table 5-11: Main Menu > System Management > Flags

Feature	Options	Description
Flags	Info only	
• BMC Flags	Read only	
• BIOS Select	Read only	Display the selection of current BIOS ROM
• ATX/AT-Mode	Read only	Display ATX/AT-Mode
• Exception Code	Read only	System exception reason

5.3.11 Main > System Management > Power Up

Table 5-12: Main Menu > System Management > Power Up

Feature	Options	Description
Power Up	Info only	
Power Up watchdog Attention: F12 disables the Power Up Watchdog.	• Enabled • **Disabled**	The Power-Up Watchdog resets the system after a certain amount of time after power-up.
ECO Mode	• **Disabled** • Enabled	Reduces the power consumption of the system
Power-up Mode Attention: The Power-Up Mode only has effect, if the module is in ATX-Mode.	• **Turn on** • Remain off • Last State	Turn On: The machine starts automatically when the power supply is turned on. Remain Off: To start the machine the power button has to be pressed. Last State: When powered on during a power failure the system will automatically power on when power is restored.



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With ECO Mode set to Enabled, the external RTC battery must be connected, or the system will not power on normally.

Avec le Mode ECO réglé sur Activé, la batterie RTC externe doit être connectée, sinon le système ne s'allumera pas normalement.

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5.3.12 Main > System Management > LVDS Backlight

Table 5-13: Main Menu > System Management > LVDS Backlight

Feature	Options	Description
LVDS Backlight	Info only	
LVDS Backlight Bright	255	The value range starts at 0 and ends at 255.

5.3.13 Main > System Management > Smart Fan

Table 5-14: Main Menu > System Management > Smart Fan

Feature	Options	Description
Smart Fan	Info only	
CPU Smart Fan Temperature Source	• **CPU Sensor** • System Sensor	Select CPU smart fan source
CPU Fan Mode	• **AUTO (Smart Fan)** • Fan Off • Fan On	Select CPU fan mode
CPU Trigger Point 1	Read only	
• Trigger Temperature	15	Specifies the temperature threshold at which the BMC turns on the CPU fan with the specified PWM level
• PWM Level	30	Select PWM level
CPU Trigger Point 2	Read only	
• Trigger Temperature	60	Specifies the temperature threshold at which the BMC turns on CPU fan the specified PWM level
• PWM Level	40	Select PWM level
CPU Trigger Point 3	Read only	
• Trigger Temperature	70	Specifies the temperature threshold at which the BMC turns on CPU fan the specified PWM level
• PWM Level	63	Select PWM level
CPU Trigger Point 4	Read only	
• Trigger Temperature	80	Specifies the temperature threshold at which the BMC turns on CPU fan the specified PWM level
• PWM Level	100	Select PWM level

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5.3.14 Main > System Date and Time

Table 5-15: Main Menu > System Date and Time

Feature	Options	Description
System Date	Day of Week, MM/DD/YYYY	Requires the alpha-numeric entry of the day of the week, day of the month, calendar month, and all 4 digits of the year, indicating the century and year (Fri XX/XX/20XX)
System Time	HH/MM/SS	Presented as a 24-hour clock setting in hours, minutes, and seconds

5.4 Advanced Menu

This menu contains the settings for most of the user interfaces in the system.

5.4.1 Advanced > CPU Configuration

Table 5-16: Advanced Menu > CPU Configuration

Feature	Options	Description
CPU Configuration	Info only	
Socket 0 CPU Information ►	Submenu	Socket specific CPU Information
• CPU Brand Name	Info only	Display CPU brand name
• CPU Signature	Info only	Display CPU signature
• Microcode Patch	Info only	Display microcode patch
• Max CPU speed	Info only	Display max. CPU speed
• Min CPU speed	Info only	Display min. CPU speed
• Processor Cores	Info only	Display number of processor cores
• Intel HT Technology	Info only	Display Intel HT Technology support
• Intel VT-x Technology	Info only	Display Intel VT-x Technology support
• L1 Data Cache	Info only	Display cache info
• L1 Code Cache	Info only	Display cache info
• L2 Cache	Info only	Display cache info
• L3 Cache	Info only	Display cache info
CPU Thermal Configuration ►	Submenu	CPU Thermal Configuration options
• DTS	• **Enabled** • Disabled	Enabled/Disabled Digital Thermal Sensor
PPM Configuration ►	Submenu	PPM Configuration Parameters
• CPU C state Report	• **Enabled** • Disabled	Enable/Disable CPU C state report to OS
• Max CPU C-State	• **C6** • C1	This option controls Max C state that the processor will support
• S0ix	• **Disabled** • Enabled	Enable/Disable CPU S0ix state
CPU Speed	Info only	Display Current CPU speed

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Table 5-16: Advanced Menu > CPU Configuration (Continued)

Feature	Options	Description
64-bit	Info only	Display 64-bit support
Limit CPUID Maximum	• **Disabled** • Enabled	Disabled for Windows XP
Execute Disabled Bit	• Disabled • **Enabled**	XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, Red Hat Enterprise 3 Update 3.)
Intel Virtualization Technology	• Disabled • **Enabled**	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.
Power Technology	• Disable • **Energy Efficient** • Custom	Enable the power management features

5.4.2 Advanced > Graphics Configuration

Table 5-17: Advanced Menu > Graphics Configuration

Feature	Options	Description
Graphics	Info only	
IGFX VBIOS Version	Info only	
Intel IGD Configuration ►	Submenu	Config Intel IGD Settings
GOP – LCD Control ►	Submenu	GOP LCD Control Settings
Graphics Power Management Control►	Submenu	Graphics Power Management Control Options
AMI Graphic Output Protocol Policy►	Submenu	User select monitor output by Graphic output protocol

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5.4.3 Advanced > SATA Configuration

Table 5-18: Advanced Menu > SATA Configuration

Feature	Options	Description
IDE Configuration	Info only	
Serial-ATA (SATA)	• **Enabled** • Disabled	Enable/Disable Serial ATA.
SATA Test Mode	• Enabled • **Disabled**	Test Mode enable/disable
SATA Controller Speed	• Gen1 • **Gen2**	SATA speed support Gen1 or Gen2.
SATA ODD Port	• Port0 ODD • No ODD	SATA ODD is Port 0 or Port1
SATA Mode	• IDE Mode • **AHCI Mode**	Select IDE/AHCI
Serial-ATA Port 0	• **Enabled** • Disabled	Enable / Disable Serial ATA Port 0
SATA Port0 HotPlug	• Enabled • **Disabled**	Enable /Disable SATA Port0 Hotplug
Serial-ATA Port 1	• **Enabled** • Disabled	Enable / Disable Serial ATA Port 1
SATA Port1 HotPlug	• Enabled • **Disabled**	Enable /Disable SATA Port1 Hotplug
SATA Port0	Info only	Display SATA present
SATA Port1	Info only	Display SATA present

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5.4.4 Advanced > USB Configuration

Table 5-19: Advanced Menu > USB Configuration

Feature	Options	Description
USB	Info only	
USB Module Version	Info only	
USB Devices	Info only	Drives, keyboards, mouse, hubs
Legacy USB Support	• **Enabled** • Disabled • Auto	Enables legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications and setup.
XHCI Hand-off	• **Enabled** • Disabled	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by the XHCI OS driver.
EHCI Hand-off	• Enabled • **Disabled**	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by the EHCI OS driver.
USB Mass Storage Driver Support	• **Enabled** • Disabled	Enable/Disable USB mass storage driver support.
Port 60/64 Emulation	• Disabled • **Enabled**	Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.
USB hardware delays and time-outs:	Info only	
USB transfer time-out	• 1 sec • 5 sec • 10 sec • **20 sec**	The time-out value for control, bulk, and interrupt transfers
Device reset time-out	• 10 sec • **20 sec** • 30 sec • 40 sec	USB mass storage device Start Unit command time-out.
Device power-up delay	• **Auto** • Manual	Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.
USB Configuration	Info only	
USB Configuration ►	Submenu	USB configuration settings

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5.4.5 Advanced > SDIO Configuration

Table 5-20: Advanced Menu > SDIO Configuration

Feature	Options	Description
SDIO Configuration	Info only	
SDIO Access Mode	• **Auto** • DMA • PIO	Auto Option: Access SD device in DMA mode if controller supports it, otherwise in PIO mode. DMA option: Access SD device in DMA mode.PIO option: Access SD device in PIO mode.

5.4.6 Advanced > Network Configuration

Table 5-21: Advanced Menu > Network Configuration

Feature	Options	Description
Network	Info only	
Network Stack	• Enabled • **Disabled**	Enable/Disable UEFI network stack.

5.4.7 Advanced > Audio Configuration

Table 5-22: Advanced Menu > Audio Configuration

Feature	Options	Description
Audio Configuration	Info only	
LPE Audio Support	• **Disabled** • LPE Audio PCI mode • LPE Audio ACPI ode	Select LPE Audio ACPI mode or PCI mode
Audio Controller	• Disabled • **Enabled**	Control Detection of the Azalia device. Disable = Azalia will be unconditionally disabled. Enabled = Azalia will be unconditionally enabled.
• Azalia VCi Enable	• Disabled • **Enabled**	Enable/Disable Virtual Channel 1 of Audio Controller
• Azalia Docking Support Enable	• **Disabled** • Enabled	Enable/Disable Azalia Docking Support of Audio Controller.
• Azalia PME Enable	• Disabled • **Enabled**	Enable/Disable Power Management capability of Audio Controller.
• Azalia HDMI Codec	• Disabled • **Enabled**	Enable/Disable internal HDMI codec for Azalia

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5.4.8 Advanced > PCI and PCIe Configuration

Table 5-23: Advanced Menu > PCI and PCIe Configuration

Feature	Options	Description
PCI / PCIe Configuration	Info only	
PCI Chipset Settings ►	Submenu	PCI Express Configuration settings
PCI Latency	• **32 PCI Bus Clocks** • 64 PCI Bus Clocks • 96 PCI Bus Clocks • 128 PCI Bus Clocks • 160 PCI Bus Clocks • 192 PCI Bus Clocks • 224 PCI Bus Clocks • 248 PCI Bus Clocks	Value to be programmed into PCI latency timer register.
VGA Palette Snoop	• **Disabled** • Enabled	Enables or Disables VGA palette registers snooping.
PERR# Generation	• Enabled • **Disabled**	Enable or Disable the PCI Express port 1 in the chipset.
SERR# Generation	• Enabled • **Disabled**	Enables or Disables PCI Device to generate SERR#.
PCI Express Settings	• Info only	
Relaxed Ordering	• **Disabled** • Enabled	Enables or Disables PCI Express device relaxed ordering.
Extended Tag	• **Disabled** • Enabled	If Enabled, allows device to use 8-bit tag field as a requester.
No Snoop	• Disabled • **Enabled**	Enables or Disables PCI Express device No Snoop option.
Maximum Payload	• **Auto** • 128 Bytes • 256 Bytes • 512 Bytes • 1024 Bytes • 2048 Bytes • 4096 Bytes	Set maximum payload of PCI Express device or allow system BIOS to select the value.
Maximum Read Request	• **Auto** • 128 Bytes • 256 Bytes • 512 Bytes • 1024 Bytes • 2048 Bytes • 4096 Bytes	Set maximum read request size of PCI Express device or allow system BIOS to select the value.
PCI Express Link Register Settings	• Info only	
ASPM Support WARNING: Enabling ASPM may cause some PCI-E devices to fail	• **Disabled** • Auto • Force L0s	Set the ASPM Level: Force L0s - Force all links to L0s Auto - BIOS auto configure Disabled - Disables ASPM

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Table 5-23: Advanced Menu > PCI and PCIe Configuration (Continued)

Feature	Options	Description
Extended Synch	• **Disabled** • Enabled	If enabled, allows generation of Extended Synchronization patterns.
Link Training Retry	• Disable • 2 • 3 • **5**	Defines number of retry attempts software will take to retrain the link if previous training attempt was unsuccessful.
Link Training Timeout (Us)	1000	Defines number of microseconds software will wait before polling 'Link Training' bit in Link Status register. Value range from 10 to 10000 uS.
Unpopulated Links	• **Keep Link ON** • Disabled	In order to save power, software will disable unpopulated PCI Express links if this option set to Disabled.
Restore PCIE Registers	• Enabled • **Disabled**	On non-PCI Express aware OSes (pre Windows Vista) some devices may not be correctly reinitialized after S3. Enabling this restores PCI Express device configurations on S3 resume. Warning: Enabling this may cause issues with other hardware after S3 resume.
PCIe Configuration	Info only	
PCIe Configuration ►	Submenu	

5.4.9 Advanced > PCI and PCIe > PCIe Configuration Settings

Table 5-24: Advanced Menu > PCI and PCIe > PCIe Configuration Settings

Feature	Options	Description
PCI Express Configuration		
PCI Express Port x	• **Enabled** • Disabled	Enable or disable the PCI Express port x in the chipset.
Hot Plug	• Disabled • **Enabled**	Enable or disable PCI Express hotplug.
Speed	• **Auto** • Gen 2 • Gen 1	Configure PCIe port speed.

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5.4.10 Advanced > PCI and PCIe > PCI Subsystem Settings

Table 5-25: Advanced Menu > PCI and PCIe > PCI Subsystem Settings

Feature	Options	Description
PCI Bus Driver Version	Info only	
PCI Devices Common Settings:		
PCI Latency	• **32 PCI Bus Clocks** • 64 PCI Bus Clocks • 96 PCI Bus Clocks • 128 PCI Bus Clocks • 160 PCI Bus Clocks • 192 PCI Bus Clocks • 224 PCI Bus Clocks • 248 PCI Bus Clocks	Value to be programmed into PCI latency timer register.
PCI-X Latency Timer	• 32 PCI Bus Clocks • **64 PCI Bus Clocks** • 96 PCI Bus Clocks • 128 PCI Bus Clocks • 160 PCI Bus Clocks • 192 PCI Bus Clocks • 224 PCI Bus Clocks • 248 PCI Bus Clocks	Value to be programmed into PCI latency timer register.
VGA Palette Snoop	• **Disabled** • Enabled	Enables or Disables VGA palette registers snooping.
PERR# Generation	• Enabled • **Disabled**	Enable or Disable the PCI Express port 1 in the chipset.
SERR# Generation	• Enabled • **Disabled**	Enables or Disables PCI Device to generate SERR#.
Above 4G Decoding	• **Disabled** • Enabled	Enables or Disables 64bit capable Devices to be Decoded in Above 4G Address Space.(Only if system supports 64bit PCI Decoding)
SR-IOV Support	• **Disabled** • Enabled	If system has SR-IOV capable PCIe Devices, this option Enables or Disables Single Root IO Virtualization Support.
PCI Express Settings ►	Submenu	Change PCI Express Devices Settings.
PCI Express GEN 2 Settings ►	Submenu	Change PCI Express GEN Devices Settings.

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5.4.11 Advanced > Baytrail Features Configuration

Table 5-26: Advanced Menu > Baytrail Features Configuration

Feature	Options	Description
LPSS & SCC Devices Mode	• **ACPI mode** • PCI mode	LPSS & SCC Devices Mode Settings
SCC Configuration	• Info only	
SCC SD Card Support	• **Enabled** • Disabled	SCC SD Card Support Enable/ Disable
SDR25 Support for SDCard	• **Enabled** • Disabled	Disable/Enable SDR25 Capability in SD Card controller
SDR50 Support for SDCard	• Enabled • **Disabled**	Disable/Enable SDR25 Capability in SD Card controller. (Gray item, if SDR25 Support disable, this item will enable.)
MIPI HIS Support	• Enabled • **Disabled**	MIPI HIS Support Enable/ Disable
LPSS Configuration	• Info only	
LPSS HSURT #1 Support	• **Enabled** • Disabled	LPSS HSUART #1 Support Enable/Disable

5.4.12 Advanced > ACPI Settings

Table 5-27: Advanced Menu > ACPI Settings

Feature	Options	Description
ACPI Settings	Info only	
Enable ACPI Auto Configuration	• **Disabled** • Enabled	Enables or Disables BIOS ACPI Auto Configuration
Enable Hibernation	• **Disabled** • Enabled	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This item may be not effective with some OSs.
ACPI Sleep State	• Suspend Disabled • **S3 (Suspend to RAM)**	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
Lock Legacy Resources	• **Disabled** • Enabled	Enables or Disables Lock of Legacy Resources.

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5.4.13 Advanced > Serial Port Console Redirection

Table 5-28: Advanced Menu > Serial Port Console Redirection

Feature	Options	Description
COM0	Info only	
Console Redirection	• **Disabled** • Enabled	Console Redirection Enable or Disable.
COM1	• Info only	
Console Redirection	• **Disabled** • Enabled	Console Redirection Enable or Disable.
COM2	• Info only	
Console Redirection	• **Disabled** • Enabled	Console Redirection Enable or Disable.
COM3	• Info only	
Console Redirection	• **Disabled** • Enabled	Console Redirection Enable or Disable.
Legacy Console Redirection	• Info only	
Legacy Console Redirection Settings►	• Submenu	Console Redirection Settings
Serial Port for Out-of-Band Management/Windows Emergency Management Services (EMS)	• Info Only	
Console Redirection	• **Disabled** • Enabled	Console Redirection Enable or Disable.
Console Redirection Settings ►	Submenu	This settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. (If EMS Console Redirection enable, this item will be lunched.)

5.4.14 Advanced > Thermal Configuration

Table 5-29: Advanced Menu > Thermal Configuration

Feature	Options	Description
Thermal Configuration Param	Info only	
Critical Trip Point	• **Disabled** • 95 C • 85 C	The value controls the temperature of the ACPI critical Trip Point in which the OS will shut the system off.
Passive Trip Point	• **Disabled** • 95 C • 85 C	The item controls the temperature of the ACPI critical Trip point – the point in which the OS will begin throtting the processor.

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5.4.15 Advanced > Security Configuration

Table 5-30: Advanced Menu > Security Configuration

Feature	Options	Description
Intel(R) TXE Configuration	Info only	
TXE	• **Enable** • Disable	Enable/Disable TXE
TXE HMRFPO	• Enable • **Disable**	Enable/Disable TXE HMRFPO
TXE Firmware Update	• **Enable** • Disable	Enable/Disable TXE Firmware Update
TXE EOP Message	• **Enable** • Disable	Send EOP Message Before Enter OS
TXE Unconfiguration Perform		Revert TXE settings to factory defaults
Intel(R) Anit-Theft Technology Configuration	Info only	
Intel(R) AT	• Enable • **Disable**	Enable/Disable BIOS AT code from Running
Intel(R) AT Platform PBA	• **Enable** • Disable	Enable/Disable BIOS AT code from Running
Intel AT Suspend Mode	• Enable • **Disable**	Gray item

5.4.16 Advanced > Miscellaneous

Table 5-31: Advanced Menu > Miscellaneous

Feature	Options	Description
Miscellaneous	Info only	
High Precision Timer	• **Enable** • Disable	Enable or Disable the High Precision Event Timer
Serial IRQ Mode	• **Quiet** • Continuous	Configure Serial IRQ Mode.
Global SMI Lock	• **Enable** • Disable	Enable or Disable SMI lock.
PCI Express Dynamic Clock Gating	• Enabled • **Disabled**	Enable/Disable PCIE Dynamic Clock Gating.
OS Selection	• Windows 8.X • **Windows 7**	OS Selection

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5.4.17 Advanced > NCT5104D Super IO Configuration

Table 5-32: Advanced Menu > NCT5104D Super IO Configuration

Feature	Options	Description
NCT5104D Super IO Configuration	Info only	
Super IO Chip	Info only	
Serial Port 0 Configuration ►	Submenu	
Serial Port 0 Configuration • Serial Port • Device Settings • Change Settings • Enable 921Kbps Yes/No	 • **Enabled** • Disabled • IO=3F8h; IRQ=4 • **Auto** • IO=3F8h; IRQ=4 • IO=3F8h; IRQ=4 • IO=2F8h; IRQ=4 • IO=3E8h; IRQ=4 • IO=2E8h; IRQ=4 • **No** • Yes	 Enable/Disable Serial Port 0 (COM0). Fixed configuration of serial port. Select an optimal setting for Super IO device.
Serial Port 1 Configuration ►	Submenu	
Serial Port 1 Configuration • Serial Port • Device Settings • Change Settings • Enable 921Kbps Yes/No	 • **Enabled** • Disabled • IO=2F8h; IRQ=3 • **Auto** • IO=2F8h; IRQ=3 • IO=3F8h; IRQ=3 • IO=3E8h; IRQ=3 IO=2E8h; IRQ=3 • **No** • Yes	 Enable/Disable Serial Port 1 (COM1). Fixed configuration of serial port. Select an optimal setting for Super IO device.
Serial Port 2 Configuration ►	Submenu	

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Table 5-32: Advanced Menu > NCT5104D Super IO Configuration (Continued)

Feature	Options	Description
Serial Port 2 Configuration		
• Serial Port	• **Enabled** Disabled	Enable/Disable Serial Port 2 (COM2).
• Device Settings	• IO=3E8h; IRQ=6	Fixed configuration of serial port.
• Change Settings	• **Auto** • IO=3E8h; IRQ=6 • IO=3F8h; IRQ=4 • IO=2E8h; IRQ=6 • IO=2F0h; IRQ=6 IO=2E0h; IRQ=6	Select an optimal setting for Super IO device.
• Enable 921Kbps Yes/No	• **No** • Yes	
Serial Port 3 Configuration ►	Submenu	
Serial Port 3 Configuration • Serial Port	• **Enabled** • Disabled	Enable/Disable Serial Port 3 (COM3).
• Device Settings	IO=2E8h; IRQ=11	Fixed configuration of serial port.
Change Settings	• **Auto** • IO=3E8h; IRQ=11 • IO=3E8h; IRQ=11 • IO=2F8h; IRQ=11 • IO=2F0h; IRQ=11 • IO=2E0h; IRQ=11	Select an optimal setting for Super IO device.
• Enable 921Kbps Yes/No	• **No** • Yes	
COM0 and COM1	Info only	
• Serial mode	• RS-232 • RS-422	The COM port is capable to drive RS-232 or RS-422. Please select the mode in which the COM port shall work.
• Serial mode	• RS-232 • RS-422	The COM port is capable to drive RS-232 or RS-422. Please select the mode in which the COM port shall work.
COM2	Info only	
• Serial mode	• RS-232 • RS-422	The COM port is capable to drive RS-232 or RS-422. Please select the mode in which the COM port shall work.
COM3	Info only	
• Serial mode	• RS-232 • RS-422	The COM port is capable to drive RS-232 or RS-422. Please select the mode in which the COM port shall work.

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5.4.18 Advanced > Ethernet Controls

Table 5-33: Advanced Menu > Ethernet Configuration

Feature	Options	Description
Ethernet Controls	Info only	
Ethernet Controller 0	• **Enabled** • Disabled	Ethernet Controller 0
Ethernet Controller 1	• **Enabled** • Disabled	Ethernet Controller 1

5.4.19 Advanced > Mini-PCIe-Slot function

Table 5-34: Advanced Menu > Mini-PCIe-Slot function

Feature	Options	Description
Mini-PCIe-Slot function	Info only	
Mini-PCIe-Slot function	• **Mini-PCI-Express** • Mini-SATA	The mini-PCIe-Slot supports either mini-PCI-Express or mini-SATA.
RADIO-1 activation	• **Enabled (Low)** • Disabled (High)	Decide whether RADIO-1 should be activated or not. Respectively, decide whether PIN 20 on the Mini-PCIe-Slot should be set to high or low.
RADIO-2 activation	• **Enabled (Low)** • Disabled (High)	Decide whether RADIO-2 should be activated or not. Respectively, decide whether PIN 51 on the Mini-PCIe-Slot should be set to high or low.

5.4.20 Advanced > USB Controls

Table 5-35: Advanced Menu > USB Controls

Feature	Options	Description
SUSB Controlls	Info only	
USB port 0 activation	• **Enabled** • Disabled	Decide whether USB port 0 should be activated or not.
USB port 1/2 activation	• **Enabled** • Disabled	Decide whether USB port 1/2 should be activated or not.

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5.5 Boot Menu

This menu contains the settings for system boot-up functions.

5.5.1 Boot > Boot Configuration

Table 5-36: Boot Menu > Boot Configuration

Feature	Options	Description
Boot Configuration	Info only	
Setup Prompt Timeout	• **1**	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
Bootup NumLock State	• **On** • Off	Select the keyboard NumLock state.
Quiet Boot	• **Disabled** • Enabled	Enable or disables Quiet Boot option.
Fast Boot	• **Disabled** • Enabled	Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect on BBS boot options.
CSM Configuration ►	Submenu	CSM configuration: Enable/Disable, Option ROM execution settings, etc.
Boot Option Priorities	Info only	
Delete Boot Option ►	Submenu	Remove an EFI boot option from the boot order

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5.5.2 Boot > Boot Configuration > CSM Configuration

Table 5-37: Boot Menu > Boot Configuration > CSM Configuration

Feature	Options	Description
Compatibility Support Module Configuration	Info only	
CSM Support	• **Enabled** • Disable	Enable/Disable CSM Support.
CSM16 Module Version	Info only	
GataA20 Active	• **Upon Request** • Always	Upon Request – GA20 can be disabled using BIOS services. Always – do not allow disabling of GA20; this option is useful when any RT code is executed above 1MB.
Option ROM Messages	• **Force BIOS** • Keep Current	Set display mode for Option ROM.
Boot option filter	• **UEFI and Legacy** • Legacy only • UEFI only	This option controls legacy/UEFI ROM priority.
Option ROM execution	Info only	
Network	• Do not launch • **UEFI only** • Legacy only	Controls the execution of UEFI and legacy PXE OpROM.
Storage	• Do not launch • **UEFI only** • Legacy only	Controls the execution of UEFI and legacy storage OpROM.
Video	• Do not launch • UEFI only • **Legacy only**	Controls the execution of UEFI and legacy video OpROM.
Other PCI devices	• **UEFI only** • Legacy only	Determines OpROM execution policy for devices other than network, storage or video.

5.6 Security Menu

Table 5-38: Security Menu

Feature	Options	Description
Administrator Password	Enter password	
User Password	Enter password	

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5.7 Save & Exit Menu

Table 5-39: Save & Exit Menu

Feature	Options	Description
Save Changes and Exit	Yes No	Exit system setup after saving the changes.
Discard Changes and Exit	Yes No	Exit system setup without saving any changes.
Save Changes and Reset	Yes No	Reset the system after saving the changes.
Discard Changes and Reset	Yes No	Reset system setup without saving any changes.
Save Options	Info only	
Save Changes	Yes No	Save Changes done so far to any of the setup options.
Discard Changes	Yes No	Discard Changes done so far to any of the setup options.
Restore Defaults	Yes No	Restore/Load Default values for all the setup options.
Save as User Defaults	Yes No	Save the changes done so far as User Defaults.
Restore User Defaults	Yes No	Restore the User Defaults to all the setup options.

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6 System Resources

This chapter provides system resource specifications for the CMx-BTx including Memory Address Map, IO Address Map, PCI Configuration Registers, IO Register Maps, and System Interrupt Map.

6.1 Memory Address Map

There are 64 GB (36-bits) of physical address space that can be used as:

- Memory Mapped IO (MMIO - IO fabric)
- Physical Memory (DRAM)

The CPU core can access the full physical address space, while downstream devices can only access SoC DRAM, and each CPU core's local APIC. Peer to peer transactions are not supported.

Most devices map their registers and memory to physical address space. This chapter summarizes the possible mappings.

The SoC supports four different address spaces:

- Physical Address Space
- IO Address Space
- PCI Configuration Space
- Message Bus Space

The SoC Transaction Router maps the physical address space as follows:

- CPU core to DRAM
- CPU core to IO fabric (MMIO)
- CPU core to extended PCI registers (ECAM accesses)
- IO fabric to CPU cores (local APIC interrupts)

The CPU core can only directly access memory space through memory reads and writes and IO space through the IN and OUT IO port instructions. PCI configuration space is indirectly accessed through IO or memory space, and the Message Bus space is accessed through PCI configuration space.

Although 64 GB (36-bits) of physical address space is accessible, some MMIO must exist for devices and software with 32-bit limits. Further, all DRAM should remain accessible for devices and software with access to memory above 4 GB. These goals are accomplished by moving a section DRAM to start at the fixed 4 GB boundary, leaving a hole below 4 GB for MMIO. This creates the following distinct memory regions:

- DOS DRAM + Low DRAM
- Low MMIO
- High DRAM
- High MMIO

There are two registers used to create these regions, BMBOUND and BMBOUND_HI.

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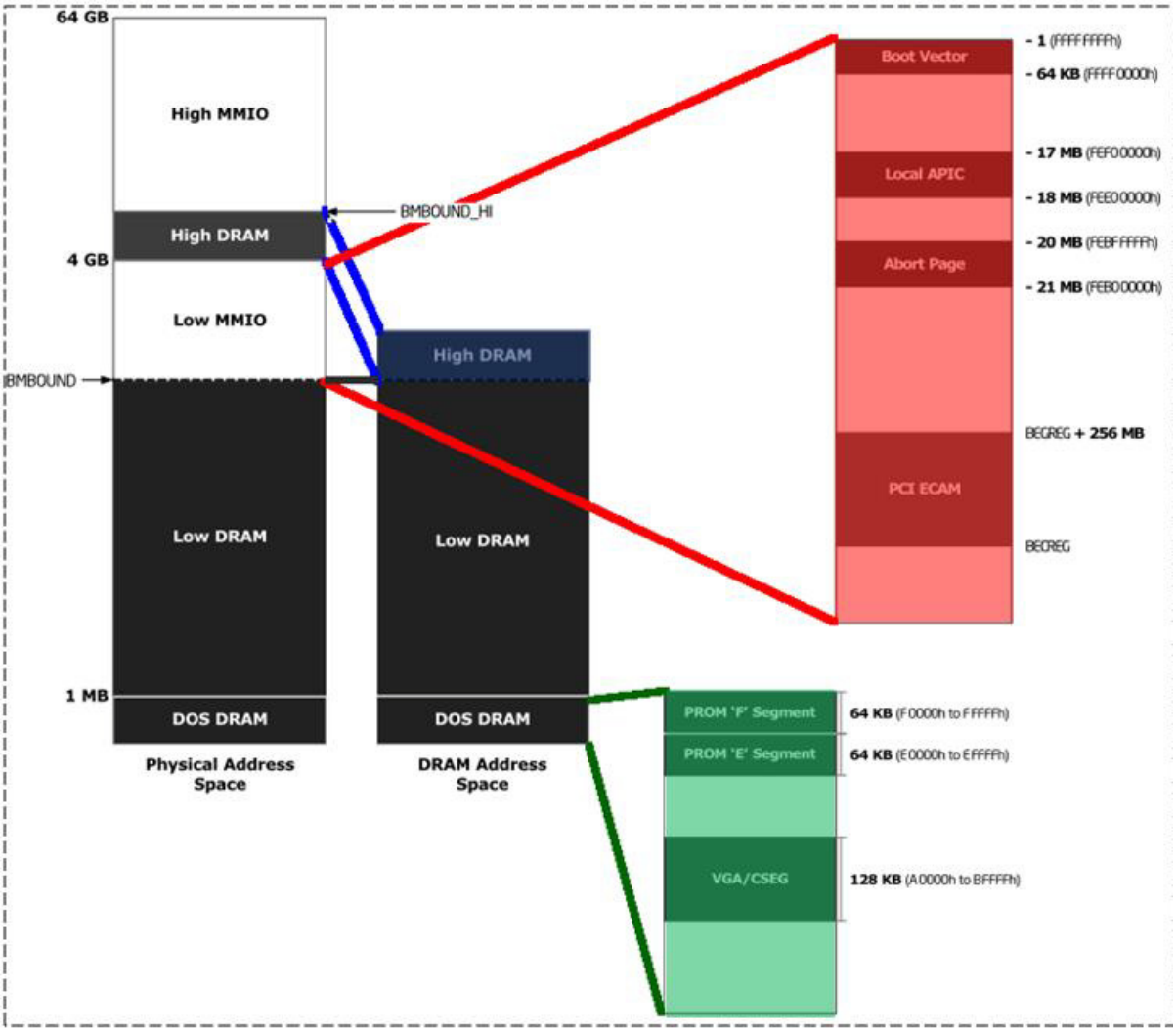


Table 6-1: Memory Address Map

Address Range	Size	Comment
BMBOUND_HI – FFFFFFFFFh	64 GB - BMBOUND_HI	High MMIO
100000000 – BMBOUND_HI	BMBOUND_HI - 4 GB	High DRAM
FFFF:0000h – FFFF:FFFFh	64 KB -1	Boot Vector
FEE0:0000h – FEF0:0000h	1 MB	Local APIC
FEB0:0000h – FEBF:FFFFh	1 MB	Abort Page
BEGREG – BEGREG + 256 MB	256 MB	PCI ECAM
BMBOUND – FFFF:FFFFh	4 GB - BMBOUND	Low MMIO
100000h – BMBOUND	up to 4 GB - (DOS DRAM + Low MMIO)	Low DRAM
F0000h – 000F:FFFFh	64 KB	PROM “F” Segment
E0000h – 000E:FFFFh	64 KB	PROM “E” Segment
A0000h – 000B:FFFFh	128 KB	VGA/CSEG
0h – 0009:FFFFh	640 KB	DOS Area

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Memory accesses targeting MMIO are routed by the IO fabric to programmed PCI ranges, or routed to the PCU by default (subtractive agent). Programmed PCI ranges can be moved within low or high MMIO, and most can be disabled.



Not all devices can be mapped to high MMIO.

Fixed MMIO is claimed by the Platform Controller Unit (PCU). The default regions are listed below. Movable ranges are not shown.

Table 6-2: Fixed Memory Ranges in the CPU

Device	IO Address	Comment
Low BIOS (Flash Boot)	000E0000h – 000FFFFFh	Starts 128 KB below 1 MB; Firmware/BIOS
IO APIC	FEC00000h – FEC00040h	Starts 20 MB below 4 GB
HPET	FED00000h – FED003FFh	Starts 19 MB below 4 GB
TPM (LPC)	FFD40000h – FFD40FFFh	Starts 16 KB above HPET range
High BIOS/Boot Vector	FFFF0000h FFFFFFFFFh	Starts 64 KB below 4 GB; Firmware/BIOS

The following PCI devices may claim memory resources in MMIO space:

- Graphics/Display (High MMIO capable)
- PCI Express (High MMIO capable)
- SATA
- SD/MMC/SDIO
- SIO
- HD Audio
- Platform Controller Unit (PCU) (Multiple BARs)
- xHCI USB
- EHCI USB
- USB Device
- LPE/I2S
- ISP/MIPI-CSI

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The following devices are **not** supported with the CMx-BTx modules:

- LPE/I2S
- ISP/MIPI-CSI
- TPM

CAUTION:
MISE EN GARDE

Variable memory ranges should not be set to conflict with other memory ranges. There will be unpredictable results if the configuration software allows conflicts to occur. Hardware does not check for conflicts.

Les plages de mémoire variable ne doivent pas être définies pour entrer en conflit avec d'autres plages de mémoire. Il y aura des résultats imprévisibles si le logiciel de configuration permet à des conflits de se produire. Le matériel ne recherche pas les conflits.

6.2 I/O Address Map

There are 64 KB + 3 bytes of IO space (0h-10002h) for accessing IO registers. Most IO registers exist for legacy functions in the PCU or for PCI devices, while some are claimed by the SoC Transaction Router for graphics and for the PCI configuration space access registers.

Table 6-3: Fixed IO Ranges in the CPU

Device	IO Address	Comment
8259 Master	20h-21h, 24h-25h, 28h-29h, 2Ch-2Dh, 30h-31h, 34h-35h, 38h-39-, 3Ch-3Dh	
8254s	40h-43h, 50h-53h	
PS Control	60h, 64h	
NMI Controller	61h, 63h, 65h, 67h	
RTC	70h-77h	
Port 80h	80h-83h	
Init Register	92h	
8259 Slave	A0h-A1h, A4h-A5h, A8h-A9h, ACh-ADh, B0h-B1h, B4h-B5h, B8h-B9h, BCh-BDh, 4D0h-4D1h	
PCU UART	3F8h-3FFh	used by the LPC-UART
Reset Control	CF9h	Overlaps PCI IO registers
Active Power Management	B2h-B3h	

The following table shows the variable IO decode ranges. They are set using base address registers (BARs) or other similar means. Plug-and-play (PnP) software (PCI/ACPI) can use their configuration mechanisms to set and adjust these values.

Table 6-4: Variable IO Address Ranges Decoded by PCI Devices in the IO Fabric

Device	Size / Bytes	Comment
ACPI Power Management (PCU)	128	ACPI_BASE_ADDR (PM1BLK): PCI[B:0,D:31,F:0] + 40h
GPIO (PCU)	256	GBA: PCI[B:0,D:31,F:0] + 48h

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Table 6-4: Variable IO Address Ranges Decoded by PCI Devices in the IO Fabric

RCBA (PCU)	1024	RCRB_BA: PCI[B:0,D:31,F:0] + F0h

CAUTION:

MISE EN GARDE

Variable IO ranges should not be set to conflict with other IO ranges. There will be unpredictable results if the configuration software allows conflicts to occur. Hardware does not check for conflicts.

Les plages d'E/S variables ne doivent pas être définies pour entrer en conflit avec d'autres plages d'E / S. Il y aura des résultats imprévisibles si le logiciel de configuration permet à des conflits de se produire. Le matériel ne recherche pas les conflits.

6.3 PCI Configuration Registers

The devices and functions can be accessed by the PCI Configuration Registers.

Table 6-5: PCI Configuration Registers

Address Range (hex)	Description
0CFB – 0CF8	PCI Configuration Address Register
0CFF – 0CFC	PCI Configuration Data Register

Table 6-6: PCI CONFIG_ADDRESS Register Mapping (IO Port CF8h)

Field	CONFIG_ADDRESS Bits
Enable PCI Configuration Space Mapping	31
Reserved	30:24
Bus Number	23:16
Device Number	15:11
Function Number	10:08
Register / Offset Number	07:02

NOTE:

Bit 31 of CONFIG_ADDRESS must be set for a configuration cycle to be generated.

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Table 6-7: PCI Devices and Functions

Bus#	Device#	Function#	Device ID	Description	Function
0	0	0	0F00h	SoC Transaction Router	
0	2	0	0F31h	Graphics & Display	
0	3	0	0F38h	Camera Image Signal Processor	
0	16	0	0F14h	Storage Control Cluster (SCC)	MMC
0	17	0	0F15h		SDIO
0	18	0	0F16h		SD Port
0	19	0	0F20h (IDE) 0F21h (IDE) 0F22h (AHCI) 0F23h (AHCI)	SATA	
0	20	0	0F35h	xHCI USB	
0	21	0	0F28h	Low Power Engine Audio	
0	22	0	0F37h	USB Device	
0	24	0	0F40h	Serial IO (SIO)	DMA
		1	0F41h		I²C Port 1
		2	0F42h		I²C Port 2
		3	0F43h		I²C Port 3
		4	0F44h		I²C Port 4
		5	0F45h		I²C Port 5
		6	0F46h		I²C Port 6
		7	0F47h		I²C Port 7
0	26	0	0F18h	Trusted Execution Engine	
0	27	0	0F40h	HD Audio	
0	28	0	0F48h	PCI Express	Root Port 1 (ETH1)
0		1	0F4Ah	PCI Express	Root Port 2 (ETH2)
0		2	0F4Ch	PCI Express	Root Port 3 (PCIe2PCI)
0		3	0F4Eh	PCI Express	Root Port 4 (mini-PCIe socket)
0	29	0	0F34h	EHCI USB	
0	30	0	0F06h	Serial IO (SIO)	DMA
0		1	0F08h		PWM Port 1
0		2	0F09h		PWM Port 2
0		3	0F0Ah		HSUART Port 1
0		4	0F0Ch		HSUART Port 2
0		5	0F0Eh		SPI Port
0	31	0	0F1Ch	Platform Controller Unit	LPC: Bridge to Intel Legacy Block (LPC to ISA, LPC to UART)

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6.4 IO Register Maps

6.4.1 CMOS Memory and RTC Registers

The RTC internal registers and RAM are organized as two banks of 128 bytes each, called the standard and extended banks.

The first 14 bytes of the standard bank contain the RTC time and date information along with four registers, A - D, that are used for configuration of the RTC. The extended bank contains a full 128 bytes of battery backed SRAM. All data movement between the host CPU and the RTC is done through register mapped standard I/O space.



It is not possible to disable the extended bank.



Registers reg_RTC_IR_type and reg_RTC_TR_type are used for data movement to and from the standard bank. Registers reg_RTC_RIR_type and reg_RTC_RTR_type are used for data movement to and from the extended bank. All of these registers have alias I/O locations, as indicated below.

Table 6-8: RTC IO Registers Alias Locations

Register	Original IO location	Alias IO location
reg_RTC_IR_type	70h	74h
reg_RTC_TR_type	71h	75h
reg_RTC_RIR_type	72h	76h
reg_RTC_RTR_type	73h	77h

Table 6-9: RTC Indexed Registers

Start	End	Name
00h	00h	Seconds
01h	01h	Seconds Alarm
02h	02h	Minutes
03h	03h	Minutes Alarm
04h	04h	Hours
05h	05h	Hours Alarm
06h	06h	Day of Week
07h	07h	Day of Month
08h	08h	Month
09h	09h	Year
0Ah	0Ah	Register A
0Bh	0Bh	Register B
0Ch	0Ch	Register C
0Dh	0Dh	Register D
0Eh	7Fh	114 Bytes of User RAM

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6.5 Interrupts

6.5.1 SERIRQ Interrupt Mapping

Below the SERIRQ Interrupt Mapping is shown:

Table 6-10: SERRIRQ Interrupt Mapping

Data Frame#	Interrupt	Clocks Past Start Frame	Comment
1	IRQ0	2	Ignored. Can only be generated via the internal 8524
2	IRQ1	5	Before port 60h latch
3	SMI#	8	Causes SMI# if low. Sets SMI_STS.ILB_SMI_STS register bit
4	IRQ3	11	Default: COM0
5	IRQ4	14	Default: COM1
6	IRQ5	17	
7	IRQ6	20	Default: COM2
8	IRQ7	23	
9	IRQ8	26	Ignored. IRQ8# can only be generated internally
10	IRQ9	29	
11	IRQ10	32	
12	IRQ11	35	
13	IRQ12	38	Before port 60h latch / Default: COM3
14	IRQ13	41	Ignored
15	IRQ14	44	Ignored
16	IRQ15	47	
17	IOCHCK#	50	Same as ISA IOCHCK# going active
18	PCI INTA#	53	
19	PCI INTB#	56	
20	PCI INTC#	59	
21	PCI INTD#	62	



The IRQ16 up to IRQ23 (APIC) are not supported by serial IRQs.

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