DAQ/DAQe/PXI-2204/2205/2206/2208

64-/96-ch High Performance
Multi-Function Data Acquisition Card
User's Manual

Manual Rev. 1.0

Revision Date: Dec. 28, 2023

Part No: 50M-12258-1000

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Revision History

Revision	Release Date	Description of Change(s)
2.01	2007-12-04	Previous release PN: 50-11220-2010
1.0	2023-12-28	▶ Initial release under new part number. ▶ Added 1.4 Software Support. ▶ Added 2.4 Switch and Jumper Settings. ▶ Added Board ID Configuration note and figure to 2.4.1. ▶ Added SSI connector pin assignment on PXI J2. ▶ Added 4.1.7 Bus-mastering DMA Data Transfer.

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Preface

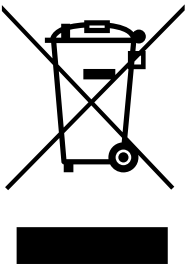
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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

NOTE: Additional information, aids, and tips that help users perform tasks.

CAUTION: Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

WARNING: Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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Table of Contents

Preface iii

List of Tables vii

List of Figures ix

1 Introduction 1

1.1 Features 2
1.2 Applications 3
1.3 Specifications 4
1.4 Software Support 14

2 Installation 19

2.1 Contents of Package 19
2.2 Unpacking 20
2.3 Card Layout 21
2.4 Switch and Jumper Settings 23
2.5 PCI Configuration 27

3 Signal Connections 29

3.1 Connectors Pin Assignment 29
3.2 Analog Input Signal Connection 37

4 Operation Theory 41

4.1 A/D Conversion 41
4.2 D/A Conversion 61
4.3 Digital I/O 71
4.4 General Purpose Timer/Counter Operation 71
4.5 Trigger Sources 79
4.6 User-controllable Timing Signals 86

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5 Calibration 95
5.1 Loading Calibration Constants 95
5.2 Auto-calibration 96
5.3 Saving Calibration Constants 96

Important Safety Instructions 97

Getting Service 99

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List of Tables

Table 1-1: Programmabel Input Range 5
Table 1-2: Bandwidth 6
Table 1-3: System Noise 7
Table 1-4: CMRR (DC to 60 Hz) 7
Table 1-5: Settling Time to Full Scale Step 8
Table 2-1: Board ID SW1 DIP Switch Pin Definitions 24
Table 3-1: CN1 Pin Assignment for DAQ/DAQe/PXI-2204/2205/2206 30
Table 3-2: CN1 Pin Assignment for DAQ/DAQe/PXI-2208 31
Table 3-3: CN2 Pin Assignment for DAQ/DAQe/PXI-2204/2205/2206 32
Table 3-4: CN2 Pin Assignment for DAQ/DAQe/PXI-2208 33
Table 3-5: CN1/CN2 Signal Description 34
Table 3-6: SSI Connector Pin Assignment 35
Table 3-7: SSI Connector Pin Assignment on PXI J2 36
Table 3-8: SSI Connector Legend 36
Table 4-1: Bipolar Analog Input Range and Output Digital Code on DAQ/DAQe/PXI-2204/2208 43
Table 4-2: Unipolar Analog Input Range and Output Digital Code on DAQ/DAQe/PXI-2204/2208 43
Table 4-3: Bipolar Analog Input Range and Output Digital Code for DAQ/DAQe/PXI-2205/2206 44
Table 4-4: Unipolar Analog Input Range and Output Digital Code for DAQ/DAQe/PXI-2205/2206 44
Table 4-5: Bipolar Output Code Table 61
Table 4-6: Unipolar Output Code Table 62
Table 4-7: Analog Trigger SRC1 (EXTATRIG) Ideal Transfer Characteristic 80
Table 4-8: User-controllable Timing Signals and Functionalities 87
Table 4-9: Auxiliary Function Input Signals and Functionalities 89
Table 4-10: SSI Timing Signal and Functions 91

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List of Figures

Figure 2-1: DAQe-2204/2205/2206/2208 Card Layout 21
Figure 2-2: DAQ-2204/2205/2206/2208 Card Layout 22
Figure 2-3: PXI-2204/2205/2206/2208 Card Layout 22
Figure 2-4: Board ID SW1 DIP Switch 23
Figure 2-5: Enable Board ID Configuration 25
Figure 2-6: DIO Initial Status (JP4) 26
Figure 3-1: Floating Source and RSE Input Connections 38
Figure 3-2: Ground-referenced Sources and NRSE Input Connections 39
Figure 3-3: Ground-referenced Source and Differential Input 39
Figure 3-4: Floating Source and Differential Input 40
Figure 4-1: Synchronous Digital Inputs Block Diagram 42
Figure 4-2: Synchronous Digital Inputs Timing 42
Figure 4-3: Scan Timing 47
Figure 4-4: Pre-trigger (Trigger occurs after M scans) 50
Figure 4-5: Pre-trigger (Trigger with scan in progress) 51
Figure 4-6: Pre-trigger with M_enable=0 (Trigger occurs before M scans) 52
Figure 4-7: Pre-trigger with M_enable=1 53
Figure 4-8: Middle-Trigger with M_enable = 1 54
Figure 4-9: Middle-Trigger (Trigger occurs when a scan is in progress) 55
Figure 4-10: Post-trigger 56
Figure 4-11: Delay trigger 57
Figure 4-12: Post trigger with Re-trigger 58
Figure 4-13: Linked List of PCI Address DMA Descriptors 60
Figure 4-14: Typical D/A Timing of Waveform Generation 64
Figure 4-15: Post Trigger Waveform Generation 65
Figure 4-16: Delay Trigger Waveform Generation 66
Figure 4-17: Re-triggered Waveform Generation with Post-Trigger (DLY2_Counter=0) 66
Figure 4-18: Finite Iterative Waveform Generation with Post-trigger (DLY2_Counter = 0) 67
Figure 4-19: Infinite Iterative Waveform Generation with Post-trigger (DLY2_Counter = 0) 68
Figure 4-20: Stop Mode I 69
Figure 4-21: Stop Mode II 70
Figure 4-22: Stop Mode III 70

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Figure 4-23: Mode1 Operation 73
Figure 4-24: Mode2 Operation 73
Figure 4-25: Mode3 Operation 74
Figure 4-26: Mode4 Operation 75
Figure 4-27: Mode5 Operation 76
Figure 4-28: Mode6 Operation 77
Figure 4-29: Mode7 Operation 77
Figure 4-30: Mode8 Operation 78
Figure 4-31: Analog Trigger Block Diagram 80
Figure 4-32: Below-Low Analog Trigger Condition 81
Figure 4-33: Above-High Analog Trigger Condition 81
Figure 4-34: Inside-Region Analog Trigger Condition 82
Figure 4-35: High-Hysteresis Analog Trigger Condition 83
Figure 4-36: Low-Hysteresis Analog Trigger Condition 84
Figure 4-37: External Digital Trigger 85
Figure 4-38: DAQ signals routing 86

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1 Introduction

The DAQ/DAQe/PXI-2204/2205/2206/2208 card is an advanced data acquisition card based on the 32-bit PCI or PCI Express® architecture. High performance designs and state-of-the-art technology make these cards ideal for data logging and signal analysis applications in medical, process control, etc.

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1.1 Features

The DAQ/DAQe/PXI-2204/2205/2206/2208 advanced data acquisition card has the following features:

- 32-bit PCI bus (DAQ/PXI models) or PCI Express (DAQe model), plug and play
- Up to 96 single-ended inputs or 48 differential inputs supporting combinations of SE and DI analog input signals
- Up to 1024 words analog input Channel Gain Queue configuration size
- Analog input resolution and sampling rate:
  - DAQ/DAQe/PXI-2204/2208: 12-bit and up to 3 MHz
  - DAQ/DAQe/PXI-2205: 16-bit and up to 500 KHz
  - DAQ/DAQe/PXI-2206: 16-bit and up to 250 KHz
- Programmable bipolar/unipolar analog input
- Programmable gain:
  - DAQ/DAQe/PXI-2204/2208: x1, x2, x4, x5, x8, x10, x20, x40, x50, x200
  - DAQ/DAQe/PXI-2205/2206: x1, x2, x4, x8
- A/D FIFO size: 1024 samples
- Versatile trigger sources: software trigger, external digital trigger, analog trigger and trigger from System Synchronization Interface (SSI)
- A/D data transfer: software polling and bus-mastering DMA with scatter/gather functionality
- Four A/D trigger modes including post-trigger, delay-trigger, pre-trigger and middle-trigger
- Two-channel D/A outputs with waveform generation capability (except DAQ/DAQe/PXI-2208)
- 1024 word length output data FIFO for D/A channels
- D/A data transfer: Software update and bus-mastering DMA with scatter/gather functionality
- Support System Synchronization Interface (SSI)
- Full A/D and D/A auto-calibration
- Jumper-free and software-configurable

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1.2 Applications

- Automotive Testing
- Cable Testing
- Transient signal measurement
- ATE
- Laboratory Automation
- Biotech measurement

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1.3 Specifications

Analog Input (AI)

- Programmable channels:
  - DAQ/DAQe/PXI-2204/2205/2206: 64 single-ended (SE) or 32 differential input (DI)
  - DAQ/DAQe/PXI-2208: 96 single-ended (SE) or 48 differential input (DI)
  - Mixing of SE and DI analog signal sources (Software selectable per channel)
- A/D converter:
  - DAQ/DAQe/PXI-2204/2008: LT1412 or equivalent
  - DAQ/DAQe/PXI-2205: A/D7665 or equivalent
  - DAQ/DAQe/PXI-2206: A/D7663 or equivalent
- Max sampling rate:
  - DAQ/DAQe/PXI-2204/2008: 3 MS/s (single-channel)
    1 MS/s (multi-channel)
  - DAQ/DAQe/PXI-2205: 500 kS/s
  - DAQ/DAQe/PXI-2206: 250 kS/s
- Resolution:
  - DAQ/DAQe/PXI-2204/2208: 12-bit, no missing code
  - DAQ/DAQe/PXI-2205/2206: 16-bit, no missing code
- Input coupling: DC
- FIFO buffer size:
  - DAQ/DAQe/PXI-2010: 8K samples
  - DAQ/DAQe/PXI-2005/2006/2016: 512 samples

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- Programmable input range:

Device	Bipolar input range	Unipolar input range
2204/ 2208	±10 V	—
	±5 V	0 to 10 V
	±2.5 V	0 to 5 V
	±2 V	0 to 4 V
	±1.25 V	0 to 2.5 V
	±1 V	0 to 2 V
	±0.5 V	0 to 1 V
	±0.25 V	0 to 0.5 V
	±0.2 V	0 to 0.4 V
	±0.05 V	0 to 0.1 V
2205/ 2206	±10 V	0 to 10 V
	±5 V	0 to 5 V
	±2.5 V	0 to 2.5 V
	±1.25 V	0 to 1.25 V

Table 1-1: Programmabel Input Range

- Operational common mode voltage range: ±11V
- Over-voltage protection:
  - Power on: Continuous ±30V
  - Power off: Continuous ±15V
- FIFO buffer size: 1024 samples
- Data transfers:
  - Programmed I/O
  - Bus-mastering DMA with scatter/gather
- Channel Gain Queue configuration size:
  - DAQ/DAQe/PXI-2204/2205/2206: 512 words
  - DAQ/DAQe/PXI-2208: 1024 words

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- Bandwidth (Typical 25ºC):

Device	Input range		Small signal bandwidth (-3dB)	Large signal bandwidth (1% THD)
2204/ 2208	±10 V	—	2000 kHz	—
	±5 V	0 V to 10 V		
	±2.5 V	0 V to 5 V		
	±1.25 V	0 V to 2.5 V		
	±2 V	0 V to 4 V	1450 kHz	—
	±0.5 V	0 V to 1 V		
	±1 V	0 V to 2 V	990 kHz	—
	±0.25 V	0 V to 0.5 V		
	±0.2 V	0 V to 0.4 V	240 kHz	—
	±0.05 V	0 V to 0.1 V		
2205	±10 V	0 V to 0 V	1600 kHz	300 kHz
	±5 V	0 V to 5 V	1400 kHz	310 kHz
	±2.5 V	0 V to 2.5 V	1000 kHz	310 kHz
	±1.25 V	0 V to 1.25 V	600 kHz	330 kHz
2206	±10 V	0 V to 10 V	760 kHz	300 kHz
	±5 V	0 V to 5 V	720 kHz	310 kHz
	±2.5 V	0 V to 2.5 V	610 kHz	310 kHz
	±1.25 V	0 V to 1.25 V	450 kHz	330 kHz

Table 1-2: Bandwidth

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- System Noise (LSBrms, including Quantization, Typical, 25°C)

Device	Input Range	System Noise	Input Range	System Noise
2205	±10 V	0.95 LSBrms	0 V to 10 V	1.5 LSBrms
	±5 V	1.0 LSBrms	0 V to 5 V	1.6 LSBrms
	±2.5 V	1.1 LSBrms	0 V to 2.5 V	1.7 LSBrms
	±1.25 V	1.3 LSBrms	0 V to 1.25 V	1.9 LSBrms
2206	±10 V	0.8 LSBrms	0 V to 10 V	0.9 LSBrms
	±5 V	0.85 LSBrms	0 V to 5 V	1.0 LSBrms
	±2.5 V	0.85 LSBrms	0 V to 2.5 V	1.0 LSBrms
	±1.25 V	0.9 LSBrms	0 V to 1.25 V	1.2 LSBrms

Table 1-3: System Noise

- Input impedance:
  - Normal power on: 1 GΩ/100 pF
  - Power off: 820 Ω
  - Overload: 820 Ω
- CMRR (DC to 60 Hz, Typical)

Device	Input Range	CMRR	Input Range	CMRR
2204/2208	All ranges	90 dB	—	—
2205/2206	±10 V	83 dB	0 V to 10 V	87 dB
	±5 V	87 dB	0 V to 5 V	90 dB
	±2.5 V	90 dB	0 V to 2.5 V	92 dB
	±1.25 V	92 dB	0 V to 1.25 V	93 dB

Table 1-4: CMRR (DC to 60 Hz)

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▶ Settling time to full-scale step (Typical, 25°C):

Device	Input Range		Condition	Settling time
2204/ 2208	±10 V		• Multiple channels, multiple ranges. • All samples in unipolar/ bipolar mode.	1 µs to 0.1% error
	±5 V	0 to 10 V		
	±2.5 V	0 to 5 V		
	±2 V	0 to 4 V		
	±1.25 V	0 to 2.5 V		
	±0.5 V	0 to 1 V		
	±10 V		• Multiple channels, multiple ranges. • All samples in unipolar/ bipolar mode.	1.25 µs to 0.1% error
	±5 V	0 to 10 V		
	±2.5 V	0 to 5 V		
	v2 V	0 to 4 V		
	±1.25 V	0 to 2.5 V		
	±0.5 V	0 to 1 V		
	±1 V	0 to 2 V	• Multiple channels, multiple ranges. • All samples in unipolar/ bipolar mode.	2 µs to 0.1% error
	±0.25 V	0 to 0.5 V		
	±0.2 V	0 to 0.4 V	• Multiple channels, multiple ranges. • All samples in unipolar/ bipolar mode.	5 µs to 0.1% error
	±0.05 V	0 to 0.1 V		
2205/ 2206	All Ranges		• Multiple channels, multiple ranges. • All samples in unipolar/ bipolar mode.	2 µs to 0.1% error, 4 µs to 0.01% error
	All Ranges		• Multiple channels, multiple ranges. • All samples in unipolar/ bipolar mode.	2 µs to 0.2% error, 4 µs to 0.01% error

Table 1-5: Settling Time to Full Scale Step

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- Time-base source:
  - Internal 40 MHz or external clock Input (f_{max}: 40 MHz, f_{min}: 1 MHz, 50% duty cycle)
- Trigger modes: Post-trigger, delay-trigger, pre-trigger and middle-trigger
- Offset error:
  - ±50mV max. for DAQ/DAQe/PXI-2204/2208
  - ±1mV max. for DAQ/DAQe/PXI-2205/2206
- Gain error (relative to calibration reference):
  - 0.6% of reading max. for DAQ/DAQe/PXI-2204/2208
  - 0.05% of reading max. for DAQ/DAQe/PXI-2205/2206

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Analog Output (AO)

NOTEThe DAQ/DAQe/PXI-2208 card does not support this function.

- Channels: Two-channel analog voltage output
- DA converter: LTC7545 or equivalent
- Max update rate: 1 MS/s
- Resolution: 12-bit
- FIFO buffer size:
  - 512 samples per channel when both channels are enabled for timed DA output
  - 1024 samples when only one channel is used for timed DA output
- Data transfers:
  - Programmed I/O
  - Bus-mastering DMA with scatter/gather
- Output range: ±10 V, 0 V to 10 V, ±AOEXTREF, 0 to AOEX-TREF
- Settling time: 3 S to 0.5 LSB accuracy
- Slew rate: 20 V/µS
- Output coupling: DC
- Protection: Short-circuit to ground
- Output impedance: 0.01Ω typical
- Output driving current: ±5 mA max
- Stability: Any passive load, up to 1500 pF
- Power-on state: 0V steady-state
- Power-on glitch: ±1.5 V/500 µS
- Relative accuracy: ±0.5 LSB typical, ±1 LSB max
- DNL: ±0.5 LSB typical, ±1.2 LSB max
- Offset error: ±1 mV max
- Gain error: ±0.05% of output max

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General Purpose Digital I/O (G.P. DIO, 82C55A)

- Channels: 24 programmable input/output
- Compatibility: TTL
- Input voltage:
  - Logic Low: VIL=0.8 V max; IIL=0.2 mA max
  - High: VIH=2.0 V max; IIH=0.02 mA max
- Output voltage:
  - Low: VOL=0.5 V max; IOL=8 mA max
  - High: VOH=2.7 V min; IOH=400 µA
- Synchronous Digital Inputs (SDI): On DAQ/DAQe/PXI-2204 model only.
  - Channels: 8 digital inputs sampled simultaneously with the analog signal input
  - Compatibility: TTL/CMOS
  - Input voltage:

  Logic Low: VIL=0.8 V max; IIL=0.2mA max

  Logic High: VIH=2.7 V min; IIL=0.02mA max

General Purpose Timer/Counter (GPTC)

NOTEThe DAQ/DAQe/PXI-2208 does not support this function.

- Channels: 2 independent up/down timer/counters
- Resolution: 16-bit
- Compatibility: TTL
- Clock source: Internal or external
- Max source frequency: 10 MHz

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Analog Trigger (A.Trig)

- Source:
  - All analog input channels
  - External analog trigger (EXTATRIG)
- Level: ±Full-scale, internal; ±10 V external
- Resolution: 8-bit
- Slope: Positive or negative (software-selectable)
- Hysteresis: Programmable
- Bandwidth: 400 kHz

External Analog Trigger Input (EXTATRIG)

- Input Impedance:
  - 40 kΩ for DAQ/DAQe/PXI-2204/2208
  - 20 kΩ for DAQ/DAQe/PXI-2205/2206
- Coupling: DC
- Protection: Continuous ±35 V maximum

Digital Trigger (D.Trig)

- Compatibility: TTL/CMOS
- Response: Rising or falling edge
- Pulse Width: 10 ns min

System Synchronous Interface (SSI)

- Trigger lines: 7

Stability

- Recommended warm-up time: 15 minutes
- On-board calibration reference:
  - Level: 5.000 V
  - Temperature coefficient: ±2 ppm/°C
  - Long-term stability: 6 ppm/1000 Hr

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Physical

- Dimensions:
  - 175mm by 107mm for DAQ-/DAQe-2204/2205/2206/2208
  - Standard CompactPCI form factor for PXI-2204/2205/2206/2208
- I/O connector: 68-pin female VHDCI type (e.g. AMP-787254-1)

Power Requirement (typical)

- +5 VDC
  - 1.3 A for DAQ/DAQe/PXI-2204
  - 1.2 A for DAQ/DAQe/PXI-2205/2206
  - 950 mA for DAQ/DAQe/PXI-2208
- +12 VDC
  - 358 mA for DAQe-2204
  - 344 mA for DAQe-2205
  - 390 mA for DAQe-2206
  - 258 mA for DAQe-2208
- +3.3 VDC
  - 815 mA for DAQe-2204
  - 735 mA for DAQe-2205
  - 710 mA for DAQe-2206
  - 815 mA for DAQe-2208

Operating Environment

- Ambient temperature: 0°C to 55°C
- Relative humidity: 10% to 90% non-condensing

Storage Environment

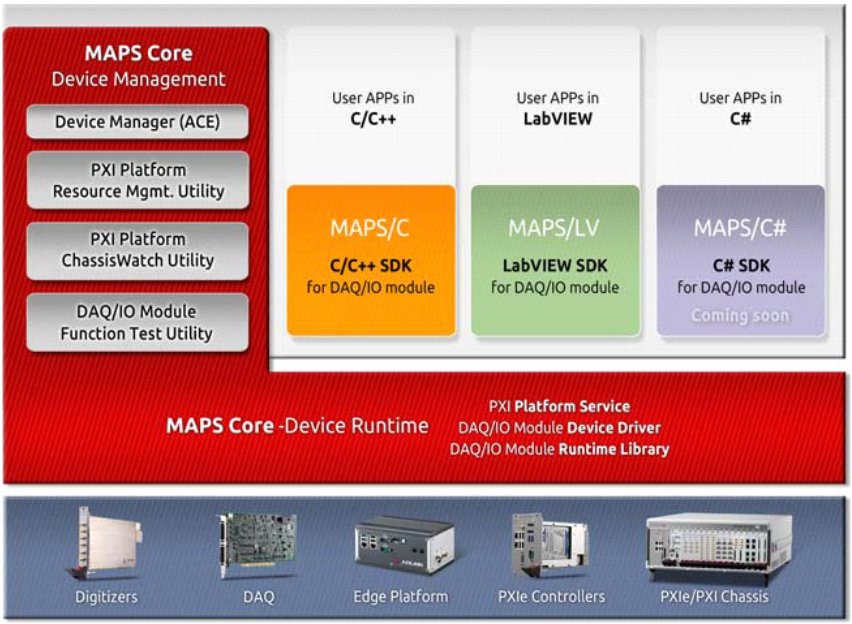
- Ambient temperature: -20°C to 80°C
- Relative humidity: 5% to 95% non-condensing

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1.4 Software Support

ADLINK provides versatile software drivers and packages to suit various user approaches to building a system. Aside from programming libraries, such as DLLs, for most Windows-based systems, ADLINK also provides drivers for other application environments such as LabVIEW. All software can be downloaded from the ADLINK official website. Commercial software drivers are protected with licensing authorization codes. Without an authorization code, you can install and run the demo version for trial/demonstration purposes for up to two hours. Contact your ADLINK dealer to purchase a software license. ADLINK Measurement, Automation & Platform Service (MAPS) is a software service package designed for data acquisition, automation and PXI platforms.

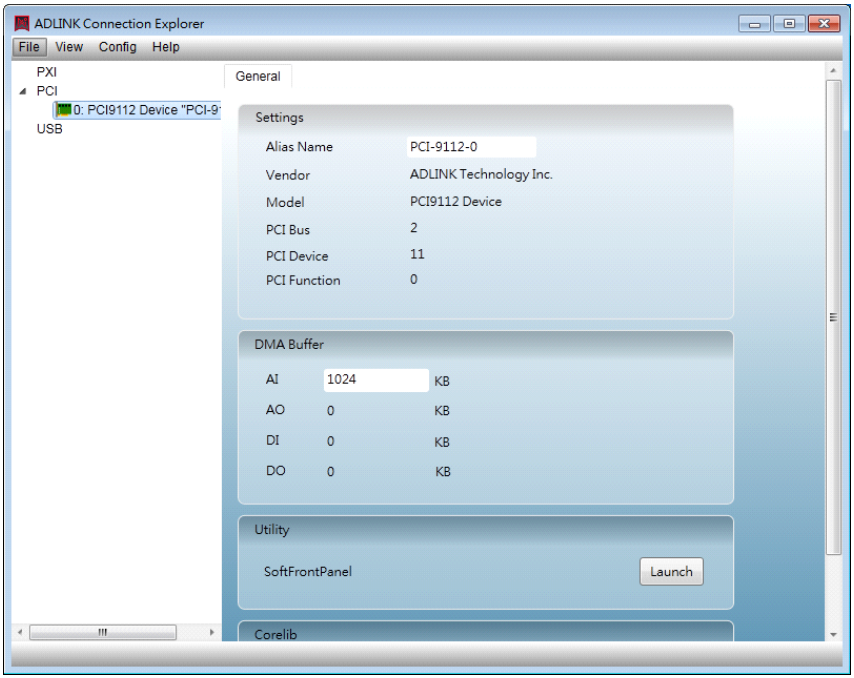
By leveraging low-level kernel management and a user friendly API, users can easily manage devices under a Windows environment and focus on developing applications.



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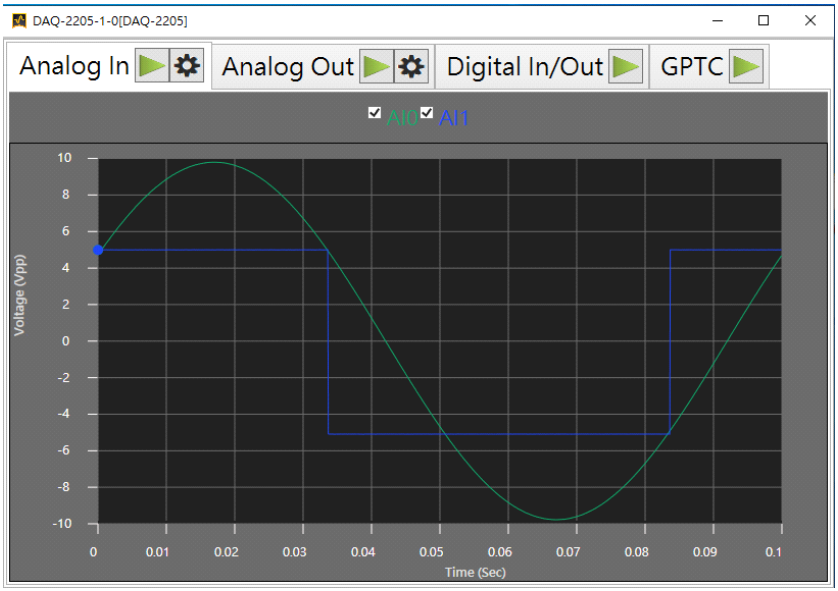
1.4.1 MAPS Core

ADLINK MAPS Core is a software package that includes all the device drivers for Windows and a system level management tool called ACE (ADLINK Connection Explorer). With MAPS Core installed, the operating system can identify ADLINK devices and assign the necessary resources for low-level access, such as IO read/write or direct memory access. MAPS Core is necessary for all ADLINK DAQ modules. To ensure the user has the latest software, go to the ADLINK product webpage or contact ADLINK technical service. MAPS Core also comes with a system management portal called ADLINK Connection Explorer (ACE). Through ACE, users can discover and manage ADLINK DAQ modules to reserve a certain size of memory buffer for DMA operation or set the user alias name for operating the module in a LabVIEW environment.



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ADLINK Connection Explorer (ACE) also provides a ready-to-use soft-front panel for digitizer products. Clicking the Launch button in the "Utility" block allows users to control digitizers through the UI and display the acquired waveform/data on the screen.



1.4.2 MAPS/LV, LabVIEW Support

Customers who develop their own programs in LabVIEW must install the MAPS/LV software package. MAPS/LV, also called DAQ-LabVIEW Plus, includes the software library and sample program for LabVIEW. For more information, download and install the latest MAPS/LV software from the following website and refer to the MAPS/LV manual:

https://www.adlinktech.com/Products/Data_Acquisition/DAQSoftware_Utility/MAPS_LV

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1.4.3 MAPS/C, C & C++ Support

Customers who develop their own programs in C or C++ environments must install the MAPS/C software package. MAPS/C includes all the software components required for developing applications in C/C++, such as header files, a device API library and versatile sample programs for understanding how to manipulate the device correctly. Find the latest MAPS/C on the ADLINK website.

https://www.adlinktech.com/Products/Data_Acquisition/DAQSoftware_Utility/MAPS_C

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2 Installation

This chapter describes how to install the DAQ/DAQe/PXI-2204/2205/2206/2208 card. The contents of the package and unpacking information that you should be aware of are outlined first.

2.1 Contents of Package

In addition to this User's Manual, the package includes the following items:

- DAQ/DAQe/PXI-2204/2205/2206/2208 multi-function data acquisition card
- Software Installation Guide

If any of these items are missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in case you want to ship or store the product in the future.

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2.2 Unpacking

Your DAQ/DAQe/PXI-2204/2205/2206/2208 card contains electro-static sensitive components that can be easily be damaged by static electricity.

Therefore, the card should be handled on a grounded anti-static mat. The operator should be wearing an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the card package for obvious damages. Shipping and handling may cause damage to the card. Be sure there are no shipping and handling damages on the modules carton before continuing.

After opening the card module carton, extract the system module and place it only on a grounded anti-static surface with component side up.

Again, inspect the module for damages. Press down on all the socketed IC's to make sure that they are properly seated. Do this only with the module place on a firm flat surface.

You are now ready to install your DAQ/DAQe/PXI-2204/2205/2206/2208 card.


NOTE:

DO NOT APPLY POWER TO THE CARD IF IT HAS BEEN DAMAGED.

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2.3 Card Layout

2.3.1 DAQe-2204/2205/2206/2208

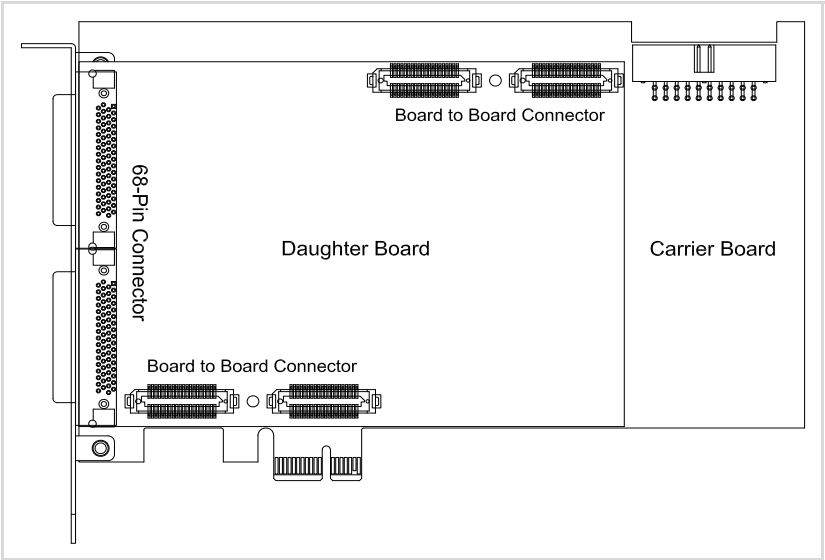


Figure 2-1: DAQe-2204/2205/2206/2208 Card Layout

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2.3.2 DAQ-2204/2205/2206/2208

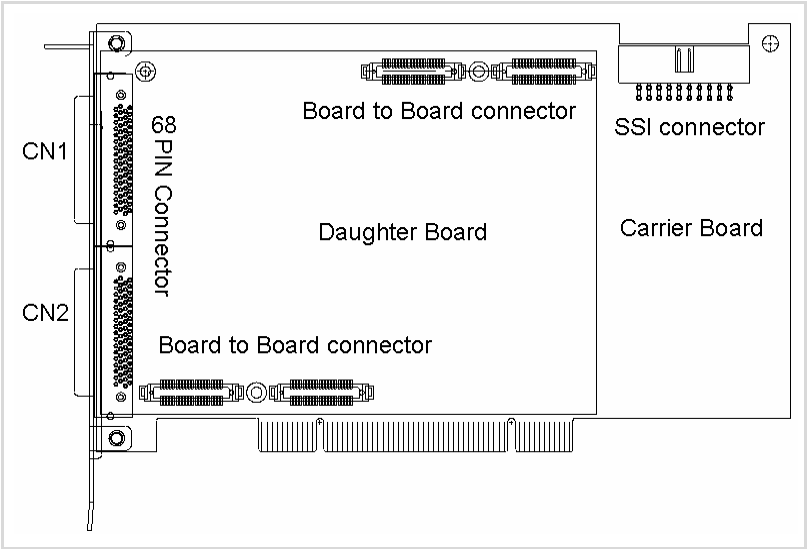


Figure 2-2: DAQ-2204/2205/2206/2208 Card Layout

2.3.3 PXI-2204/2205/2206/2208

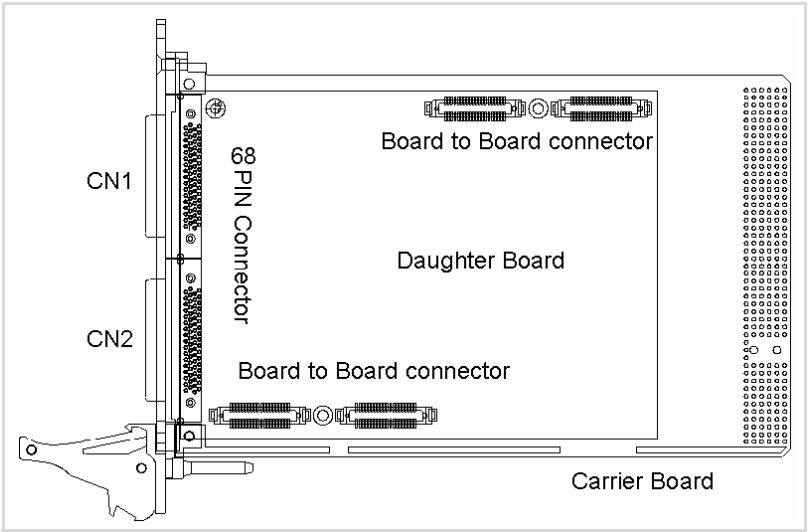


Figure 2-3: PXI-2204/2205/2206/2208 Card Layout

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2.4 Switch and Jumper Settings

2.4.1 Board ID (SW1)

The DAQ/DAQe-2000 Series has a built-in DIP switch (SW1), which is used to define each card's board ID. When there are multiple cards on the same platform, this board ID switch is useful for identifying each card's device number. After setting each DAQ/DAQe-2000 Series card, you can identify each card in the system with different device numbers. The default value of the Board ID is 0 and if you need to adjust it to another value, set the SW1 switch as shown in the table below.



Figure 2-4: Board ID SW1 DIP Switch

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SW1	Pin 1	Pin 2	Pin 3	Pin 4
Board ID	ID0	ID1	ID2	ID3
0	Off	Off	Off	Off
1	On	Off	Off	Off
2	Off	On	Off	Off
3	On	On	Off	Off
4	Off	Off	On	Off
5	On	Off	On	Off
6	Off	On	On	Off
7	On	On	On	Off
8	Off	Off	Off	On
9	On	Off	Off	On
10	Off	On	Off	On
11	On	On	Off	On
12	Off	Off	On	On
13	On	Off	On	On
14	Off	On	On	On
15	On	On	On	On

Table 2-1: Board ID SW1 DIP Switch Pin Definitions

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NOTE:

Board ID configuration is disabled by default. To enable Board ID configuration, install D2K-DASK and launch W2K_D2kUtil.exe in C:\ADLINK\D2K-DASK\Utility\. Select your Card Type and uncheck Ignore Board ID. See figure below.

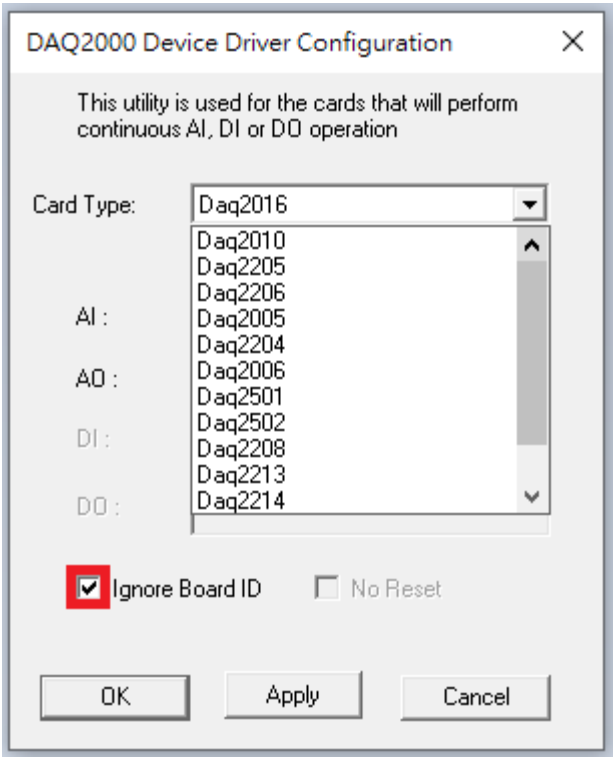


Figure 2-5: Enable Board ID Configuration

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2.4.2 DIO Initial Status (JP4)

The default jumper setting is enabled, making the DIO initial status low by using a 1K ohm resistor poll down to GND. To disable this feature, move the jumper cap as shown in the table below.

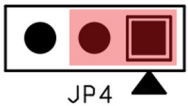
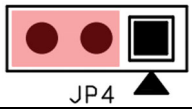
Disabled	
Enabled	

Figure 2-6: DIO Initial Status (JP4)

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2.5 PCI Configuration

2.5.1 Plug and Play

With support for plug and play, the card requests an interrupt number via its PCI controller. The system BIOS responds with an interrupt assignment based on the card information and on known system parameters. These system parameters are determined by the installed drivers and the hardware load seen by the system.

2.5.2 Configuration

The board configuration is done on a board-by-board basis for all PCI boards in the system. Because configuration is controlled by the system and software, there is no jumper setting required for base address, DMA, and interrupt IRQ.

The configuration is subject to change with every boot of the system as new boards are added or removed.

2.5.3 Troubleshooting

If your system doesn't boot or if you experience erratic operation with your PCI board in place, it is likely caused by an interrupt conflict. The BIOS Setup may be incorrectly configured. Consult the BIOS documentation that comes with your system to solve this problem.

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3 Signal Connections

This chapter describes DAQ/DAQe/PXI-2204/2205/2206/2208 card connectors and the signal connection between the DAQ/DAQe/PXI-2204/2205/2206/2208 card and external devices.

3.1 Connectors Pin Assignment

The DAQ/DAQe/PXI-2204/2205/2206/2208 card is equipped with two 68-pin VHDCI-type connector (AMP-787254-1). It is used for digital input/output, analog input/output, timer/counter signals, etc. One 20-pin ribbon male connector is used for SSI (System Synchronous Interface) in DAQ-/DAQe-2204/2205/2206/2208 card. The pin assignments of the connectors are defined in Table 3-1, Table 3-2, Table 3-3, and Table 3-4.

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3.1.1 CN1 Connector

AI0 (AIH0)	1	35	(AIL0) AI32
AI1 (AIH1)	2	36	(AIL1) AI33
AI2 (AIH2)	3	37	(AIL2) AI34
AI3 (AIH3)	4	38	(AIL3) AI35
AI4 (AIH4)	5	39	(AIL4) AI36
AI5 (AIH5)	6	40	(AIL5) AI37
AI6 (AIH6)	7	41	(AIL6) AI38
AI7 (AIH7)	8	42	(AIL7) AI39
AI8 (AIH8)	9	43	(AIL8) AI40
AI9 (AIH9)	10	44	(AIL9) AI41
AI10 (AIH10)	11	45	(AIL10) AI42
AI11 (AIH11)	12	46	(AIL11) AI43
AI12 (AIH12)	13	47	(AIL12) AI44
AI13 (AIH13)	14	48	(AIL13) AI45
AI14 (AIH14)	15	49	(AIL14) AI46
AI15 (AIH15)	16	50	(AIL15) AI47
AISENSE	17	51	AIGND
AI16 (AIH16)	18	52	(AIL16) AI48
AI17 (AIH17)	19	53	(AIL17) AI49
AI18 (AIH18)	20	54	(AIL18) AI50
AI19 (AIH19)	21	55	(AIL19) AI51
AI20 (AIH20)	22	56	(AIL20) AI52
AI21 (AIH21)	23	57	(AIL21) AI53
AI22 (AIH22)	24	58	(AIL22) AI54
AI23 (AIH23)	25	59	(AIL23) AI55
AI24 (AIH24)	26	60	(AIL24) AI56
AI25 (AIH25)	27	61	(AIL25) AI57
AI26 (AIH26)	28	62	(AIL26) AI58
AI27 (AIH27)	29	63	(AIL27) AI59
AI28 (AIH28)	30	64	(AIL28) AI60
AI29 (AIH29)	31	65	(AIL29) AI61
AI30 (AIH30)	32	66	(AIL30) AI62
AI31 (AIH31)	33	67	(AIL31) AI63
EXTATRIG	34	68	AIGND

Table 3-1: CN1 Pin Assignment for DAQ/DAQe/PXI-2204/2205/2206

* Symbols in “()” are for differential mode connection.

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AI0 (AIH0)	1	35	(AIL0) AI48
AI1 (AIH1)	2	36	(AIL1) AI49
AI2 (AIH2)	3	37	(AIL2) AI50
AI3 (AIH3)	4	38	(AIL3) AI51
AI4 (AIH4)	5	39	(AIL4) AI52
AI5 (AIH5)	6	40	(AIL5) AI53
AI6 (AIH6)	7	41	(AIL6) AI54
AI7 (AIH7)	8	42	(AIL7) AI55
AISENSE	9	43	AIGND
AI8 (AIH8)	10	44	(AIL8) AI56
AI9 (AIH9)	11	45	(AIL9) AI57
AI10 (AIH10)	12	46	(AIL10) AI58
AI11 (AIH11)	13	47	(AIL11) AI59
AI12 (AIH12)	14	48	(AIL12) AI60
AI13 (AIH13)	15	49	(AIL13) AI61
AI14 (AIH14)	16	50	(AIL14) AI62
AI15 (AIH15)	17	51	(AIL15) AI63
AI16 (AIH16)	18	52	(AIL16) AI64
AI17 (AIH17)	19	53	(AIL17) AI65
AI18 (AIH18)	20	54	(AIL18) AI66
AI19 (AIH19)	21	55	(AIL19) AI67
AI20 (AIH20)	22	56	(AIL20) AI68
AI21 (AIH21)	23	57	(AIL21) AI69
AI22 (AIH22)	24	58	(AIL22) AI70
AI23 (AIH23)	25	59	(AIL23) AI71
AIGND	26	60	AIGND
AI24 (AIH24)	27	61	(AIL24) AI72
AI25 (AIH25)	28	62	(AIL25) AI73
AI26 (AIH26)	29	63	(AIL26) AI74
AI27 (AIH27)	30	64	(AIL27) AI75
AI28 (AIH28)	31	65	(AIL28) AI76
AI29 (AIH29)	32	66	(AIL29) AI77
AI30 (AIH30)	33	67	(AIL30) AI78
AI31 (AIH31)	34	68	(AIL31) AI79

Table 3-2: CN1 Pin Assignment for DAQ/DAQe/PXI-2208

* Symbols in “()” are for differential mode connection.

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3.1.2 CN2 Connector

DA0OUT	1	35	AOGND
DA1OUT	2	36	AOGND
AOEXTREF	3	37	AOGND
NC	4	38	NC
DGND	5	39	DGND
EXTWFTRIG	6	40	DGND
EXTDTRIG	7	41	DGND
SSHOUT	8	42	SDI0 / DGND*
RESERVED	9	43	SDI1 / DGND*
RESERVED	10	44	SDI2 / DGND*
AFI1	11	45	SDI3 / DGND*
AFI0	12	46	DGND
GPTC0_SRC	13	47	DGND
GPTC0_GATE	14	48	DGND
GPTC0_UPDOWN	15	49	DGND
GPTC0_OUT	16	50	DGND
GPTC1_SRC	17	51	DGND
GPTC1_GATE	18	52	DGND
GPTC1_UPDOWN	19	53	DGND
GPTC1_OUT	20	54	DGND
EXTTIMEBASE	21	55	DGND
PB7	22	56	PB6
PB5	23	57	PB4
PB3	24	58	PB2
PB1	25	59	PB0
PC7	26	60	PC6
PC5	27	61	PC4
DGND	28	62	DGND
PC3	29	63	PC2
PC1	30	64	PC0
PA7	31	65	PA6
PA5	32	66	PA4
PA3	33	67	PA2
PA1	34	68	PA0

Table 3-3: CN2 Pin Assignment for DAQ/DAQe/PXI-2204/2205/2206

**Pin 42~45 are SDI<0.3> for DAQ/DAQe/PXI-2204; DGND for DAQ/DAQe/PXI-2205/2206*

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AI32 (AIH32)	1	35	(AIL32) AI80
AI33 (AIH33)	2	36	(AIL33) AI81
AI34 (AIH34)	3	37	(AIL34) AI82
AI35 (AIH35)	4	38	(AIL35) AI83
AI36 (AIH36)	5	39	(AIL36) AI84
AI37 (AIH37)	6	40	(AIL37) AI85
AI38 (AIH38)	7	41	(AIL38) AI86
AI39 (AIH39)	8	42	(AIL39) AI87
EXTATRIG	9	43	AIGND
AI40 (AIH40)	10	44	(AIL40) AI88
AI41 (AIH41)	11	45	(AIL41) AI89
AI42 (AIH42)	12	46	(AIL42) AI90
AI43 (AIH43)	13	47	(AIL43) AI91
AI44 (AIH44)	14	48	(AIL44) AI92
AI45 (AIH45)	15	49	(AIL45) AI93
AI46 (AIH46)	16	50	(AIL46) AI94
AI47 (AIH47)	17	51	(AIL47) AI95
AIGND	18	52	AIGND
NC	19	53	NC
EXTDTRIG	20	54	AFI0
EXTTIMEBASE	21	55	DGND
PB7	22	56	PB6
PB5	23	57	PB4
PB3	24	58	PB2
PB1	25	59	PB0
PC7	26	60	PC6
PC5	27	61	PC4
DGND	28	62	DGND
PC3	29	63	PC2
PC1	30	64	PC0
PA7	31	65	PA6
PA5	32	66	PA4
PA3	33	67	PA2
PA1	34	68	PA0

Table 3-4: CN2 Pin Assignment for DAQ/DAQe/PXI-2208

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CN1/CN2 Connector Signal Description

Signal Name	Reference	Direction	Description
AIGND	—	—	Analog ground for AI. All three ground references (AIGND, AOGND, and DGND) are connected together on board.
AI<0..63/95>	AIGND	Input	• For DAQ/DAQe/PXI-2204/2205/2206: Analog Input Channels 0~63. Each channel pair, AI<i, i+32> (I=0..31) can be configured either two single-ended inputs or one differential input pair(marked as AIH<0..31> and AIL<0..31>). • For DAQ/DAQe/PXI-2208: Analog Input Channels 0~95. Each channel pair, AI<i, i+48> (I=0..37) can be configured either two single-ended inputs or one differential input pair(marked as AIH<0..47> and AIL<0..47>).
AISENSE	AIGND	Input	Analog Input Sense. This pin is the reference for any channels AI<0..63> in NRSE input configuration.
EXTATRIG	AIGND	Input	External AI analog trigger
DA0OUT	AOGND	Output	AO channel 0
DA1OUT	AOGND	Output	AO channel 1
AOEXTREF	AOGND	Input	External reference for AO channels
AOGND	—	—	Analog ground for AO
EXTWFTRIG	DGND	Input	External AO waveform trigger
EXTDTRIG	DGND	Input	External AI digital trigger
RESERVED	—	Output	Reserved. Please leave it open

Table 3-5: CN1/CN2 Signal Description

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Signal Name	Reference	Direction	Description
SDI<0..3> *(for 2204 only)*	DGND	Input	Synchronous digital inputs. These 4 digital inputs are sampled simultaneously with the analog signal input.
GPTC<0,1>_SRC	DGND	Input	Source of GPTC<0,1>
GPTC<0,1>_GATE	DGND	Input	Gate of GPTC<0,1>
GPTC<0,1>_OUT	DGND	Input	Output of GPTC<0,1>
GPTC<0,1>_UPDOWN	DGND	Input	Up/Down of GPTC<0,1>
EXTTIMEBASE	DGND	Input	External Timebase
DGND	—	—	Digital ground
PB<7,0>	DGND	PIO*	Programmable DIO of 8255 Port B
PC<7,0>	DGND	PIO*	Programmable DIO of 8255 Port C
PA<7,0>	DGND	PIO*	Programmable DIO of 8255 Port A
AFI0	DGND	Input	Auxiliary Function Input 0 (ADCONV, AD_START)
AFI1	DGND	Input	Auxiliary Function Input 1 (DAWR, DA_START)

Table 3-5: CN1/CN2 Signal Description

3.1.3 SSI Connector

SSI_TIMEBASE	1	2	DGND
SSI_ADCONV	3	4	DGND
SSI_DAWR / RESERVED*	5	6	DGND
SSI_SCAN_START	7	8	DGND
RESERVED	9	10	DGND
SSI_AD_TRIG	11	12	DGND
SSI_DA_TRIG / RESERVED*	13	14	DGND
RESERVED	15	16	DGND
RESERVED	17	18	DGND
RESERVED	19	20	DGND

Table 3-6: SSI Connector Pin Assignment

*Pin 5 and 13 are reserved for DAQ/PXI-2208.

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SSI Connector Signal Description on PXI J2:

Sync. Signal	PXI J2 location	PXI Trigger Bus
SSI_TIMEBASE	B18	PXI_TRIG4
SSI_ADCONV	A16	PXI_TRIG1
SSI_SCAN_START	A18	PXI_TRIG3
SSI_AD_TRIG	C18	PXI_TRIG5
SSI_DAWR	A17	PXI_TRIG2
SSI_DA_START	B16	PXI_TRIG0
SSI_DA_TRIG	E18	PXI_TRIG6

Table 3-7: SSI Connector Pin Assignment on PXI J2

SSI Connector Signal Description:

SSI Timing Signal	Setting	Function
SSI_TIMEBASE	Master	Send the TIMEBASE out
	Slave	Accept the SSI_TIMEBASE to replace the internal TIMEBASE signal.
SSI_ADCONV	Master	Send the ADCONV out
	Slave	Accept the SSI_ADCONV to replace the internal ADCONV signal.
SSI_SCAN_START	Master	Send the SCAN_START out
	Slave	Accept the SSI_SCAN_START to replace the internal SCAN_START signal.
SSI_AD_TRIG	Master	Send the internal AD_TRIG out
	Slave	Accept the SSI_AD_TRIG as the digital trigger signal.
SSI_DAWR	Master	Send the DAWR out.
	Slave	Accept the SSI_DAWR to replace the internal DAWR signal.
SSI_DA_TRIG	Master	Send the DA_TRIG out.
	Slave	Accept the SSI_DA_TRIG as the digital trigger signal.

Table 3-8: SSI Connector Legend

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3.2 Analog Input Signal Connection

The DAQ/DAQe/PXI-2204/2205/2206/2208 card provides up to 64 single-ended or 32 differential analog input channels. You can fill the Channel Gain Queue to get desired combination of the input signal types. The analog signal can be converted to digital values by the A/D converter. To avoid ground loops and get more accurate measurements from the A/D conversion, it is important to understand the signal source type and how to connect the analog input signals.

3.2.1 Types of signal sources

Floating Signal Sources

A floating signal source means it is not connected in any way to the buildings ground system. A device with an isolated output is a floating signal source, such as optical isolator outputs, transformer outputs, and thermocouples.

Ground-Referenced Signal Sources

A ground-referenced signal means it is connected in some way to the building system. That is, the signal source is already connected to a common ground point with respect to the DAQ/DAQe/PXI-2204/2205/2206/2208 card, assuming that the computer is plugged into the same power system. Non-isolated outputs of instruments and devices that plug into the buildings power system are ground-referenced signal sources.

3.2.2 Input Configurations

Single-Ended Connections

A single-ended connection is used when the analog input signal is referenced to a ground that can be shared with other analog input signals. There are two types of single-ended connections: RSE and NRSE. In RSE configuration, the DAQ/DAQe/PXI-2204/2205/2206/2208 card provides the grounding point for the external analog input signals and is suitable for floating signal sources. In the NRSE configuration the board does not provide the grounding point, the external analog input

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signal provides its own reference grounding point and is suitable for ground-referenced signals.

Referenced Single-ended (RSE) Mode

In referenced single-ended mode, all input signals are connected to the ground provided by the DAQ/DAQe/PXI-2204/2205/2206/2208 card. This is suitable for connections with floating signal sources. Figure 3-1 shows an illustration. Note that when more than two floating sources are connected, these sources will be referenced to the same common ground.

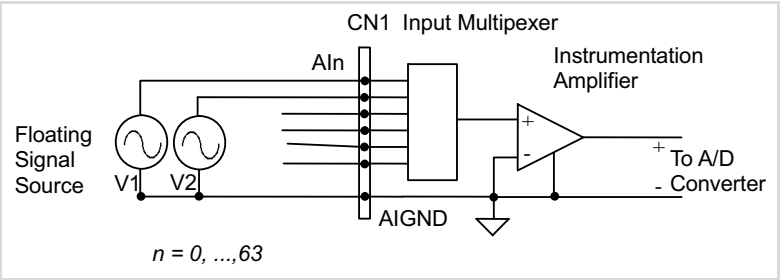


Figure 3-1: Floating Source and RSE Input Connections

Non-Referenced Single-ended (NRSE) Mode

To measure ground-referenced signal sources, which are connected to the same ground point, you can connect the signals in NRSE mode. Figure 3-2 illustrates the connection. The signals local ground reference is connected to the negative input of the instrumentation Amplifier (AISENSE pin on CN1 connector), and the common-mode ground potential between signal ground and the ground on board will be rejected by the instrumentation amplifier.

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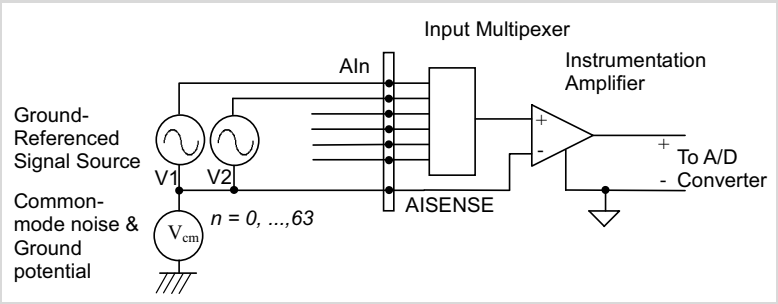


Figure 3-2: Ground-referenced Sources and NRSE Input Connections

3.2.3 Differential Input Mode

The differential input mode provides two inputs that respond to signal voltage difference between them. If the signal source is ground-referenced, the differential mode can be used for the common-mode noise rejection. Figure 3-3 shows the connection of ground-referenced signal sources under differential input mode.

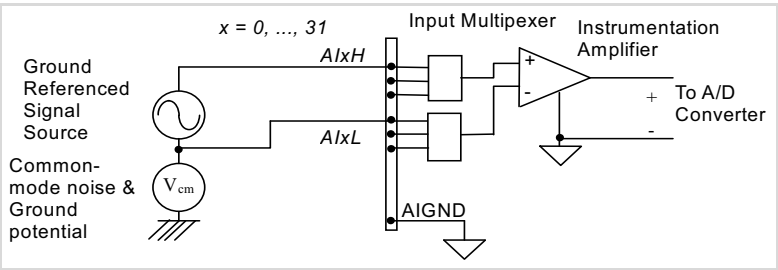


Figure 3-3: Ground-referenced Source and Differential Input

Ground-referenced Source and Differential Input

Figure 3-4 shows how to connect a floating signal source to the DAQ/DAQe/PXI-2204/2205/2206/2208 card in differential input mode. For floating signal sources, you need to add a resistor at each channel to provide a bias return path. The resistor value should be about 100 times the equivalent source impedance. If the source impedance is less than 100ohms, you can simply connect the negative side of the signal to AIGND as well as the negative input of the Instrumentation Amplifier without any

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resistors. In differential input mode, less noise couples into the signal connections than in single-ended mode.

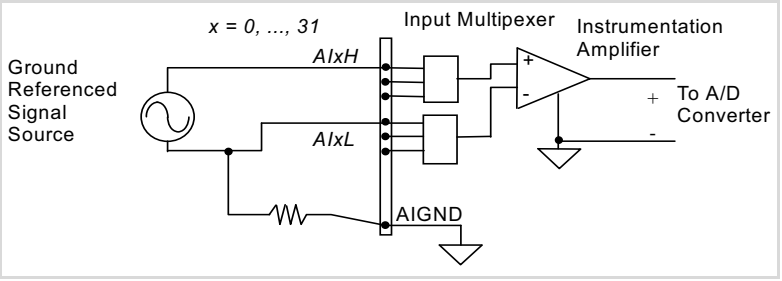


Figure 3-4: Floating Source and Differential Input

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4 Operation Theory

The operation theory of the DAQ/DAQe/PXI-2204/2205/2206/2208 card functions are described in this chapter. The functions include the A/D conversion, D/A conversion, digital I/O, and general purpose counter/timer. The operation theory can help you understand how to configure and program the DAQ/DAQe/PXI-2204/2205/2206/2208 card.

4.1 A/D Conversion

When using an A/D converter, you must know about the properties of the signal to be measured. You may decide which channel to use and how to connect the signals to the card. In addition, users should define and control the A/D signal configurations, including channels, gains, and polarities (unipolar/bipolar).

The A/D acquisition is initiated by a trigger source and you must decide how to trigger the A/D conversion. The data acquisition will start once a trigger condition is matched.

After the end of an A/D conversion, the A/D data is buffered in a Data FIFO. The A/D data can now be transferred into the system memory for further processing.

4.1.1 DAQ/DAQe/PXI-2204/2208 AI Data Format

Synchronous Digital Inputs (DAQ/DAQe/PXI-2204 only)

When each A/D conversion is completed, the 14-bits converted digital data accompanied with 2 bits of SDI<1..0>_X per channel from J5 will be latched into the 16-bit register and data FIFO as shown in Figure 4-1 and Figure 4-2. Therefore, you can simultaneously sample one analog signal with four digital signals. The data format of every acquired 16-bit data is as follows:

```
D11, D10, D9 ..... D1, D0, b3, b2, b1, b0
Where
D11, D10, D9 ..... D1, D0: 2's complement A/D
     12-bit data
b3, b2, b1, b0: Synchronous Digital Inputs
     SDI<3..0>
```


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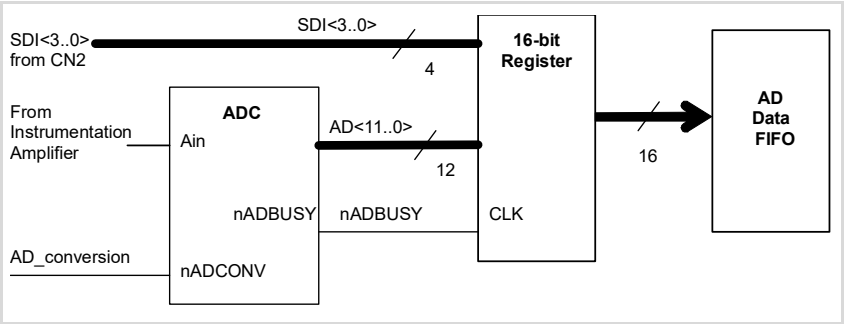


Figure 4-1: Synchronous Digital Inputs Block Diagram

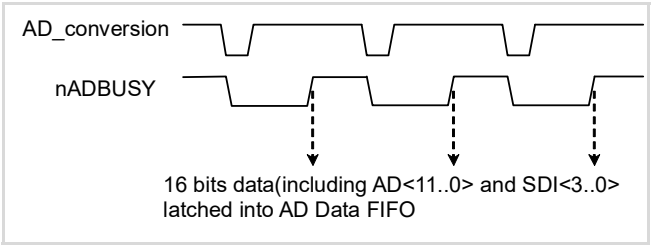


Figure 4-2: Synchronous Digital Inputs Timing

NOTE:

Since the analog signal is sampled when an A/D conversion starts (falling edge of A/D_conversion signal), while SDI<3..0> are sampled right after an A/D conversion completes (rising edge of nADBUSY signal). Precisely SDI<3..0> are sampled with 280ns lag to the analog signal.

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Table 4-1and Table 4-2 illustrate the ideal transfer characteristics of various input ranges of the DAQ/DAQe/PXI-2204/2205/2206/2208 card.

Description	Bipolar Analog Input Range				Digital code
Full-scale Range	±10V	±5V	±2.5V	±1.25V	—
Least significant bit	4.88mV	2.44mV	1.22mV	0.61mV	—
FSR-1LSB	9.9951V	4.9976V	2.4988V	1.2494V	7FFX
Midscale +1LSB	4.88mV	2.44mV	1.22mV	0.61mV	001X
Midscale	0V	0V	0V	0V	000X
Midscale –1LSB	-4.88mV	-2.44mV	-1.22mV	-0.61mV	FFFX
-FSR	-10V	-5V	-2.5V	-1.25V	800X

Table 4-1: Bipolar Analog Input Range and Output Digital Code on DAQ/DAQe/PXI-2204/2208

Note that the last 4 digital codes are SDI<3..0> and is supported only on DAQ/DAQe/PXI-2204)

Description	Unipolar Analog Input Range			Digital code
Full-scale Range	0V to 10V	0 to +5V	0 to +2.5V	—
Least significant bit	2.44mV	1.22mV	0.61mV	—
FSR-1LSB	9.9976V	4.9988V	2.9994V	7FFX
Midscale +1LSB	5.00244V	2.50122V	1.25061V	001X
Midscale	5V	2.5V	1.25V	000X
Midscale –1LSB	4.9976V	2.4988V	1.2494V	FFFX
-FSR	0V	0V	0V	800X

Table 4-2: Unipolar Analog Input Range and Output Digital Code on DAQ/DAQe/PXI-2204/2208

Note that the last 4 digital codes are SDI<3..0> and is supported only on DAQ/DAQe/PXI-2204.

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4.1.2 DAQ/DAQe/PXI-2005/2006/2016 AI Data Format

The data format of the acquired 16-bit A/D data is **2's Complement coding**. Table 4-3 and Table 4-4 illustrate the valid input ranges and the ideal transfer characteristics.

Description	Bipolar Analog Input Range				Digital code
Full-scale Range	±10V	±5V	±2.5V	±1.25V	—
Least significant bit	305.2 µV	152.6 µV	76.3 µV	38.15 µV	—
FSR-1LSB	9.999695V	4.999847V	2.499924V	1.249962V	7FFF
Midscale +1LSB	305.2 µV	152.6 µV	76.3 µV	38.15 µV	0001
Midscale	0V	0V	0V	0V	0000
Midscale -1LSB	-305.2 µV	-152.6 µV	-76.3 µV	-38.15 µV	FFFF
-FSR	-10V	-5V	-2.5V	-1.25V	8000

Table 4-3: Bipolar Analog Input Range and Output Digital Code for DAQ/DAQe/PXI-2205/2206

Description	Unipolar Analog Input Range				Digital code
Full-scale Range	0V to 10V	0 to +5V	0 to +2.5V	0 to +1.25V	—
Least significant bit	152.6 µV	76.3 µV	38.15 µV	19.07 µV	—
FSR-1LSB	9.999847V	4.999924V	2.499962V	1.249981V	7FFF
Midscale +1LSB	5.000153V	2.500076V	1.250038V	0.625019V	0001
Midscale	5V	2.5V	1.25V	0.625V	0000
Midscale -1LSB	4.999847V	2.499924V	1.249962V	0.624981V	FFFF

Table 4-4: Unipolar Analog Input Range and Output Digital Code for DAQ/DAQe/PXI-2205/2206

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4.1.3 Software Conversion with Polling Data Transfer Acquisition Mode (Software Polling)

This is the easiest way to acquire a single A/D data. The A/D converter starts one conversion whenever the dedicated software command is executed. Then the software would poll the conversion status and read the A/D data back when it is available.

This method is very suitable for applications that needs to process A/D data in real time. Under this mode, the timing of the A/D conversion is fully controlled by the software. However, it is difficult to control the A/D conversion rate.

Specifying Channel, Gain, and Input Configurations in the Channel Gain Queue

In Software Polling and Programmable Scan Acquisition mode, the channel, gain, polarity, and input configuration (RSE, NRSE, or DIFF) can be specified in the Channel Gain Queue. You can fill the channel number in the Channel Gain Queue in any order. The channel order of acquisition will be the same as the order you set in the Channel Gain Queue. Therefore, you can acquire data with user-defined channel orders and with different settings on each channel.

When the specified channels have been sampled from the first data to the last data in the Channel Gain Queue, the settings in Channel Gain Queue are maintained. You do not need to reconfigure the Channel Gain Queue if you want to keep on sampling data in the same order. The maximum number of entries you can set in the Channel Gain Queue is 512.

Example:

First you can set entries in Channel Gain Queue:

- Ch3 with bipolar ±10V, RSE connection
- Ch1 with bipolar ±2.5V, DIFF connection
- Ch2 with unipolar 5V, NRSE connection
- Ch1 with bipolar ±2.5V, DIFF connection

If you read 10 data by software polling method, then the acquisition sequence of channels is 3, 1, 2, 1, 3, 1, 2, 1, 3, 1.

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4.1.4 Programmable Scan Acquisition Mode

Scan Timing and Procedure

It is recommended that you use this mode if your applications need a fixed and precise A/D sampling rate. You can accurately program the period between conversions of individual channels. There are at least four counters which need to be specified:

- SI_counter (24-bit): Specify the Scan Interval = SI_counter / Timebase
- SI2_counter (16-bit): Specify the data Sampling Interval = SI2_counter/Timebase
- PSC_counter (24-bit): Specify Post Scan Counts after a trigger event
- NumChan_counter (9-bit): Specify the number of samples per scan

The acquisition timing and the meanings of the 2 counters are illustrated in Figure 4-3.

TIMEBASE Clock Source

In scan acquisition mode, all the A/D conversions start on the output of counters, which use TIMEBASE as the clock source. By software you can specify the TIMEBASE to be either an internal clock source (onboard 40 MHz clock) or an external clock input (EXTTIMEBASE) on CN2 connector. The external TIMEBASE is useful when you want to acquire data at rates not available with the internal A/D sample clock. The external clock source should generate TTL-compatible continuous clocks and with a maximum frequency of 40 MHz while the minimum should be 1 MHz. Refer to section 4.6 for information on user-controllable timing signals.

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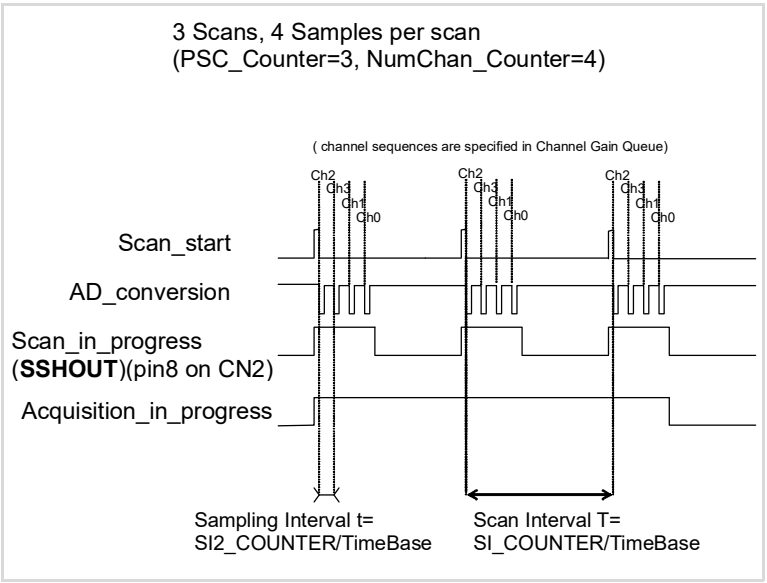


Figure 4-3: Scan Timing

There are four trigger modes to start the scan acquisition. Refer to section 4.1 for details. The data transfer mode is discussed in the following section.

NOTE:

The maximum A/D sampling rate is 3 MHz for DAQ/DAQe/PXI-2204/2208, 500 kHz for DAQ/DAQe/PXI-2205, and 250 kHz for DAQ/DAQe/PXI-2206. Therefore, the minimum setting of SI2_counter is 14 for DAQ/DAQe/PXI-2204/2208, 80 for DAQ/DAQe/PXI-2205, and 160 for DAQ/DAQe/PXI-2206 while using the internal TIMEBASE.

The SI_counter is a 24-bit counter and the SI2_counter is a 16-bit counter. The maximum scan interval using the internal Timebase = 2^{24}/40 Ms = 0.419 s, and the maximum sampling interval between two channels using the internal Timebase = 2^{16}/40 Ms = 1.638 ms.

The scan interval may not be smaller than the product of the data sampling interval and the NumChan_counter value. The relationship can be represented as: SI_counter>=SI2_counter * NumChan_counter.

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Scan with SSH

You can send the SSHOUT signal on CN2 to external S&H circuits to sample and hold all signals if you want to simultaneously sample all channels in a scan, as illustrated in Figure 4-3.


NOTE:

The DAQ/DAQe/PXI-2208 does not support this function.

The SSHOUT signal is sent to external S&H circuits to hold the analog signal. You must implement external S&H circuits on their own to carry out the S&H function. There are no onboard S&H circuits.

4.1.5 Specifying Channels, Gains, and Input Configurations in the Channel Gain Queue

Like software polling acquisition mode, the channel, gain, and input configurations can be specified in the Channel Gain Queue under the scan acquisition mode. Note that in scan acquisition mode, the number of entries in the Channel Gain Queue is normally equivalent to the value of NumChan_counter (that is, the number of samples per scan).

Example: Set

- SI2_counter = 160
- SI_counter = 640
- PSC_counter = 3
- NumChan_counter = 4
- Timebase = Internal clock source
- Channel entries in the Channel Gain Queue: ch1, ch2, ch0, ch2

Then

- Acquisition sequence of channels: 1, 2, 0, 2, 1, 2, 0, 2, 1, 2, 0, 2
- Sampling interval: 160/40 Ms = 4 µs
- Scan interval: 640/40 Ms = 16 µs
- Equivalent sampling rate of ch0, ch1: 62.5 kHz
- Equivalent sampling rate of ch2: 125 kHz

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4.1.6 Trigger Modes

The DAQ/DAQe/PXI-2204/2205/2206/2208 card provides four trigger sources (internal software trigger, external analog trigger, and digital trigger sources, and SSI trigger signals). You must select one of them as the source of the trigger event. A trigger event occurs when the specified condition is detected on the selected trigger source. For example, a rising edge on the external digital trigger input. Refer to section 4.6 for more information on SSI signals.

There are four trigger modes (pre-trigger, post-trigger, middle-trigger, and delay-trigger) working with the four trigger sources to initiate different scan data acquisition timing when a trigger event occurs. They are described in the following sections. For information on trigger sources, refer to section 4.5.

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Pre-Trigger Acquisition

Use pre-trigger acquisition in applications where you want to collect data before a trigger event. The A/D starts to sample when you execute the specified function calls to begin the pre-trigger operation, and it stops when the trigger event occurs. Users must program the value M in M_counter (16 bits) to specify the amount of the stored scans before the trigger event. If an external trigger occurs, the program only stores the last M scans of data converted before the trigger event, as illustrated in Figure 4-4, where M_counter = M =3, PSC_counter = 0. The post scan count is 0 because there is no sampling after the trigger event in pre-trigger acquisition. The total stored amount of data = Number of enabled channels * M_counter.

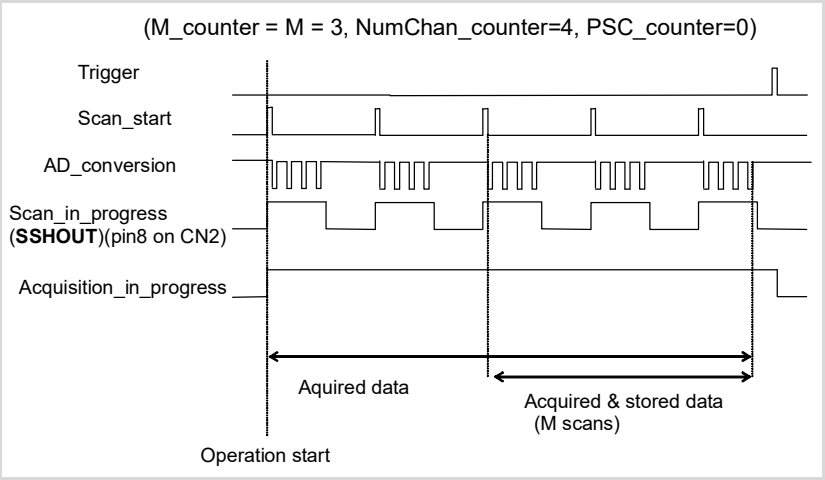


Figure 4-4: Pre-trigger (Trigger occurs after M scans)

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Note that if a trigger event occurs when a scan is in progress, the data acquisition won't stop until the scan completes, and the stored M scans of data includes the last scan. Therefore, the first stored data will always be the first channel entry of a scan (that is, the first channel entry in the Channel Gain Queue if the number of entries in the Channel Gain Queue is equivalent to the value of NumChan_counter), no matter when a trigger signal occurs, as illustrated in Figure 16, where M_counter = M =3, NumChan_counter = 4, PSC_counter = 0.

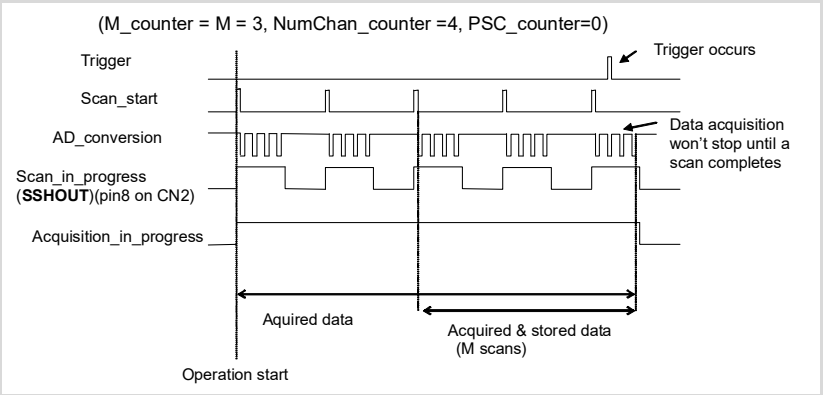


Figure 4-5: Pre-trigger (Trigger with scan in progress)

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When the trigger signal occurs before the first M scans of data are converted, the amount of stored data could be fewer than the originally specified amount M_counter, as illustrated in Figure 4-6. This situation can be avoided by setting M_enable. If M_enable is set to 1, the trigger signal will be ignored until the first M scans of data are converted, and it assures the user M scans of data under pre-trigger mode, as illustrated in Figure 4-7. However, if M_enable is set to 0, the trigger signal will be accepted any time, as shown in Figure 4-6. Note that the total amount of stored data will always be equal to the number in the M_counter because data acquisition does not stop until a scan is completed.

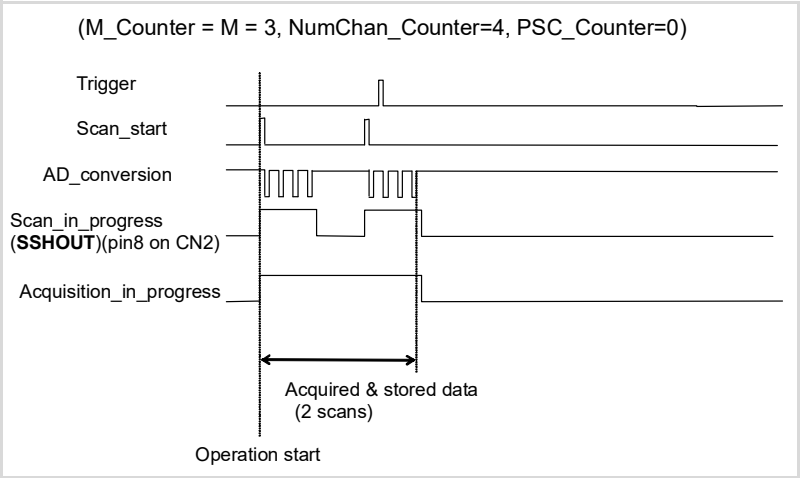


Figure 4-6: Pre-trigger with M_enable=0 (Trigger occurs before M scans)

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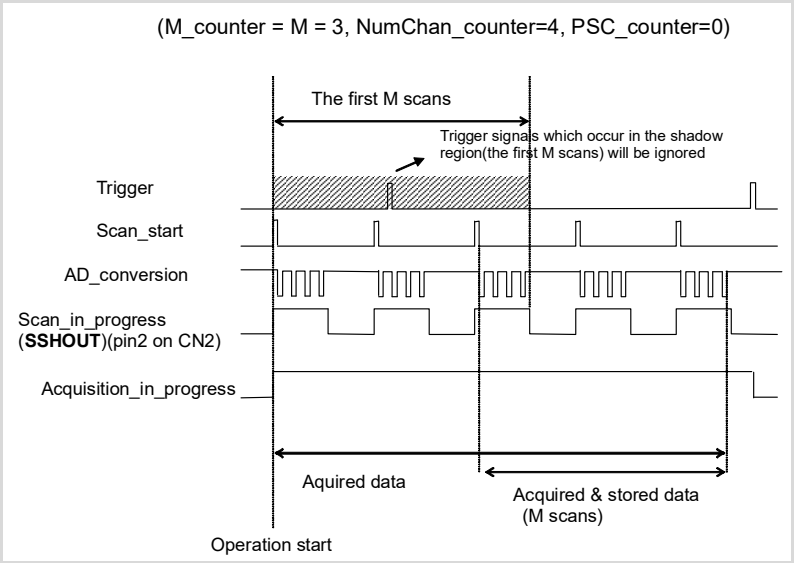


Figure 4-7: Pre-trigger with M_enable=1

NOTE:

The PSC_counter is set to 0 in pre-trigger acquisition mode.

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Middle-Trigger Acquisition

Use middle-trigger acquisition in applications where you want to collect data before and after a trigger event. The number of scans (M) stored before the trigger is specified in M_counter, while the number of scans (N) after the trigger is specified in PSC_counter.

Like pre-trigger mode, the number of stored data could be less than the specified amount of data (M+N), if an external trigger occurs before M scans of data are converted. The M_enable bit in middle-trigger mode takes the same effect as in pre-trigger mode. If M_enable is set to 1, the trigger signal will be ignored until the first M scans of data are converted, and it assures the user with (M+N) scans of data under middle-trigger mode. However, if M_enable is set to 0, the trigger signal will be accepted at any time. Figure 4-8 shows the acquisition timing with M_enable=1.

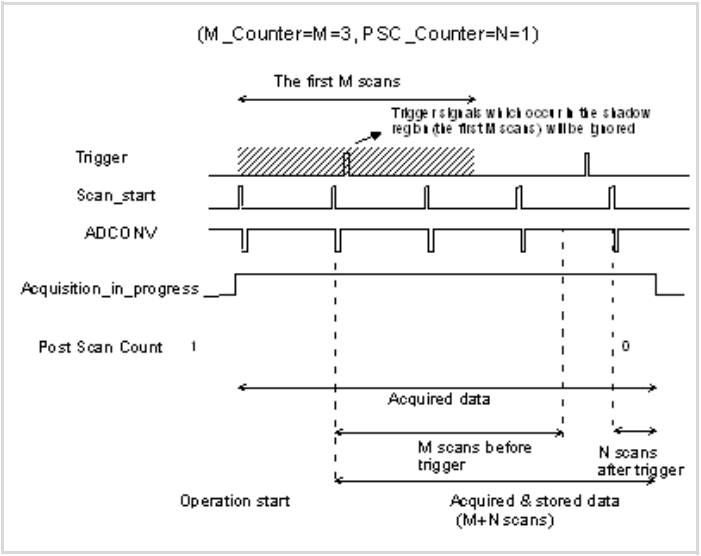


Figure 4-8: Middle-Trigger with M_enable = 1

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If the trigger event occurs when a scan is in progress, the stored N scans of data would include this scan, as illustrated in Figure 4-9.

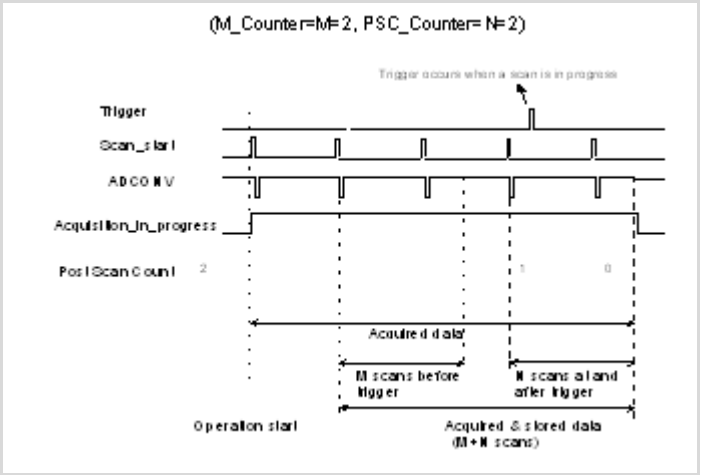


Figure 4-9: Middle-Trigger (Trigger occurs when a scan is in progress)

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Post-Trigger Acquisition

Use post-trigger acquisition in applications where you want to collect data after a trigger event. The number of scans after the trigger is specified in PSC_counter, as illustrated in Figure 4-10. The total acquired data length = NumChan_counter * PSC_counter.

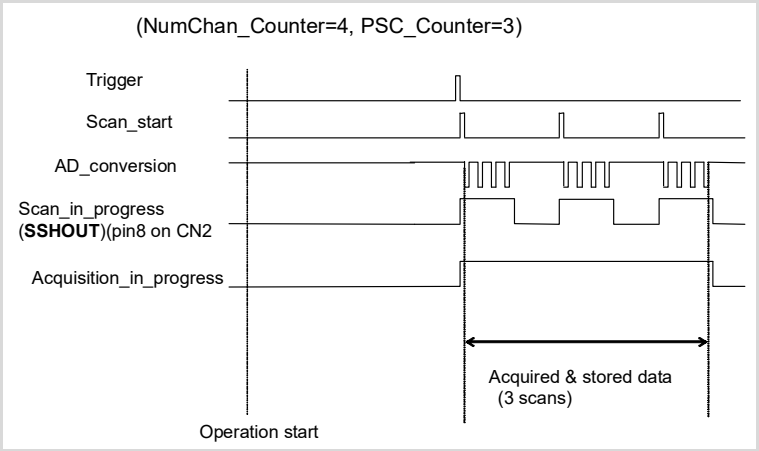


Figure 4-10: Post-trigger

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Delay Trigger Acquisition

Use delay trigger acquisition in applications where you want to delay the data collection after the occurrence of a specified trigger event. The delay time is controlled by the value, which is pre-loaded in the Delay_counter (16-bit). The counter counts down on the rising edge of the Delay_counter clock source after the trigger condition is met. The clock source can be software-programmed either by the TIMEBASE clock (40 MHz) or A/D sampling clock (TIMEBASE / SI2_counter). When the count reaches 0, the counter stops and the card starts to acquire data. The total acquired data length = NumChan_counter * PSC_counter.

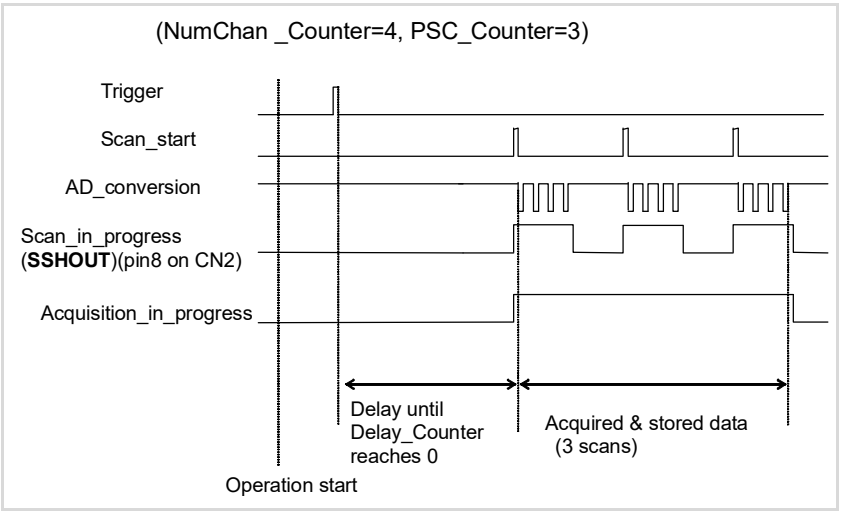


Figure 4-11: Delay trigger

NOTE:

When the Delay_counter clock source is set to TIMEBASE, the maximum delay time is 2^{16}/40 Ms or 1.638 ms. When the source is set to A/D sampling clock, the maximum delay time may be higher than 2^{16} * SI2_counter / 40M.

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Use post-trigger or delay-trigger acquisition with re-trigger function in applications where you want to collect data after several trigger events. The number of scans after each trigger is specified in PSC_counter, and users could program Retrig_no to specify the re-trigger numbers. Figure 4-12 illustrates an example. In this example, two scans of data is acquired after the first trigger signal, then the card waits for the re-trigger signal (re-trigger signals which occur before the first two scans is completed will be ignored). When the re-trigger signal occurs, two more scans are performed. The process repeats until specified amount of re-trigger signals are detected. The total acquired data length = NumChan_counter * PSC_counter * Re-trig_no.

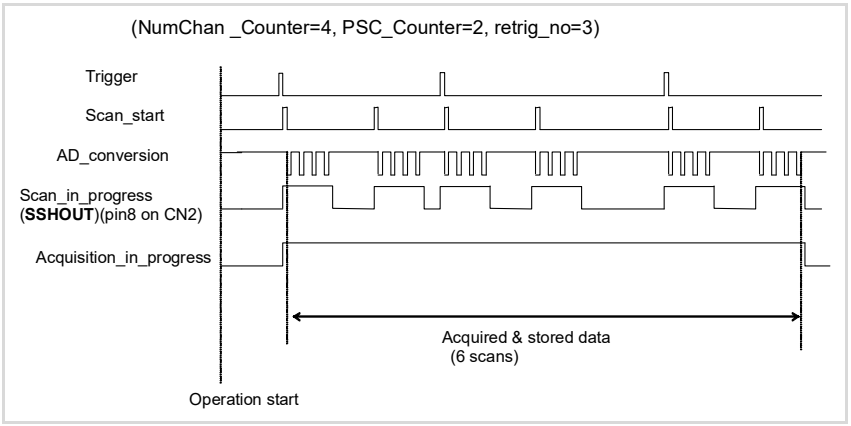


Figure 4-12: Post trigger with Re-trigger

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4.1.7 Bus-mastering DMA Data Transfer

In programmable scan acquisition mode, all DAQ/DAQe/PXI series cards supports bus-mastering DMA data transfer. PCI bus-mastering DMA is necessary for high speed DAQ in order to utilize the maximum bus bandwidth. The bus-mastering controller controls the PCI bus when it becomes the master. Bus mastering reduces the size of the onboard memory and reduces CPU loading since data is directly transferred to the system memory with no host CPU intervention.

Bus-mastering DMA provides the fastest data transfer rate on a PCI bus. Once the analog input operation starts, control returns to your program. The hardware temporarily stores the acquired data in the onboard AD Data FIFO, then transfers the data to a user-defined DMA buffer memory in the computer. Note that even when the acquired data length is less than the Data FIFO, the AD data is not kept in the Data FIFO but rather directly transferred to the host memory by the bus-mastering DMA.

The DMA transfer mode is very complex to program. It is recommended that you use a high-level program library provided by the ADLINK driver to configure this card. By using a high-level programming library for high speed DMA data acquisition, you convert through their specified counters. After the AD trigger condition is matched, the data will be transferred to the system memory by the bus-mastering DMA.

The PCI controller also supports the scatter/gather bus mastering DMA function that enables transfer of large amounts of data by linking all the memory blocks into a continuous linked list.

In a multi-user or multitasking OS, like Windows or Linux, it is difficult to allocate a large continuous memory block to do the DMA transfer. Therefore, the PCI controller provides the function of scatter-gather or chaining mode DMA to link the non-continuous memory blocks into a linked list, allowing transfers of very large amounts of data without being limited by the fragment of small size memory. You may configure the linked list for the input DMA channel or the output DMA channel. Figure 4-13 shows a linked list that is constructed by three DMA descriptors. Each descriptor contains a PCI address, a PCI dual-address, a transfer size, and the pointer to the next descriptor. PCI address and PCI dual address cycle

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support 64-bit addresses which can be mapped into more than 4 GB of the address space. You can allocate many small size memory blocks and chain their associative DMA descriptors altogether by their application programs.

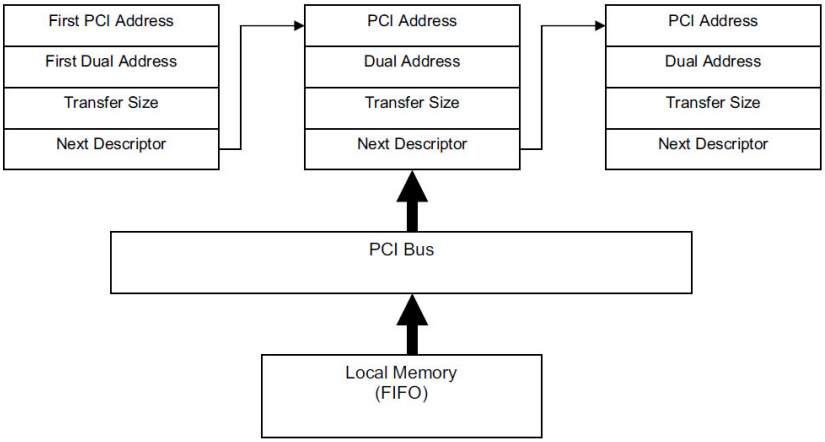


Figure 4-13: Linked List of PCI Address DMA Descriptors

In non-chaining mode, the maximum DMA data transfer size is 2M double words (8 MB). However, by using chaining mode-scatter/gather, there is no limitation for the DMA data transfer size. You may also link the descriptor nodes circularly to achieve a multi-buffered mode DMA.

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4.2 D/A Conversion

NOTEThe DAQ/DAQe/PXI-2208 card does not support this function.

There are two 12-bit D/A output channels available in the DAQ/DAQe/PXI-2204/2205/2206 card. When using D/A converters, you should assign and control the D/A converter reference sources for the D/A operation mode and D/A channels. You could also set the output polarity to unipolar or bipolar.

The reference selection control lets you utilize in full the multiplying characteristics of the D/A converters. Internal 10V reference and external reference inputs are available in the DAQ/DAQe/PXI-2204/2205/2206 card. The range of the D/A output is directly related to the reference. The digital codes that are updated to the D/A converters will multiply with the reference to generate the analog output. While using internal 10V reference, the full range would be –10V to +9.9951V in the bipolar output mode, and 0V to 9.9976V in the unipolar output mode. While using an external reference, you can reach different output ranges by connecting different references. For example, if connecting a DC –5V with the external reference, then you can get a full range from –4.9976V to +5V in the bipolar output with inverting characteristics due to the negative reference voltage. You could also have an amplitude modulated (AM) output by feeding a sinusoidal signal into the reference input. The range of the external reference should be within ±10V. Table 4-5 and Table 4-6 illustrates the relationship between digital code and output voltages with Vref=10V and if internal reference is selected.

Digital Code	Analog Output
111111111111	Vref * (2047/2048)
100000000001	Vref * (1/2048)
100000000000	0V
011111111111	-Vref * (1/2048)
000000000000	-Vref

Table 4-5: Bipolar Output Code Table

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Digital Code	Analog Output
111111111111	Vref * (4095/4096)
100000000000	Vref * (2048/4096)
000000000001	Vref * (1/4096)
000000000000	0V

Table 4-6: Unipolar Output Code Table

The D/A conversion is initiated by a trigger source. You must decide how to trigger the D/A conversion. The data output will start when a trigger condition is met. Before the start of D/A conversion, D/A data is transferred from the computer's main memory to a buffering Data FIFO.

Two D/A conversion modes are available: Software Update and Timed Waveform Generation. These are described below, including the timing, trigger source control, trigger modes, and data transfer methods. Either mode may be applied to D/A channels independently. You can simultaneously software update DA CH0 while generating timed waveforms on CH1.

4.2.1 Software Update

This is the easiest way to generate D/A output. To do this:

1. Specify the D/A output channels.
2. Set output polarity (unipolar or bipolar) and reference source (internal 10V or external AOEXTREF).
3. Update the digital values into D/A data registers through a software output command.

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4.2.2 Timed Waveform Generation

This mode can provide your applications with a precise D/A output with a fixed update rate. It can be used to generate an infinite or finite waveform. You can accurately program the update period of the D/A converters.

The D/A output timing is provided through a combination of counters in the FPGA on board. There are a total of five counters to be specified. These counters include:

- UI_counter (24 bits): specify the DA update interval is equal to CHUI_counter/TIMEBASE
- UC_counter (24 bits): specify the total update counts in a single waveform
- IC_counter (24 bits): specify the iteration counts of waveform
- DA_DLY1_counter (16 bits): specify the delay from the trigger to the first update start
- DA_DLY2_counter (16 bits): specify the delay between two consecutive waveform generations

Figure 4-14 shows a typical D/A timing diagram assuming the data in the data buffer are 2V, 4V, -4V, 0V. D/A updates its output on each rising edge of DAWR. The meaning of the counters enumerated above are discussed in the following sections.

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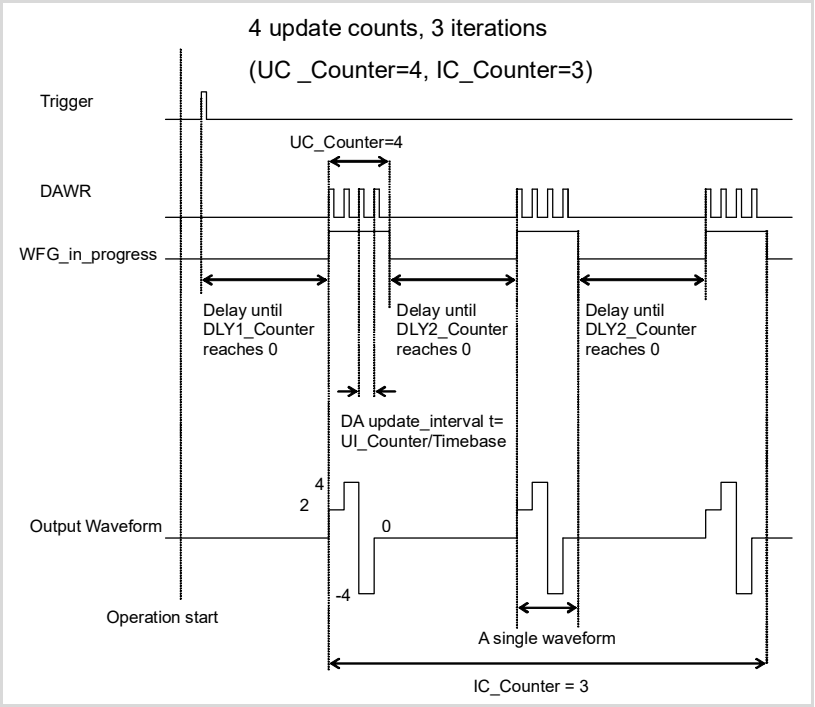


Figure 4-14: Typical D/A Timing of Waveform Generation

NOTE:

The maximum D/A update rate is 1 MHz. Therefore, the minimum setting of the UI_counter is 40 while using an internal TIMEBASE (40 MHz).

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4.2.3 Trigger Modes

Post-Trigger Generation

Use post-trigger when you want to perform DA waveform right after a trigger event occurs. In this trigger mode DLY1_Counter is ignored and not be specified. Figure 4-15 shows a single waveform generated right after a trigger signal is detected and assuming the data in the data buffer are 2V, 4V, 6V, 3V, 0V, -4V, -2V, and 4V. The trigger signal could come from a software command, an analog trigger or a digital trigger. Refer to section 4.5 for detailed information.

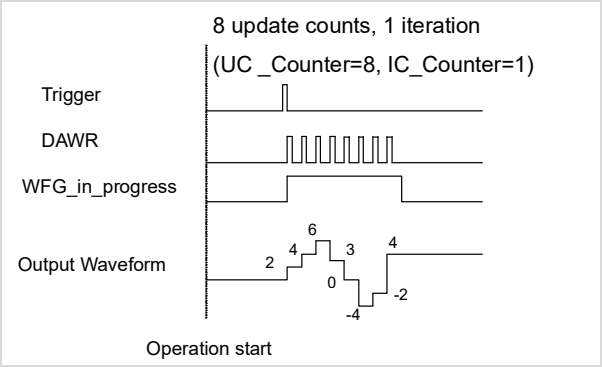


Figure 4-15: Post Trigger Waveform Generation

Delay-Trigger Generation

Use delay trigger when you want to delay the waveform generation after a trigger event. In Table 4-16, DA_DLY1_counter determines the delay time from the trigger signal to the start of the waveform generation, assuming the data in the data buffer are 2V, 4V, 6V, 3V, 0V, -4V, -2V, and 4V. DLY1_counter counts down on the rising edge of its clock source after the trigger condition is met. When the count reaches 0, the counter stops and the DAQ/DAQe/PXI-2204/2205/2206/2208 card starts the waveform generation. This DLY1_Counter is 16-bit wide and you can set the delay time in units of TIMEBASE (delay time = DLY1_Counter/TIMEBASE) or in units of update period (delay time = DLY1_Counter * UI_counter/TIMEBASE), so the delay time can reach a wider range.

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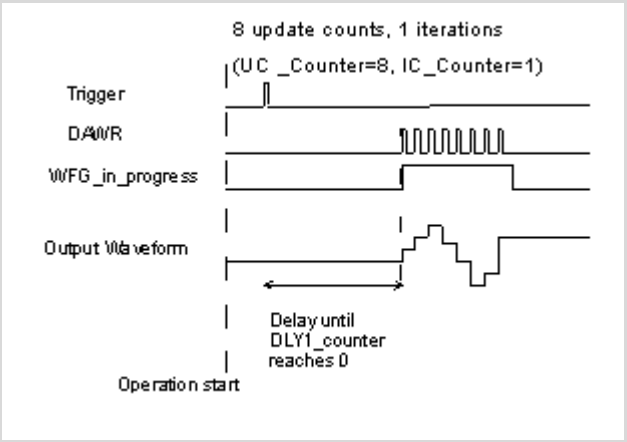


Figure 4-16: Delay Trigger Waveform Generation

Post-Trigger or Delay-Trigger with Re-trigger

Use post-trigger or delay-trigger with re-trigger function when you want to generate waveform after more than one trigger events. The re-trigger function can be enabled or disabled by software setting. In Figure 4-17, each trigger signal will initiate a waveform generation assuming the data in the data buffer are 2V, 4V, 2V, and 0V. However, the trigger event would be ignored while the waveform generation is ongoing.

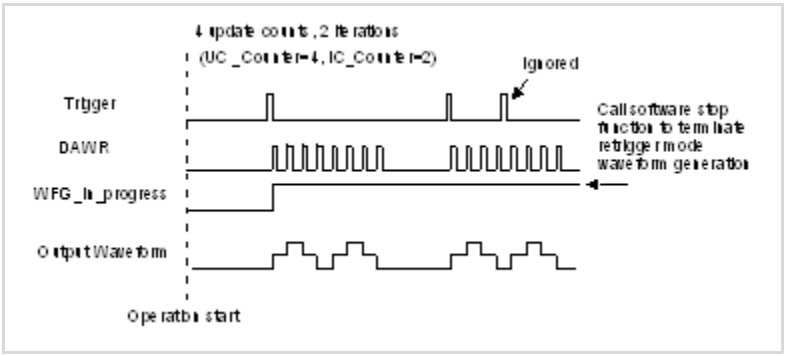


Figure 4-17: Re-triggered Waveform Generation with Post-Trigger (DLY2_Counter=0)

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Iterative Waveform Generation

Set IC_Counter in order to generate iterative waveforms from the data of a single waveform. The counter stores the iteration number and the iterations may be finite (Figure 4-18) or infinite (Figure 4-19). Take note that in infinite mode the waveform generation does not stop until software stop function is executed and IC_Counter is still valid when stop mode III is selected. Both figures assume that the data in the data buffer are 2V, 4V, 2V, and 0V.

An onboard data FIFO is used to buffer the digital data for DA output. If the data size of a single waveform you specified (That is, Update Counts in UC_counter) is less than the FIFO size, after initially transferring the data from the host PC memory to the FIFO on board, the data in the FIFO will be automatically re-transmitted whenever a single waveform is completed. Therefore, it does not occupy the PCI bandwidth when repetitive waveforms are performed. However, if the size of a single waveform were larger than that of the FIFO, it needs to be intermittently loaded from the host PC's memory via DMA, when a repetitive waveforms is performed thus PCI bandwidth would be occupied.

The data FIFO size on the DAQ/DAQe/PXI-2204/2205/2206/2208 card is 1024 (words) when one DA channel is enabled, or 512 (words) when both DA channels are enabled.

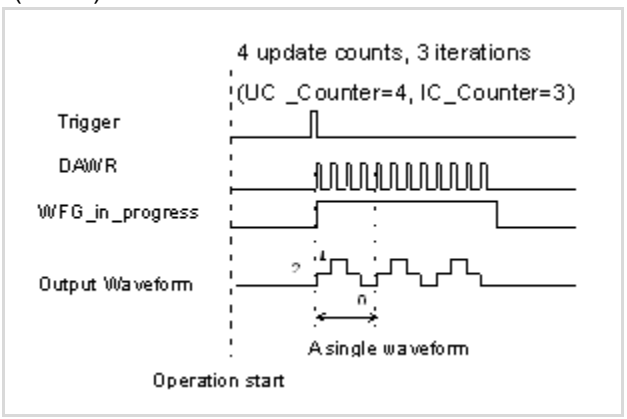


Figure 4-18: Finite Iterative Waveform Generation with Post-trigger (DLY2_Counter = 0)

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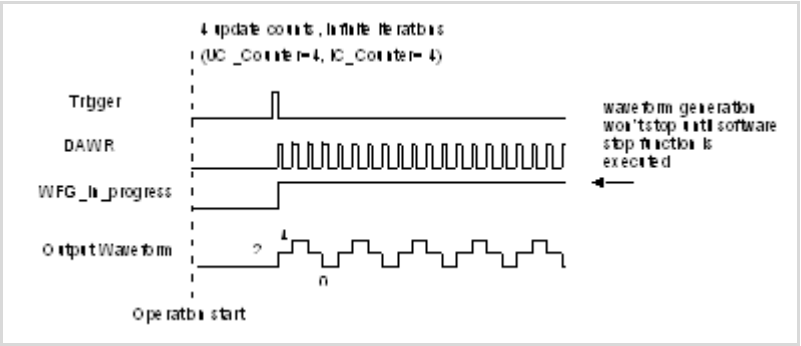


Figure 4-19: Infinite Iterative Waveform Generation with Post-trigger (DLY2_Counter = 0)

Delay2 in Iterative Waveform Generation

To stretch out the flexibility of the D/A waveform generation, we add a DLY2_Counter to separate two consecutive waveforms in iterative waveform generation. The time between two waveforms is assigned by setting the value of the DLY2_Counter. The DLY2_Counter starts to count down after a waveform generation finishes and the next waveform generation starts right after it counts down to zero, as shown in Figure 4-20. This DLY2_Counter is 16-bit wide and you may set the delay time in unit of TIMEBASE (delay time = DLY2_Counter/TIMEBASE) or in unit of update period (delay time = DLY2_Counter * UI_Counter/TIMEBASE), so the delay time can reach a wider range.

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Stop Modes of Scan Update

You can call software stop function to stop waveform generation when it is still in progress. Three stop modes are provided for timed waveform generation meant to stop the waveform generation. You can apply these three modes to stop waveform generation no matter infinite or finite waveform generation mode is selected.

Figure 4-20 illustrates an example for stop mode I, assuming the data in the data buffer are 2V, 4V, 2V, and 0V. In this mode, the waveform stops immediately when software command is asserted.

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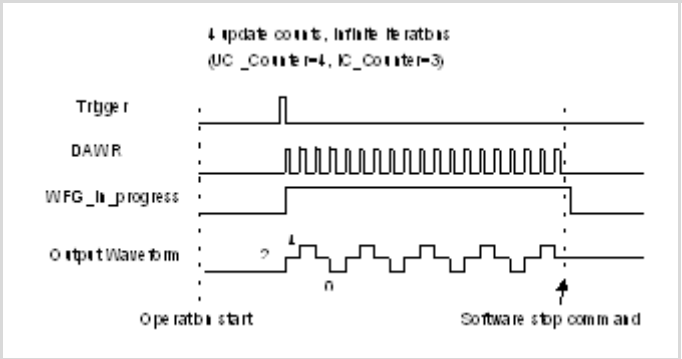


Figure 4-20: Stop Mode I

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In stop mode II, after a software stop command is given, the waveform generation does not stop until a complete single waveform is finished. See Figure 4-21. Since the UC_counter is set to four, the total DA update counts (number of pulses of DAWR signal) must be a multiple of four (update counts = 20 in this example).

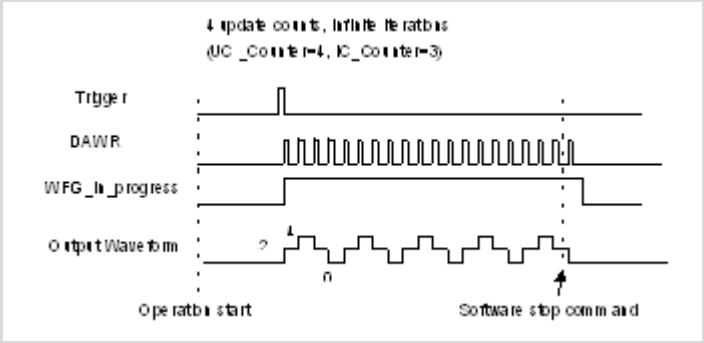


Figure 4-21: Stop Mode II

In stop mode III, after a software stop command is given, the waveform generation does not stop until the performed number of waveforms is a multiple of the IC_Counter. See Figure 4-22. Since the IC_Counter is set to three, the total generated waveforms must be a multiple of three (waveforms = 6 in this example), and the total DA update counts must be a multiple of 12 (UC_counter * IC_Counter). You can compare these three figures to see the differences.

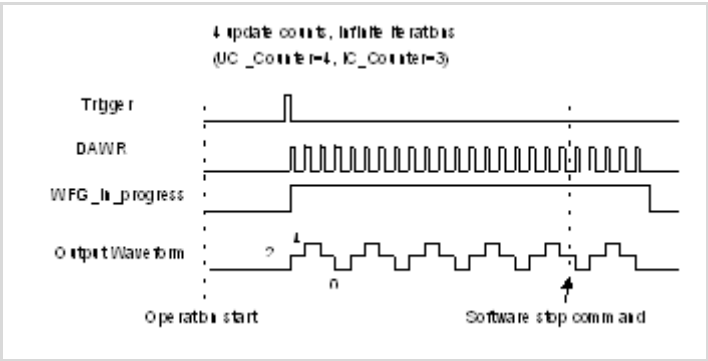


Figure 4-22: Stop Mode III

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4.3 Digital I/O

The DAQ/DAQe/PXI-2204/2205/2206/2208 card contains 24 lines of general-purpose digital I/O (GPIO) which is provided through the 82C55A chip.

The 24-line GPIO are separated into three ports: Port A, Port B and Port C. Port A and Port B can be programmed to be either input or output ports. Port C can be separated into high bit (PC4-PC7) and low bit (PC0-PC3), and both high bit and low bit ports can be programmed for input or output. Upon system startup or reset, all the GPIO pins are reset to high impedance inputs.

The DAQ/DAQe/PXI-2010 also provides two digital inputs per channel (SDI from CN2), which are sampled simultaneously with an analog signal input and is stored with the 12-bit AD data. Refer to Figure 4.1 for the more details.

4.4 General Purpose Timer/Counter Operation

NOTEThe DAQ/DAQe/PXI-2208 card does not support this function.

Two independent 16-bit up/down timer/counter are designed within FPGA for various applications. They have the following features:

- Count up/down controlled by hardware or software
- Programmable counter clock source (internal or external clock up to 10 MHz)
- Programmable gate selection (hardware or software control)
- Programmable input and output signal polarities (high active or low active)
- Initial count can be loaded from software
- Current count value can be read-back by software without affecting circuit operation

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4.4.1 The Basics of Timer/Counter Functions

Each timer/counter has three inputs that can be controlled via hardware or software. These are clock input (GPTC_CLK), gate input (GPTC_GATE), and up/down control input (GPTC_UPDOWN). The GPTC_CLK input provides a clock source input to the timer/counter. Active edges on the GPTC_CLK input make the counter increment or decrement. The GPTC_UPDOWN input controls whether the counter counts up or down. The GPTC_GATE input is a control signal which acts as a counter enable or a counter trigger signal under different applications.

The output of timer/counter is GPTC_OUT. After power-up, GPTC_OUT is pulled high by a pulled-up resister about 10K ohms. Then GPTC_OUT goes low after the DAQ/DAQe/PXI-2204/2205/2206/2208 card is initialized.

All the polarities of input/output signals can be programmed by software. In this chapter, for easy explanation, all GPTC_CLK, GPTC_GATE, and GPTC_OUT are assumed to be active high or rising-edge triggered in the figures.

4.4.2 General Purpose Timer/Counter modes

Eight programmable timer/counter modes are provided. All modes start operating following a software-start signal that is set by the software. The GPTC software reset initializes the status of the counter and re-loads the initial value to the counter. The operation remains halted until the software-start is re-executed. The operating theories under different modes are described in the following sections.

Mode1: Simple Gated-Event Counting

In this mode, the counter counts the number of pulses on the GPTC_CLK after the software-start. Initial count can be loaded from software. Current count value can be read-back by software any time without affecting the counting. GPTC_GATE is used to enable/disable counting. When GPTC_GATE is inactive, the counter halts the current count value. Figure 4-23 illustrates the operation with initial count = 5, countdown mode.

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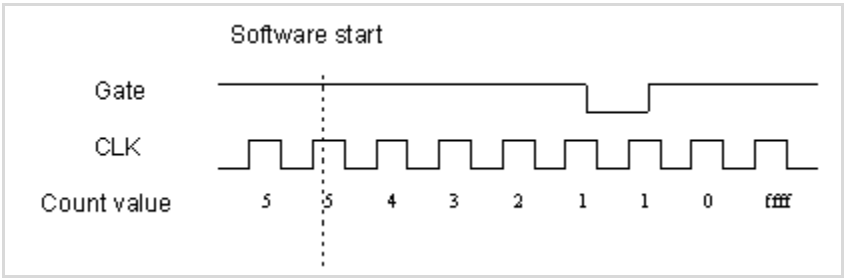


Figure 4-23: Mode1 Operation

Mode2: Single Period Measurement

In this mode, the counter counts the period of the signal on GPTC_GATE in terms of GPTC_CLK. Initial count can be loaded from software. After the software-start, the counter counts the number of active edges on GPTC_CLK between two active edges of GPTC_GATE. After the completion of the period interval on GPTC_GATE, GPTC_OUT outputs high and then current count value can be read-back by software. Figure 4-24 illustrates the operation where initial count = 0, count-up mode.

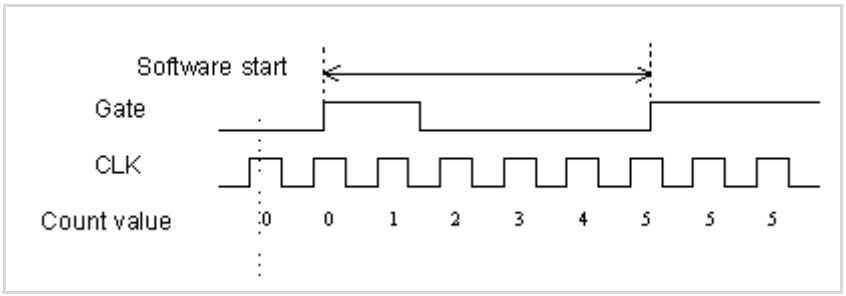


Figure 4-24: Mode2 Operation

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Mode3: Single Pulse-width Measurement

In this mode, the counter counts the pulse-width of the signal on GPTC_GATE in terms of GPTC_CLK. Initial count can be loaded from software. After the software-start, the counter counts the number of active edges on GPTC_CLK when GPTC_GATE is in its active state. After the completion of the pulse-width interval on GPTC_GATE, GPTC_OUT outputs high, then current count value can be read-back by software. Figure 4-25 illustrates the operation where initial count = 0, count-up mode.

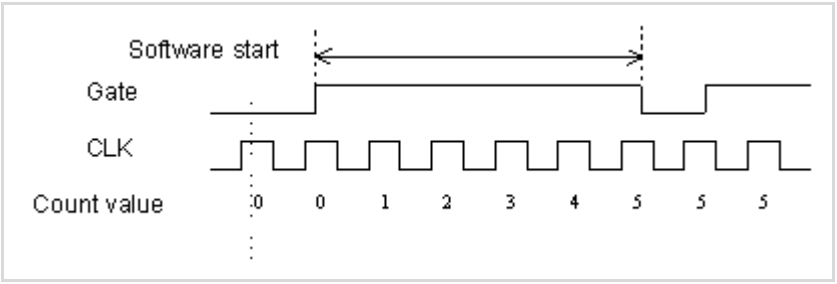


Figure 4-25: Mode3 Operation

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Mode4: Single Gated Pulse Generation

This mode generates a single pulse with programmable delay and programmable pulse-width following the software-start. The two programmable parameters could be specified in terms of periods of the GPTC_CLK input by software. GPTC_GATE is used to enable/disable counting. When GPTC_GATE is inactive, the counter halts the current count value. Figure 4-26 illustrates the generation of a single pulse with a pulse delay of two and a pulse-width of four.

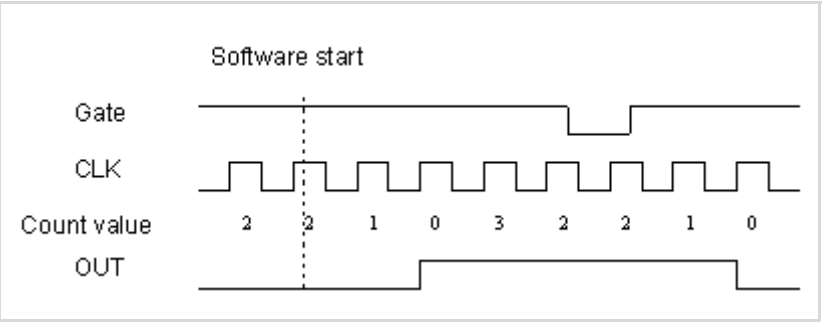


Figure 4-26: Mode4 Operation

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Mode5: Single Triggered Pulse Generation

This function generates a single pulse with programmable delay and pro-grammable pulse-width following an active GPTC_GATE edge. You could specify these programmable parameters in terms of periods of the GPTC_CLK input. Once the first GPTC_GATE edge triggers the single pulse, GPTC_GATE takes no effect until the software-start is re-executed. Figure 4-27 illustrates the generation of a single pulse with a pulse delay of two and a pulse-width of four.

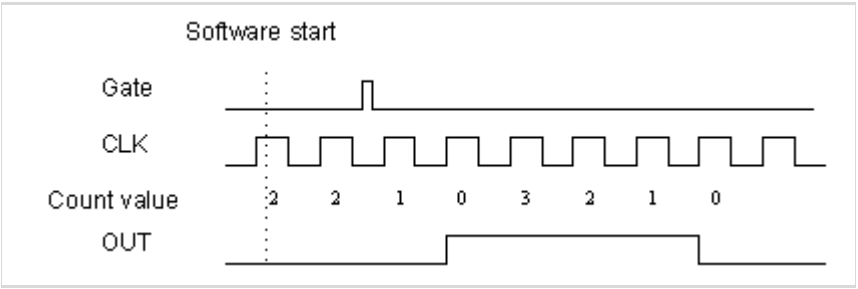


Figure 4-27: Mode5 Operation

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Mode6: Re-triggered Single Pulse Generation

This mode is similar to Mode5 except that the counter generates a pulse following every active edge of GPTC_GATE. After the software-start, every active GPTC_GATE edge triggers a single pulse with programmable delay and pulse-width. Any GPTC_GATE triggers that occur when the prior pulse is not completed would be ignored. Figure 4-28 illustrates the generation of two pulses with a pulse delay of two and a pulse-width of four.

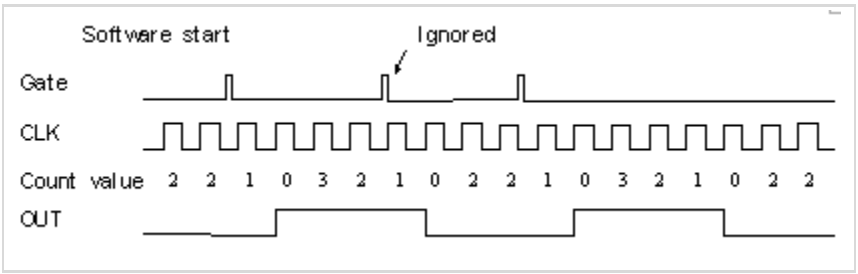


Figure 4-28: Mode6 Operation

Mode7: Single Triggered Continuous Pulse Generation

This mode is similar to Mode5 except that the counter generates continuous periodic pulses with programmable pulse interval and pulse-width following the first active edge of GPTC_GATE. Once the first GPTC_GATE edge triggers the counter, GPTC_GATE takes no effect until the software-start is re-executed. Figure 4-29 illustrates the generation of two pulses with a pulse delay of four and a pulse-width of three.

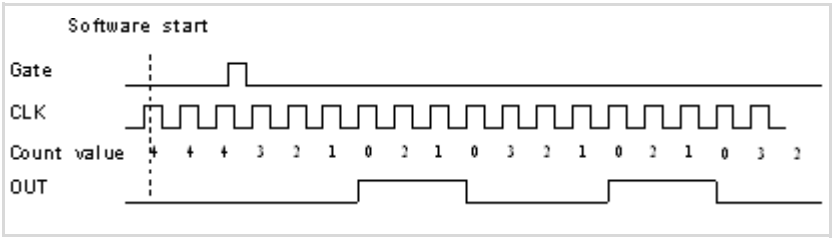


Figure 4-29: Mode7 Operation

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Mode8: Continuous Gated Pulse Generation

This mode generates periodic pulses with programmable pulse interval and pulse-width following the software-start. GPTC_GATE is used to enable/disable counting. When GPTC_GATE is inactive, the counter halts the current count value. Figure 4-30 illustrates the generation of two pulses with a pulse delay of four and a pulse-width of three.

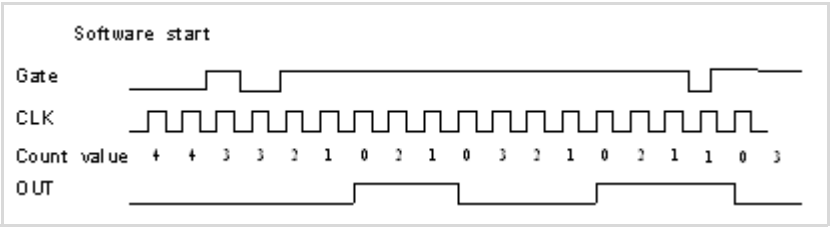


Figure 4-30: Mode8 Operation

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4.5 Trigger Sources

ADLINK provides flexible trigger selections in the DAQ/DAQe/PXI-2204/2205/2206/2208 card. In addition to the internal software trigger, the DAQ/DAQe/PXI-2204/2205/2206/2208 card also supports external analog, digital triggers, and SSI triggers. You can configure the trigger source by software for A/D and D/A processes individually. Note that the A/D and the D/A conversion share the same analog trigger.

4.5.1 Software-Trigger

This trigger mode does not need any external trigger source. The trigger asserts right after you execute the specified function calls to begin the operation. A/D and D/A processes can receive an individual software trigger.

4.5.2 External Analog Trigger

The analog trigger circuitry routing is shown in the Figure 4-31. The analog multiplexer can select either a direct analog input from the EXTATRIG pin (SRC1 in Figure 4-31) in the 68-pin connector or the input signal of ADC (SRC2 in Figure 4-31). That is, one of the four channel inputs you can select as a trigger source. Both trigger sources can be used for all trigger modes. The range of trigger level for SRC1 is ±10V and the resolution is 78mV (refer to Table 4-6), while the trigger range of SRC2 is the full-scale range of the selected channel input and the resolution is the desired range divided by 256. For example, if the channel input selected to be the trigger source is set bipolar and ±5V range, the trigger voltage would be 4.96V when the trigger level code is set to 0xFF while -4.96V when the code is set to 0x01.

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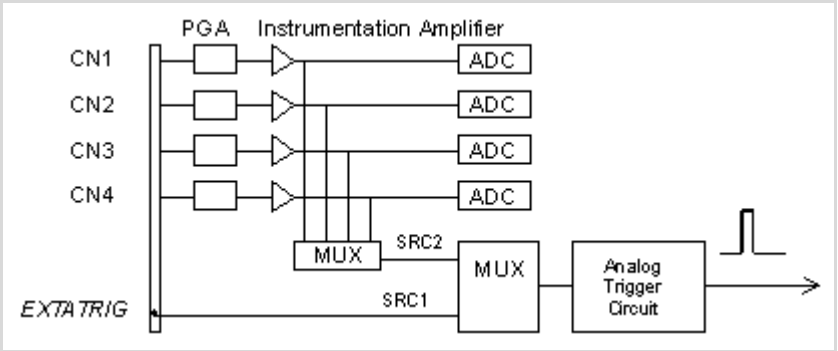


Figure 4-31: Analog Trigger Block Diagram

Trigger level digital setting	Trigger voltage
0xFF	9.92V
0xFE	9.84V
0x81	0.08V
0x80	0
0x7F	-0.08V
0x01	-9.92V

Table 4-7: Analog Trigger SRC1 (EXTATRIG) Ideal Transfer Characteristic

The trigger signal is generated when the analog trigger condition is satisfied. There are five analog trigger conditions in the DAQ/DAQe/PXI-2204/2205/2206/2208 card. The DAQ/DAQe/PXI-2204/2205/2206/2208 card uses two threshold voltages, Low_Threshold and High_Threshold to build the five different trigger conditions. You can configure the trigger conditions easily by software.

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Below-Low Analog Trigger Condition

Figure 4-32 shows the below-low analog trigger condition, the trigger signal is generated when the input analog signal is less than the Low_Threshold voltage, and the High_Threshold setting is not used in this trigger condition.

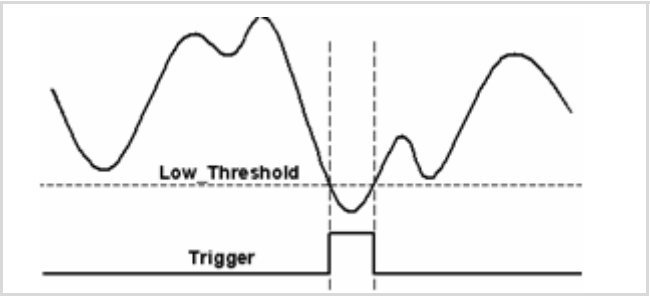


Figure 4-32: Below-Low Analog Trigger Condition

Above-High Analog Trigger Condition

Figure 4-33 shows the above-high analog trigger condition, the trigger signal is generated when the input analog signal is higher than the High_Threshold voltage, and the Low_Threshold setting is not used in this trigger condition.

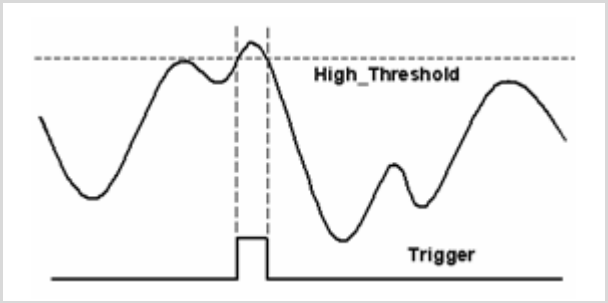


Figure 4-33: Above-High Analog Trigger Condition

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Inside-Region Analog Trigger Condition

Figure 4-34 shows the inside-region analog trigger condition, the trigger signal is generated when the input analog signal level falls in the range between the High_Threshold and the Low_Threshold voltages.

NOTE:

The High_Threshold setting should be always higher than the Low_Threshold voltage setting.

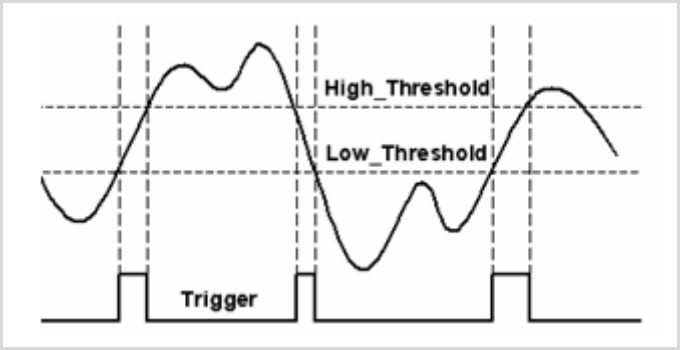


Figure 4-34: Inside-Region Analog Trigger Condition

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High-Hysteresis Analog Trigger Condition

Figure 4-35 shows the high-hysteresis analog trigger condition, the trigger signal is generated when the input analog signal level is greater than the High_Threshold voltage, and the Low_Threshold voltage determines the hysteresis duration. Note the High_Threshold setting should be always higher then the Low_Threshold voltage setting.

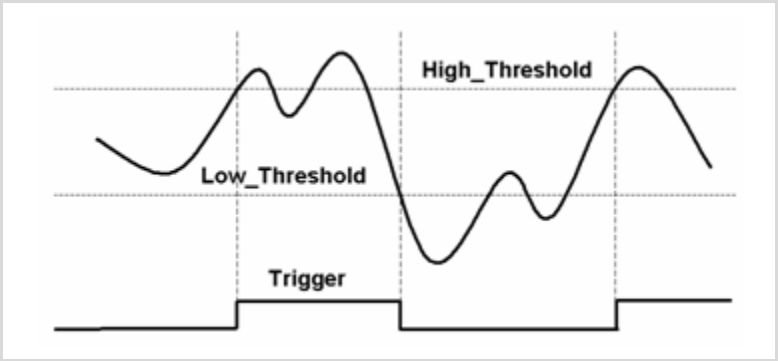


Figure 4-35: High-Hysteresis Analog Trigger Condition

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Low-Hysteresis Analog Trigger Condition

Figure 4-36 shows the low-hysteresis analog trigger condition, the trigger signal is generated when the input analog signal level is less than the Low_Threshold voltage, and the High_Threshold voltage determines the hysteresis duration. Note the High_Threshold setting should be always higher then the Low_Threshold voltage setting.

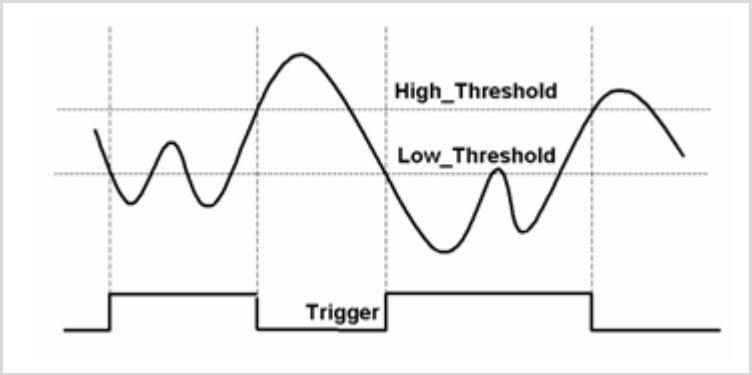


Figure 4-36: Low-Hysteresis Analog Trigger Condition

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External Digital Trigger

An external digital trigger occurs when a rising edge or a falling edge is detected on the digital signal connected to the EXTDTRIG or the EXTWFTRG of the 68-pin connector for external digital trigger. The EXTDTRIG is dedicated for A/D process, and the EXTWFTRG is used for D/A process. You can program the trigger polarity using the software drivers. Note that the signal level of the external digital trigger signals should be TTL-compatible and the minimum pulse is 20 ns.



Figure 4-37: External Digital Trigger

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4.6 User-controllable Timing Signals

In order to meet the requirements for user-specific timing and requirements for synchronizing multiple cards, the DAQ/DAQe/PXI-2204/2205/2206/2208 card provides flexible user-controllable timing signals to connect to external circuitry or additional cards.

The whole DAQ timing of the DAQ/DAQe/PXI-2204/2205/2206/2208 card is composed of a bunch of counters and trigger signals in the FPGA. These timing signals are related to the A/D, D/A conversions, and Timer/Counter applications. These timing signals can be input to or output from the I/O connectors, SSI connector, and the PXI bus. Therefore, the internal timing signals can be used to control external devices or circuitry. Note that in other models of DAQ/DAQe/PXI-2204/2205/2206/2208 card, the user-controllable timing signals may vary. However, the SSI/PXI timing signals remain the same for every DAQ/DAQe/PXI-2204/2205/2206/2208 card.

We implemented signal multiplexers in the FPGA to individually choose the desired timing signals for the DAQ operations, as shown in the Figure 4-38.

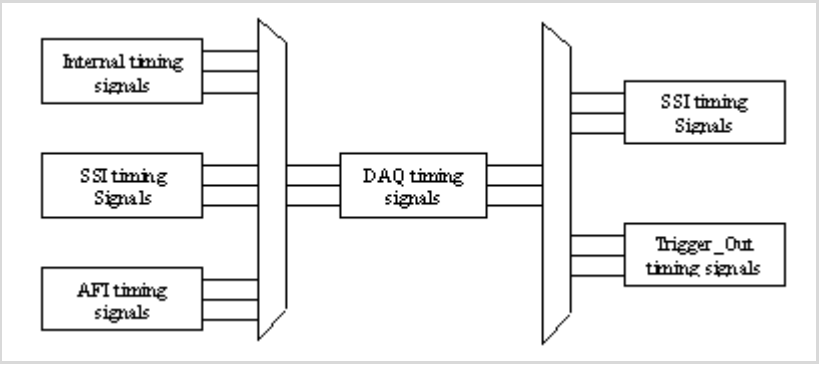


Figure 4-38: DAQ signals routing

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You can utilize the flexible timing signals through our software drivers, then simply and correctly connect the signals with the DAQ/DAQe/PXI-2204/2205/2206/2208 card. Here is the summary of the DAQ timing signals and the corresponding functionalities for DAQ/DAQe/PXI-2204/2205/2206/2208 card.

Timing signal category	Corresponding functionality
SSI/PXI signals	Multiple cards synchronization
AFI signals	Control DAQ/DAQe/PXI-2204/2205/2206/ 2208 by external timing signals

Table 4-8: User-controllable Timing Signals and Functionalities

4.6.1 DAQ timing signals



Refer to section 4.1 for the internal timing signal definition.

The DAQ/DAQe/PXI-2208 card supports SCAN_START, ADCONV and DA_TRIG, DAWR.

The user-controllable DAQ timing-signals contain:

1. TIMEBASE, providing TIMEBASE for all DAQ operations, which could be from internal 40 MHz oscillator, EXTTIMEBASE from I/O connector or the SSI_TIMEBASE. Note that the frequency range of the EXTTIMEBASE is 1 MHz to 40 MHz, and the EXTTIMEBASE must be TTL-compatible.
2. AD_TRIG, the trigger signal for the A/D operation, which could come from external digital trigger, analog trigger, internal software trigger, and SSI_AD_TRIG. Refer to section 4.5 for detailed description.
3. SCAN_START, the signal to start a scan, which would bring the following ADCONV signals for AD conversion, and could come from the internal SI_counter, AFI[0] and SSI_AD_START. This signal is synchronous to the TIMEBASE. Note that the AFI[0] should be TTL-compatible and the minimum pulse width should be the pulse width of the TIMEBASE to guarantee correct functionalities.

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4. ADCONV, the conversion signal to initiate a single conversion, which could be derived from internal counter, AFI[0] or SSI_ADCONV. Note that this signal is edge-sensitive. When using AFI[0] as the external ADCONV source, each rising edge of AFI[0] would bring an effective conversion signal. Also note that the AFI[0] signal should be TTL-compatible and the minimum pulse width is 20 ns.
5. DA_TRIG, the trigger signal for the D/A operation, which could be derived from external digital trigger, analog trigger, internal software trigger, and SSI_AD_TRIG. Refer to section 4.5 for detailed description.
6. DAWR, the update signal to initiate a single D/A conversion, which could be derived from internal counter, AFI[1] or SSI_DAWR. Note that this signal is edge-sensitive. When using AFI[1] as the external DAWR source, each rising edge of AFI[1] would bring an effective update signal. Also note that the AFI[1] signal should be TTL-compatible and the minimum pulse width is 20 ns.

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4.6.2 Auxiliary Function Inputs (AFI)

You can use the AFI in applications that take advantage of external circuitry to directly control the DAQ/DAQe/PXI-2204/2205/2206/2208 card. The AFI includes two categories of timing signals: one group is the dedicated input, and the other is the multi-function input. Table 4-9 illustrates this categorization.

Category	Timing signal	Functionality	Constraints
Dedicated input	EXTTIMEBASE	Replace the internal TIMEBASE	• TTL-compatible • 1 MHz to 40 MHz • Affects on both A/D and D/A operations.
	EXTDTRIG	External digital trigger input for A/D operation	• TTL-compatible • Minimum pulse width = 20ns • Rising edge or falling edge
	EXTWFTRG	External digital trigger input for D/A operation	• TTL-compatible • Minimum pulse width = 20ns • Rising edge or falling edge
Multi-function input	AFI[0] (Dual-functions)	Replace the internal ADCONV	• TTL-compatible • Minimum pulse width = 20ns • Rising–edge sensitive only
		Replace the internal SCAN_START	• TTL-compatible • Minimum Pulse width > 2/ TIMEBASE
	AFI[1]	Replace the internal DAWR	• TTL-compatible • Minimum pulse width = 20ns • Rising–edge sensitive only

Table 4-9: Auxiliary Function Input Signals and Functionalities

EXTDTRIG and EXTWFTRIG

EXTDTRIG and EXTWFTRIG are dedicated digital trigger input signals for A/D and D/A operations respectively. Refer to section 4.5 for details.

EXTTIMEBASE

When the applications needs specific sampling frequency or update rate that the card could not generate from its internal TIMEBASE — the 40 MHz clock — you could utilize the EXTTIMEBASE with internal counters to achieve the specific timing

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intervals for both A/D and D/A operations. Note that once you choose the TIMEBASE source, both A/D and D/A operations will be affected because A/D and D/A operations share the same TIMEBASE.

AFI[0]

Alternatively, you can also directly apply an external A/D conversion signal to replace the internal ADCONV signal. This is another way to achieve customized sampling frequencies. The external ADCONV signal can only be inputted from the AFI[0]. As section 4.1 describes, the SI_counter triggers the generation of the A/D conversion signal, ADCONV, but when using the AFI[0] to replace the internal ADCONV signal, the SI_counter and the internally generated SCAN_START is not effective. By controlling the ADCONV externally, you can sample the data according to external events. In this mode, the Trigger signal and trigger mode settings are not available.

AFI[0] could also be used as SCAN_START signal for A/D operations. Refer to section 4.1 and section 4.6 for detailed descriptions of the SCAN_START signal. When using external signal (AFI[0]) to replace the internal SCAN_START signal, the pulse width of the AFI[0] must be greater than two time of the period of Timebase. This feature is suitable for the DAQ-2200/DAQe-2200/PXI-2200 Series, which can scan multiple channels data controlled by an external event. Note that the AFI[0] is a multi-purpose input, and it can only be utilized for one function at any one time.

AFI[1]

Regarding the D/A operations, users could directly input the external D/A update signal to replace the internal DAWR signal. This is another way to achieve customized D/A update rates. The external DAWR signal can only be inputted from the AFI[1]. Note that the AFI[1] is a multi-purpose input, and it can only be utilized for one function at any one time. AFI[1] currently only has one function. ADLINK reserves it for future development.

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4.6.3 System Synchronization Interface

SSI (System Synchronization Interface) provides the DAQ timing synchronization between multiple cards. In DAQ/DAQe/PXI-2204/2205/2206/2208 card, we designed a bi-directional SSI I/O to provide flexible connection between cards and allow one SSI master to output the signal and up to three slaves to receive the SSI signal. Note that the SSI signals are designed for card synchronization only and not for external devices.

SSI Timing Signal	Setting	Function
SSI_TIMEBASE	Master	Send the TIMEBASE out
	Slave	Accept the SSI_TIMEBASE to replace the internal TIMEBASE signal.
SSI_ADCONV	Master	Send the ADCONV out
	Slave	Accept the SSI_ADCONV to replace the internal ADCONV signal.
SSI_SCAN_START	Master	Send the SCAN_START out
	Slave	Accept the SSI_SCAN_START to replace the internal SCAN_START signal.
SSI_AD_TRIG	Master	Send the internal AD_TRIG out
	Slave	Accept the SSI_AD_TRIG as the digital trigger signal.
SSI_DAWR	Master	Send the DAWR out.
	Slave	Accept the SSI_DAWR to replace the internal DAWR signal.
SSI_DA_TRIG	Master	Send the DA_TRIG out.
	Slave	Accept the SSI_DA_TRIG as the digital trigger signal.

Table 4-10: SSI Timing Signal and Functions

In PCI form factor, there is a connector on the top right corner of the card for the SSI. Refer to section 2.3 for the connector position. All the SSI signals are routed to the 20-pin connector from the FPGA. To synchronize multiple cards, users can connect a special ribbon cable (ACL-SSI) to all the cards in a daisy-chain configuration.

In PXI form factor, we utilize the PXI trigger bus built on the PXI backplane to provide the necessary timing signal connections. All the SSI signals are routed to the P2 connector. No additional cable

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is needed. For detailed information of the PXI specifications, refer to the PXI Specification Revision 2.0 from PXI System Alliance (www.pxisa.org).

The six internal timing signals could be routed to the SSI or the PXI trigger bus through software drivers. Refer to section 4.6 for detailed information on the six internal timing signals. Physically, the signal routings are accomplished in the FPGA. Cards that are connected together through the SSI or the PXI trigger bus, will still achieve synchronization on the six timing signals.

The SSI/PXI Mechanism

We adopt master-slave configuration for SSI/PXI. In a system, for each timing signal, there shall be only one master, and other cards are SSI slaves or with SSI function disabled.

For each timing signal, the SSI master does not have to be in a single card. For example:

We want to synchronize the A/D operation through the ADCONV signal for four DAQ/DAQe/PXI-2204/2205/2206/2208 cards. Card 1 is the master, and Card 2, 3, 4 are slaves. Card 1 receives an external digital trigger to start the post trigger mode acquisition. The SSI setting could be:

- Set the SSI_ADCONV signal of Card 1 to be the master.
- Set the SSI_ADCONV signals of Card 2, 3, 4 to be the slaves.
- Set external digital trigger for Card 1's A/D operation.
- Set the SI_counter and the post scan counter (PSC) of all other cards.
- Start DMA operations for all cards, so all the cards are waiting for the trigger event.

When the digital trigger condition of Card 1 occurs, Card 1 will internally generate the ADCONV signal and output this ADCONV signal to SSI_ADCONV signal of Card 2, 3 and 4 through the SSI/PXI connectors. Thus we can achieve 16-channel acquisition simultaneously.

You could arbitrarily choose each of the six timing signals as the SSI master from any one of the cards. The SSI master can

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output the internal timing signals to the SSI slaves. With the SSI, users could achieve better card-to-card synchronization.

Note that when power-up or reset, the DAQ timing signals are reset to use the internal generated timing signals.

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5 Calibration

This chapter introduces the calibration process to minimize AD measurement errors and DA output errors.

5.1 Loading Calibration Constants

The DAQ/DAQe/PXI-2204/2205/2206/2208 card is factory-calibrated before shipment. The associated calibration constants of the TrimDACs firmware to the onboard EEPROM. TrimDACs are devices containing multiple DACs within a single package. TrimDACs do not have memory capability. That means the calibration constants do not retain their values after the system power is turned off. Loading calibration constants is the process of loading the values of TrimDACs firmware stored in the onboard EEPROM. ADLINK provides a software utility that automatically reads the calibration constants automatically, if necessary.

There is a dedicated space for storing calibration constants in the EEPROM. In addition to the default bank of factory calibration constants, there is one user-utilization bank. This bank allows you to load the TrimDACs firmware values either from the original factory calibration or from a subsequently-performed calibration.

Because of the fact that measurements and outputs errors may vary depending on time and temperature, it is recommended that you calibrate the card when it is integrated in your computing environment. The auto-calibration function is presented in the following sections.

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5.2 Auto-calibration

Through the DAQ/DAQe/PXI-2204/2205/2206/2208 card auto-calibration feature, the calibration software measures and corrects almost all calibration errors without any external signal connections, reference voltage, or measurement devices.

The DAQ/DAQe/PXI-2204/2205/2206/2208 card comes with an onboard calibration reference to ensure the accuracy of auto-calibration. The reference voltage is measured in the production line through a digital potentiometer and compensated in the software. The calibration constant is memorized after this measurement. We do not recommended adjustment of the onboard calibration reference except when an ultra-precision calibrator is available.


NOTE:

- Warm the card up for at least 15 minutes before initiating auto-calibration.
- Remove the cable before auto-calibrating the card since the DA outputs are changed during the process.

5.3 Saving Calibration Constants

When auto-calibration is completed, you can save the new calibration constants to the user-configurable banks in the EEPROM. The date and the temperature when you ran auto-calibration is saved with the calibration constants. You can store three sets of calibration constants according to three different environments and re-load the calibration constants later.

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Important Safety Instructions

For user safety, please read and follow all instructions, Warnings, Cautions, and Notes marked in this manual and on the associated device before handling/operating the device, to avoid injury or damage.

S'il vous plaît prêter attention stricte à tous les avertissements et mises en garde figurant sur l'appareil , pour éviter des blessures ou des dommages.

- Read these safety instructions carefully.
- Keep the User's Manual for future reference.
- Read the Specifications section of this manual for detailed information on the recommended operating environment.
- The device can be operated at an ambient temperature of 50ºC.
- When installing/mounting or uninstalling/removing device, or when removal of a chassis cover is required for user servicing:
  - Turn off power and unplug any power cords/cables.
  - Reinstall all chassis covers before restoring power.
- To avoid electrical shock and/or damage to device:
  - Keep device away from water or liquid sources.
  - Keep device away from high heat or humidity.
  - Keep device properly ventilated (do not block or cover ventilation openings).
  - Always use recommended voltage and power source settings.
  - Always install and operate device near an easily accessible electrical outlet.
  - Secure the power cord (do not place any object on/over the power cord).
  - Only install/attach and operate device on stable surfaces and/or recommended mountings.
- If the device will not be used for long periods of time, turn off and unplug it from its power source
- Never attempt to repair the device, which should only be serviced by qualified technical personnel using suitable tools
- A Lithium-type battery may be provided for uninterrupted backup or emergency power.

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CAUTION:

Risk of explosion if battery is replaced with one of an incorrect type; please dispose of used batteries appropriately.
Risque d'explosion si la pile est remplacée par une autre de type incorrect. Veuillez jeter les piles usagées de façon appropriée.

- The device must be serviced by authorized technicians when:
  - The power cord or plug is damaged.
  - Liquid has entered the device interior.
  - The device has been exposed to high humidity and/or moisture.
  - The device is not functioning or does not function according to the User's Manual.
  - The device has been dropped and/or damaged and/or shows obvious signs of breakage.
- Disconnect the power supply cord before loosening the thumbscrews and always fasten the thumbscrews with a screwdriver before starting the system up.
- It is recommended that the device be installed only in a server room or computer room where access is:
  - Restricted to qualified service personnel or users familiar with restrictions applied to the location, reasons therefor, and any precautions required.
  - Only afforded by the use of a tool or lock and key, or other means of security, and controlled by the authority responsible for the location.



BURN HAZARD
Touching this surface could result in bodily injury. To reduce risk, allow the surface to cool before touching.

RISQUE DE BRÛLURES
Ne touchez pas cette surface, cela pourrait entraîner des blessures.
Pour éviter tout danger, laissez la surface refroidir avant de la toucher.

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