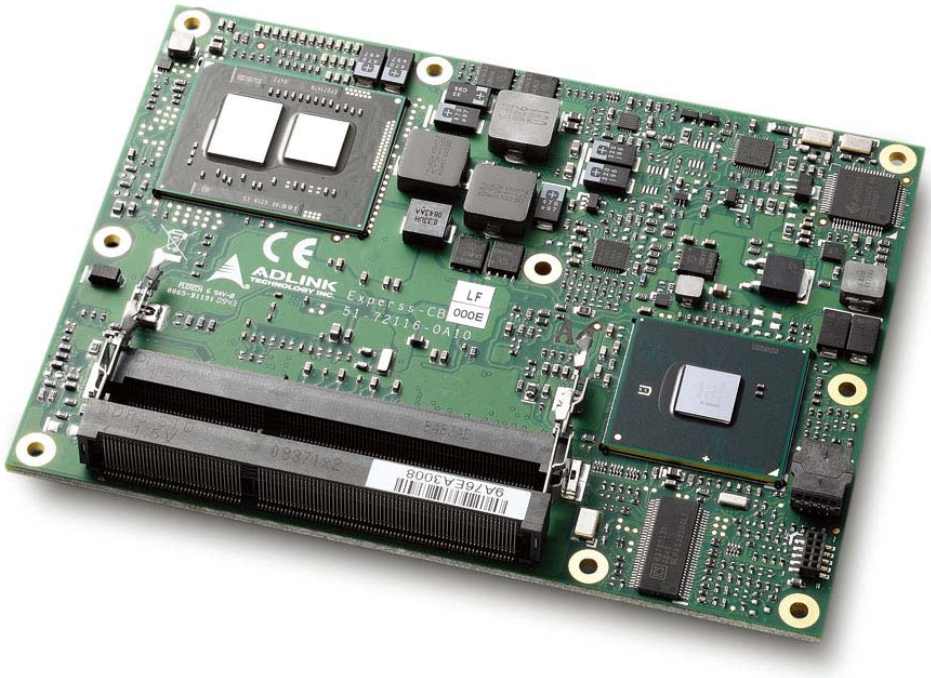
COM Express

Express-CB / CBE



Manual Revision: 2.02

Revision Date: September 7, 2012

Part Number: 50-1J033-1010

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ADLINK TECHNOLOGY INC.

Revision History

Release	Date	Change
2.00	Nov. 26, 2010	Initial Release
2.01	Feb. 22, 2011	Update pinouts, add content for Express-CBE
2.02	Sept. 7, 2012	Add PCI Express x16 Configuration switch SWY1; remove VGA hotplug feature

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Preface

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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.



Additional information, aids, and tips that help users perform tasks.



Information to prevent ***mino***r physical injury, component damage, data loss, and/or program corruption when trying to complete a task.



Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

1.1 Description

The Express-CB and Express-CBE are COM Express™ COM.0 R1.0 Type 2 modules supporting the 64-bit Intel® Core™ i7/i5 processor with CPU, memory controller, and graphics processor on the same chip. Based on the latest Mobile Intel® QM57 Express chipset, the Express-CB is specifically designed for customers who need high-level processing and graphics performance in a long product life solution.

The Express-CB features the Intel® Core™ i7/i5 processor supporting Intel® Hyper-threading Technology (2 cores, 4 threads) and up to 8GB of DDR3 dual-channel memory at 1066 MHz (EEC on Express-CBE) to provide excellent overall performance. Intel® Flexible Display Interface and Direct Media Interface provide high speed connectivity to the Intel® QM57 Express chipset.

Integrated graphics includes features such as OpenGL 2.1, DirectX10, and Intel® Dynamic Video Memory Technology (Intel® DVMT 5.0). Graphics outputs include VGA, LVDS and Embedded DisplayPort. The Express-CB is specifically designed for customers with high-performance processing graphics requirements who want to outsource the custom core logic of their systems for reduced development time.

The Express-CB has dual stacked SODIMM sockets for up to 8 GB DDR3 memory. The Intel® Mobile QM57 Express chipset integrates VGA and single/dual-channel 18/24-bit LVDS display output. In addition to the onboard integrated graphics, a multiplexed PCI Express® x16 Graphics bus is available for discrete graphics expansion, Embedded DisplayPort, or general purpose x8, x4 or x1 PCI Express® connectivity.

The Express-CB features a single onboard Gigabit Ethernet port, up to eight USB 2.0 ports and four SATA 3 Gb/s ports with optional support for RAID 0/1/5/10. Additional storage interfaces include an optional SATA based Solid State Disk (8/16/32 GB), and a single IDE (PATA) channel. Legacy support is also provided for 32-bit PCI, LPC, SMBus and I^2C. The module is equipped with an AMI EFI BIOS with CMOS backup, supporting embedded features such as remote console, CMOS backup, hardware monitor, and watchdog timer.

The Express-CB is a RoHS compliant and lead-free product.

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2 Specifications

2.1 General

- **CPU:** **Penryn Core PGA type**
  Intel® Core™ i7-610E Processor (4M Cache, 2.53 GHz) 35 W
  Intel® Core™ i5-520E Processor (3M Cache, 2.40 GHz) 35 W
  Intel® Core™ i7-620LE Processor (4M Cache, 2.00 GHz) 25 W
  Intel® Core™ i7-620UE Processor (4M Cache, 1.06 GHz) 18 W
  Intel® Celeron® Processor P4500 (2M Cache, 1.86 GHz) 35 W
- **Memory:** Dual stacked SODIMM socket memory supporting dual channel memory bandwidth, max. 8 GB of 800/1066 MHz DDR3 (ECC on Express-CBE)
- **Chipset:** Mobile Intel® QM57 Express
- **L2 Cache:** 2 MB (Celeron® M), 4/3 MB (Intel® Core™ i7/i5)
- **BIOS:** AMI EFI with CMOS backup in 16 Mbit SPI BIOS
- **Hardware Monitor:** Supply voltages and CPU temperature
- **Watchdog Timer:** Programmable timer ranges to generate RESET

2.2 Expansion Busses

- **On Processor:**
  - PCI Express x16 Graphics bus for discrete graphics solution or General Purpose PCI Express (2 x8, 2 x4, or 2 x1) or **Embedded Display Port** (eDP, see below)
- **On Chipset:**
  - 7 PCI Express x1: 0/1/2/3/4/5 are free, 6 is occupied by GbE LAN can be optionally configured as 1 x4 (on 0/1/2/3) and 2 x1 (4/5)
  - 32-bit PCI: PCI ver. 2.3 at 33MHz, supporting 4 bus masters
  - LPC bus: for optional connections to SIO, UART etc
- **SMBus** (system), **I²C** (user)

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2.3 Video

- **Core:** Gen 5.75 with 12 execution units
- **Integrated Graphics Features:**

  - DirectX 10 and OpenGL 2.1
  - Intel® Dynamic Video Memory Technology (Intel® DVMT 5.0)
  - Video capture via concurrent PCI Express x1 port
  - PAVP (Protected Audio-Video Path) support for Protected Intel® HD Audio Playback
  - High performance MPEG-2 decoding
  - WMV9 (VC-1) and H.264 (AVC) support
  - Hardware acceleration for MPEG2 VLD/iDCT
  - Blu-ray support @ 40 Mb/s
  - Hardware motion compensation
  - Intermediate Z in classic rendering

- **VGA Interface:** Analog VGA support up to QXGA, 300MHz DAC
- **LVDS Interface:** Single or dual channel 18/24-bit at 25~112 MHz
- **Embedded DisplayPort:** One data pair supporting XGA (1024x768) over two wires or two data pairs supporting SXGA (1280x1024) over four wires (see Note below).



Embedded DisplayPort (eDP)
DisplayPort is a VESA interface standard for digital display. It defines a new license-free, royalty-free, state-of-the-art digital audio/video interconnect, intended to be used primarily between a computer and its display monitor, or a computer and a home-theater system. It features 1.62 Gb/s and 2.7 Gb/s transfer rates over 1, 2 or 4 data lanes, 8b 10b coding, Hot-Plug detect support and HDCP support. Embedded DisplayPort does not offer all features of standard DisplayPort because embedded applications do not require features such as link training, hot plug detection or logo testing. The eDP standard supports one data pair supporting XGA (1024x768) over two wires. Optionally 4 wires can be used for two data pairs to support 1280x1024.

2.4 Audio

- **Chipset:** Integrated in Intel® I/O Controller Hub 9 Mobile (ICH9M)
- **Audio Codec:** on carrier (ALC888)

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2.5 LAN

- **Chipset**: Integrated in Intel® QM57 with Intel® 82577 PHY
- **Interface:** 10/100/1000 Mbps Ethernet operates in full-duplex at all supported speeds or half-duplex at 10/100 Mbps; adheres to the IEEE 802.3x Flow Control Specification

2.6 Multi I/O

- **PATA:** SATA-to-PATA JM20330 controller on SATA channel 0, Master only
- **SATA**: Four ports SATA 3 Gb/s (2, 3, 4, 5)
- **USB**: Supports up to eight ports USB 2.0

2.7 Super I/O

- Connected to LPC bus on carrier if needed

2.8 TPM (Trusted Platform Module)

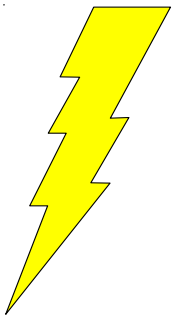
- **Chipset**: Infineon SLB9635TT1.2
- **Type:** TPM 1.2

2.9 Power Specifications

- **Input Power:** AT mode (12 V +/- 5%) and ATX mode (12 V and 5 Vsb +/- 5%)
- **Power States:** supporting S0, S1, S3, S4, S5
- **Smart Battery Support:** yes

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2.10 Power Consumption



The 12V measurement is power to the module only (excluding carrier board power draw). The 5Vsb measurement (in S3/S5 mode) includes both module power consumption plus active 5Vsb powered peripherals (such as PS/2 and USB) on the carrier that are needed for wakeup. Although all voltages were measured, only 12 V and 5 VSB are relevant because they are the only ones used by the Express module. The *Idle* power level was measured under Windows XP with no applications running (login screen). *Max Load* was measured under Windows XP running BurnIn software. Measurements were made with two 1GB 1066 MHz DDR3 SODIMM memory modules installed.

Intel® Core™ i7-620UE, 1.06 GHz

Power State	+12V	$+5V_{SB}$	Power Consumption
Idle (Windows XP login)	0.70 A	N.S.	8.4 W
Max. Load (Windows XP - BurnIn)	2.30 A	N.S.	27.6 W
S1 (standby powered on)	0.97 A	N.S.	11.6 W
S3 (suspend to RAM)	-	0.28 A	1.4 W
S5 (soft off)	-	0.18 A	0.9 W

Intel® Core™ i7-620LE, 2.00 GHz

Power State	+12V	$+5V_{SB}$	Power Consumption
Idle (Windows XP login)	0.74 A	N.S.	8.9 W
Max. Load (Windows XP - BurnIn)	3.01 A	N.S.	36.1 W
S1 (standby powered on)	1.08 A	N.S.	13.0 W
S3 (suspend to RAM)	-	0.29 A	1.5 W
S5 (soft off)	-	0.17 A	0.9 W

Intel® Core™ i7-520E, 2.40 GHz

Power State	+12V	$+5V_{SB}$	Power Consumption
Idle (Windows XP login)	0.74 A	N.S.	8.9 W
Max. Load (Windows XP - BurnIn)	3.30 A	N.S.	39.6 W
S1 (standby powered on)	1.06 A	N.S.	12.7 W
S3 (suspend to RAM)	-	0.29 A	1.5 W
S5 (soft off)	-	0.18 A	0.9 W

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Power Consumption (cont'd)

Intel® Core™ i7-610E, 2.40 GHz

Power State	+12V	$+5V_{SB}$	Power Consumption
Idle (Windows XP login)	0.76 A	N.S.	9.1 W
Max. Load (Windows XP - BurnIn)	3.10 A	N.S.	37.2 W
S1 (standby powered on)	1.13 A	N.S.	13.6 W
S3 (suspend to RAM)	-	0.28 A	1.4 W
S5 (soft off)	-	0.17 A	0.9 W

CMOS Battery Power Consumption

Current (+3V)	Power
3.2 µA	0.0000096 W

2.11 Operating Systems

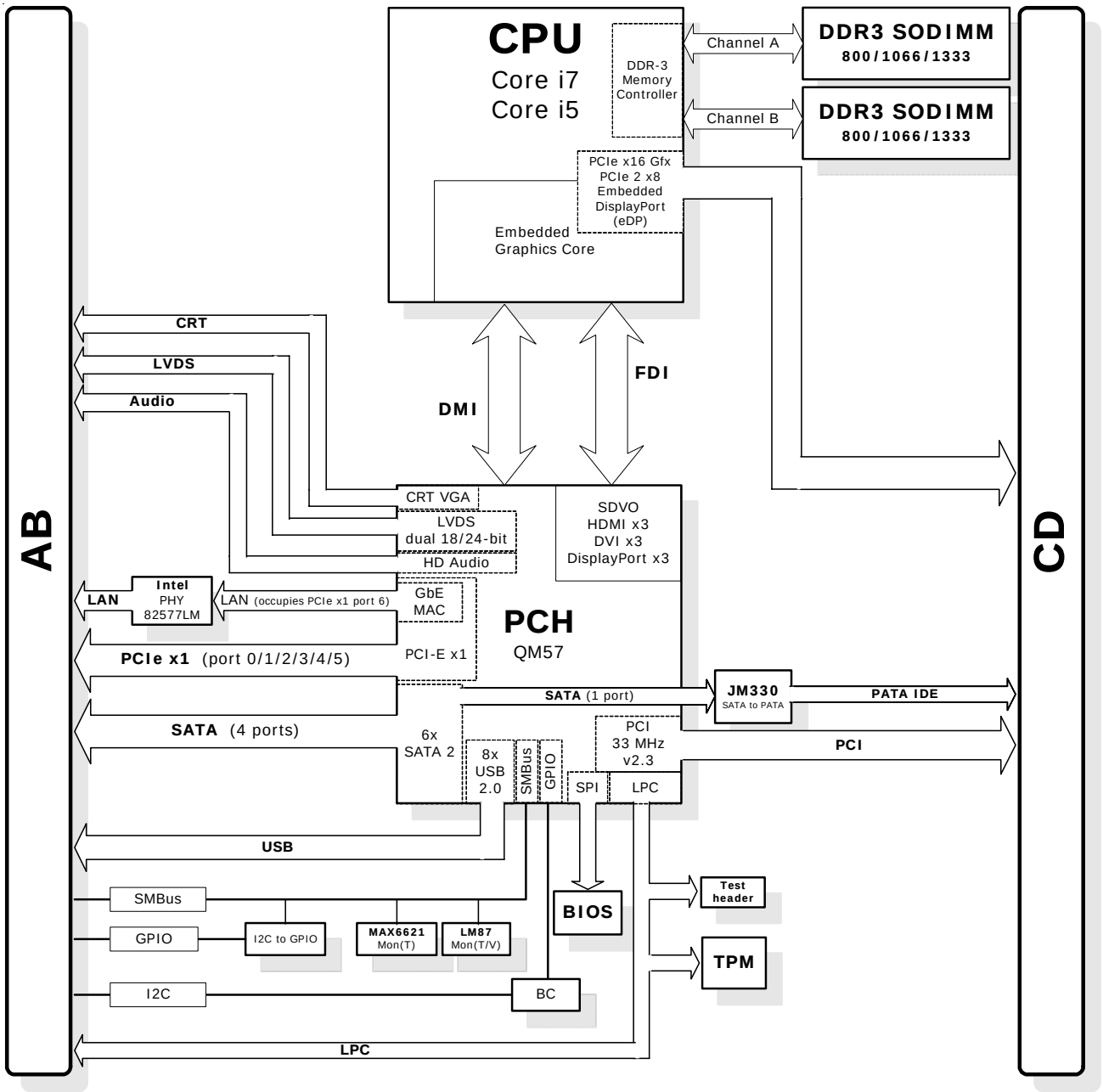
- **Standard Support**
  - Windows XP 32/64-bit
  - Windows Vista 32/64-bit
  - Windows Server 2003/2008
- **Extended Support (BSP)**
  - Embedded XP BSP
  - WinCE 6.0 BSP
  - AIDI I2C Library for Win32, WinCE and Linux

2.12 Mechanical and Environmental

- **Form Factor and Type:** PICMG COM.0, COM Express™ Basic form factor
- **Compatibility:** PICMG COM.0 R1, Type 2 pinout
- **Dimensions:** 95 x 125 mm
- **Standard Operating Temperature:** 0°C to 60°C
- **Relative Humidity:** up to 90% at 60°C

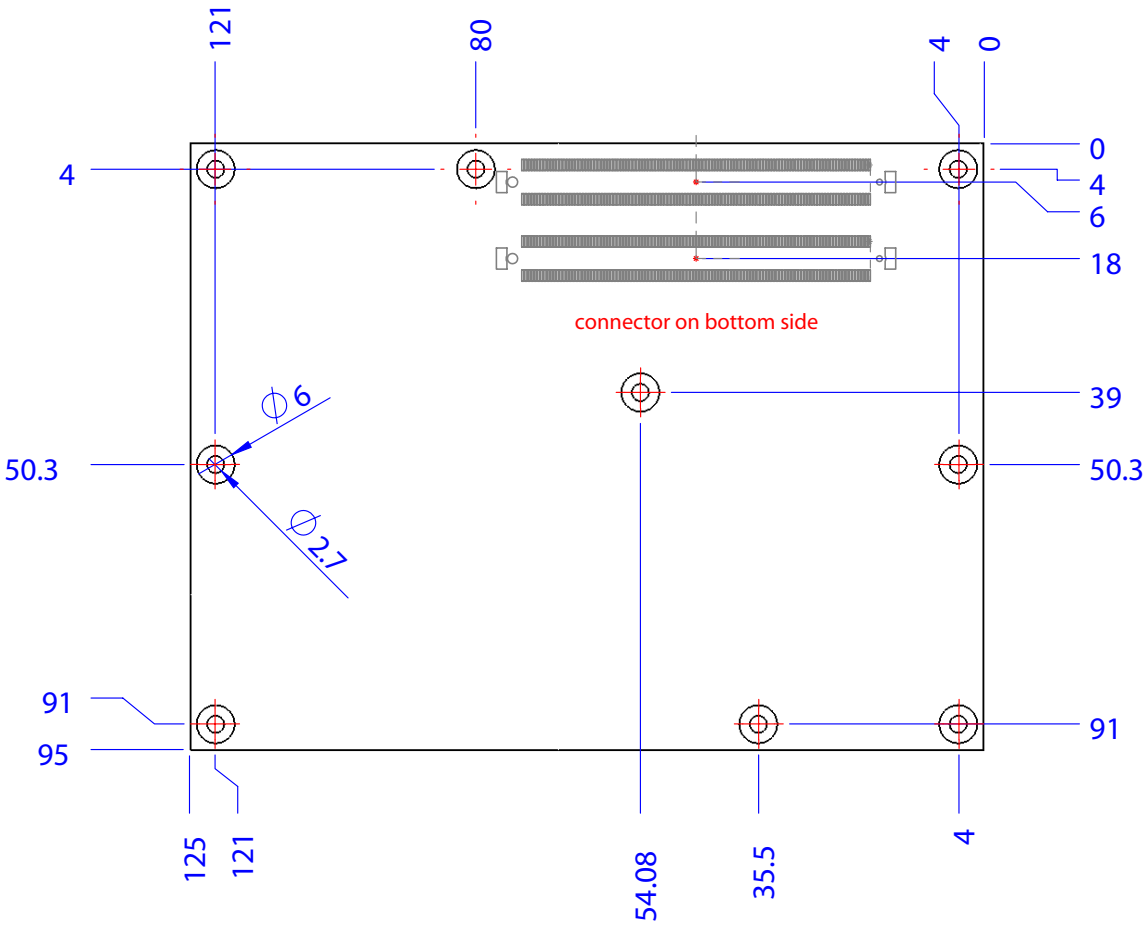
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3 Function Diagram



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4 Mechanical Dimensions



TOP VIEW

All Ø tolerances ± 0.05 mm
Other tolerances ± 0.2 mm

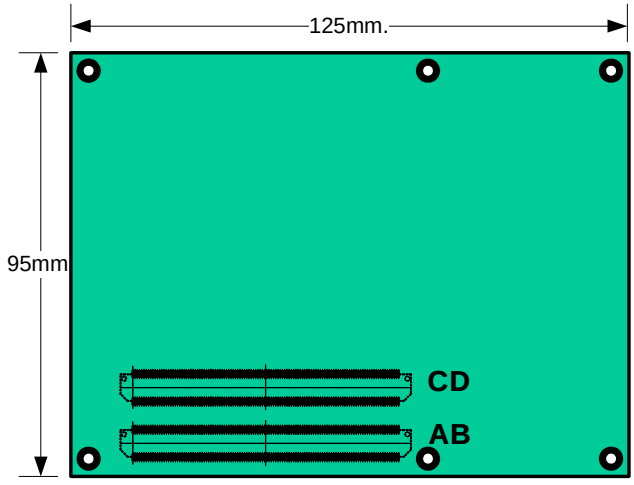
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5 Pinout, Signal and Switch Descriptions

5.1 COM Express® Type 2 compatible pinout

All signals on AB and CD connectors of the Express-CB comply with pinouts and conventions used in the original "**PICMG® COM.0 R1.0: COM Express® Module Base Specification"**.

AB Connector
1 Gigabit Ethernet port
LPC interface
4 Serial ATA channels
High Definition Audio
8 USB 2.0 ports
5 PCI Express Lanes x1
Dual 24-bit LVDS channels
Analog VGA
8 GPIO pins
SMBus and I^2C bus
+12V primary power input
+5V standby and 3V RTC

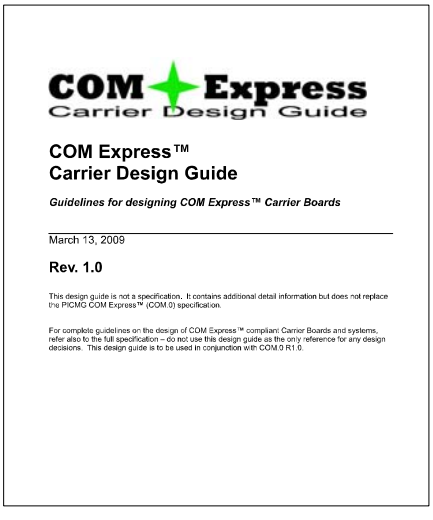


CD Connector
Parallel ATA, IDE port alternate definition assigns this to 2 additional Gigabit Ethernet ports
32-bit PCI v2.3 bus alternate definition assigns this to 10 additional PCI Express x1 lanes
PCI Express x16 for Graphics these pins can also be assigned to two SDVO extensions (multiplexed)
Power / Thermal control
+12V primary power input

NOTE: The above function mappings are a generic description of COM Express pinouts, and not necessarily supported on the module described in this manual.

5.2 Carrier Board Design Guide

The PICMG COM Express Carrier Design Guide is a 160-page document that provides information on designing a custom carrier board for COM Express modules. The design guide includes reference schematics for the external circuitry required to implement the various COM Express peripheral functions, explains how to extend the supported buses, and how to add additional peripherals and expansion slots to a COM Express-based system. You can download the document Carrier Design Guide at: http://www.adlinktech.com/ccps/picmg_comdg_100.pdf


COM Express
Carrier Design Guide

COM Express™
Carrier Design Guide

Guidelines for designing COM Express™ Carrier Boards

March 13, 2009

Rev. 1.0

This design guide is not a specification. It contains additional detail information but does not replace the PICMG COM Express™ (COM.0) specification.

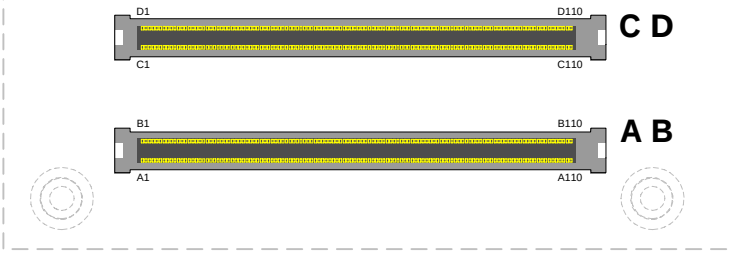
For complete guidelines on the design of COM Express™ compliant Carrier Boards and systems, refer also to the full specification – do not use this design guide as the only reference for any design decisions. This design guide is to be used in conjunction with COM.0 R1.0.

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5.3 Pin Definitions

Pinouts for:

COM.0 R1.0 Type 2



Row A			Row B	
Pin No.	Pin Name		Pin No.	Pin Name
A1	GND (FIXED)		B1	GND (FIXED)
A2	GBE0_MDI3-		B2	GBE0_ACT#
A3	GBE0_MDI3+		B3	LPC_FRAME#
A4	GBE0_LINK100#		B4	LPC_AD0
A5	GBE0_LINK1000#		B5	LPC_AD1
A6	GBE0_MDI2-		B6	LPC_AD2
A7	GBE0_MDI2+		B7	LPC_AD3
A8	GBE0_LINK#		B8	LPC_DRQ0#
A9	GBE0_MDI1-		B9	LPC_DRQ1#
A10	GBE0_MDI1+		B10	LPC_CLK
A11	GND (FIXED)		B11	GND (FIXED)
A12	GBE0_MDI0-		B12	PWRBTN#
A13	GBE0_MDI0+		B13	SMB_CK
A14	GBE0_CTREF		B14	SMB_DAT
A15	SUS_S3#		B15	SMB_ALERT#
A16	SATA0_TX+		B16	SATA1_TX+
A17	SATA0_TX-		B17	SATA1_TX-
A18	SUS_S4#		B18	SUS_STAT#
A19	SATA0_RX+		B19	SATA1_RX+
A20	SATA0_RX-		B20	SATA1_RX-
A21	GND (FIXED)		B21	GND (FIXED)
A22	SATA2_TX+		B22	SATA3_TX+
A23	SATA2_TX-		B23	SATA3_TX-
A24	SUS_S5#		B24	PWR_OK
A25	SATA2_RX+		B25	SATA3_RX+
A26	SATA2_RX-		B26	SATA3_RX-
A27	BATLOW#		B27	WDT
A28	ATA_ACT#		B28	AC_SDIN2
A29	AC_SYNC		B29	AC_SDIN1
A30	AC_RST#		B30	AC_SDIN0
A31	GND (FIXED)		B31	GND (FIXED)
A32	AC_BITCLK		B32	SPKR
A33	AC_SDOUT		B33	I2C_CK
A34	BIOS_DISABLE#		B34	I2C_DAT
A35	THRMTRIP#		B35	THRM#
A36	USB6-		B36	USB7-
A37	USB6+		B37	USB7+
A38	USB_6_7_OC#		B38	USB_4_5_OC#
A39	USB4-		B39	USB5-
A40	USB4+		B40	USB5+
A41	GND (FIXED)		B41	GND (FIXED)
A42	USB2-		B42	USB3-
A43	USB2+		B43	USB3+
A44	USB_2_3_OC#		B44	USB_0_1_OC#
A45	USB0-		B45	USB1-
A46	USB0+		B46	USB1+
A47	VCC_RTC		B47	EXCD1_PERST#
A48	EXCD0_PERST#		B48	EXCD1_CPPE#
A49	EXCD0_CPPE#		B49	SYS_RESET#
A50	LPC_SERIRQ		B50	CB_RESET#

Row C			Row D	
Pin No.	Pin Name		Pin No.	Pin Name
C1	GND FIXED)		D1	GND FIXED)
C2	IDE_D7		D2	IDE_D5
C3	IDE_D6		D3	IDE_D10
C4	IDE_D3		D4	IDE_D11
C5	IDE_D15		D5	IDE_D12
C6	IDE_D8		D6	IDE_D4
C7	IDE_D9		D7	IDE_D0
C8	IDE_D2		D8	IDE_REQ
C9	IDE_D13		D9	IDE_IOW#
C10	IDE_D1		D10	IDE_ACK#
C11	GND (FIXED)		D11	GND (FIXED)
C12	IDE_D14		D12	IDE_IRQ
C13	IDE_IORDY		D13	IDE_A0
C14	IDE_IOR#		D14	IDE_A1
C15	PCI_PME#		D15	IDE_A2
C16	PCI_GNT2#		D16	IDE_CS1#
C17	PCI_REQ2#		D17	IDE_CS3#
C18	PCI_GNT1#		D18	IDE_RESET#
C19	PCI_REQ1#		D19	PCI_GNT3#
C20	PCI_GNT0#		D20	PCI_REQ3#
C21	GND (FIXED)		D21	GND (FIXED)
C22	PCI_REQ0#		D22	PCI_AD1
C23	PCI_RESET#		D23	PCI_AD3
C24	PCI_AD0		D24	PCI_AD5
C25	PCI_AD2		D25	PCI_AD7
C26	PCI_AD4		D26	PCI_C/BE0#
C27	PCI_AD6		D27	PCI_AD9
C28	PCI_AD8		D28	PCI_AD11
C29	PCI_AD10		D29	PCI_AD13
C30	PCI_AD12		D30	PCI_AD15
C31	GND (FIXED)		D31	GND (FIXED)
C32	PCI_AD14		D32	PCI_PAR
C33	PCI_C/BE1#		D33	PCI_SERR#
C34	PCI_PERR#		D34	PCI_STOP#
C35	PCI_LOCK#		D35	PCI_TRDY#
C36	PCI_DEVSEL#		D36	PCI_FRAME#
C37	PCI_IRDY#		D37	PCI_AD16
C38	PCI_C/BE2#		D38	PCI_AD18
C39	PCI_AD17		D39	PCI_AD20
C40	PCI_AD19		D40	PCI_AD22
C41	GND (FIXED)		D41	GND (FIXED)
C42	PCI_AD21		D42	PCI_AD24
C43	PCI_AD23		D43	PCI_AD26
C44	PCI_C/BE3#		D44	PCI_AD28
C45	PCI_AD25		D45	PCI_AD30
C46	PCI_AD27		D46	PCI_IRQC#
C47	PCI_AD29		D47	PCI_IRQD#
C48	PCI_AD31		D48	PCI_CLKRUN#
C49	PCI_IRQA#		D49	PCI_M66EN (GND)
C50	PCI_IRQB#		D50	PCI_CLK

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Row A			Row B	
Pin No.	Pin Name		Pin No.	Pin Name
A51	GND (FIXED)		B51	GND (FIXED)
A52	PCIE_TX5+		B52	PCIE_RX5+
A53	PCIE_TX5-		B53	PCIE_RX5-
A54	GPI0		B54	GPO1
A55	PCIE_TX4+		B55	PCIE_RX4+
A56	PCIE_TX4-		B56	PCIE_RX4-
A57	GND		B57	GPO2
A58	PCIE_TX3+		B58	PCIE_RX3+
A59	PCIE_TX3-		B59	PCIE_RX3-
A60	GND (FIXED)		B60	GND (FIXED)
A61	PCIE_TX2+		B61	PCIE_RX2+
A62	PCIE_TX2-		B62	PCIE_RX2-
A63	GPI1		B63	GPO3
A64	PCIE_TX1+		B64	PCIE_RX1+
A65	PCIE_TX1-		B65	PCIE_RX1-
A66	GND		B66	WAKE0#
A67	GPI2		B67	WAKE1#
A68	PCIE_TX0+		B68	PCIE_RX0+
A69	PCIE_TX0-		B69	PCIE_RX0-
A70	GND (FIXED)		B70	GND (FIXED)
A71	LVDS_A0+		B71	LVDS_B0+
A72	LVDS_A0-		B72	LVDS_B0-
A73	LVDS_A1+		B73	LVDS_B1+
A74	LVDS_A1-		B74	LVDS_B1-
A75	LVDS_A2+		B75	LVDS_B2+
A76	LVDS_A2-		B76	LVDS_B2-
A77	LVDS_VDD_EN		B77	LVDS_B3+
A78	LVDS_A3+		B78	LVDS_B3-
A79	LVDS_A3-		B79	LVDS_BKLT_EN
A80	GND (FIXED)		B80	GND (FIXED)
A81	LVDS_A_CK+		B81	LVDS_B_CK+
A82	LVDS_A_CK-		B82	LVDS_B_CK-
A83	LVDS_I2C_CK		B83	LVDS_BKLT_CTRL
A84	LVDS_I2C_DAT		B84	VCC_5V_SBY
A85	GPI3		B85	VCC_5V_SBY
A86	KBD_RST#		B86	VCC_5V_SBY
A87	KBD_A20GATE		B87	VCC_5V_SBY
A88	PCIE0_CK_REF+		B88	RSVD
A89	PCIE0_CK_REF-		B89	VGA_RED
A90	GND (FIXED)		B90	GND (FIXED)
A91	RSVD		B91	VGA_GRN
A92	RSVD		B92	VGA_BLU
A93	GPO0		B93	VGA_HSYNC
A94	RSVD		B94	VGA_VSYNC
A95	RSVD		B95	VGA_I2C_CK
A96	GND		B96	VGA_I2C_DAT
A97	VCC_12V		B97	~~TV_DAC_A~~
A98	VCC_12V		B98	~~TV_DAC_B~~
A99	VCC_12V		B99	~~TV_DAC_C~~
A100	GND (FIXED)		B100	GND (FIXED)
A101	VCC_12V		B101	VCC_12V
A102	VCC_12V		B102	VCC_12V
A103	VCC_12V		B103	VCC_12V
A104	VCC_12V		B104	VCC_12V
A105	VCC_12V		B105	VCC_12V
A106	VCC_12V		B106	VCC_12V
A107	VCC_12V		B107	VCC_12V
A108	VCC_12V		B108	VCC_12V
A109	VCC_12V		B109	VCC_12V
A110	GND (FIXED)		B110	GND (FIXED)

Row C			Row D	
Pin No.	Pin Name		Pin No.	Pin Name
C51	GND (FIXED)		D51	GND (FIXED)
C52	PEG_RX0+		D52	PEG_TX0+
C53	PEG_RX0-		D53	PEG_TX0-
C54	TYPE0#		D54	PEG_LANE_RV#
C55	PEG_RX1+		D55	PEG_TX1+
C56	PEG_RX1-		D56	PEG_TX1-
C57	TYPE1#		D57	TYPE2#
C58	PEG_RX2+		D58	PEG_TX2+
C59	PEG_RX2-		D59	PEG_TX2-
C60	GND (FIXED)		D60	GND (FIXED)
C61	PEG_RX3+		D61	PEG_TX3+
C62	PEG_RX3-		D62	PEG_TX3-
C63	RSVD		D63	RSVD
C64	RSVD		D64	RSVD
C65	PEG_RX4+		D65	PEG_TX4+
C66	PEG_RX4-		D66	PEG_TX4-
C67	RSVD		D67	GND
C68	PEG_RX5+		D68	PEG_TX5+
C69	PEG_RX5-		D69	PEG_TX5-
C70	GND (FIXED)		D70	GND (FIXED)
C71	PEG_RX6+		D71	PEG_TX6+
C72	PEG_RX6-		D72	PEG_TX6-
C73	~~SDVO_DATA~~		D73	~~SDVO_CLK~~
C74	PEG_RX7+		D74	PEG_TX7+
C75	PEG_RX7-		D75	PEG_TX7-
C76	GND		D76	GND
C77	RSVD		D77	IDE_CBLID#
C78	PEG_RX8+		D78	PEG_TX8+
C79	PEG_RX8-		D79	PEG_TX8-
C80	GND (FIXED)		D80	GND (FIXED)
C81	PEG_RX9+		D81	PEG_TX9+
C82	PEG_RX9-		D82	PEG_TX9-
C83	RSVD		D83	RSVD
C84	GND		D84	GND
C85	PEG_RX10+		D85	PEG_TX10+
C86	PEG_RX10-		D86	PEG_TX10-
C87	GND		D87	GND
C88	PEG_RX11+		D88	PEG_TX11+
C89	PEG_RX11-		D89	PEG_TX11-
C90	GND (FIXED)		D90	GND (FIXED)
C91	PEG_RX12+		D91	PEG_TX12+
C92	PEG_RX12-		D92	PEG_TX12-
C93	GND		D93	GND
C94	PEG_RX13+		D94	PEG_TX13+
C95	PEG_RX13-		D95	PEG_TX13-
C96	GND		D96	GND
C97	RSVD		D97	PEG_ENABLE#
C98	PEG_RX14+		D98	PEG_TX14+
C99	PEG_RX14-		D99	PEG_TX14-
C100	GND (FIXED)		D100	GND (FIXED)
C101	PEG_RX15+		D101	PEG_TX15+
C102	PEG_RX15-		D102	PEG_TX15-
C103	GND		D103	GND
C104	VCC_12V		D104	VCC_12V
C105	VCC_12V		D105	VCC_12V
C106	VCC_12V		D106	VCC_12V
C107	VCC_12V		D107	VCC_12V
C108	VCC_12V		D108	VCC_12V
C109	VCC_12V		D109	VCC_12V
C110	GND (FIXED)		D110	GND (FIXED)

~~XXX~~ Strikethrough pin names indicates that the signal is not supported on this module.

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5.4 Signal Descriptions

Row A

Pin	Signal	Description	Type	PU/PD	Comment
A1	GND	Ground	PWR	-	-
A2	GBE0_MDI3-	Ethernet Media Dependent Interface -	I/O - DP	-	-
A3	GBE0_MDI3+	Ethernet Media Dependent Interface +	I/O - DP	-	-
A4	GBE0_LINK100#	Ethernet Speed LED (100Mb)	OD	-	On at 100Mb/s
A5	GBE0_LINK1000#	Ethernet Speed LED (1000Mb)	OD	-	On at 1000Mb/s
A6	GBE0_MDI2-	Ethernet Media Dependent Interface -	I/O - DP	-	-
A7	GBE0_MDI2+	Ethernet Media Dependent Interface +	I/O - DP	-	-
A8	GBE0_LINK#	LAN Link LED	O-3.3		-
A9	GBE0_MDI1-	Ethernet Media Dependent Interface -	I/O - DP	-	-
A10	GBE0_MDI1+	Ethernet Media Dependent Interface +	I/O - DP	-	-
A11	GND	Ground	PWR	-	-
A12	GBE0_MDI0-	Ethernet Media Dependent Interface -	I/O - DP	-	-
A13	GBE0_MDI0+	Ethernet Media Dependent Interface +	I/O - DP	-	-
A14	GBE0_CTREF	ETHCTREF	O-1,8	-	-
A15	SUS_S3#	PM_SLP_S#3	O-3.3	-	-
A16	SATA0_TX+	SATA0_TX+ | SATA 0 Transmit Data +	O - DP	-	-
A17	SATA0_TX-	SATA0_TX- | SATA 0 Transmit Data -	O - DP	-	-
A18	SUS_S4#	PM_SLP_S#4	O-3.3	-	-
A19	SATA0_RX+	SATA0_RX+ | SATA 0 Receive Data +	I - DP	-	-
A20	SATA0_RX-	SATA0_RX - | SATA 0 Receive Data -	I - DP	-	-
A21	GND	Ground	PWR	-	-
A22	SATA2_TX+	SATA2_TX+ | SATA 2 Transmit Data +	O - DP	-	-
A23	SATA2_TX-	SATA2_TX- | SATA 2 Transmit Data -	O - DP	-	-
A24	SUS_S5#	PM_SLP_S#5	O-3.3	-	-
A25	SATA2_RX+	SATA2_RX+ | SATA 2 Receive Data +	I - DP	-	-
A26	SATA2_RX-	SATA2_RX- | SATA 2 Receive Data -	I - DP	-	-
A27	BATLOW#	PM_BATLOW# | Battery Low	I-3.3	PU 8k2 3.3Vsb	-
A28	ATA_ACT#	ATA_LED# | SATA LED	O-3.3	PU 10k 3.3V	
A29	AC_SYNC	AC_SYNC | AC'97 Sync	O-3.3	-	int. PD 20k in QM57
A30	AC_RST#	AC_RST# | AC'97 Reset	O-3.3	-	int. PD 20k in QM57
A31	GND	Ground	PWR	-	
A32	AC_BITCLK	AC_BITCLK | AC'97 Clock	O-3.3	-	int. PD 20k in QM57
A33	AC_SDOUT	AC_SDATAOUT | AC'97 Data	O-3.3	-	int. PD 20k in QM57
A34	BIOS_DISABLE#	BIOS_DISABLE#	I-3.3	PU 10k 3.3Vsb	-
A35	THRMTRIP#	PM_THRMTRIP#_CON	O-3.3	PU 330 3.3V	-
A36	USB6-	USB_PN6 | USB Data – Port6	I/O - DP	-	int. PD 20k in QM57
A37	USB6+	USB_PP6 | USB Data + Port6	I/O - DP	-	int. PD 20k in QM57
A38	USB_6_7_OC#	USB_OC#_6_7 | USB OverCurrent Port 6/7	I-3.3	PU 10k 3.3Vsb	-
A39	USB4-	USB_PN4 | USB Data - Port4	I/O - DP	-	int. PD 20k in QM57
A40	USB4+	USB_PP4 | USB Data + Port4	I/O - DP	-	int. PD 20k in QM57
A41	GND	Ground	PWR	-	-
A42	USB2-	USB_PN2 | USB Data - Port2	I/O - DP	-	int. PD 20k in QM57
A43	USB2+	USB_PP2 | USB Data + Port2	I/O - DP	-	int. PD 20k in QM57
A44	USB_2_3_OC#	USB_OC#_2_3 | USB OverCurrent Port 2/3	I-3.3	PU 10k 3.3Vsb	
A45	USB0-	USB_PN0 | USB Data - Port0	I/O - DP	-	int. PD 20k in QM57
A46	USB0+	USB_PP0 | USB Data + Port0	I/O - DP	-	int. PD 20k in QM57
A47	VCC_RTC	V_BAT	PWR	-	-
A48	EXCD0_PERST#	Express Card Support [0]|card reset	O-3.3	PU 10k 3.3Vsb	-
A49	EXCD0_CPPE#	Express Card Support [0]| capable request	I-3.3	PU 10k 3.3V	-
A50	LPC_SERIRQ	INT_SERIRQ | Serial Interrupt Request	IO-3.3	PU 10k 3.3V	-
A51	GND	Ground	PWR	-	-
A52	PCIE5_TX+	PCI Express 5 Transmit +	O - DP	-	-
A53	PCIE5_TX-	PCI Express 5 Transmit -	O - DP	-	-
A54	GPI0	General Purpose Input 0	I-3.3	PU 10k 3.3Vsb	-
A55	PCIE4_TX+	PCI Express 4 Transmit +	O - DP	-	-

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Signal Descriptions (cont'd)

Row A

Pin	Signal	Description	Type	PU/PD	Comment
A56	PCIE4_TX-	PCI Express 4 Transmit -	O - DP	-	-
A57	GND	Ground	PWR	-	-
A58	PCIE3_TX+	PCI Express 3 Transmit +	O - DP	-	-
A59	PCIE3_TX-	PCI Express 3 Transmit -	O - DP	-	-
A60	GND	Ground	PWR	-	-
A61	PCIE2_TX+	PCI Express 2 Transmit +	O - DP	-	-
A62	PCIE2_TX-	PCI Express 2 Transmit -	O - DP	-	-
A63	GPI1	General Purpose Input 1	I-3.3	PU 10k 3.3Vsb	-
A64	PCIE1_TX+	PCI Express 1 Transmit +	O - DP	-	-
A65	PCIE1_TX-	PCI Express 1 Transmit -	O - DP	-	-
A66	GND	Ground	PWR	-	-
A67	GPI2	General Purpose Input 2	I-3.3	PU 10k 3.3Vsb	-
A68	PCIE0_TX+	PCI Express 0 +	O - DP	-	-
A69	PCIE0_TX-	PCI Express 0 -	O - DP	-	-
A70	GND	Ground	PWR	-	-
A71	LVDS_A0+	LVDS_AP0 | LVDS Channel A	O - DP	-	-
A72	LVDS_A0-	LVDS_AN0 | LVDS Channel A	O - DP	-	-
A73	LVDS_A1+	LVDS_AP1 | LVDS Channel A	O - DP	-	-
A74	LVDS_A1-	LVDS_AN1 | LVDS Channel A	O - DP	-	-
A75	LVDS_A2+	LVDS_AP2 | LVDS Channel A	O - DP	-	-
A76	LVDS_A2-	LVDS_AN2 | LVDS Channel A	O - DP	-	-
A77	LVDS_VDD_EN	LVDS_VDDEN | LVDS Panel Power	O-2,5	PD 10k	-
A78	LVDS_A3+	LVDS_AP3 | LVDS Channel A	O - DP	-	-
A79	LVDS_A3-	LVDS_AN3 | LVDS Channel A	O - DP	-	-
A80	GND	Ground	PWR	-	-
A81	LVDS_A_CK+	LVDS_CLKAP | LVDS Channel A	O - DP	-	-
A82	LVDS_A_CK-	LVDS_CLKAN | LVDS Channel A	O - DP	-	-
A83	LVDS_I2C_CK	LVDS_DDCPCLK | JILI I2C Clock	IO-3.3	PU 2k2 3.3V	-
A84	LVDS_I2C_DAT	LVDS_DDCPDATA | JILI I2C Data	IO-3.3	PU 2k2 3.3V	-
A85	GPI3	General Purpose Input 3	I-3.3	PU 10k 3.3Vsb	-
A86	KBD_RST#	H_RCIN# | Keyboard Reset	I-3.3	PU 10k 3.3V	-
A87	KBD_A20GATE	H_A20GATE	I-3.3	PU 8k2 3.3V	-
A88	PCIE_CK_REF+	CLK_PCIE_REF P	O - DP	-	-
A89	PCIE_CK_REF-	CLK_PCIE_REF N	O - DP	-	-
A90	GND	Ground	PWR	-	-
A91	RSVD	NC	NC	-	-
A92	RSVD	NC	NC	-	-
A93	GPO0	General Purpose Output 0	O-3.3	PU 10k 3.3Vsb	-
A94	RSVD	NC	NC	-	-
A95	RSVD	NC	NC	-	-
A96	GND	Ground	PWR	-	-
A97	VCC_12V	Power 12V	PWR	-	-
A98	VCC_12V	Power 12V	PWR	-	-
A99	VCC_12V	Power 12V	PWR	-	-
A100	GND	Ground	PWR	-	-
A101	VCC_12V	Power 12V	PWR	-	-
A102	VCC_12V	Power 12V	PWR	-	-
A103	VCC_12V	Power 12V	PWR	-	-
A104	VCC_12V	Power 12V	PWR	-	-
A105	VCC_12V	Power 12V	PWR	-	-
A106	VCC_12V	Power 12V	PWR	-	-
A107	VCC_12V	Power 12V	PWR	-	-
A108	VCC_12V	Power 12V	PWR	-	-
A109	VCC_12V	Power 12V	PWR	-	-
A110	GND	Ground	PWR	-	-

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Signal Descriptions (cont'd)

Row B

Pin	Signal	Description	Type	PU/PD	Comment
B1	GND	Ground	PWR	-	-
B2	GBE0_ACT#	LAN_ACTLED# | Ethernet Activity LED	OD	PU 1k 3.3V	-
B3	LPC_FRAME#	LPC_FRAME# | LPC Frame Indicator	O-3.3	-	-
B4	LPC_AD0	LPC_AD0 | LPC Adress & DATA Bus	IO-3.3	-	
B5	LPC_AD1	LPC_AD1 | LPC Adress & DATA Bus	IO-3.3	-	
B6	LPC_AD2	LPC_AD2 | LPC Adress & DATA Bus	IO-3.3	-	
B7	LPC_AD3	LPC_AD3 | LPC Adress & DATA Bus	IO-3.3	-	
B8	LPC_DRQ0#	SIO_DRQ#0 | LPC Serial DMA Request 0	I-3.3	-	int. PU 20k in QM57
B9	LPC_DRQ1#	SIO_DRQ#1 | LPC Serial DMA Request 1	I-3.3	-	int. PU 20k in QM57
B10	LPC_CLK	CLK_SIOEXTPCI	O-3.3	-	-
B11	GND	Ground	I-3.3	-	-
B12	PWRBTN#	Power Button	I-5	PU 10k 3.3Vsb	-
B13	SMB_CK	SMBUS Clock	O-3.3	PU 2k2 3.3Vsb	-
B14	SMB_DAT	SMBUS Data	IO-3.3	PU 2k2 3.3Vsb	-
B15	SMB_ALERT#	SMB_ALERT#	I-3.3	PU 10k 3.3Vsb	-
B16	SATA1_TX+	SATA1_TX+ | SATA 1 Transmit Data +	O - DP	-	-
B17	SATA1_TX-	SATA1_TX- | SATA 1 Transmit Data -	O - DP	-	-
B18	SUS_STAT#	PM_SUS_ STAT#	O-3.3	-	-
B19	SATA1_RX+	SATA1_RX+ | SATA 1 Receive Data +	I - DP	-	-
B20	SATA1_RX-	SATA1_RX - | SATA 1 Receive Data -	I - DP	-	-
B21	GND	Ground	PWR	-	-
B22	SATA3_TX+	SATA3_TX+ | SATA 3 Transmit Data +	O - DP	-	-
B23	SATA3_TX-	SATA3_TX- | SATA 3 Transmit Data -	O - DP	-	-
B24	PWR_OK	Power OK	I,3.3	PU 10k 3.3Vsb	-
B25	SATA3_RX+	SATA3_RX+ | SATA 3 Receive Data +	I - DP	-	-
B26	SATA3_RX-	SATA3_RX - | SATA 3 Receive Data -	I - DP	-	-
B27	WDT	Watch Dog Timer	O-3.3		-
B28	AC_SDIN2	AC_SDATAIN2	I-3.3	-	int. PD 20k in QM57
B29	AC_SDIN1	AC_SDATAIN1	I-3.3	-	int. PD 20k in QM57
B30	AC_SDIN0	AC_SDATAIN0	I-3.3	-	int. PD 20k in QM57
B31	GND	Ground	PWR	-	
B32	SPKR	AC_SPKR	O-3.3	-	int. PD 20k in QM57
B33	I2C_CK	I2CLK	O-3.3	PU 10k 3.3V	-
B34	I2C_DAT	I2DAT	IO-3.3	PU 10k 3.3V	-
B35	THRM#	PM THRM# CON | Over Temperature	I-3.3		-
B36	USB7-	USB_PN7 | USB Data – Port7	I/O - DP	-	int. PD 20k in QM57
B37	USB7+	USB_PP7 | USB Data + Port7	I/O - DP	-	int. PD 20k in QM57
B38	USB_4_5_OC#	USB_OC#_4_5 | USB OverCurrent Port	I-3.3	PU 10k 3.3Vsb	
B39	USB5-	USB_PN5 | USB Data- Port5	I/O - DP	-	int. PD 20k in QM57
B40	USB5+	USB_PP5 | USB Data+ Port5	I/O - DP	-	int. PD 20k in QM57
B41	GND	Ground	I-3.3	-	-
B42	USB3-	USB_PN3 | USB Data- Port3	I/O - DP	-	int. PD 20k in QM57
B43	USB3+	USB_PP3 | USB Data+ Port3	I/O - DP	-	int. PD 20k in QM57
B44	USB_0_1_OC#	USB_OC#_0_1 | USB OverCurrent Port	I-3.3	PU 10k 3.3Vsb	-
B45	USB1-	USB_PN1 | USB Data- Port1	I/O - DP	-	int. PD 20k in QM57
B46	USB1+	USB_PP1 | USB Data+ Port1	I/O - DP	-	int. PD 20k in QM57
B47	EXCD1_PERST#	Express Card Support [1]|card reset	O-3.3	PU 10k 3.3Vsb	-
B48	EXCD1_CPPE#	Express Card Support [1]| capable c.	I-3.3	PU 10k 3.3V	-
B49	SYS_RESET#	ETX_SYS_RESET# | Reset Input	I-3.3	PU 10k 3.3Vsb	-
B50	CB_RESET#	PCI_RST# | PCI Bus Reset	O-3.3	-	-
B51	GND	Ground	PWR	-	-
B52	PCIE5_RX+	PCI Express 5 Recieve +	I - DP	-	-
B53	PCIE5_RX-	PCI Express 5 Receive -	I - DP	-	-
B54	GPO1	General Purpose Output 1	O-3.3	PU 10k 3.3Vsb	-
B55	PCIE4_RX+	PCI Express 4 Recieve +	I - DP	-	-

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Signal Descriptions (cont'd)

Row B

Pin	Signal	Description	Type	PU/PD	Comment
B56	PCIE4_RX-	PCI Express 4 Receive -	I - DP	-	-
B57	GPO2	General Purpose Output 2	O-3.3	PU 10k 3.3Vsb	-
B58	PCIE3_RX+	PCI Express 3 Recieve +	I - DP	-	-
B59	PCIE3_RX-	PCI Express 3 Receive -	I - DP	-	-
B60	GND	Ground	PWR	-	-
B61	PCIE2_RX+	PCI Express 2 Receive +	I - DP	-	-
B62	PCIE2_RX-	PCI Express 2 Receive -	I - DP	-	-
B63	GPO3	General Purpose Output 3	O-3.3	PU 10k 3.3Vsb	-
B64	PCIE1_RX+	PCI Express 1 Receive +	I - DP	-	-
B65	PCIE1_RX-	PCI Express 1 Receive -	I - DP	-	-
B66	WAKE0#	PCIE_WAKEI#	I-3.3	PU 1k 3.3Vsb	-
B67	WAKE1#	WAKE1#	I-3.3	PU 10k 3.3Vsb	-
B68	PCIE0_RX+	PCI Express 0 Receive +	I - DP	-	-
B69	PCIE0_RX-	PCI Express 0 Receive -	I - DP	-	-
B70	GND	Ground	PWR	-	-
B71	LVDS_B0+	LVDS_BP0 | LVDS Channel B Data0+	O - DP	-	-
B72	LVDS_B0-	LVDS_BN0 | LVDS Channel B Data0-	O - DP	-	-
B73	LVDS_B1+	LVDS_BP1 | LVDS Channel B Data1+	O - DP	-	-
B74	LVDS_B1-	LVDS_BN1 | LVDS Channel B Data1-	O - DP	-	-
B75	LVDS_B2+	LVDS_BP2 | LVDS Channel B Data2+	O - DP	-	-
B76	LVDS_B2-	LVDS_BN2 | LVDS Channel B Data2-	O - DP	-	-
B77	LVDS_B3+	LVDS_BP3 | LVDS Channel B Data3+	O - DP	-	-
B78	LVDS_B3-	LVDS_BN3 | LVDS Channel B Data3-	O - DP	-	-
B79	LVDS_BKLT_EN	LVDS Panel Backlight Enable	O-3.3	PD 100k	-
B80	GND	Ground	PWR	-	-
B81	LVDS_B_CK+	LVDS_CLKBP | LVDS Channel B	O - DP	-	-
B82	LVDS_B_CK-	LVDS_CLKBM | LVDS Channel B	O - DP	-	-
B83	LVDS_BKLT_CTRL	Backlight Brightness	O-3.3	PD 100k	-
B84	VCC_5V_SBY	5V Standby	PWR	-	-
B85	VCC_5V_SBY	5V Standby	PWR	-	-
B86	VCC_5V_SBY	5V Standby	PWR	-	-
B87	VCC_5V_SBY	5V Standby	PWR	-	-
B88	RSVD	NC	NC	-	-
B89	VGA_RED	Analog Video RGB-RED	OA	PD 150R	-
B90	GND	Ground	PWR	-	-
B91	VGA_GRN	Analog Video RGB-GREEN	OA	PD 150R	-
B92	VGA_BLU	Analog Video RGB-BLUE	OA	PD 150R	-
B93	VGA_HSYNC	Analog Video H-Sync	O-3.3	-	-
B94	VGA_VSYNC	Analog Video V-Sync	O-3.3	-	-
B95	VGA_I2C_CK	Display Data Channel - Clock	O-3.3		-
B96	VGA_I2C_DAT	Display Data Channel - Data	IO-3.3		-
B97	RSVD	NC	NC	-	-
B98	RSVD	NC	NC	-	-
B99	RSVD	NC	NC	-	-
B100	GND	Ground	PWR	-	-
B101	VCC_12V	Power 12V	PWR	-	-
B102	VCC_12V	Power 12V	PWR	-	-
B103	VCC_12V	Power 12V	PWR	-	-
B104	VCC_12V	Power 12V	PWR	-	-
B105	VCC_12V	Power 12V	PWR	-	-
B106	VCC_12V	Power 12V	PWR	-	-
B107	VCC_12V	Power 12V	PWR	-	-
B108	VCC_12V	Power 12V	PWR	-	-
B109	VCC_12V	Power 12V	PWR	-	-
B110	GND	Ground	PWR	-	-

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Signal Descriptions (cont'd)

Row C

Pin	Signal	Description	Type	PU/PD	Comment
C1	GND	Ground	PWR	-	-
C2	IDE_D7	IDE Data Bus	IO	PD 10k	-
C3	IDE_D6	IDE Data Bus	IO	-	-
C4	IDE_D3	IDE Data Bus	IO	-	-
C5	IDE_D15	IDE Data Bus	IO	-	-
C6	IDE_D8	IDE Data Bus	IO	-	-
C7	IDE_D9	IDE Data Bus	IO	-	-
C8	IDE_D2	IDE Data Bus	IO	-	-
C9	IDE_D13	IDE Data Bus	IO	-	-
C10	IDE_D1	IDE Data Bus	IO	-	-
C11	GND	Ground	PWR	-	-
C12	IDE_D14	IDE Data Bus	IO	-	-
C13	IDE_IORDY	IDE I/O Ready	I-3.3	PU 4K7 3.3V	-
C14	IDE_IOR#	I/O read line to IDE device	O-3.3		-
C15	PCI_PME#	PCI Power Management Event	IO-3.3		int. PU 20k in QM57
C16	PCI_GNT2#	PCI Bus Grant 2	O-3.3		int. PU 20k in QM57
C17	PCI_REQ2#	PCI Bus Request 2	I-3.3	PU 8K2 3.3V	-
C18	PCI_GNT1#	PCI Bus Grant 1	O-3.3		int. PU 20k in QM57
C19	PCI_REQ1#	PCI Bus Request 1	I-3.3	PU 8K2 3.3V	-
C20	PCI_GNT0#	PCI Bus Grant 0	O-3.3		int. PU 20k in QM57
C21	GND	Ground	PWR		-
C22	PCI_REQ0#	PCI Bus Reqest 0	I-3.3	PU 8K2 3.3V	-
C23	PCI_RESET#	PCI Bus Reset	O-3.3	-	-
C24	PCI_AD0	PCI Adress & Data Bus line	IO-3.3	-	-
C25	PCI_AD2	PCI Adress & Data Bus line	IO-3.3	-	-
C26	PCI_AD4	PCI Adress & Data Bus line	IO-3.3	-	-
C27	PCI_AD6	PCI Adress & Data Bus line	IO-3.3	-	-
C28	PCI_AD8	PCI Adress & Data Bus line	IO-3.3	-	-
C29	PCI_AD10	PCI Adress & Data Bus line	IO-3.3	-	-
C30	PCI_AD12	PCI Adress & Data Bus line	IO-3.3	-	-
C31	GND	Ground	PWR	-	-
C32	PCI_AD14	PCI Adress & Data Bus line	IO-3.3	-	-
C33	PCI_C/BE1#	PCI Bus Command and Byte enables	IO-3.3	-	-
C34	PCI_PERR#	PCI Bus Grant Error	IO-3.3	PU 8K2 3.3V	-
C35	PCI_LOCK#	PCI Bus Lock	IO-3.3	PU 8K2 3.3V	-
C36	PCI_DEVSEL#	PCI Bus Device Select	IO-3.3	PU 8K2 3.3V	-
C37	PCI_IRDY#	PCI Bus Bus Initiator Ready	IO-3.3	PU 8K2 3.3V	-
C38	PCI_C/BE2#	PCI Bus Command and Byte enables	IO-3.3		-
C39	PCI_AD17	PCI Adress & Data Bus line	IO-3.3	-	-
C40	PCI_AD19	PCI Adress & Data Bus line	IO-3.3	-	-
C41	GND	Ground	PWR	-	-
C42	PCI_AD21	PCI Adress & Data Bus line	IO-3.3	-	-
C43	PCI_AD23	PCI Adress & Data Bus line	IO-3.3	-	-
C44	PCI_C/BE3#	PCI Bus Command and Byte enables	IO-3.3	-	-
C45	PCI_AD25	PCI Adress & Data Bus line	IO-3.3	-	-
C46	PCI_AD27	PCI Adress & Data Bus line	IO-3.3	-	-
C47	PCI_AD29	PCI Adress & Data Bus line	IO-3.3	-	-
C48	PCI_AD31	PCI Adress & Data Bus line	IO-3.3		-
C49	PCI_IRQA#	PCI Bus Interrupt Request A	I-3.3	PU 8K2 3.3V	-
C50	PCI_IRQB#	PCI Bus Interrupt Request B	I-3.3	PU 8K2 3.3V	-
C51	GND	Ground	PWR		-
C52	PEG_RX0+	PCIe 0 Recieve +	I - DP		-
C53	PEG_RX0-	PCIe 0 Recieve -	I - DP	-	-
C54	TYPE0#	Module type ID pin 0	STO	-	not connected
C55	PEG_RX1+	PCIe 1 Recieve +	I - DP	-	-

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Signal Descriptions (cont'd)

Row C

Pin	Signal	Description	Type	PU/PD	Comment
C56	PEG_RX1-	PCIe 1 Recieve -	I - DP	-	-
C57	TYPE1#	Module type ID pin 1	STO	-	not connected
C58	PEG_RX2+	PCIe 2 Recieve +	I - DP	-	-
C59	PEG_RX2-	PCIe 2 Recieve -	I - DP	-	-
C60	GND	Ground	PWR	-	-
C61	PEG_RX3+	PCIe 3 Recieve +	I - DP	-	-
C62	PEG_RX3-	PCIe 3 Recieve -	I - DP	-	-
C63	RSVD	NC	NC	-	-
C64	RSVD	NC	NC	-	-
C65	PEG_RX4+	PCIe 4 Recieve +	I - DP	-	-
C66	PEG_RX4-	PCIe 4 Recieve -	I - DP	-	-
C67	RSVD	FAN_PWM_CTRL	0-5	-	-
C68	PEG_RX5+	PCIe 5 Recieve +	I - DP	-	-
C69	PEG_RX5-	PCIe 5 Recieve -	I - DP	-	-
C70	GND	Ground	PWR	-	-
C71	PEG_RX6+	PCIe 6 Recieve +	I - DP	-	-
C72	PEG_RX6-	PCIe 6 Recieve -	I - DP	-	-
C73	RSVD	NC	NC	-	-
C74	PEG_RX7+	PCIe 7 Recieve +	I - DP	-	-
C75	PEG_RX7-	PCIe 7 Recieve -	I - DP	-	-
C76	GND	Ground	PWR	-	-
C77	RSVD	FAN_TACH	I-5	-	-
C78	PEG_RX8+	PCIe 8 Recieve +	I - DP	-	-
C79	PEG_RX8-	PCIe 8 Recieve -	I - DP	-	-
C80	GND	Ground	PWR	-	-
C81	PEG_RX9+	PCIe 9 Recieve +	I - DP	-	-
C82	PEG_RX9-	PCIe 9 Recieve -	I - DP	-	-
C83	RSVD	Physical Presence	I-3.3	PU 10k 3.3Vsb	-
C84	GND	Ground	PWR	-	-
C85	PEG_RX10+	PCIe 10 Recieve +	I - DP	-	-
C86	PEG_RX10-	PCIe 10 Recieve -	I - DP	-	-
C87	GND	Ground	PWR	-	-
C88	PEG_RX11+	PCIe 11 Recieve +	I - DP	-	-
C89	PEG_RX11-	PCIe 11 Recieve –	I - DP	-	-
C90	GND	Ground	PWR	-	-
C91	PEG_RX12+	PCIe 12 Recieve +	I - DP	-	-
C92	PEG_RX12-	PCIe 12 Recieve -	I - DP	-	-
C93	GND	Ground	PWR	-	-
C94	PEG_RX13+	PCIe 13 Recieve +	I - DP	-	-
C95	PEG_RX13-	PCIe 13 Recieve -	I - DP	-	-
C96	GND	Ground	PWR	-	-
C97	RSVD	NC	NC	-	-
C98	PEG_RX14+	PCIe 14 Recieve +	I - DP	-	-
C99	PEG_RX14-	PCIe 14 Recieve -	I - DP	-	-
C100	GND	Ground	PWR	-	-
C101	PEG_RX15+	PCIe 15 Recieve +	I - DP	-	-
C102	PEG_RX15-	PCIe 15 Recieve -	I - DP	-	-
C103	GND	Ground	PWR	-	-
C104	VCC_12V	Power 12V	PWR	-	-
C105	VCC_12V	Power 12V	PWR	-	-
C106	VCC_12V	Power 12V	PWR	-	-
C107	VCC_12V	Power 12V	PWR	-	-
C108	VCC_12V	Power 12V	PWR	-	-
C109	VCC_12V	Power 12V	PWR	-	-
C110	GND	Ground	PWR	-	-

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Signal Descriptions (cont'd)

Row D

Pin	Signal	Description	Type	PU/PD	Comment
D1	GND	Ground	PWR	-	-
D2	IDE_D5	IDE Data Bus	IO	-	-
D3	IDE_D10	IDE Data Bus	IO	-	-
D4	IDE_D11	IDE Data Bus	IO	-	-
D5	IDE_D12	IDE Data Bus	IO	-	-
D6	IDE_D4	IDE Data Bus	IO	-	-
D7	IDE_D0	IDE Data Bus	IO	-	-
D8	IDE_REQ#	IDE Device DMA Request.	IO	PD 5k6	-
D9	IDE_IOW#	IDE IO Write	O-3.3	-	-
D10	IDE_ACK#	IDE DMA Acknowledge	O-3.3	-	-
D11	GND	Ground	PWR	-	-
D12	IDE_IRQ	IDE Interrupt Request	I-3.3	PD 10k	-
D13	IDE_A0	IDE Adress Bus	O-3.3	-	-
D14	IDE_A1	IDE Adress Bus	O-3.3	-	-
D15	IDE_A2	IDE Adress Bus	O-3.3	-	-
D16	IDE_CS1#	IDE Chip Select for 1F0h to 1FFh range	O-3.3	-	-
D17	IDE_CS3#	IDE Chip Select for 3F0h to 3FFh range	O-3.3	-	-
D18	IDE_RESET#	IDE Reset Output to Device	O-3.3	-	-
D19	PCI_GNT3#	PCI Bus Grant 3	O-3.3	-	int. PU 20k in QM57
D20	PCI_REQ3#	PCI Bus Reqest 3	I-3.3	PU 8K2 3.3V	-
D21	GND	Ground	PWR	-	-
D22	PCI_AD1	PCI Adress & Data Bus line	IO-3.3	-	-
D23	PCI_AD3	PCI Adress & Data Bus line	IO-3.3	-	-
D24	PCI_AD5	PCI Adress & Data Bus line	IO-3.3	-	-
D25	PCI_AD7	PCI Adress & Data Bus line	IO-3.3	-	-
D26	PCI_C/BE0#	PCI Bus Command and Byte enables 0	IO-3.3	-	-
D27	PCI_AD9	PCI Adress & Data Bus line	IO-3.3	-	-
D28	PCI_AD11	PCI Adress & Data Bus line	IO-3.3	-	-
D29	PCI_AD13	PCI Adress & Data Bus line	IO-3.3	-	-
D30	PCI_AD15	PCI Adress & Data Bus line	IO-3.3	-	-
D31	GND	Ground	PWR	-	-
D32	PCI_PAR	PCI Bus Parity	IO-3.3	-	-
D33	PCI_SERR#	PCI Bus System Error	IO-3.3	PU 8K2 3.3V	-
D34	PCI_STOP#	PCI Bus Stop	IO-3.3	PU 8K2 3.3V	-
D35	PCI_TRDY#	PCI Bus Target Ready	IO-3.3	PU 8K2 3.3V	-
D36	PCI_FRAME#	PCI Bus Cycle Frame	IO-3.3	PU 8K2 3.3V	-
D37	PCI_AD16	PCI Adress & Data Bus line	IO-3.3	-	-
D38	PCI_AD18	PCI Adress & Data Bus line	IO-3.3	-	-
D39	PCI_AD20	PCI Adress & Data Bus line	IO-3.3	-	-
D40	PCI_AD22	PCI Adress & Data Bus line	IO-3.3	-	-
D41	GND	Ground	PWR	-	-
D42	PCI_AD24	PCI Adress & Data Bus line	IO-3.3	-	-
D43	PCI_AD26	PCI Adress & Data Bus line	IO-3.3	-	-
D44	PCI_AD28	PCI Adress & Data Bus line	IO-3.3	-	-
D45	PCI_AD30	PCI Adress & Data Bus line	IO-3.3	-	-
D46	PCI_IRQC#	PCI Bus Interrupt Request C	I-3.3	PU 8K2 3.3V	-
D47	PCI_IRQD#	PCI Bus Interrupt Request D	I-3.3	PU 8K2 3.3V	-
D48	PCI_CLKRUN#	PCI Clock Run	I-3.3	PU 8K2 3.3V	-
D49	PCI_M66EN#	Control PCI Speed 33/66 Mhz	I-3.3	-	Fixed to 33 MHz
D50	PCI_CLK	PCI Clock	O-3.3	-	-
D51	GND	Ground	PWR	-	-
D52	PEG_TX0+	PCIe 0 Transmit +	O - DP	-	-
D53	PEG_TX0-	PCIe 0 Transmit -	O - DP	-	-
D54	PEG_LANE_RV#	PCIe Lane Reversal	I-3.3	-	-
D55	PEG_TX1+	PCIe 1 Transmit +	O - DP	-	-

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Signal Descriptions (cont'd)

Row D

Pin	Signal	Description	Type	PU/PD	Comment
D56	PEG_TX1-	PCIe 1 Transmit -	O - DP	-	-
D57	TYPE2#	Module type ID pin 2	STO	-	not connected
D58	PEG_TX2+	PCIe 2 Transmit +	O - DP	-	-
D59	PEG_TX2-	PCIe 2 Transmit -	O - DP	-	-
D60	GND	Ground	PWR	-	-
D61	PEG_TX3+	PCIe 3 Transmit +	O - DP	-	-
D62	PEG_TX3-	PCIe 3 Transmit -	O - DP	-	-
D63	RSVD	NC	NC	-	-
D64	RSVD	NC	NC	-	-
D65	PEG_TX4+	PCIe 4 Transmit +	O - DP	-	-
D66	PEG_TX4-	PCIe 4 Transmit -	O - DP	-	-
D67	GND	Ground	PWR	-	-
D68	PEG_TX5+	PCIe 5 Transmit +	O - DP	-	-
D69	PEG_TX5-	PCIe 5 Transmit -	O - DP	-	-
D70	GND	Ground	PWR	-	-
D71	PEG_TX6+	PCIe 6 Transmit +	O - DP	-	-
D72	PEG_TX6-	PCIe 6 Transmit -	O - DP	-	-
D73	RSVD	NC	NC	-	-
D74	PEG_TX7+	PCIe 7 Transmit +	O - DP	-	-
D75	PEG_TX7-	PCIe 7 Transmit -	O - DP	-	-
D76	GND	Ground	PWR	-	-
D77	IDE_CBLID#	IDE Cable Indicator Signal	I-3.3	PD 10k	-
D78	PEG_TX8+	PCIe 8 Transmit +	O - DP	-	-
D79	PEG_TX8-	PCIe 8 Transmit -	O - DP	-	-
D80	GND	Ground	PWR	-	-
D81	PEG_TX9+	PCIe 9 Transmit +	O - DP	-	-
D82	PEG_TX9-	PCIe 9 Transmit -	O - DP	-	-
D83	RSVD	NC	NC	-	-
D84	GND	Ground	PWR	-	-
D85	PEG_TX10+	PCIe 10 Transmit +	O - DP	-	-
D86	PEG_TX10-	PCIe 10 Transmit -	O - DP	-	-
D87	GND	Ground	PWR	-	-
D88	PEG_TX11+	PCIe 11 Transmit +	O - DP	-	-
D89	PEG_TX11-	PCIe 11 Transmit -	O - DP	-	-
D90	GND	Ground	PWR	-	-
D91	PEG_TX12+	PCIe 12 Transmit +	O - DP	-	-
D92	PEG_TX12-	PCIe 12 Transmit -	O - DP	-	-
D93	GND	Ground	PWR	-	-
D94	PEG_TX13+	PCIe 13 Transmit +	O - DP	-	-
D95	PEG_TX13-	PCIe 13 Transmit -	O - DP	-	-
D96	GND	Ground	PWR	-	-
D97	PEG_ENABLE#	PCIe Enable	I-3.3	PU 43K2 3.3V	-
D98	PEG_TX14+	PCIe 14 Transmit +	O - DP	-	-
D99	PEG_TX14-	PCIe 14 Transmit -	O - DP	-	-
D100	GND	Ground	PWR	-	-
D101	PEG_TX15+	PCIe 15 Transmit +	O - DP	-	-
D102	PEG_TX15-	PCIe 15 Transmit -	O - DP	-	-
D103	GND	Ground	PWR	-	-
D104	VCC_12V	Power 12V	PWR	-	-
D105	VCC_12V	Power 12V	PWR	-	-
D106	VCC_12V	Power 12V	PWR	-	-
D107	VCC_12V	Power 12V	PWR	-	-
D108	VCC_12V	Power 12V	PWR	-	-
D109	VCC_12V	Power 12V	PWR	-	-
D110	GND	Ground	PWR	-	-

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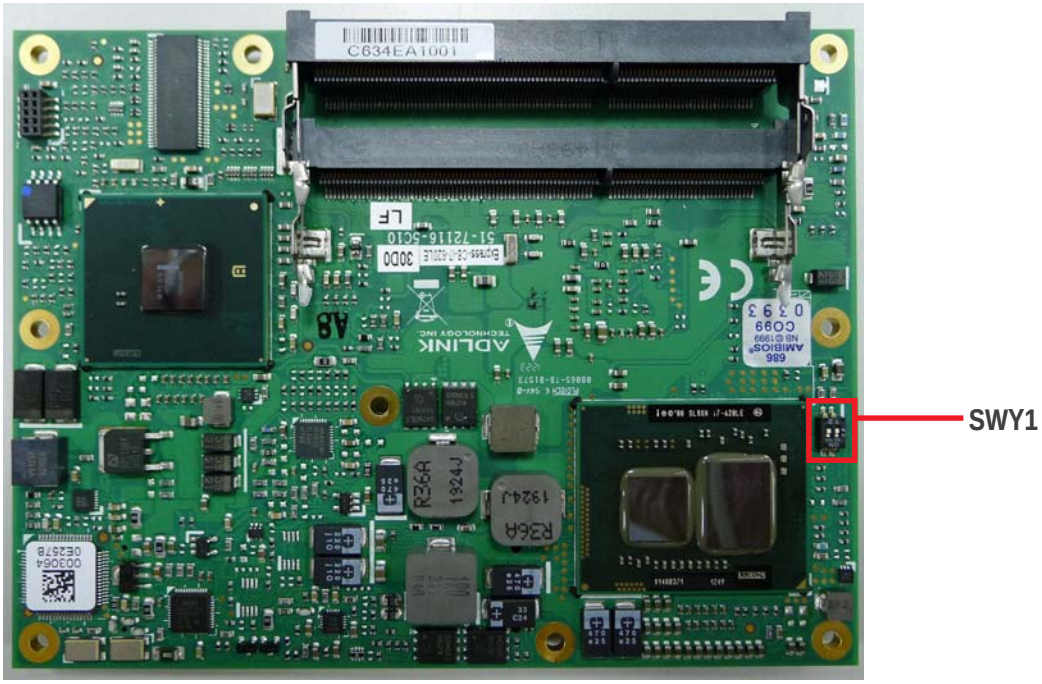
Signal Descriptions (cont'd)

Signal Type Legend	
IO-2,5	Bi-directional 2,5 V Input/Output
IO-3,3	Bi-directional 3,3 V Input/Output
IO-5	Bi-directional 5 V Input/Output
I-3,3	3,3 V Input
I-5	5 V Input
O-2,5	2,5 V Output
O-3,3	3,3 V Output
O-5	5 V Output
IO	Input/Output
OA	Analog Output
OD	Digital Output
I/O - DP	Differential Pair Input/Output
O - DP	Differential Pair Output
I - DP	Differential Pair Input
PWR	Power or Ground
STO	Strapping Output
PU	Pull Up Resistor
PD	Pull Down Resistor
NC	Not Connected / Reserved

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5.5 PCI Express x16 Configuration

Switch SWY1 allows you to configure the PCI Express x16 lanes from the CPU as 1 PCIe x16 or 2 PCIe x8.



SWY1: PCI Express Configuration Switch

Mode	Pin 1	Pin 2
1x PCIe x16 (default)	Off	Off
2x PCIe x8	On	Off

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6 Embedded Functions

All embedded board functions on ADLINK's Computer on Modules are supported at the operating system level using the ADLINK Intelligent Device Interface (AIDI) library. The AIDI API programming interface is compatible and identical across all ADLINK Computer on Modules and all supported operating systems. The AIDI library includes a demo program to demonstrate the library's functionallity.

6.1 Watchdog Timer

The Express-CB implements a Watchdog timer that can be used to automatically detect software execution problems or system hangs and reset the board if necessary. The Watchdog timer consists of a counter that counts down from an initial value to zero. When the system is operating normally, the software that sets the intial value periodically resets the counter so that the it never reaches zero. If the counter reaches zero before the software resets it, the system is presumed to be malfunctioning and a reset signal is asserted.

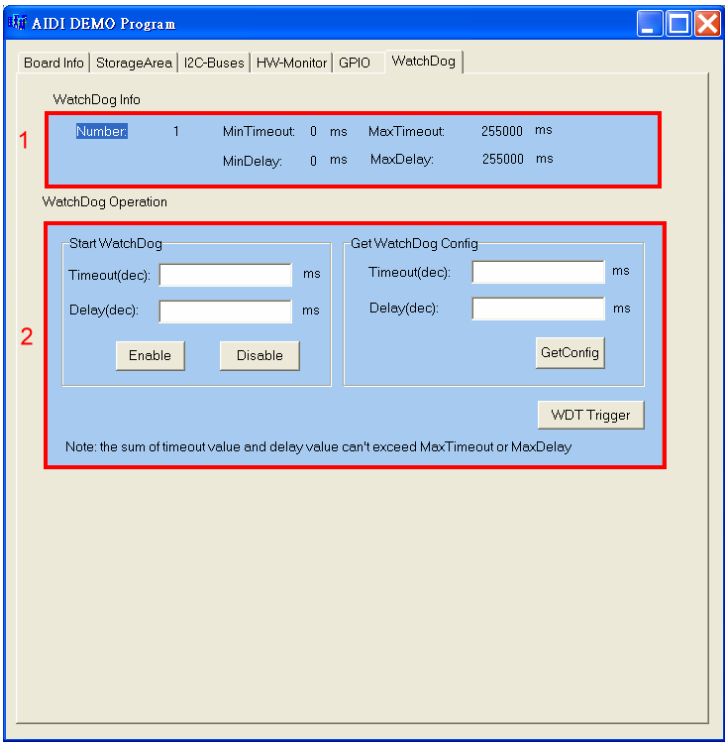


The AIDI Library Watchdog functions support Watchdog control of the board. If the Watchdog begins countdown and reaches zero, it will access the CPU's RESET signal to reset the system. This application must call another function named AidiWDogTrigger that triggers the Watchdog to restart to prevent system reset.

AIDI Demo Program
- Watchdog Tab

The AIDI Demo Program allows retrieval of the current Watchdog status and updating of the Watchdog settings

If the Watchdog is enabled, the user can click the *WDT Trigger* button to manually reset the counter and prevent the system from resetting



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6.2 GPIO

GPIO library support is limited to GPIO signals that originate from the Computer on Module and extend to the carrier board. COM Express modules support 4 GPO and 4 GPI signals. Some of ADLINK's COM Express boards can configure all 8 ports for GPI or GPO use.

GPIO signals can be monitored and controlled by using the ADLINK Intelligent Device Interface (AIDI) library that is compatible and identical across all ADLINK COM Express modules and all supported operating systems.

The COM Express Type 2 standard assigns the following pins for either GPI or GPO

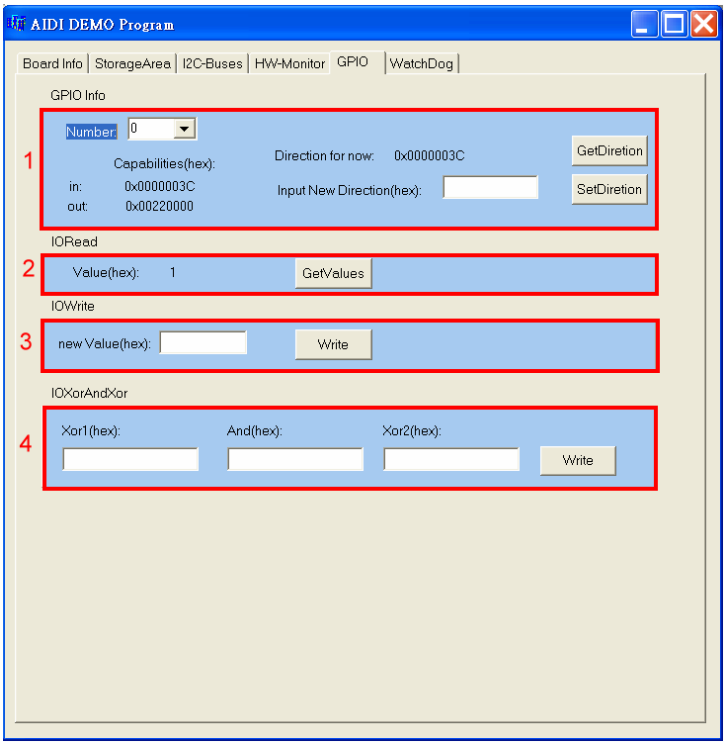
Pin	Signal Type #	AIDI ID (bit)	Remark
A54	GPI0	0	Express-CB can configure this pin for GPI and GPO
A63	GPI1	1	Express-CB can configure this pin for GPI and GPO
A67	GPI2	2	Express-CB can configure this pin for GPI andGPO
A85	GPI3	3	Express-CB can configure this pin for GPI andGPO
A93	GPO0	4	Express-CB can configure this pin for GPI and GPO
B54	GPO1	5	Express-CB can configure this pin for GPI and GPO
B57	GPO2	6	Express-CB can configure this pin for GPI and GPO
B63	GPO3	7	Express-CB can configure this pin for GPI and GPO

AIDI Demo Program - GPIO Tab

The AIDI Demo Program displays current GPI or GPO status and allows reading of GPI and writing to GPO.

The table above links logical port numbers in AIDI to physical port numbers on the COM Express board-to-board connector.

For boards that support *multi-direction* the "SetDirection" button can configure the port for either GPI or GPO



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6.3 Hardware Monitoring

To ensure system health of your embedded system ADLINK's COM Express modules come with built in support for monitoring and control of CPU and system temperatures, fan speed and critical module voltage levels.

The AIDI Library provides simple APIs at the application level to support these functions and adds alarm functions when voltage or temperature levels exceed the upper or lower limit set by the user.

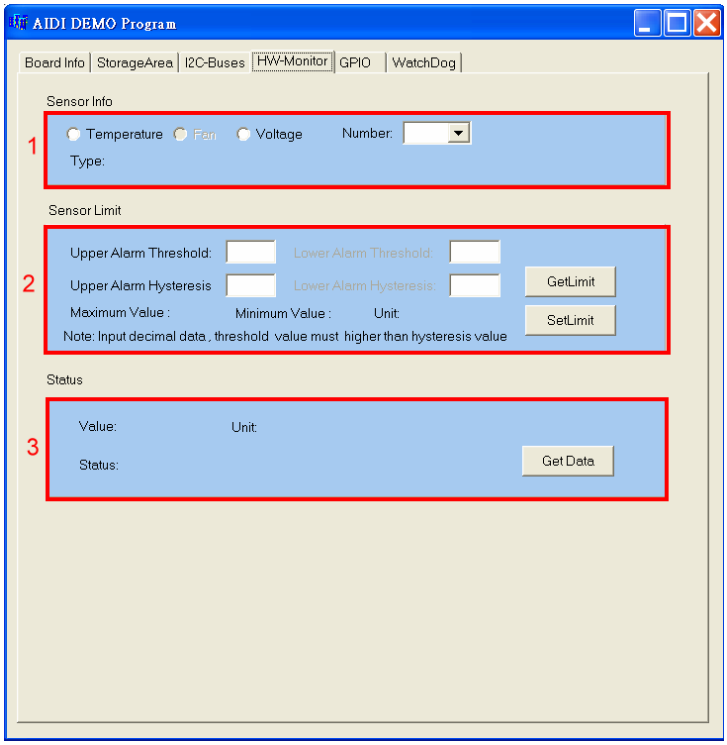
On the Express-CB the following monitored values can be read from the module:
CPU temperature, system temperature, Vcore, 1.8V, 5V, 3.3V and 12V.

AIDI Demo Program
- HW Monitor Tab

Field 1 displays detected sensors (number).

Field 2 allows setting of upper and lower alarm limits.

Field 3 displays read out information of sensors.



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7 System Resources

7.1 System Memory Map

Address Range (dec.)	Address Range (hex)	Size	Description
(4GB-2MB)	FFE00000 - FFFFFFFF	2 MB	High BIOS Area
(4GB-18MB) - (4GB-17MB-1)	FEE00000 - FEEFFFFF	1 MB	FSB Interrupt Memory Space
(4GB-20MB) - (4GB-19MB-1)	FEC00000 - FECFFFFF	1 MB	APIC Configuration Space
960 K - 1024 K	F0000 - FFFFF	64 KB	System BIOS Area
896 K - 960 K	E0000 - EFFFF	64 KB	Extended System BIOS Area
768 K - 896 K	C0000 - DFFFF	128 KB	PCI expansion ROM area C0000 - C7FFF: Onboard VGA BIOS CB800 - CC7FFF: Intel 82577LM PXE option ROM when onboard LAN boot ROM is enabled.
640 K - 768 K	A0000 - BFFFF	128 KB	Video Buffer & SMM space
0 K - 640 K	00000 - 9FFFF	640 KB	DOS Area

7.2 Direct Memory Access Channels

Channel Number	Data Width	System Resource	Comment
0	8-bits	Parallel port	Note (1)
1	8-bits	Parallel port	Note (1)
2	8-bits	Diskette drive	Note (1)
3	8-bits	Parallel port	Note (1)
4		Reserved - cascade channel	
5	16-bits	Open	
6	16-bits	Open	
7	16-bits	Open	

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7.3 Legacy I/O Map

Address Range (hex)	Description
000-01F	DMA controller 1, 8237A-5 equivalent
020-02D and 030-03F	Interrupt controller 1, 8259 equivalent
02E-02F	LPC SIO (W83627HG-AW) configuration index/data registers
040-05F	Timer, 8254-2 equivalent
060, 062, 064, 066, 068-06F	8742 equivalent (keyboard)
061, 063, 065, 067	NMI control and status
070-07F	Real Time Clock Controller(bit 7 -NMI mask)
080-091	DMA page register
93-9F	DMA page registers continued
0A0-0B1 and 0B4-0BF	Interrupt controller 2, 8259 equivalent
0B2h	APM Control I/O Address
0B3h	APM Status I/O Address
0C0-0DF	DMA controller 2, 8237A-5 equivalent
0F0	Co-processor error register
0F1	N/A
0F2-0F3	N/A
0F4	IDE ID port
0F5-0F7	N/A
0F8	IDE Index port
0F9-0FB	N/A
0FC	IDE Data port
0FD-0FF	N/A
170-177 and 376	Secondary IDE Channel
180-181	Default AIM4 SRAM control register (may be remapped)
1F0-1F7 and 3F6	Primary IDE Controller (AT Drive)
290	SIO_PME_BASE_ADDRESS
2E8-2EF	Serial port 4
2F8-2FF	Serial port 3
370-377	Secondary Floppy Disk Controller
378- 37F	Printer Port (LPT 1)
3B0-3BF	Mono/VGA mode video
3C0-3DF	VGA registers
3E8-3EF	Serial port 2
3F0-3F7	Primary Floppy disk controller
3F8-3FF	Serial port 1
400	SMBUS IO base
4D0	Master PIC Edge/Level Trigger register
4D1	Slave PIC Edge/Level Trigger register
500	GPIO base address for SB
800	alias for ACPI I/O base address.
830	SMI Control Registers.
860	alias for ICH TCO base address
CF9	Reset Control register (8 bit I/O)
CF8-CFC	The PCI config space index/data ports
0A00-0AFF	Reserved for SIO functions base address (eg: Hardware Monitor, GPIO, etc)

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7.4 Interrupt Request (IRQ) Lines

PIC Mode

IRQ#	Typical Interrupt Resource	Connected	Available
0	Counter 0	N/A	No
1	Keyboard controller	N/A	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 2 (COM2)	IRQ3 via SERIRQ, IRQ3 at ISA bus	Note (1)
4	Serial Port 1 (COM1) / PCI / ISA	IRQ4 via SERIRQ, IRQ4 at ISA bus	Note (1)
5	PCI / ISA	IRQ5 via SERIRQ, IRQ5 at ISA bus	Note (1)
6	Floppy Drive Controller	IRQ6 via SERIRQ	No
7	PCI / ISA	IRQ7 via SERIRQ, IRQ7 at ISA bus	Note (1)
8	Real-time clock	N/A	No
9	SCI / PCI	IRQ9 via SERIRQ, IRQ9 at ISA bus	Note (1), (2)
10	No	N/A	No
11	No	N/A	No
12	PS/2 Mouse / PCI / ISA	IRQ12 via SERIRQ, IRQ12 at ISA bus	Note (1)
13	Math Processor	N/A	No
14	Primary IDE controller / PCI / ISA	IRQ14 via SERIRQ, IRQ14 at ISA bus	Note (1)
15	No	N/A	No



(1) These IRQs can be used for PCI devices when onboard device is disabled. If IRQ is from ISA, user must reserve IRQ for ISA in BIOS setup menu.
(2) BIOS does not allow IRQ 9 setting for ISA bus.

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APIC Mode

IRQ#	Typical Interrupt Resource	Connected	Available
0	Counter 0	N/A	No
1	Keyboard controller	N/A	No
2	PCI / ISA	N/A	No
3	Serial Port 2 (COM2) / PCI / ISA	IRQ3 via SERIRQ, IRQ3 at ISA bus	Note (1)
4	Serial Port 1 (COM1) / PCI / ISA	IRQ4 via SERIRQ, IRQ4 at ISA bus	Note (1)
5	PCI / ISA	IRQ5 via SERIRQ, IRQ5 at ISA bus	Note (1)
6	Floppy Drive Controller	IRQ6 via SERIRQ	No
7	PCI / ISA	IRQ7 via SERIRQ, IRQ7 at ISA bus	Note (1)
8	Real-time clock	N/A	No
9	ACPI-Compliant system	IRQ9 via SERIRQ, IRQ9 at ISA bus	Note (1), (2)
10	PCI / ISA	IRQ10 via SERIRQ, IRQ10 at ISA bus	Note (1)
11	PCI / ISA	IRQ11 via SERIRQ, IRQ11 at ISA bus	Note (1)
12	PS/2 Mouse / PCI / ISA	IRQ12 via SERIRQ, IRQ12 at ISA bus	Note (1)
13	Math Processor	N/A	No
14	Primary IDE controller / PCI / ISA	IRQ14 via SERIRQ, IRQ14 at ISA bus	Note (1)
15	Secondary IDE controller / PCI / ISA	IRQ15 via SERIRQ, IRQ15 at ISA bus	Note (1)
16	N/A	PCIE Port 0/1/2/3/4/5/6/7, P.E.G Root Port, I.G.D, EHCI Controller #2, PCI Slot 0 HECI host 1, HECI host 2	Yes
17	N/A	PCIE Port 0/1/2/3/4/5/6/7, P.E.G Root Port, PCI Slot 1, KT Controller	Yes
18	N/A	PCIE Port 0/1/2/3/4/5/6/7, P.E.G Root Port, SATA Host controller, SMBus Controller, Thermal Controller, PCI Slot 2, IDER Controller	Yes
19	N/A	PCIE Port 0/1/2/3/4/5/6/7, P.E.G Root Port, SATA Host controller, SATA Host controller#1, PCI Slot 3	Yes
20	N/A	ICH9 internal GbE controller	No
21	N/A		No
22	N/A	ICH9 HDA	No
23	N/A	EHCI Controller 1	No



(1) These IRQs can be used for PCI devices when onboard device is disabled. If IRQ is from ISA, user must reserve IRQ for ISA in BIOS setup menu.
(2) BIOS does not allow IRQ 9 setting for ISA bus.

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7.5 PCI Configuration Space Map

Bus No.	Device No.	Function No.	Routing	Description
00h	00h	00h	N/A	Intel MCH DRAM Controls
00	01H	00H	Internal	P.E.G. Root Port
02	00H	0FFH	N/A	P.E.G. Port
00h	02h	00h	Internal	Intel Integrated Graphics Device
00h	16h	00h	Internal	Intel Management Engine Interface #1
00h	16h	01h	Internal	Intel Management Engine Interface #2
00h	16h	02h	Internal	IDE-R
00h	16h	03h	Internal	KT
00h	19h	00h	Internal	GbE Controller
00h	1Ah	00h	Internal	Intel USB EHCI Controller #2
00h	1Bh	00h	Internal	High Definition Audio controller
00h	1Ch	00h	Internal	PCI Express Root port 1
00h	1Ch	01h	Internal	PCI Express Root port 2
00h	1Ch	02h	Internal	PCI Express Root port 3
00h	1Ch	03h	Internal	PCI Express Root port 4
00h	1Ch	04h	Internal	PCI Express Root port 5
00h	1Ch	05h	Internal	PCI Express Root port 6
00h	1Ch	06h	Internal	PCI Express Root port 7
00h	1Ch	07h	Internal	PCI Express Root port 8
00h	1Dh	00h	Internal	Intel USB EHCI Controller #1
00h	1Eh	00h	N/A	Intel PCI to PCI Bridge
00h	1Fh	00h	N/A	Intel LPC Interface Bridge
00h	1Fh	02h	Internal	Intel SATA controller #1
00h	1Fh	03h	Internal	Intel SMBus Controller
00h	1Fh	05h	Internal	Intel SATA controller #2
00h	1Fh	06h	Internal	Thermal Controller
11h	00h	0FFh	Internal	PCIE Port #0
12h	00h	0FFh	Internal	PCIE Port #1
13h	00h	0FFh	Internal	PCIE Port #2
14h	00h	0FFh	Internal	PCIE Port #3
15h	00h	0FFh	Internal	PCIE Port #4
16h	00h	0FFh	Internal	PCIE Port #5
17h	00h	0FFh	Internal	PCIE Port #6
18h	00h	0FFh	Internal	PCIE Port #7
20h	04h	00h	Intemal	PCI Slot 0
20h	05h	00h	Intemal	PCI Slot 1
20h	06h	00h	Intemal	PCI Slot 2
20h	07h	00h	Intemal	PCI Slot 3

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7.6 PCI Interrupt Routing Map

PIRQ	INT Line	PEG Root Port	VGA	SATA Controller	SATA Controller 1	SMBus Controller	Therm. Controller	EHCI 1	EHCI 2	HAD	GbE	HECI Host 1	HECI Host 2	IDER Controller	KT Controller
A	INTA	INTA	X						X			X	X		
B	INTB	INTB													X
C	INTC	INTC		X		X	X							X	
D	INTD	INTD		X	X										
E											X				
F															
G										X					
H								X							

PIRQ	PCIE port 0	PCIE port 1	PCIE port 2	PCIE port 3	PCIE port 4	PCIE port 5	PCIE port 6	PCIE port 7	PCI slot 0	PCI slot 1	PCI slot 2	PCI slot 3
A	INTA	INTB	INTC	INTD	INTA	INTB	INTA	INTB	X			
B	INTB	INTC	INTD	INTA	INTB	INTC	INTB	INTC		X		
C	INTC	INTD	INTA	INTB	INTC	INTD	INTC	INTD			X	
D	INTD	INTA	INTB	INTC	INTD	INTA	INTD	INTA				X
E												
F												
G												
H												

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8 BIOS Setup Utility

The following chapter describes basic navigation for the AMIBIOS8 BIOS setup utility for the ADLINK Express-CB COM Express module.

8.1 Starting the BIOS

To enter the setup screen, follow these steps:

1. Power on the motherboard
2. Press the < Delete > key on your keyboard when you see the following text prompt:

   < Press DEL or Delete to run Setup >

3. After you press the < Delete > key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu, such as Chipset and Power menus.

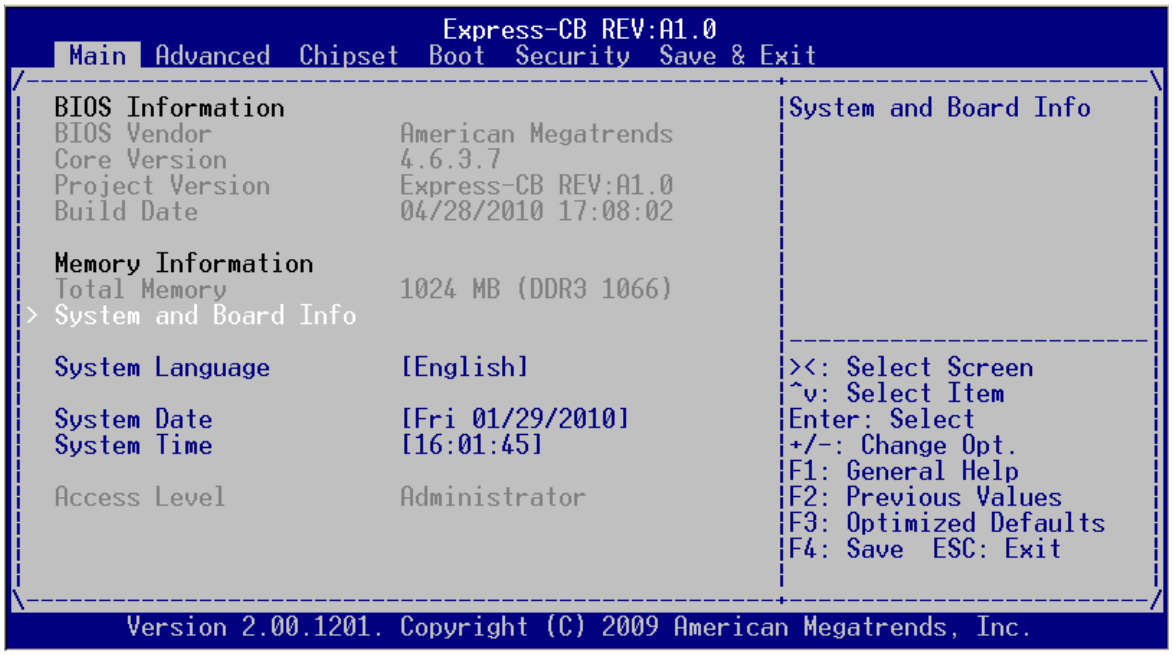


NOTE: In most cases, the < Delete > key is used to invoke the setup screen. There are several cases that use other keys, such as < F1 >, < F2 >, and so on.

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8.2 Main Setup

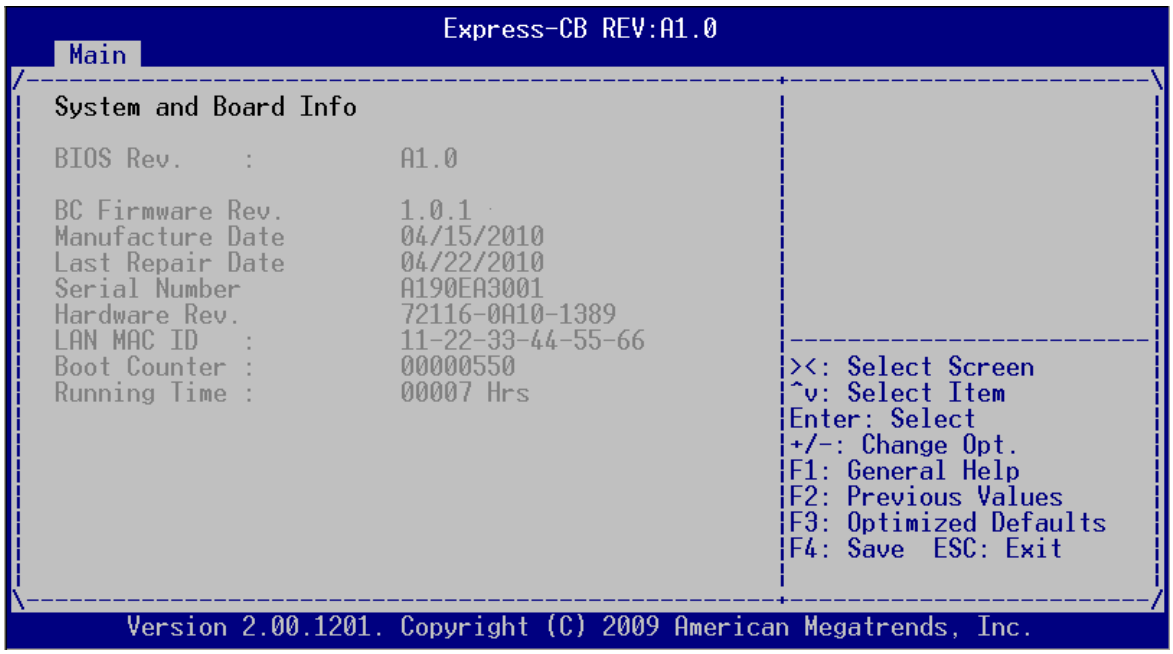
When you first enter the Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the *Main* tab. The Main BIOS Setup screen is shown below.



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8.2.1 System & Board Info

This screen reports system and board information.



BIOS Rev.

Displays the current BIOS revision.

BC Firmware Rev.

Displays the current firmware revision of board controller (BC).

Manufacture Date

Displays the date which the board was manufactured.

Last Repair Date

Displays the date on which the board was last repaired.

Serial Number

Displays the serial number of board.

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Hardware Rev.

The hardware revision is in XXXXX-YYYY-ZZZZ format. XXXXX represents the ADLINK internal P/N for this board. YYYY is the board PCB version and ZZZZ represents a special configuration of the board.

LAN MAC ID

Displays the MAC address of onboard Ethernet controller.

Boot Counter

Displays the number of times the board has been booted-up since production (max. 16777215).

Running Time

Displays the total time the board has been in operation since production. The units are in hours and the maximum value is 65535.

8.2.2 System Language

Choose the system default language.

8.2.3 System Time/System Date

Use this option to change the system time and date. Highlight *System Time* or *System Date* using the < `Arrow` > keys. Enter new values using the keyboard. Press the < `Tab` > key or the < `Arrow` > keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

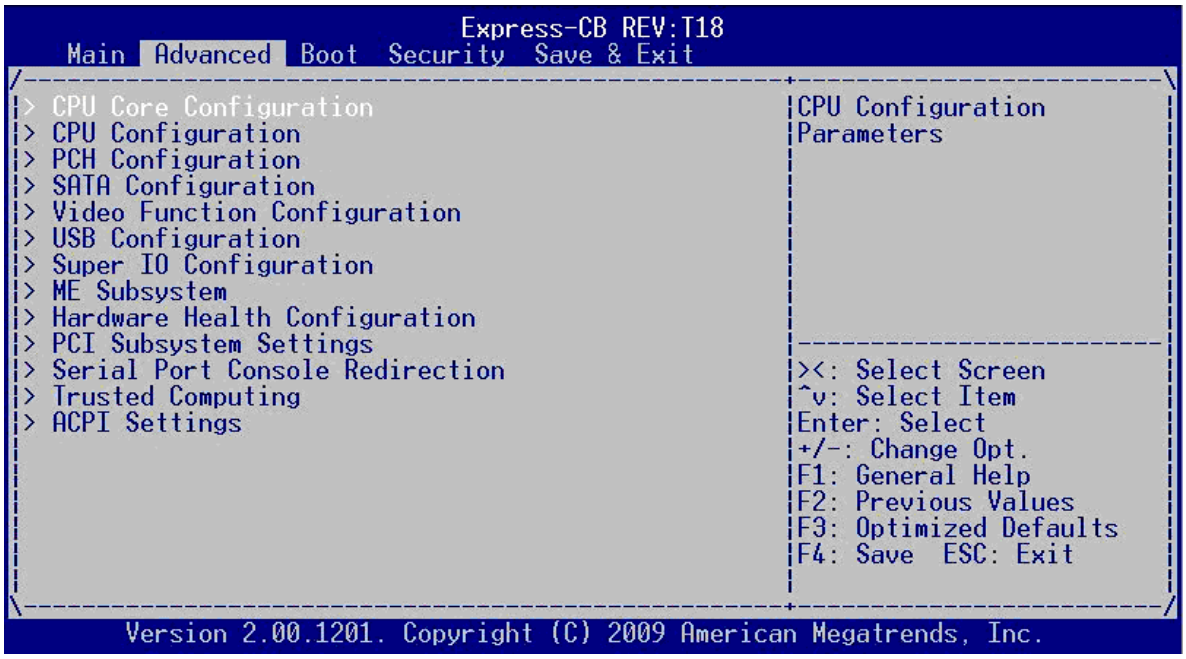


The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

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8.3 Advanced BIOS Setup

Select the *Advanced* tab from the setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as SuperIO Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the < `Arrow` > keys. The Advanced BIOS Setup screen is shown below. The sub menus are described on the following pages.

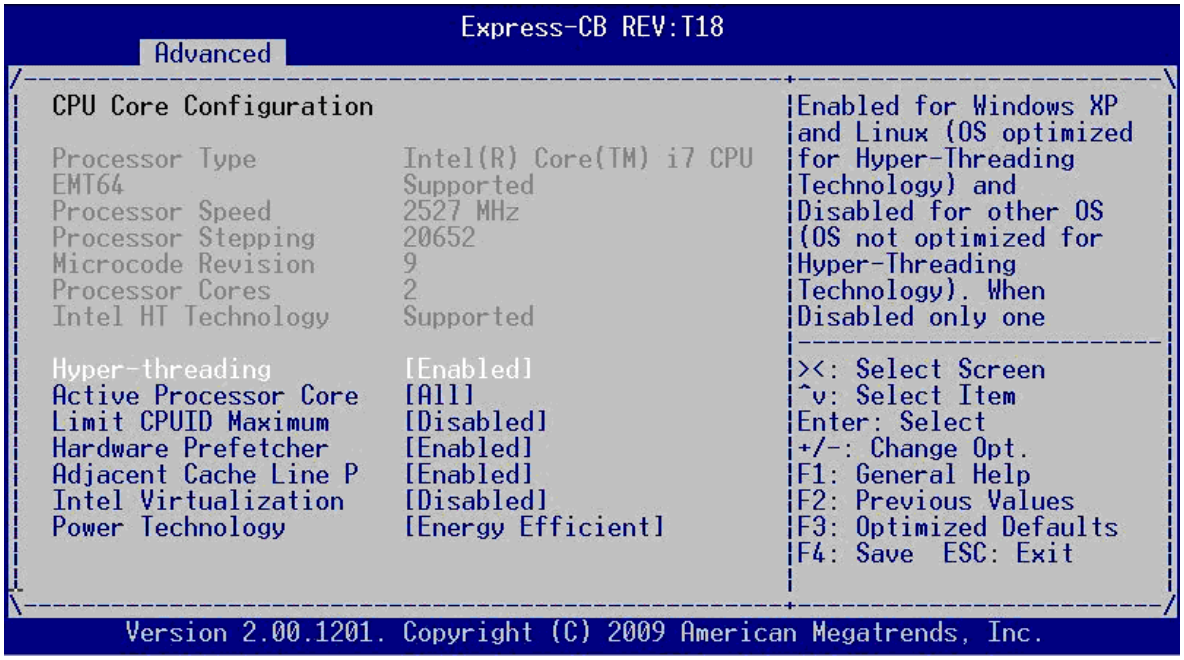




Setting incorrect or conflicting values in Advanced BIOS Setup may cause system malfunctions.

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8.3.1 CPU Core Configuration



Hyper-Threading

Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology).

Active Processor Core

Number of cores to enable in processor. Options: All, 1, 2.

Limit CPUID Maximum

Enable this option to allow compatibility with older operating systems.

Hardware Prefetcher

This feature is used for reducing the wait time of DRAM. The hardware prefetcher looks for streams of data and tries to predict what data will be needed next by the processor and proactively tries to fetch these data.

Adjacent Cache Line P

This feature is used to enable optimal use of sequential memory access for performance purposes. Disable this setting for applications requiring high use of random memory access.

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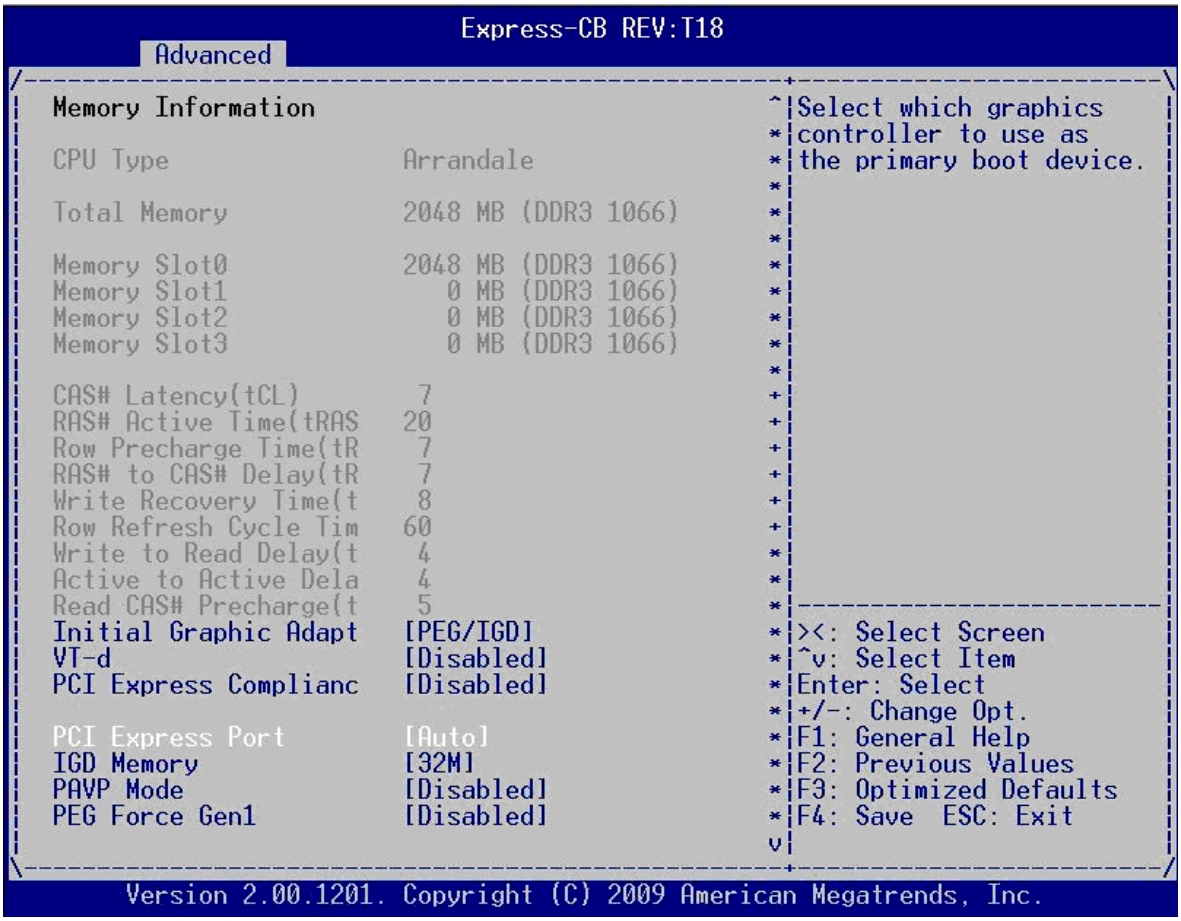
Intel Virtualization

Allows a hardware platform to run multiple operating systems separately and simultaneously, enabling one system to function virtually as several systems. Options are Enabled/Disabled.

Power Technology

Power management feature. Configuration options: Disabled, Energy Efficient, Custom.

8.3.2 CPU Configuration



Initial Graphic Adapter

Allows you to select which graphics controller to use as the primary boot device. Configuration options: IGD, PCI/IGD, PCI/PEG, PEG/IGD, PEG/PCI.

VT-d

The Intel Virtualization Technology for Directed I/O. Options are Enabled/Disabled.

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PCI Express Port

This option enables auto negotiation with a PEG device or enables/disables the use of the PEG port.

IGD Memory

IGD Shared Memory Size. Configuration options: Disable/32M/64M/128M.

PAVP Mode

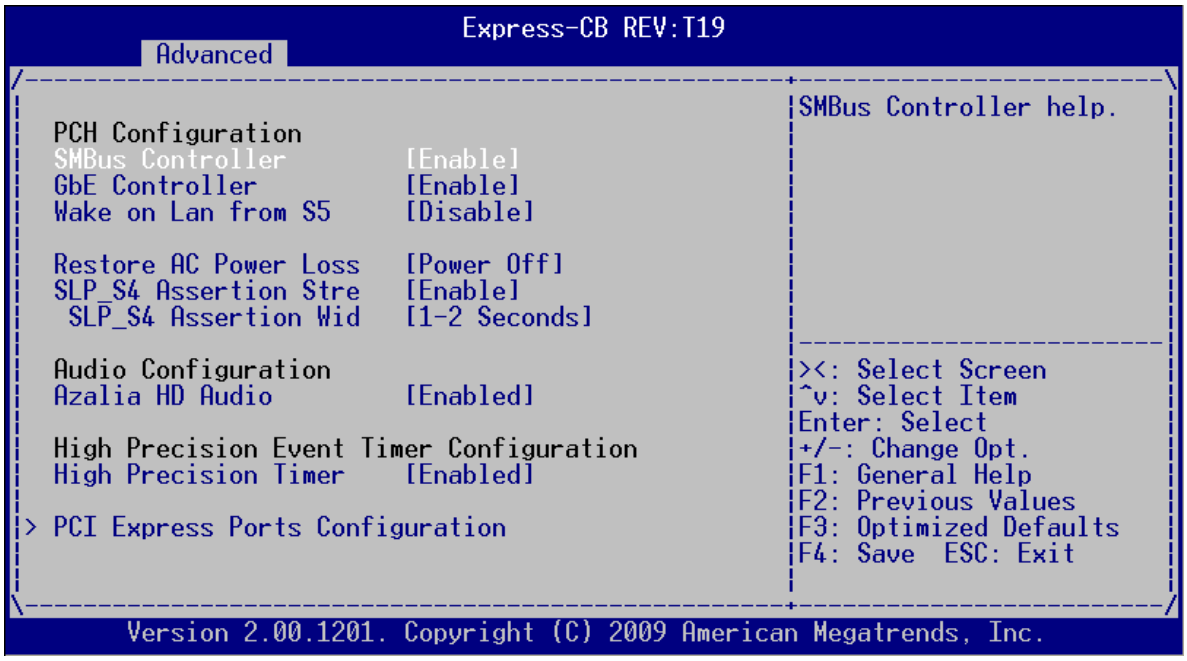
PAVP (Protected Audio Video Path) is a feature to ensure a robust and secure content protection path for high-definition video playback including Blu-ray discs on the Microsoft Windows Vista operating system. It can reduce processor utilization by off-loading the video decode onto the chipset to free up the processor to perform other tasks. Select Lite mode if want to use the PAVP feature.

PEG Force Gen1

PCI Express Port Force Gen1. Options are Enabled/Disabled.

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8.3.3 PCH Configuration



SMBus Controller

Options are Enabled/Disabled.

GbE Controller

Options are Enabled/Disabled.

Wake on Lan from S5

The GbE wake up system from S5 power mode. Options are Enabled/Disabled.

Restore on AC Power Loss

Determines what state the computer enters when AC power is restored after a power loss. The options for this value are Last State, Power On and Power Off.

Option	Description
Power Off	Set this value to always power off the system while AC power is restored.
Power On	Set this value to always power on the system while AC power is restored.
Last State	Set this value to power off/on the system depending on the last system power state while AC power is restored.

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SLP_S4 Assertion Stre

Select a minimum assertion width of the SLP_S4# signal. Options are Enabled/Disabled.

SLP_S4 Assertion Wid

SLP_S4 Assertion Width help. Configuration options: 1-2 Seconds, 2-3 Seconds, 3-4 Seconds, 4-5 Seconds.

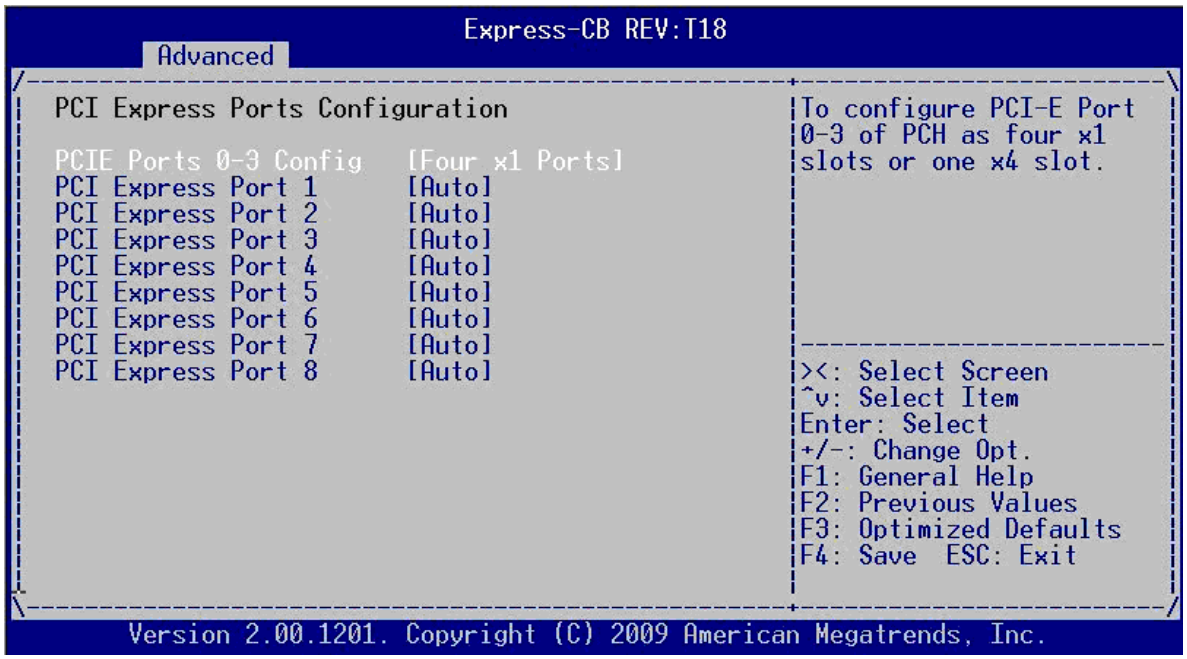
Azalia HD Audio

Onboard HDA Controller. Options are Enabled/Disabled.

High Precision Timer

Set this value to Enable or Disable.

PCI Express Port Configuration



PCI-E Ports 0-3 Config

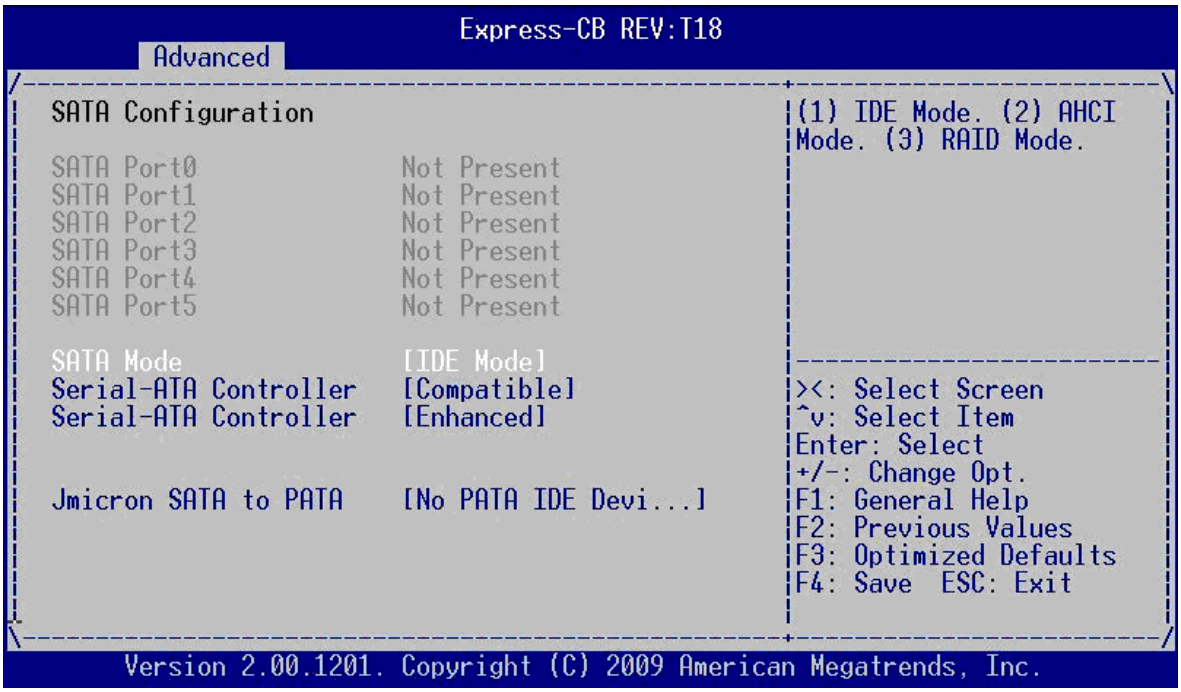
Configure PCI Express ports 0-3 as four x1 lanes or one x4 lane.

PCI Express Port 1-8

Enable/disable the PCI Express ports in the chipset. Configuration options: Auto, Enable, Disable.

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8.3.4 SATA Configuration



SATA Mode

The SATA can be configured as a legacy IDE, RAID and AHCI mode.

Serial-ATA Controller

This item specifies whether SATA Controller 0 is initialized in Compatible or Enhanced mode of operation. The settings are Disabled, Compatible and Enhanced.

Serial-ATA Controller

This item specifies whether SATA Controller 1 is initialized in Compatible or Enhanced mode of operation. The settings are Disabled, Compatible and Enhanced.

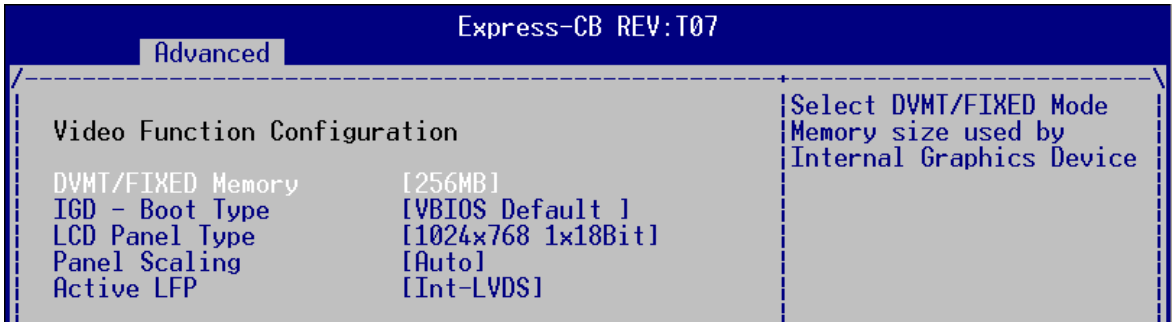
Jmicron SATA to PATA

When a PATA device is not connected to the SATA-to-PATA bridge, this option should be set to *No PATA IDE Device Connected* to avoid delay due to long detection time.

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8.3.5 Video Function Configuration

You can use this screen to select options for Video Function configuration settings. The video function BIOS Setup screen is shown below.



DVMT/FIXED Memory

Select DVMT/Fixed memory size used by the Internal Graphics Device. Configuration options: 128MB, 256MB, Maximum.

IGD – Boot Type

Select the Video Device which will be activated during POST. This has no effect if external graphics present. Configuration options: VBIOS Default, VGA, LFP, VGA+LFP, TV, LFP-SDVO, EFP, TV-SDVO, VGA+LFP-SDVO, VGA+EFP, VGA+TV+LFP.

LCD Panel Type

When LVDS is selected from Boot Display Device, this option allows you to select resolution settings for correct timing to the LVDS interface you want to use. The supported resolutions are: 640x480 1x18-bit, 800x600 1x18-bit, 1024x768 1x18-bit, 1024x768 2x18-bit,1024x768 1x24-bit, 1024x768 2x24-bit, 1280x600 1x18-bit, 1280x768 1x18-bit,1280x800 1x18-bit, 1280x1024 2x24-bit, 1400x1050 2x24-bit 108MHz, 1400x1050 2x24-bit 122MHz, 1600x1200 2x24-bit, 1920x1200 2x24-bit, 2048x1536 2x24-bit.

Panel Scaling

Select the LCD panel scaling option used by the Internal Graphics Device. Configuration options: Auto, Force Scaling, Maintain Aspect Ratio, Off.

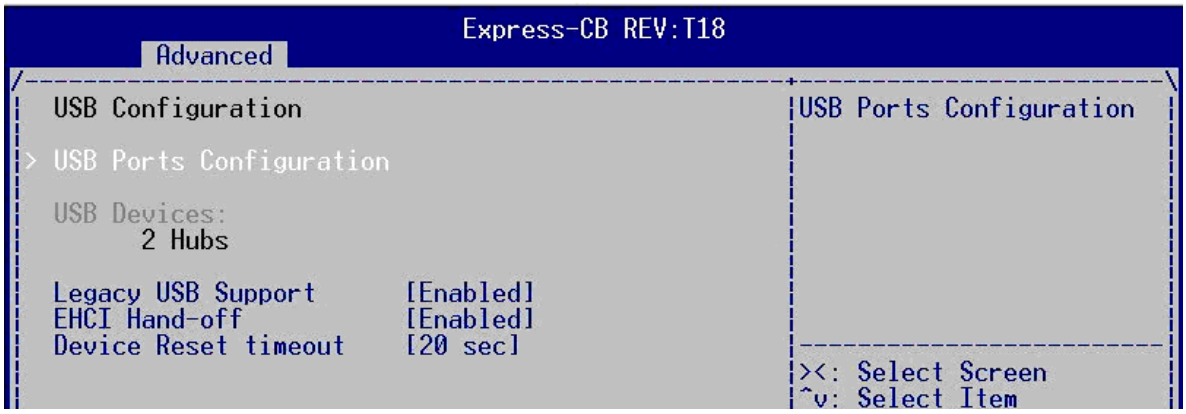
Active LFP

Select the Active LFP Configuration. Configuration options: NO LVDS, Int-LVDS.

Option	Description
No LVDS	VBIOS does not enable LVDS
Int-LVDS	VBIOS enables LVDS driver by integrated encoder

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8.3.6 USB Configuration



Legacy USB Support

Legacy USB Support refers to USB mouse and keyboard support. Normally if this option is not enabled, any attached USB mouse or keyboard will not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or keyboard can control the system even when there is no USB driver loaded on the system. Set this value to enable or disable the Legacy USB Support (see below).

Option	Description
Disabled	Set this value to prevent the use of any USB device in DOS or during system boot.
Enabled	Set this value to allow the use of USB devices during boot and while using DOS.

EHCI Hand-off

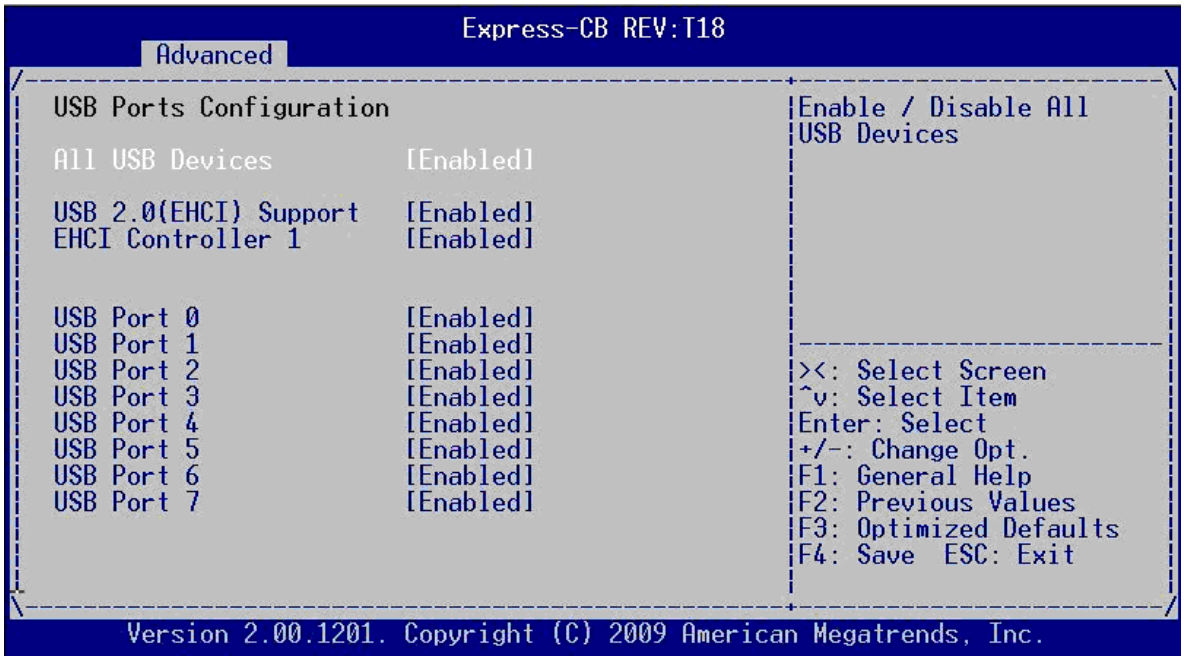
This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver. Configuration options: Enable, Disable.

Device Reset timeout

USB mass storage device Start Unit command timeout.

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USB Ports Configuration



All USB Devices

Options are Enabled/Disabled.

USB 2.0 (EHCI) Support 1

USB 2.0 (EHCI) support. Options are Enabled/Disabled.

EHCI Controller 1

USB 2.0 (EHCI) controller. Options are Enabled/Disabled.

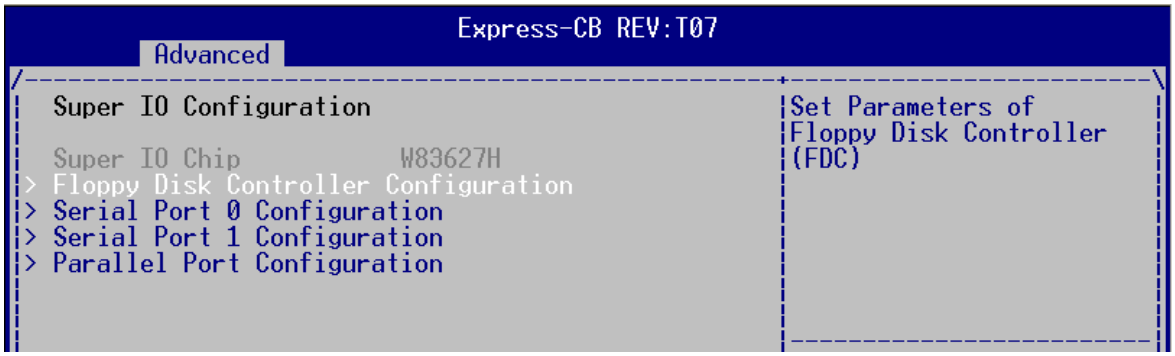
USB Port 0-7

Options are Enabled/Disabled.

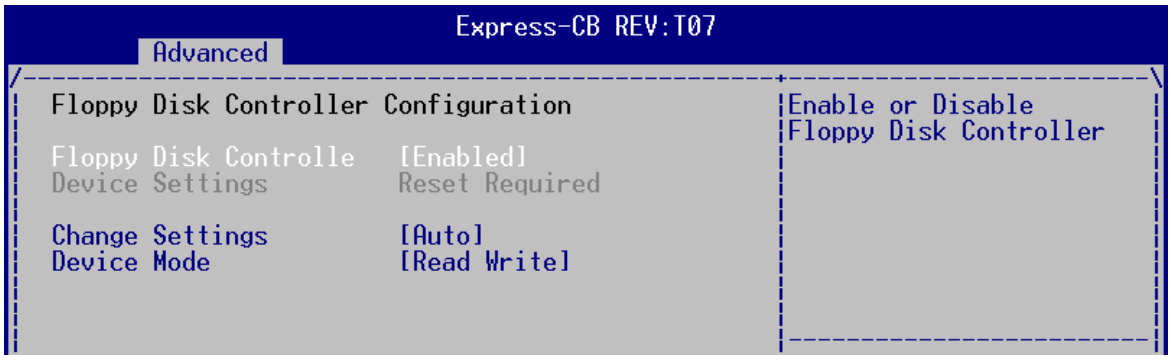
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8.3.7 SuperIO Configuration Screen

The visibility of this SuperIO configuration screen depends on the presence of an onboard SuperIO (Winbond W83627H). If the Express-CB is used on a carrier w/o a SIO chip, the legacy-free mode will take effect.



Floppy Disk Controller Configuration



Floppy Disk Controller

Options are Enabled/Disabled.

Change Settings

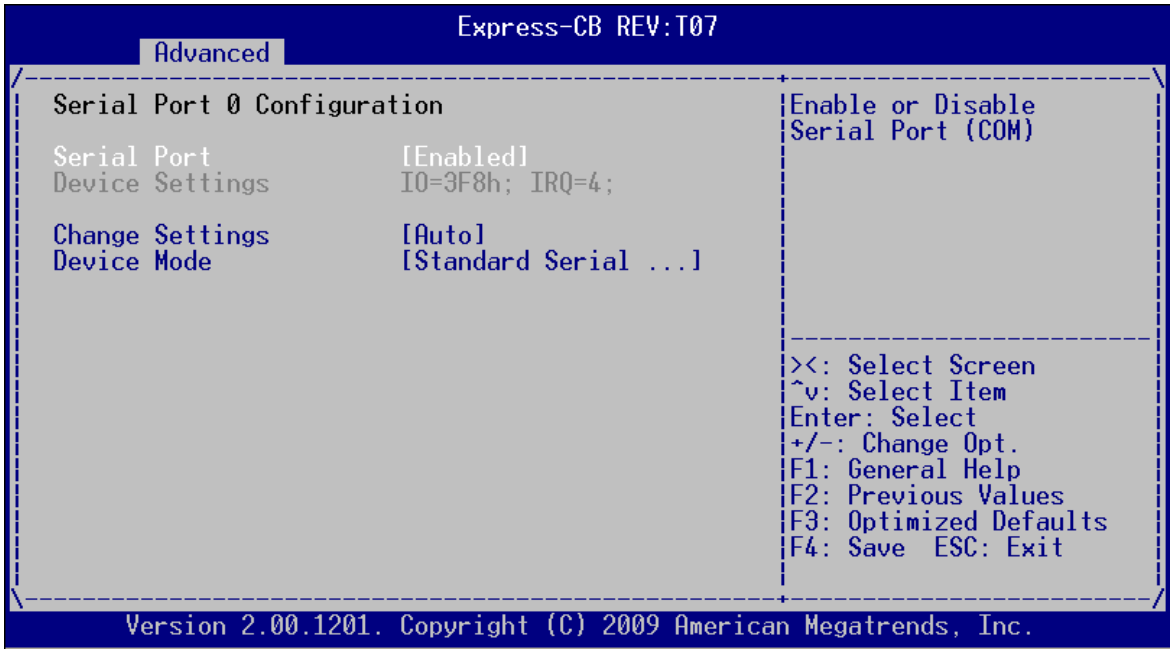
Select an optimal setting for the Floppy Disk Controller.
Options: Auto; IO=3F0, IRQ6, DMA2

Device Mode

Change Mode of Floppy Disk Controller. Select <Read Write> Mode for Normal operation Select <Write Protect> mode for Read only operation.

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Serial Port 0/1 Configuration



Serial Port 0,1 Configuration

Serial Port

Set parameters of serial port 0/1 (COM A/B). Options are Enabled/Disabled.

Change Settings

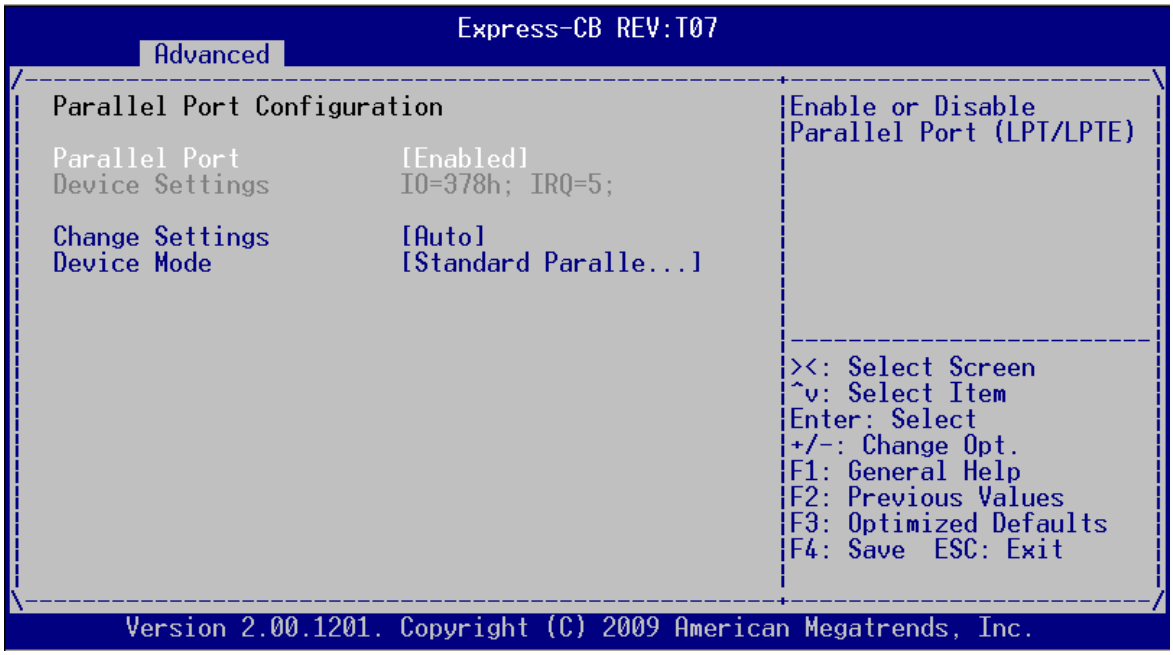
This option specifies the base I/O port address and Interrupt Request address of serial port 0, 1. Configuration options: Auto, 3F8, 3E8, 2F8, 2E8.

Device Mode

This option specifies the serial port mode. Configuration options: Standard Serial Port Mode, IrDA 1.0 (HP SIR) Mode and ASKIR Mode.

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Parallel Port Configuration



Parallel Port

The parallel Port (LPT/LPTE). Options are Enabled/Disabled.

Change Settings

This option specifies the base I/O port address.

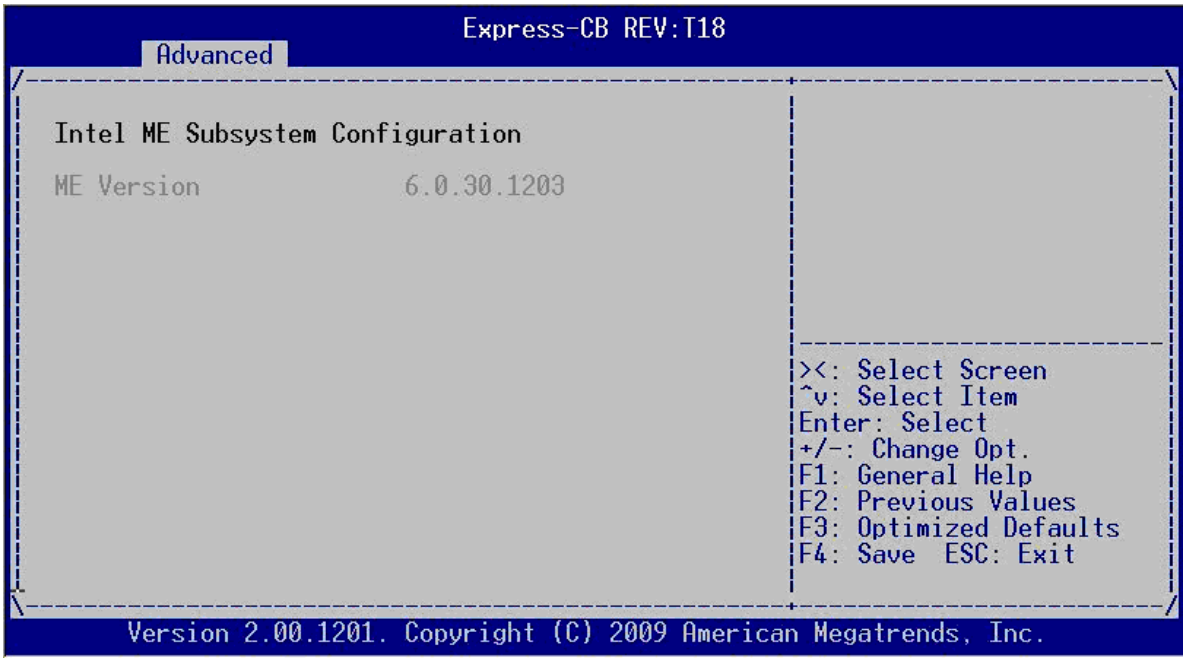
Device Mode

This option specifies the parallel port mode. Options: Standard Parallel Port Mode, EPP Mode, ECP Mode, EPP Mode & ECP Mode.

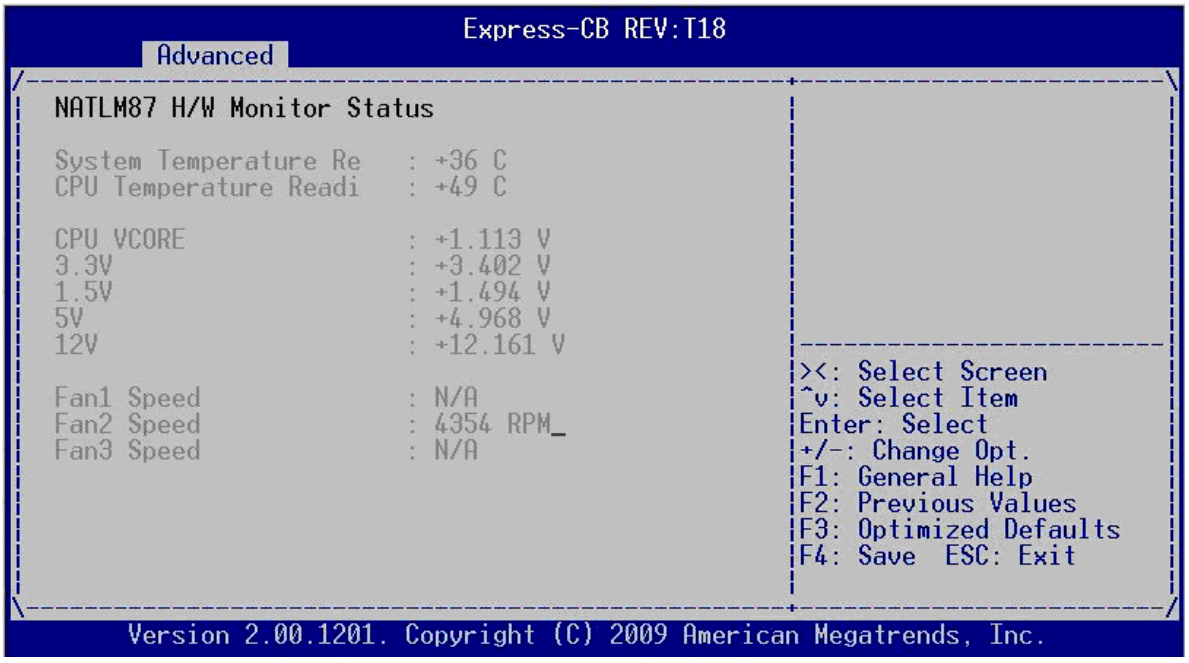
Option	Description
Standard	Set this value to allow the standard parallel port mode to be used.
EPP	The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bidirectional data transfer driven by the host device.
ECP	The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Megabits per second. ECP provides symmetric Bidirectional communication.
EPP+ECP	Allows the parallel port to support both the ECP and EPP modes simultaneously.

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8.3.8 Intel ME Subsystem Configuration

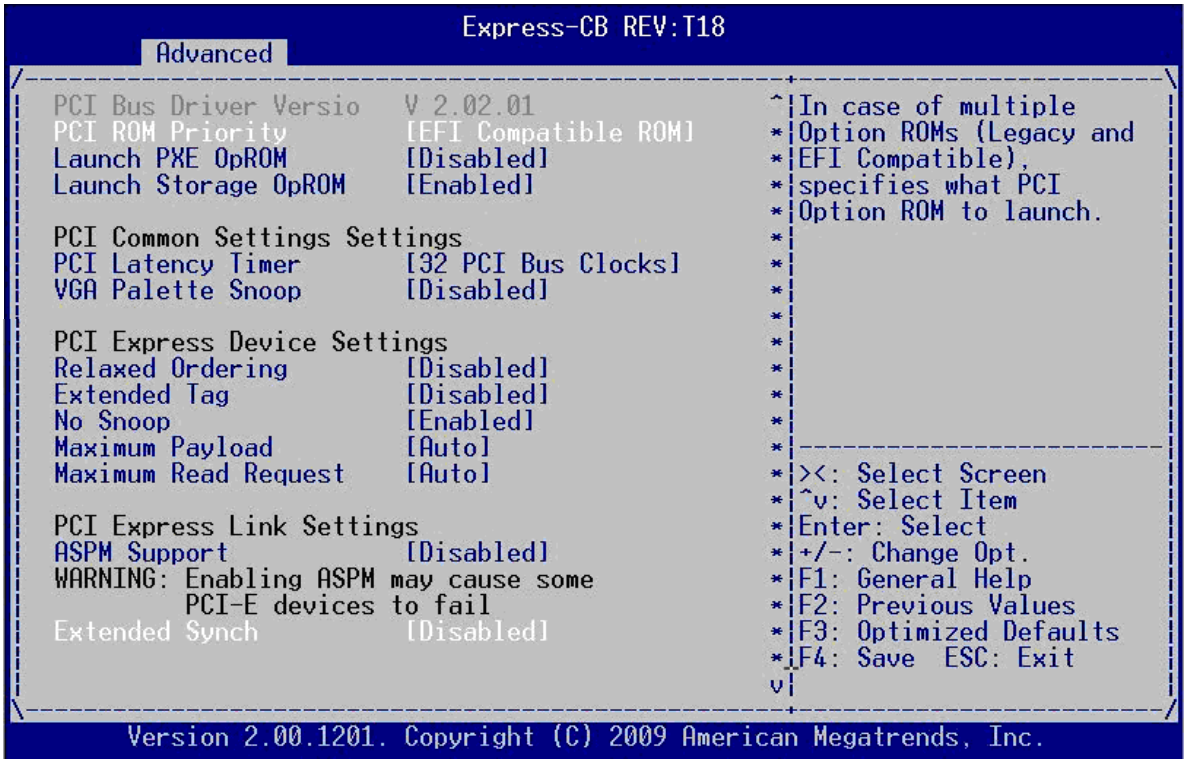


8.3.9 H/W Monitor



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8.3.10 PCI Subsystem Settings



PCI ROM Priority

In case of multiple Option ROMs (Legacy and EFI Compatible), specifies which PCI Option ROM to launch. Configuration options: Legacy ROM, EFI Compatible ROM.

Launch PXE OpROM

Boot option for legacy network devices. Options are Enabled/Disabled.

Launch Storage OpROM

Boot option for legacy mass storage devices with option ROM. Options are Enabled/ Disabled.

PCI Latency Timer

Value to be programmed into PCI Latency Timer Register. Configuration options: 32 PCI Bus Clocks, 64 PCI Bus Clocks, 96 PCI Bus Clocks, 128 PCI Bus Clocks, 160 PCI Bus Clocks, 192 PCI Bus Clocks, 224 PCI Bus Clocks, 248 PCI Bus Clocks.

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VGA Palette Snoop

The VGA Palette registers snooping. Options are Enabled/Disabled.

Relaxed Ordering

Enable/Disable PCI Express device relaxed ordering.

Extended Tag

If enabled, allows device to use 8-bit tag field as a requester. Options are Enabled/Disabled.

No Snoop

Enable/Disable PCI Express Device No Snoop option.

Maximum Payload

Set maximum payload of PCI Express device or allow system BIOS to select the value. Configuration options: Auto, 128 Bytes, 256 Bytes, 512 Bytes, 1024 Bytes, 2048 Bytes, 4096 Bytes.

Maximum Read Request

Set maximum read request size of PCI Express device or allow system BIOS to select the value. Configuration options: Auto, 128 Bytes, 256 Bytes, 512 Bytes, 1024 Bytes, 2048 Bytes, 4096 Bytes.

ASPM Support

Set the ASPM support level:

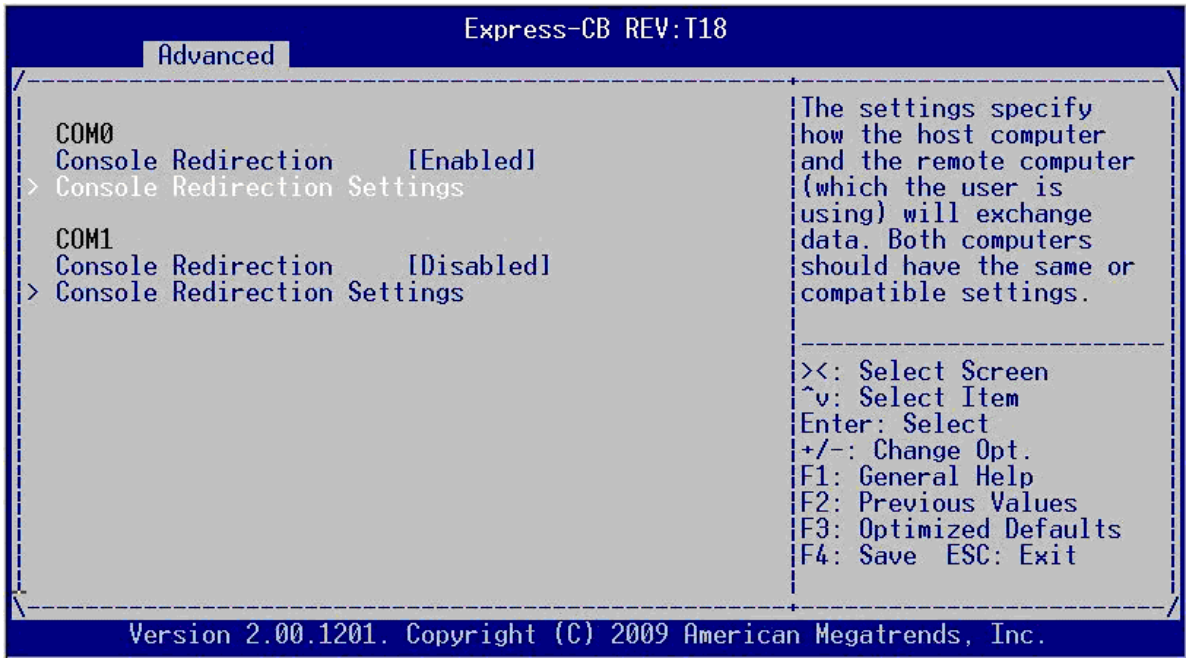
Option	Description
Disabled	Disable ASPM
Auto	BIOS auto configure
Force L0	Force all links to L0 state

Extended Synch

If enabled, allows generation of Extended Synchronization patterns. Options are Enabled/Disabled.

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8.3.11 **Serial Port Console Redirection**

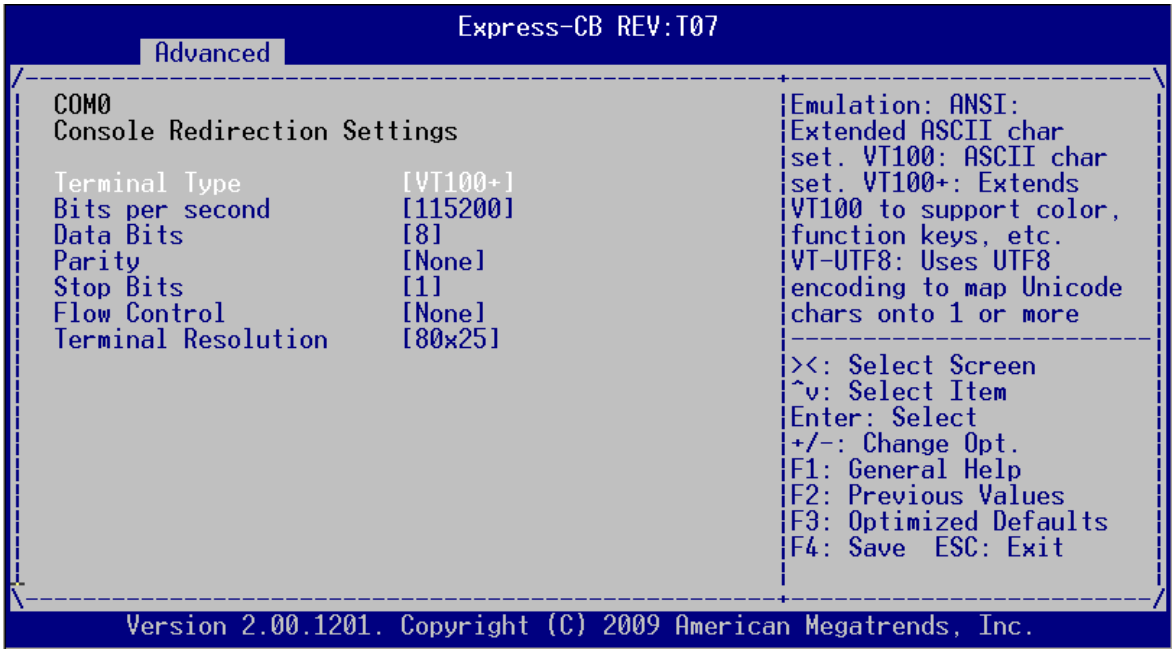


Console Redirection

Options are Enabled/Disabled.

Console Redirection Settings

The settings specify how the host computer and the remote computer will exchange data. Both computers should have the same or compatible settings.



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Console Redirection Settings (cont'd)

Terminal Type

VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. Configuration options: VT100, VT100+, VT-UTF8, ASNI.

Bits per second

Select the bits per second you want the serial port to use for console redirection. The options are 115200 ,57600 ,19200, 9600.

Data Bits

Select the data bits you want the serial port to use for console redirection. Set this value to 7 or 8.

Parity

Set this option to select parity for console redirection. The settings for this value are None, Even, Odd, Mark and Space.

Stop Bits

Stop bits indicate the end of a serial data packet. The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit. Set this value to 1 or 2.

Flow Control

Set this option to select Flow Control for console redirection. The settings for this value are None, Hardware and Software.

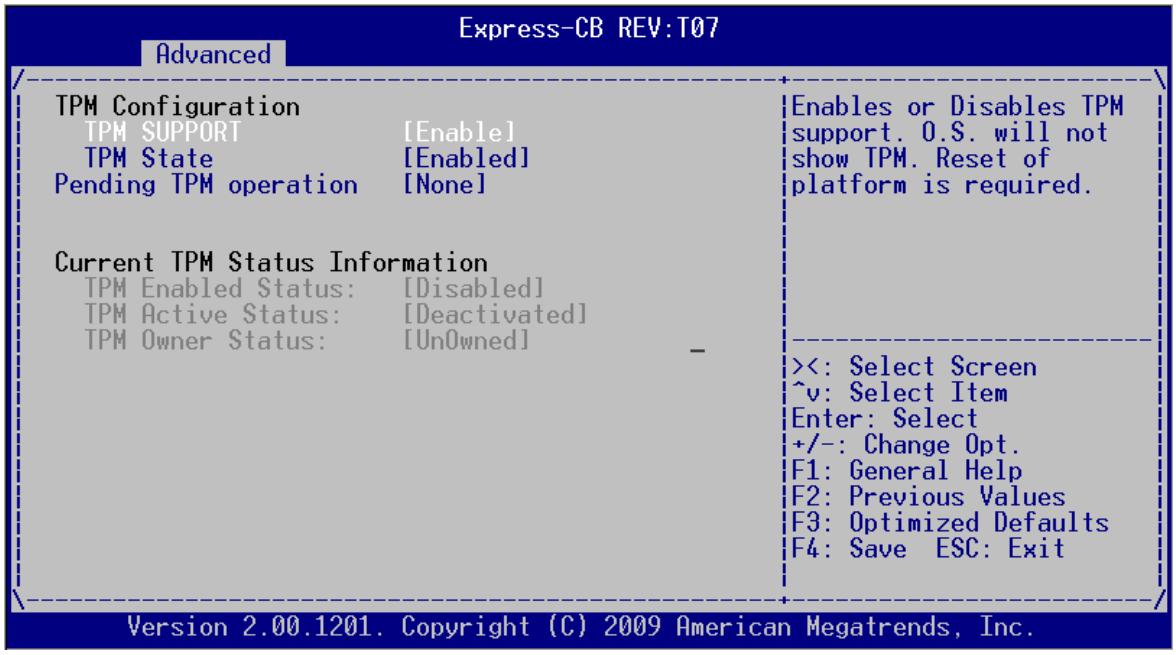
Terminal Resolution

Remote Terminal Resolution. Set this value to 80x25 or 100x31.

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8.3.12 Trusted Computing

Trusted Computing is an industry standard to make personal computers more secure through a dedicated hardware chip, called a Trusted Platform Module (TPM). This option allows you to enable or disable the TPM support.



TPM Support

Options are Enabled/Disabled.

TPM State

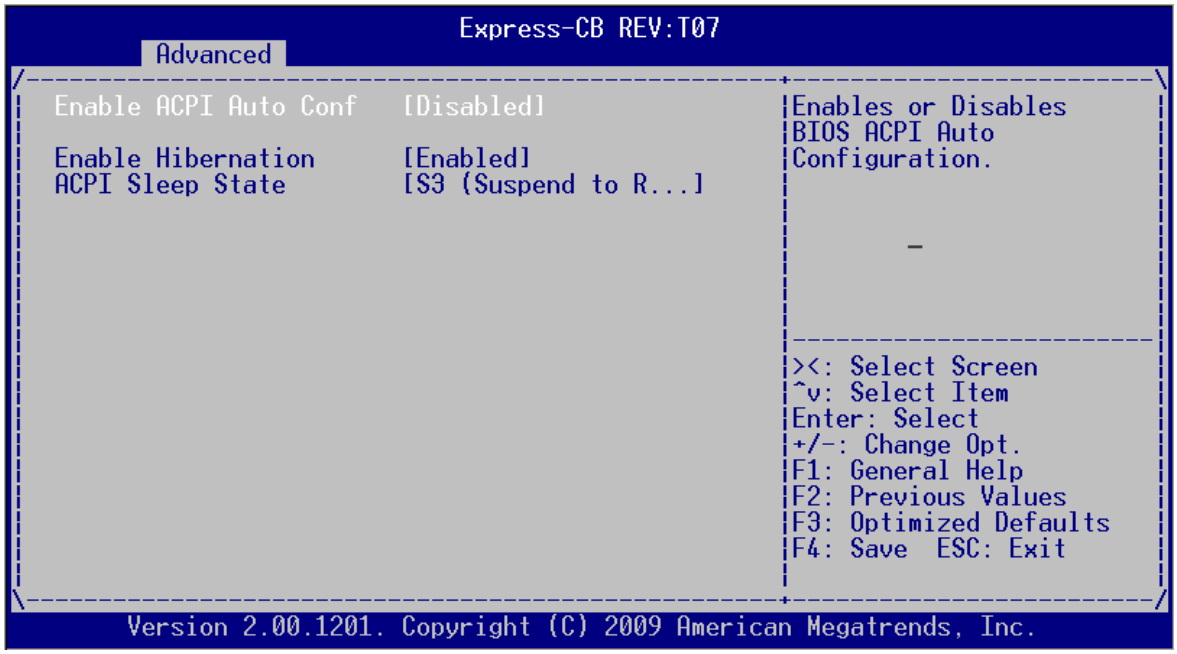
Determines whether a TPM state change requires Password Authentication. Options are Enabled/Disabled.

Pending TPM Operation

Schedule a TPM operation. The settings for this value are None, Enable Take Ownership, Disable Take Ownership, and TPM Clear.

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8.3.13 ACPI Settings



Enable ACPI Auto Configuration

BIOS ACPI Auto Configuration. Options are Enabled/Disabled.

Enable Hibernation

Options are Enabled/Disabled.

ACPI Sleep State

Select the highest ACPI sleep state the system will enter, when the Suspend button is pressed. Configuration options: S1, S3, Suspend Disable.

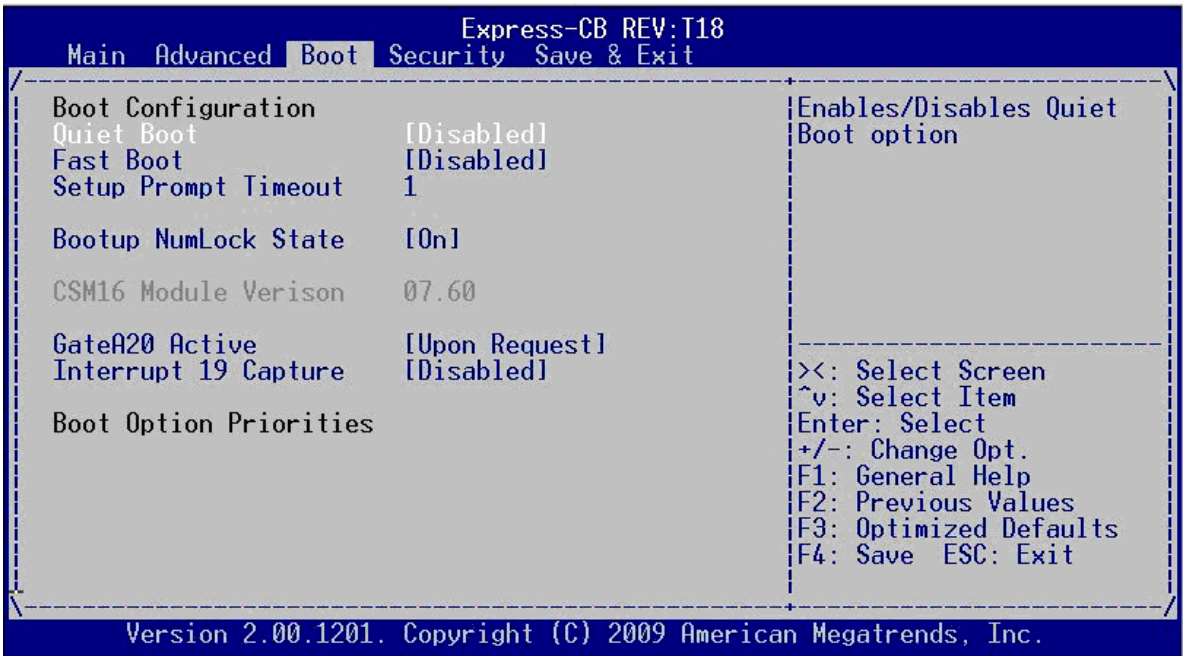
S1 (POS): Power On Suspend - Under this setting the CPU is not executing instructions, all power resources that supply system level reference of S0 are off, system memory context is maintained, devices that reference power resources that are on are on, and devices that can wake-up the system can cause the cpu to continue to execute from where it left off.

S3 (STR): Suspend to RAM - Under this setting the system enters a low power state instead of being completely shut off. This allows the computer system to boot up in a few seconds.

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8.5 Boot Configuration

Select the Boot tab from the setup screen to enter the Boot BIOS Setup screen. You can select any of Boot BIOS options by highlighting it using the < Arrow > keys. The Boot BIOS Setup screen is shown below.



Quiet Boot

Disabled - Set this value to allow the computer system to display the POST messages.
Enabled - Set this value to allow the computer system to display the OEM logo.

Fast Boot

Disabled - Set this value to allow the BIOS to perform all POST tests.
Enabled - Set this value to allow the BIOS to skip certain POST tests to boot faster.

Setup Prompt Timeout

Number of seconds to wait for setup activation key. 65535 (0xFFFF) means wait indefinitely.

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Bootup Num-Lock

Set this value to allow the Number Lock setting to be modified during boot up.
Off - This option does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard will light up when the Number Lock is engaged.
On - Set this value to allow the Number Lock on the keyboard to be enabled automatically when the computer system is boot up. This allows the immediate use of 10-keys numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard will be lit.

GateA20 Active

Upon Request - GA20 can be disabled using BIOS services. Always - do not allow disabling of GA20; this option is useful when any RT code is executed above 1MB.

Interrupt 19 Capture

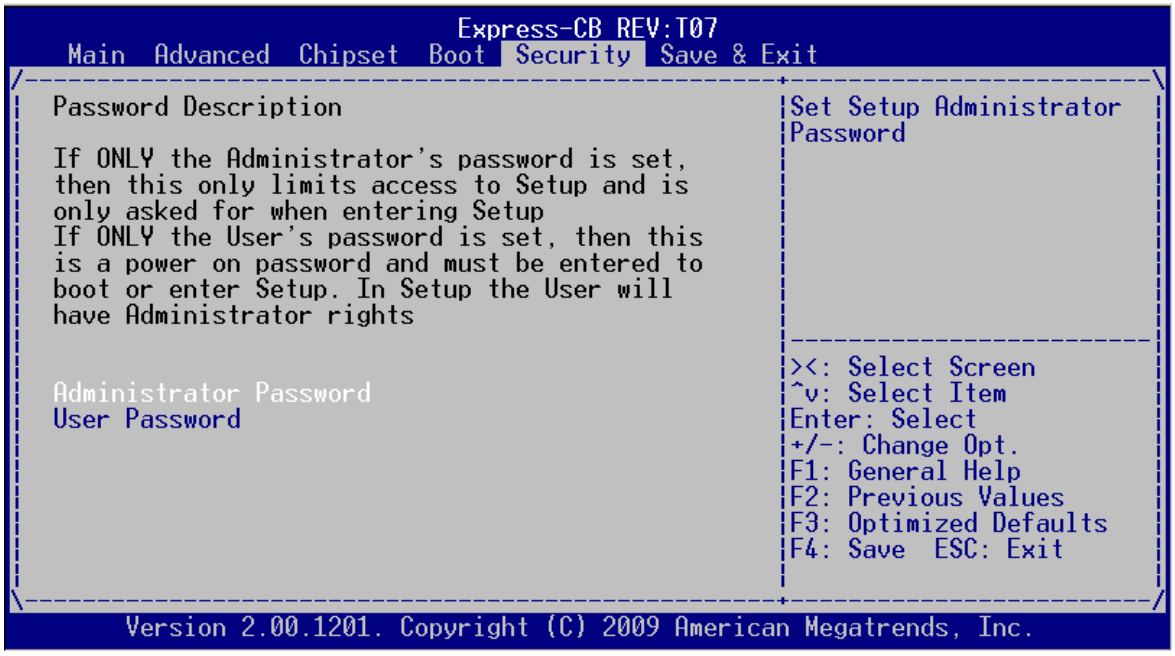
Allows option ROMs to trap Int 19. Set this value to Enabled/Disabled.

Hard Drive BBS Priorities

The boot devices are listed in groups by device type. First press <Enter> to enter the sub-menu. Then you may use the arrow keys to select the desired device, then press <+>, <-> or <PageUp>, <PageDown> key to move it up/down in the priority list. Only the first device in each device group will be available for selection in Boot Option.

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8.6 Security Setup



Administrator Password

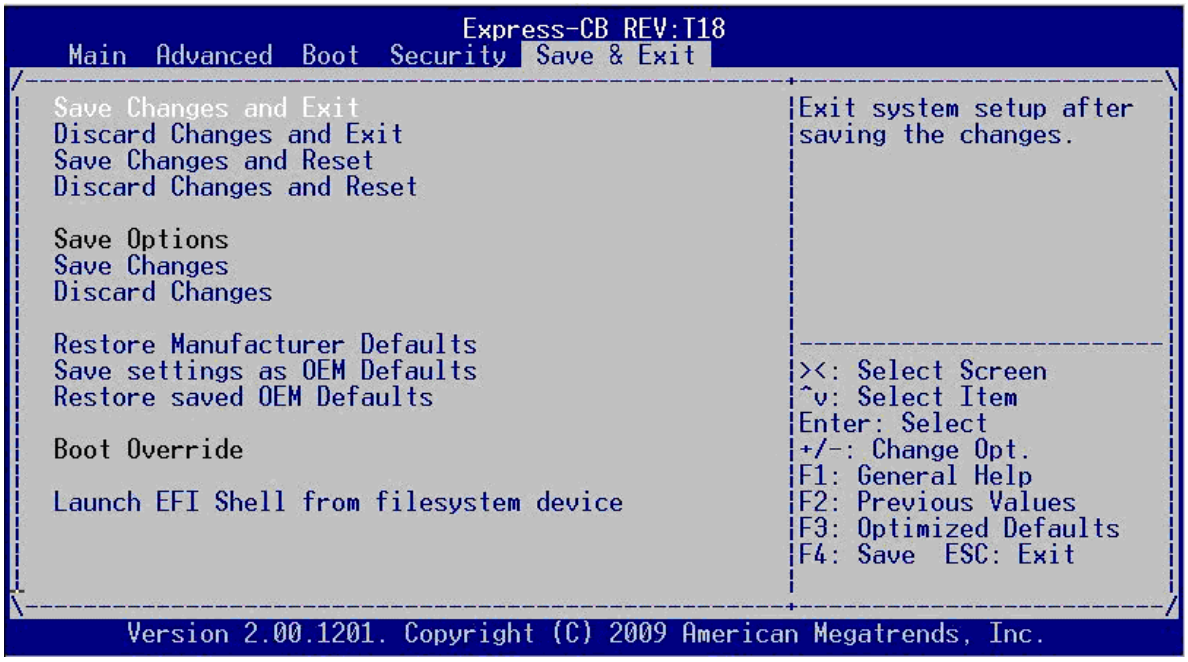
Use this option to set a password for administrators with full control of the BIOS setup utility.

User Password

Use this option to set a password for users with limited access to the BIOS setup utility.

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8.6 Save & Exit



Save Changes and Exit

When you have completed the system configuration changes, select this option to save changes and continue booting the system. New configuration parameters will take effect after the next system restart.

Discard Changes and Exit

Select this option to quit Setup without saving changes to the system configuration and continue booting.

Save Changes and Reset

Reset the system after saving the changes.

Discard Changes and Reset

Reset system setup without saving any changes.

Save Changes

Save changes made so far to any of the setup options.

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Discard Changes

Discard any unsaved changes

Restore Manufacturer Defaults

Restore standard default values for all the setup options.

Save Settings as OEM Defaults

Save the changes made so far as OEM Defaults.

Restore saved OEM Defaults

Restore the OEM Defaults to all the setup options.

Boot Override

Use the up/down arrow keys to highlight a boot device or "Launch EFI Shell" to immediately exit the BIOS Setup and boot from the selected device.

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9 BIOS Checkpoints, Beep Codes

This section of this document lists checkpoints and beep codes generated by AMIBIOS. The checkpoints defined in this document are inherent to the AMIBIOS generic core, and do not include any chipset or board specific checkpoint definitions.

Checkpoints and Beep Codes Definition

A checkpoint is either a byte or word value output to I/O port 80h. The BIOS outputs checkpoints throughout bootblock and Power-On Self Test (POST) to indicate the task the system is currently executing. Checkpoints are very useful for debugging problems that occur during the preboot process.

Beep codes are used by the BIOS to indicate a serious or fatal error. They are used when an error occurs before the system video has been initialized, and generated by the system board speaker.

Viewing BIOS Checkpoints

Viewing all checkpoints generated by the BIOS requires a checkpoint card, also referred to as a “POST Card” or “POST Diagnostic Card”. These are PCI add-in cards that show the value of I/O port 80h on a LED display.

Some computers display checkpoints in the bottom right corner of the screen during POST. This display method is limited, since it only displays checkpoints that occur after the video card has been activated.

Keep in mind that not all computers using AMIBIOS enable this feature. In most cases, a checkpoint card is the best tool for viewing AMIBIOS checkpoints.

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9.1 Status Code Ranges

Status Code Range	Description
0x01 – 0x0F	SEC Status Codes & Errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0xCF	DXE execution up to BDS
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

9.2 Standard Status Codes

SEC Status Codes

Status Code	Description
0x0	Not used
Progress Codes	
0x1	Power on. Reset type detection (soft/hard).
0x2	AP initialization before microcode loading
0x3	North Bridge initialization before microcode loading
0x4	South Bridge initialization before microcode loading
0x5	OEM initialization before microcode loading
0x6	Microcode loading
0x7	AP initialization after microcode loading
0x8	North Bridge initialization after microcode loading
0x9	South Bridge initialization after microcode loading
0xA	OEM initialization after microcode loading
0xB	Cache initialization
SEC Error Codes	
0xC – 0xD	Reserved for future AMI SEC error codes
0xE	Microcode not found
0xF	Microcode not loaded

SEC Beep Codes

None.

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PEI Status Codes

Status Code	Description
0x0	Not used
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started

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PEI Status Codes (cont'd)

PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
S3 Resume Error Codes	
0xE8	S3 Resume Failed in PEI
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

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PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
7	Reset PPI is not available
4	Recovery failed
4	S3 Resume failed

DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started

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DXE Status Codes (cont'd)

Status Code	Description
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes

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DXE Status Codes (cont'd)

DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

DXE Beep Codes

# of Beeps	Description
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
1	Invalid password
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

ACPI/ASL Status Codes

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

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9.3 OEM-Reserved Status Code Ranges

Status Code	Description
0x5	OEM SEC initialization before microcode loading
0xA	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

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Important Safety Instructions

For user safety, please read and follow all instructions, **warnings**, **cautions**, and **notes** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:

  - Turn off power and unplug any power cords/cables.

- To avoid electrical shock and/or damage to equipment:

  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.
- A Lithium-type battery may be provided for uninterrupted, backup or emergency power.



Risk of explosion if battery is replaced by an incorrect type. Dispose of used batteries according to the instructions.

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- Equipment must be serviced by authorized technicians when:

  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

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Getting Service

Contact us should you require any service or assistance.

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