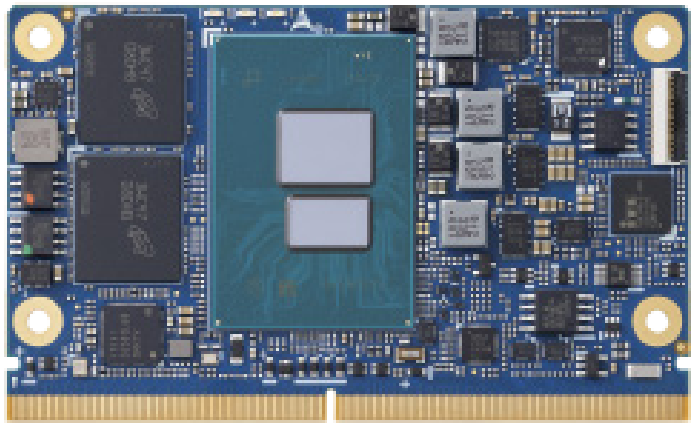
LEC-ALN/ASL

User's Guide



SMARC module

Revision:	1.8
Date:	2026-09-14
Part Number:	50M-72519-1080

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Revision History

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1.2	Introduction, specifications, block diagram, and pinout and signal descriptions updated	2025-05-27	AL
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1.8	Specifications updated	2026-09-14	AL

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Preface

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- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
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- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
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Note: This information adds clarity or specifics to text and illustrations.



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1. Introduction

1.1 LEC-ALN / ASL

ADLINK LEC-ALN / ASL is a SMARC module based on Intel Atom® x7000 series (e.g., x7425E, x7213RE) processors (formerly Alder Lake N or Amston Lake) with integrated Intel® UHD graphics and high-speed interfaces. It supports up to 16GB LPDDR5 memory and is available with rugged operating temperature range and low power envelope, making it ideal for mission-critical fanless edge computing applications that require safety and reliability at all times.

1.2 The SMARC Form Factor

The SMARC ("Smart Mobility ARChitecture") is a versatile small form factor computer-on-module definition targeting applications that require low power and high performance at low costs. Typically, under 6W, the modules often utilize ARM and other alternative low-power option CPUs, and are used in many familiar handheld devices, such as tablet computers and smart phones.

Two module sizes are defined in SMARC: 82 mm x 50 mm and 82 mm x 80 mm.

The module PCBs have 314 edge fingers that mate with a low-profile 314 pin, 0.5 mm pitch, right angle connector (the connector is sometimes identified as a 321-pin connector, with 7 pins used by the key).

SMARC modules are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE, and a single-channel LVDS display transmitter, are concentrated on the module. Modules are used with application-specific carrier boards that implement other features such as audio codecs, touch controllers, wireless devices, and more.

The modular approach allows scalability, faster time to market, and upgradability while still maintaining low costs, low power, and small physical size.

SGeT STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

SMARC module and carrier specifications are available at: https://sget.org/standards/smarc/

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2. Specifications

2.1 Core System

SoC

- 7th Gen Intel® Atom® series (formerly Alder Lake N)
  - I3-N305
  - N200
  - N97
  - N95
  - N50
  - x7425E
  - x7213E
  - x7211E

Standard embedded parts

- 7th Gen Intel® Atom® series (formerly Amston Lake)
  - x7405C
  - x7213RE
  - x7433RE
  - x7835RE
  - x7203C
  - x7211RE

Industrial grade parts

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L2 Cache

6MB

Memory

4/8/16 GB LPDDR5 at 4800 MT/s memory down type with IBECC.

2.2 Video

LEC-ALN / ASL standard display supports 4K-capable HDMI® 2.0a, 4K DP++ and single/dual-channel 24-bit LVDS.

Note: The LVDS output is derived from an eDP to LVDS bridge. As build option, the bridge can be removed.

GPU Core

Intel Gen11LP UHD Graphics

HDMI

HDMI 2.0a supporting up to 4K (4096 x 2160 at 60Hz)

LVDS

LVDS single/dual channel 24-bit at max. 1920x 1200 over eDP to LVDS bridge (removable option)

2.3 Audio

HDA audio interface (used by default).

Note: Audio codec is located on carrier.

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2.4 Dual Ethernet

Primary LAN (GbE0)

Intel® Ethernet Controller I226 Series with optional IEEE-1588 PTP (Precision Time Protocol)

Supports 2.5Gb data transfer rates, both full-duplex and half-duplex.

Secondary LAN (GbE1)

Intel® Ethernet Controller I226 Series with optional IEEE-1588 PTP (Precision Time Protocol)

Supports 2.5Gb data transfer rates, both full-duplex and half-duplex.

2.5 Expansion Busses

PCIe

4x PCI Express Gen3 x1 interfaces (configurable to one x4, two x2 or one x2 + two x1 or four x1)

SATA

1x SATA Gen3, BOM option (BOM option, replaces 1x PCIe D lane as needed)

USB

2x USB 3.1, 6x USB 2.0, no OTG support

UART

4x UART interface SER0, 2(Tx/Rx/CTS/RTS) and SER1, SER3 (Tx/Rx)

7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none)

Programmable baud rates up to 4 Mbps.



Note: The EC UART (4-wire mode) does not support auto flow control.

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CAN bus

2x CAN 2.0B only or mixed CAN 2.0B, with a data bit rate of up to 1 Mbps, via USB to CAN (removable option)

SPI

1x SPI 1x eSPI /GSPI

HDA

1x High-Definition Audio (HDA) as default

I2C

4x I2C interfaces

Supports 7-bit and 10-bit address modes

Software programmable clock frequency:

- 100 kbit/s in Standard-mode
- 400 kbit/s in Fast-mode
- 1 Mbit/s in Fast-mode Plus

GPIO

14x G

PIO with interrupt (GPIO4 used as HDA_RST# by default)

2.6 Board Controller

BMC lite for power sequence

SEMA BMC Error Code

Exception Code	Error Code
0	NOERROR
2	NO_VIN
3	NO_SDM_RESIN_N
4	NO_SDM_RESIN_N

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2.7 System Storage

eMMC

Soldered on module 32, 64, 128 GB (build option) either standard or at -40 to 85°C temperature range

Compatible with eMMC specification 4.51 and higher

2.8 SEMA® Board Management Controller

Voltage/current monitoring, boot configuration, logistics, forensic information, flat panel control, watchdog timer

2.9 Debug Header

Flat cable connector for use with optional DB-30 debug module

Provides JTAG, BMC access; UART, power test points; diagnostic LEDs, Power, Reset, Boot configuration

2.10 BIOS

Single BIOS chip, AMI Aptio V UEFI BIOS

2.11 Power

Supply Voltage

5V +/- 5%

Power Sequencing

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VDD_IN is the first power domain to be turned on by the carrier circuit during power-up. Other circuit components on the carrier, which are galvanically coupled to the module, shall not be supplied to avoid feedback. From the moment VDD_IN is stable — recognizable by VIN_PWR_BAD# de-asserted — the module takes over control of the power sequencing. As soon as the module reaches the next system state standby, CARRIER_PWR_ON signals the carrier to switch on all its standby voltages. No feedback is provided to allow the carrier to signal Power OK to the modules power state machine. When the state Runtime is reached, the module de-asserts CARRIER_STBY#. The carrier then switches on the remaining rails.

2.12 Mechanical and Environmental

Form Factor

SGET SMARC Specifications v2.1.1

Dimensions

SMARC small size module, 82mm x 50mm

Operating Temperature

Standard: 0°C to 60°C

Rugged: -40°C to 85°C (optional)

Humidity

5-90% RH operating, non-condensing

5-95% RH storage (and operating with conformal coating)

Shock and Vibration

IEC 60068-2-64 and IEC-60068-2-27, MIL-STD-202 F, Method 213B, Table 213-I, Condition A and Method 214A, Table 214-I, Condition D

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3. Block Diagram

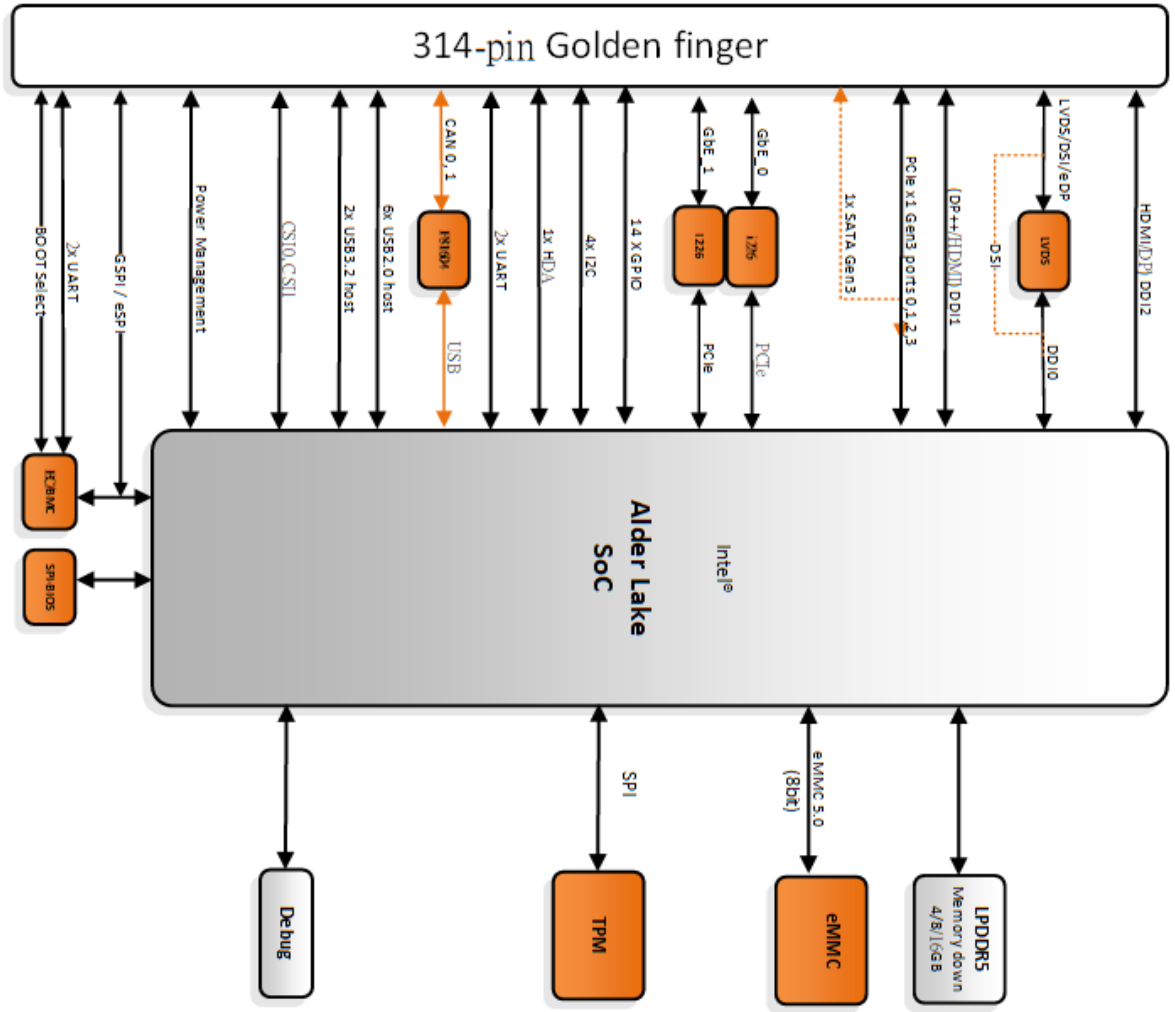


Figure 1 – Module function diagram

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4. Pinout and Signal Descriptions

4.1 Pin Summary

The below tables are a list of all signal pins on the MXM 3 connector in the standard specification of SMARC 2.1.

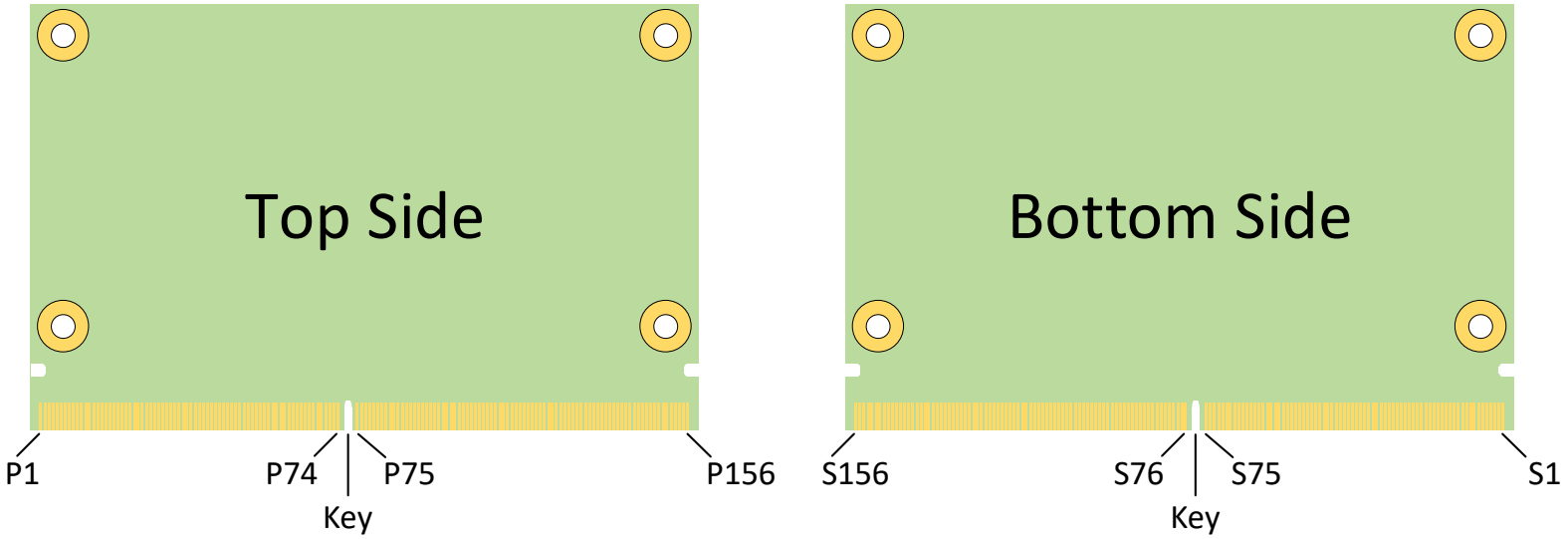


Figure 2 – Module top/bottom side pin numbering

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4.2 Signal Terminology Descriptions

Signals described in the specification but not supported on the LEC-ALN / ASL are marked with ~~STRIKETHROUGH~~.

Term	Description
I	Input to the module
O	Output from the module
O OD	Open drain output from the module
I OD	Open drain input to the module, with mandatory PU (pull up) on module
OD	Open drain
I/O	Bi-directional Input/Output
PU	PU (pull-up) resistor on module
PD	PD (pull-down) resistor on module
VDD_IN	Main power source from carrier to module
CMOS	Logic input or output
GBE MDI	Differential analog signaling for Gigabit Media Dependent Interface
LVDS DP	Low Voltage Differential Signal for DisplayPort interface
MIPI D-PHY	Low Voltage Differential Signal for MIPI CSI-2 cameras and DSI displays
MIPI D-PHY	Low Voltage Differential Signal for MIPI CSI-3 cameras
LVDS LCD	Low Voltage Differential Signal for LCD displays
LVDS PCIE	Low Voltage Differential Signal for PCIe
LVDS SATA	Low Voltage Differential Signal for SATA
TMDS HDMI	Transition Minimized Differential Signal for HDMI displays
USB	DC coupled differential signaling for traditional (non-Superspeed) USB signals
USB SS	Differential signal for SuperSpeed USB signals
USB VBUS 5V	5V tolerant input for USB VBUS detection
3.3V	3.3V Power Domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
1.8V	1.8V Power Domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
3.3Vsb	3.3V Power Domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)
1.8Vsb	1.8V Power Domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)

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4.3 Signal Description by Function

4.3.1 The First Display Interface

The first display interface is a group of 30pins that is split into a channel 0 and channel 1. The SMARC specification allows support for dual-channel LVDS ports, 2 separate single channel LVDS ports, 2 MIPI DSI ports of 4 lanes each, or 2 eDP ports 4 lanes each. A mix of different display types, such as DSI and eDP is also permitted. The tables below show which display ports are supported on this particular module.

Pin #	LVDS Name	MIPI DSI Name	eDP Name
S125	LVDS0_0+	~~DSI0_D0+~~	eDP0_TX0+
S126	LVDS0_0-	~~DSI0_D0-~~	eDP0_TX0-
S128	LVDS0_1+	~~DSI0_D1+~~	eDP0_TX1+
S129	LVDS0_1 -	~~DSI0_D1-~~	eDP0_TX1-
S131	LVDS0_2+	~~DSI0_D2+~~	eDP0_TX2+
S132	LVDS0_2-	~~DSI0_D2-~~	eDP0_TX2-
S137	LVDS0_3+	~~DSI0_D3+~~	eDP0_TX3+
S138	LVDS0_3-	~~DSI0_D3-~~	eDP0_TX3-
S134	LVDS0_CK+	~~DSI0_CLK+~~	eDP0_AUX+
S135	LVDS0_CK-	~~DSI0_CLK-~~	eDP0_AUX-
S133	LCD0_VDD_EN	~~LCD0_VDD_EN~~	LCD0_VDD_EN
S127	LCD0_BKLT_EN	~~LCD0_BKLT_EN~~	LCD0_BKLT_EN
S141	LCD0_BKLT_PWM	~~LCD0_BKLT_PWM~~	LCD0_BKLT_PWM
S144		~~DSI0_TE~~	eDP0_HPD

Pin #	LVDS Name	MIPI DSI Name	eDP Name
S111	LVDS1_0+	~~DSI1_D0+~~	~~eDP1_TX0+~~
S112	LVDS1_0-	~~DSI1_D0-~~	~~eDP1_TX0-~~
S114	LVDS1_1+	~~DSI1_D1+~~	~~eDP1_TX1+~~
S115	LVDS1_1 -	~~DSI1_D1-~~	~~eDP1_TX1-~~
S117	LVDS1_2+	~~DSI1_D2+~~	~~eDP1_TX2+~~
S118	LVDS1_2-	~~DSI1_D2-~~	~~eDP1_TX2-~~
S120	LVDS1_3+	~~DSI1_D3+~~	~~eDP1_TX3+~~
S121	LVDS1_3-	~~DSI1_D3-~~	~~eDP1_TX3-~~
S108	LVDS1_CK+	~~DSI1_CLK+~~	~~eDP1_AUX+~~
S109	LVDS1_CK-	~~DSI1_CLK-~~	~~eDP1_AUX-~~
S116	LCD1_VDD_EN	~~LCD1_VDD_EN~~	~~LCD1_VDD_EN~~
S107	LCD1_BKLT_EN	~~LCD1_BKLT_EN~~	~~LCD1_BKLT_EN~~
S122	LCD1_BKLT_PWM	~~LCD1_BKLT_PWM~~	~~LCD1_BKLT_PWM~~
S113		~~DSI1_TE~~	~~eDP1_HPD~~

S139	I2C_LCD_CK	~~I2C_LCD_CK~~	I2C_LCD_CK
S140	I2C_LCD_DAT	~~I2C_LCD_DAT~~	I2C_LCD_DAT

Note:

1. LVDS0/LVDS1 are standard supported through eDP to LVDS bridge on the module
2. eDP can be used by build option, disabling the LVDS0 ports.

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4.3.1.1 LVDS0/LVDS1 Mode

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
LVDS0_0+ LVDS0_0- LVDS0_1+ LVDS0_1 - LVDS0_2+ LVDS0_2- LVDS0_3+ LVDS0_3-	S125 S126 S128 S129 S131 S132 S137 S138	Primary LVDS Channel Differential Pair Data Lines	O LVDS		Runtime		A 100ohm differential termination across the differential pairs at the endpoint of the signal path, usually on the display assembly.
LVDS0_CK+ LVDS0_CK-	S134 S135	Primary LVDS Channel Differential Pair Clock Lines	O LVDS		Runtime		A 100-ohm differential termination across the differential pair at the endpoint of the signal path, usually on the display assembly.
LCD0_VDD_EN	S133	Primary LVDS Channel Power Enable	O CMOS	1.8V	Runtime		Active high
LCD0_BKLT_EN	S127	Primary LVDS Channel Backlight Enable	O CMOS	1.8V	Runtime		Active high
LCD0_BKLT_PWM	S141	Primary LVDS Channel Brightness Control	O CMOS	1.8V	Runtime		Through pulse width modulation (PWM)
LVDS1_0+ LVDS1_0- LVDS1_1+ LVDS1_1 - LVDS1_2+ LVDS1_2- LVDS1_3+ LVDS1_3-	S111 S112 S114 S115 S117 S118 S120 S121	Secondary LVDS Channel Differential Pair Data Lines	O LVDS		Runtime		A 100-ohm differential termination across the differential pairs at the endpoint of the signal path, usually on the display assembly.
LVDS1_CK+ LVDS1_CK-	S108 S109	Secondary LVDS Channel Differential Pair Clock Lines	O LVDS		Runtime		A 100-ohm differential termination across the differential pair at the endpoint of the signal path, usually on the display assembly.
~~LCD1_VDD_EN~~	~~S116~~	~~Secondary LVDS Channel Power Enable~~	~~O CMOS~~	~~1.8V~~	~~Runtime~~	-	~~Active high~~ ~~Only in use, when two separate LVDS ports are supported, please check Module user manual~~

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~~LCD1_BKLT_EN~~	~~S107~~	~~Secondary LVDS Channel Backlight Enable~~	~~O CMOS~~	~~1.8V~~	~~Runtime~~	-	~~Active high Only in use, when two separate LVDS ports are supported, please check Module user manual~~
~~LCD1_BKLT_PWM~~	~~S122~~	~~Secondary LVDS Channel Brightness Control~~	~~O CMOS~~	~~1.8V~~	~~Runtime~~	-	~~Through pulse width modulation (PWM) only in use, when two separate LVDS ports are supported, please check Module user manual~~
I2C_LCD_DAT	S140	DDC data line used for flat panel detection and control	I/O OD CMOS	1.8V	Runtime	PU 2k2	Possible conflict if two LVDS panels are used
I2C_LCD_CK	S139	DDC clock line used for flat panel detection and control	O OD CMOS	1.8V	Runtime	PU 2k2	Possible conflict if two LVDS panels are used

4.3.1.2 eDP Mode (Build Option)

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
eDP0_TX0+ eDP0_TX0- eDP0_TX1+ eDP0_TX1- eDP0_TX2+ eDP0_TX2- eDP0_TX3+ eDP0_TX3-	S125 S126 S128 S129 S131 S132 S137 S138	Primary 4-Lane eDP Differential Pair Data Lines	O DP		Runtime		AC coupled off Module 100 nF DC blocking capacitors ***shall*** be placed on the Carrier.
eDP0_AUX+ eDP0_AUX-	S134 S135	Primary Bidirectional Channel used for Link Management and Device Control	I/O DP		Runtime		AC coupled off module
LCD0_VDD_EN	S133	Primary Panel Power Enable	O CMOS	1.8V	Runtime		Active high
LCD0_BKLT_EN	S127	Primary Panel Backlight Enable	O CMOS	1.8V	Runtime		Active high
LCD0_BKLT_PWM	S141	Primary Panel Brightness Control	O CMOS	1.8V	Runtime		Through pulse width modulation (PWM)
eDP0_HPD	S144	Detection of Hot Plug / Unplug of Primary eDP Display and Notification of the Link Layer	I CMOS	1.8V	Runtime	PD 1M	Module must tolerate high level in stand-by mode

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4.3.2 Second Display Interface

Pin #	HDMI signal names	DP++ signal names
P92 P93 P95 P96 P98 P99	HDMI_D2+ HDMI_D2- HDMI_D1+ HDMI_D1- HDMI_D0+ HDMI_D0-	DP1_LANE0+ DP1_LANE0- DP1_LANE1+ DP1_LANE1- DP1_LANE2+ DP1_LANE2-
P101 P102	HDMI_CK+ HDMI_CK-	DP1_LANE3+ DP1_LANE3-
S105	HDMI_CTRL_CK	DP1_AUX+
S106	HDMI_CTRL_DAT	DP1_AUX-
P104	HDMI_HPD	DP1_HPD

4.3.2.1 HDMI

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
HDMI_D2+ HDMI_D2- HDMI_D1+ HDMI_D1- HDMI_D0+ HDMI_D0-	P92 P93 P95 P96 P98 P99	HDMI port, differential pair data lines	O TMDS HDMI		Runtime		AC coupled off module
HDMI_CK+ HDMI_CK-	P101 P102	HDMI port, differential pair clock lines	O TMDS HDMI		Runtime		AC coupled off module

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HDMI_CTRL_CK	P105	I2C_CLK line dedicated to HDMI	O OD COMS	1.8V	Runtime	PU 2.2K	A level shifter FET and a 5V PU resistor ***shall*** be placed between the module and the HDMI connector. A stronger pull-up is demanded on the carrier board. The pull-ups may be part of an integrated HDMI ESD protection and control-line level shift device, such as the Texas Instruments TPD12S016. If discrete carrier pull-ups are used, the value depends on the individual carrier board implementation.
HDMI_CTRL_DAT	P106	I2C_DAT line dedicated to HDMI	I/O OD COMS	1.8V	Runtime	PU 2.2K	A level shifter FET and a 5V PU resistor ***shall*** be placed between the module and the HDMI connector. A stronger pull-up is demanded on the carrier board. The pull-ups may be part of an integrated HDMI ESD protection and control-line level shift device, such as the Texas Instruments TPD12S016. If discrete carrier pull-ups are used, the value depends on the individual carrier board implementation.
HDMI_HPD	P104	HDMI Hot plug active high detection signal serves as an interrupt request	I CMOS	1.8V	runtime	PD 100K	A module must tolerate high voltage levels while in stand-by mode

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4.3.3 MIPI Camera Support

4.3.3.1 MIPI CSI0

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CSI0_RX0+ CSI0_RX0- CSI0_RX1+ CSI0_RX1-	S11 S12 S14 S15	CSI0 differential input (point to point)	I D-PHY / I M-PHY		Runtime		
CSI0_CK+ CSI0_CK-	S8 S9	CSI0 differential clock input (point to point)	I D-PHY		Runtime		
I2C_CAM0_DAT /CSI0_TX-	S7	I2C data for serial camera data support link or differential data lane	I/O OD CMOS / O M-PHY	1.8V	Runtime	PU 4.7K	MIPI-CSI 2.0 uses I2C_CAM0_DAT which requires PU MIPI-CSI 3.0 uses CSI0_TX-, no PU required
I2C_CAM0_CK / CSI0_TX+	S5	I2C clock for serial camera data support link or differential data lane	O OD CMOS / O M-PHY	1.8V	Runtime	PU 4.7K	MIPI-CSI 2.0 uses I2C_CAM0_CK which requires PU MIPI-CSI 3.0 uses CSI0_TX+, no PU required
CAM0_PWR# / GPIO0	P108	Camera 0 Power Enable, active low output.	O CMOS	1.8V	Runtime		Shared with GPIO0
CAM0_RST# / GPIO2	P110	Camera 0 reset, active low output	O CMOS	1.8V	Runtime		Shared with GPIO2
CAM_MCK	S6	Master clock output	O CMOS	1.8V	Runtime		

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4.3.3.2 CSI1 (4 Lanes)

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CSI1_RX0+ CSI1_RX0- CSI1_RX1+ CSI1_RX1- CSI1_RX2+ CSI1_RX2- CSI1_RX3+ CSI1_RX3-	P7 P8 P10 P11 P13 P14 P16 P17	CSI1 differential input	I LVDS D-PHY / I LVDS M-PHY		Runtime		
CSI1_CK+ CSI1_CK-	P3 P4	CSI1 differential clock input (point to point)	I LVDS D-PHY		Runtime		
I2C_CAM1_DAT / CSI1_TX-	S2	I2C data for serial camera data support link or differential data lane	I/O OD CMOS / O LVDS M-PHY	1.8V	Runtime	PU 4.7K	MIPI-CSI 2.0 uses I2C_CAM0_DAT which requires PU MIPI-CSI 3.0 uses CSI0_TX-, no PU required
I2C_CAM1_CK / CSI1_TX+	S1	I2C clock for serial camera data support link or differential data lane	O OD CMOS / O LVDS M-PHY	1.8V	Runtime	PU 4.7K	MIPI-CSI 2.0 uses I2C_CAM0_CK which requires PU MIPI-CSI 3.0 uses CSI0_TX+, no PU required
CAM1_PWR# / GPIO1	P109	Camera 1 Power Enable, active low output.	O CMOS	1.8V	Runtime		Shared with GPIO1
CAM1_RST# / GPIO3	P111	Camera 1 reset, active low output	O CMOS	1.8V	Runtime		Shared with GPIO 3
CAM_MCK	S6	Master clock output	O CMOS	1.8V	Runtime		

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4.3.4 HDA (Audio)

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
HDA_SYNC / I2S2_LRCK	S50	High-definition audio sample synchronization clock to codec	I/O CMOS	1.8V / 1.5V	Runtime		LEC-ALN does not support 1.5V for HDA. Please ensure that the audio codec used is compatible with 1.8V I/O voltage. This specification does not account for mismatched voltage levels, and only 1.8V-compatible audio codecs should be used.
HDA_SDO / I2S2_SDOUT	S51	High-definition audio data out to codec	O CMOS	1.8V / 1.5V	Runtime		
HDA_SDI / I2S2_SDIN	S52	High-definition audio data in from codec	I/O CMOS	1.8V / 1.5V	Runtime		
HDA_CK / I2S2_CK	S53	High-definition audio clock to codec	O CMOS	1.8V / 1.5V	Runtime		
HDA_RST# / GPIO4	P112	High-definition audio reset output to codec, low active.	O CMOS	1.8V / 1.5V	Runtime		

Note: The support for I2S1 signalling pins has been removed after the SMARC 2.0 specification update.

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4.3.5 USB Ports

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
USB0+ USB0-	P60 P61	USB differential data pairs for port 0	I/O USB	USB	Standby		
USB0_EN_OC#	P62	USB over-current sense for port 0	I OD CMOS	3.3Vsb / 3.3V	Standby	PU 10K	Pulled low by the module OD driver to disable the USB0 power. Pulled low by the carrier OD driver to indicate an over-current situation.
~~USB0_VBUS_DET~~	~~P63~~	~~USB port 0 host power detection, when this port is used as a device.~~	~~I USB VBUS 5V~~	~~USB VBUS 5V~~	~~Standby~~		Can be connected to a USB client port VBUS pin
~~USB0_OTG_ID~~	~~P64~~	~~Input pin to announce OTG device insertion on USB 2.0 port~~	~~I CMOS~~	~~3.3Vsb / 3.3V~~	~~Standby~~		
USB1+ USB1-	P65 P66	USB differential data pairs for port 1	I/O USB	USB	Standby		
USB1_EN_OC#	P67	USB over-current sense for port 1	I OD CMOS	3.3Vsb / 3.3V	Standby	PU 10K	Pulled low by the module OD driver to disable the USB0 power. Pulled low by the carrier OD driver to indicate an over-current situation.
USB2+ USB2-	P69 P70	USB differential data pairs for port 2	I/O USB	USB	Standby		
USB2_SSRX+ USB2_SSRX-	S74 S75	Receive signal differential pairs for SuperSpeed on port 2	I USB SS	USB SS	Standby		Coupling caps for the RX pairs are on the USB Device
USB2_SSTX+ USB2_SSTX-	S71 S72	Transmit signal differential pairs for SuperSpeed on port 2	O USB SS	USB SS	Standby		Coupling caps for the TX pairs are on the Module
USB2_EN_OC#	P71	USB over-current sense for port 2	I OD CMOS	3.3Vsb / 3.3V	Standby	PU 10K	Pulled low by the module OD driver to disable the USB0 power. Pulled low by the carrier OD driver to indicate an over-current situation.
USB3+ USB3-	S68 S69	USB differential data pairs for port 3	I/O USB	USB	Standby		
USB3_SSRX+ USB3_SSRX-	S65 S66	Receive signal differential pairs for SuperSpeed on port 3	I USB SS	USB SS	Standby		Coupling caps for the RX pairs are on the USB Device

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USB3_SSTX+ USB3_SSTX-	S62 S63	Transmit signal differential pairs for SuperSpeed on port 3	O USB SS	USB SS	Standby		Coupling caps for the TX pairs are on the Module
USB3_EN_OC#	P74	USB over-current sense for port 3	I OD CMOS	3.3Vsb / 3.3V	Standby	PU 10K	Pulled low by the module OD driver to disable the USB0 power. Pulled low by the carrier OD driver to indicate an over-current situation.
~~USB3_VBUS_DET~~	~~S37~~	~~USB port 3 host power detection, when this port is used as a device.~~	~~I USB VBUS 5V~~	~~USB VBUS 5V~~	~~Standby~~		
~~USB3_OTG_ID~~	~~S104~~	~~Input pin to announce OTG device insertion on USB 3.0 port~~	~~I CMOS~~	~~3.3Vsb / 3.3V~~	~~Standby~~		
USB4+ USB4-	S35 S36	USB differential data pairs for port 4	I/O USB	USB	Standby		
USB4_EN_OC#	P76	USB over-current sense for port 4	I OD CMOS	3.3Vsb / 3.3V	Standby	PU 10K	Pulled low by the module OD driver to disable the USB0 power. Pulled low by the carrier OD driver to indicate an over-current situation.
USB5+ USB5-	S59 S60	USB differential data pairs for port 5	I/O USB	USB	Standby		
USB5_EN_OC#	S55	USB over-current sense for port 5	I OD CMOS	3.3Vsb / 3.3V	Standby	PU 10K	Pulled low by the module OD driver to disable the USB0 power. Pulled low by the carrier OD driver to indicate an over-current situation.

Note: All USB connections are directly from SoC, there is no support for OTG.

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4.3.6 PCIe Ports

The module supports 4x PCIe Gen 3.0 ports. Refer to the table below for port details.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
PCIE_A_TX+ PCIE_A_TX-	P89 P90	Differential PCIe link A transmit data pair	O LVDS PCIE		Runtime		Series AC coupled on the module
PCIE_A_RX+ PCIE_A_RX-	P86 P87	Differential PCIe link A receive data pair	I LVDS PCIE		Runtime		Series AC coupled off the module
PCIE_A_REFCK+ PCIE_A_REFCK-	P83 P84	Differential PCIe Link A reference clock output	O LVDS PCIE		Runtime		
PCIE_A_RST#	P75	PCIe Port A reset output	O CMOS	3.3V	Runtime		
PCIE_A_CKREQ#	P78	PCIe Port A clock request	I OD CMOS	3.3V	Runtime	PU 10K	Can be used for power saving mode on PCIe - Pulled up or terminated on the module
PCIE_B_TX+ PCIE_B_TX-	S90 S91	Differential PCIe link B transmit data pair	O LVDS PCIE		Runtime		Series AC coupled on module
PCIE_B_RX+ PCIE_B_RX-	S87 S88	Differential PCIe link B receive data pair	I LVDS PCIE		Runtime		Series AC coupled off module
PCIE_B_REFCK+ PCIE_B_REFCK-	S84 S85	Differential PCIe Link B reference clock output	O LVDS PCIE		Runtime		
PCIE_B_RST#	S76	PCIe Port B reset output	O CMOS	3.3V	Runtime		
PCIE_B_CKREQ#	P77	PCIe Port B clock request	I OD CMOS	3.3V	Runtime	PU 10K	Can be used for power saving mode on PCIe - Pulled up or terminated on the module
PCIE_C_TX+ PCIE_C_TX-	S81 S82	Differential PCIe link C transmit data pair	O LVDS PCIE		Runtime		Series AC coupled on the module
PCIE_C_RX+ PCIE_C_RX-	S78 S79	Differential PCIe link C receive data pair	I LVDS PCIE		Runtime		Series AC coupled off the module
PCIE_C_REFCK+ PCIE_C_REFCK-	P80 P81	Differential PCIe Link C reference clock output	O LVDS PCIE		Runtime		
PCIE_C_RST#	S77	PCIe Port C reset output	O CMOS	3.3V	Runtime		

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PCIE_D_TX+ PCIE_D_TX-	S29 S30	Differential PCIe link D transmit data pair	O LVDS PCIE		Runtime		Series AC coupled on the module
PCIE_D_RX+ PCIE_D_RX-	S32 S33	Differential PCIe link D receive data pair	I LVDS PCIE		Runtime		Series AC coupled off the module
PCIE_WAKE#	S146	PCIe wake up interrupt to host – common to PCIe links A, B, C, D	I OD CMOS	3.3V	Standby	PU 1K	

4.3.7 SATA Gen 3 Ports

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SATA0_TX+ SATA0_TX-	P48 P49	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Runtime		Series AC coupled on the module 10 nF
SATA0_RX+ SATA0_RX-	P51 P52	Serial ATA channel 0, Receive Input differential pair.	I SATA		Runtime		Series AC coupled on the module 10 nF
SATA_ACT#	S54	SATA activity indicator	O OD CMOS	3.3V	Runtime		Shall be able to sink 24mA or more carrier LED current

Note: SATA is a BIOS option that reduces the available PCIe ports to 3 lanes if enabled.

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4.3.8 LAN Ports

4.3.8.1 First LAN Port

The first LAN port is derived from the PCIe-connected I226 Ethernet controller.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	P30 P29 P27 P26 P24 P23 P20 P19	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations	I/O GBE MDI		Standby		Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: 1000 / 100 / 10 MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-
GBE0_LINK100#	P21	Link Speed Indication LED for GBE0 10/100Mbps	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more carrier LED current [1]
GBE0_LINK1000#	P22	Link Speed Indication LED for GBE0 1000Mbps	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more carrier LED current [1]
GBE0_LINK_ACT#	P25	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more carrier LED current [1]
GBE0_CTREF	P28	Center -Tap reference voltage for Carrier board Ethernet magnetic (if required by the Module GBE PHY)	Analog	0 to 3.3V max	Standby		
GBE0_SDP	P6	IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol)	IO CMOS	3.3V	Standby		

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4.3.8.2 Second LAN Port

The second LAN port is derived from the PCIe-connected I226 Ethernet controller.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GBE1_MDI0+ GBE1_MDI0- GBE1_MDI1+ GBE1_MDI1- GBE1_MDI2+ GBE1_MDI2- GBE1_MDI3+ GBE1_MDI3-	S17 S18 S20 S21 S23 S24 S26 S27	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations	I/IO GBE MDI		Standby		Gigabit Ethernet Controller 1: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: 1000 / 100 / 10 MDI[0]+/- B1_DA+/- / TX+/- / TX+/- MDI[1]+/- B1_DB+/- / RX+/- / RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-
GBE1_LINK100#	S19	Link Speed Indication LED for GBE1 10/100Mbps	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more Carrier LED current [1]
GBE1_LINK1000#	S22	Link Speed Indication LED for GBE1 1000Mbps	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more Carrier LED current [1]
GBE1_LINK_ACT#	S31	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity	O OD CMOS	3.3V	Standby		Shall be able to sink 24mA or more Carrier LED current [1]
GBE1_CTREF	S28	Center-Tap reference voltage for Carrier board Ethernet magnetic (if required by the Module GBE PHY)	Analog	0 to 3.3V max	Standby		
GBE1_SDP	P5	IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol)	IO CMOS	3.3V	Standby		

Note:
1. Both LAN interfaces use a PCIe connected Intel® Ethernet Controller I226 Series.
2. LAN LEDs are inactive when the LAN transfer rate is 2.5Gb.

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4.3.9 SPI & ESPI

4.3.9.1 SPI0

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SPI0_CS0#	P43	SPI0 Master Chip Select 0	O CMOS	1.8V	Standby		This signal can be used to select carrier SPI as boot device
SPI0_CS1#	P31	SPI0 Master Chip Select 1	O CMOS	1.8V	Standby		
SPI0_CK	P44	SPI0 Clock	O CMOS	1.8V	Standby		
SPI0_DIN	P45	SPI0 Master input / Slave output	I CMOS	1.8V	Standby		Also referred to as MISO
SPI0_DO	P46	SPI0 Master output / Slave input	O CMOS	1.8V	Standby		Also referred to as MOSI

~~SPI1_CS0#~~	~~P54~~	~~SPI1 Master Chip Select 0~~	~~O CMOS~~	~~1.8V~~	~~Standby~~	-	See ESPI
~~SPI1_CS1#~~	~~P55~~	~~SPI1 Master Chip Select 1~~	~~O CMOS~~	~~1.8V~~	~~Standby~~	-	See ESPI
~~SPI1_CK~~	~~P56~~	~~SPI1 Clock~~	~~O CMOS~~	~~1.8V~~	~~Standby~~	-	See ESPI
~~SPI1_DIN~~	~~P57~~	~~SPI1 Master input / Slave output~~	~~I CMOS~~	~~1.8V~~	~~Standby~~	-	See ESPI
~~SPI1_DO~~	~~P58~~	~~SPI1 Master output / Slave input~~	~~O CMOS~~	~~1.8V~~	~~Standby~~	-	See ESPI

Note: SPI0 is free to use on the carrier but only supports one device through CS0.

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4.3.9.2 ESPI

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
ESPI_CS0#	P54	ESPI1 Master Chip Select 0	O CMOS	1.8V	Standby		
ESPI_CK	P56	ESPI Master Clock Output	O CMOS	1.8V	Standby		
ESPI_RESET#	S58	ESPI Reset	O CMOS	1.8V	Standby		Reset the eSPI interface for both master and slaves. eSPI Reset# is typically driven from eSPI master to eSPI slaves
ESPI_ALERT0# ESPI_ALERT1#	S43 S44	ESPI ALERT	I OD CMOS	1.8V	Standby		This pin is used by eSPI slave to request service from eSPI.master.Alert# is an open-drain output from the slave. This pin is optional for Single Master-Single Slave configuration where I/O[1] can be used to signal the Alert event.
ESPI_IO_0 ESPI_IO_1 ESPI_IO_2 ESPI_IO_3	P58 P57 S56 S57	ESPI Master Data Input / Output.	I/O CMOS	1.8V	Standby		ESPI_IO_0 can also be used as SPI1_DO (MOSI) ESPI_IO_1 can also be used as SPI1_DIN (MISO) In Single I/O mode, ESPI_IO_0 is the eSPI master output / eSPI slave input (MOSI) whereas ESPI_IO_1 is the SPI master input / eSPI slave output (MISO).

Note: eSPI / GSPI can be switched by zero Ohm resistors (BOM option).

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4.4 General Purpose I2C

The SMARC specification supports a total of 6 different I2C busses on its pinout. Most of these busses are designated for specific functions such as I2C for camera management, I2C for EDID on HDMI, LVDS panels, or I2C for PMIC. Only one I2C bus is marked as General purpose.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
I2C_GP_DAT	S49	General purpose I2C data signal	I/O OD CMOS	1.8V	Runtime	PU 2k2	
I2C_GP_CK	S48	General purpose I2C clock signal	O OD CMOS	1.8V	Runtime	PU 2k2	

Most of the other I2C busses are described in their designated function tables rather than in a combined list.

Below is an overview of all I2C busses and their locations.

Name	Pin #	Description	Location
I2C_LCD_DAT	S140	DDC data line used for flat panel detection and control	LVDS / DSI / eDP tables
I2C_LCD_CK	S139	DDC clock line used for flat panel detection and control	LVDS / DSI / eDP tables
HDMI_CTRL_CK	P105	I2C_CLK line dedicated to HDMI	HDMI table
HDMI_CTRL_DAT	P106	I2C_DAT line dedicated to HDMI	HDMI table
I2C_CAM0_DAT	S7	I2C data for serial camera data support link	MIPI CSI table
I2C_CAM0_CK	S5	I2C clock for serial camera data support link	MIPI CSI table
I2C_CAM1_DAT	S2	I2C data for serial camera data support link	MIPI CSI table
I2C_CAM1_CK	S1	I2C clock for serial camera data support link	MIPI CSI table
I2C_PM_DAT	P122	Power management I2C bus DATA (SMBus for x86)	Power and System Management
I2C_PM_CK	P121	Power management I2C bus CLK (SMBus for x86)	Power and System Management
I2C_GP_DAT	S49	General purpose I2C data signal	General purpose I2C
I2C_GP_CK	S48	General purpose I2C clock signal	General purpose I2C

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4.4.1 GPIO

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GPIO0 / CAM0_PWR#	P108	General purpose I/O pin 0.	I/O CMOS	1.8V	Runtime	PU 470K	Default use is GPIO0, alternative use is Camera 0 Power Enable - active low, through DTS
GPIO1 / CAM1_PWR#	P109	General purpose I/O pin 1.	I/O CMOS	1.8V	Runtime	PU 470K	Default use is GPIO1 alternative use is Camera 1 Power Enable - active low, through DTS
GPIO2 / CAM0_RST#	P110	General purpose I/O pin 2.	I/O CMOS	1.8V	Runtime	PU 470K	Default use is GPIO2, alternative use is Camera 0 Reset - active low, through DTS
GPIO3 / CAM1_RST#	P111	General purpose I/O pin 3.	I/O CMOS	1.8V	Runtime	PU 470K	Default use is GPIO3, alternative use is Camera 1 Reset - active low, through DTS
~~GPIO4~~ / HDA_RST#	P112	General purpose I/O pin 4.	I/O CMOS	1.8V	Runtime	PU 470K	GPIO 4 support requires BOM change
GPIO5 / ~~PWM_OUT~~	P113	General purpose I/O pin 5.	I/O CMOS	1.8V	Runtime	PU 470K	
GPIO6	P114	General purpose I/O pin 6.	I/O CMOS	1.8V	Runtime	PU 470K	
GPIO7	P115	General purpose I/O pin 7.	I/O CMOS	1.8V	Runtime	PU 470K	
GPIO8	P116	General purpose I/O pin 8.	I/O CMOS	1.8V	Runtime	PU 470K	
GPIO9	P117	General purpose I/O pin 9.	I/O CMOS	1.8V	Runtime	PU 470K	
GPIO10	P118	General purpose I/O pin 10.	I/O CMOS	1.8V	Runtime	PU 470K	
GPIO11	P119	General purpose I/O pin 11.	I/O CMOS	1.8V	Runtime	PU 470K	
GPIO12	S142	General purpose I/O pin 12	I/O CMOS	1.8V	Runtime	PU 470K	
GPIO13	S123	General purpose I/O pin 13	I/O CMOS	1.8V	Runtime	PU 470K	

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4.4.2 UART

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SER0_TX	P129	Asynchronous serial data output port 0	O CMOS	1.8V	Runtime		
SER0_RX	P130	Asynchronous serial data input port 0	I CMOS	1.8V	Runtime		PU 100K
SER0_RTS#	P131	"Request to Send" handshake line for port 0	O CMOS	1.8V	Runtime		
SER0_CTS#	P132	"Clear to Send" handshake line for port 0	I CMOS	1.8V	Runtime		PU 100K
SER1_TX	P134	Asynchronous serial data output port 1	O CMOS	1.8V	Runtime		
SER1_RX	P135	Asynchronous serial data input port 1	I CMOS	1.8V	Runtime		PU 100K
SER2_TX	P136	Asynchronous serial data output port 2	O CMOS	1.8V	Runtime		
SER2_RX	P137	Asynchronous serial data input port 2	I CMOS	1.8V	Runtime		PU 100K
SER2_RTS#	P138	"Request to Send" handshake line for port 2	O CMOS	1.8V	Runtime		
SER2_CTS#	P139	"Clear to Send" handshake line for port 2	I CMOS	1.8V	Runtime		PU 100K
SER3_TX	P140	Asynchronous serial data output port 3	O CMOS	1.8V	Runtime		
SER3_RX	P141	Asynchronous serial data input port 3	I CMOS	1.8V	Runtime		PU 100K

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4.4.3 CAN bus

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CAN0_TX	P143	CAN port 0 Transmit output	O CMOS	1.8V	Runtime		supported on Linux and windows
CAN0_RX	P144	CAN port 0 Receive input	I CMOS	1.8V	Runtime		supported on Linux and windows
							supported on Linux and windows
CAN1_TX	P145	CAN port 1 Transmit output	O CMOS	1.8V	Runtime		supported on Linux and windows
CAN1_RX	P146	CAN port1 Receive input	I CMOS	1.8V	Runtime		supported on Linux and windows

Note: CAN bus is derived from a USB to CAN controller

4.4.4 Miscellaneous

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
TEST#	S157	Held low by the carrier to invoke the module vendor's specific test function(s).	I CMOS	3.3V	Runtime	PU 10K on the module, driven by OD on the carrier.	The module must implement PU but actual value is depended on particular module design. Carrier Board should leave this pin floating for normal operation
WDT_TIME_OUT#	S145	Watch-Dog-Timer Output, low active.	O CMOS	1.8V	Runtime		Driven only during runtime

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4.4.5 Power and System Management

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
BATLOW#	S156	Battery low indication to Module. Carrier to float the line in inactive state.	I OD CMOS	3.3V	Runtime	PU 10K	Driven by OD on Carrier. Pulled up on module.
CARRIER_PWR_ON	S154	Carrier board circuits (apart from power management and power path circuits) should not be powered up until the Module asserts the CARRIER_PWR_ON signal.	O CMOS	1.8Vsb / 1.8V	-		1.8Vsb is only used for signaling, not a power source to the module
CARRIER_STBY#	S153	The Module shall drive this signal low when the system is in a standby power state.	O CMOS	1.8Vsb / 1.8V	-		
CHARGER_PRSNT#	S152	Held low by Carrier if DC input for battery charger is present.	I OD CMOS	3.3V	Runtime	PU 10K	Driven by OD on Carrier. Pulled up on module.
CHARGING#	S151	Held low by Carrier during battery charging. Carrier to float the line when charge is complete.	I OD CMOS	3.3V	Runtime	PU 10K	Driven by OD on Carrier. Pulled up on module.
VIN_PWR_BAD#	S150	Power bad indication from Carrier board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) shall not be enabled while this signal is held low by the Carrier.	I OD CMOS	5V	Runtime	PU 10K	Driven by OD on Carrier Module must implement PU but actual value is dependent on a particular module design.
SLEEP#	S149	Sleep indicator from Carrier board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module.	I OD CMOS	3.3V	Runtime	PU 10K	Driven by OD on Carrier. Pulled up on module.
LID#	S148	Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module.	I OD CMOS	3.3V	Runtime	PU 10K	Driven by OD on Carrier. Pulled up on module.
POWER_BTN#	P128	Power-button input from Carrier board. Carrier to float the line in in-active state. Active low, level sensitive. Should be debounced on the Module.	I OD CMOS	3.3V	Runtime	PU 10K	Driven by OD on Carrier. Pulled up on module.
RESET_OUT#	P126	General purpose reset output to Carrier board.	O CMOS	1.8V	Runtime		

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Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
RESET_IN#	P127	Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise.	I OD CMOS	3.3V	Runtime	PU 10K	Driven by OD on Carrier. Pulled up on module.
I2C_PM_DAT	P122	Power management I2C bus DATA	I/O OD CMOS	1.8V	Runtime	PU 2k2	On x86 systems these serve as SMB DATA. Pulled up on module.
I2C_PM_CK	P121	Power management I2C bus CLK	O OD CMOS	1.8V	Runtime	PU 2k2	On x86 systems these serve as SMB CLK. Pulled up on module.
SMB_ALERT_1V8#	P1	SMBus Alert# (interrupt) signal	I OD CMOS	1.8V	Runtime	PU 10K	only used on x86 design

4.4.6 Boot Select

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
BOOT_SEL0# BOOT_SEL1# BOOT_SEL2#	P123 P124 P125	Input straps determine the Module boot	I OD CMOS	1.8Vsb	Standby	PU 10K	Driven by OD on Carrier. Pulled up on module. Supports MODE 7 (default) and MODE 3.
~~FORCE_RECOV#~~	S155		~~I OD CMOS~~	~~1.8Vsb~~	~~Standby~~	~~PU 10K~~ -	~~Driven by OD on Carrier.~~ ~~Pulled up on module.~~ ~~Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked. Pulled high on the Module.~~ ~~For SOCs that do not implement a USB based Force Recovery functions, then a low on the Module FORCE_RECOV# pin may invoke the SOC native Force Recovery mode – such as over a Serial Port.~~ ~~For x86 systems this signal may be used to load BIOS defaults.~~ ~~Pulled up on Module. Driven by OD part on Carrier.~~

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4.4.7 Power

Name	Pin #	Description	I/O Type	Power Rail / Tolerance	PU / PD	Comments
VDD_IN	P147, P148, P149, P150, P151, P152, P153, P154, P155, P156	Module power input voltage 4.75 min to 5.25V max	P	4.75 to 5.25V		
GND	P2, P9, P12, P15, P18, P32, P38, P47, P50, P53, P59, P68, P79, P82, P85, P88, P91, P94, P97, P100, P103, P120, P133, P142, S3, S10, S16, S25, S34, S47, S61, S64, S67, S70, S73, S80, S83, S86, S89, S92, S101, S110, S119, S124, S130, S136, S143, S158	Module signal and power return, and GND reference	P	Ground		
VDD_RTC	S147	Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based Lithium cell or Super Cap.	P	[2 to 3.25] / 3.25V		

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4.5 SMARC Pin to Controller Mapping

Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	Native Function	Power Rail
P1	SMB_ALERT_1V8#	-	-	-			_	-
P2	GND	-	-	-	-	-	_	-
P3	CSI1_CK+	In	-	MIPI D-PHY		MIPI_CSI2_CLK_P	_	VCCPRIM
P4	CSI1_CK-	In	-	MIPI D-PHY		MIPI_CSI2_CLK_N	_	VCCPRIM
P5	GBE1_SDP	Out	-	GPIO/3.3V		SPD0		
P6	GBE0_SDP	Out	-	GPIO/3.3V		CLK_OUT		
P7	CSI1_RX0+	In	-	MIPI D-PHY		MIPI_CSI2_D0_P	_	VCCPRIM
P8	CSI1_RX0-	In	-	MIPI D-PHY		MIPI_CSI2_D0_N	_	VCCPRIM
P9	GND	-	-	-	-	-		
P10	CSI1_RX1+	In	-	MIPI D-PHY		MIPI_CSI2_D1_P	_	VCCPRIM
P11	CSI1_RX1-	In	-	LVDS D-PHY		MIPI_CSI2_D1_N	_	VCCPRIM
P12	GND	-	-	-	-	-		
P13	CSI1_RX2+	In	-	MIPI D-PHY		MIPI_CSI2_D2_P	_	VCCPRIM
P14	CSI1_RX2-	In	-	MIPI D-PHY		MIPI_CSI2_D2_N	_	VCCPRIM
P15	GND	-	-	-	-	-		
P16	CSI1_RX3+	In	-	MIPI D-PHY		MIPI_CSI2_D3_P	_	VCCPRIM
P17	CSI1_RX3-	In	-	MIPI D-PHY		MIPI_CSI2_D3_N	_	VCCPRIM
P18	GND	-	-	-	-	-	_	-
P19	GBE0_MDI3-	Bi-Dir	-	GBE MDI	Intel® I226 Series	TD_M_D	_	VDDIO
P20	GBE0_MDI3+	Bi-Dir	-	GBE MDI	Intel® I226 Series	TD_P_D	_	VDDIO
P21	GBE0_LINK100#	Out/OD	-	GPIO / 3.3V	Intel® I226 Series	LED_1	_	VDDIO
P22	GBE0_LINK1000#	Out/OD	-	GPIO / 3.3V	Intel® I226 Series	LED_2	_	VDDIO
P23	GBE0_MDI2-	Bi-Dir	-	GBE MDI	Intel® I226 Series	TD_M_C	_	VDDIO
P24	GBE0_MDI2+	Bi-Dir	-	GBE MDI	Intel® I226 Series	TD_P_C	_	VDDIO
P25	GBE0_LINK_ACT#	Out/OD	-	GPIO / 3.3V	Intel® I226 Series	LED_0	_	VDDIO
P26	GBE0_MDI1-	Bi-Dir	-	GBE MDI	Intel® I226 Series	TD_M_B	_	VDDIO
P27	GBE0_MDI1+	Bi-Dir	-	GBE MDI	Intel® I226 Series	TD_P_B	_	VDDIO
P28	GBE0_CTREF	PWR	-	-	-	-	_	-

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Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	Native Function	Power Rail
P29	GBE0_MDI0-	Bi-Dir	-	GBE MDI	Intel® I226 Series	TD_M_A	-	VDDIO
P30	GBE0_MDI0+	Bi-Dir	-	GBE MDI	Intel® I226 Series	TD_P_A	-	VDDIO
P31	SPI0_CS1#	Out	-	SPI/1.8V	ALN/ASL x7000	SPIO_CS1#	-	VCC_SPI
P32	GND	-	-	-	-	-	-	-
~~P33~~	~~SDIO_WP~~	~~In~~	~~-~~	~~SD2 / 3.3V~~	~~ALN/ASL x7000~~	~~SD2_WP~~	~~ALT0~~	~~NVCC_SD2~~
~~P34~~	~~SDIO_CMD~~	~~Bi-Dir~~	~~-~~	~~SD2 / 3.3V~~	~~ALN/ASL x7000~~	~~SD2_CMD~~	~~ALT0~~	~~NVCC_SD2~~
~~P35~~	~~SDIO_CD#~~	~~In~~	~~-~~	~~SD2 / 3.3V~~	~~ALN/ASL x7000~~	~~SD2_CD~~	~~ALT0~~	~~NVCC_SD2~~
~~P36~~	~~SDIO_CK~~	~~Out~~	~~-~~	~~SD2 / 3.3V~~	~~ALN/ASL x7000~~	~~SD2_CLK~~	~~ALT0~~	~~NVCC_SD2~~
~~P37~~	~~SDIO_PWR_EN~~	~~Out~~	~~-~~	~~GPIO / 3.3V~~	~~ALN/ASL x7000~~	~~GPIO1_IO12~~	~~ALT0~~	~~NVCC_GPIO1~~
P38	GND	-	-	-	-	-		
~~P39~~	~~SDIO_D0~~	~~Bi-Dir~~	~~-~~	~~SD2 / 3.3V~~	~~ALN/ASL x7000~~	~~SD2_DATA0~~	~~ALT0~~	~~NVCC_SD2~~
~~P40~~	~~SDIO_D1~~	~~Bi-Dir~~	~~-~~	~~SD2 / 3.3V~~	~~ALN/ASL x7000~~	~~SD2_DATA1~~	~~ALT0~~	~~NVCC_SD2~~
~~P41~~	~~SDIO_D2~~	~~Bi-Dir~~	~~-~~	~~SD2 / 3.3V~~	~~ALN/ASL x7000~~	~~SD2_DATA2~~	~~ALT0~~	~~NVCC_SD2~~
~~P42~~	~~SDIO_D3~~	~~Bi-Dir~~	~~-~~	~~SD2 / 3.3V~~	~~ALN/ASL x7000~~	~~SD2_DATA3~~	~~ALT0~~	~~NVCC_SD2~~
P43	SPI0_CS0#	Out	-	SPI / 1.8V	ALN/ASL x7000	SPI0_CS0#	ALT0	VCC_SPI
P44	SPI0_CK	Out	-	SPI / 1.8V	ALN/ASL x7000	SPI0_CLK	ALT0	VCC_SPI
P45	SPI0_DIN	In	-	SPI / 1.8V	ALN/ASL x7000	SPI0_MISO	ALT0	VCC_SPI
P46	SPI0_DO	Out	-	SPI / 1.8V	ALN/ASL x7000	SPI0_MOSI	ALT0	VCC_SPI
P47	GND	-	-	-	-	-	-	-
P48	SATA_TX+	out	-	-	ALN/ASL x7000	PCIE12_TXP/SATA1_TXP	-	-
P49	SATA_TX-	out	-	-	ALN/ASL x7000	PCIE12_TXP/SATA1_TXN	-	-
P50	GND	-	-	-	-	-	-	-
P51	SATA_RX+	In	-	-	ALN/ASL x7000	PCIE12_TXP/SATA1_RXP	-	-
P52	SATA_RX-	In	-	-	ALN/ASL x7000	PCIE12_TXP/SATA1_RXN	-	-
P53	GND	-	-	-	-	-	-	-
P54	ESPI_CS0# / SPI1_CS0#	Out	-	SPI / 1.8V	ALN/ASL x7000	ESPI_CS1#	ALT0	VCCPRIM
P55	ESPI_CS1# / SPI1_CS1#	-	-	-	ALN/ASL x7000	N.C.	-	-
P56	ESPI_CK / SPI1_CK	Out	-	SPI / 1.8V	ALN/ASL x7000	ESPI_CLK	ALT0	VCCPRIM
P57	ESPI_IO_1 / SPI1_DIN	In	-	SPI / 1.8V	ALN/ASL x7000	ESPI_MISO	ALT0	VCCPRIM
P58	ESPI_IO_0 / SPI1_DO	Out	-	SPI / 1.8V	ALN/ASL x7000	ESPI_MOSI	ALT0	VCCPRIM

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Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	Native Function	Power Rail
P59	GND	-	-	-	-	-		
P60	USB0+	Bi-Dir	-	USB	ALN/ASL x7000	USB2P_1		VCC_DSW
P61	USB0-	Bi-Dir	-	USB	ALN/ASL x7000	USB2N_1		VCC_DSW
P62	USB0_EN_OC#	In	PU-10K	GPIO / 3.3V	ALN/ASL x7000	USB_OC0#	ALT0	VCCPRIM
~~P63~~	~~USB0_VBUS_DET~~	~~PWR~~	~~-~~	~~USB~~	~~ALN/ASL x7000~~	~~USB1_VBUS~~	~~-~~	~~USB1_VDD33~~
~~P64~~	~~USB0_OTG_ID~~	~~In~~	~~-~~	~~USB~~	~~ALN/ASL x7000~~	~~USB1_ID~~	~~-~~	~~USB1_VDD33~~
P65	USB1+	Bi-Dir	-	USB	ALN/ASL x7000	USB2P_2	-	VCC_DSW
P66	USB1-	Bi-Dir	-	USB	ALN/ASL x7000	USB2N_2	-	VCC_DSW
P67	USB1_EN_OC#	In	-PU-10K	GPIO / 3.3V	ALN/ASL x7000	USB_OC1#	-	VCCPRIM
P68	GND	-	-	-	-	-		
P69	USB2+	Bi-Dir	-	PHY	ALN/ASL x7000	USB2P_3	-	VCC_DSW
P70	USB2-	Bi-Dir	-	PHY	ALN/ASL x7000	USB2N_3	-	VCC_DSW
P71	USB2_EN_OC#	In	PU-10K	GPIO / 3.3V	ALN/ASL x7000	USB_OC1#	-	VCCPRIM
P72	RSVD	-	-	-	N.C.	N.C.		
P73	RSVD	-	-	-	N.C.	N.C.		
P74	USB3_EN_OC#	In	PU-10K	GPIO / 3.3V	ALN/ASL x7000	USB_OC1#	-	VCCPRIM
P75	PCIE_A_RST#	Out	-	GPIO / 3.3V	ALN/ASL x7000	PLTRST#	~~ALT5~~	VCCPRIM
P76	USB4_EN_OC#	In	-	GPIO / 3.3V	ALN/ASL x7000	USB_OC2#	-	VCCPRIM
P77	PCIE_B_CKREQ#	-	PU-10K	-	ALN/ASL x7000	SRCCLKREQ1#	-	VCCPRIM
P78	PCIE_A_CKREQ#	-	PU-10K	-	ALN/ASL x7000	SRCCLKREQ0#	-	VCCPRIM
P79	GND	-	-	-	-	-	-	-
P80	PCIE_C_REFCK+	Out	-	PCIe	ALN/ASL x7000	CLKOUT_PCIE_P2	-	VCCPRIM
P81	PCIE_C_REFCK-	Out	-	PCIe	ALN/ASL x7000	CLKOUT_PCIE_N2	-	VCCPRIM
P82	GND	-	-	-	-	-	-	-
P83	PCIE_A_REFCK+	Out	~~Serial-0.1uF~~	PCIe	ALN/ASL x7000	CLKOUT_PCIE_P0	-	VCCPRIM
P84	PCIE_A_REFCK-	Out	~~Serial-0.1uF~~	PCIe	ALN/ASL x7000	CLKOUT_PCIE_N0	-	VCCPRIM
P85	GND	-	-		-	-	-	-
P86	PCIE_A_RX+	In	~~Serial-0.1uF~~	PCIe	ALN/ASL x7000	PCIE9_RXP	-	VCCPRIM
P87	PCIE_A_RX-	In	~~Serial-0.1uF~~	PCIe	ALN/ASL x7000	PCIE9_RXN	-	VCCPRIM

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Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	Native Function	Power Rail
P88	GND	-	-	-	-	-	_	-
P89	PCIE_A_TX+	Out	Serial-0.1uF	PCIe	ALN/ASL x7000	PCIE9_TXP	_	VCCPRIM
P90	PCIE_A_TX-	Out	Serial-0.1uF	PCIe	ALN/ASL x7000	PCIE2_TXN_N	_	VCCPRIM
P91	GND	-	-	-	-	-		
P92	HDMI_D2+ / DP1_LANE0+	Out	-	HDMI	ALN/ASL x7000	TCP1_TX_P0	_	VCCPRIM
P93	HDMI_D2- / DP1_LANE0-	Out	-	HDMI	ALN/ASL x7000	TCP1_TX_N0	_	VCCPRIM
P94	GND	-	-	-	-	-	_	-
P95	HDMI_D1+ / DP1_LANE1+	Out	-	HDMI	ALN/ASL x7000	TCP1_TX_P1		VCCPRIM
P96	HDMI_D1- / DP1_LANE1-	Out	-	HDMI	ALN/ASL x7000	TCP1_TX_N1		VCCPRIM
P97	GND	-	-	-	-	-	_	-
P98	HDMI_D0+ / DP1_LANE2+	Out	-	HDMI	ALN/ASL x7000	TCP1_TX_P2	_	VCCPRIM
P99	HDMI_D0- / DP1_LANE2-	Out	-	HDMI	ALN/ASL x7000	TCP1_TX_N2	_	VCCPRIM
P100	GND	-	-	-	-	-	_	-
P101	HDMI_CK+ / DP1_LANE3+	Out	-	HDMI	ALN/ASL x7000	TCP1_TX_P3	_	VCCPRIM
P102	HDMI_CK- / DP1_LANE3-	Out	-	HDMI	ALN/ASL x7000	TCP1_TX_N3	`	VCCPRIM
P103	GND	-	-	-	-	-	_	-
P104	HDMI_HPD / DP1_HPD	In		HDMI	ALN/ASL x7000	DDSP_HPD2	_	VCCPRIM
P105	HDMI_CTRL_CK / DP1_AUX+	Out	PU-2.2K / PD-100K	HDMI	ALN/ASL x7000	DDP2_CTRLCLK TCP1_AUX_P	-	VCCPRIM
P106	HDMI_CTRL_DAT / DP1_AUX-	Bi-Dir	PU-2.2K / PD-100K	HDMI	ALN/ASL x7000	DDP2_CTRLDATA TCP1_AUX_N	-	VCCPRIM
P107	DP1_AUX_SEL	Out	PD-1M	HDMI		-	_	-
P108	GPIO0 / ~~CAM0_PWR#~~	Out	PU-470K	GPIO / 1.8V	SX1509	I/O0	~~ALT0~~	VCC_GPIO
P109	GPIO1 / ~~CAM1_PWR#~~	Out	PU-470K	GPIO / 1.8V	SX1509	I/O1	~~ALT0~~	VCC_GPIO
P110	GPIO2 / ~~CAM0_RST#~~	Out	PU-470K	GPIO / 1.8V	SX1509	I/O2	~~ALT0~~	VCC_GPIO
P111	GPIO3 / ~~CAM1_RST#~~	Out	PU-470K	GPIO / 1.8V	SX1509	GPIO1_I/O3	~~ALT0~~	VCC_GPIO
P112	~~GPIO4~~ / HDA_RST#	Out	PU-470K	GPIO / 1.8V	ALN/ASL x7000	HDA_RST#	_	VCCPGPPR
P113	GPIO5 / ~~PWM_OUT~~	Out	PU-470K	GPIO / 1.8V	SX1509	I/O5	_	VCC_GPIO
P114	GPIO6 / ~~TACHIN~~	In	PU-470K	GPIO / 1.8V	SX1509	I/O6	_	VCC_GPIO

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Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	Native Function	Power Rail
P115	GPIO7	In	PU-470K	GPIO / 1.8V	SX1509	I/O7	-	VCC_GPIO
P116	GPIO8	In	PU-470K	GPIO / 1.8V	SX1509	I/O8	-	VCC_GPIO
P117	GPIO9	In	PU-470K	GPIO / 1.8V	SX1509	I/O9	-	VCC_GPIO
P118	GPIO10	In	PU-470K	GPIO / 1.8V	SX1509	I/O10	-	VCC_GPIO
P119	GPIO11	In	PU-470K	GPIO / 1.8V	SX1509	I/O11	-	VCC_GPIO
P120	GND	-	-	-	-	-		
P121	I2C_PM_CK	Out	PU-2k2	I2C2	ALN/ASL x7000	SMBCLK	~~ALT0~~	NVCC_I2C
P122	I2C_PM_DAT	Bi-Dir	PU-2k2	I2C2	ALN/ASL x7000	SMBDATA	~~ALT0~~	NVCC_I2C
P123	BOOT_SEL0#	In	PU-10K	GPIO / 1.8V	EC	KSO13	-	EC_VCC
P124	BOOT_SEL1#	In	PU-10K	GPIO / 1.8V	EC	KSO14	-	EC_VCC
P125	BOOT_SEL2#	In	PU-10K	GPIO / 1.8V	EC	KSO15	-	EC_VCC
P126	RESET_OUT#	Out	-	GPIO / 1.8V	ALN/ASL x7000	PLTRST#	-	VCCPRIM
P127	RESET_IN#	In	PU-4K7	GPIO / 3.3V	ALN/ASL x7000	SYS_RESET#	-	VCCPRIM
P128	POWER_BTN#	In	PU-4K7	GPIO / 3.3V	EC	GPE4	-	EC_VCC
P129	SER0_TX	Out	-	UART / 1.8V	EC	TXD	ALT0	EC_VCC
P130	SER0_RX	In	-	UART / 1.8V	EC	RXD	ALT0	EC_VCC
P131	SER0_RTS#	In	-	UART / 1.8V	EC	RTS0	ALT1	EC_VCC
P132	SER0_CTS#	Out	-	UART / 1.8V	EC	CTS0	ALT1	EC_VCC
P133	GND	-	-	-	-	-	-	-
P134	SER1_TX	Out	-	UART / 1.8V	EC	CTX	ALT0	EC_VCC
P135	SER1_RX	In	-	UART / 1.8V	EC	CRX	ALT0	EC_VCC
P136	SER2_TX	Out	-	UART / 1.8V	ALN/ASL x7000	UART2_TXD	-	VCCPRIM
P137	SER2_RX	In	-	UART / 1.8V	ALN/ASL x7000	UART2_RXD	-	VCCPRIM
P138	SER2_RTS#	In	-	UART / 1.8V	ALN/ASL x7000	UART2_RTS#	-	VCCPRIM
P139	SER2_CTS#	Out	-	UART / 1.8V	ALN/ASL x7000	UART2_CTS#	-	VCCPRIM
P140	SER3_TX	Out	-	UART / 1.8V	ALN/ASL x7000	UART1_TXD	ALT0	VCCPRIM
P141	SER3_RX	In	-	UART / 1.8V	ALN/ASL x7000	UART1_RXD	ALT0	VCCPRIM
P142	GND	-	-	-	-	-	-	-
P143	CAN0_TX	Out	-	CAN	F81604	CAN1_TX	-	VCC_CAN
P144	CAN0_RX	In	-	CAN	F81604	CAN1_RX	-	VCC_CAN

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Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	Native Function	Power Rail
P145	CAN1_TX	-	-	-	F81604	CAN2_TX		VCC_CAN
P146	CAN1_RX	-	-	-	F81604	CAN2_RX		VCC_CAN
P147	VDD_IN	PWR	-	-	From Carrier board	-	_	3 ~ 5.25 V
P148	VDD_IN	PWR	-	-	From Carrier board	-	_	3 ~ 5.25 V
P149	VDD_IN	PWR	-	-	From Carrier board	-	_	3 ~ 5.25 V
P150	VDD_IN	PWR	-	-	From Carrier board	-	_	3 ~ 5.25 V
P151	VDD_IN	PWR	-	-	From Carrier board	-	_	3 ~ 5.25 V
P152	VDD_IN	PWR	-	-	From Carrier board	-	_	3 ~ 5.25 V
P153	VDD_IN	PWR	-	-	From Carrier board	-	_	3 ~ 5.25 V
P154	VDD_IN	PWR	-	-	From Carrier board	-	_	3 ~ 5.25 V
P155	VDD_IN	PWR	-	-	From Carrier board	-	_	3 ~ 5.25 V
P156	VDD_IN	PWR	-	-	From Carrier board	-	_	3 ~ 5.25 V
S1	CSI1_TX+ / I2C_CAM1_CK	In	PU-2k2	I2C3	ALN/ASL x7000	I2C5_SCL	ALT0	VCCPRIM
S2	CSI1_TX- / I2C_CAM1_DAT	In	PU-2k2	I2C3	ALN/ASL x7000	I2C5_SDA	ALT0	VCCPRIM
S3	GND	-	-	-	-	-	_	-
S4	RSVD	In	-	-	N.C.	N.C.	_	-
S5	CSI0_TX- / I2C_CAM0_CK	Out	PU-2k2	I2C4	ALN/ASL x7000	I2C1_SCL	ALT0	VCCPRIM
S6	CAM_MCK	Out	-	GPIO / 1.8V	ALN/ASL x7000	IMGCLKOUT0	ALT5	VCCPRIM
S7	CSI0_TX+ / I2C_CAM0_DAT	Bi-Dir	PU-2k2	I2C4	ALN/ASL x7000	I2C1_SDA	ALT0	VCCPRIM
S8	CSI0_CK+	In	-	MIPI-CSI	ALN/ASL x7000	CSI0_B_CLK_P	_	VCCPRIM
S9	CSI0_CK-	In	-	MIPI-CSI	ALN/ASL x7000	CSI0_B_CLK_N	_	VCCPRIM
S10	GND	-	-	-	-	-	_	-
S11	CSI0_RX0+	In	-	MIPI-CSI	ALN/ASL x7000	CSI0_B_D0_P	_	VCCPRIM
S12	CSI0_RX0-	In	-	MIPI-CSI	ALN/ASL x7000	CSI0_B_D0_N	_	VCCPRIM
S13	GND	-	-	-	-	-	_	-
S14	CSI0_RX1+	In	-	MIPI-CSI	ALN/ASL x7000	CSI0_B_D1_P	_	VCCPRIM
S15	CSI0_RX1-	In	-	MIPI-CSI	ALN/ASL x7000	CSI0_B_D1_N	_	VCCPRIM

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Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	Native Function	Power Rail
S16	GND	-	-	-	-	-	_	-
S17	GBE1_MDI0+	Bi-Dir	-	GBE MDI	Intel® I226 Series	MDI_A_P	_	VCC_GBE1
S18	GBE1_MDI0-	Bi-Dir	-	GBE MDI	Intel® I226 Series	MDI_A_N	_	VCC_GBE1
S19	GBE1_LINK100#	Out	-	GPIO / 3.3V	Intel® I226 Series	LED0	_	-
S20	GBE1_MDI1+	Bi-Dir	-	GBE MDI	Intel® I226 Series	MDI_B_P	_	VCC_GBE1
S21	GBE1_MDI1-	Bi-Dir	-	GBE MDI	Intel® I226 Series	MDI_B_N	_	VCC_GBE1
S22	GBE1_LINK1000#	Out	-	GPIO / 3.3V	Intel® I226 Series	LED2	_	VCC_GBE1
S23	GBE1_MDI2+	Bi-Dir	-	GBE MDI	Intel® I226 Series	MDI_C_P	_	VCC_GBE1
S24	GBE1_MDI2-	Bi-Dir	-	GBE MDI	Intel® I226 Series	MDI_C_N	_	VCC_GBE1
S25	GND	-	-	-	-	-	_	-
S26	GBE1_MDI3+	Bi-Dir	-	GBE MDI	Intel® I226 Series	MDI_D_P	_	VCC_GBE1
S27	GBE1_MDI3-	Bi-Dir	-	GBE MDI	Intel® I226 Series	MDI_D_N	_	VCC_GBE1
S28	GBE1_CTREF	-	-	-	N.C.	N.C.	_	-
S29	PCIE_D_TX+ / SERDES_1_TX+	-	-	-	PCIE_D	PIE12_TXP	_	VCCPRIM
S30	PCIE_D_TX- / SERDES_1_TX-	-	-	-	PCIE_D	PCIE12_TXN	_	VCCPRIM
S31	GBE1_LINK_ACT#	Out	-	GPIO / 3.3V	Intel ® I226 Series	LED1	_	VCC_GBE1
S32	PCIE_D_RX+ / SERDES_1_RX+	-	-	-	PCIE_D	PIE12_RXP	_	VCCPRIM
S33	PCIE_D_RX- / SERDES_1_RX-	-	-	-	PCIE_D	PCIE12_RXN	_	VCCPRIM
S34	GND	-	-	-	-	-		
S35	USB4+	Bi-Dir	-	USB	ALN/ASL x7000	USB2P_5	_	VCC_DSW
S36	USB4-	Bi-Dir	-	USB	ALN/ASL x7000	USB2N_5	_	VCC_DSW
S37	USB3_VBUS_DET	-	-	-	N.C.	N.C.	_	-
S38	AUDIO_MCK	Out	-	SAI / 1.8V	ALN/ASL x7000	I2S_MCLK1_OUT	ALT0	VCCPRIM
S39								N.C.
S40								N.C.
S41								N.C.
S42								N.C.
S43	ESPI_ALERT0#	In	-	SAI / 1.8V	ALN/ASL x7000	ESPI_ALERT0#	ALT5	VCCPRIM
S44	ESPI_ALERT1#	-	-	-	N.C.	N.C.		

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Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	Native Function	Power Rail
~~S45~~	~~MDIO_CLK~~	~~-~~	~~-~~	~~-~~	~~N.C.~~	~~N.C.~~		
~~S46~~	~~MDIO_DAT~~	~~-~~	~~-~~	~~-~~	~~N.C.~~	~~N.C.~~		
S47	GND	-	-	-	-	-		
S48	I2C_GP_CK	Out	PU-2.2K	I2C3	EC	SMCLK4	ALT0	VCC_EC
S49	I2C_GP_DAT	Bi-Dir	PU-2.2K	I2C3	EC	SMDAT4	ALT0	VCC_EC
S50	HDA_SYNC / I2S2_LRCK	-	-	SAI / 1.8V	ALN/ASL x7000	HDA_SYNC	ALT0	VCCPRIM
S51	HDA_SDO / I2S2_SDOUT	-	-	SAI / 1.8V	ALN/ASL x7000	HDA_SDO	ALT0	VCCPRIM
S52	HDA_SDI / I2S2_SDIN	-	-	SAI / 1.8V	ALN/ASL x7000	HDA_SDI	ALT0	VCCPRIM
S53	HDA_CK / I2S2_CK	-	-	SAI / 1.8V	ALN/ASL x7000	HDA_SCLK	ALT0	VCCPRIM
S54	SATA_ACT#	-	-	-	ALN/ASL x7000	SATA_LED#	_	VCCPRIM
S55	USB5_EN_OC#	-	-	-	ALN/ASL x7000	USB_OC2#	_	VCCPRIM
S56	ESPI_IO_2	-	-	-	ALN/ASL x7000	ESPI_IO2	_	VCCPRIM
S57	ESPI_IO_3	-	-	-	ALN/ASL x7000	ESPI_IO3	_	VCCPRIM
S58	ESPI_RESET#	Out	-	GPIO / 1.8V	ALN/ASL x7000	ESPI_RESET#	_	VCCPRIM
S59	USB5+	-	-	-	ALN/ASL x7000	USB2P_6	_	VCC_DSW
S60	USB5-	-	-	-	ALN/ASL x7000	USB2N_6	_	VCC_DSW
S61	GND	-	-	-	-	-	_	-
S62	USB3_SSTX+	Out	Serial-0.1uF	USB	ALN/ASL x7000	USB32_2_TXP	_	VCCPRIM
S63	USB3_SSTX-	Out	Serial-0.1uF	USB	ALN/ASL x7000	USB32_2_TXN	_	VCCPRIM
S64	GND	-	-	-	-	-	_	-
S65	USB3_SSRX+	In	-	USB	ALN/ASL x7000	USB32_2_RXP	_	VCCPRIM
S66	USB3_SSRX-	In	-	USB	ALN/ASL x7000	USB32_2_RXN	_	VCCPRIM
S67	GND	-	-	-	-	-	_	-
S68	USB3+	Bi-Dir	-	USB	ALN/ASL x7000	USB2P_4	_	VCC_DSW
S69	USB3-	Bi-Dir	-	USB	ALN/ASL x7000	USB2N_4	_	VCC_DSW
S70	GND	-	-	-	-	-	_	-
S71	USB2_SSTX+	Out	Serial-0.1uF	USB	ALN/ASL x7000	USB32_1_TXP	_	VCCPRIM
S72	USB2_SSTX-	Out	Serial-0.1uF	USB	ALN/ASL x7000	USB32_1_TXN	_	VCCPRIM
S73	GND	-	-	-	-	-	_	-

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Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	Native Function	Power Rail
S74	USB2_SSRX+	In	-	USB	ALN/ASL x7000	USB32_1_RXP	_	VCCPRIM
S75	USB2_SSRX-	In	-	USB	ALN/ASL x7000	USB32_1_RXN	_	VCCPRIM
S76	PCIE_B_RST#	Out	-	GPIO / 3.3V	ALN/ASL x7000	PLTRST#	~~ALT5~~	VCCPRIM
S77	PCIE_C_RST#	-	-	-	ALN/ASL x7000	PLTRST#	_	VCCPRIM
S78	PCIE_C_RX+ / SERDES_2_RX+	-	-	-	ALN/ASL x7000	PCIE11_RXP	_	VCCPRIM
S79	PCIE_C_RX- / SERDES_2_RX-	-	-	-	ALN/ASL x7000	PCIE11_RXN	_	VCCPRIM
S80	GND	-	-	-	-	-	_	-
S81	PCIE_C_TX+ / SERDES_2_TX+	-	-	-	ALN/ASL x7000	PCIE11_TXP	_	VCCPRIM
S82	PCIE_C_TX- / SERDES_2_TX-	-	-	-	ALN/ASL x7000	PCIE11_TXN	_	VCCPRIM
S83	GND	-	-	-	-	-	_	-
S84	PCIE_B_REFCK+	Out	Serial-0.1uF	PCIe	ALN/ASL x7000	CLKOUT_PCIE_P1	_	VCCPRIM
S85	PCIE_B_REFCK-	Out	Serial-0.1uF	PCIe	ALN/ASL x7000	CLKOUT_PCIE_N1	_	VCCPRIM
S86	GND	-	-	-	-	-	_	-
S87	PCIE_B_RX+	In	Serial-0.1uF	PCIe	ALN/ASL x7000	PCIE10_RXP	_	VCCPRIM
S88	PCIE_B_RX-	In	Serial-0.1uF	PCIe	ALN/ASL x7000	PCIE10_RXN	_	VCCPRIM
S89	GND	-	-	-	-	-	_	-
S90	PCIE_B_TX+	Out	Serial-0.1uF	PCIe	ALN/ASL x7000	PCIE10_TXP	_	VCCPRIM
S91	PCIE_B_TX-	Out	Serial-0.1uF	PCIe	ALN/ASL x7000	PCIE10_RXP	_	VCCPRIM
S92	GND	-	-	-	-	-	_	-
S93	DP0_LANE0+	-	-	-	ALN/ASL x7000	TCP0_TX_P0	_	VCCPRIM
S94	DP0_LANE0-	-	-	-	ALN/ASL x7000	TCP0_TX_N0	_	VCCPRIM
S95	DP0_AUX_SEL	Out	PD-1M	DP0			_	-
S96	DP0_LANE1+	-	-	-	ALN/ASL x7000	TCP0_RX_P0	_	VCCPRIM
S97	DP0_LANE1-	-	-	-	ALN/ASL x7000	TCP0_RX_N0	_	VCCPRIM
S98	DP0_HPD	-	-	-	ALN/ASL x7000	DDSP_HPD1	_	VCCPRIM
S99	DP0_LANE2+	-	-	-	ALN/ASL x7000	TCP0_TX_P1	_	VCCPRIM
S100	DP0_LANE2-	-	-	-	ALN/ASL x7000	TCP0_TX_N1	_	VCCPRIM
S101	GND	-	-	-	-	-	_	-
S102	DP0_LANE3+	-	-	-	ALN/ASL x7000	TCP0_RX_P1	_	VCCPRIM
S103	DP0_LANE3-	-	-	-	ALN/ASL x7000	TCP0_RX_N1	_	VCCPRIM

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Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	Native Function	Power Rail
~~S104~~	~~USB3_OTG_ID~~	~~-~~	~~-~~	~~-~~	~~N.C.~~	~~N.C.~~	~~-~~	~~-~~
S105	DP0_AUX+	-	-	-	ALN/ASL x7000	TCP0_AUX_P	-	VCCPRIM
S106	DP0_AUX-	-	-	-	ALN/ASL x7000	TCP0_AUX_N	-	VCCPRIM
~~S107~~	~~LCD1_BKLT_EN~~	~~-~~	~~-~~	~~-~~	~~N.C.~~	~~N.C.~~	~~-~~	~~-~~
S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	Out	Serial-0R	LVDS	PTN3460	LVSCKE_P	-	VCC_LVDS
S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	Out	Serial-0R	LVDS	PTN3460	LVSCKE_N	-	VCC_LVDS
S110	GND	-	-	-			-	-
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	Out	Serial-0R	LVDS	PTN3460	LVSAE_P	-	VCC_LVDS
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	Out	Serial-0R	LVDS	PTN3460	LVSAE_N	-	VCC_LVDS
~~S113~~	~~eDP1_HPD / DSI1_TE~~	~~-~~	~~-~~	~~-~~	~~N.C.~~	~~N.C.~~	~~-~~	~~-~~
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	Out	Serial-0R	LVDS	PTN3460	LVSBE_P	-	VCC_LVDS
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	Out	Serial-0R	LVDS	PTN3460	LVSBE_N	-	VCC_LVDS
~~S116~~	~~LCD1_VDD_EN~~	~~-~~	~~-~~	~~-~~	~~N.C.~~	~~N.C.~~	~~-~~	~~-~~
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	Out	Serial-0R	LVDS	PTN3460	LVSCE_P	-	VCC_LVDS
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	Out	Serial-0R	LVDS	PTN3460	LVSCE_N	-	VCC_LVDS
S119	GND	-	-	-	-	-	-	-
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	Out	Serial-0R	LVDS	PTN3460	LVSDE_P	-	VCC_LVDS
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	Out	Serial-0R	LVDS	PTN3460	LVSDE_N	-	VCC_LVDS
~~S122~~	~~LCD1_BKLT_PWM~~	~~-~~	~~-~~	~~-~~	~~N.C.~~	~~N.C.~~	~~-~~	~~-~~
S123	GPIO13	-	-	-	SX1509	I/IO13	-	VCC_GPIO
S124	GND	-	-	-	-	-	-	-
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	Out	Serial-0R	LVDS	PTN3460	LVSAO_P	-	VCC_LVDS

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S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	Out	Serial-0R	LVDS	PTN3460	LVSAO_N	-	VCC_LVDS
S127	LCD0_BKLT_EN	Out	-	GPIO / 1.8V	PTN3460	BKLTEN	-	VCC_LVDS
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	Out	Serial-0R	LVDS	PTN3460	LVSBO_P	-	VCC_LVDS
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	Out	Serial-0R	LVDS	PTN3460	LVSBO_N	-	VCC_LVDS
S130	GND	-	-	-	-	-	-	-
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	Out	Serial-0R	LVDS	PTN3460	LVSCO_P	-	VCC_LVDS
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	Out	Serial-0R	LVDS	PTN3460	LVSCO_N	-	VCC_LVDS
S133	LCD0_VDD_EN	Out	-	GPIO/1.8V	PTN3460	PVCCEN	-	VCC_LVDS
S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	Out	Serial-0R	LVDS	PTN3460	LVSCKO_P	-	VCC_LVDS
S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	Out	Serial-0R	LVDS	PTN3460	LVSCKO_N	-	VCC_LVDS
S136	GND	-	-	-	-	-	-	-
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	Out	Serial-0R	LVDS	PTN3460	LVSDO_P	-	VCC_LVDS
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	Out	Serial-0R	LVDS	PTN3460	LVSDO_N	-	VCC_LVDS
S139	I2C_LCD_CK	Out	PU-2.2K	I2C4	PTN3460	DDC_SCL	~~ALT0~~	VCC_LVDS
S140	I2C_LCD_DAT	Bi-Dir	PU-2.2K	I2C4	PTN3460	DDC_SDA	~~ALT0~~	VCC_LVDS
S141	LCD0_BKLT_PWM	Out	-	GPIO / 1.8V	ALN/ASL x7000	eDP_BKLTCTL	ALT1	VCCPRIM
S142	GPIO12	In	PU-10K	GPIO / 1.8V	SX1509	I/O12	-	VCC_GPIO
S143	GND	-	-	-	-	-	-	-
S144	eDP0_HPD / DSI0_TE	-	-	-	N.C.	N.C.	-	-
S145	WDT_TIME_OUT#	Out	-	GPIO / 1.8V	EC	KSO0/PD0	-	VCC_EC
S146	PCIE_WAKE#	In	-	GPIO / 3.3V	ALN/ASL x7000	WAKE#	~~ALT5~~	VCC_DSW
S147	VDD_RTC	PWR	-	PWR	-	-	-	-
S148	LID#	In	PU-4.7K	GPIO / 3.3V	EC	GPC6	~~ALT5~~	VCC_EC

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Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	Native Function	Power Rail
S149	SLEEP#	In	PU-4.7K	GPIO / 3.3V	ALN/ASL x7000	GPP_H9	ALT5	VCPRIM
S150	VIN_PWR_BAD#	In	PU-10K	GPIO / 5V	EC	GPH6/ID6	-	VCC_EC
S151	CHARGING#	Out	PU-68K	GPIO / 3.3V	EC	KSI6	~~ALT5~~	VCC_EC
S152	CHARGER_PRSNT#	Out	PU-100K	GPIO / 3.3V	EC	KSI7	ALT5	VCC_EC
S153	CARRIER_STBY#	Out	-	GPIO / 1.8V	EC	KSI3	-	VCC_EC
S154	CARRIER_PWR_ON	Out	-	GPIO / 1.8V	EC	GPF4	-	VCC_EC
S155	FORCE_RECOV#	In	PU-10K	GPIO / 1.8V	ALN/ASL x7000	GPP_E8	-	VCPRIM
S156	BATLOW#	In	PU-10K	GPIO / 3.3V	ALN/ASL x7000	BATLOW#	-	VCPRIM
S157	TEST#	In	PU-10K	GPIO / 3.3V	EC	KSI0	-	VCC_EC
S158	GND	-	-	-	-	-	-	-

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5. Additional Features

This chapter describes connectors, LEDs, switches, and additional items located on the module that may not necessarily be included in the PICMG standard specification. The locations of these items are illustrated below:

5.1 Module Feature Locations

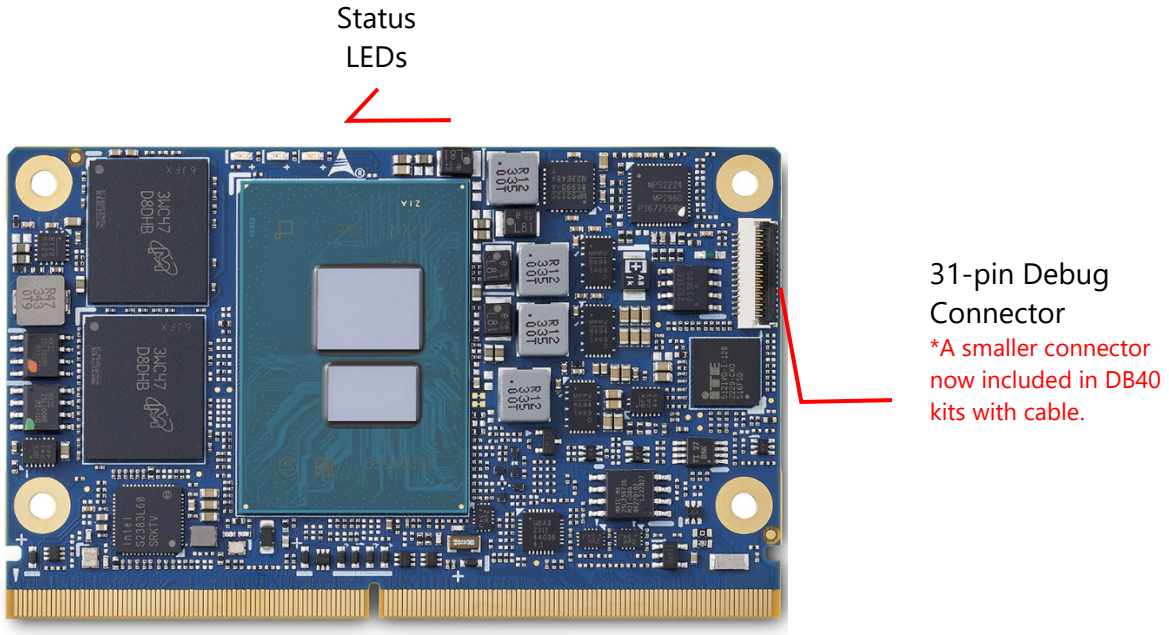
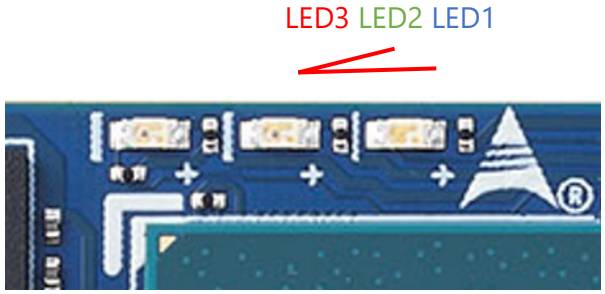


Figure 3 – Module feature locations (top side)

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5.2 Status LEDs

The integration of the status LEDs onto the module simplifies maintenance procedures, ensuring swift and efficient identification of operational status.



Name	Color	Connection	Function
LED1	Blue	BMC/EC output	Power Sequence Status Code (BMC) Power Changes, RESET (see Exception Codes below)
LED2	Green	Power Source	S0 LED ON S3/S4/S5 LED OFF ECO mode LED OFF
LED3	Red	Watchdog (WD)	Module power up WD LED = LED OFF Watchdog counting WD LED = Keep Last State Watchdog timed out WD LED = LED ON Watchdog RESET WD LED = LED ON Rebooted after WD RESET WD LED = LED ON Rebooted after PWRBTN WD LED = LED OFF Rebooted after RESET BTN WD LED = LED OFF Note: only a RESET not initiated by the BMC can clear the WD LED (user action)

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5.2.1 Exception Codes

Exception Code	Error Message
0	NOERROR
3	NO_SLP_S5
4	NO_SLP_S4
5	NO_SLP_S3
6	BIOS_FAIL
8	RESETIN_FAIL
9	NO_CB_PWROK
10	CRITICAL_TEMP
11	POWER_FAIL
12	VOLTAGE_FAIL
13	RSMRST_FAIL
14	NO_VDDQ_PG
16	NO_VCORE_PG
17	NO_SYS_GD
19	NO_V3P3A
21	NO_PWRSRC_GD

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6. System Resources

6.1 System Memory Map

Memory Range	Target	Dependency / Comments
000A0000 – 000B FFFF	PCIE port	PCIe root port
000E 0000 - 000F 3FFF	PCIE port	PCIe root port
000E 4000 - 000F 7FFF	PCIE port	PCIe root port
000E 8000 - 000F BFFF	PCIE port	PCIe root port
000E C000 – 000E FFFF	PCIE port	PCIe root port
000F 0000 - 000F FFFF	PCIE port	PCIe root port
0080400000 – 00BFFFFFFF	PCIE port	PCIe root port
00C0000000- 00CFFFFFFF	Motherboard resources	
00FD690000 – 00FD69FFFF	Serial IO GPIO Host Controller	Serial IO GPIO Host Controller – INTC1057
00FD6A0000 – 00FD6AFFFF	Serial IO GPIO Host Controller	Serial IO GPIO Host Controller – INTC1057
00FD6D0000 – 00FD6DFFFF	Serial IO GPIO Host Controller	Serial IO GPIO Host Controller – INTC1057
00FD6E0000 – 00FD6EFFFF	Serial IO GPIO Host Controller	Serial IO GPIO Host Controller – INTC1057
00FE010000- 00FE010FFF	SPI Controller	SPI Controller – 54A4
00FED00000- 00FED003FF	High precision event timer	
00FED20000-00FED7FFFF	Motherboard resources	
00FED45000-00FED8FFFF	Motherboard resources	
00FED90000-00FED93FFF	Motherboard resources	
00FEDA0000-00FEDA0FFF	Motherboard resources	
00FEDA1000-00FEDA1FFF	Motherboard resources	
00FEDC0000-00FEDC7FFF	Motherboard resources	
00FEE00000-00FEEFFFFF	Motherboard resources	
004000000000 – 00 400FFFFFFF	Intel UHD Graphics	
006000000000 – 00600FFFFFFF	Intel UHD Graphics	
006001100000-00600110FFFF	XHCI Controller	Intel USB3.0 XHCI Controller
006001118000-0060011180FF	SMBus	SMBus-54A3

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00600111B000-00600111BFFF	Intel SD Host Controller	
007FFFEF3000-007FFFEF3FFF	UART#0	Intel Serial IO UART Host Controller – 54A8
007FFFEF4000-007FFFEF4FFF	UART#1	Intel Serial IO UART Host Controller – 54C7
007FFFEF5000-007FFFEF5FFF	I2C#0	Intel Serial IO I2C Host Controller – 54C6
007FFFEF6000-007FFFEF6FFF	I2C#1	Intel Serial IO I2C Host Controller-54C5
007FFFEF7000-007FFFEF7FFF	Intel ME	Intel ME Interface #1
007FFFEF8000-007FFFEF8FFF	I2C#2	Intel Serial IO I2C Host Controller-54E9
007FFFEF9000-007FFFEF9FFF	I2C#3	Intel Serial IO I2C Host Controller-54E8
007FFFEFA000-007FFFEFAFFF	UART#2	Intel Serial IO UART Host Controller – 54A9
007FFFEFB000-007FFFEFBFFF	GNA	Intel GNA Scoring Accelerator module
007FFFEFC000-007FFFEFCFFF	HDA	High Definition Audio Controller
007FFFF00000-007FFFFFFFFF	HDA	High Definition Audio Controller

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6.2 I/O Map

Fixed I/O Decode Ranges

Hex Range	Device
020h – 02Dh & 030h – 03Dh	Programmable interrupt controller
02Eh – 02Fh	Motherboard resource
040h – 043h & 050h – 053h	System Timer
04Eh – 04Fh	Motherboard resource
062h, 066h	Microsoft ACPI-Compliant Embedded Controller
061h, 063h, 065h, 067h, 070h, 080h, 092h	Motherboard resource
0A0h – 0B1h & 0B4h – 0BDh	Interrupt Controller
0B2h and 0B3h	Motherboard resource
0E0h – 0EFh	Available
0F0h	Co-processor error register
200h - 201h	SEMA Embedded Controller
2F8h – 2FFh	Serial Port 2
3F8h – 3FFh	Serial Port 1
378h – 37Fh	Available
380h – 3AFh	Available
4D0h-4D1h	Interrupt Controller
680h – 69Fh & 0A00h – 0A6Fh & 164Eh -164Fh & 1854h-1857h & 2000h-20FEh	Motherboard resource
3000h-303Fh	Intel UHD Graphics
EFA0h- EFBFh	SMBus – 54A3
020h – 02Dh & 030h – 03Dh	Programmable interrupt controller
02Eh – 02Fh	Motherboard resource

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6.3 Interrupt Request (IRQ) Lines

APIC Mode

IRQ#	Typical Intterupt Resource	Connected to Pin	Available
0	System timer	N/A	No
3	Serial Port 2 (COM2)	IRQ3 via SERIRQ/PIRQ	No
4	Serial Port 1 (COM1)	IRQ4 via SERIRQ/PIRQ	No
14	Intel Serial IO GPIO Host Controller	N/A	No
16	Intel SD Host Controller	PCI Usage	No
16	Intel Serial IO UART Host Controller-54A8	PCI Usage	No
17	Intel Serial IO UART Host Controller-54A9	PCI Usage	No
19	High Definition Audio Controller	PCI Usage	No
27	Intel Serial IO I2C Host Controller-54E8	PCI Usage	No
31	Intel Serial IO I2C Host Controller-54C5	PCI Usage	No
32	Intel Serial IO I2C Host Controller-54C6	PCI Usage	No
36	Intel Serial IO SPI Host Controller-54AA	PCI Usage	No
40	Intel Serial IO I2C Host Controller-54E9	PCI Usage	No
42	Intel Serial IO UART Host Controller-54C7	PCI Usage	No
43-511	Microsoft ACPI-Compliant System	N/A	Yes

Note: These IRQs can be used for PCI devices when the onboard device is disabled.

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6.4 PCI Configuration Space Map

Bus Number	Device Number	Function Number	Routing	Description
00h	00h	00h	N/A	Intel Corporation Host Bridge
00h	02h	00h	Internal	Intel VGA Controller
00h	08h	00h	Internal	Intel system device
00h	14h	00h	Internal	USB xHCI Controller
00h	14h	02h	Internal	RAM Controller
00h	15h	00h	Internal	I2C Controller #0
00h	15h	01h	Internal	I2C Controller #1
00h	16h	00h	Internal	Intel® CSME Interface #1
00h	19h	00h	Internal	I2C Controller #2
00h	19h	01h	Internal	I2C Controller #3
00h	19h	02h	Internal	UART #0
00h	1Ah	00h	Internal	SD Host Controller
00h	1Ch	00h	Internal	Intel PCI Express Root port 4
00h	1Eh	00h	Internal	UART #1
00h	1Eh	01h	Internal	UART #2
00h	1Fh	00h	Internal	Intel ISA bridge
00h	1Fh	03h	Internal	HD Audio
00h	1Fh	04h	Internal	SMBus Controller
00h	1Fh	05h	Internal	SPI Contoller
01h	00h	00h	Internal	Intel Ethernet controller I226-V

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6.5 PCI Interrupt Routing Map

INT Line	xHCI Controller	SATA Controller	SMBus Controller
Int0	INTD: 16	INTA: 16	INTA: 16
Int1		INTB: 17	INTB: 17
Int2		INTC: 18	INTC: 18
Int3		INTD: 19	INTD: 19

INT Line	PCIe Port 4	PCIe Port 7	PCIe Port 9	PCIe Port 10	PCIe Port 11	PCIe Port 12
Int0	INTA: 16	INTB: 17	INTC: 18	INTD: 19	INTA: 16	INTB: 17
Int1	INTB: 17	INTC: 18	INTD: 19	INTA: 16	INTB: 17	INTC: 18
Int2	INTC: 18	INTD: 19	INTA: 16	INTB: 17	INTC: 18	INTD: 19
Int3	INTD: 19	INTA: 16	INTB: 17	INTC: 18	INTD: 19	INTA: 16

6.6 SMBus Address Table

Device	Address
IT5121(EC)	050h
SX1509	03Fh
PTN3460	0C0h

6.7 I2C Address Table

Device	Address
THRM-Sensor (SU1)	92h
THRM-Sensor (SU2)	90h
EEPROM (U33)	50h

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7. BIOS Configurations

This section presents the six primary menus of the BIOS Setup Utility. Use the following table as a quick reference for the contents of the BIOS Setup Utility. The subsections in this section describe the submenus and setting options for each menu item. The default setting options are presented in **bold**, and the function of each setting is described in the right-hand column of the respective table.

Main	Advanced	Chipset	Security	Boot	Save & Exit
BIOS Information System Information Board Information ► System Date System Time	CPU Configuration ► Power & Performance ► Inter(R) Time Coordinated Computing ► Power Management ► System Management ► Thermal Management ► Watchdog Timer ► Super IO Configuration ► Miscellaneous ► USB Configuration ► AMI Graphics Output Protocol Policy ► Serial Port Console Redirection ► Network Stack Configuration ► Trusted Computing ►	System Agent (SA) Configuration ► PCH-IO Configuration ►	Setup Administrator Password User Password Secure Boot	Boot Configuration FIXED BOOT ORDER Priorities UEFI USB Key Drive BBS Priorities	Save Change and Exit Discard Changes and Exit Save Changes and Reset Discard Changes and Reset Save Options Boot Override

Note: ► indicates a submenu

Gray text indicates info only

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7.1 Main

The Main Menu provides read-only information about your system and also allows you to set the system date and time. Refer to the tables below for details of the submenus and settings.

7.1.1 Main > BIOS Information

Feature	Options	Description
BIOS Vendor	Info only	American Megatrends
BIOS Version	Info only	Display Core version
Build Date	Info only	Display compliancy information
MRC Version	Info only	Display compliancy information
GOP Version	Info only	ADLINK BIOS version.
ME FW Version	Info only	ADLINK BIOS version.
BIOS Vendor	Info only	American Megatrends

7.1.2 Main > System Information

Feature	Options	Description
Project Name	Info only	Display Project Name.
CPU Board Version	Info only	Display CPU Signature.
CPU Brand String	Info only	Display CPU Brand Name.
CPU Frequency	Info only	Display CPU Frequency
Total Memory	Info only	Display installed memory size.
Memory Frequency	Info only	Display memory frequency.
PCH SKU	Info only	Display PCH Information.

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Feature	Options	Description
Board Information	Submenu	

7.1.3 Main > Board Information

Feature	Options	Description
Serial Number	Read only	Display SMC serial Number
Manufacturing Date	Read only	Display SMC manufacturing date.
Last Repair Date	Read only	Display SMC last repair date.
MAC ID	Read only	Display SMC MAC ID.
MAC ID 2	Read only	Display SMC MAC ID 2.
UUID	Read only	Display SMC UUID
Runtime Statistics	Info only	
Total Runtime	Read only	The returned value specifies the total time in minutes the system is running in S0 state.
Current Runtime	Read only	The returned value specifies the time in seconds the system is running in S0 state. This counter is cleared when the system is removed from the external power supply.
Power Cycles	Read only	The returned value specifies the number of times the external power supply has been shut down.
Boot Cycles	Read only	The Bootcounter is increased after a HW- or SW-Reset or after a successful power-up.
Boot Reason	Read only	The boot reason is the event which causes the reboot of the system.

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7.1.4 Main > System Date and Time

Feature	Options	Description
System Date	Weekday, MM/DD/YYYY	Requires the alpha-numeric entry of the day of the week, day of the month, calendar month, and all 4 digits of the year, indicating the century and year (Fri XX/XX/20XX)
System Time	HH/MM/SS	Presented as a 24-hour clock setting in hours, minutes, and seconds
Access Level	Read only	It shows what access level is used to enter BIOS setup menu.

7.2 Advanced

The Advanced menu contains the settings for most of the user interfaces in the system.

7.2.1 Advanced > CPU Configuration

Feature	Options	Description
ID	Info only	Display CPU information.
Brand String	Info only	Display CPU information.
Microcode Revision	Info only	Display Microcode Revision
VMX	Info only	Display Intel Virtualization Technology support or not.
SMX/TXT	Info only	Display Intel SMX Technology support or not.
Intel (VMX) Virtualization Technology	Disabled, **Enabled**	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.
Active Efficient-cores	**All**,7,6,5,4,3,2,1,0	The number of E-cores to enable in each processor package. Note: The number of cores and E-cores are taken into account together. When both are {0,0}, Pcode will enable all cores.

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7.2.2 Advanced > Power & Performance

7.2.2.1 Advanced > Power & Performance > CPU – Power Management

Feature	Options	Description
Boot Performance Mode	Max Battery, Max Non-Turbo Performance, **Turbo Performance**	Select the performance state that the BIOS will set starting from the reset vector.
Intel(R) SpeedStep(tm)	Disabled, **Enabled**	Allows more than two frequency ranges to be supported.
Race To Halt (RTH)	Disabled, **Enabled**	Enable/Disable Race To Halt feature. RTH will dynamically increase CPU frequency in order to enter pkg C-State faster to reduce overall power. (RTH is controlled through MSR 1FC bit 20)
Intel(R) Speed Shift Technology	Disabled, **Enabled**	Enable/Disable Intel(R) Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states.
Per Core P State OS control P State	Disabled, **Enabled**	Enable/Disable Per Core P state OS control mode. Disabling will set Bit 31 = 1 command 0x06. When set, the highest core request is used for all other core requests.
HwP Autonomous Per Core P State	Disabled, **Enabled**	Disable Autonomous PCPS (Bit 30 = 1, command 0x11). Autonomous will request the same value for all cores all the time. Enable PCPS (default Bit 30 = 0, command 0x11)
HwP Autonomous EPP Grouping	Disabled, **Enabled**	Enable EPP grouping (default Bit 29 =0, command 0x11) Autonomous will request the same values for all cores with same EPP. Disable EPP grouping (Bit 29 =1 , command 0x11) autonomous will not necessarily request same values for all cores with same EPP.
EPB override over PECI	**Disabled**, Enabled	Enable/Disable EPB override over PECI. Enable by sending pcode command 0x2b , subcommand 0x3 to 1. This will allow OOB EPB PECI override control
HwP Lock	Disabled, **Enabled**	Enable/Disable HWP Lock support in Misc Power Management MSR.
HDC Control	Disabled, **Enabled**	This option allows HDC configuration.
Turbo Mode	Disabled, **Enabled**	Enable/Disable processor Turbo Mode (requires EMTTM enabled too). AUTO means enabled.
View/Configure Turbo Options	Submenu	
Current Turbo Settings		
Max Turbo Power Limit	Info only	
Min Turbo Power Limit	Info only	

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Feature	Options	Description
Package TDP Limit	Info only	
Power Limit 1	Info only	
Power Limit 2	Info only	
Turbo Ratio Limit Options	Submenu	
Energy Efficient P-state	Disabled, **Enabled**	Enable/Disable Energy Efficient P-state feature. When set to 0, will disable access to ENERGY_PERFORMANCE_BIAS MSR and CPUID Function 6 ECX[3] will read 0 indicating no support for Energy Efficient policy setting. When set to 1 will enable access to ENERGY_PERFORMANCE_BIAS MSR 1B0h and CPUID Fun
Package Power Limit MSR Lock	**Disabled**, Enabled	Enable/Disable locking of Package Power Limit settings. When enabled, PACKAGE_POWER_LIMIT MSR will be locked and a reset will be required to unlock the register.
Energy Efficient Turbo	Disabled, **Enabled**	Enable/Disable Energy Efficient Turbo Feature. This feature will opportunistically lower the turbo frequency to increase efficiency. Recommended only to disable in overclocking situations where turbo frequency must remain constant. Otherwise, leave it enabled.
Config TDP Configurations	Submenu	
Config TDP Configurations		
Enable Configurable TDP	Applies to non-cTDP, **Applies to cTDP**	Applies TDP initialization settings based on non-cTDP or cTDP. Default is 1: Applies to cTDP; if 0 then applies non-cTDP and BIOS will bypass cTDP initialzation flow
Configurable TDP Boot Mode	**Nominal**, Down2, Down1, Deactivate	Configurable TDP Mode as Nominal/Up/Down/Deactivate TDP selection. Deactivate option will set MSR to Nominal and MMIO to Zero.
Configurable TDP Lock	Enabled, **Disabled**	Configurable TDP Mode Lock sets the Lock bits on TURBO_ACTIVATION_RATIO and CONFIG_TDP_CONTROL. Note: When CTDP Lock is enabled Custom ConfigTDP Count will be forced to 1 and Custom ConfigTDP Boot Index will be forced to 0.
CTDP BIOS control	Enabled, **Disabled**	Enables Configurable Processor Base Power (cTDP) control via runtime ACPI BIOS methods. This "BIOS only" feature does not require EC or driver support.
ConfigTDP Levels	2	Configurable Processor Base Power (cTDP) Levels Supported from MSR
ConfigTDP Turbo Activation Ratio	17 (Unlocked)	Configurable Processor Base Power (cTDP) Turbo Activation Ratio values from MSR
Power Limit 1	15.0W (MSR:15.0)	Power Limit 1 values from MMIO

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Feature	Options	Description
Power Limit 2	15.0W (MSR:15.0)	Power Limit 2 values from MMIO
Custom Settings Nominal		
ConfigTDP Nominal	Ratio:18 TAR:17 PL1:15.0W	Configurable Processor Base Power (cTDP) Nominal Ratio and Processor Base Power (TDP) from MSR
Power Limit 1	0	Power Limit 1 in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Overclocking SKU: Value must be between Max and Min Power Limits (specified by PACKAGE_POWER_SKU_MSR). Other SKUs: This value must be between Min Power Limit and TDP
Power Limit 2	15000	Power Limit 2 value in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Processor applies control policies such that the package power does not exceed this limit.
Power Limit 1 Time Window*	**0**, 1, 2, 3, 4, 5, 6, 7, 8, 10, 12, 14, 16, 20, 24, 28, 32, 40, 48, 56, 64, 80, 96, 112, 128	Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0 = default value (28 sec for Mobile and 8 sec for Desktop). Defines time window which TDP value should be maintained.
ConfigTDP Turbo Activation Ratio	[Max-Value, Min-Value, Step-Value] = [0xFF, 0x00, 0x01]	Custom value for Turbo Activation Ratio. Needs to be configured with valid values from LFM to Max Turbo. 0 means don't use custom value.
Custom Settings Level1		
ConfigTDP Level1	Ratio:10 TAR:9 PL1:9.0W	
Power Limit 1	0	Power Limit 1 in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Overclocking SKU: Value must be between Max and Min Power Limits (specified by PACKAGE_POWER_SKU_MSR). Other SKUs: This value must be between Min Power Limit and TDP
Power Limit 2	0	Power Limit 2 value in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Processor applies control policies such that the package power does not exceed this limit.
Power Limit 1 Time Window*	**0**, 1, 2, 3, 4, 5, 6, 7, 8, 10, 12, 14, 16, 20, 24, 28, 32, 40, 48, 56, 64, 80, 96, 112, 128	Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0 = default value (28 sec for Mobile and 8 sec for Desktop). Defines time window which TDP value should be maintained.
ConfigTDP Turbo Activation Ratio	0	Custom value for Turbo Activation Ratio. Needs to be configured with valid values from LFM to Max Turbo. 0 means don't use custom value.

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Feature	Options	Description
CPU VR Settings	Submenu	
CPU VR Settings		
Current VccIn Aux Icc Max	108	Current VccIn Aux Icc Max
PSYS Slope	0	PSYS Slope defined in 1/100 increments. Range is 0-200. For a 1.25 slope, enter 125. 0 = AUTO. Uses BIOS VR mailbox command 0x9."
PSYS Offset	0	PSYS Offset defined in 1/1000 increments. Range is 0-63999. For an offset of 25.348, enter 25348. PSYS Uses BIOS VR mailbox command 0x4.
PSYS Prefix	**+**, -	Sets the offset value as positive or negative.
PSYS PMax Power	0	PSYS PMax power, defined in 1/8 Watt increments. Range 0-8192. For a PMax of 125W, enter 1000. 0 = AUTO. Uses BIOS VR mailbox command 0xB.
Min Voltage Override	**Disabled**, Enabled	Min Voltage Override. Enable to override minimum voltage for runtime and for C8.
VccIn Aux Icc Max	0	Sets the Max Icc VccIn Aux value defined in 1/4A increments. Range is 0-512. For an IccMax 32A, enter 128(32*4).
VccIn Aux IMON Slope	111	VccIN Aux IMON Slope defined in 1/100 increments. Range is 0-200. For a 1.25 slope, enter 125. 0 = AUTO. Uses BIOS VR mailbox command 0x18.
VccIn Aux IMON Offset	0	VccIN Aux IMON Offset defined in 1/1000 increments. Range is 0-63999. For an offset of 25.348, enter 25348. IMON Uses BIOS VR mailbox command 0x18.
VccIn Aux IMON Prefix	**+.-**	Sets the offset value as positive or negative.
Vsys/Psys Critical	**Disabled**,Psys Critical,Vsys Critical	Vsys/Psys Critical Enable or disable
Assertion Deglitch Mantissa	**1**	Assertion Deglitch Mantissa 0x4F[7-3]. Assertion Deglitch = 2µs * Mantissa * 2^(Exponent)
Assertion Deglitch Exponent	**0**	Assertion Deglitch Exponent 0x4F[3-0]. Assertion Deglitch = 2µs * Mantissa * 2^(Exponent)
De assertion Deglitch Mantissa	**13**	De Assertion Deglitch Mantissa 0x49[7-3]. Assertion Deglitch = 2µs * Mantissa * 2^(Exponent)
De assertion Deglitch Exponent	**2**	De Assertion Deglitch Exponent 0x49[3-0]. Assertion Deglitch = 2µs * Mantissa * 2^(Exponent)
VR Power Delivery Design	**Auto**	Specifies the ADL Desktop board design used for the VR settings override values. By default, BIOS will override the default Desktop VR settings based on the board design. A value of AUTO(0) will use the board ID to determine the board design. Any other value will override the board id logic to provide a custom VR Power

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Feature	Options	Description
		Delivery Design value. This is intended primarily for validation.
Acoustic Noise Settings	Submenu	
Acoustic Noise Mitigation	**Disabled**, Enabled	Enabling this option will help mitigate acoustic noise on certain SKUs when the CPU is in deeper C state
Pre Wake Time	0	Set the maximum Pre Wake randomization time in micro ticks. Range is 0-255. This is for acoustic noise mitigation Dynamic Periodicity Alteration (DPA) tuning.
Ramp Up Time	0	Set the maximum Ramp Up randomization time in micro ticks. Range is 0-255. This is for acoustic noise mitigation Dynamic Periodicity Alteration (DPA) tuning.
Ramp Down Time	0	Set the maximum Ramp Down randomization time in micro ticks. Range is 0-255. This is for acoustic noise mitigation Dynamic Periodicity Alteration (DPA) tuning.
IA VR Domain		
Disable Fast PKG C State Ramp for IA Domain	**FALSE**, TRUE	This option needs to be configured to reduce acoustic noise during the deeper C states. False: Don't disable Fast ramp during deeper C states; True: Disable Fast ramp during deeper C state.
Slow Slew Rate for IA Domain	**Fast/2,** Fast/4, Fast/8, Fast/16	Set VR IA Slow Slew Rate for Deep Package C State ramp time; Slow slew rate equals to Fast divided by number, the number is 2, 4, 8, 16 to slow down the slew rate to help minimize acoustic noise
GT VR Domain		
Disable Fast PKG C State Ramp for GT Domain	**FALSE**, TRUE	This option needs to be configured to reduce acoustic noise during deeper C states. False: Don't disable Fast ramp during deeper C states; True: Disable Fast ramp during deeper C state
Slow Slew Rate for GT Domain	**Fast/2,** Fast/4, Fast/8	Set VR GT Slow Slew Rate for Deep Package C State ramp time; Slow slew rate equals to Fast divided by number, the number is 2, 4, 8 to slow down the slew rate to help minimize acoustic noise; divide by 16 is disabled
Core/IA VR Settings	Submenu	
Core/IA VR Domain		
VR Config Enable	Disabled, **Enabled**	VR Config Enable
Current AC Loadline	500	
Current DC Loadline	500	
Current Psi1 Threshold	16	
Current Psi2 Threshold	8	

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Feature	Options	Description
Current Psi3 Threshold	4	
Current Imon Slope	0	
Current Imon Offset	1	
Current VR Current Limit	148	
Current Tdc Current Limit	208	
Current Voltage Limit	1600	
AC Loadline	0	AC Loadline defined in 1/100 mOhms. A value of 100 = 1.00 mOhm, and 1255 = 12.55 mOhm. Range is 0-6249 (0-62.49 mOhms). 0 = AUTO/HW default. Uses BIOS mailbox command 0x2.
DC Loadline	0	DC Loadline defined in 1/100 mOhms. A value of 100 = 1.00 mOhm, and 1255 = 12.55 mOhm. Range is 0-6249 (0-62.49 mOhms). 0 = AUTO/HW default. Uses BIOS mailbox command 0x2.
PS Current Threshold1	16	PS Current Threshold1, defined in 1/4 A increments. A value of 400 = 100A. Range 0-512, which translates to 0-128A. 0 = AUTO. Uses BIOS VR mailbox command 0x3.
PS Current Threshold2	8	PS Current Threshold2, defined in 1/4 A increments. A value of 400 = 100A. Range 0-512, which translates to 0-128A. 0 = AUTO. Uses BIOS VR mailbox command 0x3.
PS Current Threshold3	4	PS Current Threshold3, defined in 1/4 A increments. A value of 400 = 100A. Range 0-512, which translates to 0-128A. 0 = AUTO. Uses BIOS VR mailbox command 0x3.
PS3 Enable	Disabled, **Enabled**	PS3 Enable/Disable. 0 - Disabled, 1 - Enabled.Uses BIOS VR mailbox command 0x3.
PS4 Enable	Disabled, **Enabled**	PS4 Enable/Disable. 0 - Disabled, 1 - Enabled.Uses BIOS VR mailbox command 0x3.
IMON Slope	0	IMON Slope defined in 1/100 increments. Range is 0-200. For a 1.25 slope, enter 125. 0 = AUTO. Uses BIOS VR mailbox command 0x4.
IMON Offset	0	IMON Offset defined in 1/1000 increments. Range is 0-63999. For an offset of 25.348, enter 25348. IMON Uses BIOS VR mailbox command 0x4.
IMON Prefix	**+**,-	Sets the offset value as positive or negative.
VR Current Limit	0	Voltage Regulator Current Limit (IccMax). This value represents the Maximum instantaneous current allowed at any given time. The value is represented in 1/4 A increments. A value of 400 = 100A. 0 means AUTO. Uses BIOS VR mailbox command 0x6.

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Feature	Options	Description
VR Voltage Limit	0	Voltage Limit (VMAX). This value represents the Maximum instantaneous voltage allowed at any given time. Range is 0 - 7999mV. Uses BIOS VR mailbox command 0x8.
TDC Enable	Disabled, **Enabled**	TDC Enable. 0- Disable, 1 - Enable
TDC Current Limit	0	TDC Current Limit, defined in 1/8A increments. Range 0-32767. For a TDC Current Limit of 125A, enter 1000. 0 = 0 Amps. Uses BIOS VR mailbox command 0x1A.
TDC Time Window	1 sec	VR TDC Time Window, value in seconds. 1s is default. Range from 1s to 448s.
TDC Lock	**Disabled**, Enabled	TDC Lock
IRMS	**Disabled**, Enabled	Enables/Disables IRMS – Current root mean square
GT VR Settings	Submenu	
RFI Settings	Submenu	
RFI Domain		
RFI Current Frequency	139.200MHz	
RFI Frequency	0	Sets desired RFI frequency, in increments of 100KHz. (For a frequency of 100.6MHz, enter 1006.)
FIVR Spread Spectrum	Disabled, **Enabled**	Enables or Disables the Spread Spectrum
RFI Spread Spectrum	0.5%, 1%, **1.5%**, 2%, 3%, 4%, 5%, 6%	Set the Spread Spectrum
Platform PL1 Enable	**Disabled**, Enabled	Enables/Disables Platform Power Limit 1 programming. If this option is enabled, it activates the PL1 value to be used by the processor to limit the average power of given time window.
Platform PL2 Enable	**Disabled**, Enabled	Enables/Disables Platform Power Limit 2 programming. If this option is disabled, BIOS will program the default values for Platform Power Limit 2.
Power Limit 4 Override	**Disabled**, Enabled	Enables/Disables Power Limit 4 override. If this option is disabled, BIOS will leave the default values for Power Limit 4.
C states	**Disabled**, Enabled	Enables/Disables CPU Power Management. Allows CPU to go to C states when it's not 100% utilized.
Thermal Monitor	Disabled, **Enabled**	Enables/Disables Thermal Monitor
Interrupt Redirection Mode Selection	**Fixed Priority,**Round robin,Hash Vector,No	Interrupts Redirection Mode Select for Logical Interrupts

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Feature	Options	Description
	Change	
Timed MWAIT	**Disabled**, Enabled	Enables/Disable Timed MWAIT Support
Custom P-state Table	Submenu	
Custom P-state Table		
Number of P states	**0**	Sets the number of custom P-states. At lease 2 states must be present.
EC Turbo Control Mode	**Disabled**, Enabled	Enables/Disables EC Turbo Control mode
Energy Performance Gain	**Disabled**, Enabled	Enables/Disables Energy Performance Gain.
EPG DIMM Idd3N	**26**	
EPG DIMM Idd3P	**11**	
Power Limit 3 Settings	Submenu	
Power Limit 3 Override	**Disabled**, Enabled	Enables/Disables Power Limit 3 override. If this option is disabled, BIOS will leave the hardware default values for Power Limit 3 and Power Limit 3 Time Window.
CPU Lock Configuration	Submenu	Enables/Disables Power Limit 3 override. If this option is disabled, BIOS will leave the hardware default values for Power Limit 3 and Power Limit 3 Time Window.
CFG Lock	Disabled, **Enabled**	Configure MSR 0Xe2[15], CFG Lock bit
Overclocking Lock	Disabled, **Enabled**	Enables/Disables Overclocking Lock (BIT 20) in FLEX RATIO(194) MSR

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7.2.2.2 Advanced > Power & Performance > GT – Power Management Control

Feature	Options	Description
RC6(Render Standby)*	Disabled, **Enabled**	Check to enable render standby support.
Maximum GT frequency	**Default Max Frequency**, 100Mhz, 150Mhz, 200Mhz, 250Mhz, 300Mhz, 350Mhz, 400Mhz, 450Mhz, 500Mhz, 550Mhz, 600Mhz, 650Mhz, 700Mhz, 750Mhz, 800Mhz, 850Mhz, 900Mhz, 950Mhz, 1000Mhz, 1050Mhz, 1100Mhz, 1150Mhz, 1200Mhz	Maximum GT frequency limited by the user. Choose between 100MHz (RPN) and 1350MHz (RP0). Value beyond the range will be clipped to min/max supported by SKU
Disable Turbo GT frequency	Enabled, **Disabled**	Enabled: Disables Turbo GT frequency. Disabled: GT frequency is not limited

7.2.3 Intel® Time Coordinated Computing

Feature	Options	Description
#AC Split Lock*	Enabled, **Disabled**	Enables or Disables Alignment Check Exception (#AC). When enabled, this will assert an #AC when any atomic operation has an operand that crosses two cache lines.
#GP Fault UC Lock	Enabled, **Disabled**	Enables or Disables GP Fault Exception (GP#). When enabled, this will assert an GP# when encountering a Lock to un-cacheable memory before the bus is locked.
Intel(R) TCC Authentication*	**OEM Enrolled Key**	Intel(R) TCC Authentication determines the key to be used. OEM Enrolled Key is built in by OEM. Non-OEM Enrolled Key can be added by the user.
Intel(R) TCC Mode*	Enabled, **Disabled**	Enables or Disables Intel(R) TCC Mode. When enabled, this will modify system settings to improve real-time performance. The full list of settings and their current state are displayed below when Intel(R) TCC mode is enabled.
Intel(R) TCC Mode Affected Settings		
IO Fabric Low Latency*	**Disabled**, Enabled	Enables or Disables IO Fabric Low Latency. This will turn off some power management in the PCH IO fabrics. This option provides the most aggressive IO Fabric performance setting. S3 state is NOT supported.

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Feature	Options	Description
GT CLOS*	**Disabled**, Enabled	Enables or Disables Graphics Technology(GT) Class of Service. Enable will reduce Gfx LLC allocation to minimize impact of Gfx workload on LLC
C states*	**Disabled**, Enabled	Enables/Disables CPU Power Management. Allows CPU to go to C states when it's not 100% utilized.
Intel(R) Speed Shift Technology*	Disabled, **Enabled**	Enable/Disable Intel(R) Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware-controlled P-states.
Intel(R) SpeedStep(tm)*	Disabled, **Enabled**	Allows more than two frequency ranges to be supported.
ACPI D3Cold Support*	**Disabled**, Enabled	Enables/Disables ACPI D3Cold support to be executed on D3 entry and exit
Low Power S0 Idle Capability*	**Disabled**, Enabled	This variable determines if we enable ACPI Lower Power S0 Idle Capability (Mutually exclusive with Smart connect). While this is enabled, it the disables 8254 timer for SLP_S0 support.
SA GV*	Disabled, Fixed to 1st Point,Fixed to 2nd Point, Fixed to 3rd Point, Fixed to 4th Point, **Enabled**	System Agent Geyserville. Can disable, fix to a specific point, or enable frequency switching.
Page Close Idle Timeout*	**Enabled**, Disabled	Page Close Idle Timeout Control
Power Down Mode*	**Auto**, No Power Down, APD,PPD-DLLoff	CKE Power Down Mode Control
RC6(Render Standby)*	Disabled, **Enabled**	Check to enable render standby support.
DMI Link ASPM Control*	**Disabled**,L0s, L1, Auto	The control of Active State Power Management of the DMI Link.
Legacy IO Low Latency*	Disabled, **Enabled**	Set to enable low latency of legacy IO. Some systems require lower IO latency irrespective of power. This is a tradeoff between power and IO latency.
CPU PCI Express Configuration	Submenu	
PCH PCI Express Configuration	Submenu	

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7.2.4 Advanced > Graphics Configuration

Feature	Options	Description
Nxp configuration	Info Only	
Data format and Color Depth	VESA 24 bpp JEIDA 24 bpp JEIDA/vesa 18 bpp	Data format and Color Depth select
LVDS Output Mode	Dual LVDS bus Single LVDS bus	Single/Dual mode select
DE Polarity	Active High Active Low	DE Polarity select
Vsync Polarity	Active High Active Low	Vsync Polaity select
Hsync Polarity	Active High Active Low	Hsync Polarity select
Spreading depth	No Spreading 0.5% 1.0% 1.5% 2.0% 2.5%	Clock frequency center spreading depth.
Integrated Display Configuration	Info only	
eDP/LVDS	**Disabled** Enabled	Enables/Disables eDP/LVDS
LFP Panel Type	**VBIOS Default** 640x480 800x600 1024x768 1280x1024 1400x1050 LVDS1 1400x1050 LVDS2 1600x1200 1366x768 1680x1050 1920x1200 1440x900	Select LFP panel used by Internal Graphics Device by selecting the appropriate setup item.

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Feature	Options	Description
	1600x900 1024x768 1280x800 1920x1080 2048x1536	
LVDS Backlight Mode	**EC Mode** GTT Mode	Select LVDS Backlight control function.
LVDS Backlight	Submenu	
LVDS Backlight Brightness	Value Range (0-255)	A change takes effect immediately. The value range starts by 0 and ends of 255.
DDI port 1	No Device Display Port HDMI **DisplayPort with HDMI/DVI Compatibility**	DDI port 1 function: choose between DisplayPort or HDMI
DDI port 2	No Device Display Port HDMI **DisplayPort with HDMI/DVI Compatibility**	DDI port 2 function: choose between DisplayPort or HDMI

7.2.5 Advanced > Power Management

Feature	Options	Description
Enable ACPI Auto Configuration	**Disabled**, Enabled	Enables or disables BIOS ACPI Auto Configuration.
Enable Hibernation	Disabled, **Enabled**	Enables or disables System ability to Hibernate (OS/S4 Sleep State). This option may not be effective with some operating systems.
ACPI Sleep State*	Suspend Disabled, **S3 (Suspend to RAM)**	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
LID Function	**Disabled**, Enabled	Enables/Disables LID Function
Sleep Function	Disabled, **Enabled**	Enables/Disables Sleep Button Function
ECO Mode*	**Disabled**, Enabled	Reduces the power consumption of the system, but after a shut down, you have to wait at least 5 seconds before you can restart the system.

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Feature	Options	Description
Power-Up Mode*	**Turn On,** Remain Off, Last State	Turn On:
ATTENTION: The Power-Up Mode only has effect,		
if the module is in ATX-Mode.		
Power Consumption	Submenu	

7.2.5.1 Advanced > Power Management > Power Consumption

Feature	Options	Description
Power Consumption	Info only	
Main Current	Read only	Displays input current.
Current Input Power	Read only	Displays input power.
RTC	Read only	Displays the sensed voltage based on hardware design.
5VSB	Read only	Displays the sensed voltage based on hardware design.
VIN	Read only	Displays the sensed voltage based on hardware design
3.3V	Read only	Displays the sensed voltage based on hardware design
VMEM	Read only	Displays the sensed voltage based on hardware design
3.3VSB	Read only	Displays the sensed voltage based on hardware design
VCORE	Read only	Displays the sensed voltage based on hardware design

7.2.6 Advanced > System Management

Feature	Options	Description
System Management	Info Only	
Version	Info Only	Displays SEMA Module Version.
SEMA Firmware	Info Only	Displays SEMA Firmware Version.
SEMA Flags	Submenu	Displays SEMA Flags
SEMA Features	Info	Displays SEMA Supported Features

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7.2.6.1 Advanced > System Management > SEMA Flags

Feature	Options	Description
SEMA Flags	Info Only	
BIOS Select	Info Only	
ATX/AT-Mode	Info Only	

7.2.7 Advanced > Thermal Management

Feature	Options	Description
Thermal Management	Info Only	
Critical Trip Point	**Disabled** 80 C 90 C 95 C	The value is the temperature threshold of the Critical Trip Point.
Passive Cooling Trip Point	**Disabled** 70 C 80 C 90 C 100 C	The value is the temperature threshold of the Passive Cooling Trip Point.
Watchdog ACPI Event Shutdown	**Disabled** Enabled	Watchdog ACPI Event Shutdown Enabled/Disabled
Temperature and Fan Speed	Submenu	

7.2.7.1 Advanced > Thermal Management > Temperature and Fan Speed

Feature	Options	Description
Temperatures	Info Only	
CPU Temperature	Info Only	
Current	Info Only	Displays Current CPU Temperature
Startup	Info Only	Displays Startup Board Temperature

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Feature	Options	Description
Min	Info Only	Displays Min Board Temperature
Max	Info Only	Displays Max Board Temperature
Board Temperatures	Info Only	
Current	Info Only	Displays Current Board Temperature
Startup	Info Only	Displays Startup Board Temperature
Min	Info Only	Displays Min Board Temperature
Max	Info Only	Displays Max Board Temperature

7.2.8 Advanced > Watchdog Timer

Feature	Options	Description
Watchdog Timer	Info only	
Power-Up Watchdog	**Disabled** Enabled	The Power Up Watchdog resets the system after a certain amount of time after power up. Pressing F12 druing start up disables the Power Up Watchdog
Timeout	**65535**	Here you can enter the time the Power Up Watchdog should wait until it resets the system. The value range starts by 24 and ends by 65535
RunTime Watchdog	**Disabled** Enabled	The RunTime Watchdog resets the system after a certain amount of time after power up.
Timeout	**24**	Here you can enter the time the Runtime Watchdog should wait until it resets the system. The value range starts by 30 and ends by 65535.

7.2.9 Advanced > Super IO Configuration

Feature	Options	Description
Super IO Configuration	Info only	
IT5121E Super IO Configuration	Submenu	System Super IO Chip Parameters.

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7.2.9.1.1 Advanced > Super IO Configuration > IT5121E Super IO Configuration

Feature	Options	Description
IT5121E Super IO Configuration		
Serial Port 1 Configuration	Submenu	
Serial Port 2 Configuration	Submenu	

Submenu: Super IO Configuration > Serial Port x Configuration

Feature	Options	Description
Serial Port 1 Configuration		
Serial Port 1 Configuration	Disabled, **Enabled**	Set Parameters of Serial Port 1
Device Settings	4;	
Change Settings	Auto, IO=3F8h; IRQ=4;, IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12;, IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12;, IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12;, IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12;	Select an optimal setting for Super IO Device
Serial Port 2 Configuration		
Serial Port 2 Configuration	Disabled, **Enabled**	Serial Port 2 Configuration
Device Settings	3;	Device Settings
Change Settings	Auto, IO=2F8h; IRQ=3;, IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12;, IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12;,	Change Settings

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Feature	Options	Description
	IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12;, IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12;, Normal, High Speed	

7.2.10 Advanced > Miscellaneous

Feature	Options	Description
Power Supply Unit	Emulate AT Mode **ATX Mode**	Select Emulation AT or ATX function. If this option set to [Emulation AT], BIOS will report no suspend functions (S3 & S4) to ACPI OS. In windows XP, it will make OS show shutdown message during system shutdown. ATX: OS will turn off system power when shutdown.
I2C Speed Control	**100 kbps** 400 kbps	I2C Speed Control
WOL From S5	OFF **ON**	This Config to control power on/off LAN in S5 State by SEMA(EC).
LID Function	**Disabled** Enabled	Enable/Disable LID function.
Sleep Function	Disabled **Enabled**	Enable/Disable Sleep Function.
Smart Battery Function	**Disabled** Enabled Auto	Enable/Disable Smart Battery function. Auto: disable Smart Battery function if charger IC not be detected.

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7.2.11 Advanced > USB Configuration

Feature	Options	Description
USB Configuration	Info Only	
USB Module Version	Info Only	Display USB Module Version
USB Controllers:	Info Only	Display USB Controllers is XHCI or EHCI.
USB Devices:	Info Only	Display attachment USB devices.
Legacy USB Support	**Enabled** Disabled Auto	Enables Legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications.
XHCI Hand-off	**Enabled** Disabled	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	Disabled **Enabled**	Enable / Disable USB Mass Storge Driver Support.
USB hardware delays and time-outs:	Info Only	
USB transfer rime-out	1 sec 5sec 10sec **20 sec**	The time-out value for Control, Bulk, and Interrupt transfers.
Device reset time-out	10 sec **20 sec** 30 sec 40 sec	USB mass storage device Start Unit command time-out.
Device power-up delay	**Auto** Manual	Maximum time the device will take before it properly reports itself to the Hot Controller. 'Auto' uses default value: for a Root po\rt it is 100 ms, for a Hub port the delay is taken form Hub descriptor.
Mass Storage Device	Info Only	

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7.2.12 Advanced > AMI Graphics Output Protocol Policy

Feature	Options	Description
Intel(R) Graphics Controller		
Intel(R) GOP Driver [21.0.10XX]		
Output Select	HDMI	Auto detect Output Interface
Output Select*	HDMI/DP/eDP	Manual select Output Interface
Brightness Setting	[Max-Value, Min-Value, Step-Value, Step-Value] = [0xFFFFFFFF, 0x00000000, 0x00000001, Brightness Setting]	Item shown when eDP detected Set Gop Brightness value
BIST Enable	**Disabled**, Enabled	Item shown when eDP detected Starts or stops the BIST on the integrated display panel.

7.2.13 Advanced > Serial Console Redirection

Feature	Options	Description
Console Redirection	**Disabled,** Enabled	To enable or disable console redirection of COMx.
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

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7.2.13.1 Advanced > Serial Console Redirection > Console Redirection Settings

Feature	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Configure the type of console emulation. Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speed.
Data Bits	7 **8**	Configure the number of data bits in each transmitted or received serial character for both serial ports.
Parity	**None** Even Odd	Configures if parity bit is generated (transmit data) or checked. A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.
Stop Bits	**1** 2	Configures the number of stop bits transmitted and received in each serial character for both serial ports. Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware Software	Configures flow control for console redirection. Hardware flow control uses RTC/CTS. Software flow control uses XON/XOFF.
VT-UTF8 Combo Key Support	Disabled **Enabled**	Enable VT-UTF8 combination key support for ANSI/VT100 terminals.
Recorder Mode	**Disabled** Enabled	With this mode enabled only text will be sent. This is to capture terminal data.
Resolution 100x31	**Disabled** Enabled	Enables or disables extended terminal resolution.
Putty KeyPad	**VT100** LINUX XTERMR6	Select Function Keys and Key Pad on Putty.

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Feature	Options	Description
	SCO ESCN VT400	

7.2.14 Advanced > Network Stack Configuration

Feature	Options	Description
Network Stack	**Disabled**, Enabled	Enable/Disable UEFI Network Stack
IPv4 PXE Support	**Disabled**, Enabled	Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.
IPv4 HTTP Support	**Disabled**, Enabled	Enable/Disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.
IPv6 PXE Support	**Disabled**, Enabled	Enable/Disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.
IPv6 HTTP Support	**Disabled**, Enabled	Enable/Disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.
PXE boot wait time	[Max-Value, Min-Value, Step-Value] =[0x05, **0x00**, 0x01]	Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.
Media detect count	[Max-Value, Min-Value, Step-Value] =[0x32, **0x01**, 0x01]	Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

7.2.15 Advanced > Trusted Computing

Feature	Options	Description
Security Device Support	**Disable**, Enable	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.
NO Security Device Found		

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7.3 Chipset

Feature	Options	Description
System Agent (SA) Configuration	submenu	
PCH-IO Configuration	submenu	

7.3.1 Chipset > System Agent (SA) Configuration

Feature	Options	Description
Stop Grant Configuration	Auto	Automatic/Manual stop grant configuration
VT-d	**Enabled,** Disabled	VT-d capability
Control Iommu Pre-boot Behavior	**Disable IOMMU** Enable IOMMU during boot	Enable IOMMU in Pre-boot environment (If DMAR table is installed in DXE and If VTD_INFO_PPI is installed in PEI.)
X2APIC Opt Out	Enabled**, Disabled**	Enable/Disable X2APIC_OPT_OUT bit
DMA Control Guarantee	**Enabled,** Disabled	Enable/Disable DMA_CONTROL_GUARANTEE bit
WRC Feature	Enabled**, Disabled**	Enable/Disable SA WRC(Write Cache) Feature of IOP. When enabled, supports IO devices allocating onto the ring and into LLC.
Above 4GB MMIO BIOS assignment	**Enabled,** Disabled	Enable/Disable above 4GB MemoryMappedIO BIOS assignment\n\nThis is enabled automatically when Aperture Size is set to 2048MB.
IPU Device (B0:D5:F0)	Enabled**, Disabled**	Enable/Disable SA IPU Device.
IPU 1181 Dash Camera	Enabled**, Disabled**	Enable/Disable SA IPU 1181 Dash Camera support.

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7.3.1.1 Chipset > System Agent (SA) Configuration > Memory Configuration

Feature	Options	Description
Memory RC Version	**Info-only**	
Memory Frequency	**Info-only**	
Memory Timings (tCL-tRCD-tRP-tRAS)	**Info-only**	
Controller x Channel x Slot x	**Info-only**	
Size	**Info-only**	
Number of Ranks	**Info-only**	
Manufacturer	**Info-only**	
Memory Test on Warm Boot	**Enabled,** Disabled	Enable Or Disable Base Memory Test Run on Warm Boot
Maximum Memory Frequency	**Auto** 1067 1333 1400 1600 1800 1867 2000 2133 2200 2400 2600 2667 2800 2933 3000 3200	Maximum Memory Frequency Selections in Mhz. Valid values should match the refclk, i.e. divide by 133 or 100
Max TOLUD	**Dynamic** 1 GB 1.25 GB 1.5 GB 1.75 GB 2 GB	Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller

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Feature	Options	Description
	2.25 GB 2.5 GB 2.75 GB 3 GB 3.25 GB 3.5 GB	
SA GV	**Enabled,** Disabled	System Agent Geyserville. Can disable, fix to a specific point, or enable frequency swithing.
Controller 0, Channel X DIMM Control	**Enabled,** Disabled	Controller 0, Channel X DIMM Control Support - Enable or Disable Dimms on Controller 0, Channel X.
Controller 1, Channel X DIMM Control	**Enabled,** Disabled	Controller 1, Channel X DIMM Control Support - Enable or Disable Dimms on Controller 1, Channel X.
Force Single Rank	**Disabled,** Enabled	When enabled, only Rank 0 will be used in each DIMM
In-Band ECC Support (Industrial SKU only)	**Enabled,** Disabled	Enable/Disable In-Band ECC. Either the IBECC or the TME can be enabled.

7.3.1.2 Chipset > System Agent (SA) Configuration > Graphics Configuration

Feature	Options	Description
Skip Scanning of External Gfx Card	**Disabled**, Enabled	If enabled, it will not scan for External Gfx Card on PEG and PCH PCIE Ports
Primary Display	**Auto**, IGFX, PEG Slot, PCH PCI, HG	Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select HG for Hybrid Gfx.
External Gfx Card Primary Display Configuration	submenu	
Internal Graphics	**Auto**, Disabled, Enabled	Keep IGFX enabled based on the setup options.
GTT Size	2MB, 4MB, **8MB**	Select the GTT Size
Aperture Size	128MB, **256MB**, 512MB, 1024MB	Select the Aperture Size
DVMT Pre-Allocated	0M, 32M, 64M, 96M, 128M, 160M, 4M, 8M, 12M, 16M, 20M, 24M, 28M, 32M/F7, 36M, 40M, 44M, 48M, 52M, 56M, **60M**	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.

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Feature	Options	Description
Intel Graphics Pei Display Peim	Enabled, **Disabled**	Enable/Disable Pei (Early) Display

7.3.1.3 Chipset > System Agent (SA) Configuration > MIPI Camera Configuration

Feature	Options	Description
CVF Support	**Disabled**, Enabled	Disables/Enables CVF using either Native IOs or USB IOs Expansion.
Control Logic 1	Disabled, **Enabled**	Control Logic 1
Control logic options	submenu	Control logic options
Control logic 2	Disabled, **Enabled**	Control logic 2
Control logic options	submenu	Control logic options
Camera1	Disabled, **Enabled**	Camera1
Link options	submenu	Link options
Camera2	Disabled, **Enabled**	Camera2
Link options	submenu	Link options

7.3.2 Chipset > PCH-IO Configuration

Feature	Options	Description
PCI Express Configuration	Submenu	
SATA Configuration	Submenu	
USB Configuration	Submenu	
Security Configuration	Submenu	
HD Audio Configuration	Submenu	
Seriallo Configuration	Submenu	
SCS Configuration	Submenu	

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Feature	Options	Description
PCH LAN Controller	Info-Only	No GbE Region
Port 80h Redirection	Fixed setting - LPC Bus	Control where the Port 80h cycles are sent.
Enhance Port 80h LPC Decoding	**Enabled**, Disabled	Supports the word/dword decoding of port 80h behind LPC
Enable TCO Timer	**Disabled**, Enabled	Enable/Disable TCO timer. When disabled, it disables PCH ACPI timer, stops TCO timer, and ACPI WDAT table will not be published.
Pcie Ref Pll SSC	**Auto**, 0.0%, 0.1%, 0.2%, 0.3%, 0.4%, 0.5%, 0.6%, 0.7%, 0.8%, 0.9%, 1.0%, 1.1%, 1.2%, 1.3%, 1.4%, 1.5%, 1.6%, 1.7%, 1.8%, 1.9%, 2.0%, Disable	Pcie Pll SSC percentage.AUTO - Keep hw default, no BIOS override. Range is 0.0%-2.0%.
SPD Write Disable	**TRUE**, FALSE	Enable/Disable setting SPD Write Disable. For security recommendations, SPD write disable bit must be set.

7.3.2.1 Chipset > PCH-IO Configuration > PCI Express Configuration

Feature	Options	Description
DMI Link ASPM Control	**Disabled**, L0s, L1, L0sL1, Auto	The control of Active State Power Management of the DMI Link.
Port8xh Decode	**Disabled**, Enabled	PCI Express Port8xh Decode Enable/Disable.
PCIE Ports 9-12 Configuration	**4x1 Port,** 1x2 2x1 Port, 2x2 Port, 1x4 Port	To configure PCI-E Port 9-12 of PCH.[4X1]:Port 1-4 (x1) and Port 8 (x1) / [1x2 2x1]:Port 1 (x2), Port 2 (disabled), Ports 3 and Port 4 (x1) / [2x2]:Port 1-2 (x2) and Port 3-4 (x2) / [1x4]:Port 1 (x4), Ports 2-4 (disabled)
Select PCIE/SATA Combo port 1	**PCIE port** SATA port	Notes: Please make sure the system boots completed after changing the configuration.\r\nDo Not Attempt to Shut Down Your Computer, doing that may lead to system malfunction.
PCI Express Root Port 3	Submenu	
PCI Express Root Port 4	Submenu	
PCI Express Root Port 7	Submenu	
PCI Express Root Port 9	Submenu	
PCI Express Root Port 10	Submenu	

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Feature	Options	Description
PCI Express Root Port 11	Submenu	.
PCI Express Root Port 12	Submenu	

7.3.2.1.1 Chipset > PCH-IO Configuration > PCI Express Configuration > PCI Express Root Port#

Feature	Options	Description
PCI Express Root Port	Disabled **Enable**	Control the PCI Express Root Port.
Connection Type	Built-in **Slot**	Built-In: a built-in device is connected to this rootport. SlotImplemented bit will be clear. Slot: this rootport connects to user-accessible slot. SlotImplemented bit will be set.
ASPM	**Disabled** L0s L1 L0sL1 Auto	Set the ASPM Level. Force L0s - Force all links to L0s State Auto - BIOS auto configure; Disabled - Disables ASPM
L1 Substates	Disabled L1.1 **L1.1 & L1.2**	PCI Express L1 Substates settings.
L1 Low	Disabled **Enable**	PCI Express L1 Low Substate Enable/Disable.
ACS	Disabled **Enable**	Enable/Disable Access Control Services Extended Capability
PTM	Disabled **Enable**	Enable/Disable Precision Time Measurement
DPC	**Disabled** Enable	Enable/Disable Downstream Port Containment
EDPC	Disabled **Enable**	Enable/Disable Rootport extensions for Downstream Port Containment
URR	**Disabled** Enable	PCI Express Unsupported Request Reporting Enable/Disable.
FER	**Disabled** Enable	PCI Express Device Fatal Error Reporting Enable/Disable.

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Feature	Options	Description
NFER	**Disabled** Enable	PCI Express Device Non-Fatal Error Reporting Enable/Disable.
CER	**Disabled** Enable	PCI Express Device Correctable Error Reporting Enable/Disable.
CTO	**Disabled** Enable	PCI Express Completion Timer TO Enable/Disable
SEFE	**Disabled** Enable	Root PCI Express System Error on Fatal Error Enable/Disable.
SENFE	**Disabled** Enable	Root PCI Express System Error on Non-Fatal Error Enable/Disable.
SECE	**Disabled** Enable	Root PCI Express System Error on Correctable Error Enable/Disable.
PME SCI	Disabled **Enable**	PCI Express PME SCI Enable/Disable.
Hot Plug	**Disabled** Enable	PCI Express Hot Plug Enable/Disable.
Advanced Error Reporting	Disabled **Enable**	Advanced Error Reporting Enable/Disale.
PCIe Speed	**Auto** Gen1 Gen2 Gen3	Configure PCIe Speed.
Transmitter Half Swing	**Disabled** Enabled	Transmitter Half Swing Enable/Disable.
Detect Non-Compiance	**Disabled** Enable	Detect Non-Compliance PCI Express Device. If enabled, it will take more time at POST time.
Detect Timeout	**0**	The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.
Extra Bus Reserved	**0**	Extra Bus Reserved (0-7) for bridges behind this Root Bridge.
Reseved Memory	**10**	Reserved Memory for this Root Bridge (1-20) MB.
Reserved I/O	**4**	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.
PCH PCIe LTR Configuration	Info only	

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Feature	Options	Description
LTR	Disabled **Enable**	PCH PCIE Latency Reporting Enable/Disable.
Snoop Latency Override	Disabled Manual **Auto**	Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow."
Non Snoop Latency Override	Disabled Manual **Auto**	Non Snoop Latency Override for PCH PCIE. Disabled: Disable override.Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
LTR Lock	**Disabled** Enable	PCIE LTR Configuration Lock

7.3.2.2 Chipset > PCH-IO Configuration > SATA Configuration

Feature	Options	Description
SATA Controller(s)	Disabled, **Enabled**	Enable/Disable SATA Device.
SATA Mode Selection	AHCI	Determines how SATA controller(s) operate.
SATA Controller Speed	Default, Gen1, **Gen2**, Gen3	Indicates the maximum speed the SATA controller can support.
SATA Test Mode	**Disabled**, Enabled	Test Mode Enable/Disable (Loop Back).
Aggressive LPM Support	Disabled, **Enabled**	Enable PCH to aggressively enter link power state.
Serial ATA Port X	Info-Only	
Software Preserve	Info-Only	
Port X	Disabled, **Enabled**	Enable or Disable SATA Port
Hot Plug	**Disabled**, Enabled	Designates this port as Hot Pluggable.
Configured as eSATA	Info Only	

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Feature	Options	Description
External	**Disabled**, Enabled	Marks this port as external.
Spin Up Device	**Disabled**, Enabled	If enabled for any of ports Staggerred Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise, all drives spin up at boot.
SATA Device Type	**Hard Disk Drive**, Solid State Drive	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive
Topology	**Unknown** ISATA Direct Connect Flex M2	
SATA Port X DevSlp	**Disabled**, Enabled	
DITO Configuration	**Disabled**, Enabled	Enable/Disable DITO Configuration
DITO Value	**625**	DITO Value
DM Value	**15**	DM Value

7.3.2.3 Chipset > PCH-IO Configuration > USB Configuration

Feature	Options	Description
xDCI Support	Disabled, **Enabled**	Enable/Disable xDCI (USB OTG Device).
USB2 PHY Sus Well Power Gating	Disabled, **Enabled**	Select 'Enabled' to enable SUS Well PG for USB2 PHY. This option has no effect on PCH-H
USB PDO Programming	Disabled, **Enabled**	Select 'Enabled' if Port Disable Override functionality is used.
USB Overcurrent	Disabled, **Enabled**	Select 'Disabled' for pin-based debug. If pin-based debug is enabled but USB overcurrent is not disabled, USB DbC does not work.
USB Overcurrent Lock	Disabled, **Enabled**	Select 'Enabled' if Overcurrent functionality is used. Enabling this will make xHCI controller consume the Overcurrent mapping data
USB Audio Offload	Disabled, **Enabled**	Enable/Disable USB Audio Offload functionality
Enable HSII on xHCI	Disabled, **Enabled**	Enable/Disable HSII feature. It may lead to increased power consumption.
USB3.1 Portx Speed Selection	0	Port Selection value in decimal for Gen1; Default - Gen2; Bit 0 corresponds to Port 0 and so on

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Feature	Options	Description
USB Port Disable Override	**Disabled**, Select Per-Pin	Selectively Enable/Disable the corresponding USB port from reporting a Device Connection to the controller.

7.3.2.4 Chipset > PCH-IO Configuration > Security Configuration

Feature	Options	Description
RTC Memory Lock	Disabled, **Enabled**	Enable will lock bytes 38h-3Fh in the lower/upper 128-byte bank of RTC RAM
BIOS Lock	**Disabled**, Enabled	Enable/Disable the PCH BIOS Lock Enable feature. Required to be enabled to ensure SMM protection of flash.
Force unlock on all GPIO pads	**Disabled**, Enabled	If Enabled BIOS will force all GPIO pads to be in unlocked state

7.3.2.5 Chipset > PCH-IO Configuration > HD Audio Configuration

Feature	Options	Description
HD Audio	Disabled **Enabled**	Control Detection of the HD-Audio device.

7.3.2.6 Chipset > PCH-IO Configuration > Serial IO Configuration

Feature	Options	Description
I2C0 Controller	Disabled**, Enabled**	Enables/Disables Seriallo Controller
I2C1 Controller	Disabled**, Enabled**	Enables/Disables Seriallo Controller
I2C5 Controller	Disabled**, Enabled**	Enables/Disables Seriallo Controller
SPI0 Controller	Disabled**, Enabled**	Enables/Disables Seriallo Controller
UART0 Controller	**Disabled,** Enabled, Communication port (COM)	Enables/Disables Seriallo Controller

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Feature	Options	Description
UART1 Controller	**Disabled,** Enabled, Communication port (COM)	Enables/Disables Seriallo Controller
UART2 Controller	**Disabled,** Enabled, Communication port (COM)	Enables/Disables Seriallo Controller
GPIO IRQ Route	**IRQ14,** IRQ15	Route all GPIOs to one of the IRQ.
Serial IO UART0 Settings	Submenu	
Serial IO UART2 Settings	Submenu	

7.3.2.7 Chipset > PCH-IO Configuration > SCS Configuration

Feature	Options	Description
eMMC 5.1 Controller	Disabled**, Enabled**	Enables/Disables eMMC Controller
eMMC 5.1 HS400 Mode	Disabled**, Enabled**	Enables/Disables SCS eMMC 5.1 HS400 Mode

7.4 Security

7.4.1 Security > Password Description

Feature	Options	Description
Password Description	Info only	
Setup Administrator Password	Enter Password	Set Setup Administrator Password
User Password	Enter Password	Set User Password
Secure Boot	Submenu	

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7.4.2 Security > Secure Boot Menu

Feature	Options	Description
Secure Boot	**Disabled** Enabled	Secure Boot feature is Active if Secure Boot is enabled, platform Key(PK) is enrolled and the System is in User mode, The mode change requires platform reset
Secure Boot Mode	**Standard** Custom	Secure Boot mode options: Standard or Custom.In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication
Restore Factory Keys		Force System to User Mode.Install factory default Secure Boot key databases
Reset To Setup Mode		Delete all Secure Boot Key databases from NVRAM.
Key Management	**Submenu**	Enables expert users to modify. Secure Boot Policy variables without variable authentication.

7.5 Boot

7.5.1 Boot > Boot Configuration

Feature	Options	Description
Boot Configuration	Info only	
Setup Prompt Timeout	**1**	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
Bootup NumLock State	On **Off**	Select the keyboard NumLock state
Quiet Boot	Disabled **Enabled**	Enables or disables Quiet Boot option
Fast Boot	Disabled **Enabled**	Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for the BBS boot option.

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Feature	Options	Description
SATA Support	**Last Boot SATA Devices Only** All Sata Devices	If Last Boot SATA Devices Only is selected, only the last boot SATA device will be available in POST. If All SATA devices is selected, all SATA devices will be available in OS and POST.
VGA Support	Auto **EFI Driver**	If set to Auto, only the installed Legacy OpRom with Legacy OS and logo will NOT be shown during POST. The EFI driver will still be installed with EFI OS.
USB Support	Disabled **Full Initial** Partial Initial	If disabled, all USB devices will NOT be available until after the OS boots. If set to Partial Initial, USB mass storage and specific USB ports/devices will NOT be available before the OS boots. If enabled, all USB devices will be available in both OS and POST.
PS2 Devices Support	**Disabled** Enabled	If disabled, PS2 devices will be skipped.
NetWork Stack Driver Support	**Disabled** Enabled	If Disabled, Network Stack Driver will be skipped.
Redirection Support	Disabled **Enabled**	If disable, the Redirection function will be disabled.
Boot Mode select	**UEFI** LEGACY	Select boot mode LEGACY/UEFI
FIXED BOOT ORDER Priorities	Info only	
UEFI Hard Disk Drive BBS Priorities	**Submenu**	
UEFI Application Boot Priorities	**Submenu**	

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7.6 Save & Exit

Feature	Options	Description
Save Changes and Exit		Exit system setup after saving the changes.
Discard Changes and Exit		Exit system setup without saving any changes.
Save Changes and Reset		Reset the system after saving the changes.
Discard Changes and Reset		Reset system setup without saving any changes.
Save Options	Info only	
Save Changes		Save Changes done so far to any of the setup options.
Discard Changes		
Restore Defaults		
Save as User Defaults		Save the changes done so far as User Defaults.
Restore User Defaults		Restore the user defaults to all the setup options.
Boot Override	Info only	

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8. BIOS Checkpoints, Beep Codes

This document section lists checkpoints and beep codes generated by AMI Aptio BIOS. The checkpoints defined are inherent to the AMIBIOS generic core and do not include any chipset or board-specific checkpoint definitions.

Checkpoints and Beep Codes Definition

A checkpoint is either a byte or word value output to I/O port 80h. The BIOS outputs checkpoints throughout the boot block and Power-On Self-Test (POST) to indicate the task the system is currently executing. Checkpoints are very useful for debugging problems that occur during the preboot process.

Beep codes are used by the BIOS to indicate a serious or fatal error. They are used when an error occurs before the system video has been initialized and generated by the system board speaker.

Aptio Boot Flow

While performing the functions of the traditional BIOS, Aptio 5.x core follows the firmware model described by the Intel Platform Innovation Framework for EFI ("the Framework"). The Framework refers to the following "boot phases", which may apply to various status codes & checkpoint descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization[1]
- Driver Execution Environment (DXE) – main hardware initialization[2]
- Boot Device Selection (BDS) – system setup, pre-OS user interface & selecting a bootable device (CD/DVD, HDD, USB, Network, Shell, …)

Viewing BIOS Checkpoints

Viewing all checkpoints generated by the BIOS requires a checkpoint card, also referred to as a POST Card or POST Diagnostic Card. These are PCI add-in cards that show the value of I/O port 80h on a LED display.

Some computers display checkpoints in the bottom right corner of the screen during POST. This display method is limited- since it only displays checkpoints that occur after the video card has been activated.

Keep in mind that not all computers using AMI Aptio BIOS enable this feature. In most cases, a checkpoint card is the best tool for viewing AMI Aptio BIOS checkpoints.

[1]Analogous to "boot block" functionality of legacy BIOS
[2]Analogous to "POST" functionality in legacy BIOS

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8.1 Status Code Ranges

Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

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8.2 Standard Status Codes

8.2.1 SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization

SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

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8.2.2 SEC Phase > SEC Beep Codes

None.

8.2.3 SEC Phase > PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information

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Status Code	Description
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.

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Status Code	Description
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self-test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes

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Status Code	Description
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

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8.2.4 SEC Phase > PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

8.2.5 SEC Phase > DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started

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Status Code	Description
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration

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Status Code	Description
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)

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Status Code	Description
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password

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Status Code	Description
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

8.2.6 SEC Phase > DXE Beep Codes

# of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

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8.2.7 SEC Phase > ACPI/ASL Checkpoint

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

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8.3 OEM-reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

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9. Software Support

9.1 Yocto

Yocto is available on ADLINK Github > https://github.com/ADLINK/meta-adlink-x86-64bit

9.2 Ubuntu

Ubuntu is supported from kernel 5.15 and up.

9.3 Windows

Windows 11 is supported.

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10. Mechanical and Thermal

10.1 Module Dimensions

PCB dimension: 82 x 50 x 1.2 mm, 12 layer PCB

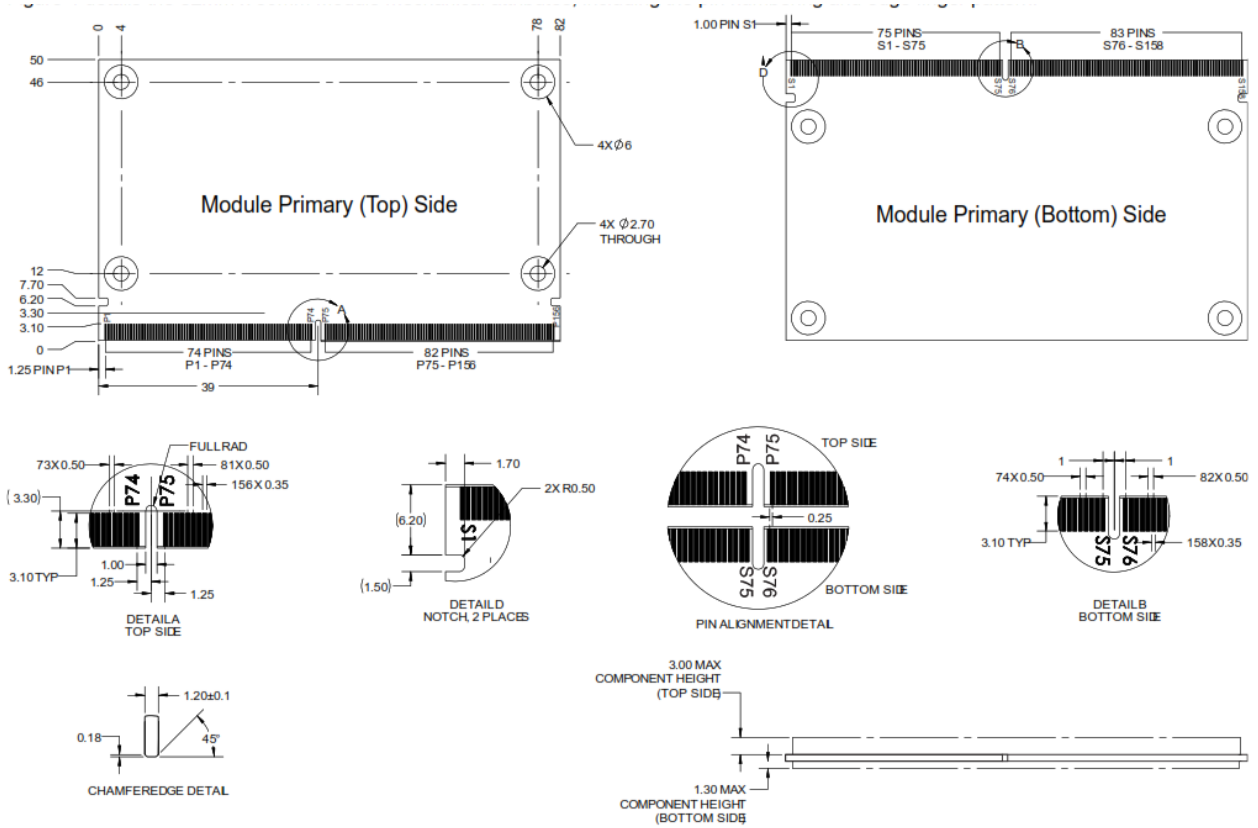
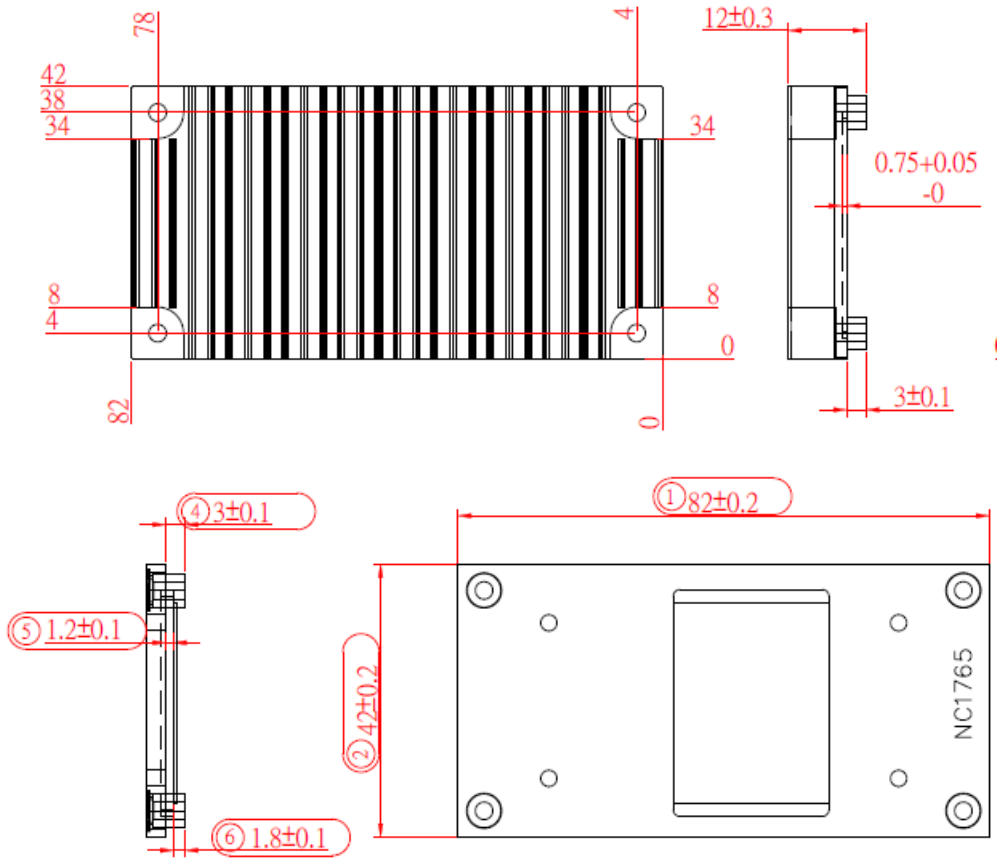


Figure 4 – Module dimensions

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10.2 Thermal Solutions

For optimal performance, LEC-ALN / ASL has to be cooled by a passive heat sink / heat spreader, which is optionally available for purchase.



HTS-sALN	Heat spreader for LEC-ALN / ASL
THS-sALN	Low profile heat sink for LEC-ALN / ASL

Figure 5 – Thermal solutions

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