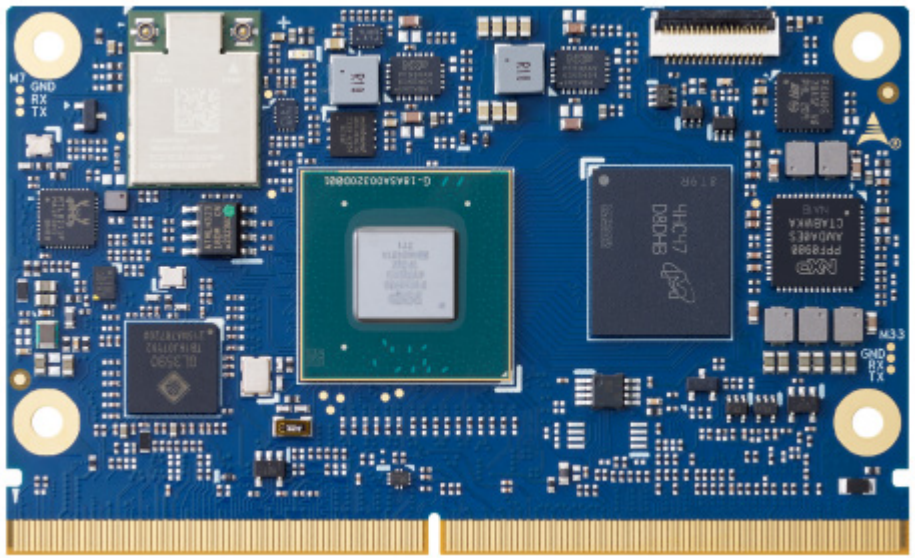
LEC-IMX95

User's Guide



SMARC module

Revision:	Rev. 1.2
Date:	2025-11-24
Part Number:	50M-72520-1020

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Revision History

Revision	Description	Date	Author
1.0	Initial release	2025-08-18	AL
1.1	Specifications updated	2025-11-05	AL
1.2	Specifications updated	2025-11-24	AL

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Preface

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Safety Instructions

For user safety, please read and follow all Instructions, **WARNING**s, **CAUTION**s, and **NOTE**s marked in this manual and on the associated equipment before handling/operating the equipment.

Read these safety instructions carefully.

- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

Conventions

The following conventions may be used throughout this manual, denoting special levels of information

Note: This information adds clarity or specifics to text and illustrations.

Caution: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.

Warning: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

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1. Introduction

1.1 LEC-IMX95

The ADLINK LEC-IMX95 is a SMARC module based on the NXP i.MX 95 series, featuring integrated Mali graphics and an NPU.
It supports up to 16 GB of LPDDR5 memory and up to 256 GB of eMMC storage, and is available with a rugged operating temperature range and a low-power envelope, making it ideal for mission-critical, fanless edge computing applications that require safety and reliability at all times.

1.2 The SMARC Form Factor

The SMARC ("Smart Mobility ARChitecture") is a versatile small form factor Computer-on-Module (CoM) specification designed for applications that require low power consumption, low cost, and high performance. The modules typically use ARM SoCs that are similar or identical to those found in many common devices, such as tablet computers and smartphones. Alternative low-power SoCs and CPUs, such as x86 processors designed for tablets and other RISC-based CPUs, may also be used. The typical power envelope of a module is under 6W.

Two module sizes are defined: 82 mm x 50 mm and 82 mm x 80 mm. Each module PCB includes 314 edge fingers that mate with a low-profile 314-pin, 0.5 mm pitch, right-angle connector. (This connector is sometimes identified as a 321-pin connector, but 7 pins are reserved for the key and therefore not used.)

The modules serve as building blocks for both portable and stationary embedded systems. The core CPU and supporting circuits — including DRAM, boot flash, power sequencing, CPU power supplies, Gigabit Ethernet (GbE), and a single-channel LVDS display transmitter — are integrated on the module. These modules are used in conjunction with application-specific carrier boards that implement additional features such as audio CODECs, touch controllers, wireless devices, and more. This modular approach enables scalability, faster time to market, and easy upgradability, while maintaining low cost, low power consumption, and compact physical size.

SGeT STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

SMARC module and carrier specifications are available at: https://sget.org/standards/smarc/

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1.3 Module Feature List

Memory: LPDDR5 4 to 16GB solder down memory

eMMC: BGA 32 ~256 GB supporting eMMC 5.1 standard

QSPI: QSPI boot flash as BOM option

WIFI / BT: standard M.2 1216 footprint available, AW-CM276NF as BOM option to provide WIFI / BT

GPIO's: 14 GPIO's via MCU and CPU

LAN: Gbe built in Mac's connected to RTL8211 PHY

POWER: standard NXP PMIC solution

Graphics: Brings LVDS0,1 / DSI / HDMI (via DSI2HDMI) to the carrier with BOM options

USB: OTG straight from SoC, Other USB's over USB3/2 HUB, 2nd USB port to Bluetooth

AUDIO: I2S on carrier

PCIe: 2x single lane GEN3

CAN: 2x CAN FD

BOOT SELECT: Various boot supported (Sd, eMMC, Serial boot, SPI boot), managed by MCU

SECURITY: Built in HAB

All other signals follow 2.2 standards.

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2. Specifications

2.1 Core System

CPU

Up to 6x ARM Cortex-A55 @2.0 GHz

1x ARM Cortex-M7 on flex domain

1x ARM M33 on low power real time domain

Memory

Several BOM options up to 16 GB LPDDR5

L2 Cache

Per core >32KB I-Cache, 32KB D-Cache, 64KB L2 cache

Unified > 512KB L3 cache

security

Crypto, Tamper detection, secure clock, Secure boot, eFuse key storage, random number generator

2.1.1 GPU

GPU Core

Mali G310

GPU Feature Support

3D GPU supporting 50 GFLOPs

OpenGL®ES 3.2

Vulkan ®1.2

OpenCL 3.0

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VPU Feature Support

- 4Kp30 H.265 and H.264 encode and decode
- 1 x JPEG Encoder
- 1 x JPEG Dec

2.1.2 Display Interfaces

MIPI DSI

1x MIPI DSI 4 lane Compliant to MIPI-DSI standard v1.2

Maximum resolution 4Kp30 (HDMI removed when using DSI)

LVDS

Dual Channel LVDS port 18/24 bit

resolutions up to 1080p60

HDMI

The HDMI interface is derived from the on chip DSI port and goes over a DSI to HDMI bridge (build option)

2.2 Camera

Supports one 4-lane MIPI CSI-2 input; a second 2-lane input shares the DSI interface

2.3 Audio

Supports I2S codec for high performance

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2.4 Dual Wired Ethernet

Primary LAN

MAC 10/100/1000 TSN Ethernet Controller on SoC with RTL8211 PHY

Supports 10/100/1000-Mbps data transfer rates, both full-duplex and half-duplex

Secondary LAN

MAC 10/100/1000 TSN Ethernet Controller on SoC with RTL8211 PHY

Supports 10/100/1000-Mbps data transfer rates, both full-duplex and half-duplex

2.5 Wi-Fi / Bluetooth

M.2 12-16 industry standard footprint with Azurewave AW-CM276NF (build option)

2.6 Extension busses

PCIe
2x single lane REV 3.0

USB
2x USB3.0, 3x USB2.0 (via HUB)

UART
Four UART interfaces SER0/2 (4W) ,1,3 (2W). Ser 2 is shared with SPI1

CANbus
CAN0,1 supports CAN2.0B only, or a mix of CAN2.0B and CAN FD modes, with data bit rates up to 8 Mbps

SPI
2x SPI (SPI 1 is shared with UART and is unavailable when the UART function is selected)

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I2S

1x I2S interface with audio resolution from 16-bits to 32-bits and a sample rate of up to 192KHz (see Audio Codec support)

I2C

Three I2C interfaces

- Support for 7-bit mode
- Software programmable clock frequency of 100 kbit/s in Standard-mode,

400 kbit/s in the Fast-mode or 1 Mbit/s in Fast-mode Plus

GPIO

14x GPIO with interrupt

2.7 System Storage

SDIO

1x SDIO (4-bit) compatible with SD3.0, MMC ver. 4.51 to edge connector

eMMC

32 ~ 256 GB (build option)

Compatible with eMMC specification 5.0 and 5.1

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2.8 Board Controller

BMC lite for power sequence

SEMA BMC Error Code

Exception Code	Error Code
0	NOERROR
2	NO_VIN
3	NO_SDM_RESIN_N
4	NO_SDM_RESIN_N

2.9 Debug Header

JTAG

2.10 FAN Control

Available from CPU

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2.11 Power

Power Modes:	ON / OFF / SUSPEND	
Power on / off behaviour same as x86	*ATX (hold off boot until PWRBTN) / AT (always boot)*	
Voltage Input:	5.0V +/- 5%	
Operating Temperatures (vs power input)		
Standard Operating Temperature:	0 to 60°C	commercial grade BOM (memory, eMMC, USB hub, SOC)
Extreme Rugged Operating Temperature:	-40 + 85°C	industrial grade BOM (memory, eMMC, USB hub, SOC)

Environmental

Humidity:	5-90% RH operating, non-condensing 5-95% RH storage (and operating with conformal coating).
EMI:	EN55022 Class B inside an enclosure
Shock and Vibration:	HALT Testing, with test report that confirms Extended Operating Temp range during and after vibration. Separate Shock test report to MIL-STD-202F, Method 213B, Table 213-I, Condition A. IN ADDITION: When installed on baseboard shall operate under 18 sawtooth mechanical shocks (3 shocks in each direction) with a peak acceleration of 40g for a duration of 18 msec each and 75g for a duration of 6 msec each. Capable of supporting Random Vibration: MIL-STD-202F, Method 214A, Table 214-I, Condition D. If HALT testing shows equal or better performance, a separate vibration test report is not necessary.
MTBF:	300,000 hrs (at 40 C), 100,000 hrs (at 85 C),

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3. Block Diagram

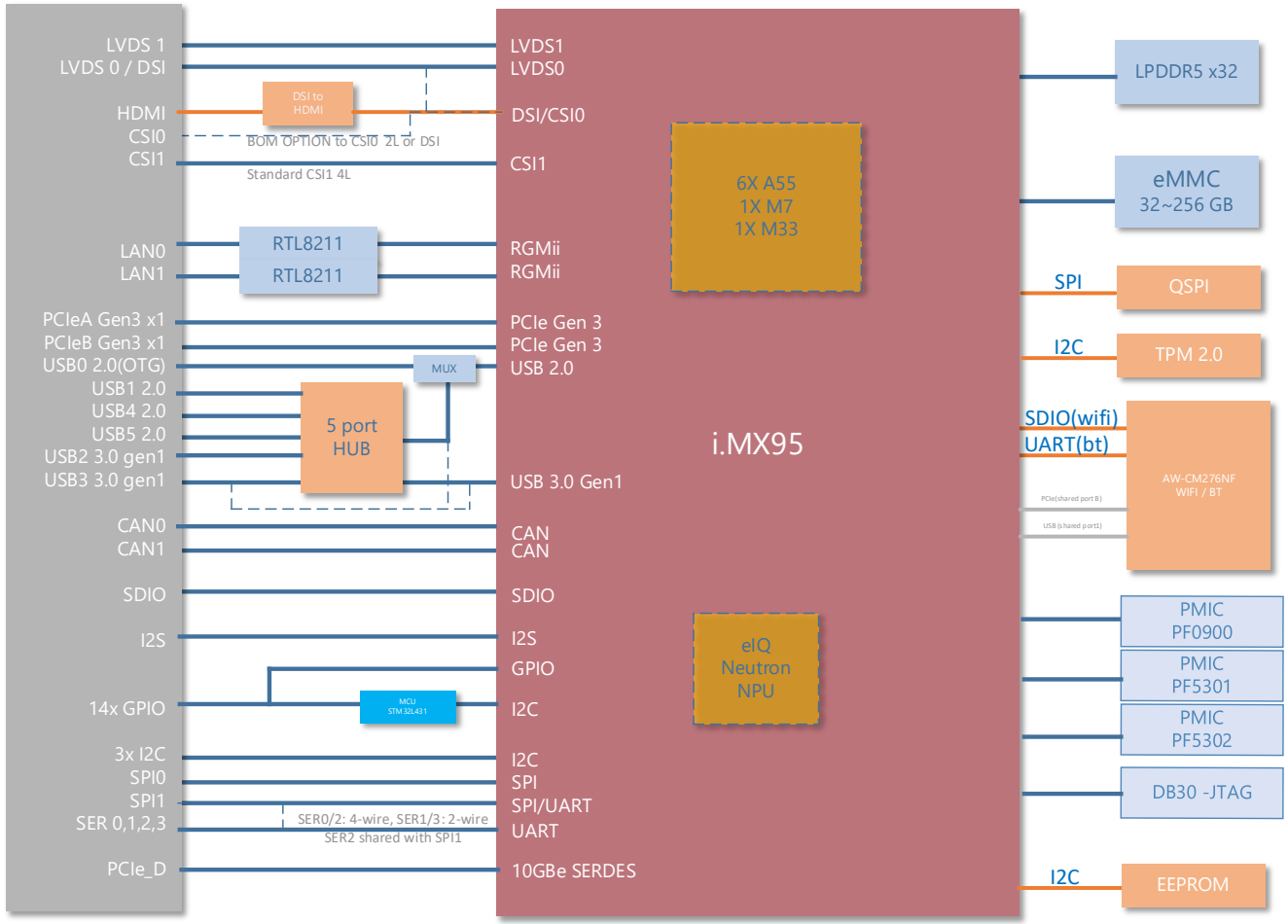


Figure 1 – Module function diagram

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4. Pinout and Signal Descriptions

4.1 Pin Summary

The below tables are a list of all signal pins on the MXM 3 connector in the standard specification of SMARC 2.1.

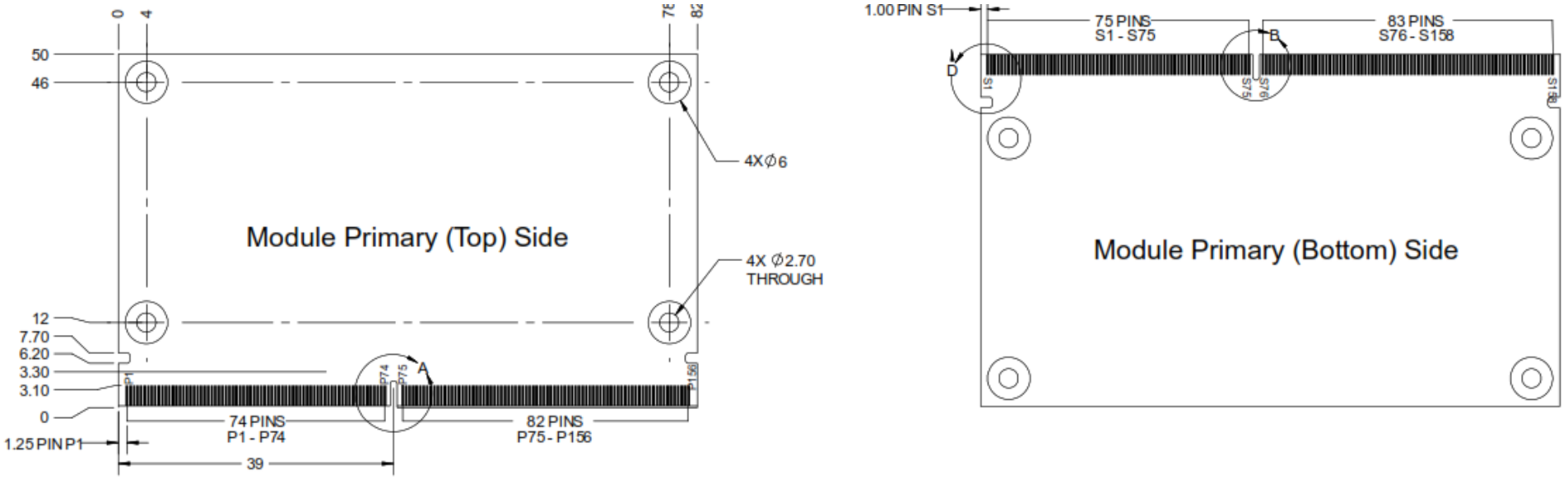


Figure 2 – Module top/bottom side pin numbering

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P-Pin	Primary (Top) Side
P1	SMB_ALERT#
P2	GND
P3	CSI1_CK+
P4	CSI1_CK-
P5	GBE1_SDP
P6	GBE0_SDP
P7	CSI1_RX0+
P8	CSI1_RX0-
P9	GND
P10	CSI1_RX1+
P11	CSI1_RX1-
P12	GND
P13	CSI1_RX2+
P14	CSI1_RX2-
P15	GND
P16	CSI1_RX3+
P17	CSI1_RX3-
P18	GND
P19	GBE0_MDI3-
P20	GBE0_MDI3+
P21	GBE0_LINK_MID#
P22	GBE0_LINK_MAX#
P23	GBE0_MDI2-
P24	GBE0_MDI2+
P25	GBE0_LINK_ACT#
P26	GBE0_MDI1-
P27	GBE0_MDI1+
P28	GBE0_CTREF
P29	GBE0_MDI0-
P30	GBE0_MDI0+
P31	SPI0_CS1#
P32	GND
P33	GND
P34	ESPI_CS0# / SPI1_CS0#
P35	ESPI_CS1# / SPI1_CS1#

S-Pin	Secondary (Bottom) Side
S1	CSI1_TX+ / I2C_CAM1_CK
S2	CSI1_TX- / I2C_CAM1_DAT
S3	GND
S4	RSVD
S5	CSI0_TX+ / I2C_CAM0_CK
S6	CAM_MCK
S7	CSI0_TX- / I2C_CAM0_DAT
S8	CSI0_CK+
S9	CSI0_CK-
S10	GND
S11	CSI0_RX0+
S12	CSI0_RX0-
S13	GND
S14	CSI0_RX1+
S15	CSI0_RX1-
S16	GND
S17	GBE1_MDI0+
S18	GBE1_MDI0-
S19	GBE1_LINK_MID#
S20	GBE1_MDI1+
S21	GBE1_MDI1-
S22	GBE1_LINK1_MAX#
S23	GBE1_MDI2+
S24	GBE1_MDI2-
S25	GND
S26	GBE1_MDI3+
S27	GBE1_MDI3-
S28	GBE1_CTREF
S29	PCIE_D_TX+ /
S30	PCIE_D_TX- /
S31	GBE1_LINK_ACT#
S32	PCIE_D_RX+ /
S33	PCIE_D_RX- /
S34	GND
S35	USB4+
S36	USB4-

P-Pin	Primary (Top) Side
P36	ESPI_CK / SPI1_CK /
P37	ESPI_IO_1 / SPI1_DIN /
P38	ESPI_IO_0 / SPI1_DO /
P39	GND
P40	USB0+
P41	USB0-
P42	USB0_EN_OC#
P43	USB0_VBUS_DET
P44	USB0_OTG_ID
P45	USB1+
P46	GND
P47	ESPI_CS0# / SPI1_CS0#
P48	ESPI_CS1# / SPI1_CS1#
P49	ESPI_CK / SPI1_CK /
P50	ESPI_IO_1 / SPI1_DIN /
P51	ESPI_IO_0 / SPI1_DO /
P52	GND
P53	USB0+
P54	USB0-
P55	USB0_EN_OC#
P56	USB0_VBUS_DET
P57	USB0_OTG_ID
P58	USB1+
P59	GND
P60	ESPI_CS0# / SPI1_CS0#
P61	ESPI_CS1# / SPI1_CS1#
P62	ESPI_CK / SPI1_CK /
P63	ESPI_IO_1 / SPI1_DIN /
P64	ESPI_IO_0 / SPI1_DO /
P65	GND
P66	USB1-
P67	USB1_EN_OC#
P68	GND
P69	USB2+
P70	USB2-
P71	USB2_EN_OC#

S-Pin	Secondary (Bottom) Side
S37	USB3_VBUS_DET
S38	AUDIO_MCK
S39	I2S0_LRCK
S40	I2S0_SDOUT
S41	I2S0_SDIN
S42	I2S0_CK
S43	ESPI_ALERT0#
S44	ESPI_ALERT1#
S45	MDIO_CLK
S46	MDIO_DAT
S47	GND
S48	I2C_GP_CK
S49	I2C_GP_DAT
S50	HDA_SYNC / I2S2_LRCK /
S51	HDA_SDO / I2S2_SDOUT /
S52	HDA_SDI / I2S2_SDIN /
S53	HDA_CK / I2S2_CK /
S54	SATA_ACT#
S55	USB5_EN_OC#
S56	ESPI_IO_2 / QSPI_IO_2
S57	ESPI_IO_3 / QSPI_IO_3
S58	ESPI_RESET#
S59	USB5+
S60	USB5-
S61	GND
S62	USB3_SSTX+
S63	USB3_SSTX-
S64	GND
S65	USB3_SSRX+
S66	USB3_SSRX-
S67	GND
S68	USB3+
S69	USB3-
S70	GND
S71	USB2_SSTX+
S72	USB2_SSTX-

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P-Pin	Primary (Top) Side
P72	RSVD
P73	RSVD
P74	USB3_EN_OC#
	Key
P75	PCIE_A_RST#
P76	USB4_EN_OC#
P77	PCIE_B_CKREQ#
P78	PCIE_A_CKREQ#
P79	GND
P80	PCIE_C_REFCK+
P81	PCIE_C_REFCK-
P82	GND
P83	PCIE_A_REFCK+
P84	PCIE_A_REFCK-
P85	GND
P86	PCIE_A_RX+
P87	PCIE_A_RX-
P88	GND
P89	PCIE_A_TX+
P90	PCIE_A_TX-
P91	GND
P92	HDMI_D2+ /
P93	HDMI_D2- /
P94	GND
P95	HDMI_D1+ /
P96	HDMI_D1- /
P97	GND
P98	HDMI_D0+ /
P99	HDMI_D0- /
P100	GND
P101	HDMI_CK+ /
P102	HDMI_CK- /
P103	GND
P104	HDMI_HPD / DP1_HPD

S-Pin	Secondary (Bottom) Side
S73	GND
S74	USB2_SSRX+
S75	USB2_SSRX-
	Key
S76	PCIE_B_RST#
S77	PCIE_C_RST#
S78	PCIE_C_RX+ /
S79	PCIE_C_RX- /
S80	GND
S81	PCIE_C_TX+ /
S82	PCIE_C_TX- /
S83	GND
S84	PCIE_B_REFCK+
S85	PCIE_B_REFCK-
S86	GND
S87	PCIE_B_RX+
S88	PCIE_B_RX-
S89	GND
S90	PCIE_B_TX+
S91	PCIE_B_TX-
S92	GND
S93	DP0_LANE0+
S94	DP0_LANE0-
S95	DP0_AUX_SEL
S96	DP0_LANE1+
S97	DP0_LANE1-
S98	DP0_HPD
S99	DP0_LANE2+
S100	DP0_LANE2-
S101	GND
S102	DP0_LANE3+
S103	DP0_LANE3-
S104	USB3_OTG_ID
S105	DP0_AUX+

P-Pin	Primary (Top) Side
P105	HDMI_CTRL_CK /
P106	HDMI_CTRL_DAT /
P107	DP1_AUX_SEL
P108	GPIO0 / CAM0_PWR#
P109	GPIO1 / CAM1_PWR#
P110	GPIO2 / CAM0_RST#
P111	GPIO3 / CAM1_RST#
P112	GPIO4 / HDA_RST#
P113	GPIO5 / PWM_OUT
P114	GPIO6 / TACHIN
P115	GPIO7
P116	GPIO8
P117	GPIO9
P118	GPIO10
P119	GPIO11
P120	GND
P121	I2C_PM_CK
P122	I2C_PM_DAT
P123	BOOT_SEL0#
P124	BOOT_SEL1#
P125	BOOT_SEL2#
P126	RESET_OUT#
P127	RESET_IN#
P128	POWER_BTN#
P129	SER0_TX
P130	SER0_RX
P131	SER0_RTS#
P132	SER0_CTS#
P133	GND
P134	SER1_TX
P135	SER1_RX
P136	SER2_TX
P137	SER2_RX
P138	SER2_RTS#
P139	SER2_CTS#
P140	SER3_TX

S-Pin	Secondary (Bottom) Side
S106	DP0_AUX-
S107	LCD1_BKLT_EN
S108	LVDS1_CK+ / eDP1_AUX+ /
S109	LVDS1_CK- / eDP1_AUX- /
S110	GND
S111	LVDS1_0+ / eDP1_TX0+ /
S112	LVDS1_0- / eDP1_TX0- /
S113	eDP1_HPD / DSI1_TE
S114	LVDS1_1+ / eDP1_TX1+ /
S115	LVDS1_1- / eDP1_TX1- /
S116	LCD1_VDD_EN
S117	LVDS1_2+ / eDP1_TX2+ /
S118	LVDS1_2- / eDP1_TX2- /
S119	GND
S120	LVDS1_3+ / eDP1_TX3+ /
S121	LVDS1_3- / eDP1_TX3- /
S122	LCD1_BKLT_PWM
S123	GPIO13
S124	GND
S125	LVDS0_0+ / eDP0_TX0+ /
S126	LVDS0_0- / eDP0_TX0- /
S127	LCD0_BKLT_EN
S128	LVDS0_1+ / eDP0_TX1+ /
S129	LVDS0_1- / eDP0_TX1- /
S130	GND
S131	LVDS0_2+ / eDP0_TX2+ /
S132	LVDS0_2- / eDP0_TX2- /
S133	LCD0_VDD_EN
S134	LVDS0_CK+ / eDP0_AUX+ /
S135	LVDS0_CK- / eDP0_AUX- /
S136	GND
S137	LVDS0_3+ / eDP0_TX3+ /
S138	LVDS0_3- / eDP0_TX3- /
S139	I2C_LCD_CK
S140	I2C_LCD_DAT
S141	LCD0_BKLT_PWM

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P-Pin	Primary (Top) Side
P141	SER3_RX
P142	GND
P143	CAN0_TX
P144	CAN0_RX
P145	CAN1_TX
P146	CAN1_RX
P147	VDD_IN
P148	VDD_IN
P149	VDD_IN

S-Pin	Secondary (Bottom) Side
S142	GPIO12
S143	GND
S144	eDP0_HPD / DSI0_TE
S145	WDT_TIME_OUT#
S146	PCIE_WAKE#
S147	VDD_RTC
S148	LID#
S149	SLEEP#
S150	VIN_PWR_BAD#

P-Pin	Primary (Top) Side
P150	VDD_IN
P151	VDD_IN
P152	VDD_IN
P153	VDD_IN
P154	VDD_IN
P155	VDD_IN
P156	VDD_IN

S-Pin	Secondary (Bottom) Side
S151	CHARGING#
S152	CHARGER_PRSNT#
S153	CARRIER_STBY#
S154	CARRIER_PWR_ON
S155	FORCE_RECOV#
S156	BATLOW#
S157	TEST#
S158	GND

Note: Above is the **complete** SMARC function set, not all signals are available.

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4.2 Signal Terminology Descriptions

Signals described in the specification but not supported on the LEC-IMX95 are marked with ~~STRIKETHROUGH~~.

Term	Description
I	Input to the module
O	Output from the module
I/O	Bi-directional input/output
OD	Open drain
PU	PU (pull-up) resistor
PD	PD (pull-down) resistor
CMOS	Logic input or output
GBE MDI	Differential analogue signalling for gigabit media dependent interface
DP	Low voltage differential signal for DisplayPort interface
D-PHY	Low voltage differential signal for MIPI CSI-2 cameras and DSI displays
M-PHY	Low voltage differential signal for MIPI CSI-3 cameras
LVDS	Low voltage differential signal for LCD displays
PCIE	Low voltage differential signal for PCIe
SATA	Low voltage differential signal for SATA
TMDS HDMI	Transition minimized differential signal for HDMI displays
USB	DC coupled differential signalling for traditional (non-Superspeed) USB signals
USB SS	Differential signal for SuperSpeed USB signals
USB VBUS 5V	5V tolerant input for USB VBUS detection
VDD_IN	Main power source from Carrier to Module
3.3V	3.3V power domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
1.8V	1.8V power domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
3.3Vsb	3.3V standby power domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)
1.8Vsb	1.8V standby power domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)
Sleep	Module is in its lowest power state
Runtime	Module is full on. CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e., both signals are high)
Standby	Module is in standby state or higher

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4.3 Signal Description by Function

4.3.1 The Primary Display Interface

LVDS and DSI are both supported on this module; eDP is **not** supported. LVDS includes both Channel 0 and Channel 1. DSI0 supports 4 lanes and is muxed with LVDS0. The tables below show which display ports are supported on this particular module.

Pin #	LVDS Name	MIPI DSI Name	eDP Name
S125 S126 S128 S129 S131 S132 S137 S138	LVDS0_0+ LVDS0_0- LVDS0_1+ LVDS0_1 - LVDS0_2+ LVDS0_2- LVDS0_3+ LVDS0_3-	DSI0_D0+ DSI0_D0- DSI0_D1+ DSI0_D1- DSI0_D2+ DSI0_D2- DSI0_D3+ DSI0_D3-	~~eDP0_TX0+~~ ~~eDP0_TX0-~~ ~~eDP0_TX1+~~ ~~eDP0_TX1-~~ ~~eDP0_TX2+~~ ~~eDP0_TX2-~~ ~~eDP0_TX3+~~ ~~eDP0_TX3-~~
S134 S135	LVDS0_CK+ LVDS0_CK-	DSI0_CLK+ DSI0_CLK-	~~eDP0_AUX+~~ ~~eDP0_AUX-~~
S133	LCD0_VDD_EN	LCD0_VDD_EN	~~LCD0_VDD_EN~~
S127	LCD0_BKLT_EN	LCD0_BKLT_EN	~~LCD0_BKLT_EN~~
S141	LCD0_BKLT_PWM	LCD0_BKLT_PWM	~~LCD0_BKLT_PWM~~
S144		DSI0_TE	~~eDP0_HPD~~

Pin #	LVDS Name	MIPI DSI Name	eDP Name
S111 S112 S114 S115 S117 S118 S120 S121	LVDS1_0+ LVDS1_0- LVDS1_1+ LVDS1_1 - LVDS1_2+ LVDS1_2- LVDS1_3+ LVDS1_3-	~~DSI1_D0+~~ ~~DSI1_D0-~~ ~~DSI1_D1+~~ ~~DSI1_D1-~~ ~~DSI1_D2+~~ ~~DSI1_D2-~~ ~~DSI1_D3+~~ ~~DSI1_D3-~~	~~eDP1_TX0+~~ ~~eDP1_TX0-~~ ~~eDP1_TX1+~~ ~~eDP1_TX1-~~ ~~eDP1_TX2+~~ ~~eDP1_TX2-~~ ~~eDP1_TX3+~~ ~~eDP1_TX3-~~
S108 S109	LVDS1_CK+ LVDS1_CK-	~~DSI1_CLK+~~ ~~DSI1_CLK-~~	~~eDP1_AUX+~~ ~~eDP1_AUX-~~
S116	LCD1_VDD_EN	~~LCD1_VDD_EN~~	~~LCD1_VDD_EN~~
S107	LCD1_BKLT_EN	~~LCD1_BKLT_EN~~	~~LCD1_BKLT_EN~~
S122	LCD1_BKLT_PWM	~~LCD1_BKLT_PWM~~	~~LCD1_BKLT_PWM~~
S113		~~DSI1_TE~~	~~eDP1_HPD~~

S139	I2C_LCD_CK	~~I2C_LCD_CK~~	~~I2C_LCD_CK~~
S140	I2C_LCD_DAT	~~I2C_LCD_DAT~~	~~I2C_LCD_DAT~~

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4.3.1.1 LVDS0/LVDS1 Mode

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
LVDS0_0+ LVDS0_0- LVDS0_1+ LVDS0_1 - LVDS0_2+ LVDS0_2- LVDS0_3+ LVDS0_3-	S125 S126 S128 S129 S131 S132 S137 S138	Primary LVDS Channel Differential Pair Data Lines	O LVDS		Runtime		100 Ohm differential termination across the differential pairs at the endpoint of the signal path, usually on the display assembly.
LVDS0_CK+ LVDS0_CK-	S134 S135	Primary LVDS channel differential pair clock lines	O LVDS LCD		Runtime		100 Ohm differential termination across the differential pair at the endpoint of the signal path, usually on the display assembly.
LCD0_VDD_EN	S133	Primary LVDS channel power enable;, active high	O CMOS	1.8V	Runtime		Active high
LCD0_BKLT_EN	S127	Primary LVDS channel backlight enable;, active high	O CMOS	1.8V	Runtime		Active high
LCD0_BKLT_PWM	S141	Primary LVDS channel brightness control through pulse width modulation (PWM)	O CMOS	1.8V	Runtime		Through Pulse Width Modulation (PWM)

LVDS1_0+ LVDS1_0- LVDS1_1+ LVDS1_1 - LVDS1_2+ LVDS1_2- LVDS1_3+ LVDS1_3-	S111 S112 S114 S115 S117 S118 S120 S121	Secondary LVDS channel differential pair data lines	O LVDS LCD		Runtime		100 Ohm differential termination across the differential pairs at the endpoint of the signal path, usually on the display assembly.
LVDS1_CK+ LVDS1_CK-	S108 S109	Secondary LVDS channel differential pair clock lines.	O LVDS LCD		Runtime		100 Ohm differential termination across the differential pair at the endpoint of the signal path, usually on the display assembly.
LCD1_VDD_EN	S116	Secondary panel power enable, active high	O CMOS	1.8V	Runtime		Active high

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LCD1_BKLT_EN	S107	Secondary panel backlight enable, active high	O CMOS	1.8V	Runtime		Only in use, when two separate LVDS ports are supported, please check Module user manual
LCD1_BKLT_PWM	S122	Secondary panel brightness control through pulse width modulation (PWM)	O CMOS	1.8V	Runtime		Through pulse width modulation (PWM)

I2C_LCD_DAT	S140	DDC data line used for flat panel detection and control	I/O OD CMOS	1.8V	Runtime	PU 2k2	Possible conflict if 2 panels are used
I2C_LCD_CK	S139	DDC clock line used for flat panel detection and control	O OD CMOS	1.8V	Runtime	PU 2k2	Possible conflict if 2 panels are used

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4.3.1.2 DSI0 Mode (Muxed on LVDS0)

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
DSI0_D0+ DSI0_D0- DSI0_D1+ DSI0_D1- DSI0_D2+ DSI0_D2- DSI0_D3+ DSI0_D3-	S125 S126 S128 S129 S131 S132 S137 S138	Primary DSI panel differential pair data lines	O D-PHY		Runtime		No blocking capacitors or termination required. Layout for 90 Ohms differential impedance.
DSI0_CLK+ DSI0_CLK-	S134 S135	Primary DSI panel differential pair clock lines.	O D-PHY		Runtime		
LCD0_VDD_EN	S133	Primary panel power enable	O CMOS	1.8V	Runtime		Active high
LCD0_BKLT_EN	S127	Primary panel backlight enable	O CMOS	1.8V	Runtime		Active high
LCD0_BKLT_PWM	S141	Primary panel brightness control through pulse width modulation (PWM)	O CMOS	1.8V	Runtime		Through pulse width modulation (PWM)
DSI0_TE	S144	Primary DSI panel tearing effect signal	I CMOS	1.8V	Runtime	1M PD	
I2C_LCD_DAT	S140	DDC data line used for flat panel detection and control	I/O OD CMOS	1.8V	Runtime	PU 2k2	
I2C_LCD_CK	S139	DDC clock line used for flat panel detection and control	O OD CMOS	1.8V	Runtime	PU 2k2	

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4.3.2 Second Display Interface

4.3.2.1 HDMI Mode (HDMI Option Disables DSI0)

HDMI displays use 5V I^2C signaling. The module's HDMI_CTRL_DAT and HDMI_CTRL_CK signals need to be level-translated on the carrier from the module's 1.8V level. A similar consideration applies to the HDMI_HPD signal.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
HDMI_D2+ HDMI_D2- HDMI_D1+ HDMI_D1- HDMI_D0+ HDMI_D0-	P92 P93 P95 P96 P98 P99	HDMI port, differential pair data lines	O TMDS HDMI		Runtime		AC coupled off module
HDMI_CK+ HDMI_CK-	P101 P102	HDMI port, differential pair clock lines	O TMDS HDMI		Runtime		AC coupled off module
HDMI_CTRL_CK	P105	I2C_CLK line dedicated to HDMI	O OD COMS	1.8V	Runtime	PU 100K	A level shifter FET and a 5V PU resistor ***shall*** be placed between the module and the HDMI connector. A stronger pull-up is demanded on the carrier board. The pull-ups may be part of an integrated HDMI ESD protection and control-line level shift device, such as the Texas Instruments TPD12S016. If discrete carrier pull-ups are used, the value depends on the individual carrier board implementation.
HDMI_CTRL_DAT	P106	I2C_DAT line dedicated to HDMI	I/O OD COMS	1.8V	Runtime	PU 100K	A level shifter FET and a 5V PU resistor ***shall*** be placed between the module and the HDMI connector. A stronger pull-up is demanded on the carrier board. The pull-ups may be part of an integrated HDMI ESD protection and control-line level shift device, such as the Texas Instruments TPD12S016. If discrete carrier pull-ups are used, the value depends on the individual carrier board implementation.
HDMI_HPD	P104	HDMI Hot plug active high detection signal serves as an interrupt request	I CMOS	1.8V	runtime	PD 1M	Important: A module must tolerate high voltage levels while in stand-by mode

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4.3.3 MIPI Camera Support

4.3.3.1 MIPI CSI0 (2 Lanes), BOM Option, Pin-Shared with DSI

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CSI0_RX0+ CSI0_RX0- CSI0_RX1+ CSI0_RX1-	S11 S12 S14 S15	CSI0 differential input (point to point)	I D-PHY / I M-PHY		Runtime		
CSI0_CK+ CSI0_CK-	S8 S9	CSI0 differential clock input (point to point)	I D-PHY		Runtime		
I2C_CAM0_DAT /CSI0_TX-	S7	I2C data for serial camera data support link or differential data lane	I/O OD CMOS / O M-PHY	1.8V	Runtime	PU 4.7K	MIPI-CSI 2.0 uses I2C_CAM0_DAT which requires PU MIPI-CSI 3.0 uses CSI0_TX-, no PU required
I2C_CAM0_CK / CSI0_TX+	S5	I2C clock for serial camera data support link or differential data lane	O OD CMOS / O M-PHY	1.8V	Runtime	PU 4.7K	MIPI-CSI 2.0 uses I2C_CAM0_CK which requires PU MIPI-CSI 3.0 uses CSI0_TX+, no PU required
CAM0_PWR# / GPIO0	P108	Camera 0 Power Enable, active low output.	O CMOS	1.8V	Runtime		Shared with GPIO0
CAM0_RST# / GPIO2	P110	Camera 0 reset, active low output	O CMOS	1.8V	Runtime		Shared with GPIO2
CAM_MCK	S6	Master clock output	O CMOS	1.8V	Runtime		

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4.3.3.2 CSI1 (4 Lanes)

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CSI1_RX0+ CSI1_RX0- CSI1_RX1+ CSI1_RX1- CSI1_RX2+ CSI1_RX2- CSI1_RX3+ CSI1_RX3-	P7 P8 P10 P11 P13 P14 P16 P17	CSI1 differential input	I LVDS D-PHY / I LVDS M-PHY		Runtime		
CSI1_CK+ CSI1_CK-	P3 P4	CSI1 differential clock input (point to point)	I LVDS D-PHY		Runtime		
I2C_CAM1_DAT / CSI1_TX-	S2	I2C data for serial camera data support link or differential data lane	I/O OD CMOS / O LVDS M-PHY	1.8V	Runtime	PU 2.2K	MIPI-CSI 2.0 uses I2C_CAM0_DAT which requires PU MIPI-CSI 3.0 uses CSI0_TX-, no PU required
I2C_CAM1_CK / CSI1_TX+	S1	I2C clock for serial camera data support link or differential data lane	O OD CMOS / O LVDS M-PHY	1.8V	Runtime	PU 2.2K	MIPI-CSI 2.0 uses I2C_CAM0_CK which requires PU MIPI-CSI 3.0 uses CSI0_TX+, no PU required
CAM1_PWR# / GPIO1	P109	Camera 1 Power Enable, active low output.	O CMOS	1.8V	Runtime		Shared with GPIO1
CAM1_RST# / GPIO3	P111	Camera 1 reset, active low output	O CMOS	1.8V	Runtime		Shared with GPIO 3

CAM_MCK	S6	Master clock output	O CMOS	1.8V	Runtime		

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4.3.4 Audio Interfaces

4.3.4.1 I2S0

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
I2S0_LRCK	S39	I2S0 Left & Right synchronization clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
I2S0_SDOUT	S40	I2S0 Digital audio Output	O CMOS	1.8V	Runtime		
I2S0_SDIN	S41	I2S0 Digital audio Input	I CMOS	1.8V	Runtime		
I2S0_CK	S42	I2S0 Digital audio clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
AUDIO_MCK	S38	Master clock output to I2S codec(s)	O CMOS	1.8V	Runtime		Shared with I2S2

Note: The support for I2S1 signalling pins has been removed after the SMARC 2.0 specification update.

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4.3.5 USB Ports

The i.MX95 SoC provides a single USB 3.2 Gen 1 port and a single USB 2.0 port. All ports routed to the carrier are derived via an on-module USB hub. USB0 is used as the serial download port.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
USB0+ USB0-	P60 P61	USB differential data pairs for port 0	I/O USB	USB	Standby		From HUB
USB0_EN_OC#	P62	USB over-current sense for port 0	I/O OD CMOS	3.3V note 1	Standby	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB0_VBUS_DET	P63	USB port 0 host power detection, when this port is used as a device.	I USB VBUS 5V	USB VBUS 5V	Standby		When this Port is used as a device it can be connected to a USB client port VBUS pin
USB0_OTG_ID	P64	Input pin to announce OTG device insertion on USB 2.0 port			Standby		Resistor value to ground according to USB specification
USB1+ USB1-	P65 P66	USB differential data pairs for port 1	I/O USB	USB	Standby		From HUB
USB1_EN_OC#	P67	USB over-current sense for port 1	I/O OD CMOS	3.3V note 1	Standby	PU 10k	Pulled low by Module OD driver to disable USB1 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB2+ USB2-	P69 P70	USB differential data pairs for port 2	I/O USB	USB	Standby		From SOC
USB2_SSRX+ USB2_SSRX-	S74 S75	Receive signal differential pairs for SuperSpeed on port 2	I USB SS	USB SS	Standby		DC blocking capacitors 100nF ***shall*** be placed on the Carrier
USB2_SSTX+ USB2_SSTX-	S71 S72	Transmit signal differential pairs for SuperSpeed on port 2	O USB SS	USB SS	Standby		DC blocking capacitors 100nF ***shall*** be placed on the Carrier
USB2_EN_OC#	P71	USB over-current sense for port 2	I/O OD CMOS	3.3V note 1	Standby	PU 10k	Pulled low by Module OD driver to disable USB2 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB3+ USB3-	S68 S69	USB differential data pairs for port 3	I/O USB	USB	Standby		

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USB3_SSRX+ USB3_SSRX-	S65 S66	Receive signal differential pairs for SuperSpeed on port 3	I USB SS	USB SS	Standby		DC blocking capacitors 100nF shall be placed on the Carrier
USB3_SSTX+ USB3_SSTX-	S62 S63	Transmit signal differential pairs for SuperSpeed on port 3	O USB SS	USB SS	Standby		DC blocking capacitors 100nF shall be placed on the Carrier
USB3_EN_OC#	P74	USB over-current sense for port 3	I/O OD CMOS	3.3V note 1	Standby	PU 10k	Pulled low by Module OD driver to disable USB3 power. Pulled low by Carrier OD driver to indicate over-current situation.
~~USB3_VBUS_DET~~	~~S37~~	~~USB port 3 host power detection, when this port is used as a device.~~	~~I USB VBUS 5V~~	~~USB VBUS 5V~~	~~Standby~~	-	-
~~USB3_OTG_ID~~	~~S104~~	~~Input pin to announce OTG device insertion on USB 3.0 port~~	~~I CMOS~~	~~3.3V~~	~~Standby~~	-	-
USB4+ USB4-	S35 S36	USB differential data pairs for port 4	I/O USB	USB	Standby		From HUB
USB4_EN_OC#	P76	USB over-current sense for port 4	I/O OD CMOS	3.3V note 1	Standby	PU 10k	Pulled low by Module OD driver to disable USB4 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB5+ USB5-	S59 S60	USB differential data pairs for port 5	I/O USB	USB	Standby		
USB5_EN_OC#	S55	USB over-current sense for port 5	I/O OD CMOS	3.3V note 1	Standby	PU 10k	Pulled low by Module OD driver to disable USB5 power. Pulled low by Carrier OD driver to indicate over-current situation.

Note: 3.3V or switched 3.3V: If a USB channel is not used, the USB[0:5]_EN_OC# pull-up rails may be held at GND to prevent leakage currents.

Note: USB downstream ports are derived from a USB 3.1 Gen 2 hub.

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4.3.6 PCIe and SerDes

PCIe Port D is used to bring out the 10GbE signal over SerDes.

4.3.6.1 PCIe Ports

The i.MX95 supports two single-lane PCIe Gen 3.0 interfaces.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
PCIE_A_TX+ PCIE_A_TX-	P89 P90	Differential PCIe link A transmit data pair	O LVDS PCIE		Runtime		Series AC coupled on module
PCIE_A_RX+ PCIE_A_RX-	P86 P87	Differential PCIe link A receive data pair	I LVDS PCIE		Runtime		Series AC coupled off module
PCIE_A_REFCK+ PCIE_A_REFCK-	P83 P84	Differential PCIe Link A reference clock output	O LVDS PCIE		Runtime		
PCIE_A_RST#	P75	PCIe Port A reset output	O CMOS	3.3V	Runtime		
PCIE_A_CKREQ#	P78	PCIe Port A clock request	I OD CMOS	3.3V	Runtime		Can be used for power saving mode on PCIe - Pulled up or terminated on Module
PCIE_B_TX+ PCIE_B_TX-	S90 S91	Differential PCIe link B transmit data pair	O LVDS PCIE		Runtime		Series AC coupled on module
PCIE_B_RX+ PCIE_B_RX-	S87 S88	Differential PCIe link B receive data pair	I LVDS PCIE		Runtime		Series AC coupled off module
PCIE_B_REFCK+ PCIE_B_REFCK-	S84 S85	Differential PCIe Link B reference clock output	O LVDS PCIE		Runtime		
PCIE_B_RST#	S76	PCIe Port B reset output	O CMOS	3.3V	Runtime		
PCIE_B_CKREQ#	P77	PCIe Port B clock request	I OD CMOS	3.3V	Runtime		Can be used for power saving mode on PCIe - Pulled up or terminated on the module

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4.3.7 Dual LAN Ports

4.3.7.1 GBE0

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	P30 P29 P27 P26 P24 P23 P20 P19	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations	I/O GBE MDI		Standby		Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: 1000 100 10 MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-
GBE0_LINK100#	P21	Link Speed Indication LED for GBE 0 100Mbps	O OD CMOS	3.3V	Standby		Shall be able to sink 24 mA or more of carrier LED current
GBE0_LINK1000#	P22	Link Speed Indication LED for GBE 0 1000Mbps	O OD CMOS	3.3V	Standby		Shall be able to sink 24 mA or more of carrier LED current
GBE0_LINK_ACT#	P25	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity	O OD CMOS	3.3V	Standby		Shall be able to sink 24 mA or more of carrier LED current
~~GBE0_CTREF~~	~~P28~~	~~Center-Tap reference voltage for Carrier board Ethernet magnetic (if required by the Module GBE PHY)~~	~~Analog~~	~~0 to 3.3V max~~	~~Standby~~	-	-
~~GBE0_SDP~~	~~P6~~	~~IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol)~~	~~IO CMOS~~	~~3.3V~~	~~Standby~~	-	-

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4.3.7.2 GBE1

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GBE1_MDI0+ GBE1_MDI0- GBE1_MDI1+ GBE1_MDI1- GBE1_MDI2+ GBE1_MDI2- GBE1_MDI3+ GBE1_MDI3-	S17 S18 S20 S21 S23 S24 S26 S27	Differential Pair Signals for External Transformer Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations	I/IO GBE MDI		Standby		Gigabit Ethernet Controller 1: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: 1000 100 10 MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-
GBE1_LINK100#	S19	Link Speed Indication LED for GBE 1 100Mbps	O OD CMOS	3.3V	Standby		Shall be able to sink 24 mA or more Carrier LED current
GBE1_LINK1000#	S22	Link Speed Indication LED for GBE 1 1000Mbps	O OD CMOS	3.3V	Standby		Shall be able to sink 24 mA or more Carrier LED current
GBE1_LINK_ACT#	S31	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity	O OD CMOS	3.3V	Standby		Shall be able to sink 24 mA or more Carrier LED current
~~GBE1_CTREF~~	~~S28~~	~~Center-Tap reference voltage for Carrier board Ethernet magnetic `~~ ~~(if required by the Module GBE PHY)`~~	~~Analog~~	~~0 to 3.3V max~~	~~Standby~~	-	-
~~GBE1_SDP~~	~~P5~~	~~IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol)~~	~~IO CMOS~~	~~3.3V~~	~~Standby~~	-	-

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4.3.8 SDIO Card (4-Bit)

The carrier SDIO card ***may*** be selected as the boot device.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SDIO_D0 SDIO_D1 SDIO_D2 SDIO_D3	P39 P40 P41 P42	SDIO Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V	Runtime		SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly
SDIO_WP	P33	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I OD CMOS	3.3V	Runtime	PU 10k	Pulled up on module
SDIO_CMD	P34	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O CMOS	1.8V or 3.3V	Runtime		SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly
SDIO_CD#	P35	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	I OD CMOS	3.3V	Runtime	PU 10k	Pulled up on module
SDIO_CK	P36	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.	O CMOS	1.8V or 3.3V	Runtime		
SDIO_PWR_EN	P37	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	O CMOS	3.3V	Runtime		should be driven low in STB Mode by the module

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4.3.9 SPI Interfaces

4.3.9.1 SPI0

A carrier SPI device ***may*** be selected as the boot device.

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SPI0_CS0#	P43	SPI0 Master Chip Select 0	O CMOS	1.8V	Standby		This signal can be used to select carrier SPI as boot device
SPI0_CS1#	P31	SPI0 Master Chip Select 1	O CMOS	1.8V	Standby		
SPI0_CK	P44	SPI0 Clock	O CMOS	1.8V	Standby		
SPI0_DIN	P45	SPI0 Master input / Slave output	I CMOS	1.8V	Standby		also referred to as MISO
SPI0_DO	P46	SPI0 Master output / Slave input	O CMOS	1.8V	Standby		also referred to as MOSI

4.3.9.2 SPI or ESPI

ESPI Mode (eCSPI on ARM)

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
ESPI_CS0#	P54	ESPI1 Master Chip Select 0	O CMOS	1.8V	Standby		
ESPI_CS1#	P55	ESPI1 Master Chip Select 1	O CMOS	1.8V	Standby		
ESPI_CK	P56	ESPI Master Clock Output	O CMOS	1.8V	Standby		Pin provides reference timing for all serial input / output operations.
~~ESPI_RESET#~~	~~S58~~	~~ESPI Reset~~	~~O CMOS~~	~~1.8V~~	~~Standby~~	-	~~Reset the eSPI interface for both master and slaves. eSPI Reset# is typically driven from eSPI master to eSPI slaves~~
~~ESPI_ALERT0#~~ ~~ESPI_ALERT1#~~	~~S43~~ ~~S44~~	~~ESPI ALERT~~	~~I OD CMOS~~	~~1.8V~~	~~Standby~~	~~4.7k PU~~	~~This pin is used by eSPI slave to request service from eSPI.master.Alert# is an open-drain output from the slave. This pin is optional for Single Master-Single Slave configuration where I/O[1] can be used to signal the Alert event.~~

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ESPI_IO_0 ESPI_IO_1	P58 P57	ESPI Master Data Input / Output	I/O CMOS	1.8V	Standby		In Single I/O mode, ESPI_IO_0 is eSPI master output / eSPI slave input (MOSI) whereas ESPI_IO_1 is SPI master input / eSPI slave output (MISO).
ESPI_IO_1 / SPI1_DIN	S56	In	I/O CMOS	1.8V			
ESPI_IO_0 / SPI1_DO	S57	Out	I/O CMOS	1.8V			

4.3.10 GPIO

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GPIO0 / CAM0_PWR#	P108	General purpose I/O pin 0.	I/O CMOS	1.8V	Runtime	PU 470K [1]	alternate use is Camera 0 Power Enable, active low output
GPIO1 / CAM1_PWR#	P109	General purpose I/O pin 1.	I/O CMOS	1.8V	Runtime	PU 470K [1]	alternate use is Camera 1 Power Enable, active low output
GPIO2 / CAM0_RST#	P110	General purpose I/O pin 2.	I/O CMOS	1.8V	Runtime	PU 470K [1]	alternate use is Camera 0 Reset, active low output
GPIO3 / CAM1_RST#	P111	General purpose I/O pin 3.	I/O CMOS	1.8V	Runtime	PU 470K [1]	alternate use is Camera 1 Reset, active low output
GPIO4 / HDA_RST#	P112	General purpose I/O pin 4.	I/O CMOS	1.8V	Runtime	PU 470K [1]	alternative use is HD Audio Reset, active low output
GPIO5 / PWM_OUT	P113	General purpose I/O pin 5.	I/O CMOS	1.8V	Runtime	PU 470K [1]	alternate use is PWM output
GPIO6 / TACHIN	P114	General purpose I/O pin 6.	I/O CMOS	1.8V	Runtime	PU 470K [1]	FAN Tachometer input (used with GPIO5 PWM_OUT)
GPIO7	P115	General purpose I/O pin 7.	I/O CMOS	1.8V	Runtime	PU 470K [1]	
GPIO8	P116	General purpose I/O pin 8.	I/O CMOS	1.8V	Runtime	PU 470K [1]	
GPIO9	P117	General purpose I/O pin 9.	I/O CMOS	1.8V	Runtime	PU 470K [1]	
GPIO10	P118	General purpose I/O pin 10.	I/O CMOS	1.8V	Runtime	PU 470K [1]	
GPIO11	P119	General purpose I/O pin 11.	I/O CMOS	1.8V	Runtime	PU 470K [1]	

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GPIO12	S142	General purpose I/O pin 12	I/O CMOS	1.8V	Runtime	PU 470K [1]	advised as INT signal to any expander on carrier.
GPIO13	S123	General purpose I/O pin 13	I/O CMOS	1.8V	Runtime	PU 470K [1]	

Note[1]: also allows for SoC-integrated pull-ups.

These can be ≤ 10kΩ. A maximum 2.2kΩ pull-down should be implemented on the carrier if a low level needs to be ensured.

4.3.11 CAN Bus

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CAN0_TX	P143	CAN port 0 Transmit output	O CMOS	1.8V	Runtime		
CAN0_RX	P144	CAN port 0 Receive input	I CMOS	1.8V	Runtime		
CAN1_TX	P145	CAN port 1 Transmit output	O CMOS	1.8V	Runtime		
CAN1_RX	P146	CAN port1 Receive input	I CMOS	1.8V	Runtime		

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4.3.12 Miscellaneous

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
TEST#	S157	Held Low by Carrier to Invoke Module Vendor Specific Test Functions	I OD CMOS	1.8 to 5 V	Runtime	PU	Module must implement PU but actual value is depended on particular Module design. Carrier Board should leave this pin floating for normal operation. Driven by OD on Carrier
WDT_TIME_OUT#	S145	Watch-Dog-Timer Output, low active.	O CMOS	1.8V	Runtime		
PWM_OUT / GPIO5	P113	Pulse Width Modulation (PWM) output	I/O CMOS	1.8V	Runtime	PU 470K	GPIO5 is the default pin configuration

4.3.13 Power and System Management

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
BATLOW#	S156	Battery low indication to Module. Carrier to float the line in inactive state.	I OD CMOS	1.8V to 5V	Standby/ Sleep	PU 10K	Driven by OD on Carrier. Pulled up on module.
CARRIER_PWR_ON	S154	Carrier Board circuits (apart from power management and power path circuits) ***should not*** be powered up until the Module asserts the CARRIER_PWR_ON signal.	O CMOS	1.8V	Standby		On x86 designs this pin should utilize a standby related power signal i.e. RSM_RST# or SLP_A# signal.
CARRIER_STBY#	S153	The Module ***shall*** drive this signal low when the system is in a standby power state.	O CMOS	1.8V	Standby		On x86 designs this pin should utilize the SUS_S3# signal.
CHARGER_PRSNT#	S152	Held low by Carrier if DC input for battery charger is present.	I OD CMOS	1.8V to 5V	Standby/ Sleep	PU 10K	Driven by OD on Carrier. Pulled up on module.
CHARGING#	S151	Held low by Carrier during battery charging. Carrier to float the line when charge is complete.	I OD CMOS	1.8V to 5V	Standby/ Sleep	PU 10K	Driven by OD on Carrier. Pulled up on module.
VIN_PWR_BAD#	S150	Power bad indication from Carrier Board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) ***shall not*** be enabled while this signal is held low by the Carrier.	I OD CMOS	VDD_IN		PU 10K	Driven by OD on Carrier Module must implement PU but actual value is depended on particular module design.
SLEEP#	S149	Sleep indicator from Carrier Board. ***May*** be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active	I OD CMOS	1.8V to 5V	Standby	PU 10K	Driven by OD on Carrier. Pulled up on module.

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		low, level sensitive. ***Should*** be de-bounced on the Module.					
LID#	S148	Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. ***Should*** be de-bounced on the Module.	I OD CMOS	1.8V to 5V	Standby	PU 10K	Driven by OD on Carrier. Pulled up on module.
POWER_BTN#	P128	Power-button input from Carrier Board. Carrier to float the line in in-active state. Active low, level sensitive. ***Should*** be debounced on the Module.	I OD CMOS	1.8V to 5V	Standby	PU 10K	Driven by OD on Carrier. Pulled up on module.
RESET_OUT#	P126	General purpose reset output to Carrier board.	O CMOS	1.8V	Standby		
RESET_IN#	P127	Reset input from Carrier Board. Carrier drives low to force a Module reset, floats the line otherwise. This signal ***Shall*** be level triggered during bootup to allow to stop booting of the module. After bootup it ***May*** act as an edge triggered signal.	I OD CMOS	1.8V to 5V	Standby	PU 10K	Driven by OD on Carrier. Pulled up on module.
I2C_PM_DAT	P122	Power management I2C bus DATA	I/O OD CMOS	1.8V	Standby/ Sleep	PU 2k2	On x86 systems these serve as SMB DATA. Pulled up on module.
I2C_PM_CK	P121	Power management I2C bus CLK	O OD CMOS	1.8V	Standby/ Sleep	PU 2k2	On x86 systems these serve as SMB CLK. Pulled up on module.
~~SMB_ALERT_1V8#~~	~~P1~~	~~SMBus Alert# (interrupt) signal~~	~~I OD CMOS~~	~~1.8V to 5V~~	~~Standby/ Sleep~~	~~PU 2k2~~	~~only used on x86 design~~

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4.3.14 Boot Select

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
BOOT_SEL0# BOOT_SEL1# BOOT_SEL2#	P123 P124 P125	Input straps determine the module boot	I OD CMOS	1.8V	Standby	PU 10K	Driven by OD on the carrier. Pulled up on the module. Booting from eMMC and SD card is supported.
FORCE_RECOV#	S155		I OD CMOS	1.8V	Standby	PU 10K	Driven by OD on the carrier. Pulled up on the module. Low on this pin allows non-protected segments of the module boot device to be rewritten/restored from an external USB host on Module USB0. The Module USB0 operates in client mode when the Force Recovery function is invoked. Pulled high on the module. For SoCs that do not implement a USB-based Force Recovery function, a low on the Module FORCE_RECOV# pin may invoke the SoC's native Force Recovery mode – such as over a serial port. For x86 systems, this signal may be used to load BIOS defaults. Pulled up on the module. Driven by OD part on carrier.

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4.3.15 Power

Name	Pin #	Description	I/O Type	Power Rail / Tolerance	PU / PD	Comments
VDD_IN	P147, P148, P149, P150, P151, P152, P153, P154, P155, P156	Module power input voltage 4.75 min to 5.25V max	P Not defined within Signal Terminology Descriptions. Should we define a specific rail?	4.75V to 5.25V / 5V		
GND	P2, P9, P12, P15, P18, P32, P38, P47, P50, P53, P59, P68, P79, P82, P85, P88, P91, P94, P97, P100, P103, P120, P133, P142, S3, S10, S16, S25, S34, S47, S61, S64, S67, S70, S73, S80, S83, S86, S89, S92, S101, S110, S119, S124, S130, S136, S143, S158	Module signal and power return, and GND reference	P Not defined within Signal Terminology Descriptions. Should we define a specific rail?	Ground		
VDD_RTC	S147	Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based Lithium cell or Super Cap.	P Not defined within Signal Terminology Descriptions. Should we define a specific rail?	[2 to 3.25] / 3.25V		

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4.3.16 Pin to Controller Mapping Table

Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	I/O Mux default
P1	SMB_ALERT_1V8#	In	PU-2.2K	GPIO / 1.8V	i.MX95	GPIO_IO18	Alt0
P2	GND	-	-	-	-	-	-
P3	CSI1_CK+	In	-	MIPI_CSI	i.MX95	MIPI_CSI1_CLK_P	-
P4	CSI1_CK-	In	-	MIPI_CSI	i.MX95	MIPI_CSI1_CLK_N	-
P5	GBE1_SDP	-	-	-	-	-	
P6	GBE0_SDP	-	-	-	-	-	-
P7	CSI1_RX0+	In	-	MIPI_CSI	i.MX95	MIPI_CSI1_D0_P	-
P8	CSI1_RX0-	In	-	MIPI_CSI	i.MX95	MIPI_CSI1_D0_N	-
P9	GND	-	-	-	-	-	-
P10	CSI1_RX1+	In	-	MIPI_CSI	i.MX95	MIPI_CSI1_D1_P	-
P11	CSI1_RX1-	In	-	MIPI_CSI	i.MX95	MIPI_CSI1_D1_N	-
P12	GND	-	-	-	-	-	-
P13	CSI1_RX2+	In	-	MIPI_CSI	i.MX95	MIPI_CSI1_D2_P	-
P14	CSI1_RX2-	In	-	MIPI_CSI	i.MX95	MIPI_CSI1_D2_N	-
P15	GND	-	-	-	-	-	-
P16	CSI1_RX3+	In	-	MIPI_CSI	i.MX95	MIPI_CSI1_D3_P	-
P17	CSI1_RX3-	In	-	MIPI_CSI	i.MX95	MIPI_CSI1_D3_N	-
P18	GND	-	-	-	-	-	-
P19	GBE0_MDI3-	Bi-Dir	-	GBE MDI	RTL8211	MDIN3	-
P20	GBE0_MDI3+	Bi-Dir	-	GBE MDI	RTL8211	MDIP3	-
P21	ENET1_LINK100#	Out/OD	-	GPIO / 3.3V	RTL8211	LED1/CFG_LDO0	-
P22	GBE0_LINK1000#	Out/OD	-	GPIO / 3.3V	RTL8211	LED2/CFG_LDO1	-

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P23	GBE0_MDI2-	Bi-Dir	-	GBE MDI	RTL8211	MDIN2	-
P24	GBE0_MDI2+	Bi-Dir	-	GBE MDI	RTL8211	MDIP2	-
P25	GBE0_LINK_ACT#	Out/OD	-	GPIO / 3.3V	RTL8211	LED0/CFG_EXT	-
P26	GBE0_MDI1-	Bi-Dir	-	GBE MDI	RTL8211	MDIN1	-
P27	GBE0_MDI1+	Bi-Dir	-	GBE MDI	RTL8211	MDIP1	-
P28	GBE0_CTREF	PWR	-	Analog / 3.3V	-	-	-
P29	GBE0_MDI0-	Bi-Dir	-	GBE MDI	RTL8211	MDIN0	-
P30	GBE0_MDI0+	Bi-Dir	-	GBE MDI	RTL8211	MDIP0	-
P31	SPI0_CS1#	Out	-	SPI / 1.8V	i.MX95	GPIO_IO24	Alt6
P32	GND	-	-	-	-	-	-
P33	SDIO_WP	In	-	SD / 1.8/3.3V	i.MX95	XSPI1_DQS	Alt0
P34	SDIO_CMD	Bi-Dir	-	SD / 1.8/3.3V	i.MX95	SD2_CMD	Alt0
P35	SDIO_CD#	In	-	SD / 1.8/3.3V	i.MX95	SD2_CD_B	Alt0
P36	SDIO_CK	Out	-	SD / 1.8/3.3V	i.MX95	SD2_CLK	Alt0
P37	SDIO_PWR_EN	Out	-	GPIO / 3.3V	i.MX95	SD2_RESET_B	Alt0
P38	GND	-	-	-	-	-	-
P39	SDIO_D0	Bi-Dir	-	SD / 1.8/3.3V	i.MX95	SD2_DATA0	Alt0
P40	SDIO_D1	Bi-Dir	-	SD / 1.8/3.3V	i.MX95	SD2_DATA1	Alt0
P41	SDIO_D2	Bi-Dir	-	SD / 1.8/3.3V	i.MX95	SD2_DATA2	Alt0
P42	SDIO_D3	Bi-Dir	-	SD / 1.8/3.3V	i.MX95	SD2_DATA3	Alt0
P43	SPI0_CS0#	Out	-	SPI / 1.8V	i.MX95	GPIO_IO00	Alt4
P44	SPI0_CK	Out	-	SPI / 1.8V	i.MX95	GPIO_IO03	Alt4
P45	SPI0_DIN	In	-	SPI / 1.8V	i.MX95	GPIO_IO01	Alt4
P46	SPI0_DO	Out	-	SPI / 1.8V	i.MX95	GPIO_IO02	Alt4
P47	GND	-	-	-	-	-	-
P48	SATA_TX+	-	-	-	-	-	-

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P49	SATA_TX-	-	-	-	-	-	-
P50	GND	-	-	-	-	-	-
P51	SATA_RX+	-	-	-	-	-	-
P52	SATA_RX-	-	-	-	-	-	-
P53	GND	-	-	-	-	-	-
P54	ESPI_CS0# / SPI1_CS0#	Out	-	SPI / 1.8V	i.MX95	GPIO_IO04	Alt4
P55	ESPI_CS1# / SPI1_CS1#	Out	-	SPI / 1.8V	i.MX95	GPIO_IO25	Alt6
P56	ESPI_CK / SPI1_CK	Out	-	SPI / 1.8V	i.MX95	GPIO_IO07	Alt4
P57	ESPI_IO_1 / SPI1_DIN	In	-	SPI / 1.8V	i.MX95	GPIO_IO05	Alt4
P58	ESPI_IO_0 / SPI1_DO	Out	-	SPI / 1.8V	i.MX95	GPIO_IO06	Alt4
P59	GND	-	-	-	-	-	-
P60	USB0+	Bi-Dir	-	USB / 3.3V	i.MX95	USB1_D_P	-
P61	USB0-	Bi-Dir	-	USB / 3.3V	i.MX95	USB1_D_N	-
P62	USB0_EN_OC#	In	PU-10K	GPIO / 3.3V	-	-	-
P63	USB0_VBUS_DET	-	-	-	-	-	-
P64	USB0_OTG_ID	In	-	USB / 3.3V	-	-	-
P65	USB1+	Bi-Dir	-	USB / 3.3V	USB Hub (GL3590)	DP_W	-
P66	USB1-	Bi-Dir	-	USB / 3.3V	USB Hub (GL3590)	DM_W	-
P67	USB1_EN_OC#	Bi-Dir	PU-10K	GPIO / 3.3V	USB Hub (GL3590)	OVCUR_W	-
P68	GND	-	-	-	-	-	-
P69	USB2+	Bi-Dir	-	USB / 3.3V	USB Hub (GL3590)	TXP1_X	-
P70	USB2-	Bi-Dir	-	USB / 3.3V	USB Hub (GL3590)	TXN1_X	-
P71	USB2_EN_OC#	Bi-Dir	PU-10K	GPIO / 3.3V	USB Hub (GL3590)	OVCUR_X	-
P72	RSVD	-	-	-	-	-	-

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P73	RSVD	-	-	-	-	-	-
P74	USB3_EN_OC#	Bi-Dir	PU-10K	GPIO / 3.3V	USB Hub (GL3590)	OVCUR_Y	-
P75	PCIE_A_RST#	Out	-	GPIO / 3.3V	GPIO expander(SX1509)	I/O6	-
P76	USB4_EN_OC#	Bi-Dir	PU-10K	GPIO / 3.3V	USB Hub (GL3590)	OVCUR_A	-
P77	PCIE_B_CKREQ#	Bi-Dir	PU-10K	GPIO / 3.3V	Clock Generator(RC21008)	CLKIN1_GPI3	-
P78	PCIE_A_CKREQ#	Bi-Dir	PU-10K	GPIO / 3.3V	9FGV0241AKILF	CKPWRGD_PD	-
P79	GND	-	-	-	-	-	-
P80	PCIE_C_REFCK+	Out	-	-	-	-	-
P81	PCIE_C_REFCK-	Out	-	-	-	-	-
P82	GND	-	-	-	-	-	-
P83	PCIE_A_REFCK+	Out	-	PCIe	Clock Generator(RC21008)	OUT3	-
P84	PCIE_A_REFCK-	Out	-	PCIe	Clock Generator(RC21008)	OUT3_B	-
P85	GND	-	-	-	-	-	-
P86	PCIE_A_RX+	In	-	PCIe	i.MX95	PCIE1_RX0_P	-
P87	PCIE_A_RX-	In	-	PCIe	i.MX95	PCIE1_RX0_N	-
P88	GND	-	-	-	-	-	-
P89	PCIE_A_TX+	Out	Serial-0.1uF	PCIe	i.MX95	PCIE1_TX0_P	-
P90	PCIE_A_TX-	Out	Serial-0.1uF	PCIe	i.MX95	PCIE1_TX0_N	-
P91	GND	-	-	-	-	-	-
P92	HDMI_D2+ / DP1_LANE0+	Out	-	HDMI	LT9611	TX_D0+	-
P93	HDMI_D2- / DP1_LANE0-	Out	-	HDMI	LT9611	TX_D0-	-
P94	GND	-	-	-	-	-	-

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P95	HDMI_D1+ / DP1_LANE1+	Out	-	HDMI	LT9611	TX_D1+	-
P96	HDMI_D1- / DP1_LANE1-	Out	-	HDMI	LT9611	TX_D1-	-
P97	GND	-	-	-	-	-	-
P98	HDMI_D0+ / DP1_LANE2+	Out	-	HDMI	LT9611	TX_D2+	-
P99	HDMI_D0- / DP1_LANE2-	Out	-	HDMI	LT9611	TX_D2-	-
P100	GND	-	-	-	-	-	-
P101	HDMI_CK+ / DP1_LANE3+	Out	-	HDMI	LT9611	TX_C+	-
P102	HDMI_CK- / DP1_LANE3-	Out	-	HDMI	LT9611	TX_C-	-
P103	GND	-	-	-	-	-	-
P104	HDMI_HPD / DP1_HPD	In	PD-1M	HDMI	LT9611	HPD_GPIO2	-
P105	HDMI_CTRL_CK / DP1_AUX+	Out	PU-100K	HDMI	LT9611	DSCL	-
P106	HDMI_CTRL_DAT / DP1_AUX-	Bi-Dir	PU-100K	HDMI	LT9611	DSDA	-
P107	DP1_AUX_SEL	-	-	-	-	-	-
P108	GPIO0 / CAM0_PWR#	In/Out	PU-470K	GPIO / 1.8V	MCU(STM32L431)	PB0	-
P109	GPIO1 / CAM1_PWR#	In/Out	PU-470K	GPIO / 1.8V	MCU(STM32L431)	PB1	-
P110	GPIO2 / CAM0_RST#	In/Out	PU-470K	GPIO / 1.8V	MCU(STM32L431)	PB2	-
P111	GPIO3 / CAM1_RST#	In/Out	PU-470K	GPIO / 1.8V	MCU(STM32L431)	PB5	-
P112	GPIO4 / HDA_RST#	In/Out	PU-470K	GPIO / 1.8V	i.MX95	GPIO_IO34	Alt0
P113	GPIO5 / PWM_OUT	In/Out	PU-470K	GPIO / 1.8V	i.MX95	GPIO_IO22	Alt4
P114	GPIO6 / TACHIN	In/Out	PU-470K	GPIO / 1.8V	i.MX95	XSPI1_DATA7	Alt5

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P115	GPIO7	In/Out	PU-470K	GPIO / 1.8V	i.MX95	GPIO_IO14	Alt0
P116	GPIO8	In/Out	PU-470K	GPIO / 1.8V	i.MX95	GPIO_IO15	Alt0
P117	GPIO9	In/Out	PU-470K	GPIO / 1.8V	i.MX95	CCM_CLKO2	Alt5
P118	GPIO10	In/Out	PU-470K	GPIO / 1.8V	i.MX95	CCM_CLKO4	Alt5
P119	GPIO11	In/Out	PU-470K	GPIO / 1.8V	MCU(STM32L431)	PB10	-
P120	GND	-	-	-	-	-	-
P121	I2C_PM_CK	Out	PU-2k2	I2C / 1.8V	i.MX95	GPIO_IO29	Alt1
P122	I2C_PM_DAT	Bi-Dir	PU-2k2	I2C / 1.8V	i.MX95	GPIO_IO28	Alt1
P123	BOOT_SEL0#	In	PU-10K	GPIO / 1.8V	MCU(STM32L431)	PC6	-
P124	BOOT_SEL1#	In	PU-10K	GPIO / 1.8V	MCU(STM32L431)	PC7	-
P125	BOOT_SEL2#	In	PU-10K	GPIO / 1.8V	MCU(STM32L431)	PC8	-
P126	RESET_OUT#	Out	PU-100K	GPIO / 1.8V	Logic IC	Logic IC	-
P127	RESET_IN#	In	PU-10K	GPIO / 1.8V	Logic IC	Logic IC	-
P128	POWER_BTN#	In	PU-100K	GPIO / 1.8V	i.MX95	ONOFF	-
P129	SER0_TX	Out	-	UART / 1.8V	i.MX95	GPIO_IO08	Alt5
P130	SER0_RX	In	-	UART / 1.8V	i.MX95	GPIO_IO09	Alt5
P131	SER0_RTS#	In	-	UART / 1.8V	i.MX95	GPIO_IO11	Alt5
P132	SER0_CTS#	Out	-	UART / 1.8V	i.MX95	GPIO_IO10	Alt5
P133	GND	-	-	-	-	-	-
P134	SER1_TX	Out	-	UART / 1.8V	i.MX95	UART1_TXD	Alt0
P135	SER1_RX	In	-	UART / 1.8V	i.MX95	UART1_RXD	Alt0
P136	SER2_TX	Out	-	UART / 1.8V	i.MX95	GPIO_IO04	Alt5
P137	SER2_RX	In	-	UART / 1.8V	i.MX95	GPIO_IO05	Alt5
P138	SER2_RTS#	In	-	UART / 1.8V	i.MX95	GPIO_IO07	Alt5
P139	SER2_CTS#	Out	-	UART / 1.8V	i.MX95	GPIO_IO06	Alt5
P140	SER3_TX	Out	-	UART / 1.8V	i.MX95	UART2_TXD	Alt0

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P141	SER3_RX	In	-	UART / 1.8V	i.MX95	UART2_RXD	Alt0
P142	GND	-	-	-	-	-	-
P143	CAN0_TX	Out	-	CAN / 1.8V	i.MX95	PDM_CLK	Alt6
P144	CAN0_RX	In	-	CAN / 1.8V	i.MX95	PDM_BIT_STREAM0	Alt6
P145	CAN1_TX	Out	-	CAN / 1.8V	i.MX95	GPIO_IO30	Alt2
P146	CAN1_RX	In	-	CAN / 1.8V	i.MX95	GPIO_IO31	Alt2
P147	VDD_IN	PWR	-	-	From Carrier board	-	-
P148	VDD_IN	PWR	-	-	From Carrier board	-	-
P149	VDD_IN	PWR	-	-	From Carrier board	-	-
P150	VDD_IN	PWR	-	-	From Carrier board	-	-
P151	VDD_IN	PWR	-	-	From Carrier board	-	-
P152	VDD_IN	PWR	-	-	From Carrier board	-	-
P153	VDD_IN	PWR	-	-	From Carrier board	-	-
P154	VDD_IN	PWR	-	-	From Carrier board	-	-
P155	VDD_IN	PWR	-	-	From Carrier board	-	-
P156	VDD_IN	PWR	-	-	From Carrier board	-	-
S1	CSI1_TX+ / I2C_CAM1_CK	Out	PU-2k2	I2C / 1.8V	i.MX95	GPIO_IO29	Alt1
S2	CSI1_TX- / I2C_CAM1_DAT	Bi-Dir	PU-2k2	I2C / 1.8V	i.MX95	GPIO_IO28	Alt1
S3	GND	-	-	-	-	-	-
S4	RSVD	-	-	-	-	-	-
S5	CSI0_TX- / I2C_CAM0_CK	Out	PU-2k2	-	i.MX95	I2C2_SCL	Alt0
S6	CAM_MCK	Out	-	GPIO / 1.8V	i.MX95	CCM_CLKO1	Alt0
S7	CSI0_TX+ / I2C_CAM0_DAT	Bi-Dir	PU-2k2	-	i.MX95	I2C2_SDA	Alt0

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S8	CSI0_CK+	In	-	MIPI_CSI	i.MX95	MIPI_DSICSI1_CLK_P	-
S9	CSI0_CK-	In	-	MIPI_CSI	i.MX95	MIPI_DSICSI1_CLK_N	-
S10	GND	-	-	-	-	-	-
S11	CSI0_RX0+	In	-	MIPI_CSI	i.MX95	MIPI_DSICSI1_D0_P	-
S12	CSI0_RX0-	In	-	MIPI_CSI	i.MX95	MIPI_DSICSI1_D0_N	-
S13	GND	-	-	-	-	-	-
S14	CSI0_RX1+	In	-	MIPI_CSI	i.MX95	MIPI_DSICSI1_D1_P	-
S15	CSI0_RX1-	In	-	MIPI_CSI	i.MX95	MIPI_DSICSI1_D1_N	-
S16	GND	-	-	-	-	-	-
S17	GBE1_MDI0+	Bi-Dir	-	GBE MDI	RTL8211	MDIP0	-
S18	GBE1_MDI0-	Bi-Dir	-	GBE MDI	RTL8211	MDIN0	-
S19	GBE1_LINK100#	Out	-	GPIO / 3.3V	RTL8211	LED0	-
S20	GBE1_MDI1+	Bi-Dir	-	GBE MDI	RTL8211	MDIP1	-
S21	GBE1_MDI1-	Bi-Dir	-	GBE MDI	RTL8211	MDIN1	-
S22	GBE1_LINK1000#	Out	-	GPIO / 3.3V	RTL8211	LED1	-
S23	GBE1_MDI2+	Bi-Dir	-	GBE MDI	RTL8211	MDIP2	-
S24	GBE1_MDI2-	Bi-Dir	-	GBE MDI	RTL8211	MDIN2	-
S25	GND	-	-	-	-	-	-
S26	GBE1_MDI3+	Bi-Dir	-	GBE MDI	RTL8211	MDIP3	-
S27	GBE1_MDI3-	Bi-Dir	-	GBE MDI	RTL8211	MDIN3	-
S28	GBE1_CTREF	PWR	-	Analog / 3.3V	-	-	-
S29	PCIE_D_TX+ / SERDES_1_TX+	Out	Serial-0.1uF	SERDES	i.MX95	ETH_TX0_P	-
S30	PCIE_D_TX- / SERDES_1_TX-	Out	Serial-0.1uF	SERDES	i.MX95	ETH_TX0_N	-
S31	GBE1_LINK_ACT#	Out	-	GPIO / 3.3V	RTL8211	LED3	-

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S32	PCIE_D_RX+ / SERDES_1_RX+	In	-	SERDES	i.MX95	ETH_RX0_P	-
S33	PCIE_D_RX- / SERDES_1_RX-	In	-	SERDES	i.MX95	ETH_RX0_N	-
S34	GND	-	-	-	-	-	-
S35	USB4+	Bi-Dir	-	USB / 3.3V	USB Hub (GL3590)	DP_A	-
S36	USB4-	Bi-Dir	-	USB / 3.3V	USB Hub (GL3590)	DM_A	-
S37	USB3_VBUS_DET	-	-	-	-	-	-
S38	AUDIO_MCK	Out	-	SAI / 1.8V	i.MX95	GPIO_IO17	Alt1
S39	I2S0_LRCK	Bi-Dir	-	SAI / 1.8V	i.MX95	GPIO_IO26	Alt7
S40	I2S0_SDOUT	Out	-	SAI / 1.8V	i.MX95	GPIO_IO21	Alt1
S41	I2S0_SDIN	In	-	SAI / 1.8V	i.MX95	GPIO_IO20	Alt1
S42	I2S0_CK	Bi-Dir	-	SAI / 1.8V	i.MX95	GPIO_IO16	Alt1
S43	ESPI_ALERT0#	-	-	-	-	-	-
S44	ESPI_ALERT1#	-	-	-	-	-	-
S45	MDIO_CLK	Out	-	SERDES / 1.8V	i.MX95	ENET1_MDC	Alt0
S46	MDIO_DAT	Bi-Dir	PU-1.5K	SERDES / 1.8V	i.MX95	ENET1_MDIO	Alt0
S47	GND	-	-	-	-	-	-
S48	I2C_GP_CK	Out	PU-2.2K	I2C / 1.8V	i.MX95	GPIO_IO12	Alt6
S49	I2C_GP_DAT	Bi-Dir	PU-2.2K	I2C / 1.8V	i.MX95	GPIO_IO13	Alt6
S50	HDA_SYNC / I2S2_LRCK	-	-	-	-	-	-
S51	HDA_SDO / I2S2_SDOUT	-	-	-	-	-	-
S52	HDA_SDI / I2S2_SDIN	-	-	-	-	-	-
S53	HDA_CK / I2S2_CK	-	-	-	-	-	-
S54	SATA_ACT#	-	-	-	-	-	-

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S55	USB5_EN_OC#	Bi-Dir	PU-10K	GPIO / 3.3V	GPIO expander(SX1509)	OVCUR_B	-
S56	ESPI_IO_2	-	-	-	-	-	-
S57	ESPI_IO_3	-	-	-	-	-	-
S58	ESPI_RESET#	-	-	-	-	-	-
S59	USB5+	Bi-Dir	-	USB / 3.3V	USB Hub (GL3590)	DP_B	-
S60	USB5-	Bi-Dir	-	USB / 3.3V	USB Hub (GL3590)	DM_B	-
S61	GND	-	-	-	-	-	-
S62	USB3_SSTX+	Out	Serial-0.1uF	USB3	USB Hub (GL3590)	TXP1_Y	-
S63	USB3_SSTX-	Out	Serial-0.1uF	USB3	USB Hub (GL3590)	TXN1_Y	-
S64	GND	-	-	-	-	-	-
S65	USB3_SSRX+	In	-	USB3	USB Hub (GL3590)	RXP1_Y	-
S66	USB3_SSRX-	In	-	USB3	USB Hub (GL3590)	RXN1_Y	-
S67	GND	-	-	-	-	-	-
S68	USB3+	Bi-Dir	-	USB / 3.3V	USB Hub (GL3590)	DP_Y	-
S69	USB3-	Bi-Dir	-	USB / 3.3V	USB Hub (GL3590)	DM_Y	-
S70	GND	-	-	-	-	-	-
S71	USB2_SSTX+	Out	Serial-0.1uF	USB3	USB Hub (GL3590)	TXP1_X	-
S72	USB2_SSTX-	Out	Serial-0.1uF	USB3	USB Hub (GL3590)	TXN1_X	-
S73	GND	-	-	-	-	-	-
S74	USB2_SSRX+	In	-	USB3	USB Hub (GL3590)	RXP1_X	-
S75	USB2_SSRX-	In	-	USB3	USB Hub (GL3590)	RXN1_X	-
S76	PCIE_B_RST#	Out	-	GPIO / 3.3V	GPIO expander(SX1509)	I/O7	-
S77	PCIE_C_RST#	Out	-	GPIO / 3.3V	GPIO expander(SX1509)	I/O2	-

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S78	PCIE_C_RX+ / SERDES_2_RX+	-	-	-	-	-	-
S79	PCIE_C_RX- / SERDES_2_RX-	-	-	-	-	-	-
S80	GND	-	-	-	-	-	-
S81	PCIE_C_TX+ / SERDES_2_TX+	-	-	-	-	-	-
S82	PCIE_C_TX- / SERDES_2_TX-	-	-	-	-	-	-
S83	GND	-	-	-	-	-	-
S84	PCIE_B_REFCK+	Out	-	PCIe	Clock Generator(RC21008)	OUT6	-
S85	PCIE_B_REFCK-	Out	-	PCIe	Clock Generator(RC21008)	OUT6_B	-
S86	GND	-	-	-	-	-	-
S87	PCIE_B_RX+	In	-	PCIe	i.MX95	PCIE2_RX0_P	-
S88	PCIE_B_RX-	In	-	PCIe	i.MX95	PCIE2_RX0_N	-
S89	GND	-	-	-	-	-	-
S90	PCIE_B_TX+	Out	Serial-0.1uF	PCIe	i.MX95	PCIE2_TX0_P	-
S91	PCIE_B_TX-	Out	Serial-0.1uF	PCIe	i.MX95	PCIE2_TX0_N	-
S92	GND	-	-	-	-	-	-
S93	DP0_LANE0+	-	-	-	-	-	-
S94	DP0_LANE0-	-	-	-	-	-	-
S95	DP0_AUX_SEL	-	-	-	-	-	-
S96	DP0_LANE1+	-	-	-	-	-	-
S97	DP0_LANE1-	-	-	-	-	-	-
S98	DP0_HPD	-	-	-	-	-	-
S99	DP0_LANE2+	-	-	-	-	-	-

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S100	DP0_LANE2-	-	-	-	-	-	-
S101	GND	-	-	-	-	-	-
S102	DP0_LANE3+	-	-	-	-	-	-
S103	DP0_LANE3-	-	-	-	-	-	-
S104	USB3_OTG_ID	-	-	-	-	-	-
S105	DP0_AUX+	-	-	-	-	-	-
S106	DP0_AUX-	-	-	-	-	-	-
S107	LCD1_BKLT_EN	Out	PD-100K	GPIO / 1.8V	MCU(STM32L431)	PA1	-
S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	Out	-	DSI/LVDS	i.MX95	LVDS1_CLK_P	-
S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	Out	-	DSI/LVDS	i.MX95	LVDS1_CLK_N	-
S110	GND	-	-	-			-
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	Out	-	LVDS	i.MX95	LVDS1_D0_P	-
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	Out	-	LVDS	i.MX95	LVDS1_D0_N	-
S113	eDP1_HPD / DSI1_TE	-	-	-	-	-	-
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	Out	-	LVDS	i.MX95	LVDS1_D1_P	-
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	Out	-	LVDS	i.MX95	LVDS1_D1_N	-
S116	LCD1_VDD_EN	Out	PD-100K	GPIO / 1.8V	MCU(STM32L431)	PA0	-

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S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	Out	-	LVDS	i.MX95	LVDS1_D2_P	-
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	Out	-	LVDS	i.MX95	LVDS1_D2_N	-
S119	GND	-	-	-	-	-	-
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	Out	-	LVDS	i.MX95	LVDS1_D3_P	-
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	Out	-	LVDS	i.MX95	LVDS1_D3_N	-
S122	LCD1_BKLT_PWM	Out	-	GPIO / 1.8V	i.MX95	GPIO_IO23	Alt4
S123	GPIO13	In/Out	PU-470K	GPIO / 1.8V	MCU(STM32L431)	PA3	-
S124	GND	-	-	-	-	-	-
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	Out	-	DSI/LVDS	i.MX95	DSICSI_D0_P/LVDS0_D0_P	-
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	Out	-	DSI/LVDS	i.MX95	DSICSI_D0_N/LVDS0_D0_N	-
S127	LCD0_BKLT_EN	Out	PD-100K	GPIO / 1.8V	MCU(STM32L431)	PA12	-
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	Out	-	DSI/LVDS	i.MX95	DSICSI_D1_P/LVDS0_D1_P	-
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	Out	-	DSI/LVDS	i.MX95	DSICSI_D1_N/LVDS0_D1_N	-
S130	GND	-	-	-	-	-	-

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S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	Out	-	DSI/LVDS	i.MX95	DSI_D2_P/LVDS0_D2_P	-
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	Out	-	DSI/LVDS	i.MX95	DSI_D2_N/LVDS0_D2_N	-
S133	LCD0_VDD_EN	Out	PD-100K	GPIO/1.8V	MCU(STM32L431)	PA11	-
S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	Out	-	DSI/LVDS	i.MX95	DSICSI_CLK_P/LVDS0_CLK_P	-
S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	Out	-	DSI/LVDS	i.MX95	DSICSI_CLK_N/LVDS0_CLK_N	-
S136	GND	-	-	-	-	-	-
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	Out	-	DSI/LVDS	i.MX95	DSI_D3_P/LVDS0_D3_P	-
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	Out	-	DSI/LVDS	i.MX95	DSI_D3_N/LVDS0_D3_N	-
S139	I2C_LCD_CK	Out	PU-2.2K	I2C / 1.8V	i.MX95	I2C2_SCL	Alt0
S140	I2C_LCD_DAT	Bi-Dir	PU-2.2K	I2C / 1.8V	i.MX95	I2C2_SDA	Alt0
S141	LCD0_BKLT_PWM	Out	-	GPIO / 1.8V	i.MX95	GPIO_IO19	Alt1
S142	GPIO12	In/Out	PU-470K	GPIO / 1.8V	MCU(STM32L431)	PA4	-
S143	GND	-	-	-	-	-	-
S144	eDP0_HPD / DSI0_TE	In	PD-1M	GPIO / 1.8V	GPIO expander(SX1509)	I/O15	-
S145	WDT_TIME_OUT#	Out	-	GPIO / 1.8V	i.MX95	WDOG_ANY	Alt0
S146	PCIE_WAKE#	In	PU-10K	GPIO / 3.3V	GPIO expander(PCAL6408)	P6	-

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S147	VDD_RTC	PWR	-	Analog / 2V~3.25V	PCF8563BS	VDD	-
S148	LID#	In	PU-10K	GPIO / 1.8V	GPIO expander(SX1509)	I/O9	-
S149	SLEEP#	In	PU-10K	GPIO / 1.8V	GPIO expander(SX1509)	I/O10	-
S150	VIN_PWR_BAD#	In	PU-10K	GPIO / 5V	Logic IC	Logic IC	-
S151	CHARGING#	Out	PU-10K	GPIO / 1.8V	GPIO expander(SX1509)	I/O11	-
S152	CHARGER_PRSNT#	Out	PU-10K	GPIO / 1.8V	GPIO expander(SX1509)	I/O12	-
S153	CARRIER_STBY#	Out	-	GPIO / 1.8V	Logic IC	Logic IC	-
S154	CARRIER_PWR_ON	Out	-	GPIO / 1.8V	Logic IC	Logic IC	-
S155	FORCE_RECOV#	In	PU-10K	GPIO / 1.8V	MCU(STM32L431)	PC9	-
S156	BATLOW#	In	PU-10K	GPIO / 1.8V	GPIO expander(SX1509)	I/O13	-
S157	TEST#	In	PU-10K	GPIO / 1.8V	GPIO expander(SX1509)	I/O14	-
S158	GND	-	-	-	-	-	-

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5. Software Support

5.1 Early Access

All software should use the standard NXP BSP release, with source code available in our Git repository.
Deliverables: Prebuilt runtime images will be available at launch for quick evaluation.

5.2 Yocto

based on the NXP Yocto upstream repository: https://github.com/Freescale/meta-freescale

Available on the ADLINK GitHub site: https://github.com/ADLINK/meta-adlink-nxp

- Yocto meta layer with u-boot, kernel, and root filesystem
- Yocto binary image for quick evaluation
- User guide for building the BSP and deploying the binary image

5.3 Android

By project basis.

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6. Mechanical and Thermal

6.1 Module Dimensions

The module must be SMARC Short Size (82 x 50 mm)

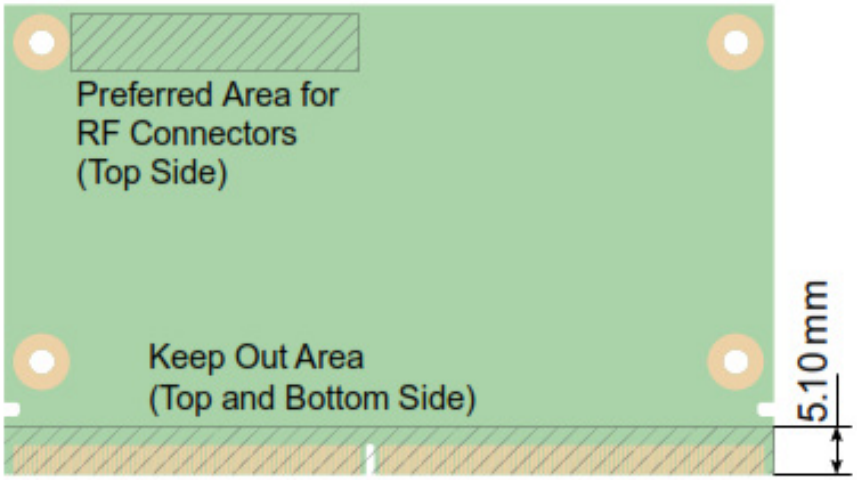


Figure 3 – Module dimensions

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6.2 Thermal Solutions

6.2.1 Heatspreader: HTS

Sustained temperature range with high-performance LAB copper heatsink and high airflow: -40°C to 85°C ambient.

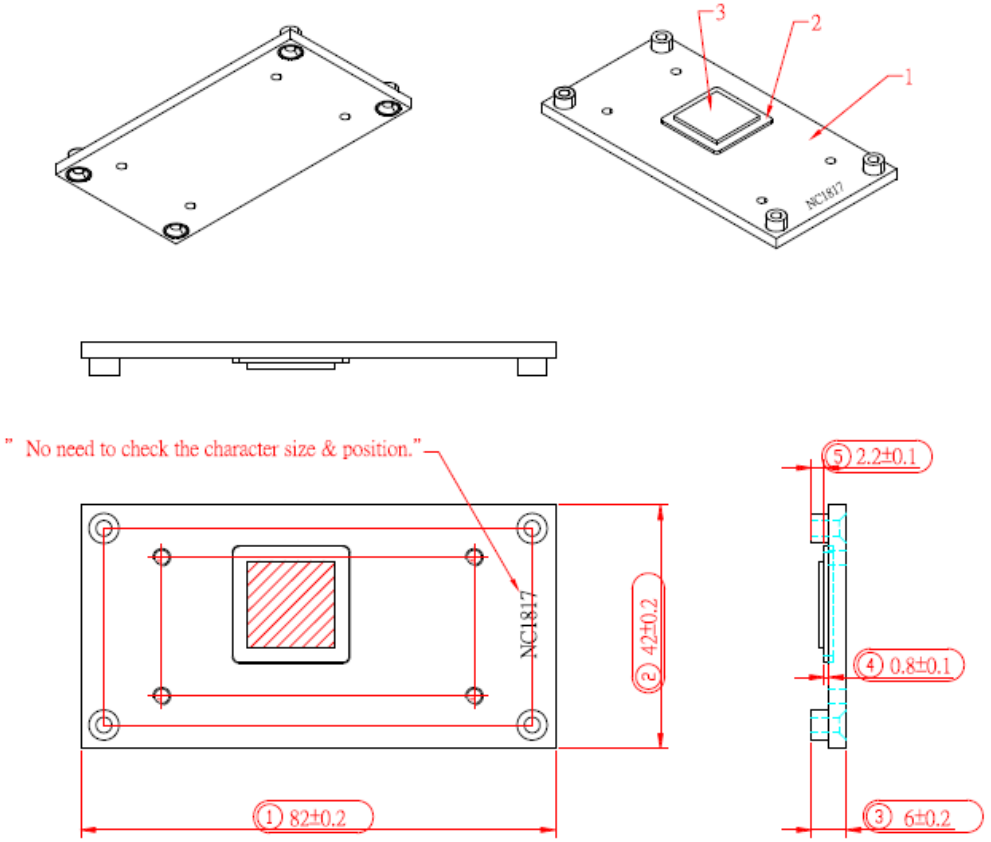


Figure 4 – Heatspreader: HTS

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6.2.2 Heatsink: THS

Sustained temperature range with moderate airflow: 0°C to 60°C ambient.

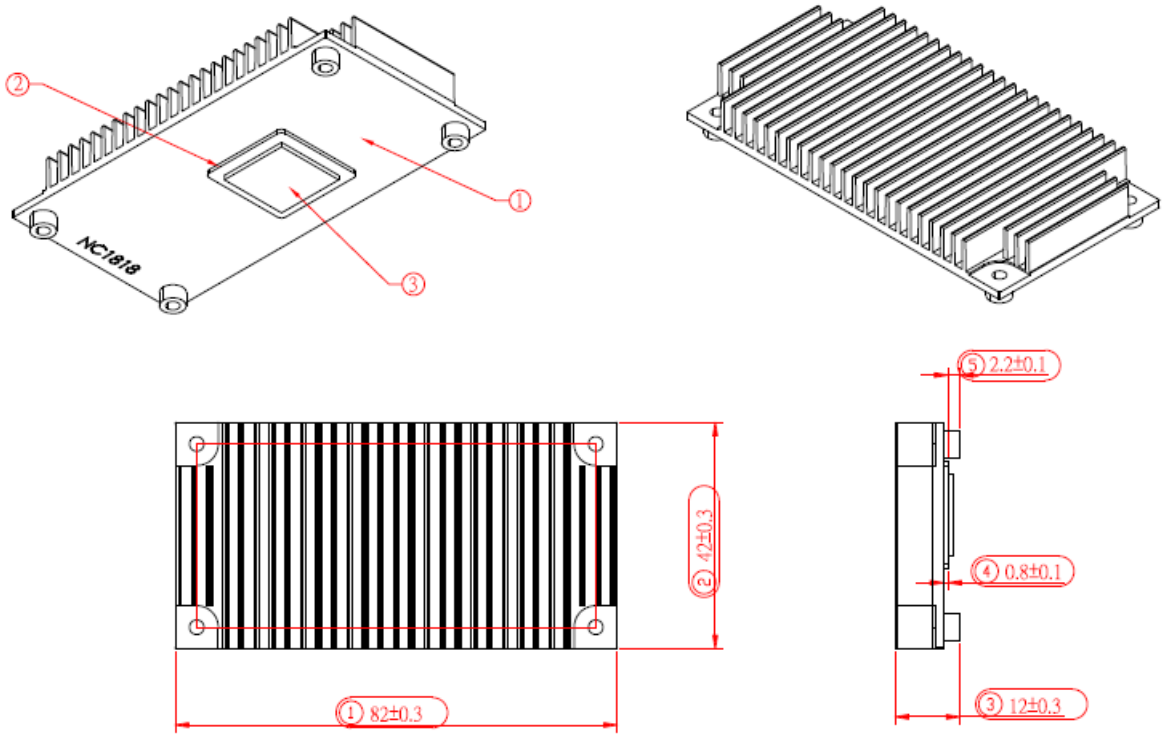


Figure 5 – Heatsink: THS

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