PCIe-9834

4CH 16-bit 80MS/s Digitizer

PCIe-9834/PCIe-9834P

User's Manual



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Revision History

Revision	Release Date	Description of Change(s)
2.00	June 3. 2016	Initial Release

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Preface

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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

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NOTE:

Additional information, aids, and tips that help users perform tasks.


CAUTION:

Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.


WARNING:

Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

The ADLINK PCIe-9834 is a 4-channel, 16-bit, 80MS/s PCI Express digitizer providing speedy, high quality data acquisition. Each of the four input channels supports up to 80MS/s sampling, with16-bit resolution A/D converter. 40MHz bandwidth analog input with 50Ω impedance receives ±0.5V, ±1V, ±5V, and ±10V high speed signals, and a simplified front end and highly stable onboard reference provide both highly accurate measurement results and high dynamic performance.

The PCIe-9834, based on x4 lane slot PCI Express technology, can be used in any standard PCI Express slot, x4, x8, or x16. With a PCI Express bus interface and extremely large onboard memory (up to 1GB), the PCIe-9834 easily manages simultaneous 4-CH data streaming even at the highest sampling rates.

The PCIe-9834 is auto-calibrated with an onboard reference circuit calibrating offset and acquiring analog input errors. Following auto-calibration, the calibration constant is stored in EEPROM, such that these values can be loaded and used as needed by the board. There is no requirement to calibrate the module manually.

1.1 Features

- Up to 80MS/s sampling
- 4 simultaneous analog inputs
- High resolution 16-bit ADC
- Up to 40 MHz bandwidth for analog input
- 1GB onboard storage
- Programmable input voltage of ±0.5V, ±1V, ±5V, or ±10V
- Scatter/gather DMA data transfer for high speed streaming
- 10 or 20MHz digital onboard filter (FPGA)
- PLL module provides precise synch (PCIe-9834P only)
- Supports:
  - One external digital trigger input
  - One external clock input
- Full auto-calibration

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1.2 Applications

- Testing/monitoring for Energy Management applications, including:
  - Partial discharge
  - Power line/device monitoring
- Non-destructive testing
- Radar acquisition
- LiDAR

1.3 Specifications

1.3.1 Analog Input

Item	Spec	Notes
Channels	4 single-ended	
Connector type	SMB	
Input coupling	DC	
ADC resolution	16-Bit	
Input range	±0.5 V, ±1 V, ± 5V, or ± 10V	± 10V only supported Input impedance 1MΩ
Bandwidth (-3dB)	40MHz	
Overvoltage	±10V sine wave/7Vrms	50Ω, ±0.5V or ±1V or ± 5V
	±10V	1MΩ, ±0.5V or ±1V
	±30V	1MΩ, ±5V or ±10V
Input impedance	50Ω or 1MΩ, software selectable	
Digital filter	10MHz or 20MHz, software selectable	
Offset Error	±0.1mV	±0.5V
	±0.2mV	±1V
	±0.5mV	±5V, or ±10V

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Item	Spec	Notes
Gain Error	±0.15%	
System Noise (RMS)	0.1mV	±0.5V
	0.15mV	±1V
	1mV	±5V
	1.5 mV	±10 V
Crosstalk	-80 dB	±0.5 V
	-90 dB	±1 V or ± 5V or ± 10V
SNR	67 dB	
THD	-78 dB	
SFDR	78 dB	

Table 1-1: Channel Characteristics

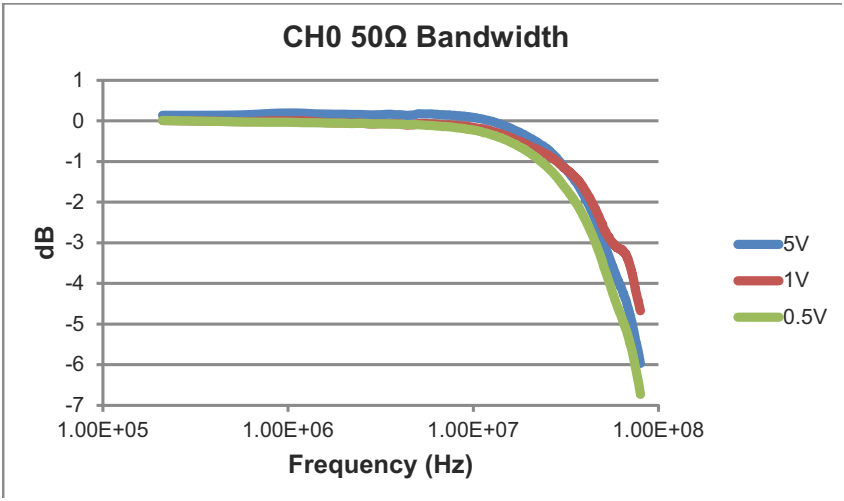


Figure 1-1: Analog Input Channel Bandwidth

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1.3.2 Timebase

Sample Clock	Detail	Comment
Timebase options	Internal : onboard crystal oscillator	
	External : CLK IN (front panel)	
Sampling clock frequency	Internal : 80MHz	1.22kS/s to 80MS/s
	External : 20MHz to 80MHz (CLK IN)	
Timebase accuracy	< ± 25ppm	
External reference clock source	REF_CLK (supported by PCI-9834P only)	
External reference clock	10MHz	
External reference clock input range	3.3V to 5V TTL	DC compliant
External sampling clock input range	1Vpp to 5Vpp	AC / DC compliant

1.3.3 Triggers

Trigger Source & Mode	
Trigger source	Software, external digital trigger, analog trigger, and SSI (system synchronized interface)
Trigger mode	Post trigger, delay trigger, pre-trigger, or middle trigger, re-trigger for post trigger and delay trigger modes

Digital Trigger Input	
Sources	Front panel SMB connector
Compatibility	3.3 V TTL, 5 V tolerant
Input high threshold	2.0 V
Input low threshold (VIL)	0.8 V
Maximum input overload	-0.5 V to +5.5 V
Trigger polarity	Rising or falling edge

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Digital Trigger Input	
Pulse width	20 ns minimum

1.3.4 General Specifications

Specifications	
Dimensions	167.64 W x 106.68 H mm (6.53 x 4.16 in)
Bus interface	PCI Express Gen 1 x 4
Operating	Temperature: 0°C - 50°C Relative humidity: 5% - 95%, non-condensing
Storage	Temperature: -20°C - +80°C Relative humidity: 5% - 95%, non-condensing

Calibration	
Onboard reference	+1.8V, +0.9V, and +0.45V
Temperature coefficient	1.0 ppm/°C
Warm-up time	15 minutes

	PCIe-9834		PCIe-9834P	
Power Rail	Standby Current (mA)	Full Load (mA)	Standby Current (mA)	Full Load (mA)
3.3V	18	18	18.7	21.4
12V	450	470	675	697
Total RMS Power (W)	5.459	5.699	8.162	8.435

1.4 Software Support

ADLINK provides versatile software drivers and packages to suit various user approaches to building a system. Aside from programming libraries, such as DLLs, for most Windows-based systems, ADLINK also provides drivers for other application environments such as LabVIEW®.

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All software options are included in the ADLINK All-in-One CD. Commercial software drivers are protected with licensing codes. Without the code, you may install and run the demo version for trial/demonstration purposes for only up to two hours. Contact your ADLINK dealer to purchase the software license.

1.4.1 WD-DASK

WD-DASK includes device drivers and DLL for Windows XP/7/8/10. DLL is binary compatible across Windows XP/7/8/10. This means all applications developed with WD-DASK are compatible with these Windows operating systems. The development environment may be VB, VB.NET, VC++, BCB, and Delphi, or any Windows programming language that allows calls to a DLL. The WD-DASK user and function reference manuals are on the ADLINK All-in-One CD.

1.4.2 LabVIEW Support

For customers who want to write their own programs in LabVIEW, a LabVIEW library toolkit, DAQ-LabVIEW Plus, is provided to support PCIe-9834 card use.

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1.5 Device Layout and I/O Array

NOTE:

All dimensions are in mm

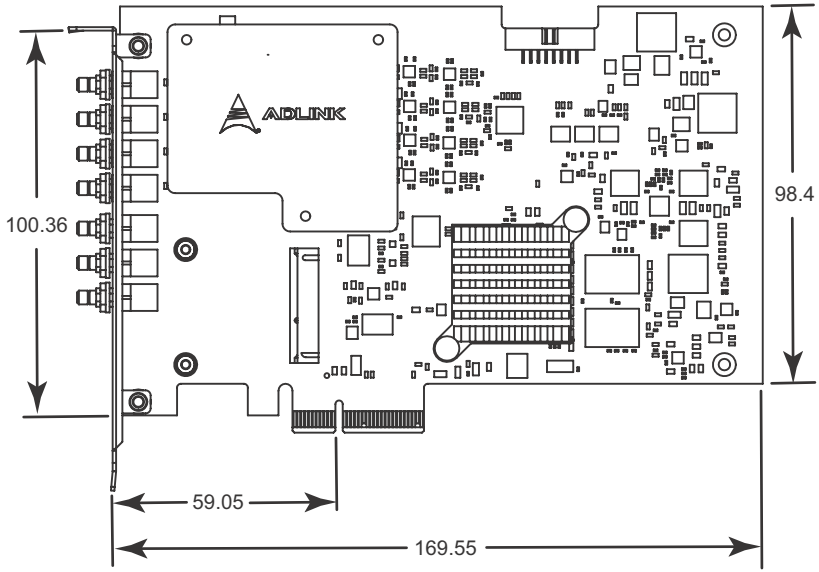


Figure 1-2: PCIe-9834 Schematic

The PCIe-9834 I/O array is labeled to indicate connectivity, as shown.

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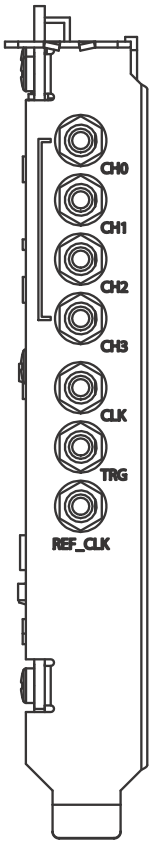


Figure 1-3: PCIe-9834 I/O Array

All I/O connectors are SMB snap-on.

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Input	Faceplate Label	Remark
Analog	CH0	Analog Input Channel
Analog	CH1	
Analog	CH2	
Analog	CH3	
Ext. Clock	CLK	Input for external sample clock to digitizer
Ext. Digital Trigger	TRG	External digital trigger input, receiving trigger signal from external instrument and initiating acquisition
Ext. Reference Clock Input	REF_CLK	(PCIe-9834P with PLL module only) REF_CLK can be used to receive an external reference 10MHz clock to generate ADC timebase. See Section 3.5.2 External Reference Clock (PCIe-9834P only)

Table 1-2: PCIe-9834 I/O Array Legend

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2 Getting Started

This chapter describes proper installation environment, installation procedures, package contents and basic information users should be aware of regarding the PCIe-9834.


NOTE:

Diagrams and illustrated equipment are for reference only. Actual system configuration and specifications may vary.

2.1 Installation Environment

When unpacking and preparing to install, please refer to Important Safety Instructions.

Only install equipment in well-lit areas on flat, sturdy surfaces with access to basic tools such as flat- and cross-head screwdrivers, preferably with magnetic heads as screws and standoffs are small and easily misplaced.

Recommended Installation Tools

- Phillips (cross-head) screwdriver
- Flat-head screwdriver
- Anti-static wrist strap
- Antistatic mat

The ADLINK PCIe-9834 is electrostatically sensitive and can be easily damaged by static electricity. The module must be handled on a grounded anti-static mat. The operator must wear an anti-static wristband, grounded at the same point as the anti-static mat.

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Inspect the carton and packaging for damage. Shipping and handling could cause damage to the equipment inside. Make sure that the equipment and its associated components have no damage before installation.



The equipment must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the equipment and wear a grounded wrist strap when servicing.

- **Package Contents**
- PCIe-9834 digitizer
- ADLINK All-in-one compact disc
- PCIe-9834 Quick Start Guide

If any of these items are missing or damaged, contact the dealer



Do not install or apply power to equipment that is damaged or missing components. Retain the shipping carton and packing materials for inspection. Please contact your ADLINK dealer/ vendor immediately for assistance and obtain authorization before returning any product.

2.2 Installing the Module

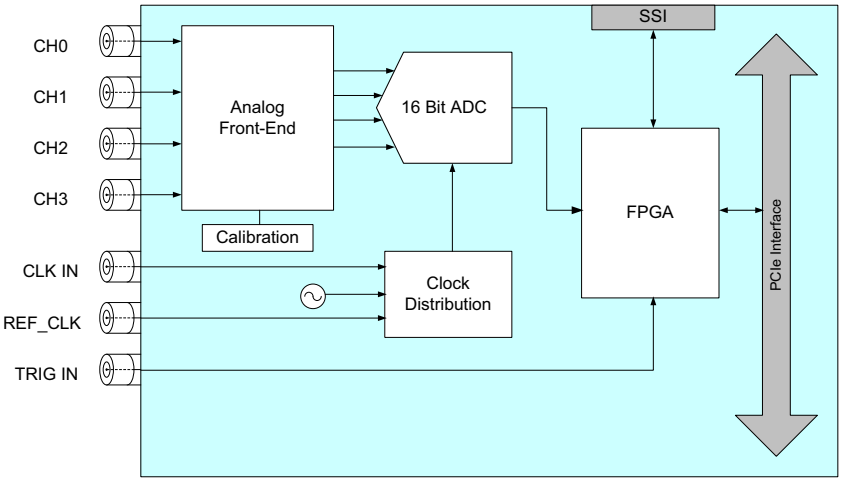
1. Turn off the computer.
2. Remove the top cover.
3. Select an available PCI express x4 slot and remove the bracket-retaining screw and the bracket cover.
4. Line up the PCI express digitizer with the PCI express slot on the back panel. Slowly push down on the top of the PCI express digitizer until its card-edge connector is resting on the slot receptacle.
5. Install the bracket-retaining screw to secure the PCI express digitizer to the back panel rail.
6. Replace the computer cover.

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3 Operations

This chapter contains information regarding analog input, triggering and timing for the PCIe-9834.

3.1 Functional Block Diagram



3.2 Analog Input Channel

3.2.1 Analog Input Front-End Configuration

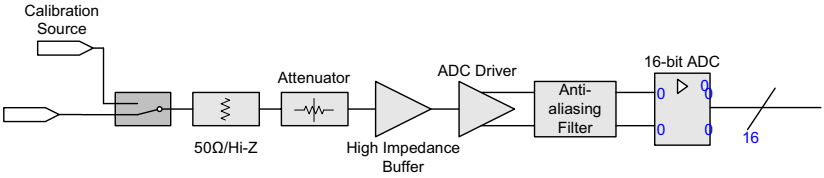


Figure 3-1: Analog Input Architecture

Input Configuration

The input channel terminates with equivalent 50Ω or 1MΩ input impedance (selected by software). The 16-bit ADC provides

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not only accurate DC performance but also high signal-to-noise ratio, and high spurious-free dynamic range in AC performance. The ADC transfers data to system memory via the high speed PCI Express Gen 1 X 4 interface.

For auto-calibration, internal calibration provides stable and accurate reference voltage to the AI.

3.2.2 Input Range and Data Format

Data format of the PCIe-9834 is 2's complement.

D15	D14	D13	D12	….	D3	D2	D1	D0
D15 to D0 bits represent the 16-bit data from ADC (2's complement)								

Table 3-1: Input Range and Data Format

	Full Scale Range	Least Significant Bit	FSR-1LSB	-FSR
Bipolar Analog Input	± 10.0V	0.305 mV	9.999694824	-10V
	± 5.0V	0.153 mV	4.999847412	-5V
	± 1.0V	0.031 mV	0.999969482	-1V
	± 0.5V	0.015 mV	0.499984741	-0.5V
Digital Code	N/A	N/A	7FFF	8000

Table 3-2: Input Range FSR and –FSR Values

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	Midscale +1LSB	Midscale	Midscale -1LSB
Bipolar Analog Input	0.305 mV	0 V	-0.305 mV
	0.153 mV	0 V	-0.153 mV
	0.031 mV	0 V	-0.031 mV
	0.015 mV	0 V	-0.015 mV
Digital Code	0001	0000	FFFF

Table 3-3: Input Range Midscale Values

3.2.3 DMA Data Transfer

The PCIe-9834, a PCIe Gen 1 X 4 device, is equipped with a 80MS/s high sampling rate ADC, generating a 640 MByte/second rate.

To provide efficient data transfer, a PCI bus-mastering DMA is essential for continuous data streaming, as it helps to achieve full potential PCI Express bus bandwidth. The bus-mastering controller releases the burden on the host CPU since data is directly transferred to the host memory without intervention. Once analog input operation begins, the DMA returns control of the program. During DMA transfer, the hardware temporarily stores acquired data in the onboard AD Data FIFO, and then transfers the data to a user-defined DMA buffer in the computer.

Using a high-level programming library for high speed DMA data acquisition, the sampling period and the number of conversions needs simply to be assigned into specified counters. After the AD trigger condition is met, the data will be transferred to the system memory by the bus-mastering DMA.

In a multi-user or multi-tasking OS, such as Microsoft Windows, Linux, or other, it is difficult to allocate a large continuous memory block. Therefore, the bus controller provides DMA transfer with scatter-gather function to link non-contiguous memory blocks into a linked list so users can transfer large amounts of data without being limited by memory limitations. In non-scatter-gather mode,

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the maximum DMA data transfer size is 2 MB double words (8 MB bytes); in scatter-gather mode, there is no limitation on DMA data transfer size except the physical storage capacity of the system.

Users can also link descriptor nodes circularly to achieve a multi-buffered DMA. Figure 3-2 illustrates a linked list comprising three DMA descriptors. Each descriptor contains a PCI address, PCI dual address, a transfer size, and the pointer to the next descriptor. PCI address and PCI dual address support 64-bit addresses which can be mapped into more than 4 GB of address space, but the subsequent descriptor address must be less than 4GB.

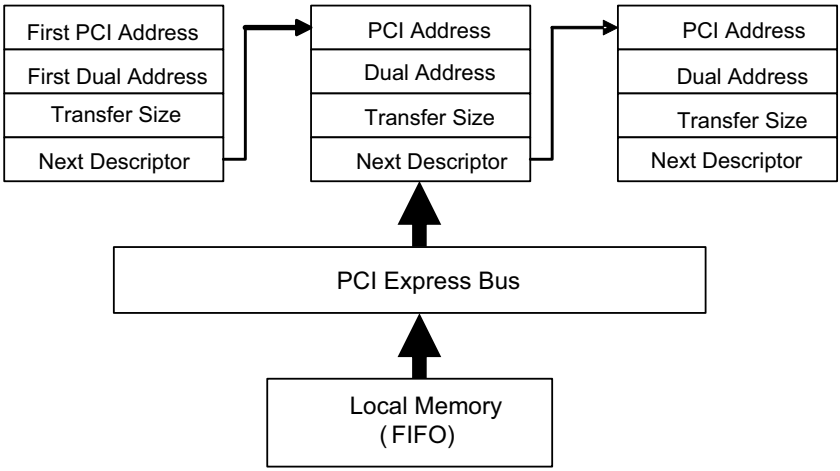


Figure 3-2: Linked List of PCI Address DMA Descriptors

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3.3 Trigger Source and Trigger Modes

This section details PCIe-9834 triggering operations.

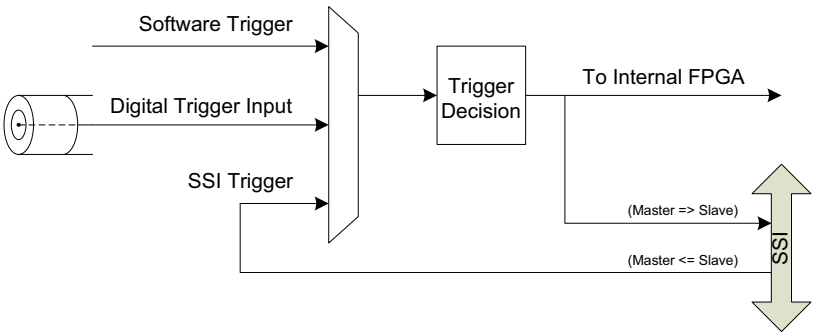


Figure 3-3: Trigger Architecture

The PCIe-9834 requires a trigger to implement acquisition of data. Configuration of triggers requires identification of trigger source. The PCIe-9834 supports internal software trigger, external digital trigger, and analog trigger.

3.3.1 Software Trigger

The software trigger, generated by software command, is asserted immediately following execution of specified function calls to begin the operation.

3.3.2 External Digital Trigger

An external digital trigger is generated when a TTL rising edge or falling edge is detected at the SMB connector TRG IN on the front panel. As shown, trigger polarity can be selected by software. Note that the signal level of the external digital trigger signal should be TTL compatible, and the minimum pulse width 20 ns.

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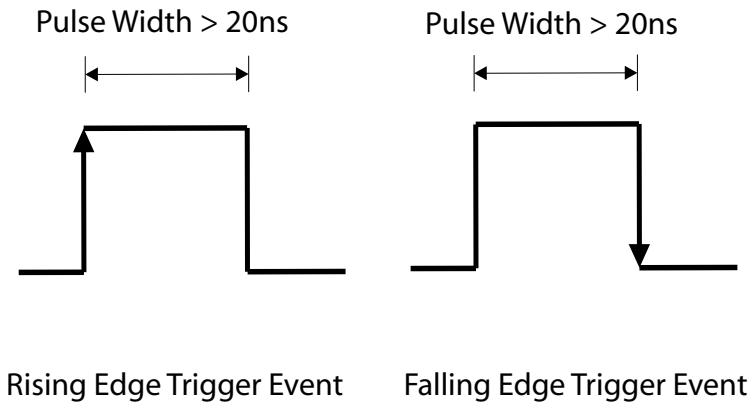


Figure 3-4: External Digital Trigger

3.3.3 Analog Trigger

An analog trigger is generated when AI input signal level is detected at the SMB connectors CH0 to CH3 (selected by software). The trigger level is also selected by software.

3.4 Trigger Modes

Trigger modes applied to trigger sources initiate different data acquisition timings when a trigger event occurs. The following trigger mode descriptions are applied to analog input function.

3.4.1 Post Trigger Mode

Post-trigger acquisition is applicable when data is to be collected after the trigger event, as shown. When the operation starts, PCIe-9834 waits for a trigger event. Once the trigger signal is received, acquisition begins. Data is generated from ADC and transferred to system memory continuously. The acquisition stops once the total data amount reaches a predefined value.

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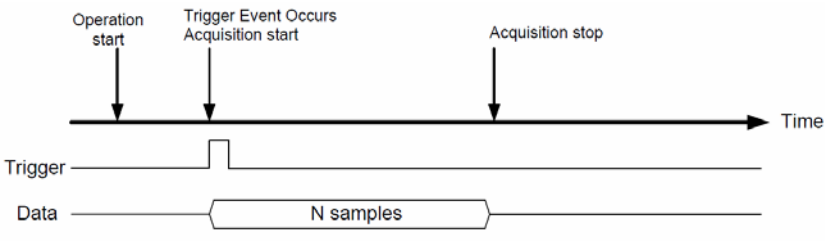


Figure 3-5: Post-Trigger Acquisition

3.4.2 Delayed Trigger Mode

Delayed-trigger acquisition is utilized to postpone data collection after the trigger event, as shown. When the PCIe-9834 receives a trigger event, a time delay is implemented before commencing acquisition. The delay is specified by a 16-bit counter value such that a maximum thereof is the period of TIMEBASE X (2^{16}), and the minimum is the Timebase period.

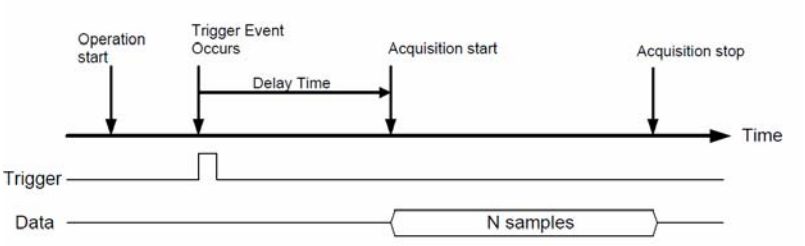


Figure 3-6: Delayed Trigger Mode Acquisition

3.4.3 Pre-Trigger Mode

Collects data before the trigger event, starting once specified function calls are executed to begin the pre-trigger operation, and stopping when the trigger event occurs. If the trigger event occurs after the specified amount of data has been acquired, the system stores only data preceding the trigger event by a specified amount, as follows.

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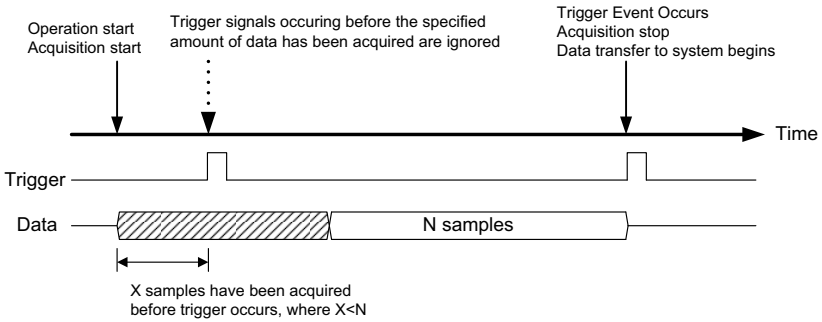


Figure 3-7: Pre-Trigger Mode Acquisition

3.4.4 Middle Trigger Mode

Collects data before and after the trigger event, with the amount to be collected set individually (M and N samples), as follows

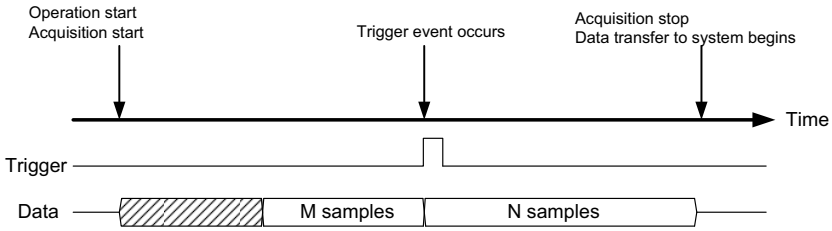


Figure 3-8: Middle Trigger Mode Acquisition

3.4.5 Acquisition with Re-Triggering

A digitizer acquires a trace of N samples/channel for a single acquisition. Re-Trigger mode can also be set to automatically acquire R traces, containing N*R samples/channel of data, without additional software intervention.

The Re-Trigger setting can be used for Post-Trigger and Delayed-Trigger modes, with different limitations on the spacing between

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trigger events in each mode. Trigger events arriving too close to the previous instance will be ignored by the digitizer.

- In Post-Trigger mode, the minimum spacing between trigger events is N+1
- In Delayed-Trigger mode, the minimum spacing between trigger events is (N+D)+1, where D is the number of the delayed setting

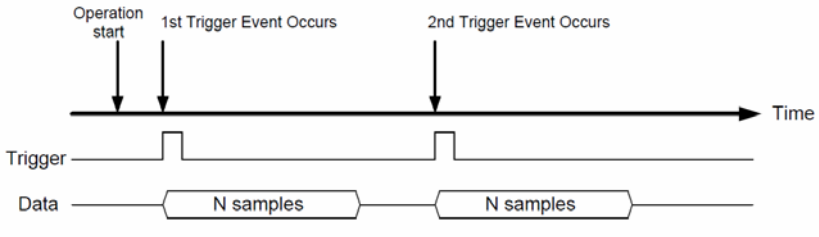


Figure 3-9: Re-Trigger Mode Acquisition

3.5 Timebase

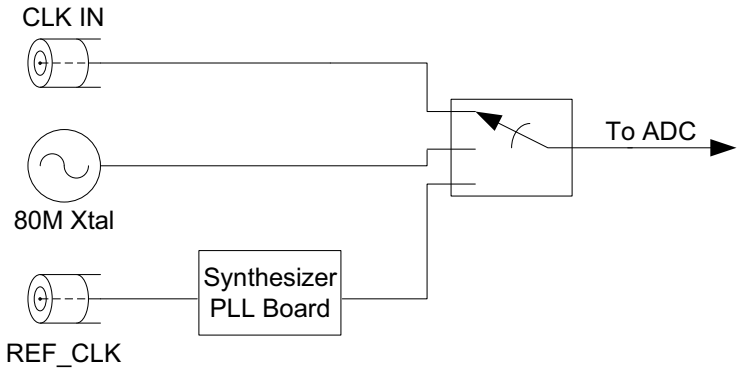


Figure 3-10: PCIe-9834 Clock Architecture

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3.5.1 Internal Sampling Clock

The PCIe-9834 internal 80MHz crystal oscillator acts as a sampling clock for ADC.

3.5.2 External Reference Clock (PCIe-9834P only)

The onboard PLL module allows REF_CLK to act as an external reference clock input, such that when multi-card synchronization for more than two modules is needed, a 10MHz clock source can be provided to REF_CLK and API function utilized to switch synthesizer input to the clock source at SMB connector REF_CLK, and generate a precise 80MHz clock for ADC. as the synthesizer's reference clock is the same for all modules, the generated 80MHz clock is synchronous.

3.5.3 External Sampling Clock

The PCIe-9834 can further choose an external clock source as ADC sampling clock. When an external sampling clock is selected, the ADC sampling frequency switches to the clock source at SMB Connector CLK IN, and clock source frequency is available from 20MHz to 80MHz. Be advised that if the frequency of the external sample clock is changed, the LVDS timebase requires recalibration.

To do so, call WD-DASK function: WD_AI_Config().

For more information, refer to the WD-DASK Function Library Reference.

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3.6 ADC Timing Control

3.6.1 Timebase Architecture

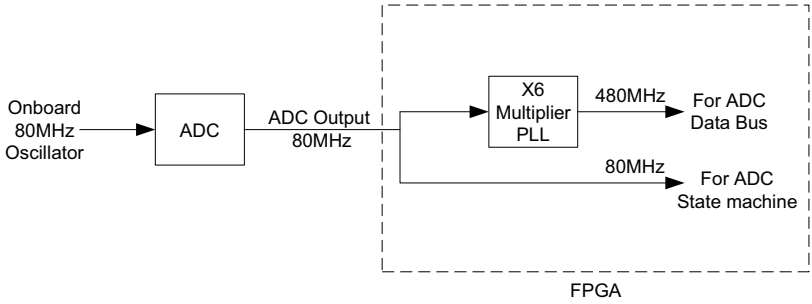


Figure 3-11: Timebase Architecture

3.6.2 Basic Acquisition Timing

The PCIe-9834 commences acquisition upon receipt of a trigger event originating with software command, external digital trigger. The Timebase is a clock provided to the ADC and acquisition engine for essential timing. The Timebase is from an onboard synthesizer. To achieve different sampling rates, a scan interval counter is used.

Using the post-trigger mode as an example, as shown, when a trigger is accepted by the digitizer, the acquisition engine commences acquisition of data from ADC, and stores the sampled data to the onboard FIFO. When FIFO is not empty, data will be transferred to system memory immediately through the DMA engine. The sampled data is generated continuously at the rising edge of Timebase according to the scan interval counter setting. When sampled data reaches a specified value, in this example 256, acquisition ends.

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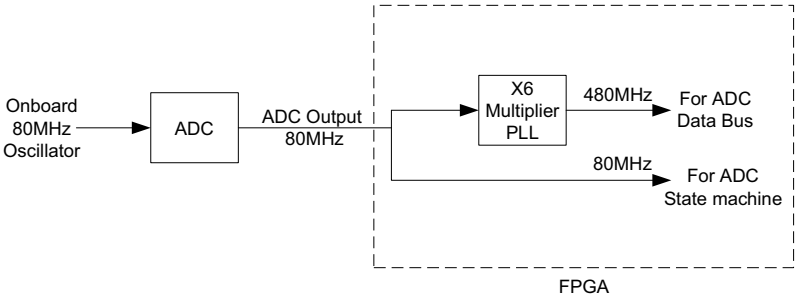


Figure 3-12: Basic Digitizer Acquisition Timing

To achieve sampling rates other than 80MS/s, a number for scan interval counter needs only be specified. For example, if the scan interval counter is set as 2, the equivalent sampling rate is 80MS/s / 2 = 40MS/s. If as 3, the equivalent sampling rate is 80MS/s / 3 = 26.66MS/s, and vice versa. The scan interval counter is 16 bits in width, therefore the lowest sampling rate is 1.221kS/s (80MS/s / 65535).

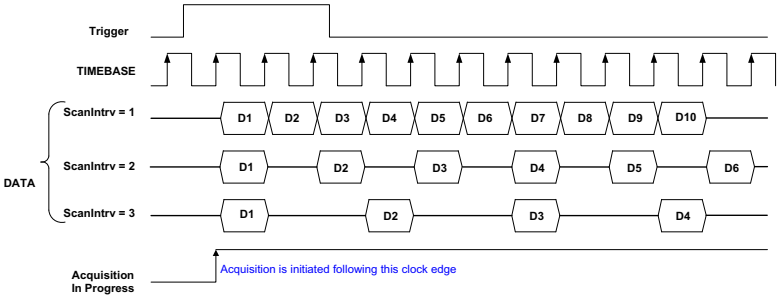


Figure 3-13: Varying Sampling Rates by Adjusting Scan Interval Counter

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Counter Name	Length	Valid Value	Description
ScanIntrv	16-bit	1-65535	Timebase divider to achieve equivalent sampling rate of the digitizer, where Sampling rate = Timebase / ScanIntrv
DataCnt	31-bit	1-2147483647	Specifies the amount of data to be acquired: 1 - 2147483648 for pre-trig or mid-trig mode operation
trigDelayTicks	16-bit	1 -65535	Indicates time between a trigger event and commencement of acquisition. The unit of a delay count is the period of the Timebase.
ReTrgCnt	31-bit	1-2147483647	Enables re-trigger to accept multiple triggers. 1 - 2147483647 for normal operation See Section 3.4.5: Acquisition with Re-Triggering

Table 3-4: Counter Parameters and Description

3.7 Synchronizing Multiple Modules

The PCIe-9834 provides a dedicated connector as system synchronization interface, enabling multiple module synchronization. As shown, bi-directional SSI I/Os provides a flexible connection between modules, allowing one SSI master PCIe-9834 to output SSI trigger signals to other slave modules.For more accurate synchronization between modules, external sampling clock or external reference clock should be applied.

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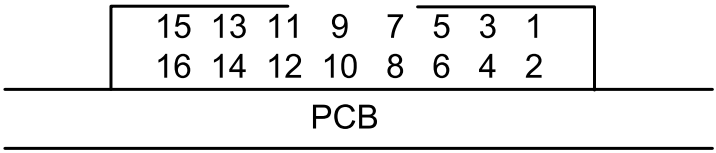
The table summarizes SSI functionalities.

NOTE:

Different signals cannot be routed onto the same trigger bus line.

SSI Timing Signal	Function
SSI Trig	Input/output trigger signal through SSI

All SSI signals are routed to the 16-pin connector from FPGA, enabling multi-module synchronization. ACL-eSSI-2/ACLeSSI-3/ ACL-eSSI-4 cables can be used to synchronize 2, 3, or 4 modules.



Signal	Direction	Descr.	Pin
SSI Trig	Input/Output	Trigger signal through SSI	1, 9, 11, 13, 15
GND		Ground	2, 4, 6, 8, 10, 12, 14, 16
Reserved	Input/Output	Reserved for future use	3, 5,7

Table 3-5: SSI Signal Location and Pin Definition

3.7.1 Card Number Configuration

When multiple cards are used in a single chassis, card number configuration via switch, as shown.

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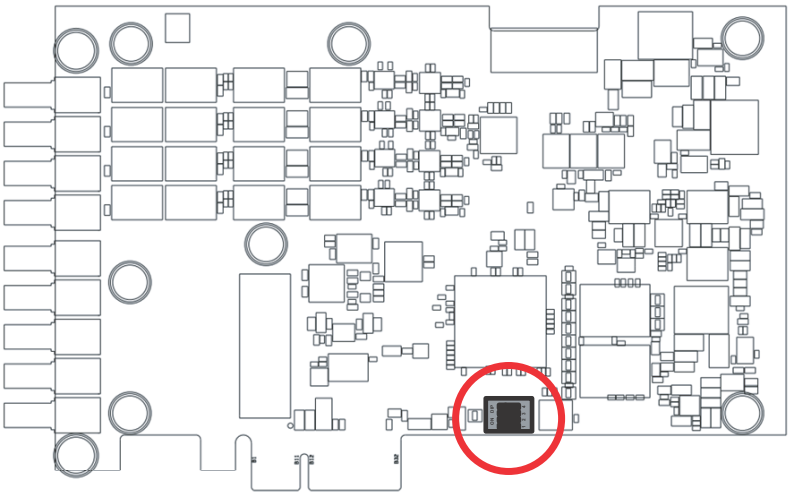


Figure 3-14: Card Number Configuration Switch

When all sliders are in ON position, card number is 15, when all are OFF, card number is 0, as shown.

Slider 1	Slider 2	Slider 3	Slider 4	Card #
OFF	OFF	OFF	OFF	0
OFF	OFF	OFF	ON	1
OFF	OFF	ON	OFF	2
OFF	OFF	ON	ON	3
OFF	ON	OFF	OFF	4
OFF	ON	OFF	ON	5
OFF	ON	ON	OFF	6
OFF	ON	ON	ON	7
ON	OFF	OFF	OFF	8

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Slider 1	Slider 2	Slider 3	Slider 4	Card #
ON	OFF	OFF	ON	9
ON	OFF	ON	OFF	10
ON	OFF	ON	ON	11
ON	ON	OFF	OFF	12
ON	ON	OFF	ON	13
ON	ON	ON	OFF	14
ON	ON	ON	ON	15

Table 3-6: Card Number Configuration Settings

Default card number is 15.

3.7.2 SSI_TRIG

As an output, the SSI_TRIG signal reflects the trigger event signal in an acquisition sequence. As an input, the PCIe-9834 accepts the SSI_TRIG signal to be the trigger event source. The signal is configured in the rising edge-detection mode.

3.8 Multi-boot

The PCIe-9834 supports software-based firmware updates. If firmware updates fail, the system may be unable to recognize the module, in which case the following steps may solve the problem.

1. Config SW2 to "on"
2. Install the module and restart the system
3. If the module is recognized, update firmware again (ensure the firmware you updated is workable)
4. Turn off the system, config SW2 to "off" and restart the system.

The default state of SW2 is "off".

If the problem remains, please contact FAE.

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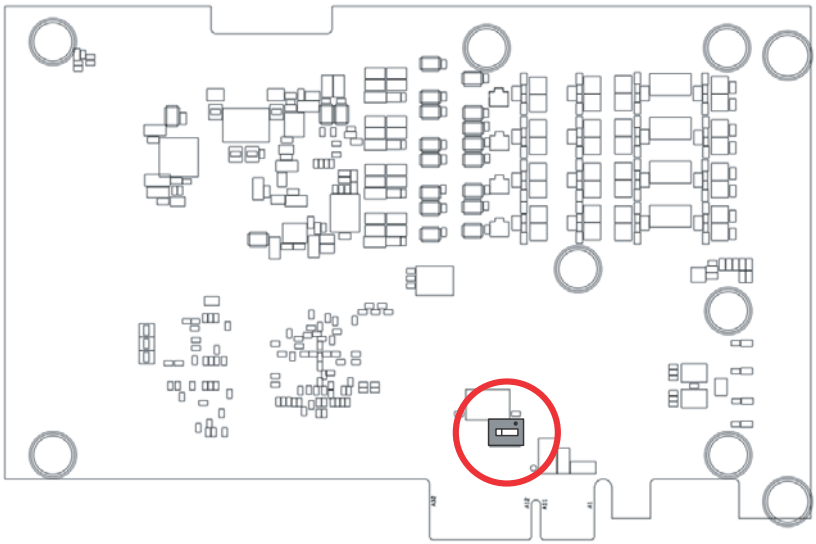


Figure 3-15: Flash Memory Configuration Switch

3.9 Measurement Function API

The PCIe-9834 supports measurement function APIs for easily conversion of basic voltage/time measurement results, with no extra programming required for development of scoping application software.

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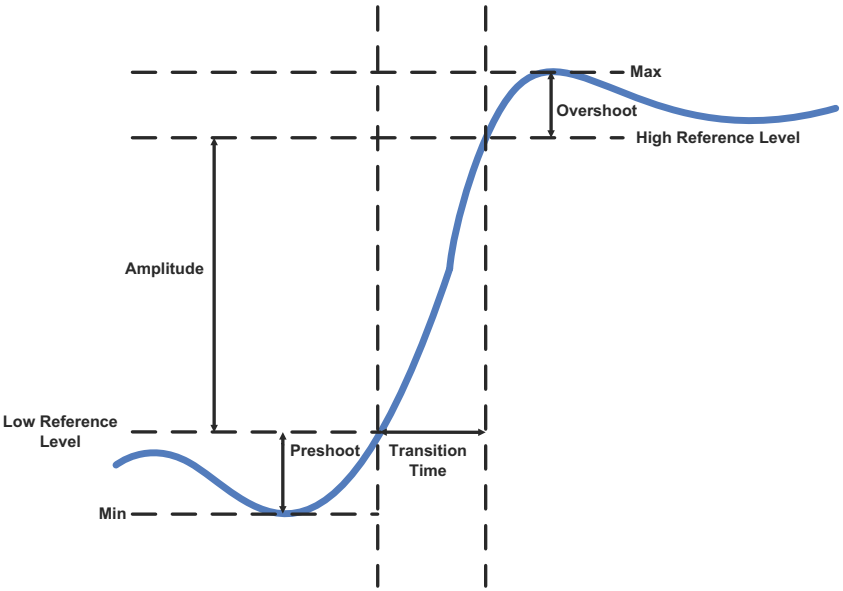


Figure 3-16: Waveform Transition

Parameter	Descr.	Comments	Type	Unit
max	Highest waveform value	Refer to Figure 3-16, “Waveform Transition”	Double	V
min	Lowest waveform value	Refer to Figure 3-16, “Waveform Transition”	Double	V
mean	Arithmetic average value of the waveform	$(\sum \text{Waveform [i]})/n$	Double	V
p2p	Peak to peak	max - min	Double	V
std	Standard deviation	$\sqrt{(\sum \text{Waveform [i]}-M^2) / (n-1)}$	Double	
rms	Root/mean/ square	$\sqrt{\sum \text{Waveform [i]}^2/n}$	Double	

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Parameter	Descr.	Comments	Type	Unit
period	Duration of one complete waveform cycle, calculated in WD-DASK via the interval between first and third mid reference level crossings		Double	Sec
freq	Reciprocal of period	1 / period	Double	Hz
negwidth	Negative pulse width, the duration between two consecutive mid reference level points of a negative waveform pulse		Double	Sec
poswidth	Positive pulse width, the duration between two consecutive mid reference level points of a positive waveform pulse		Double	Sec
negdutycycle	Negative pulse width/waveform period ratio	(negwidth/period) *100%	Double	
posdutycycle	Positive pulse width/waveform period ratio	(poswidth/period) *100%	Double	
risetime	Duration of signal rising from low to high reference level	Refer to Figure 3-16, “Waveform Transition”	Double	Sec

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Parameter	Descr.	Comments	Type	Unit
falltime	Duration of signal falling from high to low reference level	Refer to Figure 3-16, “Waveform Transition”	Double	Sec
high	Voltage high, calculated via histogram, using the voltage of the histogram bin with the maximum number of hits above 60% of the peak-to-peak value of the waveform	high->value	wd_hist_bin	V
low	Voltage low, calculated via histogram, using the voltage of the histogram bin with the maximum number of hits below 40% of the peak-to-peak value of the waveform	low->value	wd_hist_bin	V
ampl	Amplitude, difference between voltage high and voltage low	vol_high – vol_low Refer to	Double	V
pospreshoot	Peak distortion preceding a valid positive transition	((voltage low – local min)/ amplitude)*100%	Double	

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Parameter	Descr.	Comments	Type	Unit
posovershoot	Peak distortion following a valid positive transition	((local max – voltage high)/ amplitude)*100%	Double	
negpreshoot	Peak distortion preceding a valid negative transition	((local max – voltage high)/ amplitude)*100%	Double	
negovershoot	Peak distortion following a valid negative transition	((voltage low – local min)/ amplitude)*100%	Double	
cyclemean	Arithmetic average of integral number of points in one period	(∑Waveform [i]/(points/period)	Double	V
cyclerms	Rms of integral number of points in one period	$\sqrt{\sum}$Waveform [i] ^{2}/(points/period)	Double	
fft_ampl	FFT amplitude		Double	V/ rms
fft_freq	FFT frequency		Double	Hz

Table 3-7: Measurement Parameters

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Appendix A Calibration

This chapter introduces the calibration process to minimize analog input measurement errors.

A.1 Calibration Constant

The PCIe-9834 is factory calibrated before shipment, with associated calibration constants written to the onboard EEPROM. At system boot, the PCIe-9834 driver loads these calibration constants, such that analog input path errors are minimized. ADLINK provides a software API for calibrating the PCIe-9834.

The onboard EEPROM provides two banks for calibration constant storage. Bank 0, the default bank, records the factory calibrated constants, providing written protection preventing erroneous auto-calibration. Bank 1 is user-defined space, provided for storage of self-calibration constants. Upon execution of auto-calibration, the calibration constants are recorded to Bank 1.

When PCIe-9834 boots, the driver accesses the calibration constants and is automatically set to hardware. In the absence of user assignment, the driver loads constants stored in bank 0. If constants from Bank 1 are to be loaded, the preferred bank can be designated as boot bank by software. Following re-assignment of the bank, the driver will load the desired constants on system reboot. This setting is recorded to EEPROM and is retained until reconfiguration.

A.2 Auto-Calibration

Because errors in measurement and outputs will vary with time and temperature, re-calibration is recommended when the module is installed. Auto-calibration can measure and minimize errors without external signal connections, reference voltages, or measurement devices.

The PCIe-9834 has an on-board calibration reference to ensure the accuracy of auto-calibration. The reference voltage is measured on the production line and recorded in the on-board EEPROM.

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Before initializing auto-calibration, it is recommended to warm up the PCIe-9834 for at least 20 minutes and remove connected cables.

NOTE:

It is not necessary to manually factor delay into applications, as the PCIe-9834 driver automatically adds the compensation time.

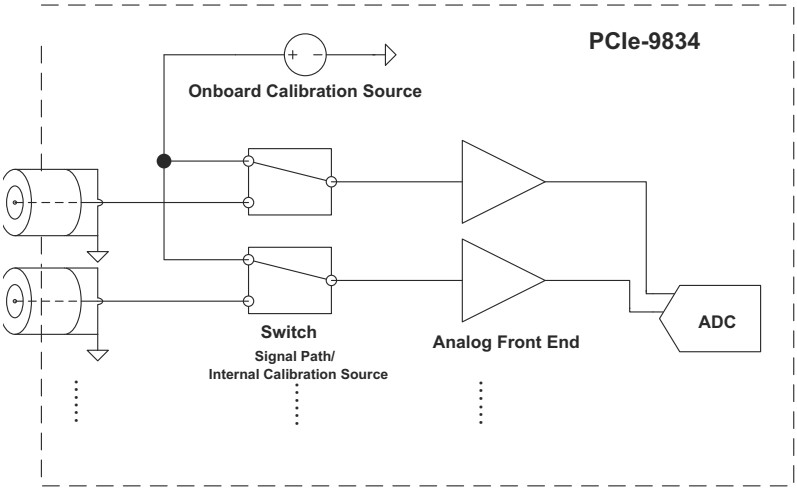


Figure A-1: Auto-Calibration Block Diagram

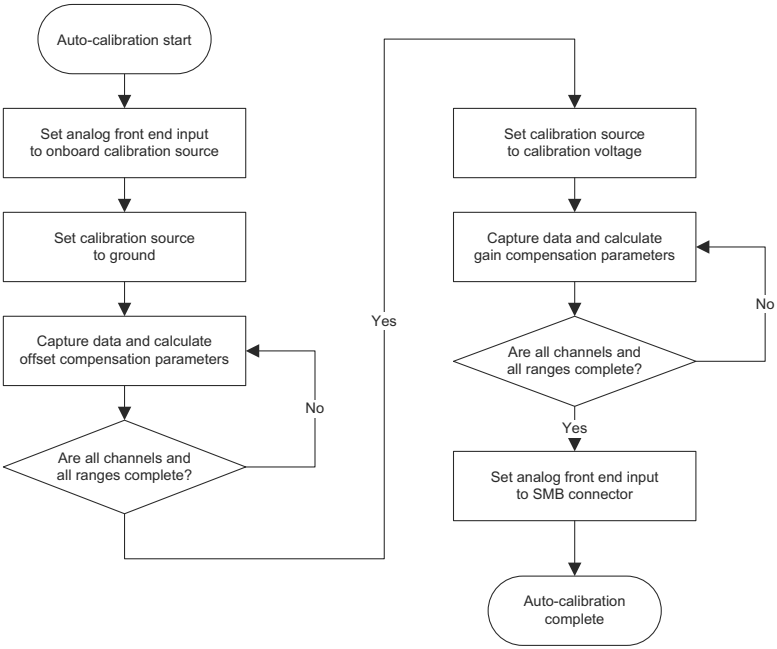


Figure A-2: Auto-Calibration Flow

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Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

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- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.
- A Lithium-type battery may be provided for uninterrupted, backup or emergency power.



Risk of explosion if battery is replaced with an incorrect type; please dispose of used batteries appropriately.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

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