

Smart Mobility Architecture Design Guide

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1 INTRODUCTION

1.1 General Introduction

SMARC ("Smart Mobility Architecture") is an open – source computer Module standard maintained by the SGeT ("Standardization Group for Embedded Technologies"). SMARC Modules are small form factor (82mm x 50mm and 82mm x 80mm), low power (typically <6W) computer modules that are used on a Carrier board that utilizes a 314 pin 0.5mm pitch right-angle memory socket style connector to host the Module. SMARC Modules may utilize ARM, low power RISC or low power x86 CPUs / SOCs.

The SMARC Modules are specified in the SGeT ***Smart Mobility Architecture Hardware Specification***. The specification document is available free of charge from the SGET web site (**www.sget.org**), subject to their terms of use.

Similarly, this ***SMARC Design Guide*** is available free of charge from the SGET web site, subject to the SGET terms of use.

1.2 Purpose of This Document

The primary purpose of this document is to serve as a Design Guide for developers of SMARC Carrier Boards and for SMARC Module customers who wish to have a SMARC based system developed.

A secondary purpose of this document is to serve as a reference to SMARC Module developers, to help them understand the application of the Modules they are developing.

Finally, this document should be valuable to FAEs and Product managers to help them understand the SMARC infrastructure.

1.3 Design Help

There are a number of ways to have a SMARC Carrier board developed:

- Design internally, but have your SMARC Module vendor review your design. Make sure to also have the appropriate semiconductor companies review the portions of the design that utilize their components.
- Use a 3rd party firm that specializes in SMARC Carrier development. Such resources may be listed on the SGET web page (**www.sget.org**).
- Contact your SMARC Module vendor. The Module vendor will have an FAE available for advice. Many vendors will also undertake custom Carrier design projects, for significant opportunities.

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1.4 Abbreviations and Acronyms Used

ADC	Analog to Digital Converter	
AFB	Alternate Function Block (from SMARC spec)	
ARM	Advanced RISC Machines	**www.arm.com**
BCT	Boot Configuration Table	
BSP	(software) Board Support Package	
CAD	Computer Aided Design	
CAN	Controller Area Network	
CPLD	Complex Programmable Logic Device	
CODEC	Coder – Decoder	
CSI	Camera Serial Interface	**www.mipi.org**
DAC	Digital to Analog Converter	
DB-9	Connector, D shaped, B shell size, 9 pins	
DE	Differential Ended (signal pair)	
DNI	Do Not Install (component is not loaded)	
DSP	Digital Signal Processor	
EDID	Extended Display Identification Data	**www.vesa.org**
EEPROM	Electrically Erasable Programmable Read Only Memory	
eMMC	Embedded Multi Media Card	**www.jedec.org**
ESD	Electro Static Discharge	
FET	Field Effect Transistor	
FIFO	First In First Out (buffer memory)	
FS	Full Speed (USB 2.0 12 Mbps)	
GBE	Gigabit Ethernet	**www.ieee.org**
Gbps	Giga bits per second	
GPIO	General Purpose Input / Output	
HDA	High Definition Audio – Intel defined format	**www.intel.com**
HDMI	High Definition Multimedia Interface	**www.hdmi.org**
HID	Human Interface Device: USB device class	
HS	High Speed (USB 2.0 480 Mbps)	
IC	Integrated Circuit	
I2C	Inter-Integrated Circuit	**www.nxp.com**
I2S	Inter-Integrated Circuit – Sound	**www.nxp.com**
IEEE	Institute of Electrical and Electronics Engineers	**www.ieee.org**
iMX6	Popular ARM SOC from Freescale Semiconductor	**www.freescale.com**
IO	Input Output	
ISO	International Organization for Standardization (French)	**www.iso.org**
JEDEC	Joint Electron Device Engineering Council	**www.jedec.org**
JPEG	Joint Photographic Experts Group	**www.jpeg.org**
LED	Light Emitting Diode	
Li-Ion	Lithium Ion (rechargeable battery technology)	
LVDS	Low Voltage Differential Signaling	
M2.5	Metric 2.5mm	
M3	Metric 3.0mm	
MAC	Media Access Controller (e.g. logic circuits in GBE)	
Mbps	Mega bits per second	
MIPI	Mobile Industry Processor Interface	**www.mipi.org**
MLC	Multi Level Cell (flash memory reference)	
MOD	Module (the SMARC Module) (schematic notation)	
MO-297	Module Outline 297 (“Slim SATA” format)	**www.jedec.org**
MO-300	Module Outline 300 (mini-PCIe Express card format)	**www.jedec.org**
MPEG	Motion Picture Experts Group	**www.mpeg.org**
MXM	Mobile pci eXpress Module	**www.mxm-sig.org**

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MXM3	MXM Revision 3	
NAND	A high density flash memory technology	
nS	Nano second (10 E -9)	
NC	Not Connected	
NXP	A semiconductor company	**www.nxp.com**
OS	Operating System	
OTG	On the Go (USB term – device can be host or client)	
PCB	Printed Circuit Board	
PHY	Physical (transceiver) – drives cable	
PICMG	PCI Industrial Computer Manufacturing Group	**www.picmg.org**
PCI	Peripheral Component Interface	**www.pcisig.org**
PCIe	PCI Express	**www.pcisig.org**
PCI-SIG	PCI Special Interest Group	**www.pcisig.org**
PCM	Pulse-Code Modulation	
PLL	Phase Locked Loop	
POE	Power Over Ethernet	
pS	Pico second (10 E -12)	
PWM	Pulse Width Modulation	
RGB	Video data in Red Green Blue pixel format	
RISC	Reduced Instruction Set Computing	
ROM	Read Only Memory	
RS232	Recommend Standard 232 (asynch serial ports)	
RS485	Asynchronous serial data, differential, multidrop	
RTC	Real Time Clock (battery backed clock and memory)	
SAR	Successive Approximation Register	
SATA	Serial ATA (serial mass storage interface)	**www.sata-io.org**
SD	Secure Digital (memory card)	
SE	Single Ended (signal, as opposed to differential)	
SGeT	Standardization Group for Embedded Technologies	**www.sget.org**
SLC	Single Level Cell (flash memory reference)	
SMARC	Smart Mobility Architecture	**www.sget.org**
SMSC	A semiconductor company	**www.smsc.com**
SOC	System On Chip	
S/PDIF	Sony/Philips Digital Interconnect Format	
SPI	Serial Peripheral Interface	
SSD	Solid State Disk	
TI	Texas Instruments – semiconductor company	**www.ti.com**
TIM	Thermal Interface Material	
UART	Universal Asynchronous Receiver Transmitter	
UL	Underwriters Laboratories	**www.ul.com**
USB	Universal Serial Bus	**www.usb.org**
VESA	Video Electronics Standards Association	**www.vesa.org**
WEC7	Windows Embedded Compact 7 (an OS)	
YUV	Video data format, more common in television	
X5R	Ceramic capacitor dielectric – good quality	
X7R	Ceramic capacitor dielectric – best quality	
X86	Intel architecture (80x86) CPUs	

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1.5 Document References

1.5.1 SGET Documents

- ***Smart Mobility Architecture Hardware Specification***, V 1.0, December 20, 2012 © SGET (Standardization Group For Embedded Technologies) **www.sget.org**

1.5.2 Industry Standards Documents

- ***CAN ("Controller Area Network")*** Bus Standards – ISO 11898, ISO 11992, SAE J2411.
- ***CSI-2 (Camera Serial Interface version 2)*** The CSI-2 standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Interface Alliance") (**www.mipi.org**).
- ***eMMC ("Embedded Multi-Media Card")*** the eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (**www.jedec.org**).
- ***GBE MDI ("Gigabit Ethernet Medium Dependent Interface")*** defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling defined by IEEE 802.3ab (**www.ieee.org**).
- ***HDMI Specification***, Version 1.3a, November 10, 2006 © Hitachi and other companies (**www.hdmi.org**).
- ***The I2C Specification,*** Version 2.1, January 2000, Philips Semiconductor (now NXP) (**www.nxp.com**).
- ***I2S Bus Specification,*** Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (**www.nxp.com**).
- ***JEDEC MO-300 (mSATA)*** defines the physical form factor of the mSATA format (**www.jedec.org**). The electrical connections are defined in the Serial ATA document.
- ***MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification***, Version 3.0, Revision 1.1, © 2009 NVidia Corporation (**www.mxm-sig.org**).
- ***PICMG® EEEP Embedded EEPROM Specification,*** Rev. 1.0, August 2010 (**www.picmg.org**).
- ***PCI Express Specifications*** (**www.pci-sig.org**).
- ***PCI Express Mini Card Electromechanical Specification Revision 2.0,*** April 21, 2012, © PCI-SIG (**www.pci-sig.org**).
- ***RS-232*** (EIA "Recommended Standard 232") this standard for asynchronous serial port data exchange dates from 1962. The original standard is hard to find. Many good descriptions of the standard can be found on-line, e.g. at Wikipedia, and in text books.
- ***Serial ATA Revision 3.1***, July 18, 2011, Gold Revision, © Serial ATA International Organization (**www.sata-io.org**).
- ***SD Specifications Part 1 Physical Layer Simplified Specification,*** Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association ("Secure Digital") (**www.sdcard.org**).
- ***SPDIF (aka S/PDIF)*** ("Sony Philips Digital Interconnect Format) - IEC 60958-3.
- ***SPI Bus –*** "Serial Peripheral Interface" – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (**http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus**).
- ***UL 1642 Lithium Batteries –*** safety standard governing the use of lithium batteries (**www.ul.com**)
- ***USB Specifications*** (**www.usb.org**).
- ***VESA Enhanced Extended Display Identification Data Standard,*** Rev. 1, Feb 9, 2000, VESA (**www.vesa.org**) See also the "EDID" page in Wikipedia.

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1.6 Schematic Example Correctness

The schematic examples shown in this Design Guide are believed to be correct but correctness can not be guaranteed. Most of the examples have been pulled from designs that have been built, tested, and are known to work. Most of them have been re-formatted to fit better in this design guide.

1.7 Software Support

Many hardware examples and suggestions are given in the following pages. SMARC Carrier hardware design is generally straightforward. However, before committing to a particular hardware selection, it is wise to check out the software driver support. A particular device may be supported in, say, for example, Linux but not in Windows Embedded Compact 7. Your overall project may go smoother if you pick out hardware that already has software support in your target OS.

There are various possible sources for software drivers for a particular IC: the IC vendor, the OS vendor, the OS community, your Module vendor, your Carrier design partner, other independent sources and of course writing your own..

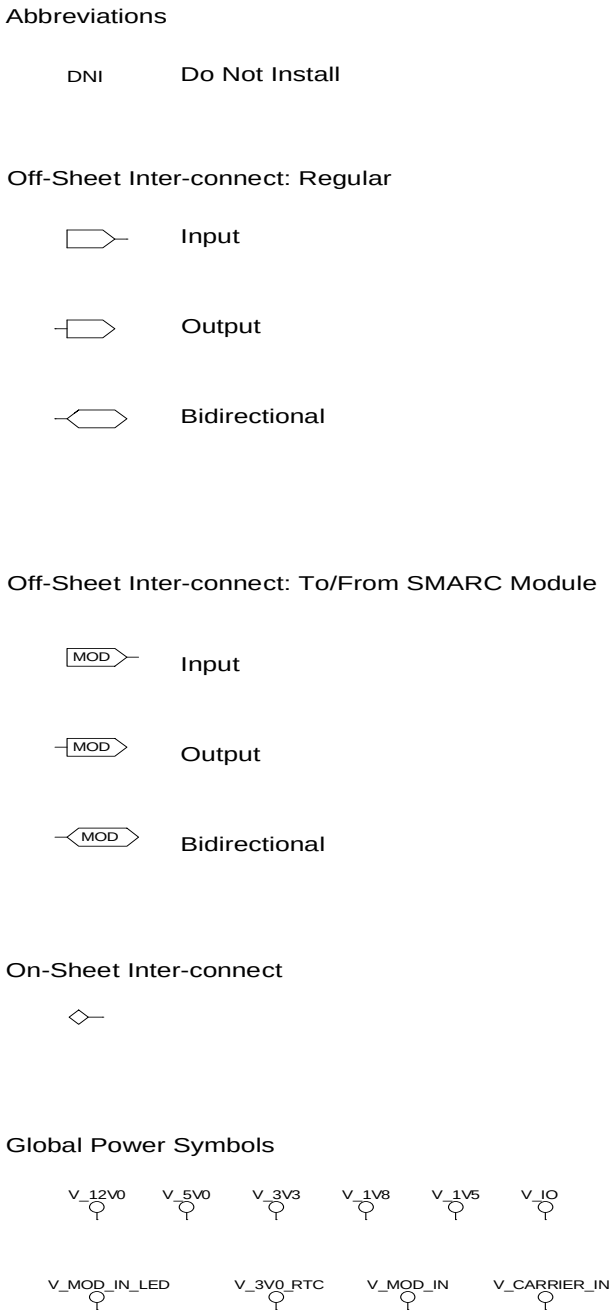
Most SMARC Module vendors offer a BSP (Board Support Package) for their Module. Your target Carrier device may be supported in the BSP – check this angle out as well.

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1.8 Schematic Example Conventions

Some of the conventions used in the schematic examples are described below. Note off-page connections that tie directly to the SMARC Module have the notation “MOD” in the off-page connect symbol.

Figure 1 Schematic Symbol Conventions



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Table 1 Schematic Power Net Naming

V_IN_RAW	Power in to the overall system, before any filtering, fusing, polarity or rise time protection
V_IN	Power in to the overall system, after (optional) filtering, fusing, polarity or rise time protection
V_MOD_IN	Power into the SMARC Module. It must be within the 3.0V to 5.25V range defined by the SMARC specification
V_CARRIER_IN	Power in to the Carrier Board. It may be the same as V_MOD_IN, depending on the design at hand. On SMARC Evaluation Carrier boards, V_CARRIER_IN is sometimes kept separate from V_MOD_IN to allow easier measurements and tracking of where the power goes.
V_5V0	5V supply on the Carrier Board
V_3V3	3.3V supply on the Carrier Board
V_1V8	1.8V supply on the Carrier Board
V_1V5	1.5V supply on the Carrier Board
V_IO	Supply voltage on the Carrier Board for Module I/O interfaces. For most SMARC systems, V_IO is 1.8V and the V_IO and V_1V8 may be the same supply. For V_IO of 1.8V, the Carrier Board should tie Module VDD_IO_SEL# pin (pin S158) to GND
V_3V0_RTC	Supply voltage from the Carrier Board to the SMARC VDD_RTC pin (pin S147) This is a low voltage, low current supply separate from V_MOD_IN, used to supply the Module RTC (Real Time Clock) in the absence of V_MOD_IN.
V_MOD_IN_LED	Same as V_MOD_IN except isolated by a series jumper – used for power status LEDs – jumper can be removed to prevent status LEDs from consuming power

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2 INFRASTRUCTURE: CONNECTOR, POWER DELIVERY, SYSTEM MANAGEMENT

2.1 Module Connector

The SMARC Module connector is well described in the ***Smart Mobility Architecture Hardware Specification*** and the complete description is not repeated here.

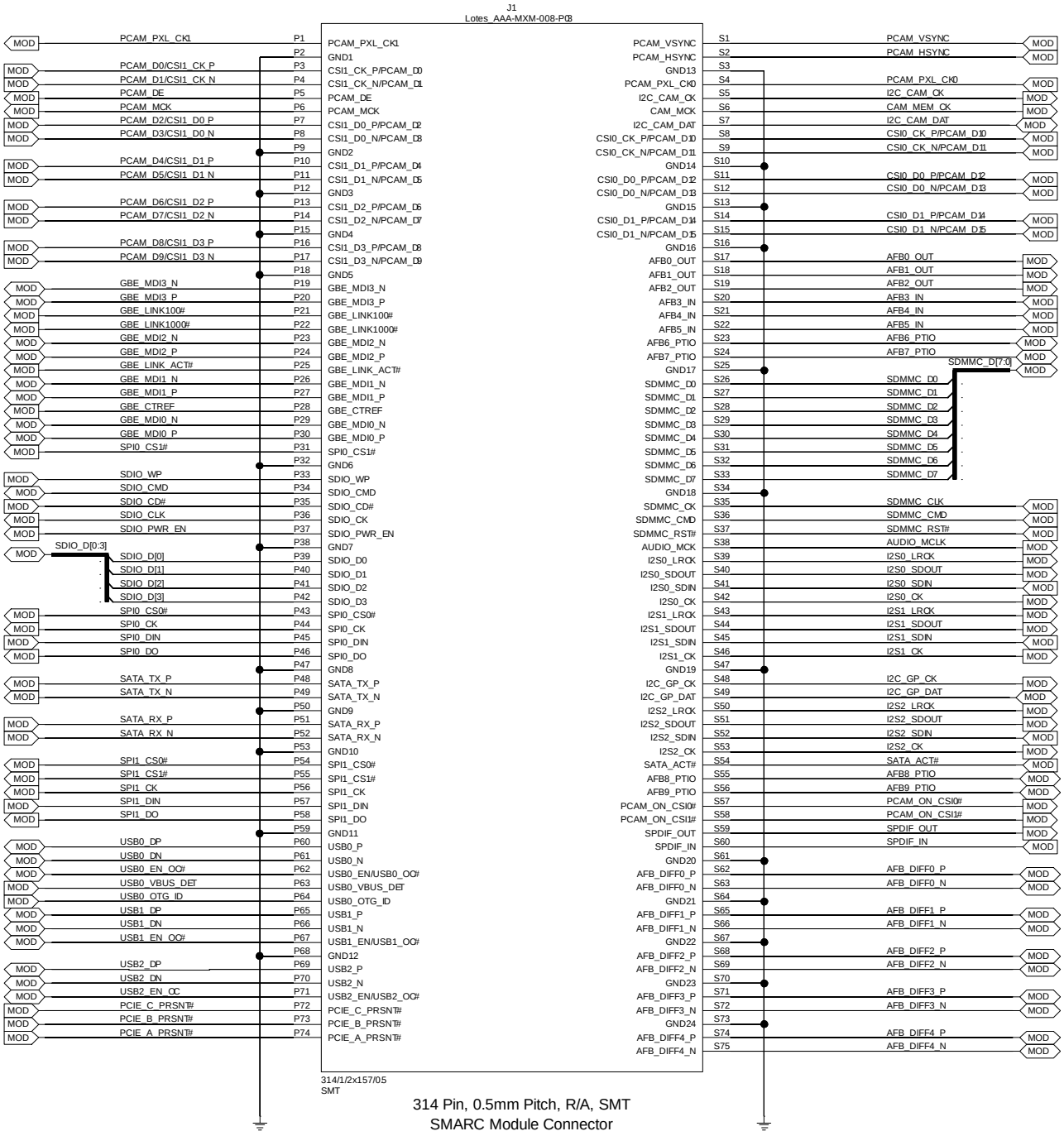
Briefly, the SMARC Module connector is a low profile, right angle 314 pin memory – socket style connector. The same connector is commonly used for MXM3 graphics cards. However, it is important to understand that the SMARC usage and pin-out of this connector is totally different from the MXM3 case.

The SMARC Module connector is available from multiple sources, including at least one vendor that has qualified their offering for automotive use.

Various height profiles are available for the SMARC Module connector. The lowest profile available has a Carrier Board PCB top-side to Module PCB bottom-side separation of 1.5mm, and a connector body height of 4.6mm.

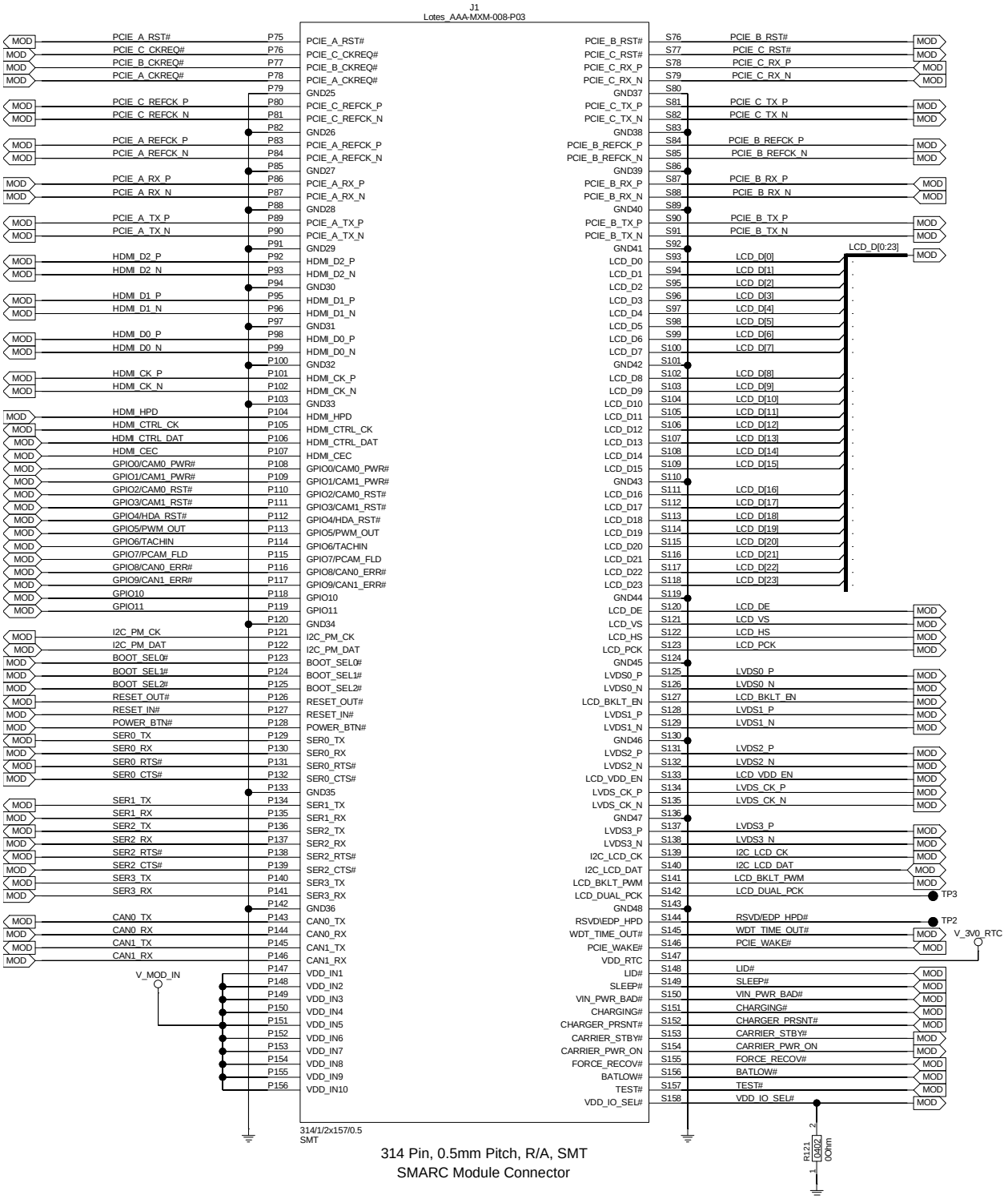
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Figure 2 Module Connector Pins P1-74 and S1-75



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Figure 3 Module Connector Pins P75-156 and S76-158



314 Pin, 0.5mm Pitch, R/A, SMT
SMARC Module Connector

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2.2 Module Power

2.2.1 Input Voltage Range

Per the SMARC Module HW specification, the SMARC Modules may accept input power over the voltage range 3.0V to 5.25V. This range coincides with the range of a single-level lithium – ion cells and allows the use of common 5V or 3.3V fixed DC supplies.

2.2.2 Input Voltage Rise Time

There are currently no limits in the SMARC Module HW Specification on the Module power supply rise times. In general, it is not wise to expose the Module and Carrier electronics to extremely fast power supply rise times (as may be the case if a low impedance power source such as a battery pack or power brick is “hot-plugged”). Input power supply rise times faster than 50V / millisecond to the Module should be avoided. If a unit is to be “hot-plugged” to a low impedance power source, then the Carrier should implement measures to slow the power rise time as seen by the Module and Carrier circuits. The Carrier can do this by implementing a FET and hot-swap controller in the input power path. This is discussed in ***Section 10.5 Power Hot Swap Controller.***

2.2.3 Module Maximum Input Power

The SMARC V1.0 specification document states that the allowable input voltage range is 3.0V to 5.25V. The rationale for this is that this range coincides with the voltage range of single level lithium-ion cells, and that it also allows the use of common 5V or 3.3V bench supplies. However, it is not clear in the V1.0 specification that Modules are required to work at the lower end (3.0V) of this range.

The SMARC Module physical connector is a MXM3 connector (although the pinout is completely different). The MXM3 specification document requires that the MXM3 connector pins be able to carry 0.5A current minimum. SMARC Modules allocate 10 pins for input power (and 48 GND pins for signal and power return). Thus, per the MXM3 connector requirement, the 10 pins should be capable of handling 5A. This allows a maximum power input range of 15W (for 3.0V power in) to 26.5W (for 5.25V power in).

For conservative design, let us operate the MXM3 connector pins at no more than 70% of their capacity. Then the following maximum power inputs are achieved:

10 pins * 0.5A * 70% * 3.0V = 10.5W (low end of Li-Ion battery)

10 pins * 0.5A * 70% * 4.75V = 16.6W (low end of 5V bench supply)

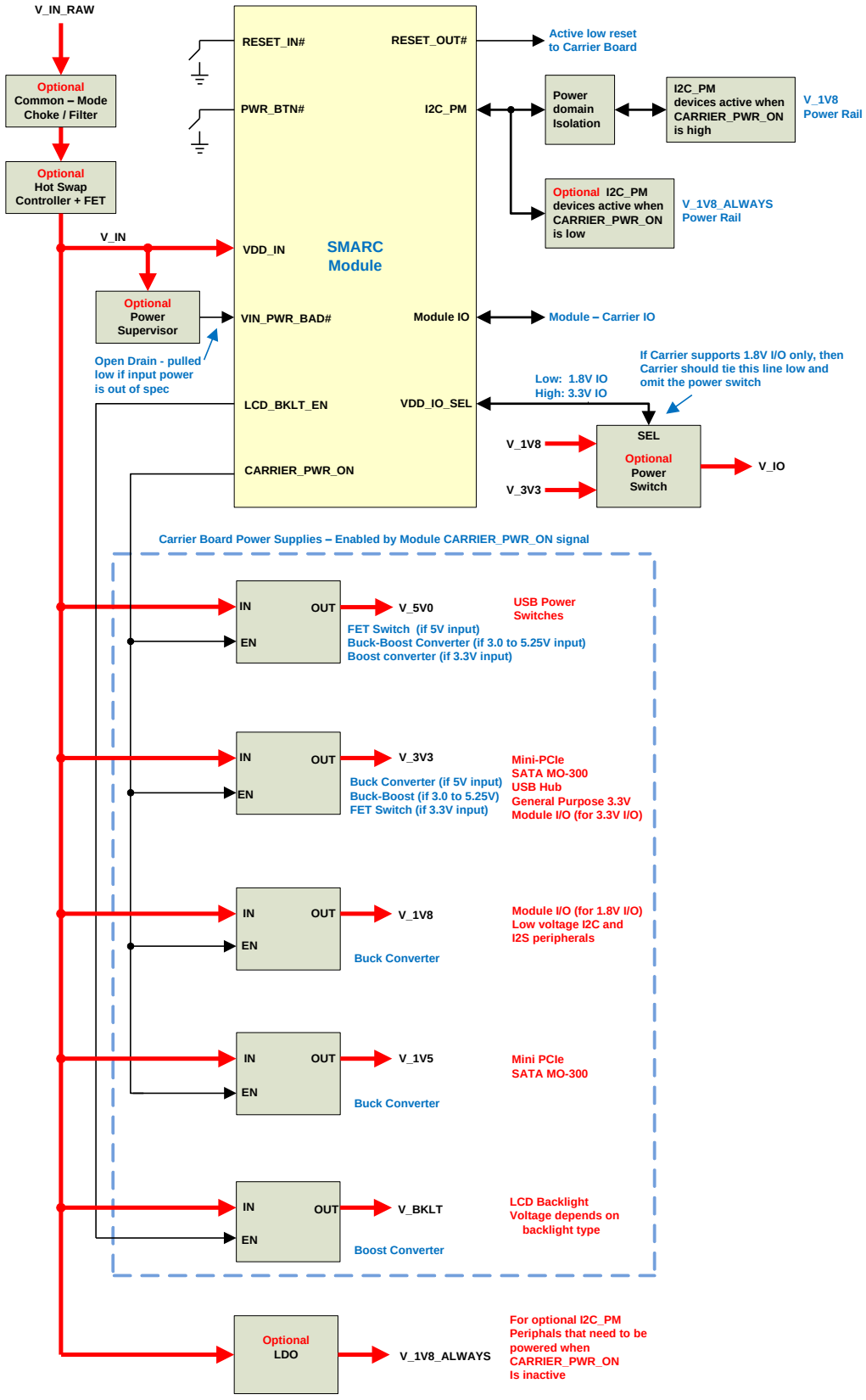
These numbers apply to the Module only, and not to the Carrier circuits. The 10.5W is adequate for low power Modules that are to be served by single level Lithium-Ion cells. The 16.6W should be adequate for higher power Modules (Including Intel Bay Trail designs) operating from a 5V supply.

2.2.4 Power Path

The power path for a basic, fixed input voltage arrangement SMARC Module and Carrier board system is shown in ***Figure 4 Basic Module and Carrier Power Path*** below. A number of features in the figure are optional and may be omitted (and bypassed) in a minimal implementation. The figure also shows Carrier Board power supply sections assuming a typical system powered by a power source in the 3.0V to 5.25V range.

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Figure 4 Basic Module and Carrier Power Path



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2.3 Module I/O Voltage

The SMARC Module HW Specification encourages the use of 1.8V Module I/O, although it allows for 1.8V or 3.3V options. A Module pin, VDD_IO_SEL# (S158), signals both the Module and the Carrier I/O voltage expectation.

I/O at 1.8V is preferred in general for low power interfaces. Recall that the power expended to charge and discharge a capacitor (i.e. the I/O pin and trace capacitance) is proportional to the square of the I/O voltage: **½ C V^2f** where **C** is the node capacitance, **V** the I/O voltage, and **f** the frequency of the I/O charging / discharging.

Many contemporary peripherals of interest are available with I/O interfaces that support 1.8V and 3.3V; some are available at 1.8V only, and others at 3.3V only. Specific examples are given in various document sections below.

2.3.1 I/O at 1.8V (Default)

The Carrier should tie VDD_IO_SEL# to GND if the Module – Carrier I/O interfaces are to run at 1.8V, as most SMARC modules do.

A Module that supports 1.8V I/O only has the VDD_IO_SEL# pin tied hard to GND on the Module.

A Module that supports 1.8V and 3.3V I/O has a 100K pull-up on VDD_IO_SEL# on the Module to VDD_IN. The Module senses the VDD_IO_SEL# pin to determine whether the Carrier expects 1.8V or 3.3V I/O. If a low value is sensed, the Module uses 1.8V I/O.

2.3.2 I/O at 3.3V

A Module that supports 3.3V I/O has a 100K pull-up on the Module on VDD_IO_SEL# to VDD_IN. The Module senses the VDD_IO_SEL# pin to determine whether the Carrier expects 1.8V or 3.3V I/O.

If a low value is sensed by the Module on VDD_IO_SEL# (because the Carrier has strapped it to GND), the Module does ***not*** power up it's 3.3V I/O interface and does **not** assert CARRIER_PWR_ON.

If a high value is sensed by the Module on VDD_IO_SEL#, the Module powers up and uses 3.3V I/O.

A Carrier that uses 3.3V I/O should float the Module VDD_IO_SEL# pin.

2.3.3 I/O at 1.8V or 3.3V

Carrier boards that operate at either 1.8V or 3.3V I/O are possible. There is a bit of overhead (i.e. extra parts on the Carrier are needed) to support this.

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2.4 VIN_PWR_BAD#

This optional signal may be used to tell the Module that the input power to the Module is not ready. An open-drain driver should be used.

2.5 CARRIER_PWR_ON

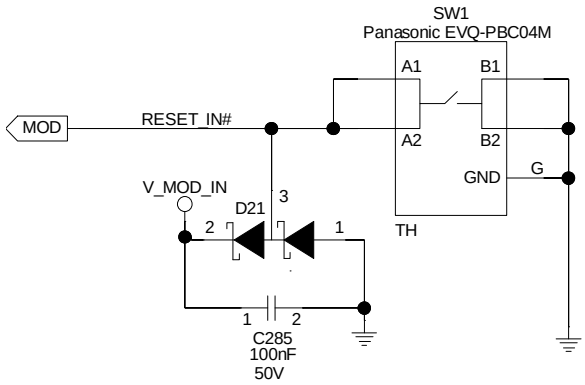
The CARRIER_PWR_ON signal is driven by the Module at the VDD_IO level. It is a signal to Carrier that the Carrier board specific power supplies may be enabled. This is illustrated in ***Figure 4 Basic Module and Carrier Power Path*** above.

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2.6 Reset In to Module

The SMARC RESET_IN# signal may be used to force a SMARC system reset. It is an input to the Module. The signal is pulled up on the Module. If used, by the Carrier board, then an open drain device or switch to GND should be used. A switch example is shown in the following figure. The signal is ESD protected in this example, as the switch (and the switch interaction with humans) introduces an ESD hazard.

Figure 5 Reset Switch



2.7 Power Button

SMARC defines a pin to allow the implementation of a Carrier based power button. However **- caution -** the SMARC HW specification does not define the power up behavior of a Module. The following possibilities exist after a cold power on:

a) Module boots

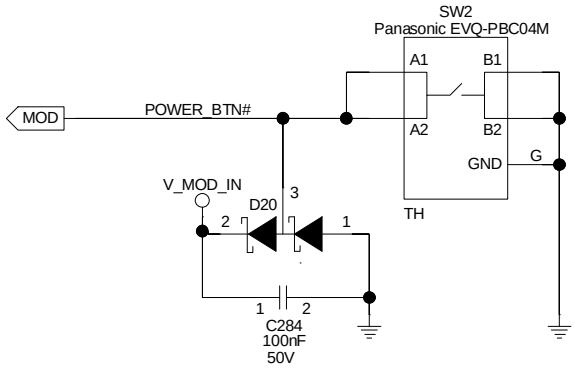
b) Module waits for a Power Button press to boot

c) The Module is configurable – either behavior a) or behavior b) may be configured

Users are advised to check with your Module vendor on this topic. A Power Button switch example is shown in the figure below. If your Module waits for a Power Button press on power up and you want it to always boot on power up, you have to arrange for a “power button press” on power up, using an open drain device to interface to the SMARC Module.

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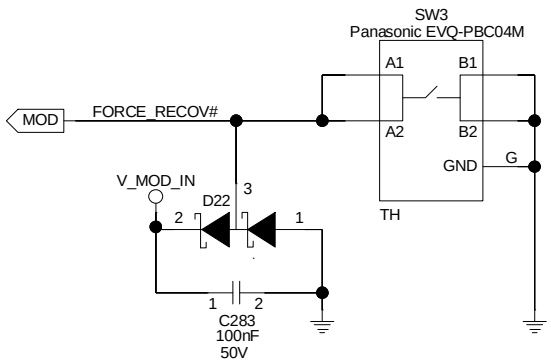
Figure 6 Power Button Switch



2.8 Force Recovery

Some Modules support a “force recovery” function in which the primary boot media can be re-initialized over a designated I/O interface, such as a USB client interface, asynchronous serial port, or Ethernet port. This is Module specific; refer to your Module documentation for further details.

Figure 7 Force Recovery Switch



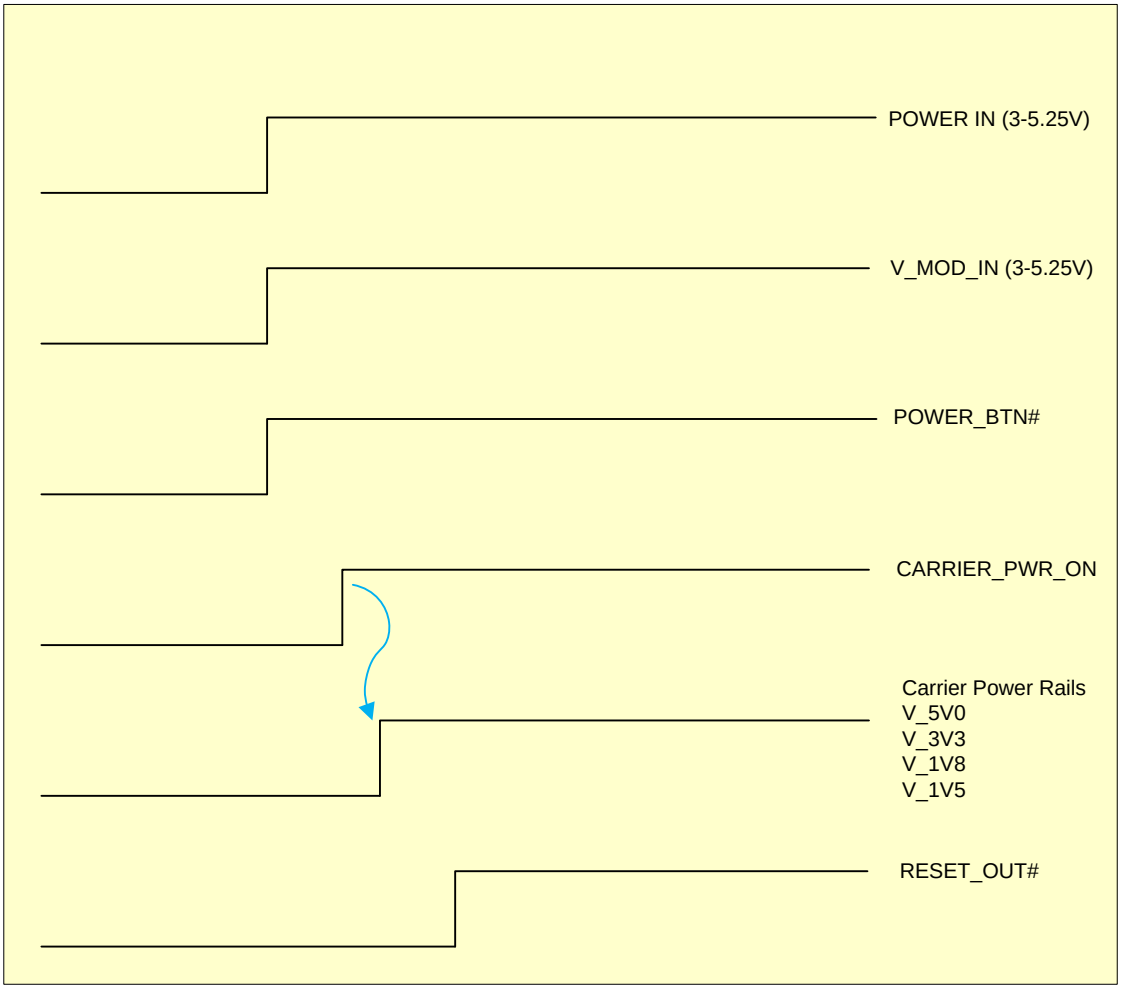
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2.9 Power Up Sequence

The basic power up sequence for SMARC Modules and Carriers is shown in the following two figures. There is a Module design and / or configuration dependence with regard to the power button behavior. Depending on design and / or configuration, the Module may always boot without waiting for a power button press, or it may wait for a power button press. These cases are shown in the figures.

It is recommended to arrange that the main Carrier power supplies not come up until the Module asserts the CARRIER_PWR_ON signal. When this is high, you know that the Module power supplies are all up. If the Carrier power is up before the Module supplies are up, there is a risk that the Carrier circuits will back-feed power to the Module I/O pins, which might interfere with a Module boot.

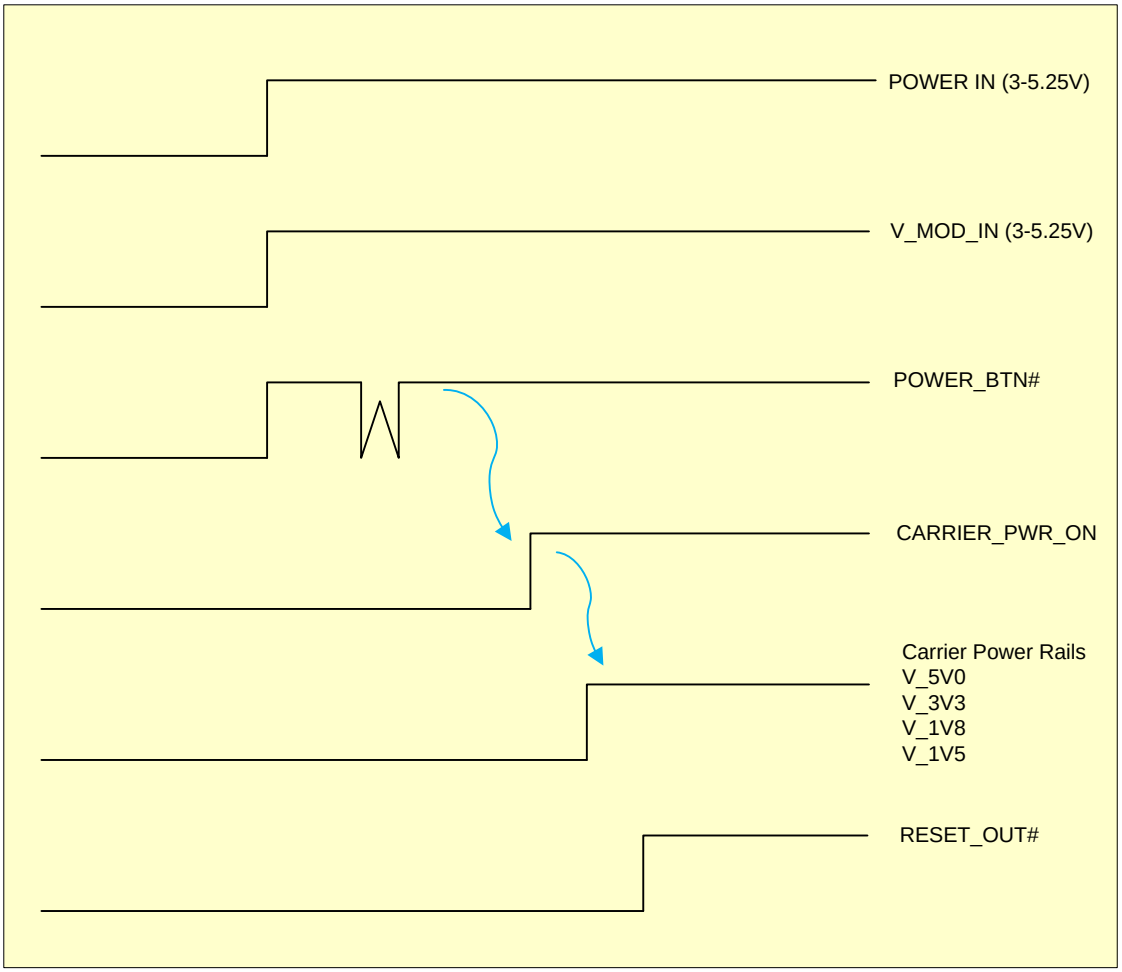
Figure 8 SMARC Carrier Power Up Sequence - No Power Button Case



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The case of a Module that is designed or configured to wait for a power button press before it comes up is diagramed below. When power is applied to the Module, in this case, only a small portion of the Module is using that power – typically, the Module Power Management section – and that circuitry waits for a power button press. When it sees one, the Module proceeds with the boot. When the main Module power rails are up, the Module asserts CARRIER_PWR_ON. The Carrier should use this signal to enable the various Carrier power rails. However, Carrier circuits that are involved in power management (battery charge level, reset monitors, etc.) may be powered ahead of CARRIER_PWR_ON, coincident with the Module power.

Figure 9 SMARC Carrier Power Up Sequence - With Power Button Case



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2.10 Boot Selection

2.10.1 Boot Definitions

Most SOCs used on SMARC Modules have the following attributes:

1) An internal ROM exists. The internal ROM code is executed after the SOC comes out of reset. This ROM code is provided by the silicon vendor and is generally not available or visible to users.

2) A set of SOC strap pins is used to select what SOC physical device interface (SD Card, SPI, eMMC, etc.) will be used for the 2nd – stage boot process (also known as BCT or Boot Configuration Table boot). There is no commonality between various SOCs as to how the strap pins are defined.

3) The SOC pin configuration is very flexible – most SOC pins can be used for several functions, and the SMARC Module designer must choose a pin configuration that works for the design at hand. The SOC pin configuration is set by a Boot Configuration Table that is read out from the external boot media (SD Card, SPI, eMMC, etc).

There are several stages in the boot process:

1) Internal SOC ROM execution

2) 2nd stage boot, from non volatile memory external to the SOC: BCT is loaded and various other system parameters are set

3) Operating System load

The Operating System load may occur from the same memory as the 2nd stage BCT boot, or the 2nd stage code may pass the Operating System load off to another device, such as a USB drive or SATA drive.

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2.10.2 SMARC BOOT_SEL Pins

The SMARC HW Specification defines 3 SMARC pins, designated BOOT_SEL0# through BOOT_SEL2#, that may be used to tell the Module what physical device to do a BCT boot from. The SMARC BOOT_SELx# pins serve to abstract the SOC – dependent strap definitions into a common SMARC definition. The table below is reproduced from the SMARC HW Specification document.

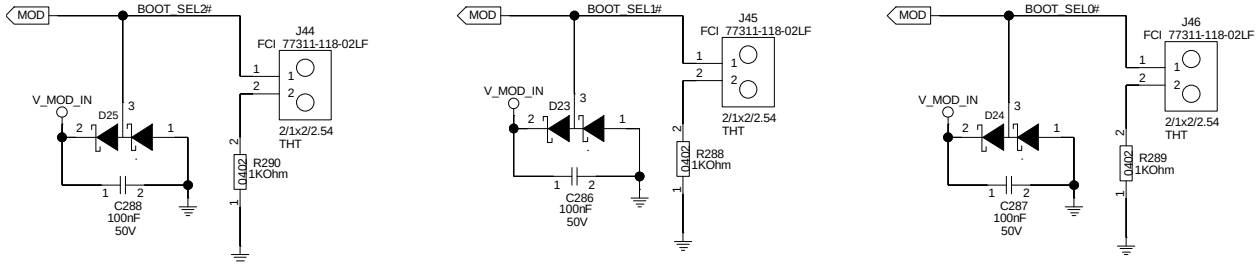
Table 2 Boot Select Pins

	Carrier Connection BOOT_SEL2#	BOOT_SEL1#	BOOT_SEL0#	Boot Source
0	GND	GND	GND	Carrier SATA
1	GND	GND	Float	Carrier SD Card
2	GND	Float	GND	Carrier eMMC Flash
3	GND	Float	Float	Carrier SPI
4	Float	GND	GND	Module device (NAND, NOR) – vendor specific
5	Float	GND	Float	Remote boot (GBE, serial) – vendor specific
6	Float	Float	GND	Module eMMC Flash
7	Float	Float	Float	Module SPI

The Module BOOT_SELx# pins may be set by jumpers on the Carrier Board, as shown in the figure below. The diodes and capacitors are for ESD protection, as the jumpers may experience ESD events.

Alternatively, the BOOT_SELx# pins can be set by low value option resistors to GND on the Carrier. The resistors are either installed (for a GND connection) or not installed, per the table above.

Figure 10 Boot Selection Jumpers



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2.11 RTC Backup Power

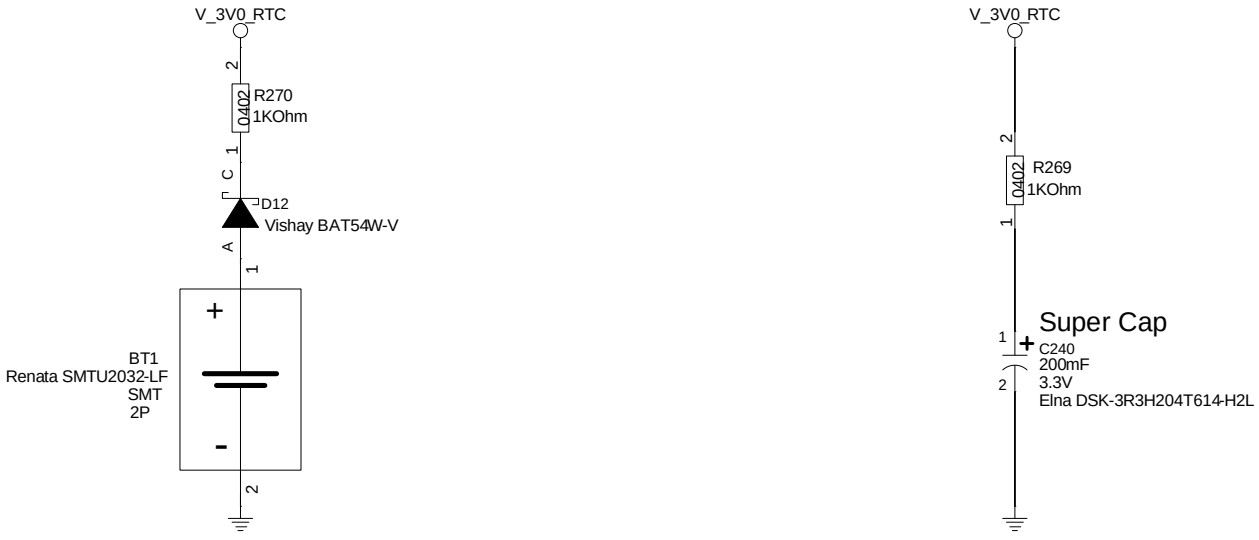
The Module RTC (Real Time Clock) circuit requires a backup power source if the Module RTC circuit is expected to keep time in the absence of the primary power source (i.e. the power to Module VDD_IN pins, P147 through P156). The RTC backup power, if used, is applied to the Module VDD_RTC pin, pin S147. The RTC backup power may be provided by a battery or by a large value capacitor, known as a "Supercap".

If a battery is used, the battery is typically a small lithium coin cell with a capacity of a few hundred mAH. Lithium coin cells offer a high energy density, low self-discharge rate, and are not rechargeable. For safety reasons, they must be protected against charging **on the Carrier board** by a redundant set of circuit elements – typically either two diodes in series or a diode and a resistor. The resistor, if used, must be large enough to limit the battery charging current to be equal to or lower than the amount specified as allowable by the battery vendor. The safety aspects of lithium battery use is governed by a UL document (***UL 1642 Lithium Batteries***, **www.ul.com**).

The Supercap solution differs from the lithium battery solution in that it needs to be charged by the Module (when the Module has its primary power source); hence a blocking diode should not be used with the Supercap.

The time period over which the RTC backup power is effective depends on the Module RTC backup current draw, the exact voltage range over which the Module RTC circuit is functional, on the capacity characteristics of the battery or Supercap, on the drops incurred across the Carrier board circuit protection elements, and on the operating temperature. In general terms, a suitable lithium battery solution can provide RTC backup current on a scale of years; the Supercap solution on a scale of days to weeks.

Figure 11 RTC Backup: Coin Battery / Super Cap



Coin Battery Holder, R/A, SMT

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2.12 Reserved / Test Interfaces

The Module TEST# pin (pin S157) should normally be left NC (not connected). If pulled low, then Module specific test function(s) may be enabled.

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3 DISPLAY INTERFACES

3.1 Module LVDS

3.1.1 NEC 1280 x 768 Single Channel LVDS Example

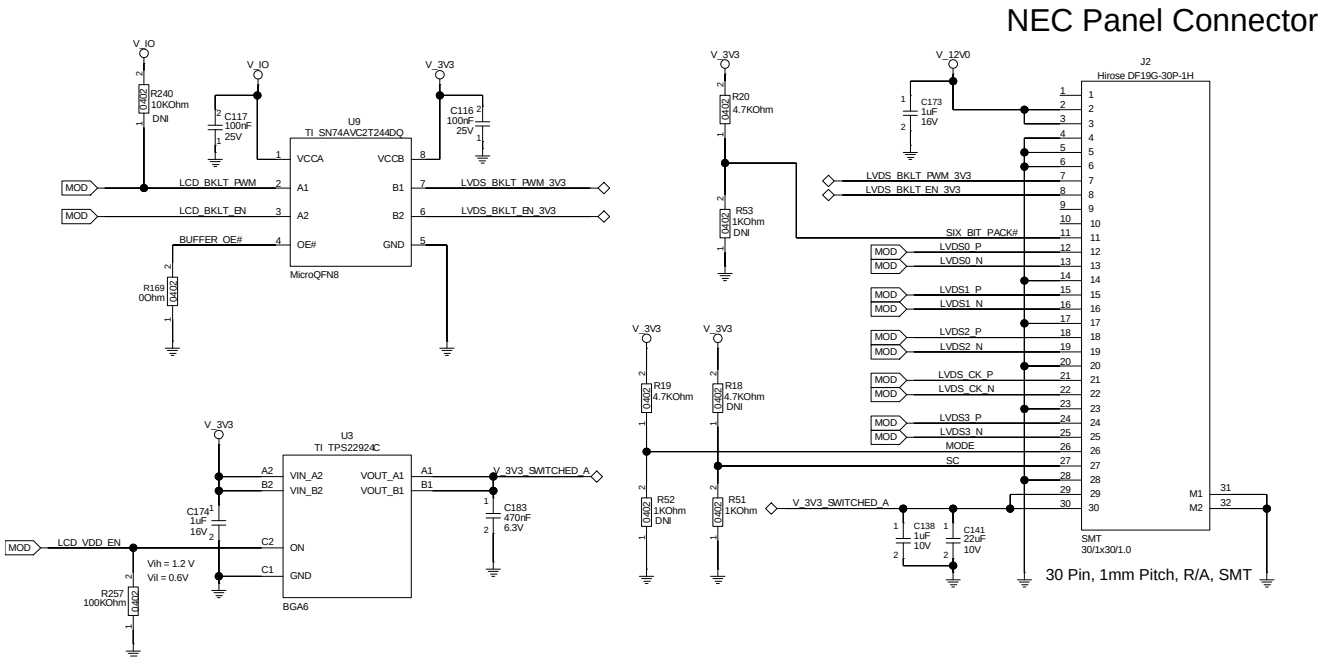
The Module LVDS interface may be used with single channel LVDS displays. SMARC Modules typically support LVDS 18 bit single channel operation (3 data pairs plus one clock pair). They may also support LVDS 24 bit single channel operation (4 data pairs plus one clock pair). Recall that there are two 24 bit color mappings in common use: most significant color bits on 4th data pair (sometimes referred to as the standard 24 bit mapping), and least significant color bits on the 4th LVDS data pair (referred to as 24 bit / 18 bit compatible or as 24 bit / 6 bit pack or similar). The standard 24 bit color mapping is more common but is incompatible with the 18 bit packing.

The example below shows an implementation used with an NEC 1280 x 768 single channel LVDS panel (NL 12876AC18-03). This panel uses a discrete wire 30 pin Hirose DF19 series connector. The panel backlight electronics accepts a 12V supply, and panel brightness is controlled by a 3.3V PWM signal. There is no EDID EEPROM on this particular NEC display.

This display happens to support 18 bit, 24 bit / 18 bit compatible and standard 24 bit LVDS packings. The panel also allows the image to be reversed. This can be useful if you find the panel connector orientations to be inconvenient – you can rotate the display 180 degrees, alter the scan direction strap, and have the image appear in the correct orientation. These options are set by pull-up and pull-down choices on connector pins 11,26 and 27 in the image below. Refer to the display data sheet for further information.

The display LVDS data and clock differential pairs may be connected directly to the SMARC Module. The backlight PWM and panel enable need level translation and / or buffering as shown in the figure.

Figure 12 Module LVDS: NEC Single Channel Display



Power for the display's logic is gated by the Module LCD_VDD_EN signal, as shown above.

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The NEC LVDS display in the example above accepts a 12V feed to power the display's LED backlight. The SMARC Module provides two backlight control signals, LCD_BKLT_EN and LCD_BKLT_PWM (enable and brightness).

Some displays require a higher voltage feed to their LED backlight electronics. An example of this is given in ***Section 10.6 High Voltage LED Supply.***

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3.1.2 Display Parameters and EDID

Flat panel display parameters (horizontal resolution, vertical resolution, pixel clock rate, blanking periods, etc.) may be hardcoded into a boot-loader or they may be read by boot-loader code from an industry standard data structure known as EDID (Extended Display Identification Data). EDID data is stored in an EEPROM accessed via I2C. The EDID EEPROM may reside on the display assembly or elsewhere in the path between the SOC and the display – on the Carrier or on a display adapter assembly.

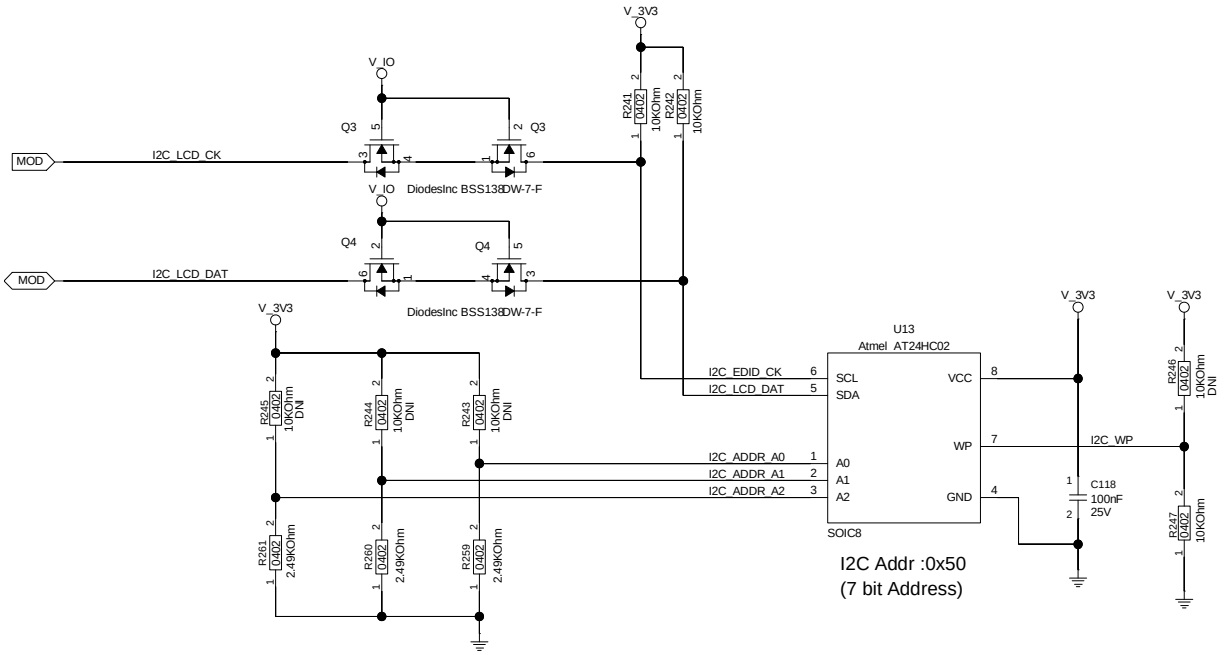
If the EDID EEPROM resides on the display, then the cabled interface to the display must include the SMARC Module I2C_LCD interface. The interface should be level translated and possibly buffered. The I2C voltage levels on the display are most likely to be at 3.3V levels. A set of back-to-back FETs may be used for I2C level translation, as shown in the figure immediately below. Alternatively, a device such as the Fairchild FXMA2102 I2C buffer / level translator may be used. There is a circuit example using the FXMA2102 later in this document.

In the display interface example above, with the 30 pin Hirose DF19 series connector, pins 9 and 10 could be used for the buffered I2C_LCD clock and data, respectively.

The figure below shows an EDID EEPROM implementation that may be used on a Carrier. It might be advantageous to use a socket for the EEPROM to allow display parameters to be swapped out. Alternatively, system software could update the EEPROM if the EEPROM WP (Write Protect) pin is set to enable writes. Or, the system designer could implement an EEPROM programming header for update purposes. Caution: if there is an EDID EEPROM on the Carrier and on the display, there will be an I2C address conflict unless one of the two is disabled or set to an alternate address. VESA EDID EEPROMs are expected at 7 bit I2C address 0x50.

There are many EDID editors available, some for free. It can be very useful to have access to one if you are trying to adapt a new panel, and if your SMARC Module software knows what to do with EDID data. Alternatively, your SMARC Module and / or Carrier board vendor may well be able to help with display adaptations.

Figure 13 Carrier EDID EEPROM



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3.2 HDMI

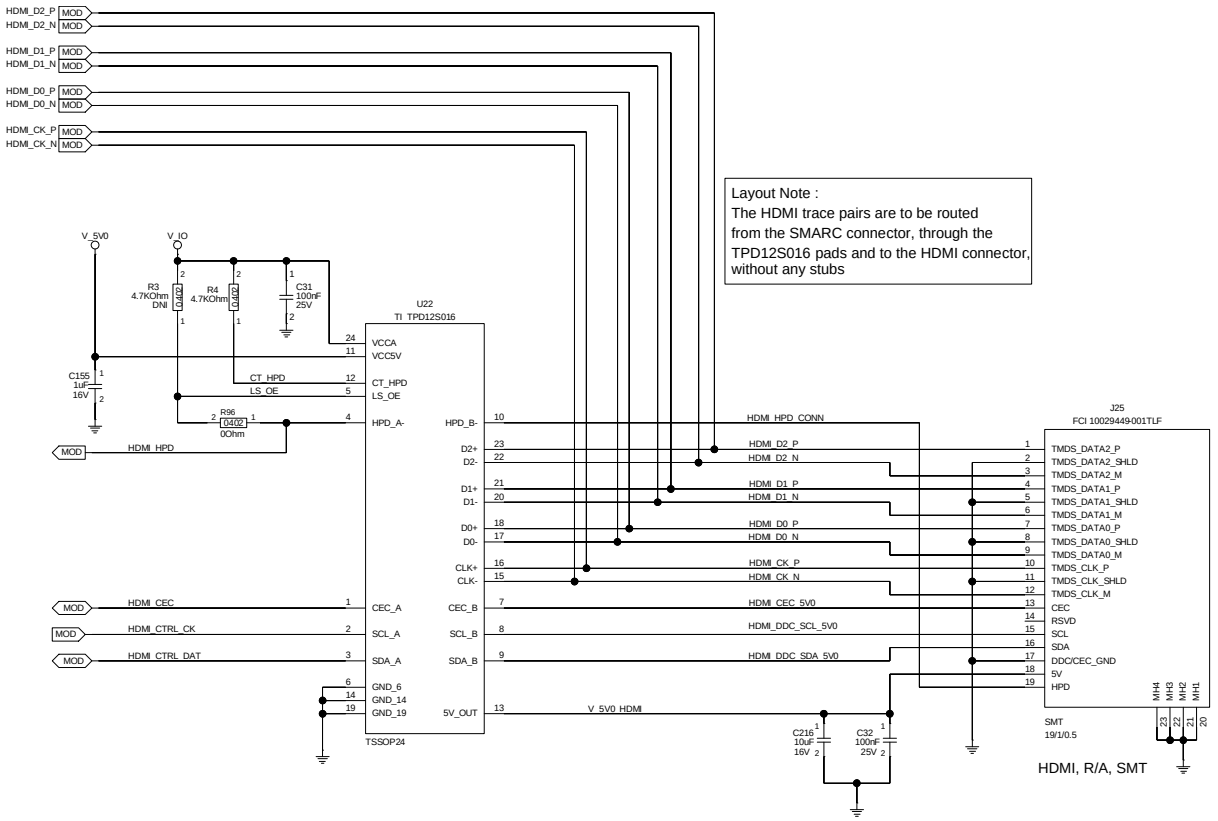
Note: a license may be needed to market HDMI capable products. Check with the HDMI organization (**www.hdmi.org**) and with your SMARC Module vendor.

The SMARC HDMI data pairs may be routed directly from the SMARC Module pins to a suitable Carrier HDMI connector. Since HDMI is a hot-plug capable interface, it is important for the Carrier to implement ESD protection on all of the HDMI lines. The ESD protection on the data lines must be low capacitance so as not to degrade high speed signaling. The data lines must route through the ESD protection device pins in a no-stub fashion. The ESD protection should be located close to the HDMI connector.

The SMARC pins HDMI_CTRL_CK, HDMI_CTRL_DAT and HDMI_CEC require level translation from V_IO to the 5V levels that HDMI uses on those pins. These lines also require pull-up resistors to V_IO (the pull-ups are not included on the SMARC Module, because integrated HDMI protection devices such as the Texas Instruments TPD12S016 and others from companies such as NXP include the pull-ups in their parts). And, finally, 5V power switching / current limiting to the HDMI connector is required on the Carrier.

The ESD protection, level translation and power switching / limiting are all dealt with in integrated devices such as the TI TPD12S016. A circuit diagram is shown in the following figure. The TPD12S016 must be placed close to the HDMI connector, and the HDMI data traces routed in daisy chain fashion (and as differential pairs) from the SMARC Module pins, to and through the TPD12S016 pins, and on to the HDMI connector pins. The TPD12S016 pin-out is specifically designed to facilitate this.

Figure 14 HDMI Implementation



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3.3 Carrier LVDS – Dual Channel 24 Bit VESA Standard

The Module parallel LCD bus may be used to feed a Carrier Board LVDS transmitter. Single and dual channel implementations are possible. Since the SMARC Module already provides a single channel LVDS output, it seems that the most common SMARC Carrier board LVDS transmitter application would be for dual channel displays. Displays are often implemented as dual channel displays for resolutions at and above 1280 x 1024. A dual channel implementation allows the cable interface to run at half the speed of a single channel implementation, at a given resolution.

The figure below shows a very cost effective dual channel LVDS transmitter circuit, based on the Texas Instruments DS90C187 part. ***Note that the DS90C187 is a 1.8V I/O part; it does not accept 3.3V I/O***.

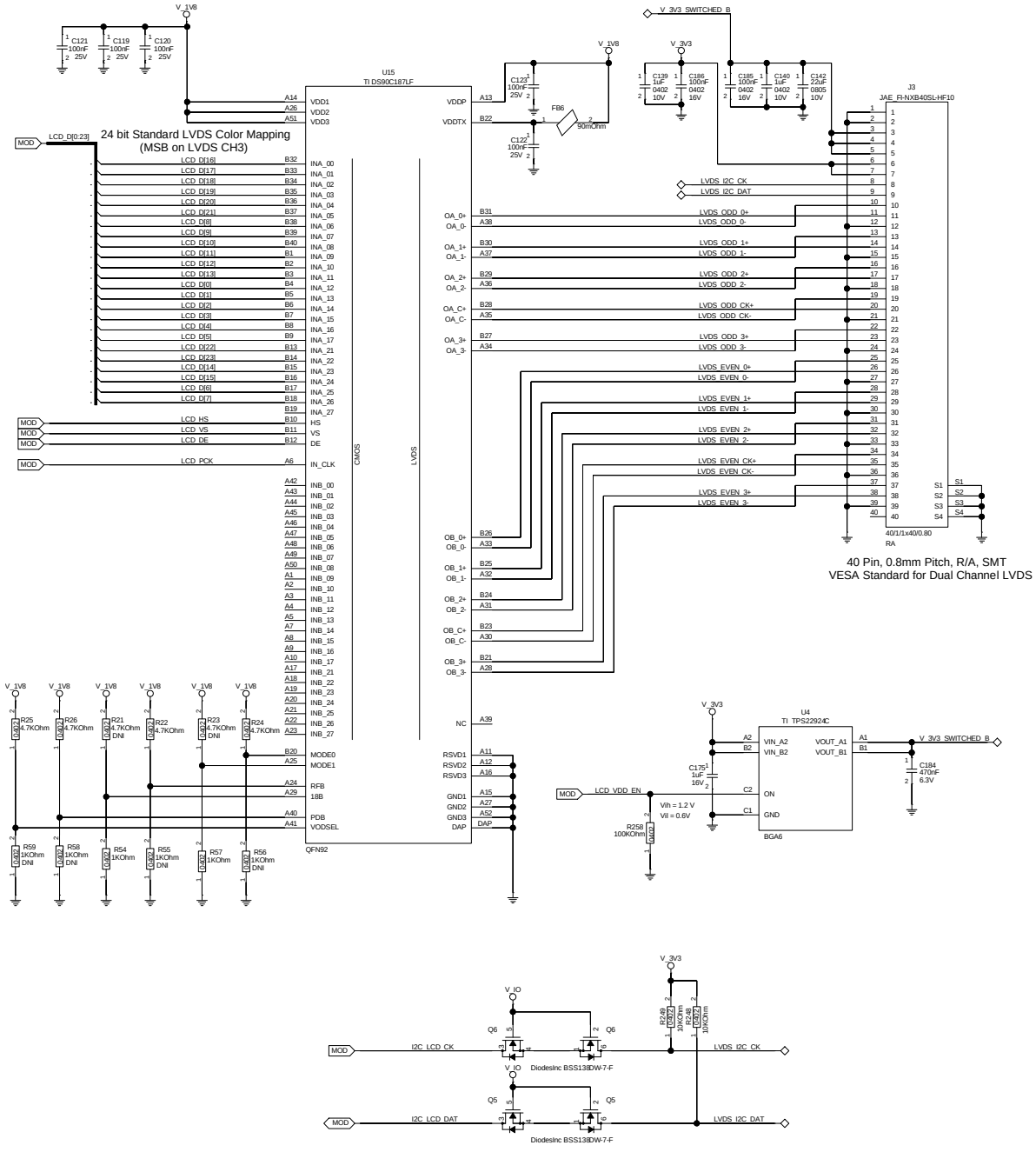
Recall that there are two different color packings used for 24 bit LVDS implementations. The implementation shown is for the “standard”, or more common packing, in which the most significant color bits are packed into the 4th LVDS data stream. It is not compatible with 18 bit color packs. It is possible to use the 18 bit compatible 24 bit color packing (least significant color bits packed into the 4th LVDS data stream) by re-arranging the order of the parallel LCD data bits as they come into the DS90C187. Refer to the TI DS90C187 data sheet for details.

If a dual channel capable LVDS transmitter with 3.3V (and 1.8V) I/O is required, the Thine Semiconductor THC63LVD827 may be used. It costs quite a bit more than the TI part though.

The discussion in Section ***3.1.2 Display Parameters and EDID*** above about display parameters and EDID data structures applies here as well.

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Figure 15 Dual Channel 24 Bit LVDS: VESA Standard



The DS90C187 part above allows numerous configuration choices, set by the strap pins shown at the lower left of the IC. These choices include single channel LVDS, dual channel LVDS, 18 bit color packing, 24 bit standard color packing, and 24 bit / 18 bit compatible color packing. There are also input clock options – see the TI data sheet for details. The straps in this example are set for dual channel LVDS, 24 bit standard color pack, 1x input clock.

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3.4 Parallel LCD

The SMARC Module parallel LCD pins may be used to drive a traditional parallel LCD interface (or they may be used to drive LVDS transmitters or other transmitters that accept parallel LCD data at the Module V_IO level).

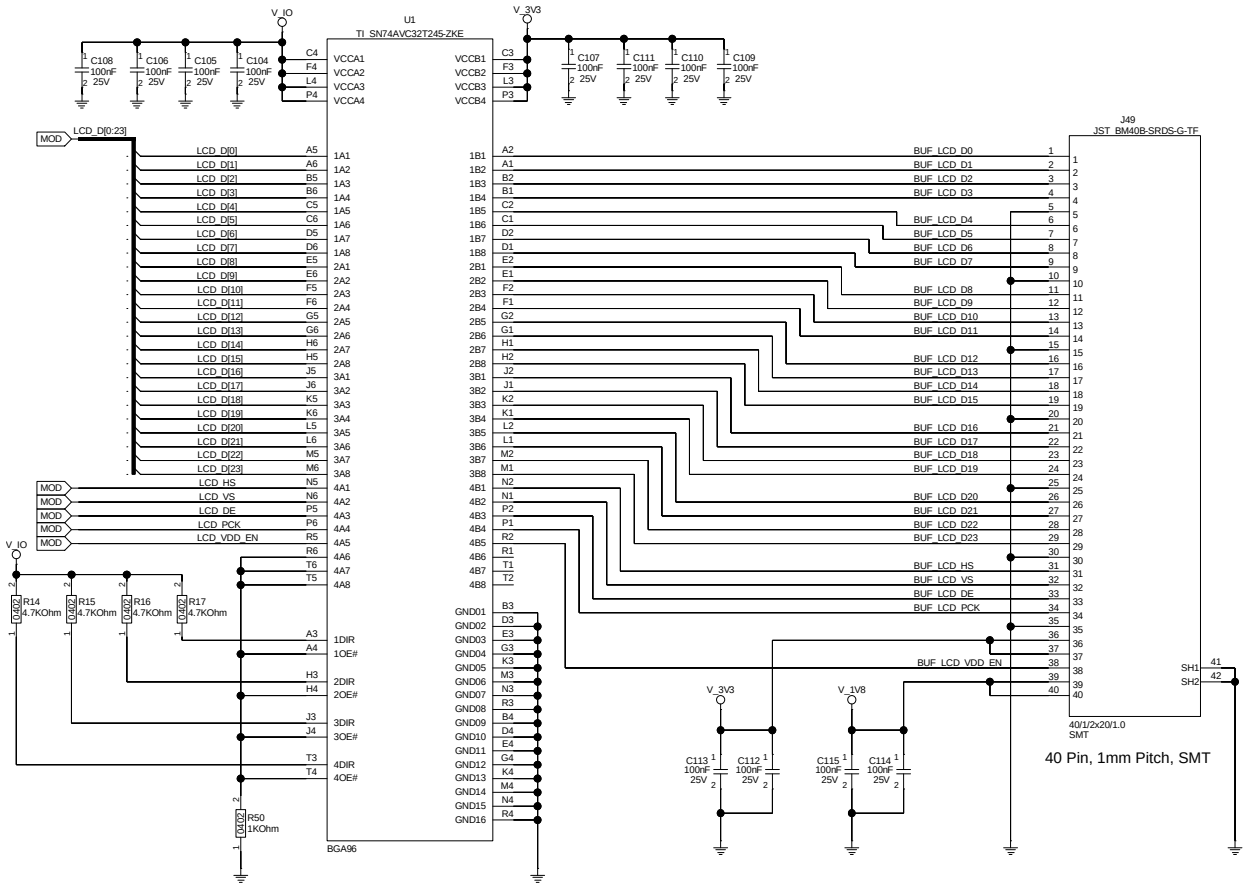
The Module V_IO is typically 1.8V. Parallel displays with 1.8V I/O are available in very small form factors (think cell phone and digital camera size). In this case, the SMARC Parallel LCD data signals may be passed directly to the display, for short cable runs.

For larger displays, the display will likely require a 3.3V data I/O level. The circuit shown in the figure below achieves signal buffering and voltage translation from V_IO to a 3.3V display.

If there is a requirement for a display cable longer than a few inches, it may be a good idea to include the buffer even if the display accepts 1.8V I/O. The buffer shown in the figure below can be used for this case as well – the power pins at the upper right side of the IC symbol would be connected to 1.8V rather than 3.3V for this case.

The discussion in Section ***3.1.2 Display Parameters and EDID*** above about display parameters and EDID data structures applies here as well.

Figure 16 Parallel LCD Implementation



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4 LOW / MEDIUM SPEED SERIAL I/O INTERFACES

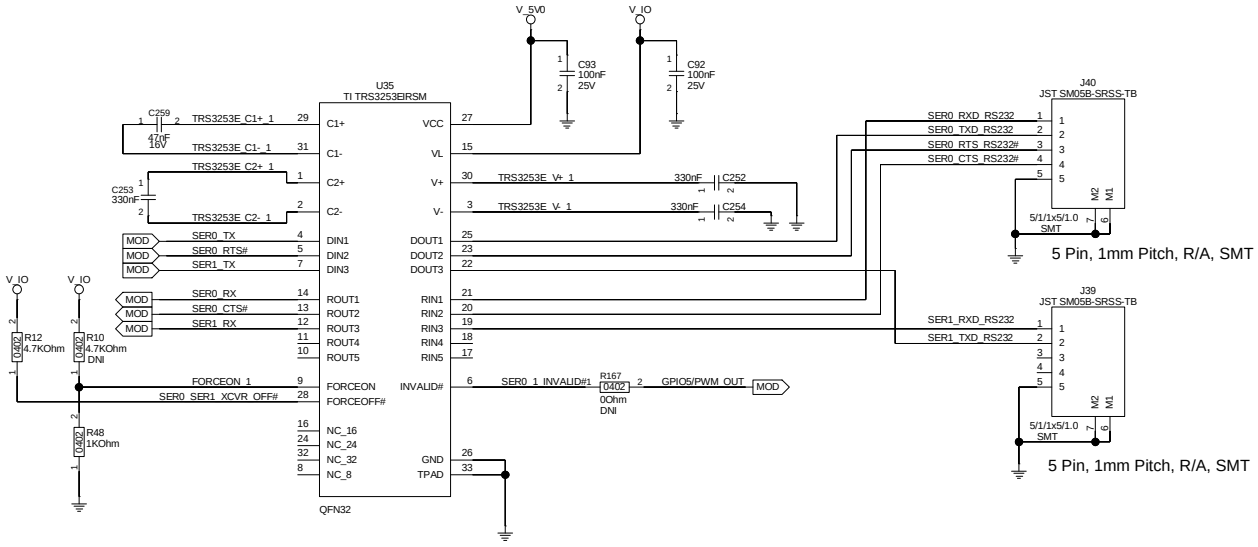
4.1 Asynchronous Serial Ports

4.1.1 RS232 Ports

The SMARC Module asynchronous serial ports run at V_IO (usually 1.8V) logic levels. The transmit and receive data lines from and to the Module are active high, and the handshake lines are active low, per industry convention.

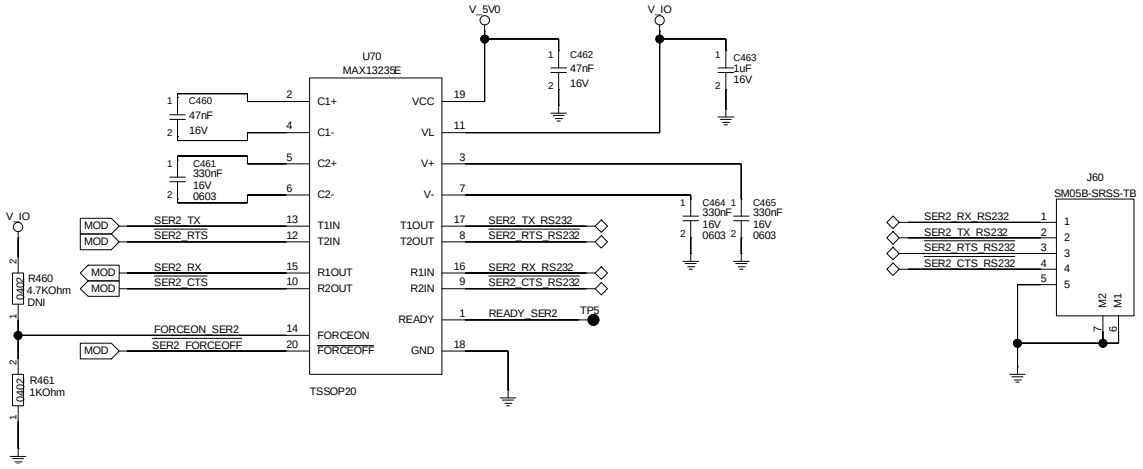
If the asynchronous ports are to interface with RS232 level devices, then a Carrier RS-232 transceiver is required. The logic side of the transceiver must be able to run at V_IO levels. The selection of 1.8V compatible transceivers is a bit limited, although more are appearing with time. Two such devices are the Texas Instruments TRS3253, and the Maxim MAX13235, illustrated in the figures below. The TI part is more cost effective, but has a top speed of 1 Mbps. The MAX 13235 can operate at maximum speeds over 3 Mbps (but your SMARC Module may or may not - check with your Module vendor). The transceivers invert the polarity of the incoming and outgoing data and handshake lines.

Figure 17 Asynchronous Serial Port Transceiver – RS232 – TRS3253



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Figure 18 Asynchronous Serial Port Transceiver – RS232 – MAX13235



4.1.2 RS485 Half-Duplex

A half-duplex RS485 asynchronous serial port implementation is shown below. This hardware implementation is suitable for multi-drop RS485 networks. The Maxim MAX13451 transceiver accepts 1.8V logic I/O and has other, flexible features of interest such as internal termination options.

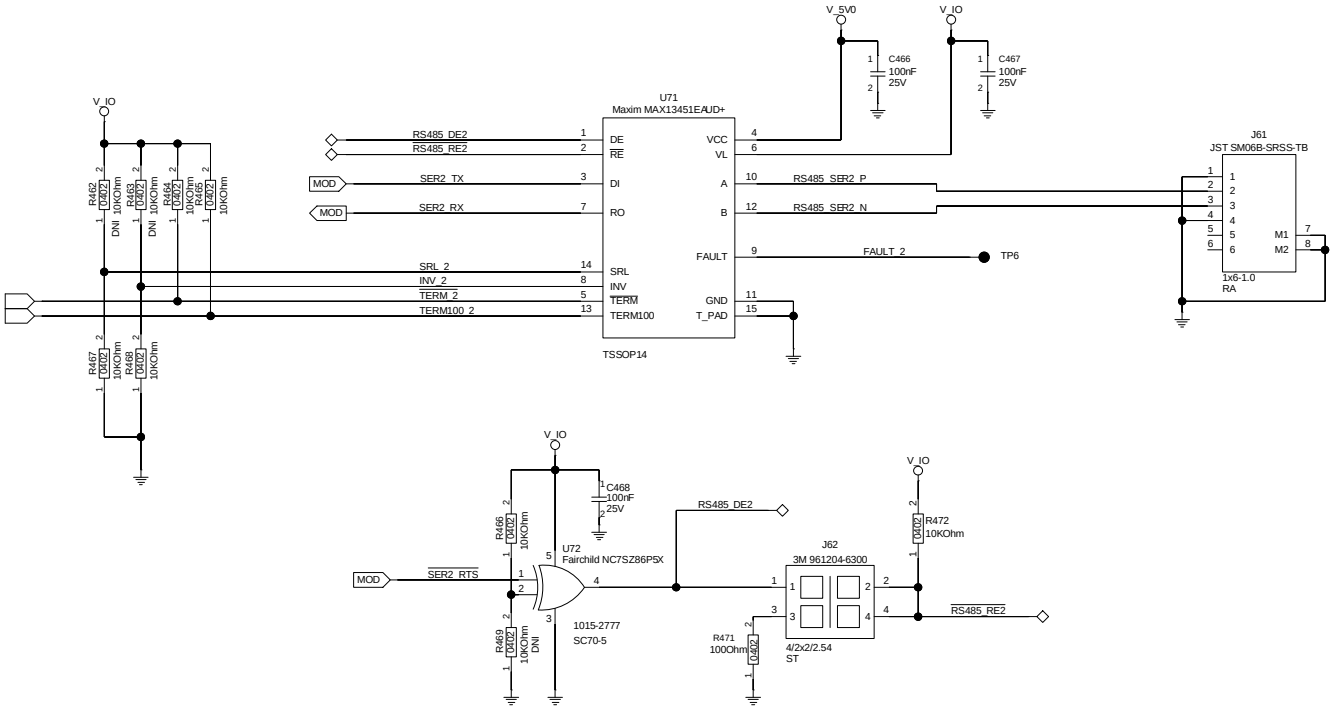
Multi-drop RS485 nodes should be strung together in daisy chain fashion using shielded twisted pair cable with a defined differential impedance (usually 120 ohms; sometimes 100 ohm cables are used). The two end-points of the system should be resistively terminated across the pair. The termination value should equal the differential impedance of the twisted pair cable used. The Maxim transceiver allows the termination to be enabled or disabled on the TERM# pin, and can be selected to be 100 ohms or 120 ohms via the TERM100 pin state. These pins can be controlled by Carrier GPIOs if desired.

The RS485 driver is enabled when the SMARC SER2_RTS# signal is asserted low (if the resistor options in front of the XOR gate are loaded as shown, such that the XOR gate inverts the SER2_RTS2# signal for the RS485_DE2 function).

A suitable, likely application specific, software driver is required to make the multi-drop RS485 network sing.

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Figure 19 Asynchronous Serial Port Transceiver - RS485 – Half Duplex



Jumper 01-02	Jumper 03-04	State
Open	Open	RS485 reciever disabled
Open	Closed	RS485 reciever always enabled
Closed	Open	RS485 reciever enbled when transmitter disabled
Closed	Closed	Invalid

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4.2 I2C Interfaces

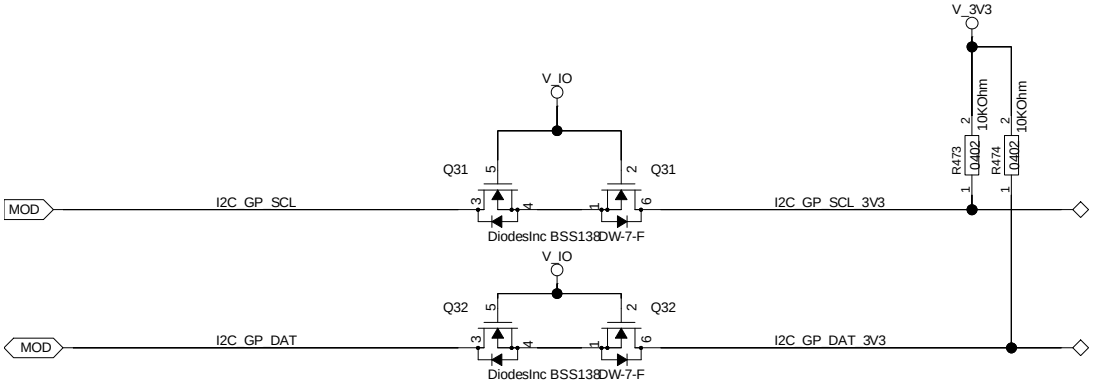
4.2.1 General

The I2C bus is a versatile low bandwidth multi-drop bus originally defined by Philips (now NXP). It is a two wire bus (clock and data) that relies on the use of open-drain drivers and passive pull-ups. The bus can be single Master or Multi-Master. SMARC Modules are always I2C Masters. Whether or not they allow other Masters is Module implementation dependent. Most SMARC systems use the I2C bus as a way for the SMARC I2C Masters to interface to a variety of I2C Slave peripherals. The standard I2C interface operation speeds are 100 KHz and 400 kHz. Some implementations allow faster speeds.

4.2.2 I2C Level Translation, Isolation and Buffering

FETs may be used to perform I2C level translation, as shown in this figure. This arrangement provides no buffering. It can provide isolation to prevent one side of the bus dragging down the other if one of the rails is collapsed. The rail that is to collapse should be the rail driving the FET gates.

Figure 20 I2C Power Domain Isolation – using FETs

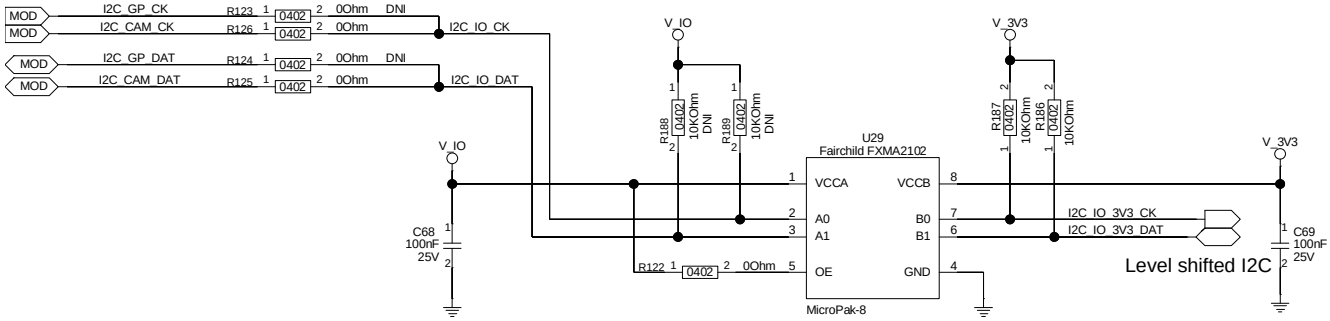


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The circuit shown just below can provide power domain isolation, voltage level shifting and I2C bus buffering. The Fairchild FXMA2102 power rails VCCA and VCCB can be at the same voltage level or at different levels, over a range of 1.65V to 5.5V. Either rail can come up before the other.

If you have many I2C devices, it is a good idea to split them up into segments with up to about 6 devices on each segment, and isolate the segments with a bi-directional I2C buffer such as the FXMA2102. I2C bus performance degrades with too much capacitive loading.

Figure 21 I2C Power Domain Isolation and Buffer – Fairchild FXMA2102



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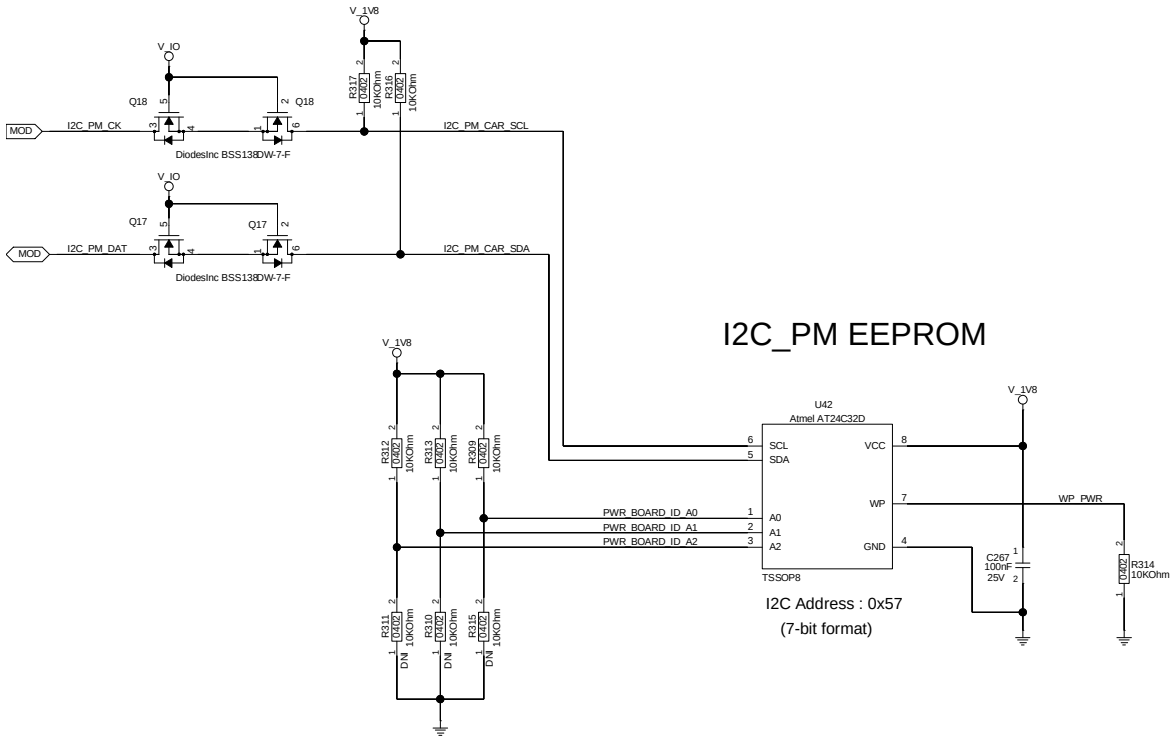
4.2.3 I2C_PM Bus EEPROMs

The SMARC I2C_PM bus is special in that it is used on the Module for power management functions, and it always runs from a 1.8V rail on the Module (even if the SMARC V_IO is set to 3.3V). The 1.8V voltage rail requirement on the I2C_PM bus allows it to be powered from a simple, low quiescent current linear or buck switching regulator from V_MOD_IN.

On the Module, since it is used for power management, it is “on” even when the Carrier power may be off (i.e. the CARRIER_PW_ON signal may be low, and Carrier circuits that are not involved in power management are powered off).

If the I2C_PM bus is used on the Carrier for functions that are not power management functions, then it needs to be isolated from the Module by a set of back to back FETs, as shown in the following figure. The V_1V8 in the figure is a Carrier board power rail that may be collapsed; the Module side of the I2C_PM must not be dragged down.

Figure 22 I2C_PM EEPROM: Carrier Power Domain

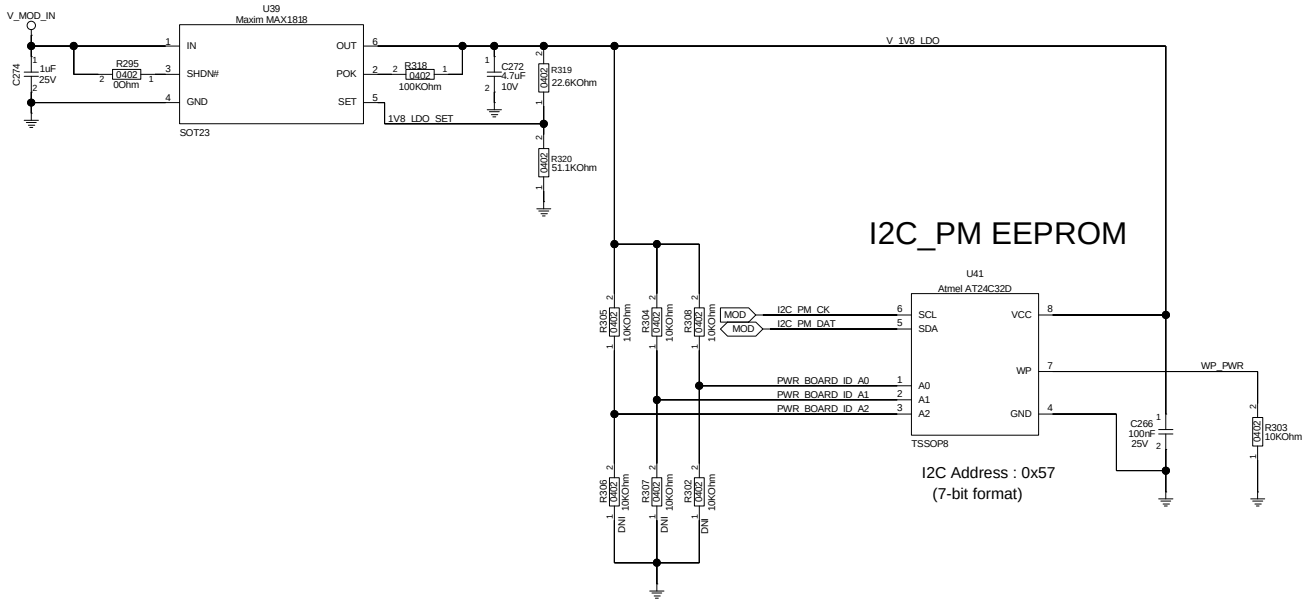


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The SMARC I2C_PM bus may be used on the Carrier for power management functions, such as interfacing to a battery charger or battery fuel gauge. In this case, the power circuits and the I2C_PM interface to the SMARC Module need to be powered whenever power is on.

A local low quiescent current low drop out linear regulator is needed to provide 1.8V for the Carrier board “Module domain” devices.

Figure 23 I2C_PM EEPROM: Module Power Domain



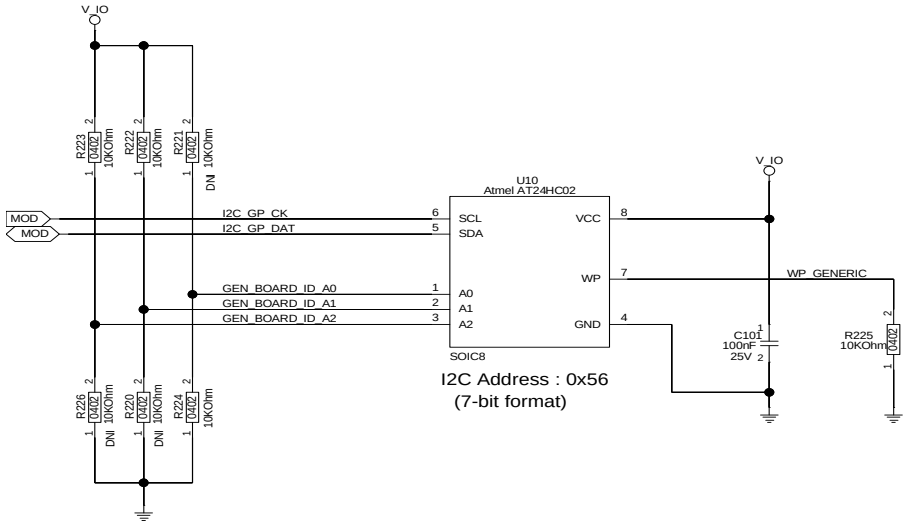
The SMARC Module specification recommends - but does not require - that Carriers have a parameter EEPROM on the I2C_PM bus, preferably configured as shown here, in the “Module Power Domain”. This, in principle, allows the Module to query the Carrier I2C_PM EEPROM before asserting the CARRIER_PWR_ON signal that enables the main Carrier board power feed.

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4.2.4 General I2C Bus EEPROMs

The “other” SMARC I2C buses (I2C_LCD, I2C_GP, I2C_CAM) operate at V_IO (typically 1.8V). The power domain isolations described in the previous section do not apply. A simple sample EEPROM circuit is shown for reference.

Figure 24 I2C_GP EEPROM



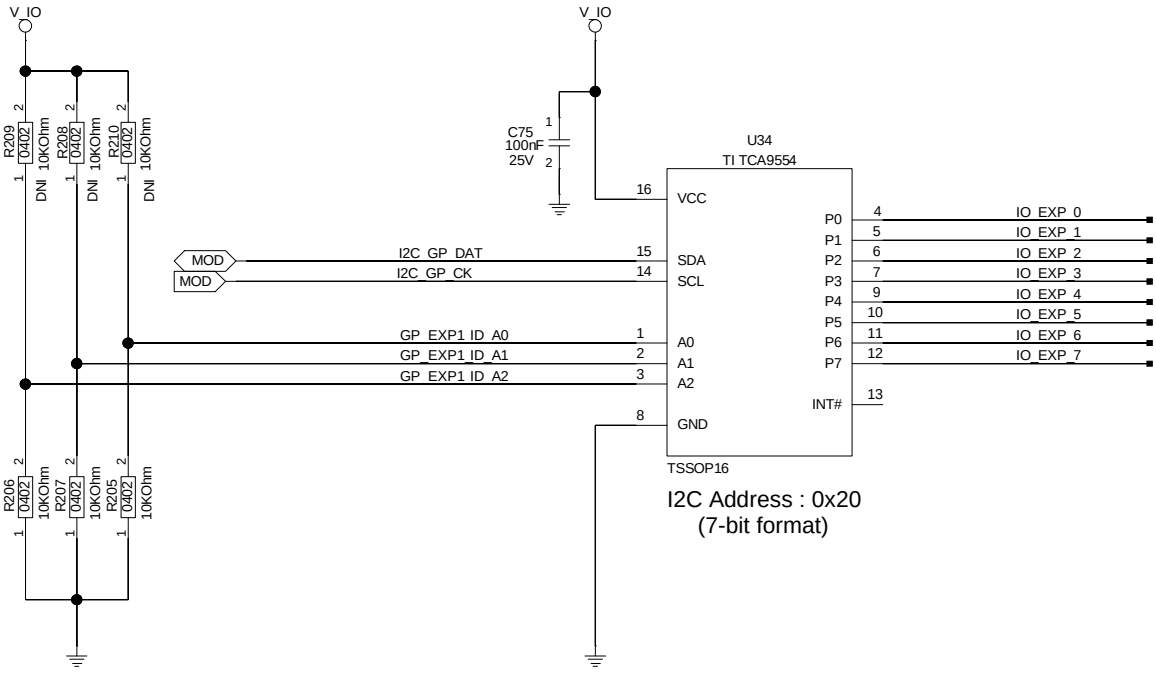
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4.2.5 I2C Based IO Expanders

I2C based “I/O Expanders” are available from Texas Instruments, NXP and others. Multiple expanders may be put onto the same I2C bus by configuring the I/O expander I2C address straps. These devices are an easy and cost effective way to realize additional IO on SMARC systems.

On the device shown in the figure, the I/O ports on the right are all in a high impedance “tri-state” mode when the device powers up. This allows the designer to tie the I/O lines through resistor pull-ups or pull-downs to define a power up state for these lines, before the I2C interface and before software are active. Wider (x16) devices are also available.

Figure 25 I2C Device: IO Expander



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4.2.6 Other I2C Devices

There is a very wide variety of I2C peripherals available on the market. Since SMARC Modules offer up to four I2C buses (not counting the HDMI private I2C bus), it is easy to incorporate I2C devices into a SMARC system. A few schematic examples are given here, and further suggestions are listed in the table at the end of this section.

Figure 26 I2C Device: Accelerometer

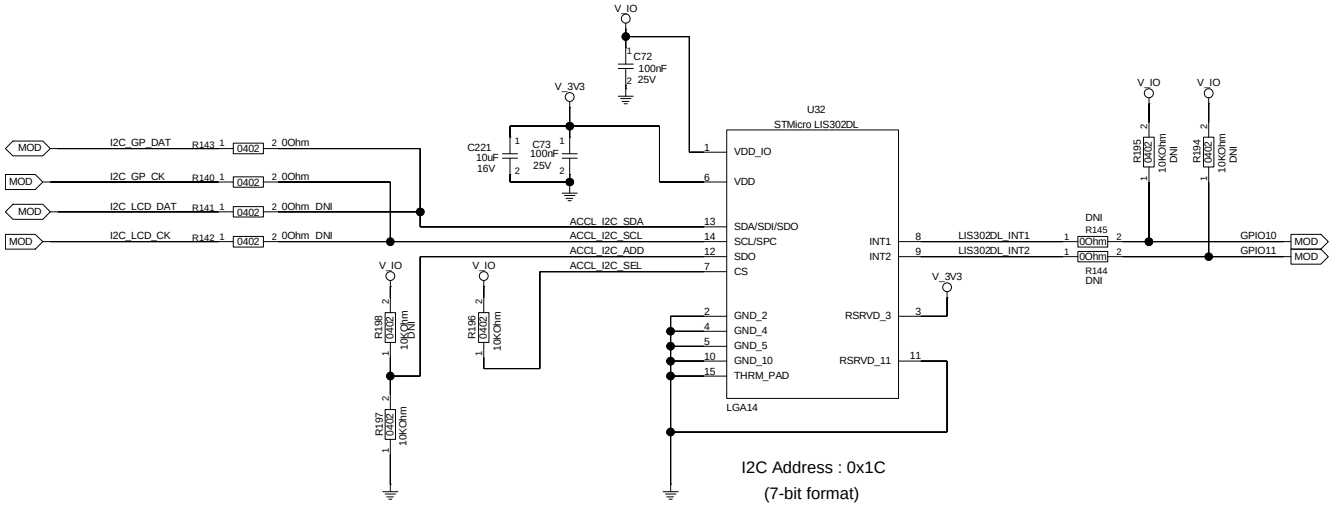
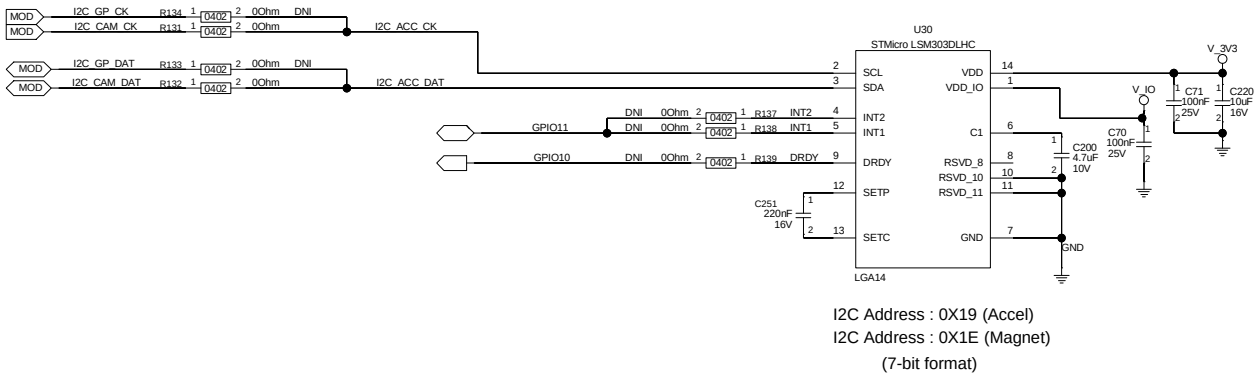
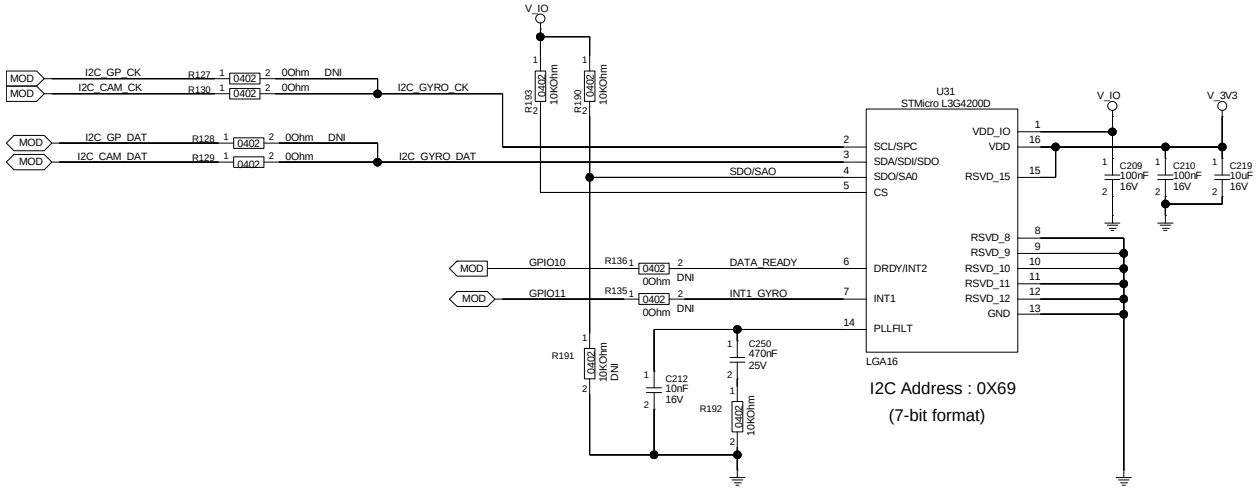


Figure 27 I2C Device: Accelerometer and Magnetometer



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Figure 28 I2C Device: Gyroscope



The table below gives a small sampling of other 1.8V I/O I2C devices that are available. The list is meant to just give the reader an idea of what types of devices are available.

Table 3 I2C Device Examples - 1.8V I/O

Function	Device Description	Vendor	Vendor P/N
ADC	8-channel, 12-bit SAR ADC with temperature sensor	Analog Devices	AD7291
Ambient Light Sensor	Digital ALS, Range: 0.025 Lux to 104,448 Lux	Maxim Integrated	MAX44007EDT
Battery fuel gauge	Li-ion battery Fuel gauge with direct battery connection	Texas Instruments	BQ27510-G2
DAC	Quad, 16-bit DAC	Analog Decices	AD5696R
LED driver	7-bit LED driver with intensity control	Texas Instruments	TCA6507
Proximity / Button sensor	Four Channels, Capacitive Proximity/Button Solution	Semtech	SX9500
Temperature Sensor	Temperature Monitor, ±1° Cel	On Semiconductor	NCT72
UART	128 Word FIFOs	Maxim Integrated	MAX3108

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4.3 Touch Screen Controller Interfaces

4.3.1 General

The two most popular touch technologies used with SMARC systems are summarized in the following table.

Table 4 Popular Touch Technologies

Technology	Notes
Resistive	Low cost; rugged. Display clarity and contrast may be compromised by the resistive touch overlay. Usually used with a stylus but may be used with bare fingers. Multi-touch is possible but not common. More straightforward to implement than capacitive touch.
Projected Capacitive	Higher cost, higher barrier to entry and better quality and user experience than resistive touch. Multi-touch capable. Excellent optics.

There are many other touch technologies, some better suited to certain situations such as user's wearing gloves and so on. An overview may be found on the EloTouch website: **www.elotouch.com** under "Touchscreens".

4.3.2 Interface Types / Driver Considerations

Various host interface types are used by touch screen controllers. A given controller may implement one or more of the following interfaces: USB client, I2C, asynchronous serial port, I2S, SPI, or other interface.

USB interfaces for touch screen controllers are attractive as there is the potential that the software effort is minimal: the touch screen controller may act as a USB HID (Human Interface Device) class device, and the operating system at hand may be able to understand the generic touch HID implementation directly. However, for more advanced touch implementations, such as multi-touch (the ability to track and decipher multiple, simultaneous touch hits on a screen), a more specialized driver is usually necessary. The driver is often touch – controller vendor specific. Additionally, a touch controller vendor may offer multiple hardware interfaces, but the driver may be optimized for one particular hardware interface. The conclusion is: check out the software driver situation before going down a particular hardware path.

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4.3.3 Touch Controller Modules / ICs / Screens

Table 5 Touch Controller Module / IC / Screen Vendors

Vendor	Notes	Web Link
Atmel	Key vendor of touch screen controller ICs for projected capacitive screens. Atmel is a silicon vendor, and generally will not help directly with touch screen integration issues, unless your company is a Tier 1 company. Atmel has a network of partners that they will steer you to for help with integration issues. Some of the partners from Atmel's list are included in this list.	**www.atmel.com**
Data Modul	Selection of touch screen panels, overlays and controller modules for projective capacitive technology and for resistive touch screens. Company is based in Germany and has a presence in the USA. Products are marketed under the "Easy Touch" trade mark.	**www.data-modul.com**
EloTouch	Elo offers a variety of finished touch panels. They also offer a popular controller chip for resistive touch panels, under the marketing name "AccuTouch COACh V Controller Chip".	**www.elotouch.com**
Ocular LCD	Selection of touch screen panels, overlays and controller modules for projective capacitive technology. The company also offers custom design services for optically bonding touch overlays to display panels. Company is based in the USA and has a presence in China. Products are marketed under the "Crystal Touch" trade mark.	**www.ocularlcd.com**
Pixcir	Vendor of controller ICs for projected capacitive screens. Based in China and in Switzerland.	**www.pixcir.com**
Precision Design Associates	Touch modules and touch overlay screens. Based in Marietta, Georgia, USA.	**www.pdaatl.com**
Touch International	Touch overlays, modules and integration services. One of the larger and better known companies in this field. Based in the state Texas, USA. The Touch International website has an overview of various touch technologies.	**www.touchinternational.com**

Also check with your SMARC Module vendor or your SMARC Carrier design partner – some of them have in-house solutions for particular display panels.

Also remember to consider the availability of software drivers for the choices that you are making.

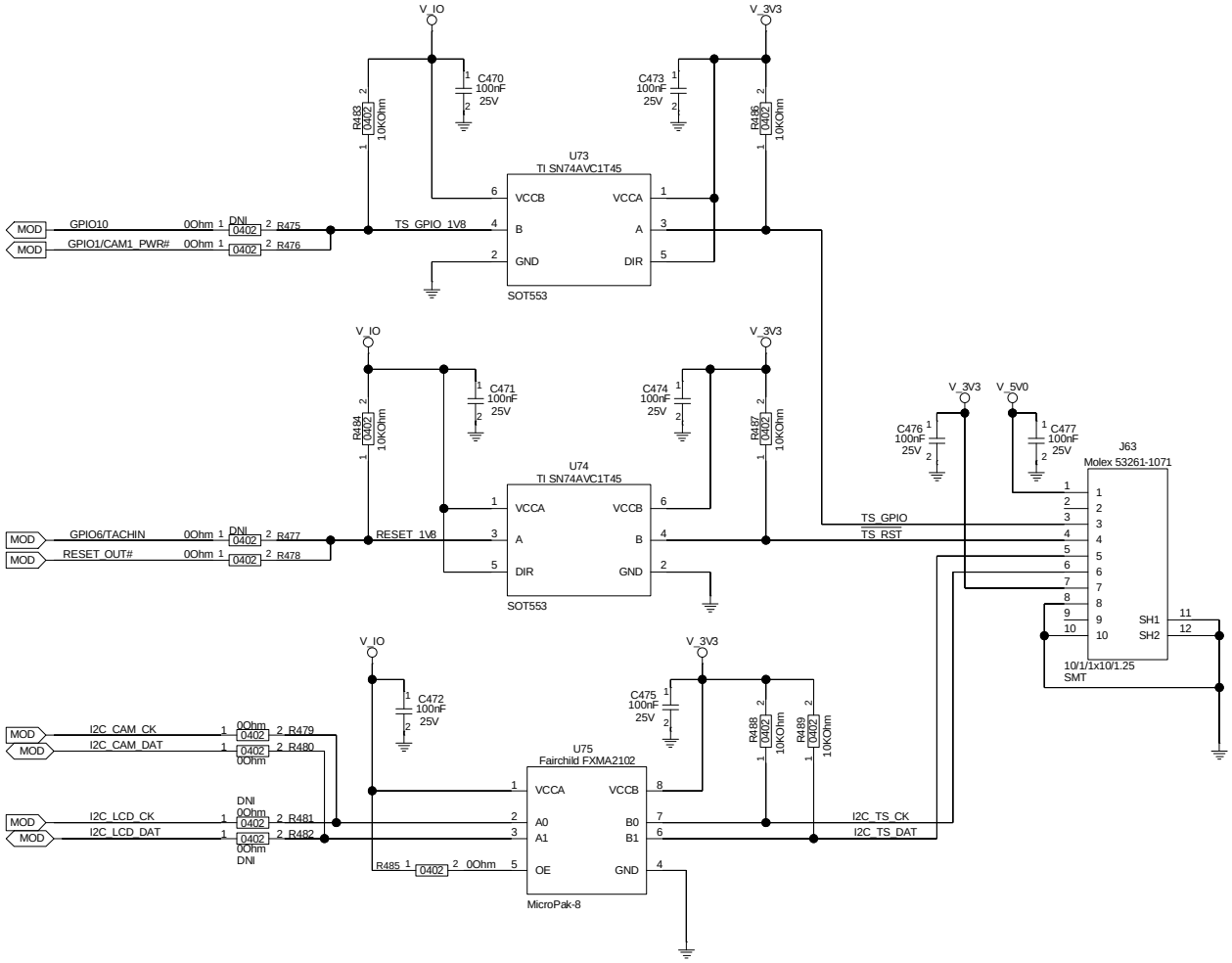
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4.3.4 I2C Interface to Touch Controller

Atmel is a popular choice for projected capacitance touch controllers. Atmel supplies USB and I2C drivers for the mXT1664S touch screen controller. Multi-touch is supported in the I2C driver but not, as of this writing apparently, in the USB driver.

The circuit shown below provides buffering and level translation for a SMARC interface to an I2C interfaced touch controller board . The Atmel mXT1664S can be configured for 1.8V I2C operation, and hence this voltage translation may not be necessary in a custom design. However, off-the-shelf touch controller modules may not be configured for 1.8V I/O (and the particular touch module behind this example was not). In any case, some buffering when cabling to an external board is not a bad thing to have, for robustness.

Figure 29 Touch Screen Connector – I2C Interface



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4.4 I2S Interfaces

4.4.1 General Information

The I2S (Inter IC Sound) bus specification was initially released in 1986 by Philips (NXP) and later revised in 1996. I2S is a synchronous serial bus used for interfacing digital audio devices such as Audio CODECs and DSP chips. Generally PCM audio data is transmitted over the I2S interface. The I2S bus may have a single bidirectional data line or two separate data lines. The signals constituting the I2S bus are a serial clock/ bit clock (output from the master), a left right clock (output from the master) that indicates the channel being transmitted and a single bidirectional data line or two data lines - one input and one output. A SMARC module can generally be configured as I2S master or slave. SMARC modules may support up to three independent I2S interfaces each having separate input and output data lines.

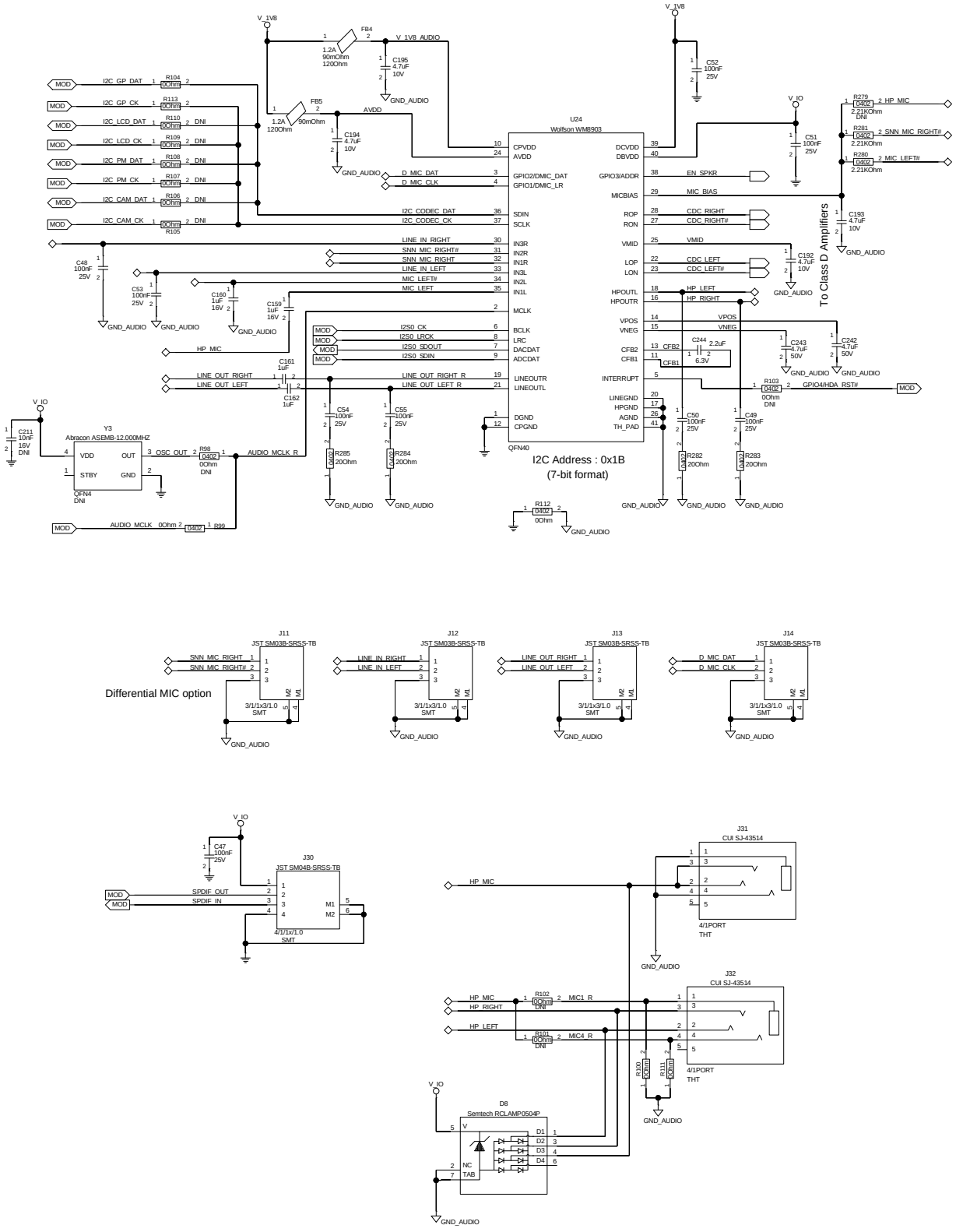
4.4.2 Wolfson Micro I2S Audio Example

An example of an I2S based audio circuit using the Wolfson Micro WM8903 CODEC and a pair of Wolfson class D amplifiers is given below.

The circuit uses a SMARC I2S interface for the audio PCM data, and a SMARC I2C interface to allow a path for software setup of registers within the CODEC.

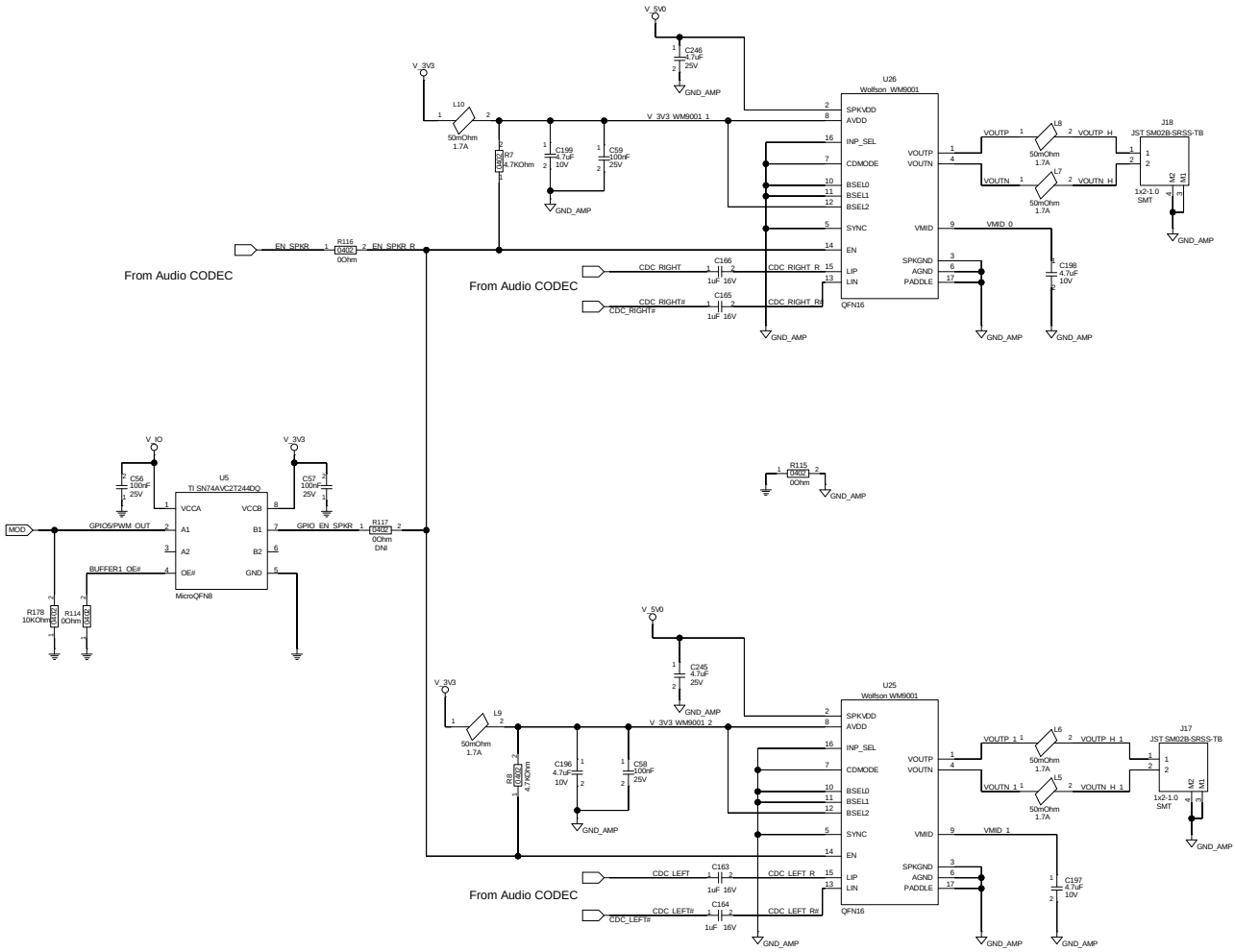
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Figure 30 I2S Audio CODEC: Wolfson Micro



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Figure 31 Audio Amplifier: Wolfson Micro



4.4.3 Texas Instruments TLV320AIC3105 I2S Audio Example

An alternative I2S audio CODEC example from TI is shown below. As in the Wolfson example, the I2S carries the PCM audio from and to the SMARC Module, and the I2C is used for chip setup parameters.

This example shows an option resistor that allows the SMARC audio MCLK (net AUDIO_MCLK) to be driven from the Carrier into the Module, rather than the other way around. This may be necessary with some Modules – check with your Module vendor.

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Figure 32 I2S Audio CODEC: Texas Instruments

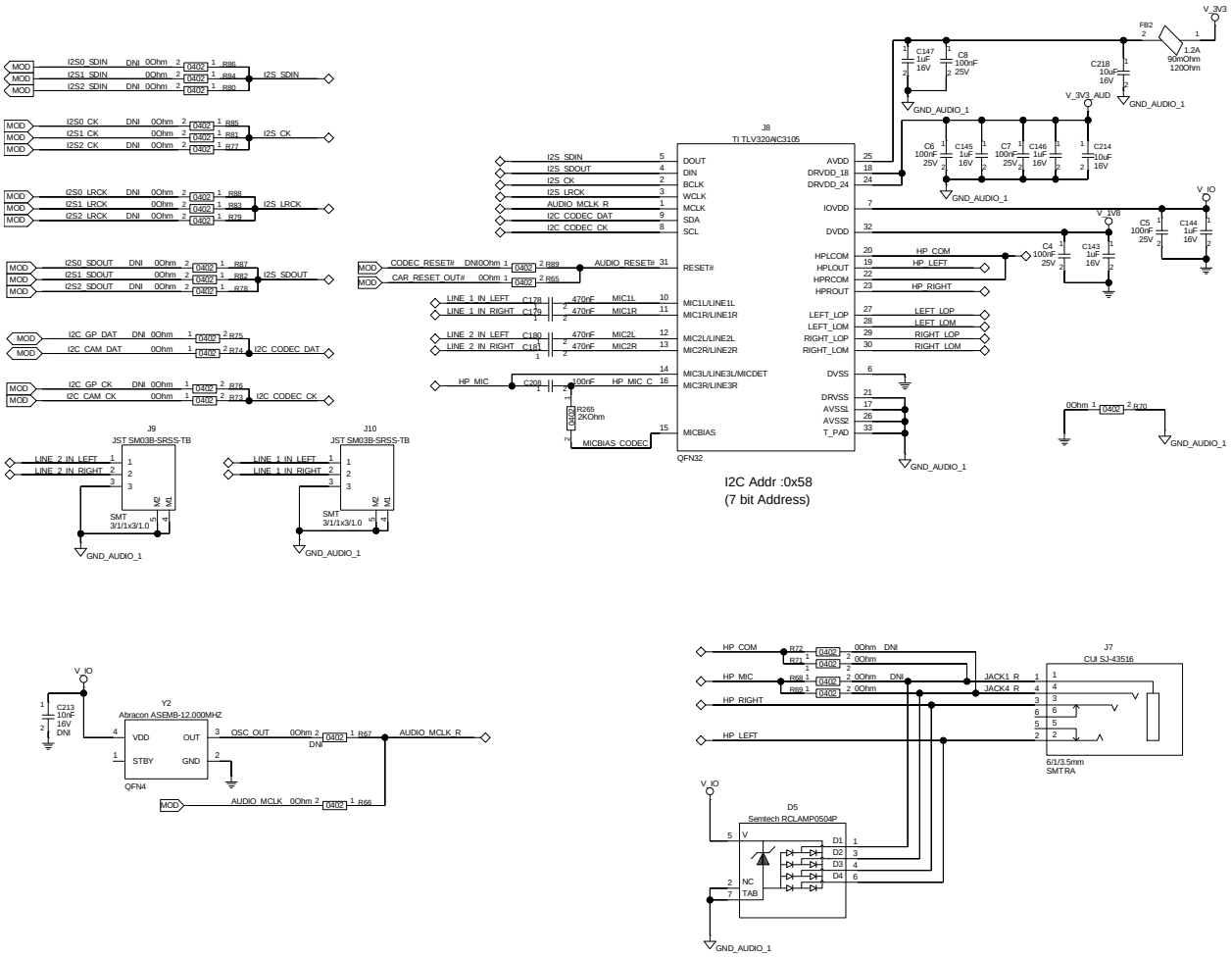
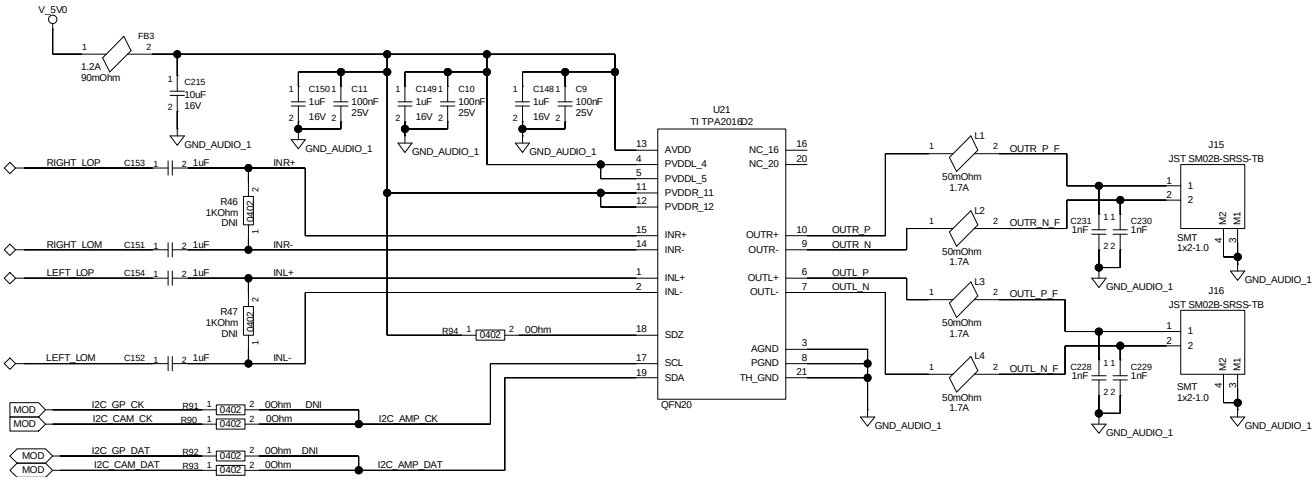


Figure 33 Audio Amplifier: Texas Instruments



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4.4.4 Intel High Definition Audio over I2S2

The SMARC specification does allow for an optional High Definition Audio implementation over the I2S2 pins (as alternate pin functions for those I2S pins). Refer to the SMARC specification for details on the pin mapping. The interface occurs at V_IO levels (typically 1.8V). The Intel HD Audio specification allows for 3.3V or 1.5V signaling, so SMARC systems using 1.8V I/O will require Carrier board level translation if interfacing to HD Audio CODECs.

Generally speaking, ARM devices implement audio using I2S and X86 devices using HD Audio. This distinction is blurring with the latest Intel X86 SOCs, some of which implement both multiple I2S and HD Audio interfaces (with the I2S interfaces running at 1.8V and the HD Audio at 1.5V ….).

High Definition Audio CODEC vendors include Cirrus, IDT, Realtek and others.

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4.5 SPI Interfaces

4.5.1 General

The SPI (Serial Peripheral Interface) is a full duplex synchronous bus supporting a single master and multiple slave devices. The SPI bus consists of a serial clock line (generated by the master); data output line from the master; a data input line to the master and one or more active low chip select signals (output from the master).

Clock frequencies from 1-100MHz may be generated by the master depending on the maximum frequency supported by the components in the system. SMARC Modules running a 1.8V I/O interface are generally limited to about a 50 MHz clock rate on this interface.

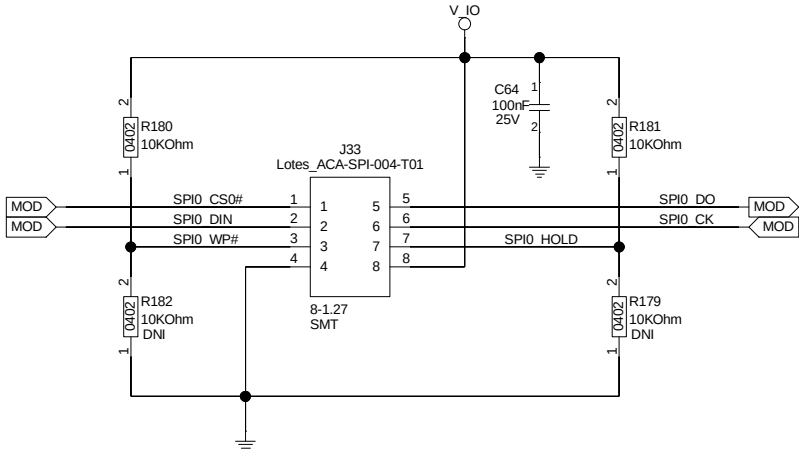
The SMARC Module will always be the SPI master. SMARC Modules may support a Carrier SPI Boot option.

4.5.2 SMARC Implementation

Each SPI device requires a chip select, a clock, a data in line and a data out line. The device I/O level must of course be compatible with the SMARC Module I/O level.

The Winbond W25Q64W is an example of a 1.8V I/O compatible SPI Flash device. The figure below illustrates a socket implementation for a SPI Flash memory.

Figure 34 SPI Flash Socket



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4.5.3 SPI Device Examples – 1.8V I/O

The table below shows a small sample of the devices available on the market with a 1.8V SPI interface. It is only a sample and is meant to give an idea of the type of devices available. Remember to check the software driver situation before settling on a particular device.

Table 6 SPI Device Examples - 1.8V I/O

Function	Device Description	Vendor	Vendor P/N
ADC	8-channel, 12-bit SAR ADC with temperature sensor	Analog Devices	AD7298
DAC	Quad, 16-bit nano DAC	Analog Devices	AD5686R
Flash Memory	64 Mbit SPI Flash memory	Winbond	W25Q64W
IO Expander	8-bit GPIO expander with integrated level shifters	Exar	XRA1404
Motion sensor	3-axis accelerometer	ST Micro	LIS33DE
Temperature Sensor	Digital thermometer ±2 °C resolution Range - 55°C to +120 °C	Dallas	DS1722
Touch Screen Controller	4 wire resistive touch screen controller	Texas Instruments	TSC2008-Q1
UART bridge	UART with 128 Word FIFOs and support for 9-bit multi-drop mode data filtering	Maxim	MAX3108

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4.6 CAN Bus

4.6.1 General

The CAN ("Controller Area Network") Bus is a differential half duplex data bus used in automotive and industrial settings. A CAN bus uses shielded or unshielded twisted differential pair wiring, terminated in the pair differential impedance of 120 ohms at the endpoints of the bus. Nodes on the bus are arranged in daisy-chain fashion, although stubs of up to 0.3 meters are allowed at each node. The standard allows data rates of up to 1 Mbps, with a maximum bus length of 40 meters at that rate. Various slower rates are defined, along with longer and longer bus lengths allowed as the data rates go down. A bus rate of 250 Kbps is in common use in automotive situations.

The two lines in a CAN twisted pair are referred to as CAN_H and CAN_L (for CAN High and CAN Low). There are two bus states on the CAN physical layer: the Dominant state and the Recessive state. In the Dominant state, CAN_L is pulled to GND through an open drain driver and CAN_H is pulled to the CAN Vcc through an open drain driver. In the Recessive state, CAN_L and CAN_H are not actively driven and they are pulled to a voltage of (Vcc / 2) by passive components. Hence the CAN bus is essentially a differential open-drain bus. On the system logic side of a CAN transceiver, the CAN Dominant state is a logic low and the Recessive state a logic high.

The CAN protocol has features important to a real time environment:

- Nodes are prioritized: CAN nodes are assigned an 11 bit identifier
  - The lower the ID number, the higher priority
- Latency time is guaranteed
- Data packets are limited to 8 bytes maximum
  - Higher level protocols take care of handling large data sets
- The bus has Multi-master capability
- There are error detection and signaling features

The CAN bus base standard is defined by ISO 11898-1:2003, available for a fee from the ISO (**www.iso.org**). There are some very helpful CAN application notes from Texas Instruments (a vendor of CAN MAC and transceiver devices) available for free. These include "***Introduction to the Controller Area Network (CAN)***", TI document number SLOA101A, and "***Controller Area Network Physical Layer Requirements***", document number SLLA270. The original CAN bus protocol definition by Bosch is also freely available on the web (***CAN Specification***, Version 2.0 © 1991 Robert Bosch GmbH).

Various connectors are used in CAN bus implementations. The use of DB-9 connectors is fairly common. The TI application note (SLLA270) referenced above has pin-out information for a couple of common CAN connector implementations.

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4.6.2 SMARC Implementation

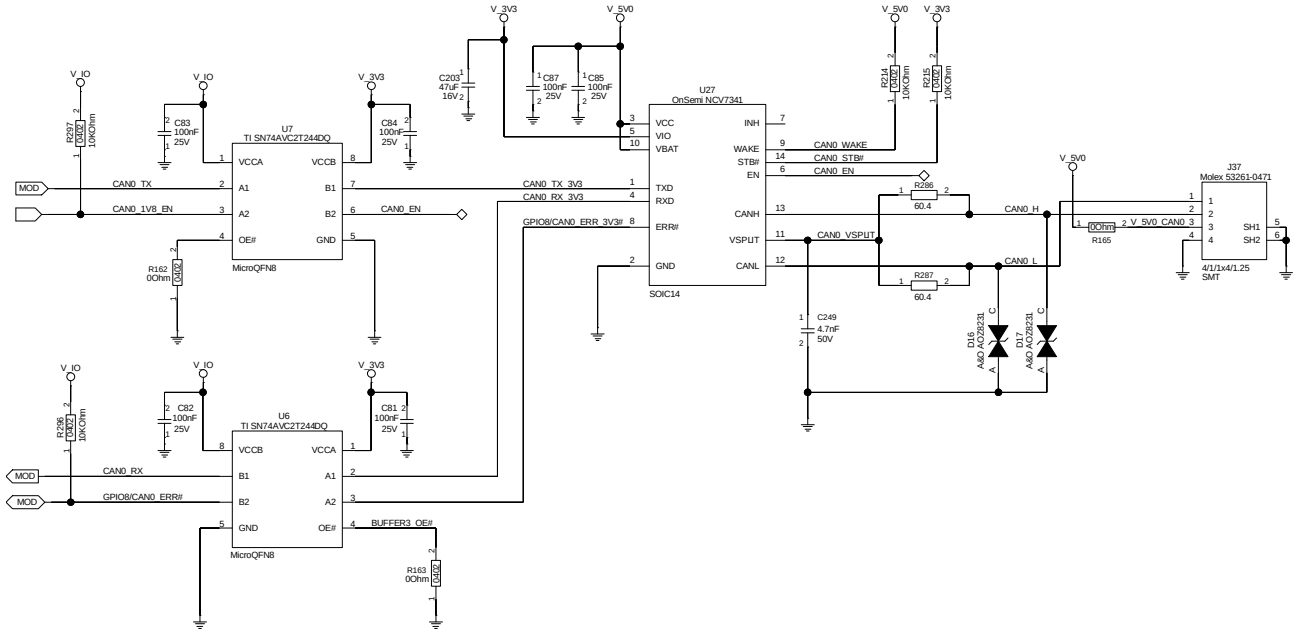
The SMARC specification allows for up to two logic level CAN ports. The ports run at the Module I/O voltage (typically 1.8V) and consist of an asynchronous CAN TX line and an RX line from and to the SMARC Module CAN protocol controller.

A Carrier based CAN transceiver is required to realize a SMARC system CAN implementation. CAN PHYs are available from Texas Instruments, On Semiconductor, NXP, Freescale, Microchip and numerous other vendors. The logic interface for CAN PHYs is typically suited for 3.3V logic I/O, so level translation is required if the SMARC Module is running 1.8V I/O.

Some (but not all) CAN transceivers include an error detect flag output pin. The SMARC specification suggests that SMARC GPIO8 be used for CAN0 error signaling, and GPIO9 for CAN1. Software modifications may be necessary to take advantage of the error signaling.

A SMARC Carrier board CAN transceiver implementation is shown below. The connector shown is a small form factor device, suitable for a demonstration board but maybe not suitable for a harsh – environment CAN application. This example shows two 60 ohm terminations (or 120 ohms across the CAN pair). This is appropriate only if the node is an end-point, and intermediate nodes should not be terminated.

Figure 35 CAN Bus Implementation



4.6.3 Isolation

Some Can transceiver application notes show optical isolation between the CAN protocol controller and the CAN transceiver. See, for example, NXP (Philips) application note AN96116 for the PCA82C250 CAN transceiver. They suggest using the 6N137 optical transceivers. Be careful to take into account the I/O levels and current sink / source requirements of the various devices in the chain.

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4.7 S/PDIF Interface

S/PDIF, or the “Sony/Philips Digital Interconnect Format”, is a digital audio interface standard supporting consumer and professional applications. A single wire or channel is used in each direction (audio out and in). Digital audio data and clock data are biphase encoded (also known as differential Manchester encoding) such that there are one to two level transitions per bit. This allows the signals to be AC coupled, or used with optical media. Clock recovery is achieved at the receiving end using PLL based clock recovery techniques. S/PDIF is defined in the IEC 60958-3:2006 standard.

S/PDIF signals can be transmitted over a 75ohm coaxial cable through RCA connector or to a fiber optic cable by TOSLINK (“Toshiba Link”) optical connector. The S/PDIF supports various data formats and rates. The most common format uses a 48 KHz sampling frequency and uses up to 24bits per sample. Multiple channels (left and right, or quad) are supported on the single link, in successive fields. Alternatively, sampling rates of 32 KHz or 44.1 KHz are sometimes used. In most of the consumer applications stereo audio is carried with a resolution of 20 bits/sample.

S/PDIF support on SMARC Modules is an optional feature of the SMARC standard. If supported, the S/PDIF signals are logic level signals at the Module V_IO (usually 1.8V) level. Either a passive component network or an optical transceiver are required on the Carrier, as illustrated below, to make use of S/PDIF.

Figure 36 SPDIF Implementation: Optical

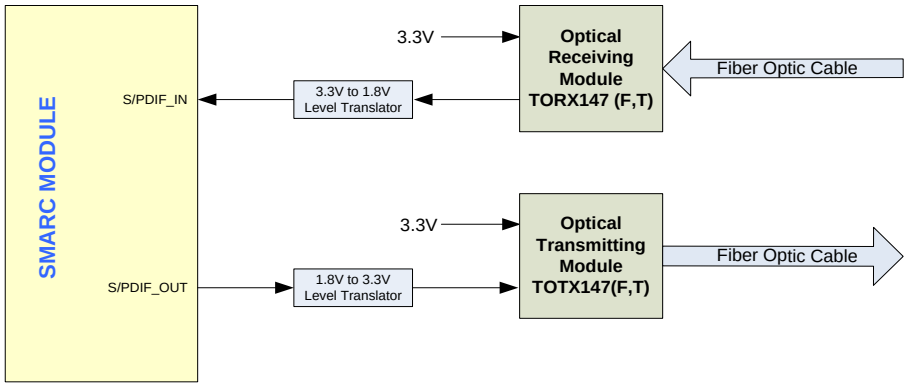
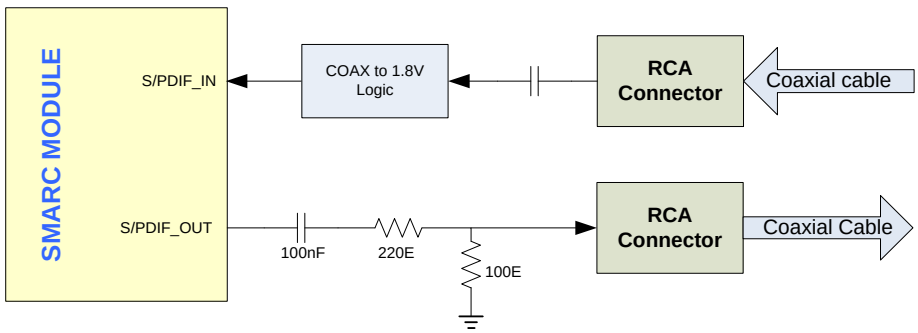


Figure 37 SPDIF Implementation: Coaxial



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5 HIGH SPEED SERIAL I/O INTERFACES

5.1 USB

5.1.1 General

The USB (Universal Serial Bus) is a hot-pluggable general purpose high speed I/O standard for computer peripherals. The standard defines connector types, cabling, and communication protocols for interconnecting a wide variety of electronic devices. The USB 2.0 Specification defines data transfer rates as high as 480 Mbps (also known as High Speed USB). A USB host bus connector uses 4 pins: a power supply pin (5V), a differential pair (D+ and D- pins) and a ground pin. Additionally a fifth pin, USB ID (mostly used in devices supporting USB-OTG), may also be used which indicates whether the device operates in Host mode or a Client/Device mode.

SMARC Modules support up to three independent USB 2.0 busses, designated USB0 to USB 2. Of these, SMARC USB0 can be configured as a host, client or OTG port. OTG operation is optional. SMARC USB1 and USB2 are always hosts. A USB host is usually the “smarter” device – a host computer for example. A USB “client” is usually a peripheral device, such as a camera, printer or mass storage device. USB clients are often based on micro-controllers that include USB client interface hardware.

At the time of this writing, USB 3.0 Super Speed (5 Gbps signaling) operation is not supported on standard SMARC Modules. Two USB 3.0 Super Speed channels are mentioned in the SMARC specification as a possible design specific use of the SMARC Alternate Function Block.

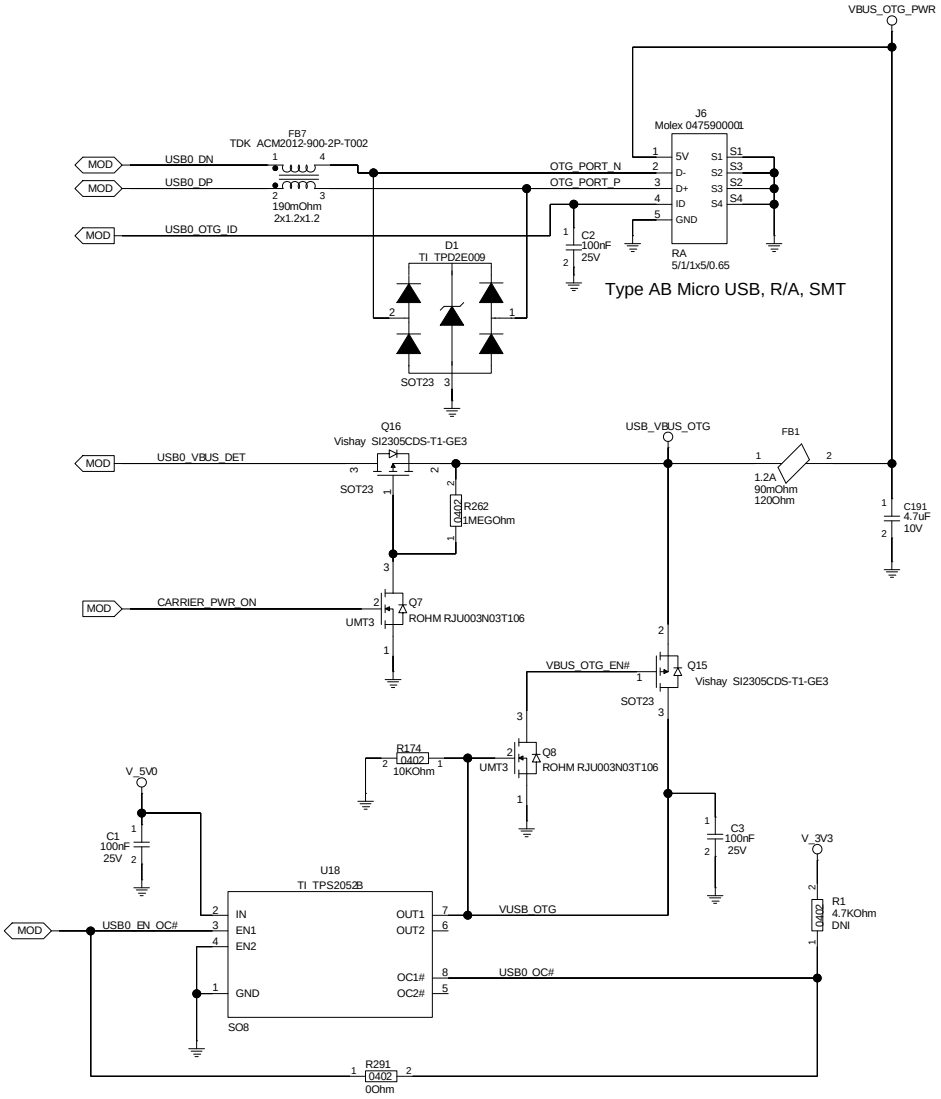
5.1.2 USB0 Client / Host Direct From Module

The figure below shows a USB-OTG implementation on the USB0 port terminated on a micro USB Type A/B connector

The ESD diodes should be placed close to the connector, and the USB traces routed as differential pairs in “no stub” fashion – the traces should go through the pads of the ESD protection devices, without introducing a stub. If the client device is bus powered, the Carrier can supply 5V, 500mA power to the client device. The Module USB0_EN_OC# signal controls the power switch and current limiter, the Texas Instruments TPS2052, which in turn supplies power to a bus-powered client device. Per the USB specification, bus powered USB 2.0 devices are limited to a maximum of 500 mA. The TPS2052 limits the current and can stand an indefinite short circuit to GND. The current limiting is somewhat imprecise, and kicks in between 500 mA and 1A.

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Figure 38 USB0 Client / Host Direct From Module



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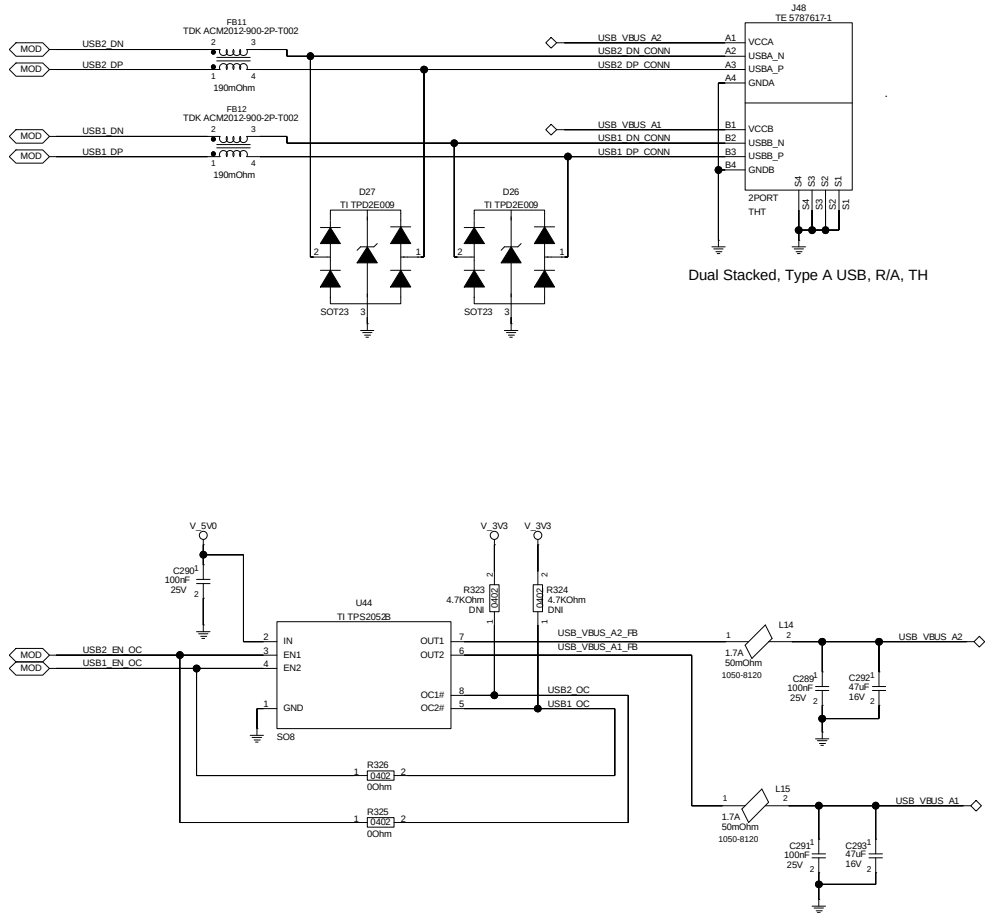
5.1.3 USB1 and USB2 Host Ports Direct from Module

Carrier board implementation of USB host ports from SMARC USB1 and 2 is straightforward. An implementation of a dual USB Type A Host port header is shown in the figure below.

The ESD diodes should be placed close to the connector, and the USB traces routed as differential pairs in “no stub” fashion – the traces should go through the pads of the ESD protection devices, without introducing a stub.

If the target USB devices are “down” on the Carrier, then much or all of this circuit may be omitted. The SMARC USB pairs are routed directly to the target device. The ferrite choke in the USB lines, the ESD diodes, and the TPS2052 power switch and associated passives may be eliminated. However, in some cases, it is desirable to have the capability to “power cycle” a USB peripheral under software control. If this is the case, it might be desirable to retain the TPS2052 power switch, or a similar device for 3.3V power switching, with the power control function performed by the USB1_EN_OC or USB2_EN_OC, as appropriate.

Figure 39 USB1 and USB2 Host Ports Direct From Module



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5.1.4 USB Hub On Carrier

Additional USB ports may be implemented on a SMARC Carrier board using a USB hub to interface with one of the SMARC USB ports (usually USB1 or USB2, saving the SMARC USB0 for possible client or OTG use). The USB 2.0 compliant (and 480 Mbps capable) family of hubs from Microchip / SMSC (**www.microchip.com** or **www.smsc.com**) is recommended. Parts with 2,3,4 or 7 downstream ports are available.

A Carrier hub implementation example using the 7 port SMSC USB2517i is shown in the two figures below. There are 3 configuration straps on this particular SMSC hub, designated CFG_SEL[2] through CFG_SEL[0]. The options need to be considered carefully. The example schematic has the 2:0 configuration straps set to binary 110, which, per the SMSC data sheet, sets the hub to the following:

- SMSC hub defaults in effect
- Other strap options disabled
- Hub LED pins configured to indicate USB speed
- Individual port power switching
- Individual port over-current sensing
- External EEPROM not used
- External I2C interface not used

Although the sample schematic shows the external EEPROM and I2C interfaces, they are not used. Note that the “DNI” designation on the schematic stands for “Do Not Install” – i.e. the part is not loaded, in this example.

If implementing such a hub (or any piece of configurable silicon), it is wise to keep your options open and have all strap options accessible for re-configuration by option resistors or other means. It may keep you out of trouble and save a board spin.

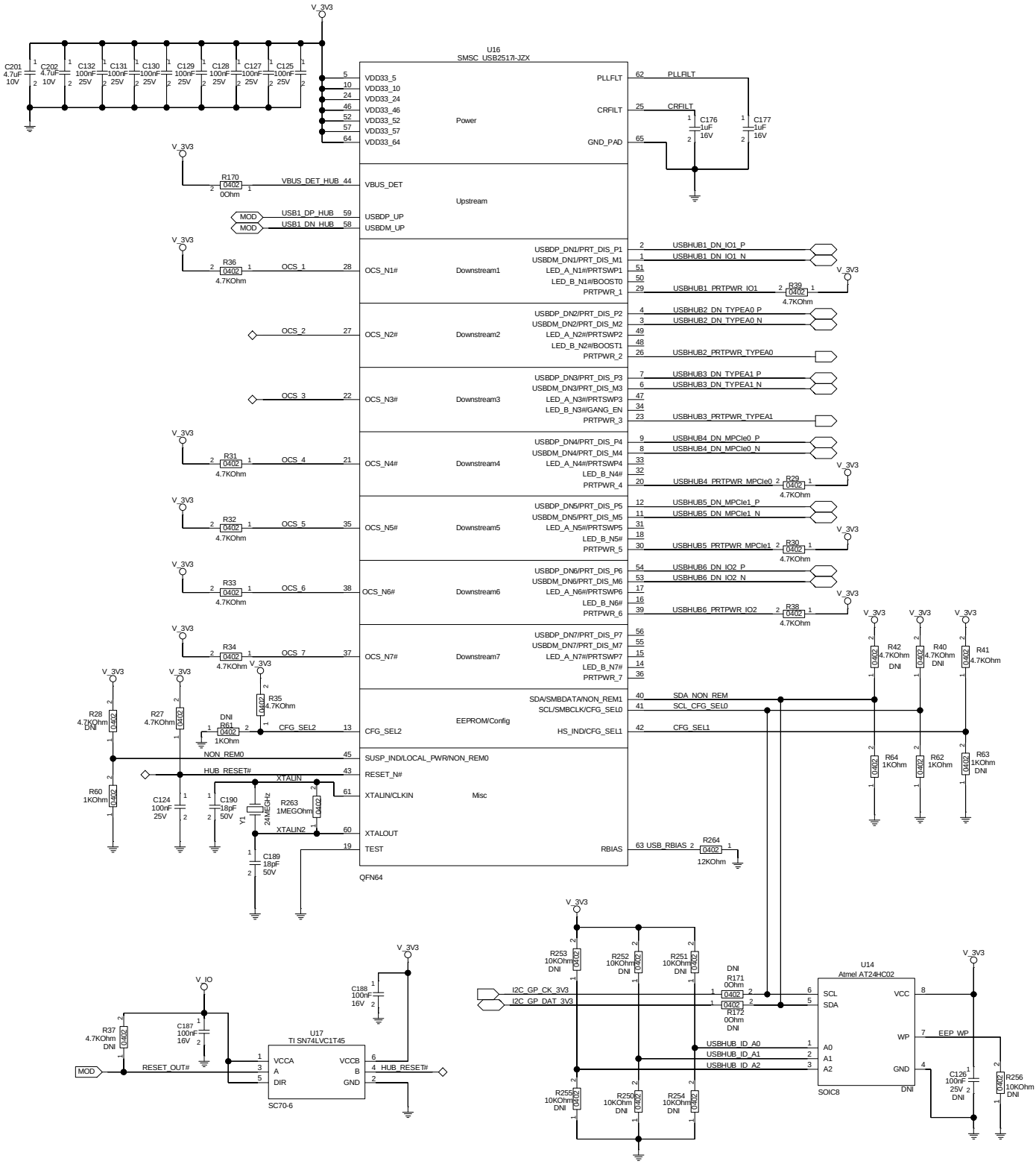
Since the hub operates at 3.3V, the signals from the SMARC Modules that are at 1.8V (RESET_OUT# and the I2C_GP_ signals, if used) levels need to be level shifted to 3.3V to interface to the hub.

In this example, there are 7 down-stream ports. Two of them are used for off-Carrier cabled connections. These nets are designated with USB_HUB2_ and USB_HUB3_ prefixes. Since they are used for cabled connections, these are protected by a USB power switch (U19, in the 2nd figure below). Four of the other hub ports are assumed to go to on-Carrier destinations (such as mini-PCIe cards, or a touch controller, or other on-Carrier USB peripheral). One of the 7 down-stream ports is not used.

The behavior of a USB port, at least initially, may differ slightly depending on whether that port is direct from the SMARC Module or whether the port is through a hub. With software adjustments, or “tweaking”, the direct and through – the –hub ports may appear virtually identical to a client device.

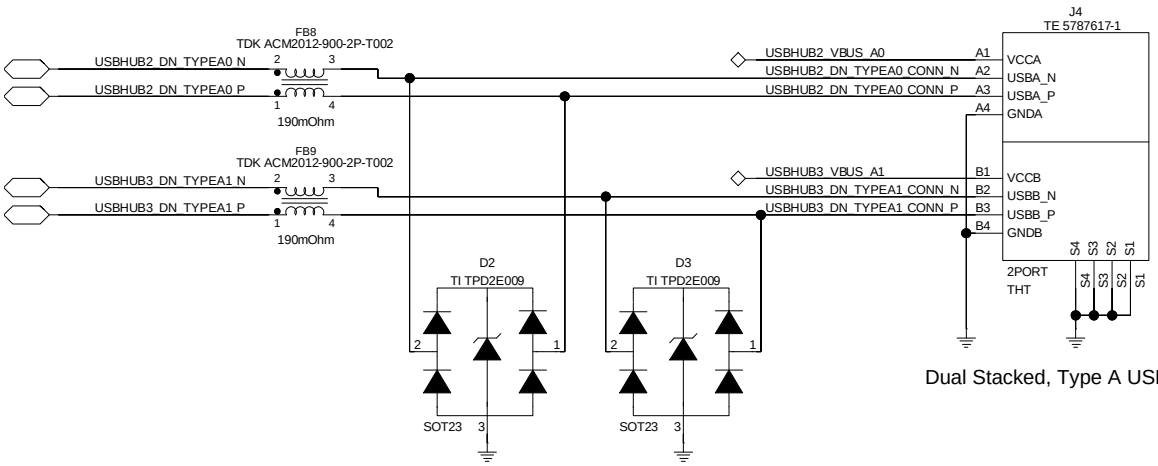
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Figure 40 USB Hub (1 of 2)

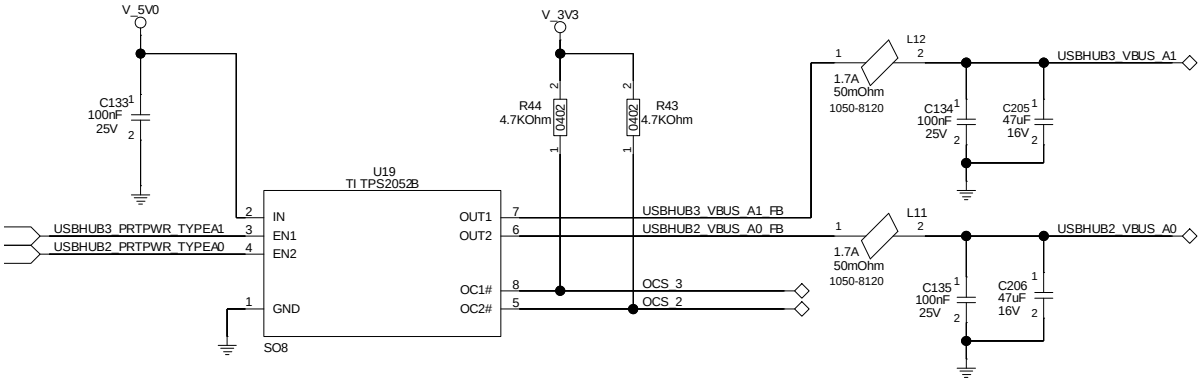


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Figure 41 USB Hub (2 of 2)



Dual Stacked, Type A USB, R/A, TH



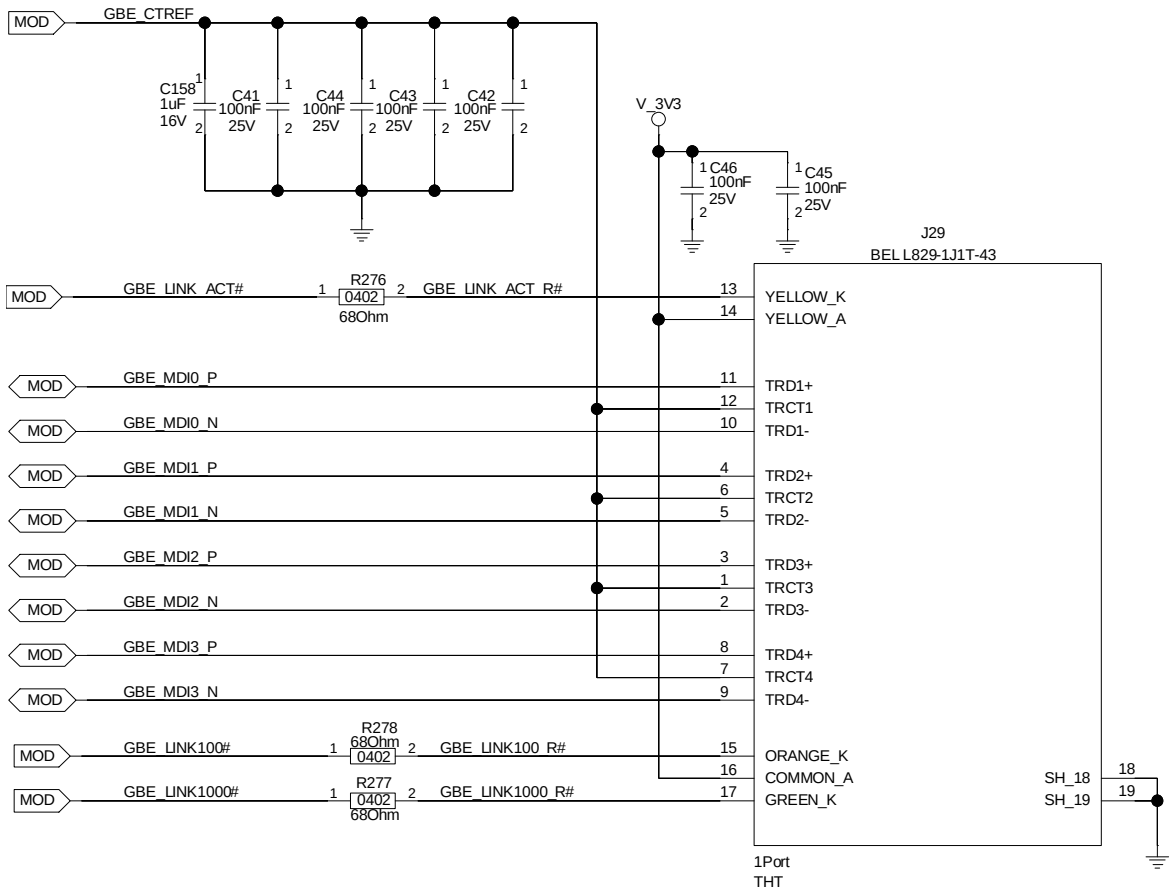
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5.2 GBE

5.2.1 GBE Carrier Connector Implementation Example

SMARC Modules include GBE MAC / PHYs but do not include the isolation magnetics. If the SMARC GBE is used, then the Carrier must include GBE compatible magnetics with 1:1 turn ratios. Usually RJ45 jacks with integrated magnetics are used. An example is given in the following figure.

Figure 42 GBE without POE



RJ45 with Magnetics, R/A, TH

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5.2.2 GBE Mag-Jack Connector Recommendations

SMARC GBE MAG-Jack (magnetics integrated into an RJ45 jack housing) should meet the following general characteristics:

- The turn ratios should be 1:1
- An integrated common mode choke should be included
- Termination resistors on the primary side (i.e. the Ethernet cable side) should be included
- The secondary side transformer center-taps may be tied together or may be brought out separately. If they are brought out separately, they are tied together on the Carrier PCB.
- The secondary side center-taps need to be tied to the SMARC GBE_CTREF voltage, with bypass capacitors connected to GND.

Mag-Jacks (and RJ45 jacks in general) are available in ***tab-up*** and ***tab-down*** configurations. The pin order on the Mag-Jack reverses between the tab-up and tab-down configurations. One of them may work better for your layout than the other (although since only 4 pairs are involved, this may not be a major concern). Tab up is generally more common; tab down parts do exist; most tab down parts target low-profile needs in which part of the Mag-Jack connector height is hidden by a Carrier PCB cutout.

Table 7 Recommended Gigabit Ethernet Connectors with Magnetics

Mfg	Mfg P/N	Description
Bel Fuse	L829-1J1T-43	Tab Up, 1:1 turns ratio, 3 LEDs, 0.950” depth
Pulse	JK0-0136NL	Tab Up, 1:1 turns ratio, 3 LEDs, 1.30” depth
Tyco	1840437-1	Tab Down, 1:1 turns ratio, 3 LEDs, special low profile feature
Wurth	7499111447	Tab Up, 1:1 turns ratio, 4 LED

Note that POE (Power Over Ethernet) capable jacks are slightly different – they have extra pins to bring the POE power into the system. A GBE POE jack may be used in a non-POE system, but not the other way around. A GBE POE example is given later in this Design Guide.

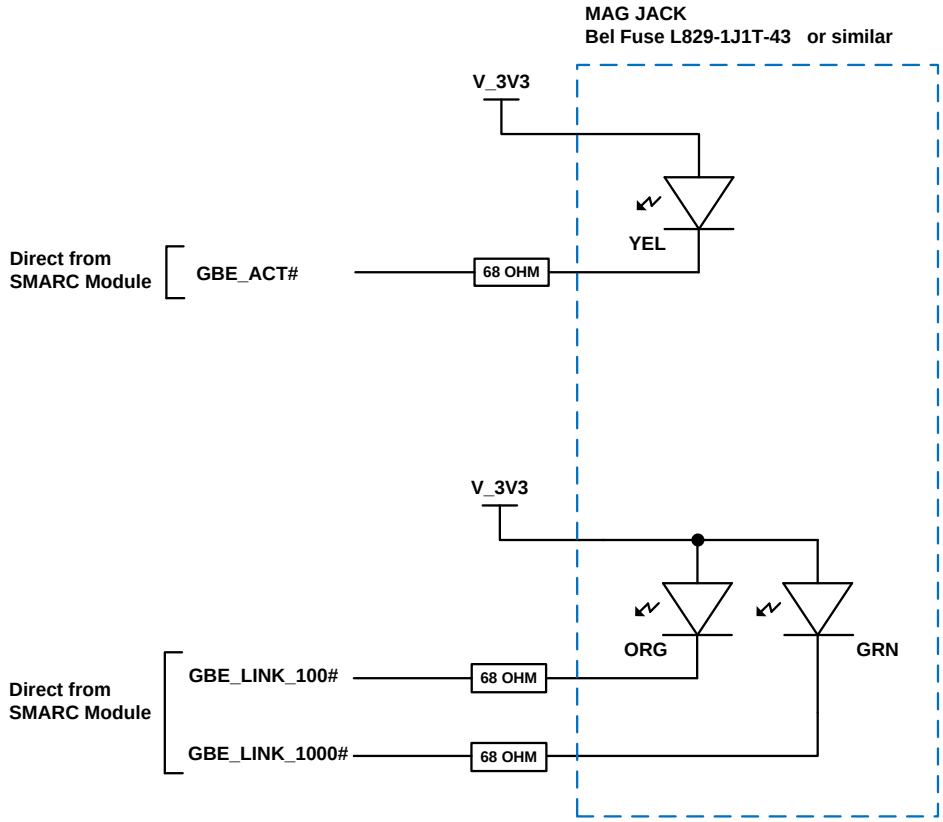
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5.2.3 GBE LEDs

Mag-Jack LED implementations vary widely. There does not seem to be any common standard, so be aware.

The SMARC GBE status LED outputs are open drain outputs that are capable of sinking a minimum of 24 mA. They may be connected directly to the cathode of GBE status LEDs as shown in the following figure. Make sure the resistors can handle the expected power dissipation.

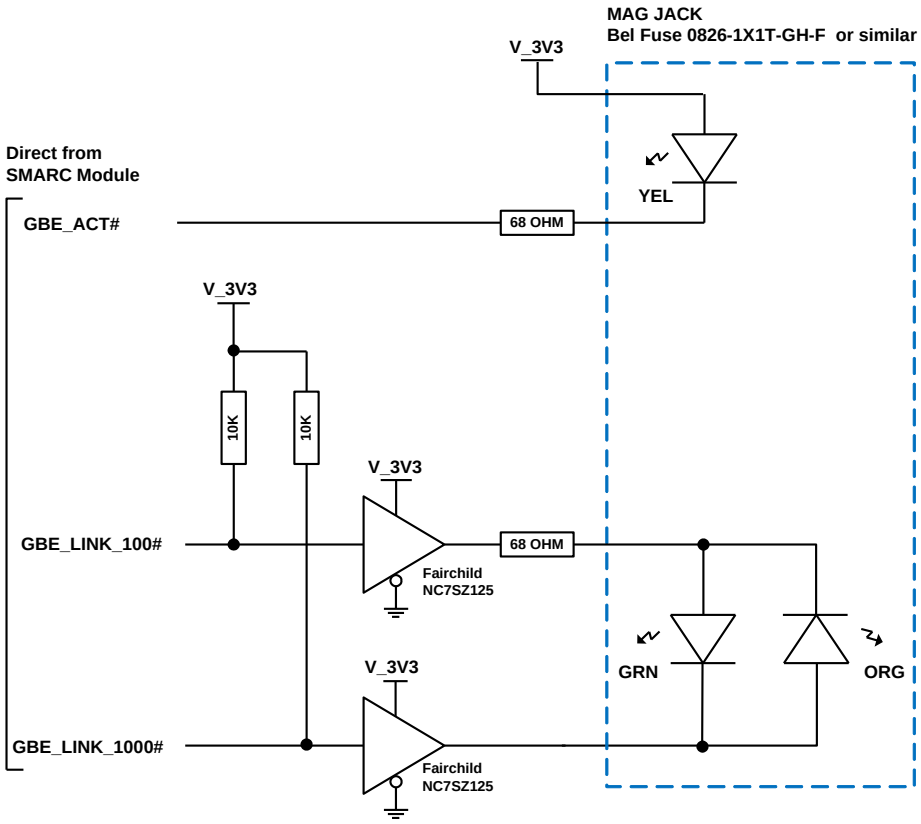
Figure 43 GBE LED Current Sink



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Some integrated GBE Mag Jacks have a pair of opposing (cathode to anode) diodes, as shown in the figure below. In this case, Carrier board buffers are required, as the SMARC Module status LED lines can sink current but can not source it.

Figure 44 GBE LED Current Sink / Source



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5.3 PCIe

5.3.1 General

PCI Express (or PCIe) is a scalable, point-to-point serial bus interface commonly used for high speed data exchange between a PCIe host, or root, and a target device. It is scalable in the sense that there may be link widths, per the PCIe specification, that are x1, x2, x4, x8, x16 or x32. SMARC currently calls out only x1 operation. Up to 3 PCIe x1 links may be implemented on a SMARC Module. There are 3 generations of PCIe defined, with each successive generation offering a speed increase, per the table below. The PCIe generation that may be supported on a particular SMARC Module is design and SOC dependent.

Table 8 PCIe Data Transfer Rates

PCIe Generation	Link Speed (x1 link)	Encoding / Overhead	Net Data Transfer Rate
1	2.5 GT/s	8b/10b 20%	250 MB/s
2	5.0 GT/s	8b/10b 20%	500 MB/s
3	8.0 GT/s	128b / 130b 1.54%	985 MB/s

PCI Express is defined in a series of documents maintained by the PCI Special Interest Group (**www.pci-sig.org**). The three most important documents to obtain are the Base Specification, the Card Electromechanical (CEM) Specification (which describes slot cards) and the Mini Card Electromechanical Specification (which describes the small format cards commonly referred to as Mini-PCIe cards).

The three possible PCIe links on a SMARC Module are designated with net name prefixes PCIE_A_, PCIE_B_ and PCIE_C_. Each of the three has the following signal set (x in the table below designates A, B or C).

Table 9 SMARC PCIe Signal Summary

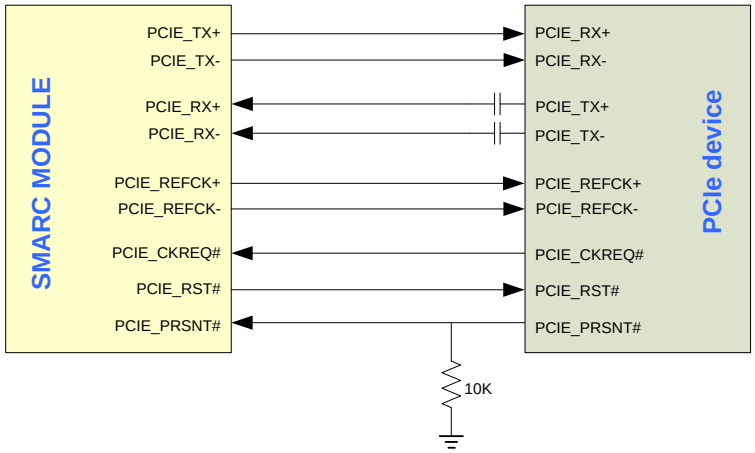
Signal	Description	Signal Type	Notes
PCIE_x_TX+ PCIE_x_TX-	Data out of Module	Differential pair	Capacitively coupled – on Module
PCIE_x_RX+ PCIE_x_RX-	Data into Module	Differential pair	Capacitively coupled – off Module
PCIE_x_REFCK+ PCIE_x_REFCK-	Reference clock out of module	Differential pair	No caps needed
PCIE_x_CKREQ#	Enables PCIE clock if pulled low on Carrier.	Single ended	Tie to GND through resistor on Carrier if not used by Carrier PCIe target device.
PCIE_x_RST#	Active low output to reset the PCIE_x device	Single ended	
PCIE_PRSNT#	Input to Module to signal the presence of a Carrier PCIe device		Tie to GND through resistor on Carrier if not used by Carrier PCIe target device.

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5.3.2 PCIe x1 Device Down on Carrier

An example of a PCIe x1 “device down” on the Carrier is shown below. Coupling caps on the SMARC PCIe TX and PCIe reference clock pairs are not needed on the Carrier. Coupling caps on the SMARC PCIe RX pair (TX pair from the Carrier PCIe device) are needed. They should be placed close to the Carrier device PCIe TX pins. Use 0402 package 0.1 uF X7R or X5R dielectric discrete ceramic capacitors. Do not use a capacitor array. Place the parts in a way to preserve the symmetry of the differential pair. Usually they are placed close to the Carrier device TX pins to avoid a via transition.

Figure 45 Interfacing a PCIe x1 Carrier Board Device

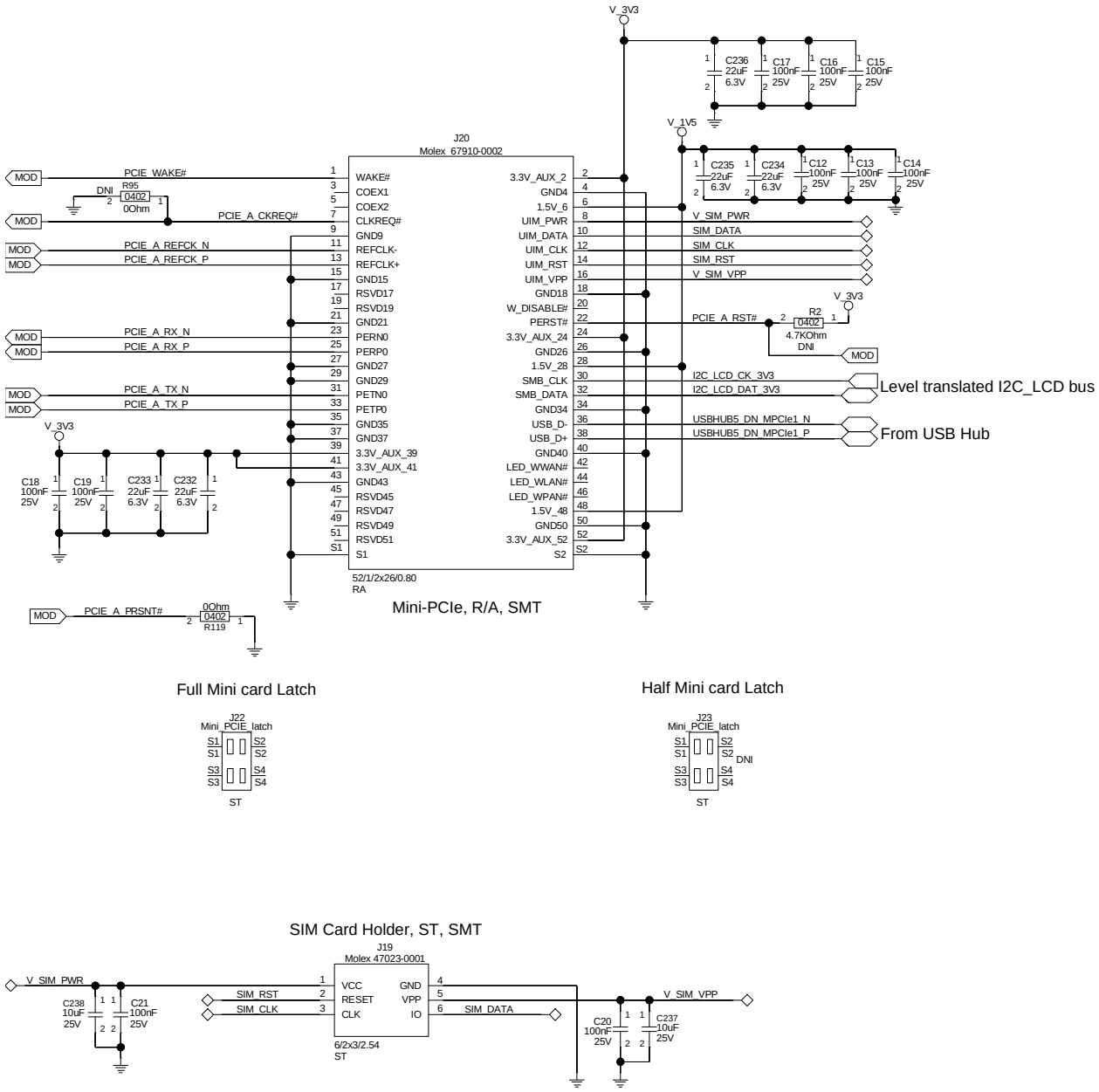


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5.3.3 Mini-PCIe

A SMARC Mini-PCIe implementation example is shown below. Mini-PCIe cards are defined to have pins for PCIe x1 and also a USB interface. A given card generally uses only one or the other. If you know exactly what Mini-PCIe card you plan to use, it is possible to omit either USB or PCIe. Generally, Mini-PCIe 802.11 WiFi cards use the PCIe interface and cellular modem cards use the USB interface.

Figure 46 Mini-PCIe Slot



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5.4 SATA

5.4.1 General

Serial ATA (or SATA) is a high speed point to point serial interface that connects a host system to a mass storage device such as rotating hard drive, solid state drive or an optical drive. Data and clock are serialized onto a single outbound differential pair and a single inbound pair. Data link rates of 1.5, 3.0 and 6.0 Gbps are defined by the SATA specification. A SATA link is AC coupled, but the coupling capacitors are defined in the SMARC specification to be on the Module, for both SATA transmit and receive pairs.

Table 10 SATA SSD Form Factors

Format	Notes
IC (chip level)	Smallest form factor. Densities to 64GB.
mSATA MO-300	Small form factor SATA module, defined in the SATA specification (search for “mSATA” in the specification). SLC and MLC versions are generally available. The mSATA form factor is roughly 30mm x 51mm x 3.5mm (see the specification for exact dimensions).
Slim SATA MO-297	Small form factor solid-state SATA modules that use a standard SATA connector (7 pin data / GND section and 15 pin power section). The connector is compatible with the connector used on larger format (2.5”) hard drives used in PC systems. Available in SLC and MLC versions. Form factor is defined by JEDEC MO-297.
CFast	Removable card format with SSD interface; similar to popular Compact Flash (parallel interface) cards. Form factor is roughly 36mmx 43mm x 3.6mm.
SSD 1.8”	Solid State Disk in traditional 1.8” format that was originally used for rotating drives
SSD 2.5”	Solid State Disk in traditional 2.5” format that was originally used for rotating drives

Table 11 SATA SSD Vendors

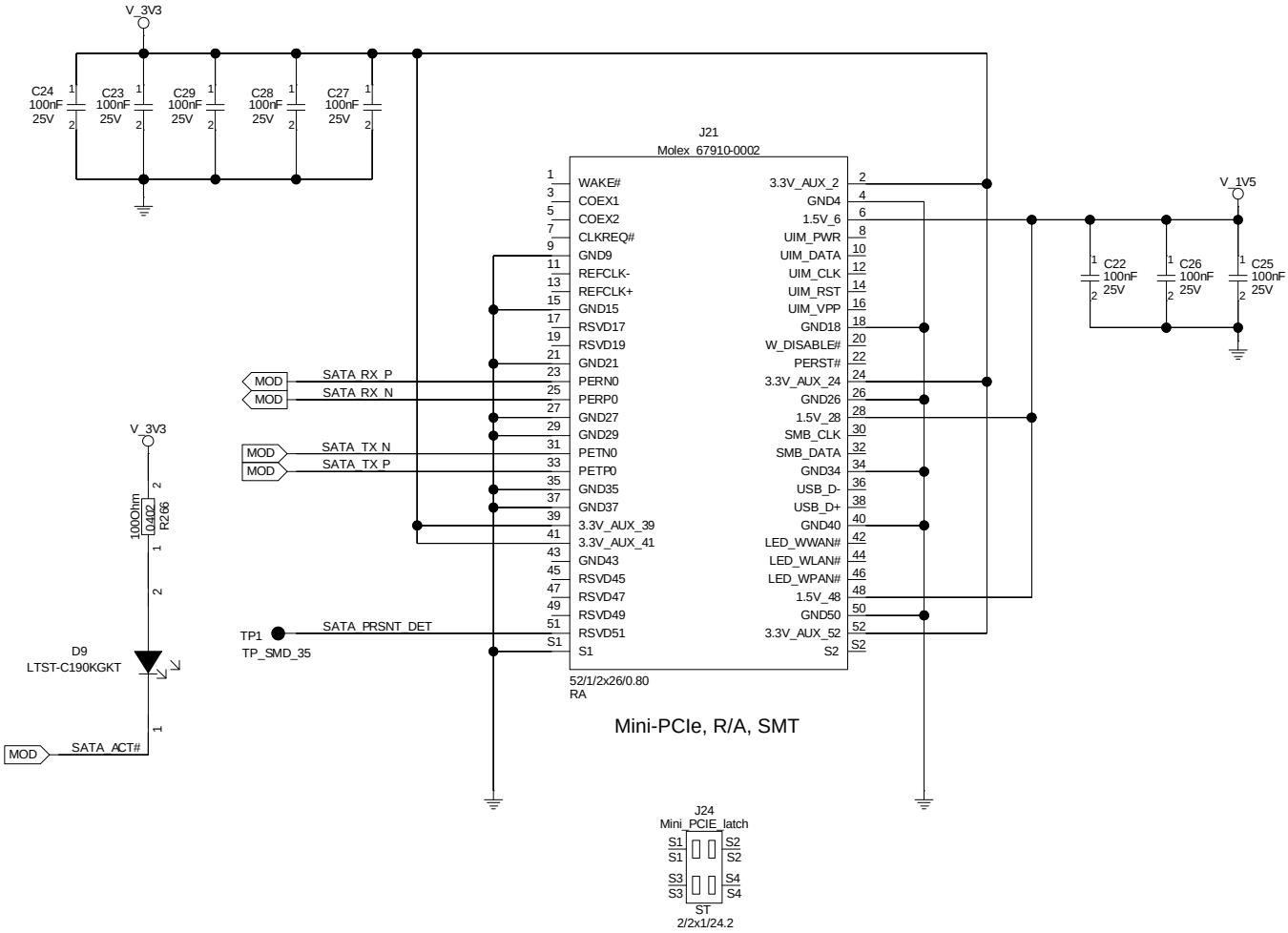
Vendor	Link	SATA Products
Greenliant	**www.greenliant.com**	Chip-level SLC and MLC NAND flash with SATA interface.
Innodisk	**www.innodisk.com**	mSATA / MO-300 Slim SATA / MO-297 CFast SSD 2.5”
Intel	**www.intel.com**	mSATA / MO-300 SSD 1.8” SSD 2.5”
SMART Modular	**www.smartm.com**	mSATA / MO-300 Slim SATA / MO-297 SSD 1.8” SSD 2.5”
Swissbit	**www.swissbit.com**	mSATA / MO-300 Slim SATA / MO-297 CFast SSD 1.8” SSD 2.5”
Transcend	**www.transcend-info.com**	mSATA / MO-300 Slim SATA / MO-297 SSD 1.8” SSD 2.5”
Virtium	**www.virtium.com**	mSATA / MO-300 Slim SATA / MO-297 SSD 1.8” SSD 2.5”

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5.4.2 mSATA / MO-300

A popular SATA form factor for SMARC systems is the mSATA / JEDEC MO-300. This is physically the same as a mini-PCIe card, and uses the same Carrier socket, but the mini-PCIe pinout is re-purposed for SATA use. A schematic example is shown below. The pin names within the J21 connector box outline below are the mini-PCIe pin names. The net connections outside the box show the appropriate connections for mSATA / MO-300 SATA use. Coupling capacitors are not needed on the Carrier SATA TX and RX pairs. mSATA / MO-300 SATA is described in the ***Serial ATA Revision 3.1*** specification document – search for "mSATA".

Figure 47 mSATA / MO-300



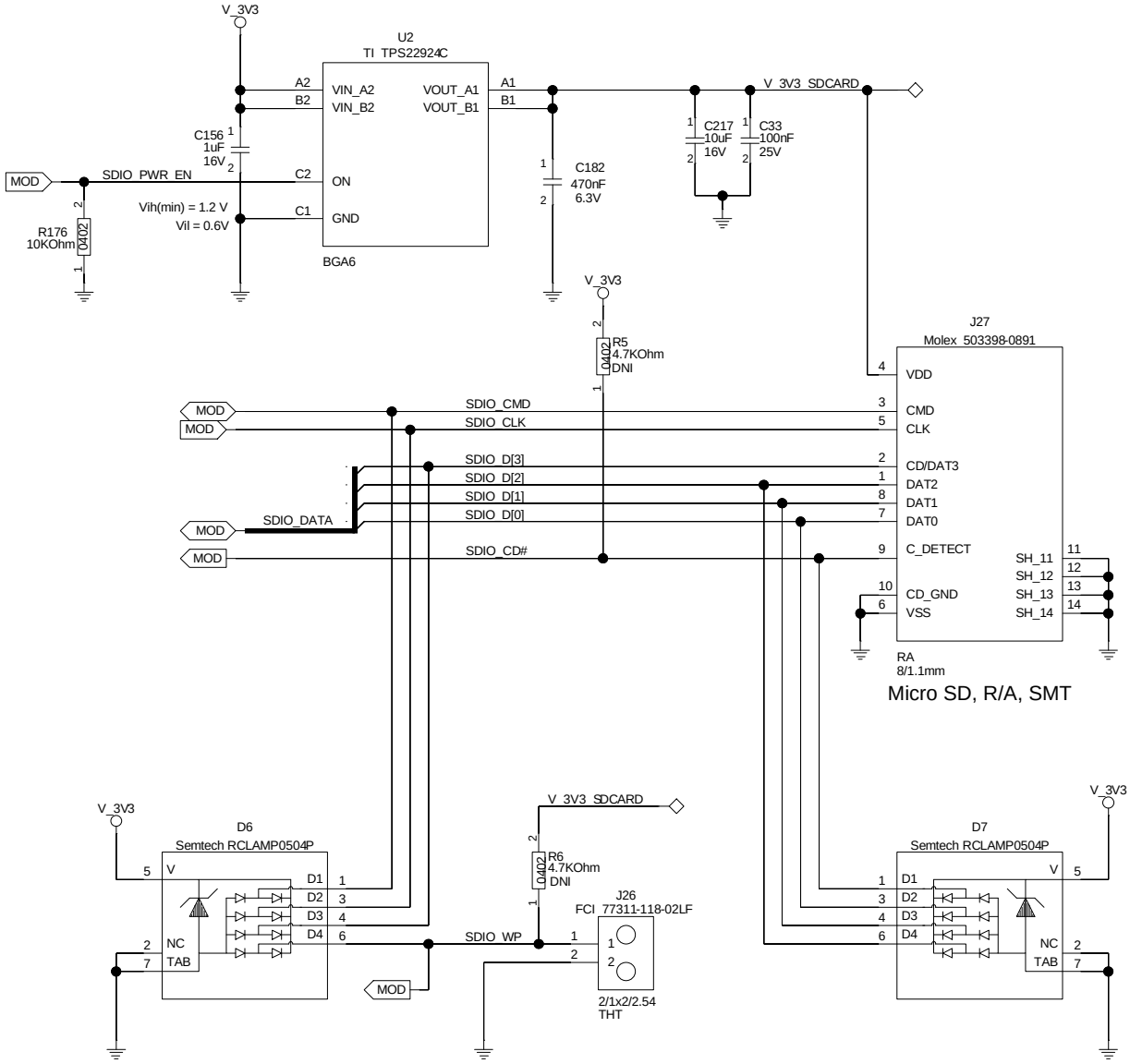
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6 MEMORY CARD INTERFACES

6.1 SD Card

The SD (Secure Digital) Card is a non volatile memory card format used as mass storage memory in portable devices. The SD standard is maintained by the SD Card Association. SMARC Modules support SD cards over the SMARC SDIO interface. The interface may be used in a 4 bit or 1 bit mode. If used in 1 bit mode, the least significant bit (SDIO0) should be used. Most SMARC Modules offer a SDIO BCT boot and an SDIO OS boot. Since SD cards can (usually) be inserted and removed by the user, it is important to implement ESD protection on all the SD lines.

Figure 48 Micro SD Card Implementation



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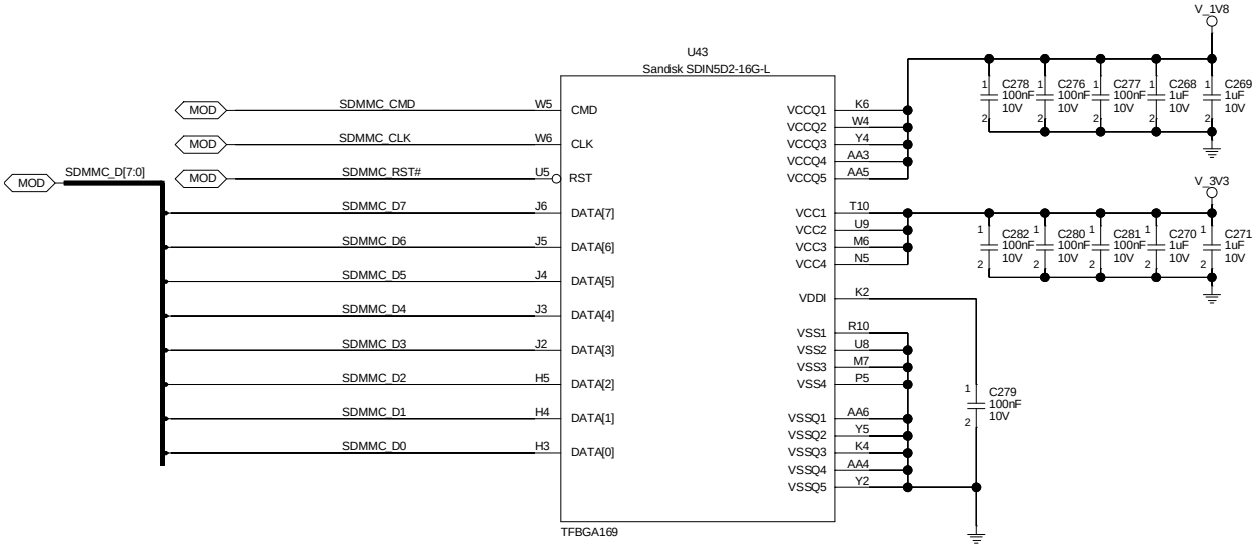
6.2 eMMC

The eMMC (embedded Multi Media Card) interface is used to connect non-volatile multimedia memory devices to host processor. The eMMC standard is maintained by JEDEC, with the latest revision being JESD84-B451: Embedded MultiMediaCard (eMMC), Electrical Standard (Version 4.51).

An eMMC includes a raw MLC NAND flash memory and microcontroller. The eMMC microcontroller performs several functions such as bad block management, wear leveling and error correction code (ECC) internally which significantly reduces the software overhead.

SMARC modules support 1 bit, 4 bit and 8 bit modes. The eMMC interface includes a clock line (maximum clock frequency of 26 MHz or 52 MHz for devices supporting High Speed mode), a command line and 8 data lines and an active low reset signal. SMARC Modules may support an eMMC Boot option.

Figure 49 eMMC Flash



eMMC flash devices are typically available in 4GB, 8GB, 16GB and 32GB densities. A selection of vendors and vendor part numbers for a 16GB eMMC flash are given in the following table. All the part numbers shown in this table are pin compatible. The package extents vary slightly between vendors. The package for the part numbers shown are approximately 14mm x 18mm x 1mm.

Table 12 16 GB eMMC Flash options

Mfg	Mfg P/N	Description	Notes
Sandisk	SDIN5C2-16G-L	16GB eMMC TFBGA169	
Transcend	TS16GEMA2-M	16GB eMMC TFBGA169	
Micron	MTFC16GJVEC-4M IT	16GB eMMC WFBGA169	Industrial Temp: -40 ^{o}C to +85 ^{o}C
Samsung	KLMAG4FE3B-A001	16GB eMMC FBGA169	

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7 CAMERA INTERFACES

7.1 General

The SMARC specification allows for serial (MIPI CSI) and parallel cameras to be interfaced to the SMARC Module. The Module camera interface is at V_IO (typically 1.8V) or CSI voltage levels. The same SMARC pin set is used for the serial and parallel interfaces, so some cautions are necessary, as outlined in the SMARC specification document and in this design guide. There are two SMARC pins (PCAM_ON CSI0#, pin S57 and PCAM_ON_CSI1#, pin S58), detailed in the SMARC specification document and referenced below, that distinguish between the serial and parallel formats. A given Module design will generally support either a serial or a parallel camera interface (or maybe no camera interface), but not both.

In the long term, it is expected that virtually all interfaces – including camera interfaces – will be serialized. However, as of this writing, in mid 2013, both serial and parallel camera interfaces are in use. In the short term, parallel interfaces may be more popular.

There are a number of camera modules available that implement both serial and parallel interface formats on the same device, set by a strap pin.

7.2 Camera Data Interface Formats

There are a wide variety of data formats that are used to convey camera data to a host system. A complete description of these formats is very much beyond the scope of this design guide. Briefly stated, camera data formats may be divided into two groups: “raw” and “processed”. The raw camera data formats need to be adjusted for camera and sensor specific characteristics (non-linearities, sensor pixel quirks, color corrections and so on). Using the raw format requires an additional level of software complexity that is beyond many users. Unless you have a specific need for a particular camera that outputs “raw” sensor data, it is best to stick with cameras that include a processor on the camera module that convert the camera sensor data to a standard format such as RGB or YUV, JPEG or others. The “Bayer” format is one of the numerous raw formats that you may wish to avoid. A variation on the above is that some cameras offer “raw” RGB, meaning that the pixel data is sorted into RGB elements but sensor nonlinearities are not processed in the camera IC.

7.3 Camera and Camera Module Vendors

Table 13 Camera and Camera Module Vendors

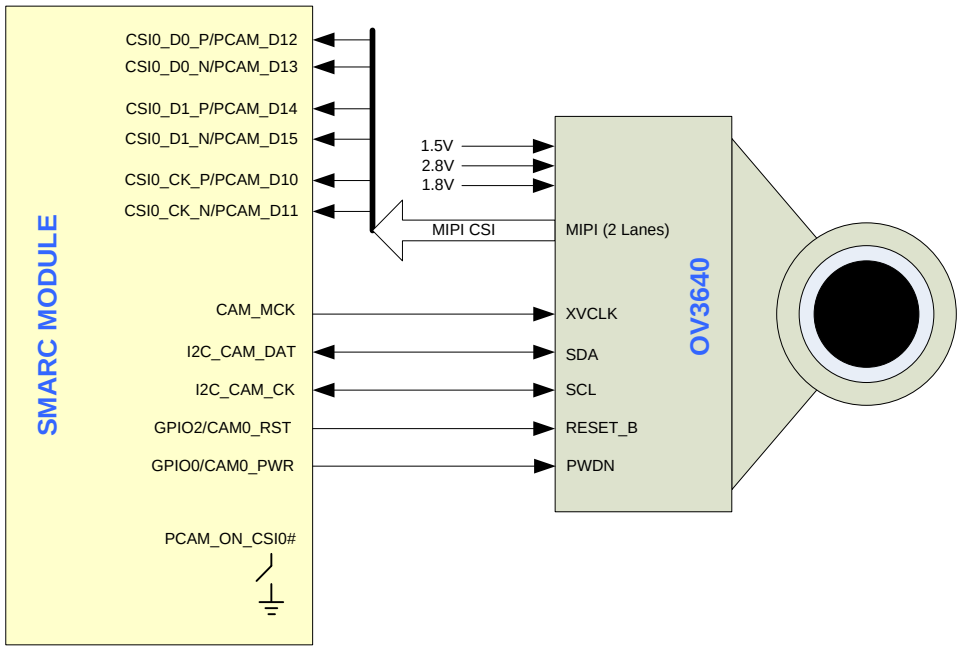
Vendor	Link	Notes
Aptina	**www.aptina.com**	Aptina is a renowned leader in camera sensors but obtaining smaller volumes from them is challenging.
Leopard Imaging	**www.leopardimaging.com**	Leopard offers camera modules (on small PCBs) using sensors from Aptina and others
Omni-Vision	**www.ovt.com**	Omni-vision offers camera sensors with output data available in RGB and YUV formats, and over CSI and parallel data paths. Many Omnivision products including the OV3640 (or OV03640) (used in the examples below) are easily available from distributors such as Digikey.

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7.4 Serial Camera Interface Example

The figure below illustrates a CSI implementation on a SMARC Carrier. The OV3640 is a 3.1 Mega-pixel CMOS sensor from Omni-Vision which supports both serial and parallel camera interfaces. Here, the output of the sensor is connected to CSI0 interface of the SMARC Module. I2C_CAM is the control interface used for configuring the sensor. CAM_MCK is the master clock output from the SMARC Module. PCAM_ON_CSI# signal should be left open in SMARC Modules supporting CSI.

Figure 50 Serial Camera Implementation



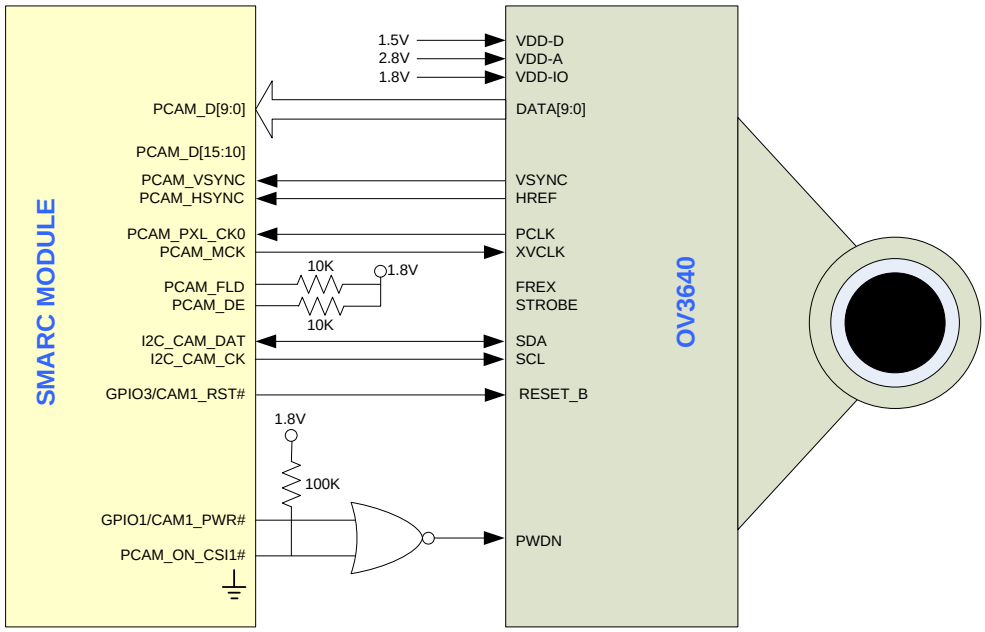
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7.5 Parallel Camera Interface Example

The following Figure illustrates a SMARC parallel camera implementation. The parallel data bus width is 10 bit in this example (widths up to 16 bits may be possible). The SMARC I2C_CAM port is used for camera control.

SMARC Modules that implement a parallel camera interface have the PCAM_ON_CSI# signal on the Module tied to GND. The Carrier should implement a power enable circuit, with a NOR gate and pull-up resistor, per the figure below. This is to prevent the camera from powering up if the SMARC Module has a CSI (serial) interface rather than a parallel interface.

Figure 51 Parallel Camera Implementation



7.6 Other Camera Options

SMARC systems have the option of using the dedicated SMARC camera interface pin set. For a dedicated system produced in high volume, this is likely to be the most cost effective option. However, other options exist. USB cameras are becoming very popular. They enjoy good software support and are becoming more and more cost effective as time passes. However, the bandwith of a HS USB interface (480 Mbps) is less than what is possible with the SMARC parallel or CSI camera interfaces.

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8 GPIO

8.1 SMARC Module Native GPIO

SMARC Modules support twelve general purpose IO pins: GPIO0 to GPIO11. Each of these can be configured as an input or output pin. The SMARC specification recommends the use of GPIO0 to GPIO5 as outputs and the use of GPIO6 to GPIO11, as inputs. SMARC Modules support only two dedicated GPIOs (GPIO10 and GPIO11). The other ten GPIOs are multiplexed pins supporting functions like Camera Power Enable, Camera Reset, CAN Error input, Tachometer input, PWM output etc. SMARC Modules generally allow the GPIO to be configured to generate an interrupt.

GPIO voltage levels depend on the V_IO level supported by the SMARC Modules. It will be either 1.8V (more common) or 3.3V.

8.2 GPIO Expansion

For a low cost, easy way to implement additional GPIO ports, see ***Section 4.2.5 I2C Based IO Expanders.***

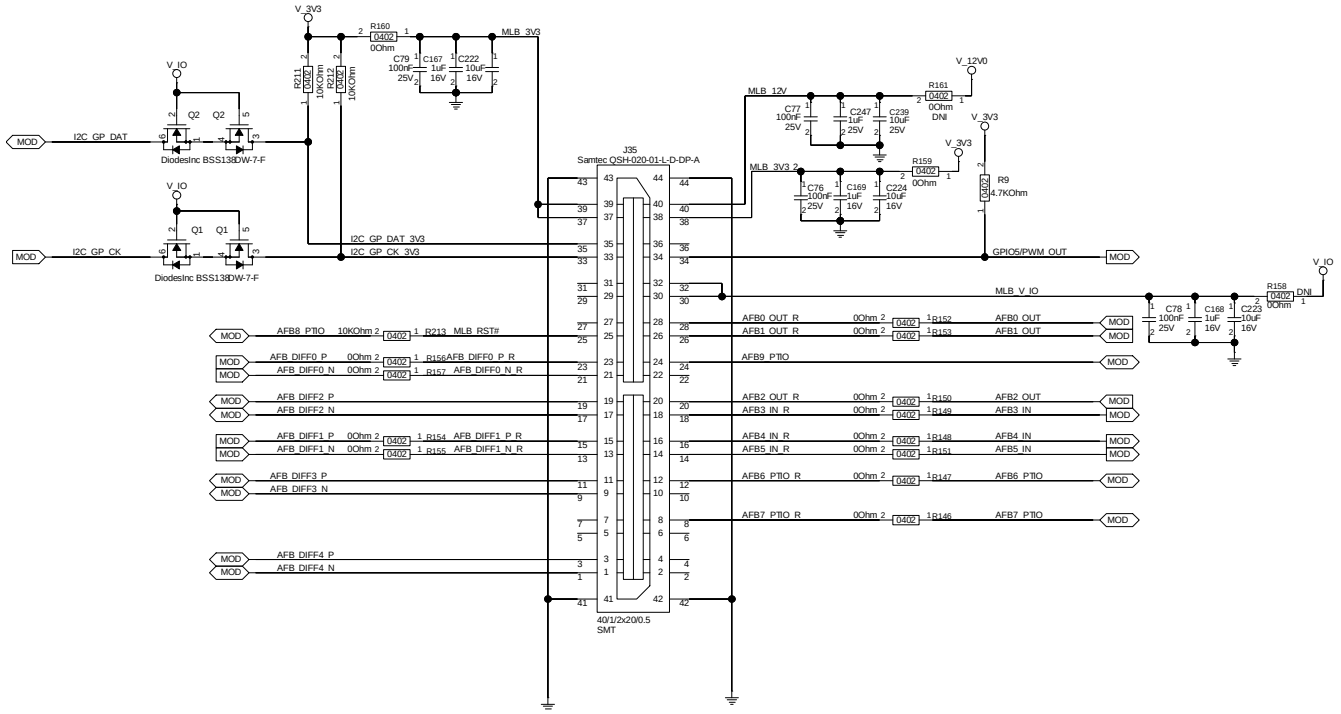
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9 ALTERNATE FUNCTION BLOCK

The Alternate Function Block (AFB) is a group of SMARC signals that are set aside for application-specific uses and for future, to-be-determined, SMARC standard use. The SMARC specification details some suggested uses and guidelines for the AFB.

The example below shows the AFB signals brought to a mezzanine connector that is suited for high speed single ended and differential pair signals. This connector is the same as the connector used on the Freescale iMX6 "Sabre" reference platform. The pin-out shown here is compatible as well. This may be of some value to iMX6 users.

Figure 52 AFB Connector



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10 CARRIER POWER CIRCUITS

10.1 Power Budgeting

One of the early steps in a SMARC Carrier design is to develop a power budget and a strategy for meeting that budget. All the power rails need to be identified and worst-case current consumptions listed. A spread-sheet is usually developed. The power circuits should be designed to meet the worst case numbers, but the actual system power consumption will usually turn out to be quite a bit less than the total indicated by the total worst case numbers for each individual rail. Once there is an understanding of the amount of power required, a plan can be developed for meeting the requirements. A sample power budget sheet is shown in the table below. This example is hypothetical and serves to illustrate the process. This example assumes that the SMARC Module is to be supplied by a fixed 5V DC source. A variable battery power source would result in a different sheet.

Table 14 Hypothetical Power Budget Example – Part 1

	12V Current	5V Current	3.3V Current	1.8V Current	1.5V Current	Power	Notes
Display Backlight	0.6A					6.0W	
USB		1.5A				7.5W	3 devices
SMARC Module		1.2A				6.0W	
Mini PCIe Module			1.0A		1.0A	4.8W	
Audio Circuits		0.5A		0.1A		2.7W	
Misc. Carrier Circuits			0.5A	0.2A		2.0W	
Current Subtotals	0.6A	3.2A	1.5A	0.3A	1.0A		
Power Totals	7.2W	16W	5.0W	0.5W	1.5W	29W	

The total shown is a worst case value, and power circuits should be designed to handle the worst case. However, experience shows that typical average system power consumptions are significantly less, on the order of 50% of worst case. The total above does not account for power conversion losses. These are added in a later section, when this hypothetical example is continued.

Many SMARC Module vendors offer evaluation platforms, and it is worth the time and effort to roughly prototype the target system with available hardware and software. This can validate power estimates and have other benefits, such as allowing performance benchmarks to be carried out before committing to the full system design.

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10.2 Input Power Sources

Table 15 Input Power Source Possibilities

Power Source	Voltage	Notes
3.3V Fixed	3.3V +/- 5%	Possible, but not a common choice, as often there are significant power requirements for USB (5V at up to 500 mA for each external USB 2.0 port) and the display backlight supply (12V at up to 600 mA is common), requiring up (boost) conversion. Some SMARC Modules may not support 3.3V power input.
5V Fixed	5.0V +/- 5%	Common choice – allows some of the higher power consuming devices (USB, SMARC Module) to be fed directly without conversion. Other, lower current devices require power conversion.
12V Fixed	12V +/- 5%	Allows display backlight to be powered directly, without conversion (if the display backlight accepts 12V). Requires buck conversion of 12V to 5V for Module and for Carrier USB and other functions.
Power "Brick"	Various ranges available 6V, 9V, 12V, 14V	Various output levels are available. The voltage regulation from a power brick is often not good, and it is best not to rely on the brick output to feed any circuit that needs to be supplied with a voltage regulated over a relatively tight range. Usually the brick output voltage is down converted and regulated on a Carrier board design.
Battery - Single Level Lithium Ion Cell	3.6V nominal	4.2V fully charged; 3.0V discharged. Most SMARC Modules operate directly from this range (check with your vendor).
Battery – Two Level Lithium Ion Cells	7.2V nominal	8.4V fully charged; 6.0V discharged
Battery – Three Level Lithium Ion Cells	10.8V nominal	12.6V fully charged; 9.0V discharged
Wide Range DC	10V – 30V (Typical)	Wide range input power supply is possible. Note that to handle higher voltages, parts rated for use at the higher voltages must be used.
Power Over Ethernet	48V	IEEE802.3af POE standard allows 12.5W load power IEEE802.3at POE standard allows 25.5W load power The POE supply output is transformer isolated from the GBE lines, with 1500V DC isolation. POE supply output voltages are design specific – 24V, 12V and 5V outputs are common.
Automotive	12V nominal (see notes)	When the engine is off, the supply battery voltage is 12V nominal. During engine cranking, the supply can dip to 6V. When the engine is running, the DC level can be up to about 16V, with a 14.4V level being typical. Transients in excess of +/- 100V are common. A user may disconnect the battery and reconnect it with the polarity reversed. All in all, it's a harsh environment that needs careful attention. A basic strategy is to have an input network with good transient and reverse polarity protection, and then use a rugged switching supply that can handle an input range from 6V to 24V, and deliver a 5V output to the SMARC Carrier.

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10.3 Power Budgeting, Continued – Fixed 5V Power Source

Once a power budget is in hand, a power architecture can be developed. Let's assume that the input power source is to be 5V fixed, and the power budget per voltage rail is as per the hypothetical example given in ***Table 14 Hypothetical Power Budget Example*** above. Next, one has to decide how to realize the various power rails. Here we assume that switch mode power converters are used to create all rails from the 5V source. The efficiency (or inefficiency) of the power converters must be accounted for, as shown in the following table.

Table 16 Hypothetical Power Budget Example – Part 2

Voltage Rail	Current	Power	Derived From	Efficiency Assumption	Power From 5V Input	Current From 5V input rail
12V	0.6A	7.2W	5V (Boost)	90%	8W	
5V	3.2A	16W		100%	16W	
3.3V	1.5A	5.0W	5V (Buck)	90%	5.6W	
1.8V	0.3A	0.5W	5V (Buck)	90%	0.6W	
1.5V	1A	1.5W	5V (Buck)	90%	1.7W	
				Total	32W	6.4A

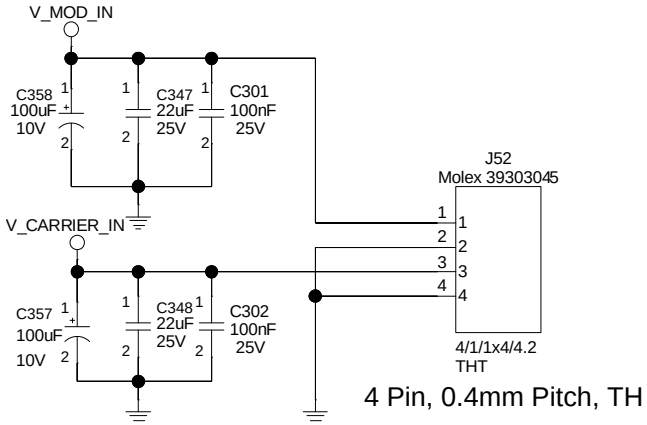
Other factors can make the process a bit more complex than this example. If some power rails are to be created with linear supplies from a higher voltage rail, for example, then the entire current used by the lower rail needs to be added to the current budget of the higher voltage source rail. If the primary source rail varies (such as from a battery) the extremes of the source rail must be taken into account.

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10.4 Fixed 5V DC Power Input Circuit Example

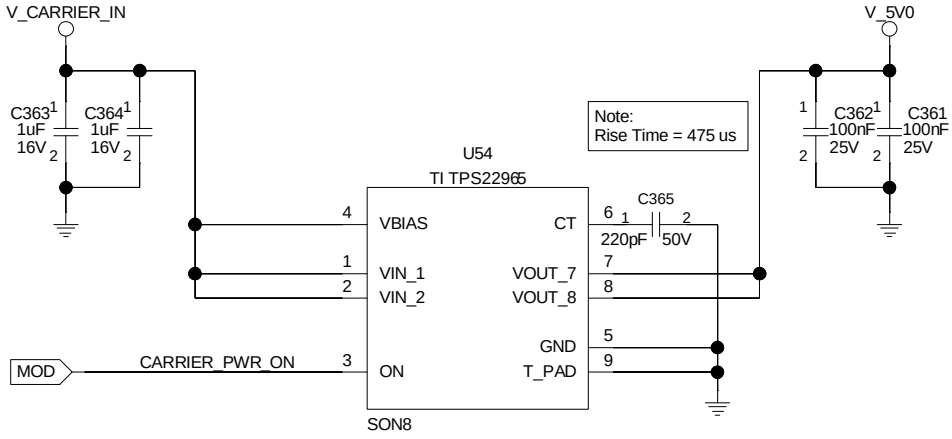
The power entry connector for this fixed 5V power source example is shown in the figure immediately below. There are two paths, given net names V_MOD_IN and V_CARRIER_IN. Both carry 5V in from a single bench supply. The nets are separated to allow separate current (and power) measurements of the SMARC Module and the Carrier board. If this separate measurement capability is not needed, then the separate entries could be combined into a single net.

Figure 53 5V Input Connector



The following figure illustrates a power switch used to hold off most Carrier board circuits from being powered until the Module asserts the “CARRIER_PWR_ON” signal. Some Carrier circuits, such as those involved in power management and those that are in the “Module Power Domain” as defined by the SMARC specification, may be powered whenever the Module has power, before (and after) the assertions of CARRIER_PWR_ON.

Figure 54 5V Carrier Power Switch



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The following three figures illustrate buck (or step-down) switching converters that create 3.3V, 1.8V and 1.5V from the V_CARRIER_IN 5V power source. Since the power needs on these rails are modest, integrated switchers with internal power FETs are well suited to the job. They are physically small and robust. The parts shown are from Texas Instruments, although similar parts exist from other vendors.

The figures show three separate enables for the three supplies, with net name designations V_3V3_EN, V_1V8_EN and V_1V5_EN. Sources for these nets are not shown. These enable pins should be driven to the “enabled” state when signal CARRIER_PWR_ON is high. They could be driven by CARRIER_PWR_ON, or by V_5V0, or by other Carrier circuitry. If the situation demands aggressive power management, it may be desirable to have Carrier I/O circuits that allow the various enables to be brought low if the power rail is not needed. If this is done, the designer should arrange that the enables do not go high before CARRIER_PWR_ON is high.

The LEDs and signal FETs on the right side of the three figures are optional. The LED lights up as a status indicator when the power rail (V_3V3, V_1V8 or V_1V5) is up. The FET prevents leakage from the main power rails (V_MOD_IN and V_CARRIER_IN) when the switchers are powered down. Rail V_MOD_IN_LED ties to V_MOD_IN through a removable jumper. Removing the jumper prevents the LEDs from burning power in standby states (and in all states).

Figure 55 3.3V 2A Buck Converter

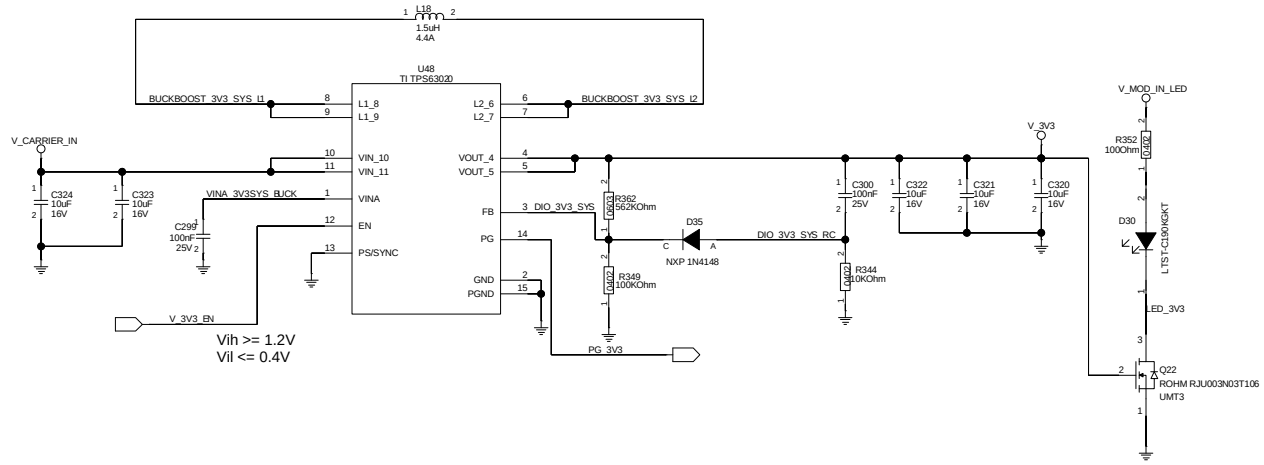
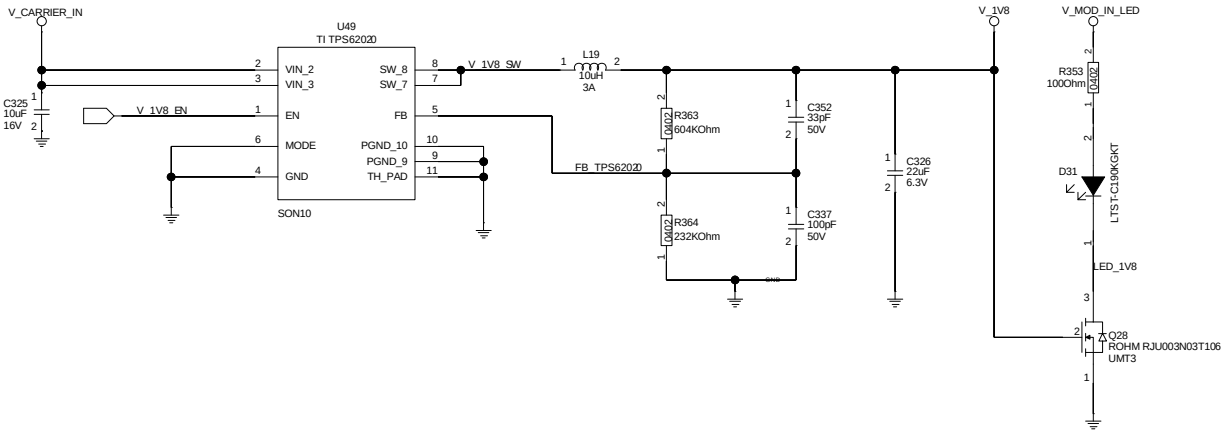
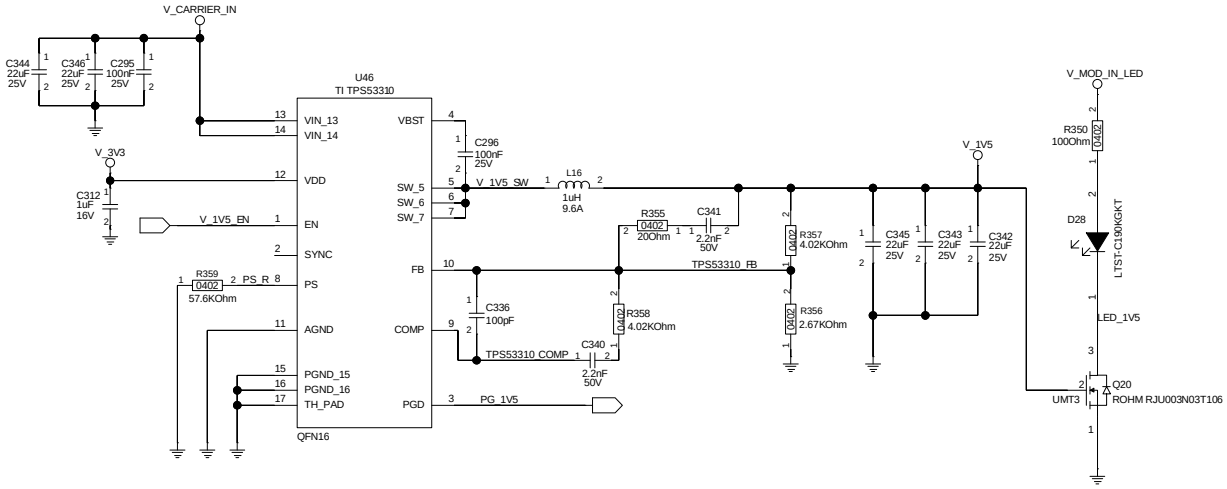


Figure 56 1.8V Buck Converter



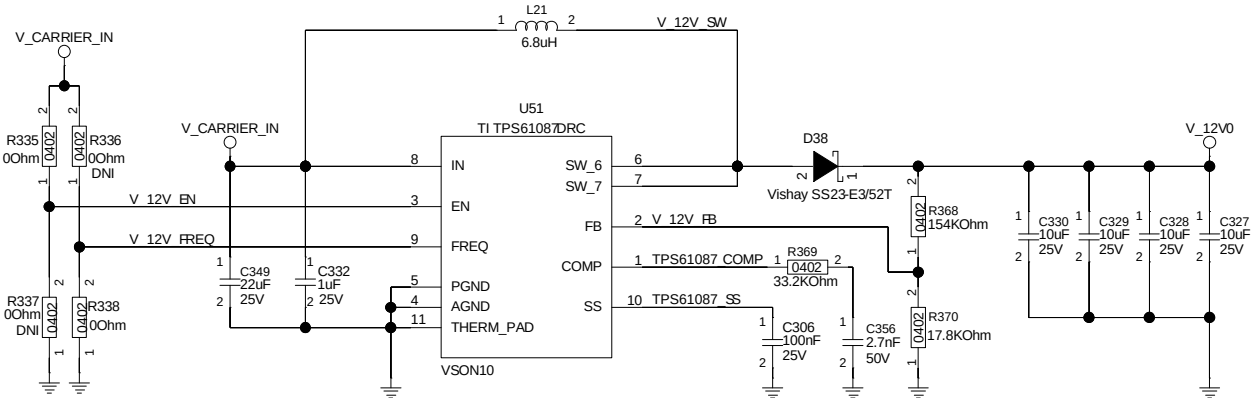
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Figure 57 1.5V Buck Converter



Many LCD backlights require a 12V power source. If the system power source is a fixed 5V supply, or a battery supply well under 12V, then a boost converter circuit is needed. An example is shown here:

Figure 58 12V Boost Converter for Backlight Power

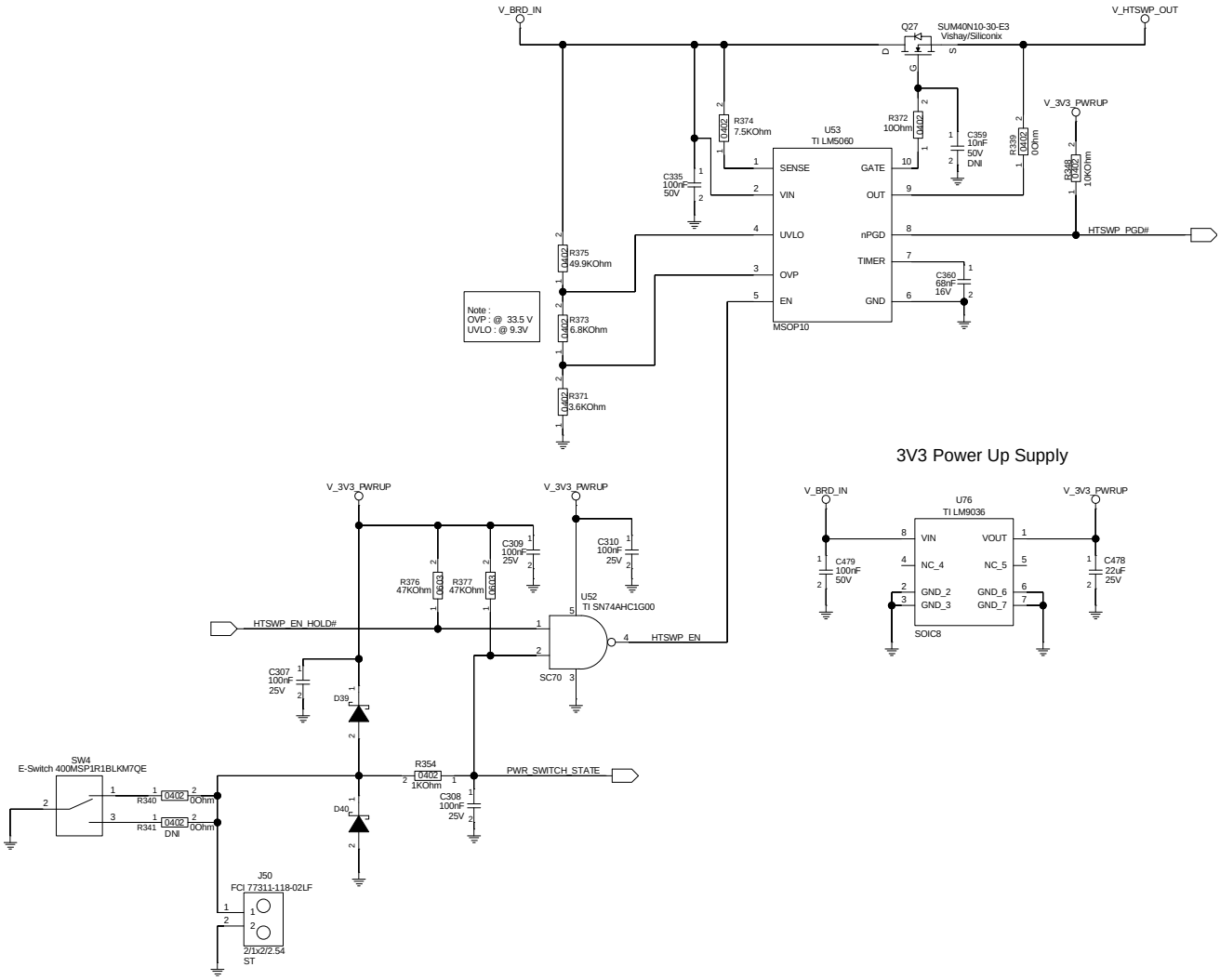


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10.5 Power Hot Swap Controller

Hot swap controller circuits can be used to control the system power supply rise time. This may be desirable when plugging circuits in live to low impedance sources, such as a battery. The figure below illustrates a high-side protection controller circuit using TI LM5060. The N-Channel MOSFET isolates the input supply (V_BRD_IN) from rest of the board (V_HTSWP_OUT). The circuit limits the in-rush current and provides a power good signal once the output voltage reaches the input voltage. An option is provided to enable LM5060 (HTSWAP_EN) from a CPLD as well as using a switch / jumper.

Figure 59 Hot Swap Controller



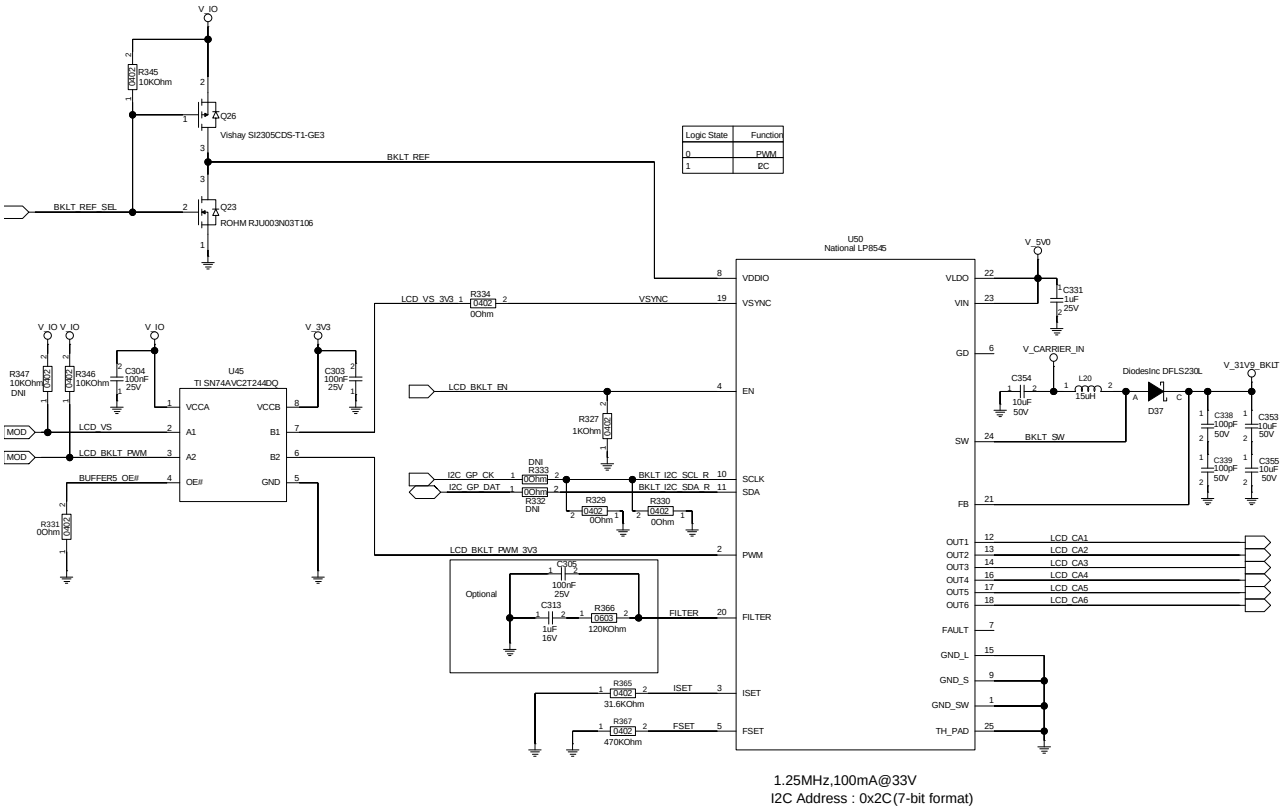
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10.6 High Voltage LED Supply

Some LCD panels have multiple sets of series LED strings that are to be driven by a high voltage LED supply. Vendors such as TI and Analog Devices provide the ICs for these supplies. A schematic example using a TI / National high voltage LED supply is given below.

The LED brightness can be controlled either using PWM control (if the IC VDDIO pin is set LOW) or by I2C (if VDDIO is HIGH). If V_IO is 1.8V, a level translator needs to be used for signals VSYNC and PWM.

Figure 60 LP8545 LED Backlight Power



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10.7 3.0V to 5.25V Power Input Example

The circuits shown below illustrate buck-boost switching converters that generate 5V and 3.3V from the V_CARRIER_IN power source (3.0V to 5.25V). Since the power needs on these rails are modest, integrated switchers with internal power FETs are well suited to the job. They are physically small and robust. The parts shown are from Texas Instruments, although similar parts exist from other vendors.

The figures show separate enables for the 5V and the 3.3V supplies, with net name designations V_5V0_EN and V_3V3_EN. Sources for these nets are not shown. These enable pins should be driven to the "enabled" state when signal CARRIER_PWR_ON is high. They could be driven by CARRIER_PWR_ON, or by V_CARRIER_IN, or by other Carrier circuitry. If the situation demands aggressive power management, it may be desirable to have Carrier I/O circuits that allow the various enables to be brought low if the power rail is not needed. If this is done, the designer should ensure that the enables do not go high before CARRIER_PWR_ON is high.

Figure 61 5V, 2A Buck-Boost Converter

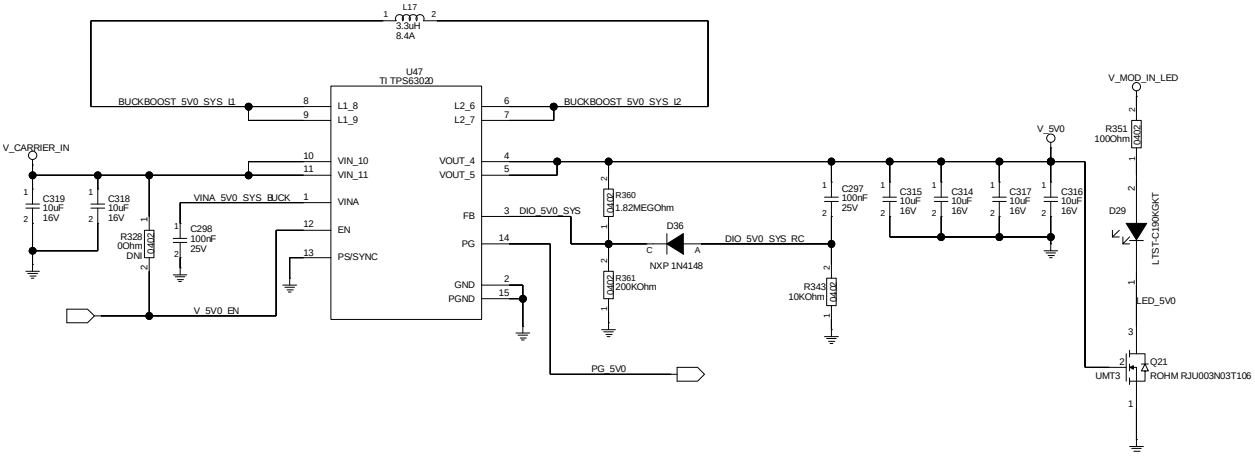
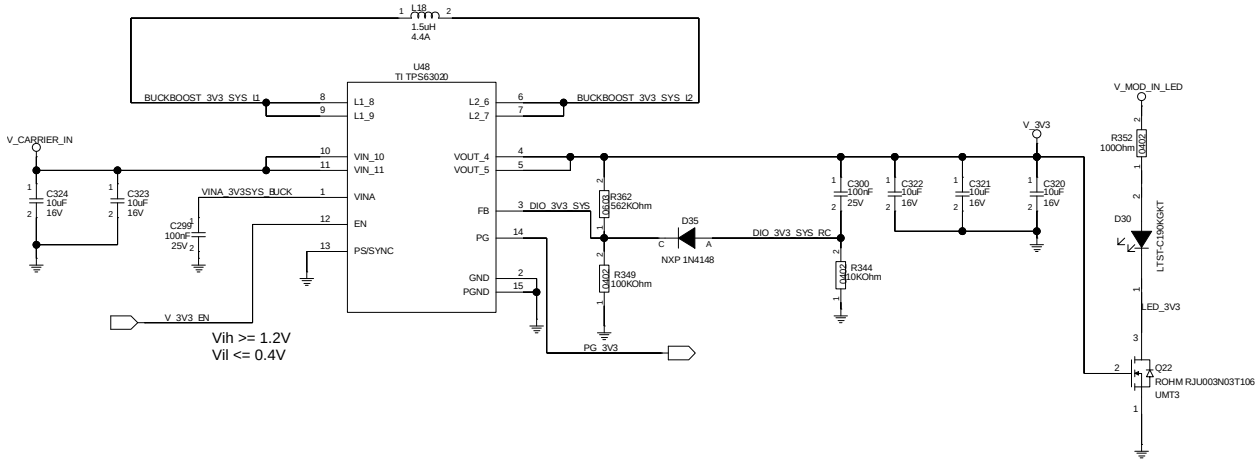


Figure 62 3.3V 2A Buck-Boost Converter

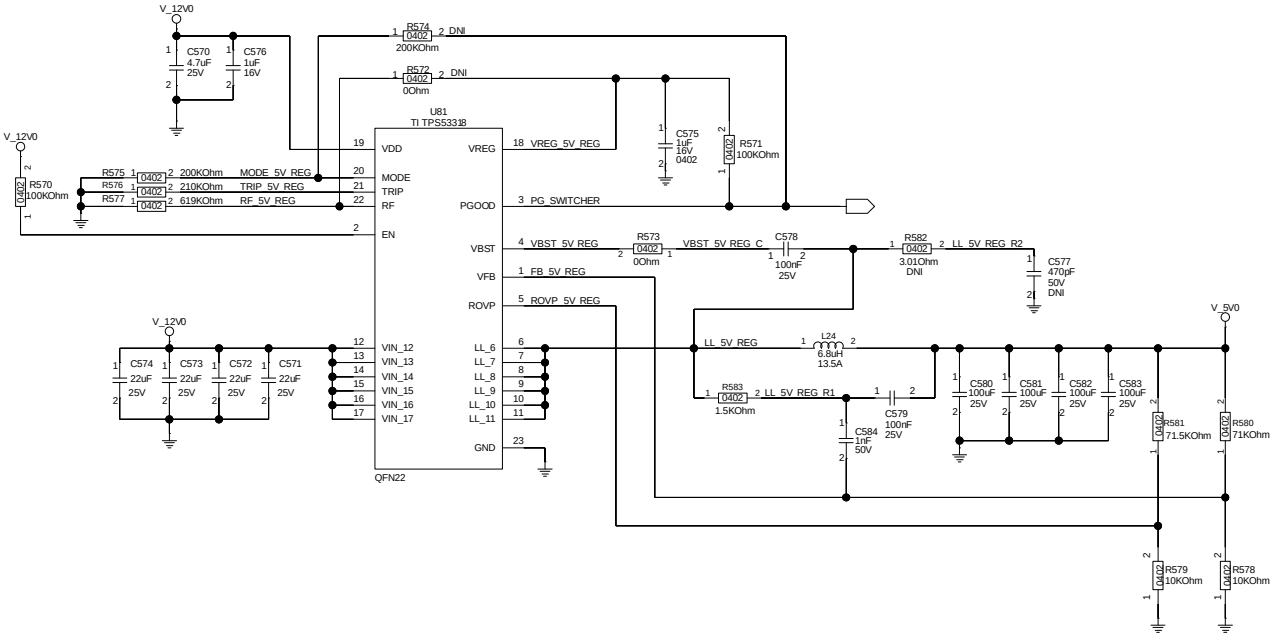


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10.8 12V Input

There are many choices for switching power supply circuits to step a 12V input down to lower voltages for SMARC use. An integrated switcher possibility from TI is shown in the following figure.

Figure 63 12V Step Down Switcher

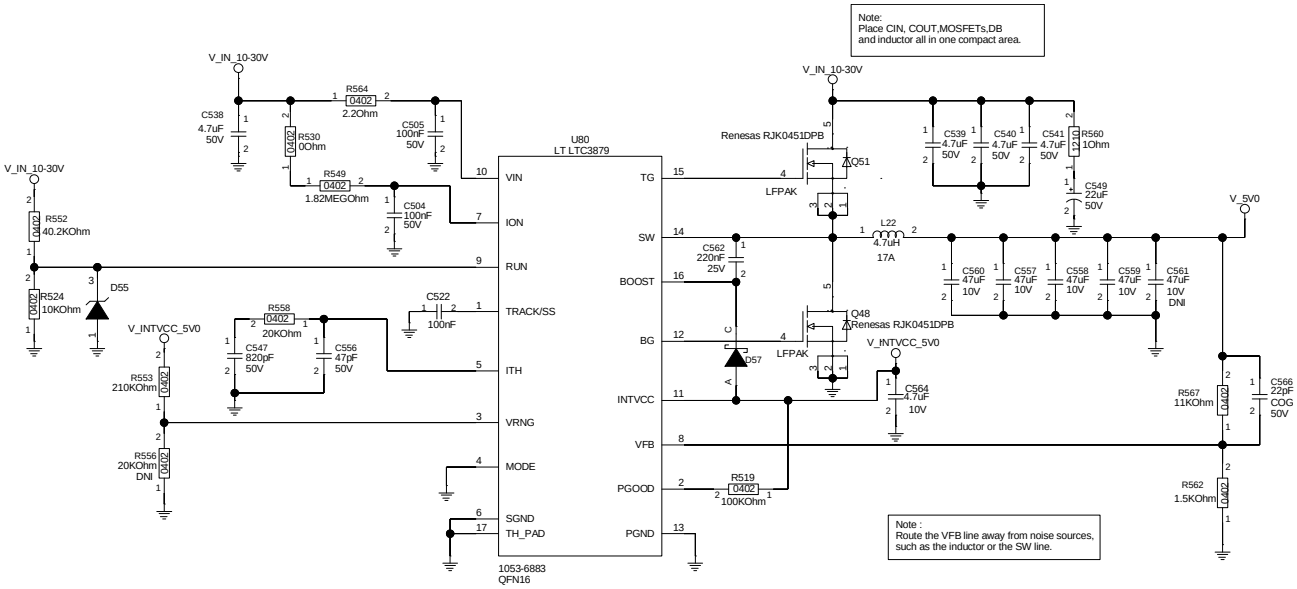


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10.9 Wide Range Power Input

In some applications it is desirable to allow for a wide range power input. This is the case in certain industrial and automotive settings. Since SMARC systems operate at low voltages (5V and under, apart from LCD backlight considerations), it is straightforward to implement a wide range buck converter. The figure below shows an example implemented with the Linear Technologies LTC3879. Similar parts are available from other vendors. The Texas Instruments TPS40170 is another part to consider for this application. The TPS40170 allowable input range spans 4.5V to 60V. If you are targeting the higher input ranges, be sure that components exposed to the input voltage are adequately rated for that high voltage.

Figure 64 Wide Range Power Input Switcher



If the load on the Carrier 3.3V is high, it may be worth having a second wide input range switcher per the above figure, configured for the 3.3V output.

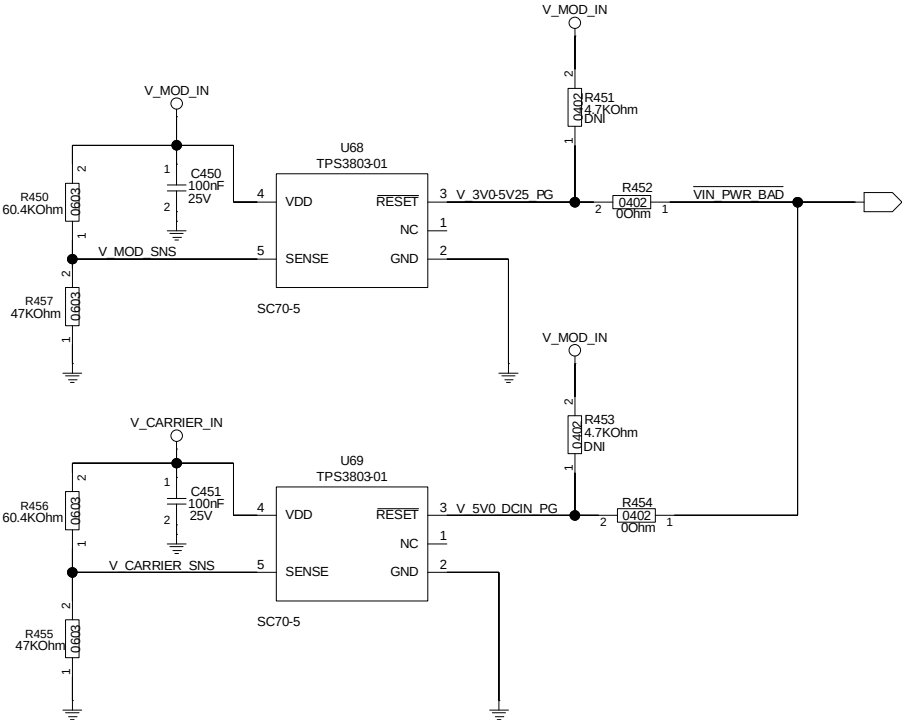
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10.10 Power Monitoring

The SMARC specification document defines a VIN_PWR_BAD# input. Its use is optional. If VIN_PWR_BAD# is held low by a Carrier or power supply circuit, the Module assumes that the source power is not ready and does not boot.

VIN_PWR_BAD# is typically generated by a power monitor / reset generator IC, such as those shown in the figure below. This figure shows two of them, although this is not really necessary if the Module and the Carrier circuits are powered by a single source and you don't want to keep them separate.

Figure 65 Power Monitor - Incoming Power



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10.11 Power Over Ethernet

Power may be delivered to a SMARC system over the Gigabit Ethernet cabling, cohabiting with the GBE data traffic. The 48V DC power is extracted from the isolated GBE cabling by a diode bridge and a specialized transformer isolated switching power supply. POE is defined by the IEEE 802.3af and IEEE 802.3at. standards. The 802.3af payload power is limited to 12.5W and the 802.3at to 25.5W.

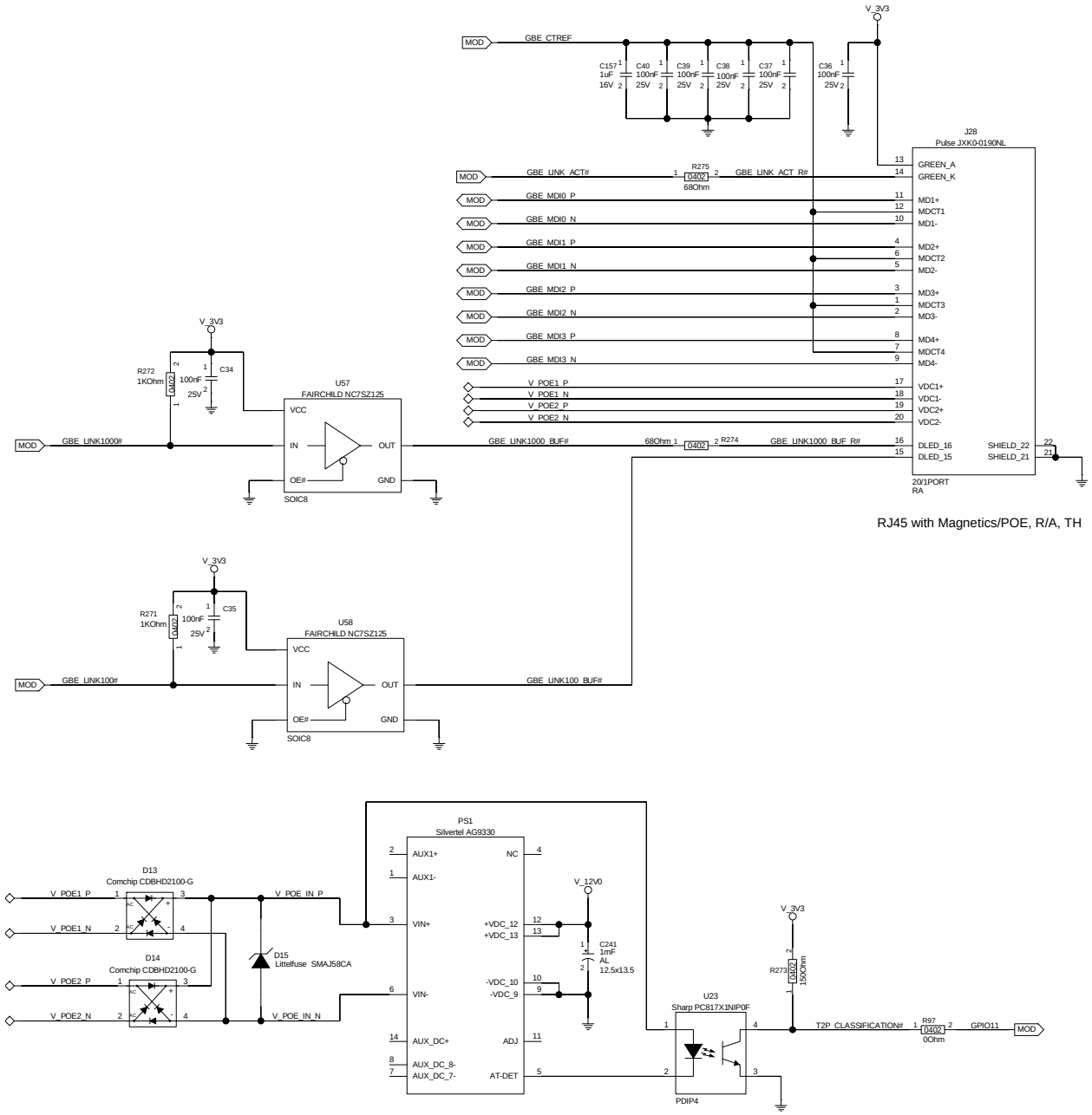
Many semiconductor vendors offer POE solutions. Designing a POE power supply is a little trickier than designing your average switching supply, as the POE supply is transformer coupled, there are isolation requirements to meet, and some sort of DC isolated feedback mechanism must be incorporated. If your product volume is high, it may be worth the trouble of implementing your own Carrier-down circuit. See Texas Instruments and Micro-Semi for POE IC solutions. Even if you don't go for the do-it-yourself approach, there are some very instructive Application Notes available from these vendors

In many cases it is more straightforward to make use of a POE module, available from various vendors. One attractive POE module line comes from Silver Telecom (**www.silvertel.com**). IEEE 802.at compliant modules with output voltage options of 24V, 12V or 5V are available. The sample circuit below uses a Silver Tel module with a 12V output. The 12V output can not be fed directly to a SMARC Module – a step down converter would be needed. However, many SMARC systems incorporate LCD displays that utilize 12V backlights – hence the POE output option of 12V may make sense. If not, then the 5V POE output option could be considered (and the 5V POE module output can be fed directly to the SMARC Module).

Note that for POE use, a particular type of GBE jack is required, to get access to the DC power coming in over the isolated GBE lines. The example shown here uses a Pulse JXK0-0190NL GBE POE Mag-Jack. Similar parts are available from Bel-Fuse, Tyco and others – but beware of differing PCB footprints.

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Figure 66 GbE with PoE



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10.12 Li-ION Battery Charger

10.12.1 General

Caution: improper battery charging can be a serious safety hazard. This section serves as a brief introduction to what is involved in designing a battery management system, but it is not enough to go on. Other source materials, from IC companies, battery vendors and the technical literature will be necessary for you to implement a safe and effective system.

Lithium Ion batteries have a fully charged cell voltage of 4.2V, nominal cell voltage level of 3.7V, and a depleted voltage of 3.0V. They are used in series combinations and parallel combinations. The voltages for various series combinations are shown in the following table.

Table 17 Lithium- Ion Battery Cell Voltages

Series Cells	Nominal Voltage	Fully Charged	Fully Depleted
1	3.7V	4.2V	3.0V
2	7.4V	8.4V	6.0V
3	11.4V	12.6V	9.0V
4	15.1V	16.8V	12.0V

Battery capacities are measured in Ampere-Hours (AH). A fully charged battery with a 2AH capacity can deliver 2A for 1 hour, or 1A for 2 hours and so on. The capacity is sometimes designated ‘C’ in battery data sheets.

Lithium-ion batteries are typically charged in two phases: a constant current portion (for the deeply depleted battery) and a constant voltage portion (when the charging process nears completion).

The constant current charging is typically done at a maximum constant current equal to the battery capacity – for example, a 2AH battery is charged at a maximum charging current of 2A. The constant voltage portion is done at the cell fully charged voltage – 4.2V for a single series cell, 8.4V for two series cells, and so on. The battery data sheet and vendor’s application notes should of course be consulted for more specific recommendations that apply to the situation at hand.

The battery temperature should be monitored during charging and use. The charging is disabled if the battery temperature exceeds a threshold set by the battery charger implementation.

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10.12.2 Battery Charger Circuit Example

A battery charger implementation is shown in the following four figures. This example uses Texas Instruments / Benchmarq parts. Similar devices are available from Linear Technology, Maxim, Analog Devices and others.

The first of the four figures shows the overall charging system in block diagram format. The actual circuit schematics are shown in the three subsequent figures.

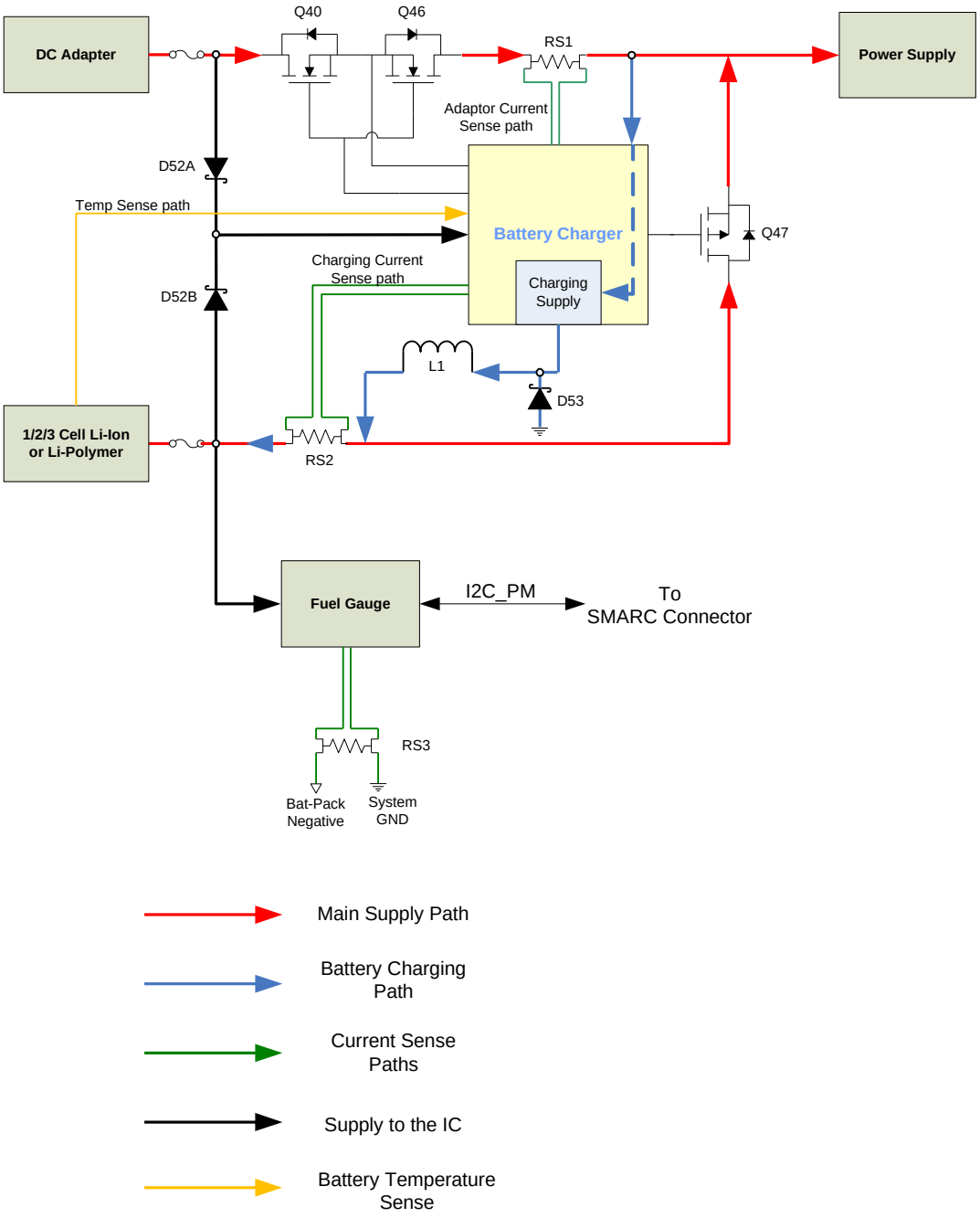
Caution: many of the component values shown here need to be adjusted to suit the details of the situation at hand – the number of series cells, the battery capacity, the battery thermistor particulars.

With reference to the following four figures:

- FETs Q40 and Q46 form an analog switch that the charger IC can use to gate power from the external DC adapter into the system. Charger current is sensed through RS1. The FETs are turned off if the charger voltage is too high, too low or if the current draw is excessive.
- FET Q47 is turned on by the charger IC to allow battery power to be delivered to the target system.
- FET Q47 is off when Q40 and Q46 are on.
- The charger IC includes charge pumps to drive the N channel FET gates to a sufficiently high voltage to turn them on.
- The charger IC in this example has an internal switch-mode power supply, with internal high side FET, that are used when charging the battery. The external components of this supply are L1 and D53 in the diagrams.
- Battery charging current is measured through RS2.
- It is important to monitor the battery temperature. Usually an NTC (negative temperature coefficient) thermistor attached to or internal to the battery is used for this. The charger IC has support for the thermistor.
- A fuel gauge IC is used to collect information about battery charge levels. The gauge tracks current into and out of the battery, via sense resistor RS3. This sense resistor is in series with the battery GND terminal. The gauge has an I2C interface to the SMARC Module.
- There are three status signals from the charger system to the SMARC Module: CHARGING#, BATLOW# and CHARGER_PRSNT#.

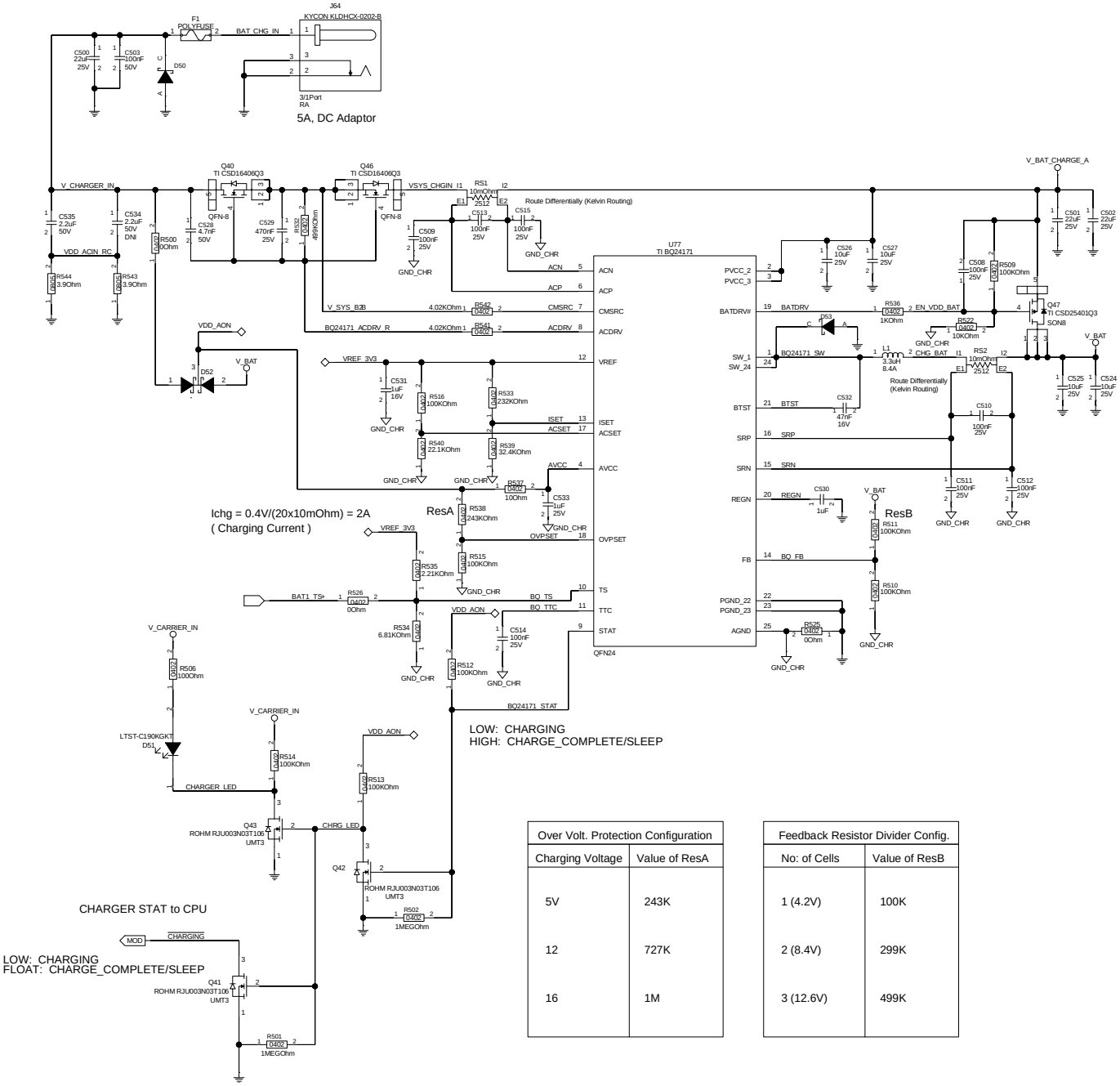
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Figure 67 Li-ION Battery Charger - Block Diagram



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Figure 68 Li-ION Battery Charger - Schematic

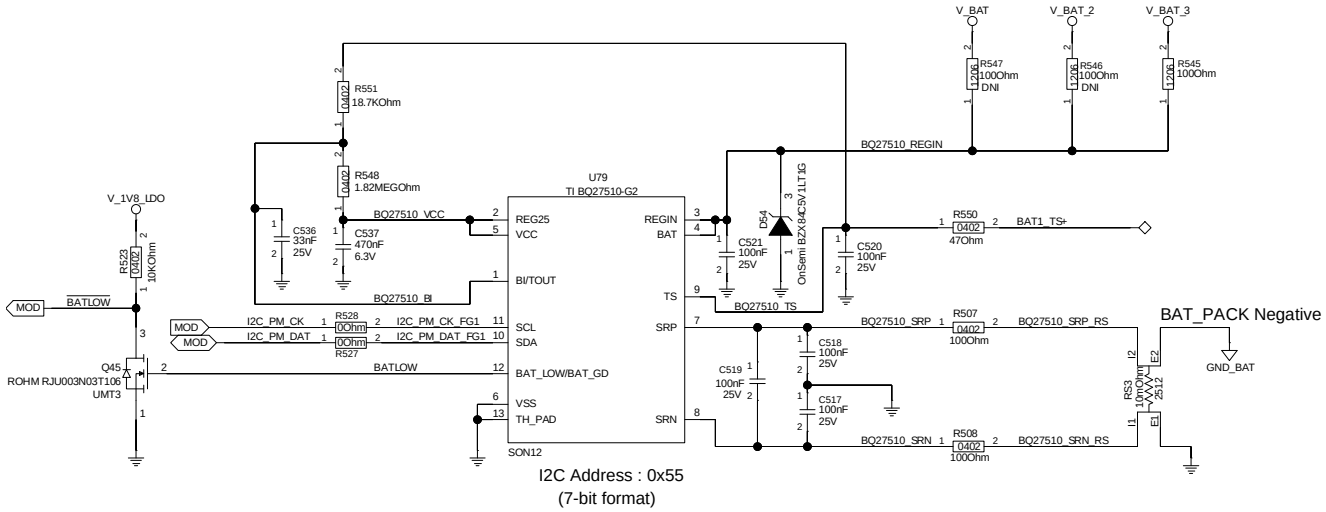


Over Volt. Protection Configuration	
Charging Voltage	Value of ResA
5V	243K
12	727K
16	1M

Feedback Resistor Divider Config.	
No: of Cells	Value of ResB
1 (4.2V)	100K
2 (8.4V)	299K
3 (12.6V)	499K

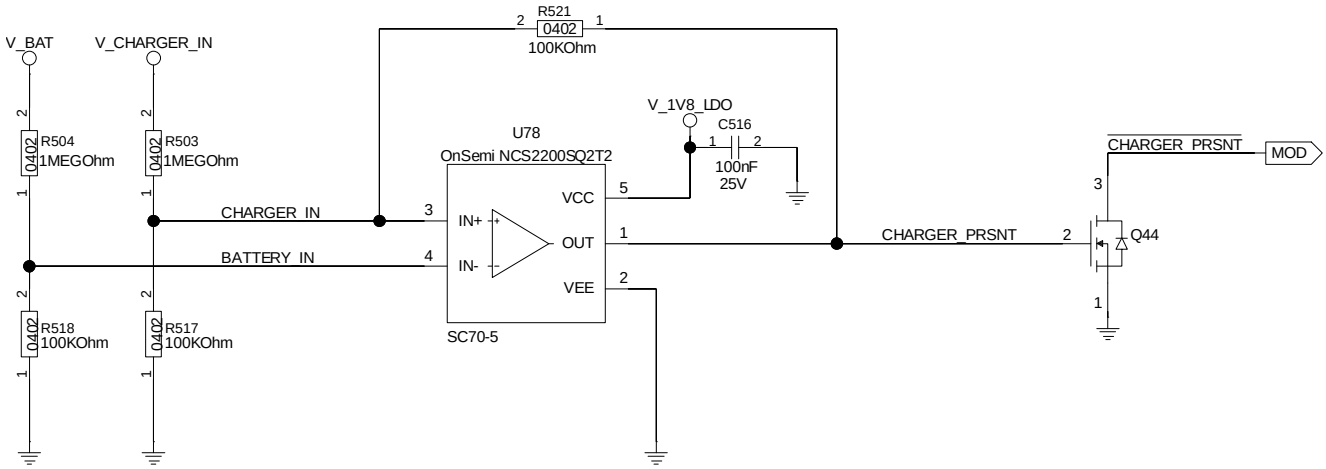
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Figure 69 Battery Fuel Gauge



A comparator circuit such as the one shown below may be used to provide an indication to the SMARC Module that the battery charger power source is present. This circuit may be incorporated into some battery charger ICs.

Figure 70 Charger Present Detection

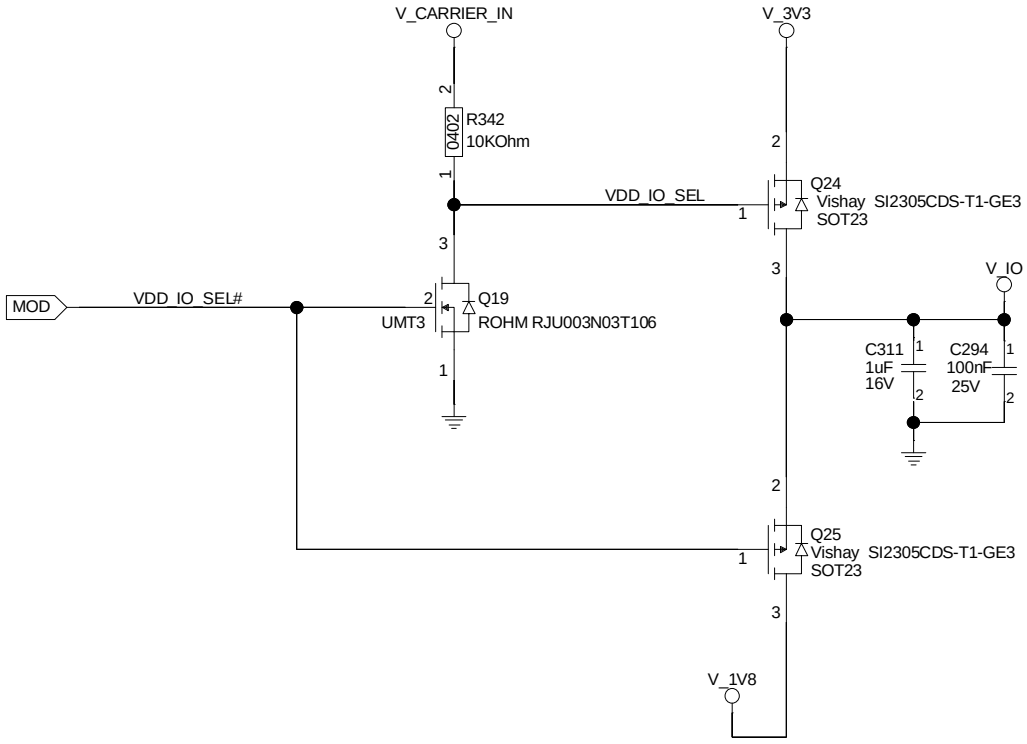


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10.13 V_IO Voltage Switching

The SMARC specification defines V_IO to be either 1.8V or 3.3V. If you want to have a Carrier that can work with either 1.8V or 3.3V I/O, then the circuit below may be used. A Module that is expecting 1.8V I/O will force the VDD_IO_SEL# line low.

Figure 71 V_IO Voltage Switching



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11 THERMAL MANAGEMENT

11.1 General

SMARC Modules generally have modest power dissipations, ranging from 2W to 6W for ARM based designs. Often they can be run in a room-temperature environment for debug and demonstration work without any heat-sinking at all – although this is not generally recommended. In a production environment, heat-sinking is usually necessary to keep the Module electronics die temperatures within limits, at the higher operating temperatures.

11.2 Heat Spreaders

Heat spreaders are available from SMARC Module vendors. Their purpose is to present a uniform thermal interface that is the same across various Module designs. A heat spreader is not a full heat sink – the heat spreader top surface is meant to be in contact with a system specific heat sink, such as the wall of an enclosure or other heat sink.

The figure below diagrams a typical heat spreader suitable for an 82mm x 50mm SMARC Module. The diagram plan view shows the heat spreader surface that the Module interfaces to. “TIM” is an abbreviation for “Thermal Interface Material” - a thermally conductive, compliant material to bridge the small gap between the heat-spreader surface and the surface of the system SOC. The Module is 82mm x 50mm, but the heat spreader is sized at 82mm x 42mm to allow the Module edge fingers to mate to the Carrier board MXM3-style socket. The heat spreader top, or “far side” surface, is 6mm above the Module PCB surface.

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Figure 72 Heat Spreader Example – 82mm x 50mm Module

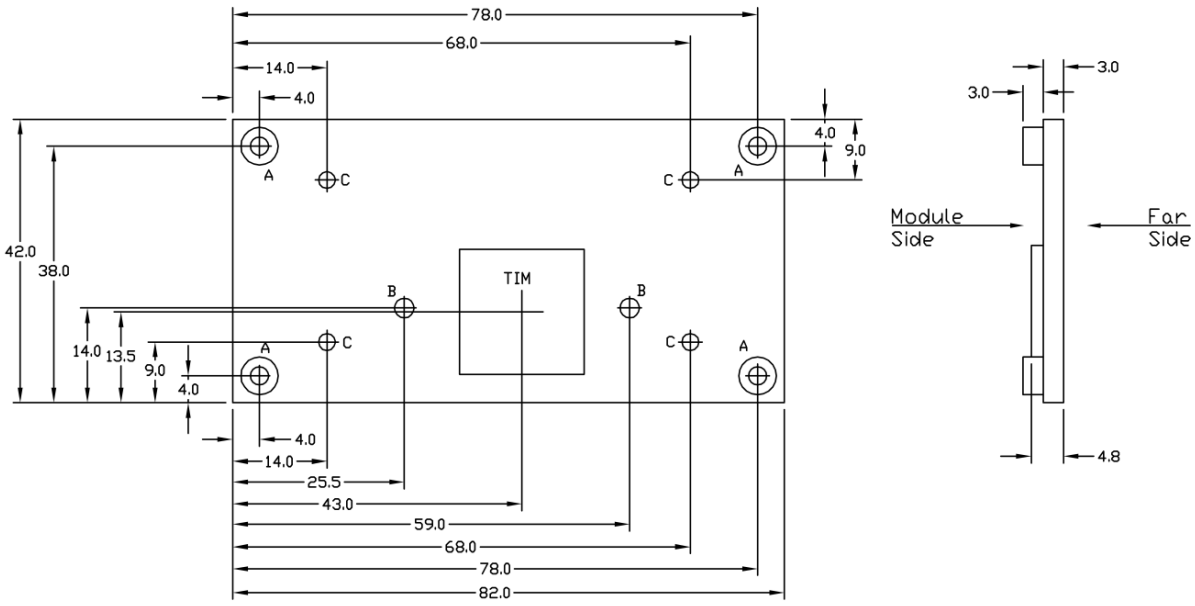


Table 18 Heat Spreader Hole Types

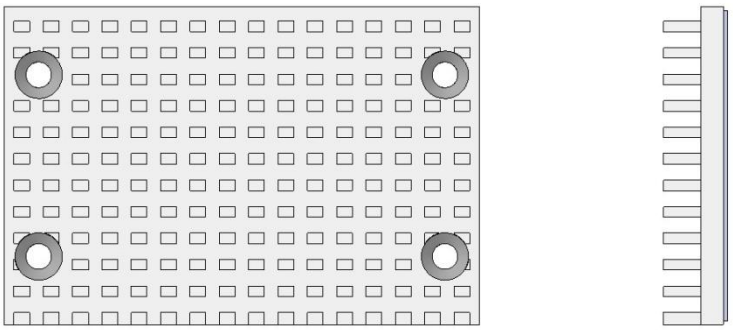
Figure Notation	Hole / Standoff Type	Notes
Holes marked 'A'	Clearance holes for M2.5 screws; 3mm tall clearance standoffs	These holes coincide with the SMARC mounting holes for 82mm x 50mm Modules
Holes marked 'B'		Module design specific holes and standoffs X-Y locations of these holes are also Module design specific. The TIM location is design specific.
Holes marked 'C'	M3 thread in heat spreader	These holes allow either a heat sink to be attached to the heat spreader, or they can allow the heat spreader (and the SMARC Module / Carrier assembly) to be secured to an enclosure wall or other heat-sinking structure.

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11.3 Heat Sinks

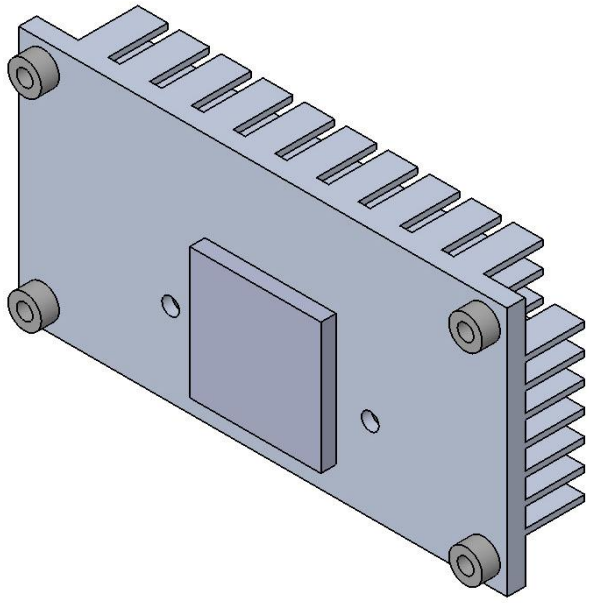
The figure below shows a heat sink that can be added to the heat spreader described in the figure above. This add-on heat sink attaches to the heat spreader through the 'C' holes marked on the heat spreader drawing above. A thermal interface material – thermally conductive paste, grease, or a gap pad – is needed between the heat spreader and the add-on heat sink, on the heat spreader "far" side.

Figure 73 Heat Sink Add-On to Heat Spreader



The best thermal transfer characteristics are usually obtained by a stand-alone heat sink. An example is shown in the following figure. The heat sink is secured to the SMARC Module through two design – specific interior holes (and design specific standoffs) that are straddling the TIM (the TIM in the figure is the square piece of foam that contacts the SMARC SOC). The four corner holes and standoffs coincide with the four SMARC Module holes (for 82mm x 50mm Modules). M2.5 screws pass through the heat-sink corner holes and standoffs, and pass through the SMARC Module, and catch the threads in the corresponding Carrier board hardware. Check with your SMARC Module vendor for the heat sinks that they offer.

Figure 74 Stand-Alone Heat Sink



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11.4 Thermal Resistance Calculations

It is easy to estimate the thermal performance of a SMARC system if you have thermal resistance data from the vendors. The vendor sources can include silicon vendors, SMARC Module and Carrier board vendors and heat sink vendors.

Thermal resistance is a simple concept, analogous to Ohm's law and electrical resistance. Thermal resistance is expressed in degrees Celsius per Watt (^{0}C/W). If a particular thermal interface has a thermal resistance of 8 ^{0}C/W and the source device dissipates 4W, then there will be a temperature rise of 8 * 4 = 32 ^{0}C across that interface.

Some hypothetical thermal parameters are given in the table below, followed by some sample calculations for various situations. The calculations are just estimates, which can be useful for design guidance. The estimates should be followed up by measurements on physical samples. It may be useful to use thermal CAD simulations as well – after the "back of the envelope" calculations and before building hardware.

Table 19 Hypothetical Thermal Parameters

Parameter	Symbol	Value (Hypothetical)
Max SOC junction Temperature(Tj)	$T_{J\text{-}MAX}$	90 ^{0}C
Thermal Resistance, CPU Junction to ambient (θ_{JA})	θ_{JA}	12 ^{0}C/W
Thermal Resistance, CPU Junction to case (θ_{JC})	θ_{JC}	0.4 ^{0}C/W
TIM interface (CPU to heat spreader or sink)	θ_{TM1}	0.5 ^{0}C/W
Heat Spreader	θ_{HS}	0.1 ^{0}C/W
TIM interface (heat spreader to add-on heat sink)	θ_{TM2}	0.4 ^{0}C/W
Add-on Heat Sink - still air (natural convection)	θ_{HS1}	4 ^{0}C/W
Stand-alone Heat Sink – still air (natural convection)	θ_{HS2}	3 ^{0}C/W
SOC maximum power dissipation	$W_{SOC\text{-}MAX}$	5W
Maximum Environmental Temperature	$T_{OP\text{-}MAX}$	To be calculated

Sample Calculations Using Hypothetical Thermal Parameters

No heat sink at all

$$T_{OP\text{-}MAX} = T_{J\text{-}MAX} - \theta_{JA} * W_{SOC\text{-}MAX}$$

$$= 90 - 12 * 5 = 30\ ^0C$$

Heat Spreader + Add-On Heat Sink

$$T_{OP\text{-}MAX} = T_{J\text{-}MAX} - (\theta_{JC} + \theta_{TM1} + \theta_{HS} + \theta_{TM2} + \theta_{HS1}) * W_{SOC\text{-}MAX}$$

$$= 90 - (0.4 + 0.5 + 0.1 + 0.4 + 4) * 5 = 63\ ^0C$$

Heat Spreader + Stand-alone Heat Sink

$$T_{OP\text{-}MAX} = T_{J\text{-}MAX} - (\theta_{JC} + \theta_{TM1} + \theta_{HS2}) * W_{SOC\text{-}MAX}$$

$$= 90 - (0.4 + 0.5 + 3) * 5 = 70.5\ ^0C$$

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12 CARRIER PCB DESIGN RULE SUMMARY

12.1 General – PCB Construction Terms

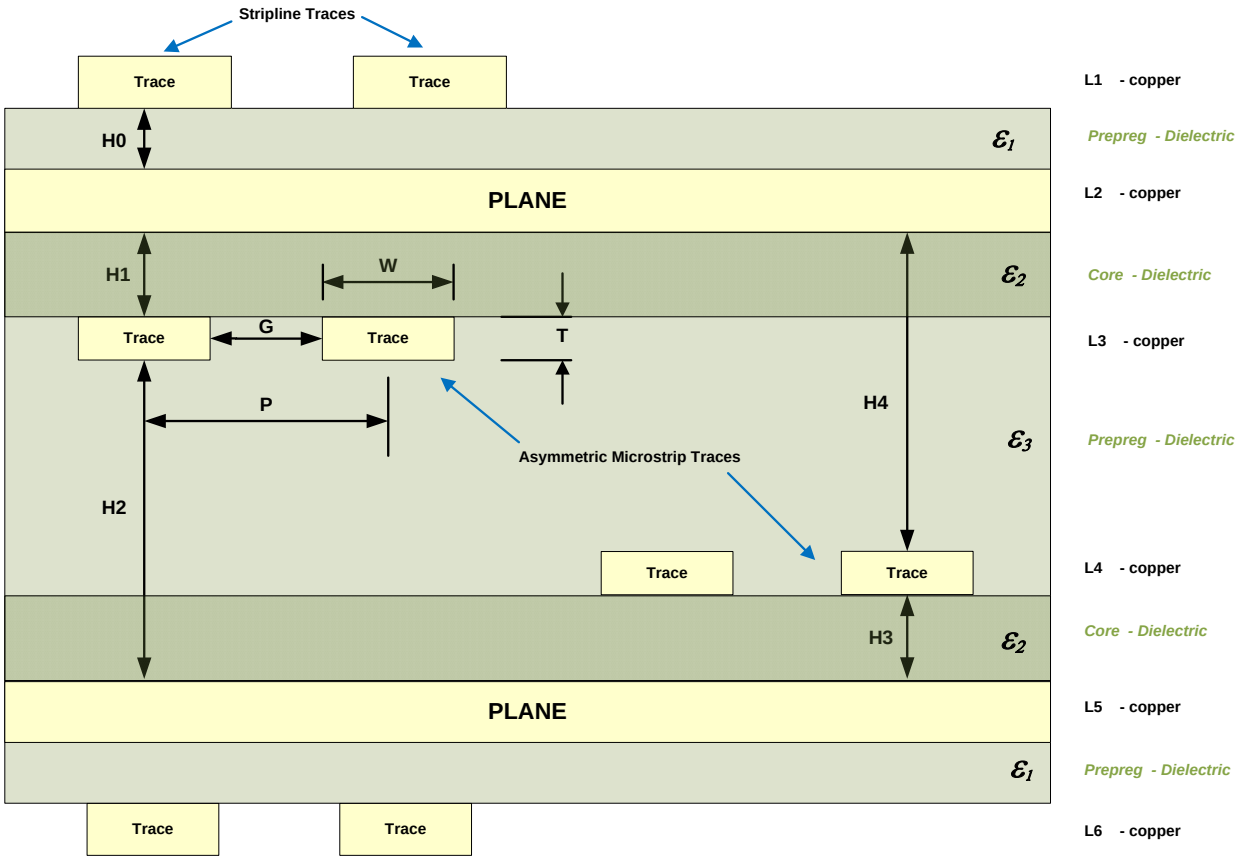
The Table and Figure below serve to define and illustrate some terms used in describing PCB construction and in trace impedances

Table 20 PCB Terms and Symbols

Term / Symbol	Definition
Stripline	Outer layer traces routed a fixed distance above an internal plane layer
Asymmetric Microstrip	Inner layer signal traces, mounted a fixed distance to a Primary Reference Plane (H1 or H3 in the figure below) and mounted a larger distance to a Secondary Reference Plane (H2 or H4 in the figure)
H	Distance (or "height") of a trace to the reference plane(s) – H0, H1, H2 etc. in the figure
W	The width of the trace. Outer layer traces generally need to be a bit wider than inner layer traces to meet the same impedance. It is best to arrange that all inner layer traces for a given impedance class have the same width.
T	The thickness of the trace. Inner layer traces are generally thinner than outer layer traces.
G	The gap (or space) between two traces that are part of an edge-coupled differential pair.
P	The pitch (or center-to-center distance) between two traces that are part of an edge-coupled differential pair. P = G + W for a given differential pair. A fairly common mistake in PCB design and fabrication is to get the pitch and the gap confused.
Clearance	(Not shown in the figure) The distance to "other" traces and features (vias, holes, pours) on the same layer
ε_1 ε_2 ε_3	The dielectric constants of the materials used in the PCB construction
Zo	Trace impedance
SE	Single Ended – trace that is single ended, not part of a differential pair
DE	Differential Ended – trace pair that are used for differential signaling

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Figure 75 PCB Cross Section – Striplines and Asymmetric Microstrips



12.2 Differential Pair Cautions

Modern high speed interfaces (CSI, GBE, HDMI, LCD LVDS, PCIe, SATA, USB) must be routed as differential pairs over a ground plane. They should be routed as a pair on the same layer (edge-coupled pairs) and not as pairs on different layers (known as broad-side coupled pairs) that follow the same X-Y path. There should be a minimum of layer transitions – ideally, just two (SMARC connector to internal layer, and internal layer to the destination connector or IC).

For edge coupled differential pairs, there are several parameters of interest:

- Differential impedance: the impedance of the trace pair as seen by a differential driving source.
- Single impedance: the impedance of one of the traces in the pair, if it were removed from the pair and driven by a single ended source.
- Gap: the inside edge to inside edge spacing between the traces in a differential pair. Labeled ‘G’ in the figure above.
- Pitch: the center-to-center distance between the pairs in a differential pair. Labeled ‘P’ in the figure above.

It is fairly common for people to mix up the Gap and the Pitch. Make sure you don’t make this mistake.

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12.3 General Routing Rules and Cautions

- High speed differential signals must be routed as differential pairs.
    - Keep the pairs symmetrical
    - Stubs are not allowed
    - Avoid tight (right angle) bends
    - Match the pair lengths, on each layer used
- Routing with reference to a GND plane is preferred:
    - If GND plane referencing is not possible, then routing against a well bypassed power plane will have to suffice.
- Do not route over plane splits.
- Layer transitions should be minimized. Ideally, there are a maximum of two vias per net: a transition at the SMARC connector to get to an inner layer, and a transition at the destination device, to get to the device pins.
- If a layer change is made and the layer change results in a reference plane change, then the two reference planes should be tied together in the same vicinity as the trace layer via. If the two reference planes are at different potentials, then they should be tied together through a “stitching capacitor”. The stitching cap isolates the DC potential between the planes but allows the high speed return currents associated with the trace. If the two reference planes are at the same potential, then they should be tied together with a “stitching via” – a seemingly useless via, except that it allows the high frequency trace return currents to flow between the reference planes. Following this advice results in lower EMI (as “loop area” is reduced) and better signal integrity.
- Controlled impedance design must be used:
    - All traces have a single ended (SE) impedance.
    - Differential pair traces have a SE impedance, and the pair has a differential (DE) impedance.
    - Recommended SE and DE impedances are given in the following sections of this Design Guide.
- Differential pairs have pair matching requirements (the two traces that make up a pair need to be matched to a certain tolerance). There are also group matching requirements: if more than one pair is needed for the function, then there are group matching requirements as well (for example LVDS[0]+/- needs to match LVDS[1]+/1 and LVDS[2]+/- and so on).
- The propagation speed of inner layer traces and outer layer traces is different.
- Differential pairs that are part of a common group (for example, the 4 LVDS data pairs in a 24 bit LVDS implementation) should be routed such that each pair in the group has the same per-layer routing length as the others.
- Routing on inner layers may reduce EMI. It is said that good EMI characteristics may be obtained by careful outer layer routing as well.
- Routing high speed traces across plane splits should be avoided. If it can not be avoided, then stitching caps to bridge the split should be used.

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- Cross-talk effects result from traces running in parallel, too close and for too long, either side by side on the same layer, or directly above / beneath each other on adjacent inner layers. For the same layer case, the mitigation is to increase the spacing to other traces. For the adjacent layer case, the traces on the adjacent layers should not run in parallel. Ideally, they are routed orthogonal to each other. If orthogonal routing is not possible, they should be at least 30 degrees off from each other.

- IC power pins need to be properly bypassed, as close as possible to the power pin.

12.4 Trace Parameters for High-Speed Differential Interfaces

Routing rules for high speed differential traces are summarized in the table below. Some notes on the table:

- The “Max Symbol Rate” in the chart below is not the data transfer rate. It is the maximum transition rate on a single differential pair of the link, including the link encoding overhead.
    - For example: 24 bit LCD LVDS is packed into 4 lanes. Including the control bits, there are actually 28 bits packed into the 4 LVDS lanes. There is no encoding overhead in LCD LVDS – it is just raw data – because there is a separate LVDS clock. So the “symbol rate” on an LVDS differential data pair, for a 40 MHz LVD clock, is (28 bits x 40 MHz / 4 lanes) = 280 Mbps.

- The “Sym Width” is the width of the pair Symbol, in pS. It is the inverse of the Max Symbol Rate.
    - Recall that the propagation speed of a msicro-strip (outer layer) trace signal is about 150 pS / inch, and for a stripline (inner layer) trace signal, about 180 pS / inch.
    - The differential pair length mis-match, when expressed in units of time, needs to be small compared to the Symbol Width.

- Lengths are shown in mils (thousandths of an inch, or 0.0254 mm). The American convention for the decimal point and comma meaning is used. The 5,000 mil max length is 5.0 inches or 127 mm.

- “Pair Match” refers to the length matching of the two parts of the differential pair.

- Group Match refers to the length matching of the different pairs in a group.

- N/A means “Not Applicable”.

- “TX/RX Match” means the length matching between the TX and RX pairs.

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Table 21 High-Speed Differential Trace Parameters

Interface	Max Symbol Rate (approximate)	Sym Width (pS)	Zo Diff (ohms)	Zo SE (ohms)	Max Length (mils)	Pair Match (mils)	Group Match (mils)	TX / RX Match (mils)
PCIe	8 Gbps (Gen 3) 5 Gbps (Gen 2) 2.5 Gbps (Gen 1)	125 200 500	92.5	47	5,000 10,000 12,000	< 10	N/A	< 2000
SATA	6 Gbps (Gen 3) 3 Gbps (Gen 2) 1.5 Gbps (Gen 1)	167 333 667	92.5	47	4,000 6,000 8,000	< 10	N/A	< 2000
HDMI	3.4 Gbps (HDMI 1.3) 1.6 Gbps (HDMI 1.2) 1.6 Gbps (HDMI 1.1) 1.6 Gbps (HDMI 1.0)	294 625 625 625	90	45	5,000	< 10	< 830	N/A
CSI	1 Gbps (CSI-2) 208 Mbps (CSI)	1000 4808	90	45	9,000	< 100	< 100	N/A
LVDS	770 Mbps (24b 110 MHz) 280 Mbps (24b 40 MHz)	1299 3571	100	50	10,000	< 100	< 100	N/A
USB 2.0	480 Mbps (HS) 12 Mbps (FS)	2083 23333	90	45	10,000	< 100	N/A	N/A
GBE	25 Mbps	N/A	100	50	4,000	< 50	< 1,000	N/A

Reference Plane: GND is preferred

Clearance to other traces: 20 mil or more

Max Vias: Three maximum; two or less preferred

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12.5 Trace Parameters for Single Ended Interfaces

Table 22 Single Ended Trace Parameters

Interface	Zo SE (ohms)	Max Length (mils)
General	50	12,000
SD Card	50	4,000

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12.6 PCB Construction Suggestions

PCB construction suggestions with trace width and gap parameters are given in the following three tables for 4,6 and 8 layer PCBs. These are meant as a starting point. It is wise to plan ahead with your PCB fabricator and get their input.

Four layer construction is difficult since the high speed signals should be referenced against a GND plane, and the 4 layer construction offers only a single trace layer that is GND referenced.

Table 23 PCB Construction Example - 4 Layers

Layer	Use		Layer Thickness (mils)	Copper (ounces)	Plane Ref	SE 50 Ohm W (mils)	Diff 90 Ohm W / G (mils)	Diff 92.5 Ohm W / G (mils)	Diff 100 Ohm W / G (mils)
		SM	0.8						
L1	Sig	Cu	1.6	0.5 + plating	L2	4.5	4.6 / 6.4	4.5 / 6.5	4.4 / 10
		Prepreg	2.9						
L2	PWR	Cu	1.2	1.0					
		Core	50.0						
L3	GND	Cu	1.2	1.0					
		Prepreg	2.9						
L4	Sig	Cu	1.6	0.5 + plating	L3	4.5	4.6 / 6.4	4.5 / 6.5	4.4 / 10
		SM	0.8						

Finished Thickness: 63.0 mil
Impedance tolerance: +/- 10%

Table 24 PCB Construction Example - 6 Layers

Layer	Use		Layer Thickness (mils)	Copper (ounces)	Plane Ref	SE 50 Ohm W (mils)	Diff 90 Ohm W / G (mils)	Diff 92.5 Ohm W / G (mils)	Diff 100 Ohm W / G (mils)
		SM	0.8						
L1	Sig	Cu	1.6	0.5 + plating	L2	4.5	4.6 / 6.4	4.5 / 6.5	4.4 / 10
		Prepreg	2.9						
L2	PWR	Cu	1.2	1.0					
		Core	3.0						
L3	Sig	Cu	0.6	0.5	L2/L5	4.0	4.0 / 6.5	4.0 / 6.5	3.5 / 8.0
		Prepreg	42.0						
L4	Sig	L6	0.6	0.5	L5/L2	4.0	4.0 / 6.5	4.0 / 6.5	3.5 / 8.0
		Core	3.0						
L5	GND	Cu	1.2	1.0					
		Prepreg	2.9						
L6	Sig	Cu	1.6	0.5 + plating	L5	4.5	4.6 / 6.4	4.5 / 6.5	4.4 / 10
		SM	0.8						

Finished Thickness: 62.2 mil
Impedance tolerance: +/- 10%

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The 8 layer example below shows an 80 mil (2mm) PCB thickness. This is often desirable for Carrier boards, and can be arranged for the 4, 6 or 8 layer versions. The thicker PCB makes for a more rugged system: the ***stiffness*** of a sheet of material (PCB or other sheet material) is proportional to the ***cube*** of the material thickness.

The eight layer construction below offers the advantage of 4 signal layers (L1, L2, L6, L8) that are GND referenced. This is best for high speed signals. This construction also makes power distribution very easy.

The **Pri/Sec** notation in the **Plane Ref** column below means the following: the plane layer to which the signal is closest is the Primary reference plane. The further plane is the Secondary.

If a high speed signal or signal pair changes reference layers (for example, L6 is referenced to L7 and L3 is referenced to L2 - so if you transition from L6 to L3, you are changing reference planes) it is recommended to put in a stitching via or via pair. The stitching vias are single net vias (GND) that tie the two reference planes together (L2 to L6) for the high frequency return signals that are trying to follow the path of the signal traces. You will have better signal integrity and fewer EMI issues if you do this. It is not necessary if reference planes are not being changed (for example, a transition from L1 to L3 keeps both referenced to L2, hence there is no reference plane transition).

Table 25 PCB Construction Example – 8 Layers

Layer	Use		Layer Thickness (mils)	Copper (ounces)	Plane Ref Pri/Sec	SE 50 Ohm W (mils)	Diff 90 Ohm W / G (mils)	Diff 92.5 Ohm W / G (mils)	Diff 100 Ohm W / G (mils)
		SM	0.8						
L1	Sig	Cu	1.6	0.5 + plating	L2	4.5	4.6 / 6.4	4.5 / 6.5	4.4 / 10
		Prepreg	2.9						
L2	GND	Cu	1.2	1.0					
		Core	3.0						
L3	Sig	Cu	0.6	0.5	L2/L4	4.0	4.0 / 6.5	4.0 / 6.5	3.5 / 8.0
		Prepreg	10.0						
L4	PWR	Cu	1.2	1.0					
		Core	38.0						
L5	PWR	Cu	1.2	1.0					
		Prepreg	10.0						
L6	Sig	Cu	0.6	0.5	L7/L5	4.0	4.0 / 6.5	4.0 / 6.5	3.5 / 8.0
		Core	3.0						
L7	GND	Cu	1.2	1.0					
		Prepreg	2.9						
L8	Sig	Cu	1.6	0.5 + plating	L7	4.5	4.6 / 6.4	4.5 / 6.5	4.4 / 10
		SM	0.8						

Finished Thickness: 80.6 mil
Impedance tolerance: +/- 10%

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13 BOM For Schematic Examples

Table 26 BOM For Schematic Examples

QTY	Description	MFG	MPN	Ref Designator
SMARC Module Connector				
1	Conn REC SMT RA MXM 314 Pin 0.5mm Pitch	LOTES	AAA-MXM-008-P03	J1
4	Standoff SMT Reflow Compatible 1.5mm height	PENN Engineering	YSMTSO-27142-ET	
24 Bit Parallel LCD				
1	Conn PLG SMT ST 2x20 1mm Pitch	JST	BM40B-SRDS-A-G-TF(LF)(SN)	J49
1	IC SMT Bus Transceiver BGA-96	TEXAS INSTRUMENTS	SN74AVC32T245ZKER	U1
Module LVDS				
1	Conn REC SMT RA WTB 1x30 1mm pitch	HIROSE	DF19G-30P-1H	J2
1	IC SMT EEPROM 2K SOIC-8	ATMEL	AT24HC02BN-SH-B	U13
1	IC SMT Load Switch 2A BGA-6	TEXAS INSTRUMENTS	TPS22924CYZPR	U3
1	IC SMT 2 Bit Voltage Translator Unidirectional DRV-8	TEXAS INSTRUMENTS	SN74AVC2T244DQER	U9
2	MOSFET Dual N Channel 50V 200mA SOT363-6	DIODES, INC.	BSS138DW-7-F	Q3, Q4
Dual Channel LVDS				
1	FB SMT 120 Ohm 1.2A 90mOhm 0402	TDK	MPZ1005S121CT	FB6
1	Conn REC SMT RA Bottom 1x40 0.8mm Pitch	JAE	FI-NXB40SL-HF10-R3000	J3
1	IC SMT Dual Pixel LVDS Serializer QFN-92	TEXAS INSTRUMENTS	DS90C187LF/NOPB	U15
1	IC SMT Load Switch 2A BGA-6	TEXAS INSTRUMENTS	TPS22924CYZPR	U4
2	MOSFET Dual N Channel 50V 200mA SOT363-6	DIODES, INC.	BSS138DW-7-F	Q5, Q6
USB				
1	IC SMT EEPROM 2K SOIC-8	ATMEL	AT24HC02BN-SH-B	U14
1	IC SMT USB2.0 Hub Controller QFN-64	SMSC (now Microchip)	USB2517I-JZX	U16
1	IC SMT 1 Bit Bus Transceiver SC70-6	TEXAS INSTRUMENTS	SN74LVC1T45DCKR	U17
1	Crystal SMT 24MHz 30/30 ppm 18pF	CALIBER	LF10D18F1-24.000MHZ	Y1
1	Conn REC TH RA Dual USB TypeA	FCI	72309-7024BLF	J4

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QTY	Description	MFG	MPN	Ref Designator
1	IC SMT Power Distribution Switch Dual 500mA SO-8	TEXAS INSTRUMENTS	TPS2052BD	U19
2	Diode SMT ESD Dual 8kV 5A 45W SOT-3	TEXAS INSTRUMENTS	TPD2E009DRTR	D2, D3
2	FB SMT 90 Ohm 0.4A 190mOhm 2012	TDK	ACM2012-900-2P-T002	FB8, FB9
2	FB SMT 30 Ohm 1.7A 50mOhm 0402	TDK	MPZ1005S300CT	L11, L12
1	IC SMT Power Distribution Switch Dual 500mA SO-8	TEXAS INSTRUMENTS	TPD2E009DRTR	D4
1	FB SMT 90 Ohm 0.4A 190mOhm 2012	TDK	ACM2012-900-2P-T002	FB10
1	Conn REC TH RA USB Type A	TE CONNECTIVITY	292303-4	J5
1	FB SMT 30 Ohm 1.7A 50mOhm 0402	TDK	MPZ1005S300CT	L13
1	IC SMT Power Distribution Switch Dual 500mA SO-8	TEXAS INSTRUMENTS	TPS2052BD	U20
1	Conn REC TH RA Dual USB TypeA	FCI	72309-7024BLF	J48
1	IC SMT Power Distribution Switch Dual 500mA SO-8	TEXAS INSTRUMENTS	TPS2052BD	U44
2	Diode SMT ESD Dual 8kV 5A 45W SOT-3	TEXAS INSTRUMENTS	TPD2E009DRTR	D26, D27
2	FB SMT 90 Ohm 0.4A 190mOhm 2012	TDK	ACM2012-900-2P-T002	FB11, FB12
2	FB SMT 30 Ohm 1.7A 50mOhm 0402	TDK	MPZ1005S300CT	L14, L15
1	Diode SMT ESD Dual 8kV 5A 45W SOT-3	TEXAS INSTRUMENTS	TPD2E009DRTR	D1
1	FB SMT 120 Ohm 1.2A 90mOhm 0402	TDK	MPZ1005S121CT	FB1
1	FB SMT 90 Ohm 0.4A 190mOhm 2012	TDK	ACM2012-900-2P-T002	FB7
1	Conn REC SMT RA Micro USB TypeA-B	MOLEX	475900001	J6
1	IC SMT Power Distribution Switch Dual 500mA SO-8	TEXAS INSTRUMENTS	TPS2052BD	U18
2	MOSFET SMT P Channel 8V 5.8A SOT23-3	VISHAY	SI2305CDS-T1-GE3	Q15, Q16
2	MOSFET SMT N Channel 30V 0.3A UMT3	ROHM	RJU003N03T106	Q7, Q8
SATA MO-300				
1	LED SMT GREEN CLEAR 2V 30mA	LITE ON	LTST-C190KGKT	D9
1	Conn SMT REC Mini PCI Exp 2x26 0.8mm Pitch	MOLEX	67910-0002	J21
1	Conn SMT Latch Mini PCI Exp 2x1	MOLEX	48099-4000	J24

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QTY	Description	MFG	MPN	Ref Designator
MINI-PCIe				
1	Conn SMT ST HINGED SIM 2x3 2.54mm pitch	MOLEX	470230001	J19
1	Conn SMT REC Mini PCI Exp 2x26 0.8mm Pitch	MOLEX	67910-0002	J20
1	Conn SMT Latch Mini PCI Exp 2x1	MOLEX	48099-4000	J22
1	Conn SMT Latch Mini PCI Exp 2x1	MOLEX	48099-4000	J23
HDMI				
1	Conn SMT REC RA HDMI Type A 19 Pin 0.5mm Pitch	FCI	10029449-001TLF	J25
1	IC SMT HDMI Buffer TSSOP-24	TEXAS INSTRUMENTS	TPD12S016PWR	U22
Micro SD				
1	Conn TH PLG ST 1x2 2.54mm pitch	FCI	77311-118-02LF	J26
1	Conn SMT RA Micro SD Card 8 Pin 1.1 mm Pitch	MOLEX	503398-0891	J27
1	IC SMT Load Switch 2A BGA-6	TEXAS INSTRUMENTS	TPS22924CYZPR	U2
2	Diode SMT 4 Channel TVS Array 1.6mm x 1.6mm	SEMTECH	RCLAMP0504PATCT	D6, D7
RTC Battery				
1	Conn SMT CR2032 Battery Holder	RENATA BATTERIES	SMTU2032-LF	BT1
1	Diode SMT Schottky 30V 200mA SOD123	VISHAY	BAT54W-V-GS08	D12
Intel GBE Controller				
1	IC SMT GBE Controller 0.85mm QFN-64	INTEL	WGI210AT	U55
1	IC SMT 4Mbit SPI Flash 150 mil SOIC-8	SST	SST25VF040B-80-4I-SAE	U56
1	Crystal SMT 25MHz 20/50 ppm 18pF	PLETRONICS	SM12T2-18-25.000M-20H1LK	Y4
2	MOSFET Dual N Channel 50V 200mA SOT363-6	DIODES, INC.	BSS138DW-7-F	Q29, Q30
GBE				
1	Conn REC TH RA RJ45 with Magnetics and LED	BEL FUSE	L829-1J1T-43	J29
GBE with POE				
1	Transient Suppressor SMT 58V 400W DO-215AB	ST MICRO	SMAJ58CA	D15
1	Conn REC TH RA RJ45 1000Base-T with Magnetics LED	PULSE	JXK0-0190NL	J28

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QTY	Description	MFG	MPN	Ref Designator
1	Module TH POE 30W 14 Pin 2.54mm Pitch	SILVERTEL	AG9330	PS1
1	IC SMT Optocoupler PDIP-4	SHARP	PC817X1NIP0F	U23
2	Diode SMT Bridge Rectifier 100V 2A PDIP-4	COMCHIP	CDBHD2100-G	D13, D14
2	IC SMT Single Buffer Three State SOT23-5	FAIRCHILD	NC7SZ125M5X	U57, U58
Audio Codec				
1	Diode SMT 4 Channel TVS Array 1.6mm x 1.6mm	SEMTECH	RCLAMP0504PATCT	D8
1	Conn PLG SMT RA Shrouded 1x4 1mm Pitch	JST	SM04B-SRSS-TB(LF)(SN)	J30
1	IC SMT Audio Codec QFN-40	WOLFSON MICRO	WM8903LGEFK/RV	U24
1	OSC SMT 12MHz 50ppm 3.3V QFN-4	ABRACON	ASEMB-12.000MHZ-LC-T	Y3
2	FB SMT 120 Ohm 1.2A 90mOhm 0402	TDK	MPZ1005S121CT	FB4, FB5
2	Conn REC TH RA 3.5mm Audio Single port	CUI	SJ-43514	J31, J32
4	Conn PLG SMT RA Shrouded 1x3 1mm Pitch	JST	SM03B-SRSS-TB(LF)(SN)	J11, J12, J13, J14
Audio Amplifier				
1	IC SMT 2 Bit Voltage Translator Unidirectional DRV-8	TEXAS INSTRUMENTS	SN74AVC2T244DQER	U5
2	Conn SMT PLG RA 1A 50V 1x2 1mm Pitch	JST	SM02B-SRSS-TB(LF)(SN)	J17, J18
2	IC SMT Speaker Driver 1W Dual mode Class AB/D QFN-16	WOLFSON MICRO	WM9001GEFL/R	U25, U26
6	FB SMT 30 Ohm 1.7A 50mOhm 0402	TDK	MPZ1005S300CT	L5, L6, L7, L8, L9, L10
TI Audio Codec and Amplifie				
1	Diode SMT 4 Channel TVS Array 1.6mm x 1.6mm	SEMTECH	RCLAMP0504PATCT	D5
1	Conn REC SMT RA 3.5mm Audio Black 6 Conductor	CUI	SJ-43516-SMT	J7
1	IC SMT Audio Codec Stereo VQFN-32	TEXAS INSTRUMENTS	TLV320AIC3105IRHBR	J8
1	IC SMT 2.8-W/Ch Stereo Class-D Audio Amp QFN-20	TEXAS INSTRUMENTS	TPA2016D2RTJR	U21
1	OSC SMT 12MHz 50ppm 3.3V QFN-4	ABRACON	ASEMB-12.000MHZ-LC-T	Y2
2	FB SMT 120 Ohm 1.2A 90mOhm 0402	TDK	MPZ1005S121CT	FB2, FB3
2	Conn SMT PLG RA 1A 50V 1x2 1mm Pitch	JST	SM02B-SRSS-TB(LF)(SN)	J15, J16

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QTY	Description	MFG	MPN	Ref Designator
2	Conn PLG SMT RA Shrouded 1x3 1mm Pitch	JST	SM03B-SRSS-TB(LF)(SN)	J9, J10
4	FB SMT 30 Ohm 1.7A 50mOhm 0402	TDK	MPZ1005S300CT	L1, L2, L3, L4
eMMC Flash and SPI Flash socket				
1	Conn SMT ST SPI Flash socket SOIC-8	LOTES	ACA-SPI-004-T02	J33
	IC 64 Mbit 1.8V SPI Flash Memory	Winbond	W25Q64W	
1	IC SMT NAND Flash 16GB TFBGA-169	SANDISK	SDIN5D2-16G-L	U43
AFB Mezzanine				
1	Conn REC SMT ST 2x20 0.5mm Pitch	SAMTEC	QSH-020-01-L-D-DP-A	J35
2	MOSFET Dual N Channel 50V 200mA SOT363-6	DIODES, INC.	BSS138DW-7-F	Q1, Q2
CAN Transceivers				
1	Conn PLG SMT RA 1x4 1.25mm Pitch	MOLEX	53261-0471	J37
1	IC SMT CAN Transceiver SOIC-14	ON SEMI	NCV7341D20G	U27
2	Transient Suppressor SMT 6V SOD923	ALPHA & OMEGA SEMI	AOZ8231NI-05L	D16, D17
2	IC SMT 2 Bit Voltage Translator Unidirectional DRV-8	TEXAS INSTRUMENTS	SN74AVC2T244DQER	U6, U7
1	Conn PLG SMT RA 1x4 1.25mm Pitch	MOLEX	53261-0471	J47
1	IC SMT CAN Transceiver SOIC-14	ON SEMI	NCV7341D20G	U40
2	Transient Suppressor SMT 6V SOD923	ALPHA & OMEGA SEMICONDUCTOR, INC	AOZ8231NI-05L	D18, D19
Serial Ports				
2	IC SMT 2 Bit Voltage Translator Unidirectional DRV-8	TEXAS INSTRUMENTS	SN74AVC2T244DQER	U37, U38
2	IC SMT RS232 Transceiver QFN-32	TEXAS INSTRUMENTS	TRS3253EIRSMR	U35, U36
4	Conn PLG SMT RA Shrouded 1x5 1mm Pitch	JST	SM05B-SRSS-TB(LF)(SN)	J39, J40, J41, J42
Camera Mezzanine				
1	Conn REC SMT ST 2x30 0.4mm Pitch	HIROSE	FX12B-60P-0.4SV	J43
I2C Devices				
1	IC SMT 2 Bit Voltage Translator MicroPak-8	FAIRCHILD	FXMA2102L8X	U29

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QTY	Description	MFG	MPN	Ref Designator
1	IC SMT Accelerometer/Magnetometer LGA-14	ST MICRO	LSM303DLHC	U30
1	IC SMT Gyroscope MEMS 3 Axis LGA-16	ST MICRO	L3G4200D	U31
1	IC SMT Accelerometer 3Axis LGA-14	ST MICRO	LIS302DL	U32
EEPROMS				
3	IC SMT EEPROM 2K SOIC-8	ATMEL	AT24HC02BN-SH-B	U10, U11, U12
I2C_PM EEPROM				
1	IC SMT LDO 500mA SOT23-6	MAXIM	MAX1818EUT18+T	U39
2	MOSFET Dual N Channel 50V 200mA SOT363-6	DIODES, INC.	BSS138DW-7-F	Q17, Q18
2	IC SMT EEPROM 32K TSSOP-8	ATMEL	AT24C32D-XHM-T	U41, U42
IO Expanders				
1	IC SMT I2C Expander 8-bit TSSOP-16	TEXAS INSTRUMENTS	TCA9554PWR	U34
Miscellaneous				
3	Conn TH PLG ST 1x2 2.54mm pitch	FCI	77311-118-02LF	J44, J45, J46
3	Switch TH ST Tactile SPST 0.02A 15V	PANASONIC	EVQPBC04M	SW1, SW2, SW3
6	Diode SMT Schottky 30V 200mA SOT23	NXP	BAT54S,215	D20, D21, D22, D23, D24, D25
Power Supply 1				
1	Conn PLG TH RA Shrouded 1x4 4.2mm Pitch	MOLEX	39303045	J52
1	Inductor SMT 3.3uH 8.4A 20.81 mOhm 2525	COILCRAFT	XAL6030-332MEC	L17
1	Inductor SMT 1.5uH 4.4A 15.8 mOhm 1616	COILCRAFT	XFL4020-152MEC	L18
1	IC SMT Load Switch 6A SON-8	TEXAS INSTRUMENTS	TPS22965DSGR	U54
2	LED SMT GREEN CLEAR 2V 30mA	LITE ON	LTST-C190KGKT	D29, D30
2	Diode SMT Switching 75V 300mA SOD523	FAIRCHILD	1N4148WT	D35, D36
2	MOSFET SMT N Channel 30V 0.3A UMT-3	ROHM	RJU003N03T106	Q21, Q22
2	IC SMT Buck Boost Adjustable 3A QFN-14	TEXAS INSTRUMENTS	TPS63020DSJR	U47, U48

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QTY	Description	MFG	MPN	Ref Designator
Power Supply 2				
1	LED SMT GREEN CLEAR 2V 30mA	LITE ON	LTST-C190KGKT	D31
1	Diode SMT Schottky 30V 2A PowerDI 123	DIODES, INC.	DFLS230L-7	D37
1	Diode SMT Schottky 30V 2A DO-214AA	VISHAY	SS23-E3/52T	D38
1	Inductor SMT 10uH 3A 105 mOhm 2525	VISHAY	IHLP2525CZER100M01	L19
1	Inductor SMT 15uH 6A 40.9 mOhm 4040	VISHAY	IHLP4040DZER150M11	L20
1	Inductor SMT 6.8uH 13A 8.98 mOhm 12.1x11.4mm	WUERTH ELEKTRONIK	7443320680	L21
1	MOSFET SMT P Channel 8V 5.8A SOT23-3	VISHAY	SI2305CDS-T1-GE3	Q26
1	IC SMT 2 Bit Voltage Translator Unidirectional DRV-8	TEXAS INSTRUMENTS	SN74AVC2T244DQER	U45
1	IC SMT Buck Regulator Adjustable 600mA SON-10	TEXAS INSTRUMENTS	TPS62020DRCR	U49
1	IC SMT LED Backlight Driver WQFN-24	NATIONAL SEMICONDUCTOR	LP8545SQX/NOPB	U50
1	IC SMT Boost Regulator Adjustable 3.2A VSON-10	TEXAS INSTRUMENTS	TPS61087DRC	U51
2	MOSFET SMT N Channel 30V 0.3A UMT-3	ROHM	RJU003N03T106	Q23, Q28
Power Supply 3				
1	LED SMT GREEN CLEAR 2V 30mA	LITE ON	LTST-C190KGKT	D28
1	Inductor SMT 1uH 9.6A 14.6 mOhm 1616	COILCRAFT	XAL4020-102MEC	L16
1	IC SMT Buck Regulator Adjustable 3A QFN-16	TEXAS INSTRUMENTS	TPS53310RGTR	U46
2	MOSFET SMT N Channel 30V 0.3AUMT-3	ROHM	RJU003N03T106	Q19, Q20
2	MOSFET SMT P Channel 8V 5.8A SOT23-3	VISHAY	SI2305CDS-T1-GE3	Q24, Q25
Optional Power connector with filtering and Optional Hot swap Controller				
1	Transient suppressor SMT 40.2V 600W DO-214AA	VISHAY	P6SMB47CA-E3/52	D32
1	FB SMT 96 Ohm 10A 4mOhm 3312	WUERTH ELEKTRONIK	74279225101	FB13
1	Choke SMT Common Mode170 Ohm 20A 10x8.5mm	LAIRD	CM3440Z171R-10	I1
1	Conn TH PLG ST 1x2 2.54mm pitch	FCI	77311-118-02LF	J50
1	Conn PLG TH RA 1x3 3.81mm	TE CONNECTIVITY	284541-3	J51

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QTY	Description	MFG	MPN	Ref Designator
1	MOSFET SMT N Channel 100V 40A TO-263	VISHAY	SUM40N10-30-E3	Q27
1	Switch TH RA Rocker SPDT 3A 28V	E-SWITCH	400MSP1R1BLKM7QE	SW4
1	IC SMT 2 input positive NAND Gate SC70-5	TEXAS INSTRUMENTS	SN74AHC1G00DCKR	U52
1	IC SMT Hot Swap Controller MSOP-10	TEXAS INSTRUMENTS	LM5060MM/NOPB	U53
2	Diode SMT Schottky 40V 5A SMC	ON SEMI	MBRS540T3G	D33, D34
2	Diode SMT Zener 3.3V 250mA 225mW SOT23-3	ON SEMI	BZX84C3V3LT1G	D39, D40
1	IC LDO 3.3V 50mA SOIC8	TEXAS INSTRUMENTS	LM9036MX-3.3	U76
High Speed Serial Port				
1	IC Logic CMOS XOR-GATE SOT353-5	FAIRCHILD	NC7SZ86P5X	U72
1	Conn Plug1X6 SMT RA 1mm Pitch	JST	SM06B-SRSS-TB(LF)(SN)	J61
1	Conn Plug1X5 SMT RA 1mm Pitch	JST	SM05B-SRSS-TB(LF)(SN)	J60
1	IC RS232 SMT TSSOP-20	MAXIM	MAX13235EEUP+	U70
1	IC RS485 SMT TSSOP-24	MAXIM	MAX13451EAUD+	U71
1	Conn Plug 2x2 SMT RA 2.54mm Pitch	3M	961204-6300-AR-TP	J62
Touch Controller and I2S Isolation Logic				
2	IC Level Shifter SMT SOT553	TEXAS INSTRUMENTS	SN74AVC1T45DRLR	U73 U74
2	MOSFET NMOS 50V 200mA SOT363	DIODES INC.	BSS138DW-7-F	Q31 Q32

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QTY	Description	MFG	MPN	Ref Designator
1	Conn Socket 1x10 SMT RA 1.25mm Pitch	MOLEX	53261-1071	J63
1	IC Level Shifter SMT SOT553 MicroPak8	FAIRCHILD	FXMA2102L8X	U75
Touch Controller and I2S Isolation Logic				
2	IC Level Shifter SMT SOT553	TEXAS INSTRUMENTS	SN74AVC1T45DRLR	U73 U74
2	MOSFET NMOS 50V 200mA SOT363	DIODES INC.	BSS138DW-7-F	Q31 Q32
1	Conn Socket 1x10 SMT RA 1.25mm Pitch	MOLEX	53261-1071	J63
1	IC Level Shifter SMT SOT553 MicroPak8	FAIRCHILD	FXMA2102L8X	U75
Battery Charger and Fuel Gauge				
2	Sense Resistor 10mOhm 1% 1W SMT 2512	VISHAY	WSL2512R0100FEA	RS1 RS2
2	MOSFET NMOS 25V 60A QFN8	TEXAS INSTRUMENTS	CSD16406Q3	Q40 Q46
1	Diode Schottky 70V 70mA SMT SOT23	ST MICRO	BAS70-05FILM	D52
1	IC Battery Charger SMT QFN24	TEXAS INSTRUMENTS	BQ24171RGYR	U77
4	MOSFET NMOS 30V 0.3A UMT3	ROHM	RJU003N03T106	Q41 Q42 Q43 Q44
1	MOSFET PMOS 20V 14A SON8	TEXAS INSTRUMENTS	CSD25401Q3	Q47
1	IC Comparator SMT SC70-5	ON SEMI	NCS2200SQ2T2G	U78
1	Polyfuse 2.6A 16V SMT 1812	BEL FUSE	0ZCC0260BF2B	F1

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QTY	Description	MFG	MPN	Ref Designator
1	Conn DC Jack 2.5mm 3 Pin THT	KYCON	KLDHCX-0202-B	J64
1	Sense Resistor 10mOhm 1% 1W SMT 2512	VISHAY	WSL2512R0100FEA	RS3
1	IC Fuel Gauge SMT SON12	TEXAS INSTRUMENTS	BQ27510DRZR-G2	U79
1	MOSFET NMOS 30V 0.3A UMT3	ROHM	RJU003N03T106	Q45
High Voltage Power Spplies				
2	Diode Schottky 40V 350mA SMT SOD323	DIODES INC.	SD103AWS-7-F	D56 D57
1	Diode Zener 5.1V 50mA SMT SOT23-5	ON SEMI	BZX84C5V1LT1G	D55
1	IC Switching Regulator 1.5-22V 8A SMT QFN22	TEXAS INSTRUMENTS	TPS53318DQPT	U81
2	IC Regulator Adjustable 25A SMT QFN16	LINEAR TECHNOLOGY	LTC3879IUD#PBF	U80 U81
4	MOSFET NMOS 40V 35A SON8 LFPAK5	RENESAS	RJK0451DPB-00-J5	Q48 Q49 Q50 Q51

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