Smart Mobility ARChitecture

Hardware Specification



Version 1.1 May 29, 2014



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REVISION HISTORY

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1.0	Dec. 20, 2012	S.Milnor / Kontron	Initial release
1.1	May 29, 2014	S.Milnor / Kontron	Change notes for V1.0 to V1.1 are at the end of this document

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INTRODUCTION

1.1 General Introduction

The SMARC ("Smart Mobility ARChitecture") is a versatile small form factor computer Module definition targeting applications that require low power, low costs, and high performance. The Modules will typically use ARM SOCs similar or the same as those used in many familiar devices such as tablet computers and smart phones. Alternative low power SOCs and CPUs, such as tablet oriented X86 devices and other RISC CPUs may be used as well. The Module power envelope is typically under 6W although designs up to about 15W are possible.

Two Module sizes are defined: 82mm x 50mm and 82mm x 80mm. The Module PCBs have 314 edge fingers that mate with a low profile 314 pin 0.5mm pitch right angle connector (the connector is sometimes identified as a 321 pin connector, but 7 pins are lost to the key).

The Modules are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE and a single channel LVDS display transmitter are concentrated on the Module. The Modules are used with application specific Carrier Boards that implement other features such as audio CODECs, touch controllers, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

Applications include:

- Mobile systems
- Industrial tablets
- HMI systems
- Instrumentation
- Gaming and Infotainment
- Medical devices
- Portable, application specific tools

1.2 SMARC vs. COM Express

COM Express ® is a very successful Computer Module standard that is optimized for PC Architecture embedded systems. The COM Express feature set exploits contemporary PC chipsets very well. There is support for lots of USB, lots of PCI Express lanes, PCI Express Graphics, the LPC bus and the PCI bus. There are power pins supporting over 100W.

The SMARC targets lower power, small form factor systems. The SMARC pin out is optimized for the features common to ARM CPUs and not common to the PC world. Some of these features include parallel LCD display interfaces; serial and parallel camera input provisions; multiple I2C, I2S and serial port options; USB client / host mode (OTG) operation; SD and eMMC card operation.

The SMARC does include some of the features found in COM express, such as a limited number of PCIe, SATA and USB ports - but the mix is different, allowing many features of interest that COM Express does not support to be brought out on the SMARC.

1.3 Purpose of This Document

This document defines the Module mechanical, electrical, signal and thermal parameters at a level of detail sufficient to provide a framework for SMARC Module and Carrier Board designs.

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1.4 Document and Standards References

- ***BT.656 ("Recommendation ITU-R BT.656-5 Interface for digital component video signals in 525-line and 625-line television systems operating at the 4:2:2 level of Recommendation ITU-R BT.601"),*** International Telecommunications Union, December 2007 (**www.itu.int**)

- ***CAN ("Controller Area Network") Bus Standards – ISO 11898, ISO 11992, SAE J2411***

- ***CSI-2 (Camera Serial Interface version 2)*** The CSI-2 standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Alliance") (**www.mipi.org**)

- ***COM Express*** – the formal title for the COM Express specification is ***"PICMG® COM.0 COM Express Module Base Specification",*** Revision 2.0, August 8, 2010. This standard is owned and maintained by the PICMG ("PCI Industrial Computer Manufacturer's Group") (**www.picmg.org**)

- ***DisplayPort*** and ***Embedded DisplayPort*** These standards are owned and maintained by VESA ("Video Electronics Standards Association") (**www.vesa.org**)

- ***D-PHY*** CSI-2 physical layer standard – owned and maintained by the MIPI Alliance (**www.mipi.org**)

- ***DSI (Display Serial Interface)*** The DSI standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Alliance") (**www.mipi.org**)

- ***eMMC ("Embedded Multi-Media Card")*** The eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (**www.jedec.org**)

- ***Fieldbus*** - this term refers to a number of network protocols used for real – time industrial control. Refer to the following web sites: **http://www.profibus.com/downloads/** and **http://www.canopen.org/**

- ***GBE MDI ("Gigabit Ethernet Medium Dependent Interface")*** This is defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (**www.ieee.org**)

- ***HDMI Specification***, Version 1.3a, November 10, 2006 © 2006 Hitachi and other companies (**www.hdmi.org**)

- ***The I2C Specification,*** Version 2.1, January 2000, Philips Semiconductor (now NXP) (**www.nxp.com**)

- ***I2S Bus Specification,*** Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (**www.nxp.com**)

- ***JTAG ("Joint Test Action Group")*** This is defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (**www.ieee.org**)

- ***Media Local Bus Specification***, Version 4.2. December 2010, © SMSC. Also referred to as "MLB" and "MediaLB". This describes the physical layer used for the MOST Bus. (**www.smsc-ais.com**)

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- ***MOST ("Media Oriented Systems Transport") Specification***, Version 3.0 E2, July 2010, MOST Corporation (**www.mostcooperation.com**)
- ***The MOST Book ("MOST The Automotive Multimedia Network – From MOST25 to MOST150"),*** © 2011 Francis Verlag GmbH and MOST Cooporation (**www.mostcooperation.com**)
- ***MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification,*** Version 3.0, Revision 1.1, © 2009 NVidia Corporation (**www.mxm-sig.org**)
- ***PICMG® EEEP Embedded EEPROM Specification,*** Rev. 1.0, August 2010 (**www.picmg.org**)
- ***PCI Express Specifications*** (**www.pci-sig.org**)
- ***Serial ATA Revision 3.1***, July 18, 2011, Gold Revision, © Serial ATA International Organization (**www.sata-io.org**)
- ***SD Specifications Part 1 Physical Layer Simplified Specification,*** Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association ("Secure Digital") (**www.sdcard.org**)
- ***SPDIF (aka S/PDIF) ("Sony Philips Digital Interface)- IEC 60958-3***
- ***SPI Bus –*** "Serial Peripheral Interface" – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (**http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus**)
- ***USB Specifications*** (**www.usb.org**)

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2 MODULE OVERVIEW

2.1 Form Factor Feature Summary

- Small form factor, low profile and low power edge-finger card format Module with pin-out optimized for ARM architecture processors; may also be used with low power, tablet oriented X86 and RISC devices.

- Two Module sizes:

    - 82mm x 50mm
    - 82mm x 80mm

- Carrier Board connector: 314 pin 0.5mm pitch R/A memory socket style connector

    - Originally defined for use with MXM3 graphics cards
    - SMARC Module pin-out is separate from and not related to MXM3 pin-out
    - Multiple sources for Carrier Board connector
    - Low cost
    - Low profile:
        - As low as 1.5mm (Carrier Board top to Module bottom)
        - Other stack height options available, including 2.7mm, 5mm, 8mm
        - Overall assembly height (Carrier Board top to tallest Module component) is less than 6mm
    - Excellent signal integrity – suitable for 2.5 GHz / 5 GHz data rate signals such as PCIe Gen 1 and Gen 2.
    - Robust, vibration resistant connector

- Module input voltage range: 3.0V to 5.25V

    - Allows operation from 3.6V nominal Lithium-ion battery packs
    - Allows operation from 3.3V fixed DC supply
    - Allows operation from 5.0V fixed DC supply
    - Single supply (no separate standby voltage)
    - Module power pins allow 5A max, or 15W max input power at 3.0V

- Low power designs

    - 2 to 6W typical Module power draw during active operation
    - Fanless
    - Passive cooling
    - Low standby power
    - Design for battery operation
    - 1.8V default I/O voltage

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2.2 Module Interface Summary

The interfaces listed below are available per the Module pin definition. Some features are optional and availability is Module design dependent.

- Display Interfaces
    - 24 bit parallel RGB LCD data and control signals
    - Single channel LVDS LCD 18 or 24 bit (usually derived from SOC parallel LCD data)
        - Panel support signals (I2C, Power Enables, PWM)
        - 2nd LVDS channel may be implemented on Carrier board
        - Support for dual channel implementations
    - Future migration to eDP defined by pin-sharing with LVDS LCD
    - HDMI port – full featured implementation

- Camera Interfaces
    - Serial configuration: CSI (2 lane) + CSI (2 or 4 lane)
    - Parallel configuration: Parallel 10, 12, 16 bit or dual 8 bit input motion video or still images

- SDIO Interfaces
    - Two SDIO interfaces
        - 4 bit SDIO card interface with support lines
        - 8 bit eMMC interface with support lines
            - Off-module boot from eMMC (optional)

- SPI Interfaces
    - Two SPI interfaces
        - One designated for (optional) off-module boot use

- I2S Interfaces
    - Three I2S interfaces
        - Typically used for connection to I2S audio CODECs
        - Also useful for connection to peripherals such as baseband modems, touch controllers, etc.
        - One of the 3 designated for optional use with an HDA CODEC

- I2C Interfaces
    - Four I2C interfaces
        - Power Management
        - General Purpose
        - Camera
        - LCD Display ID
    - HDMI interface also has private I2C interface for HDMI use

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(Module Interface Summary continued)

- Asynchronous Serial Port Interfaces
    - Four asynchronous serial ports
        - Two with 2 wire handshake (RXD, TXD, RTS#, CTS#)
        - Two with data only (RXD, TXD)
        - Logic level interface

- CAN Bus Interfaces
    - Two CAN bus interfaces
        - Logic level signals from Module based CAN bus protocol controllers
        - RXD, TXD only
        - Two Module GPIOs are designated for optional use as CAN bus error status inputs

- USB Interfaces
    - Three ports total
    - One port allows USB 2.0 OTG (USB client or host)
    - Two ports allow USB 2.0 Host operation (Full Speed and High Speed)
    - USB support signals (VBUS enable / Over-current detects, OTG support signals)

- PCI Express
    - Three PCIe x1 links
    - PCIe Gen1 or Gen 2 (Module dependent)
    - Reference clock pair for each PCIe link
    - Full set of PCIe support signals for each link (CLKREQ#, PCIE_RESET#, presence detects)
    - May be configured as PCIe target if Module chipset allows this
    - Common PCIe wake signal

- SATA Interface
    - One SATA interface
    - Gen 1, 2 or 3 (Module dependent)

- Gigabit Ethernet
    - One analog GBE MDI interface
    - No magnetics on Module
    - LED support signals
    - CTREF (center tap reference voltage) for Carrier magnetics (if required by the Module GBE PHY)

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(Module Interface Summary continued)

- SPDIF Interfaces
    - SPDIF_IN and SPDIF_OUT available for audio use
- Watchdog Timer Interface
- General Purpose I/O
    - Twelve GPIO signals
    - Specific alternate functions are assigned to some GPIOs
        - PWM / Tachometer capability
        - Camera support
        - CAN Error Signaling
        - HD Audio reset
- System and Power Management Signals
    - Reset out and Reset in
    - Power button in
    - Power source status
    - Module power state status
    - System management pins
    - Battery and battery charger management pins
    - Carrier Power On control
- Boot Source Select
    - Three pins to allow selection from Carrier Board
    - Select options to include boot from one of the following:
        - Module SPI
        - Module eMMC Flash
        - Module NAND / NOR Flash (vendor defined)
        - Module Remote Boot (Network or Serial Port, vendor defined)
        - Carrier SPI
        - Carrier eMMC
        - Carrier SD Card
        - Carrier SATA

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(Module Interface Summary continued)

- Alternate Function Block (AFB)
    - A set of 20 signal pins is set aside for Alternate functions. The AFB pins include pin sets suitable for up to 5 high speed differential pairs, and ten single ended signals.
    - The AFB pins may be assigned to specific roles in a future version of this specification. The possibilities include
        - MIPI DSI interface
        - USB SuperSpeed interface
        - Other high speed serial interface
    - There may be application specific use of the AFB, as listed below.
        - MOST (“Multimedia Oriented System Transport”) Bus AFB
        - Dual GBE AFB
        - Industrial Network / Fieldbus AFB
- JTAG functions for CPU debug and test are implemented on separate small form factor connector(s)

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2.3 Pin Group Summary

The following table summarizes the major pin groupings and shows the pin count associated with supporting the group.

Pin Group	Pin Count	Description / Primary Function	Alternate Function
Parallel LCD	28	Primary Display: 24 bit parallel RGB data	
LVDS LCD	10	Primary Display: Single channel 18 / 24 bit LVDS data	eDP
LCD Support	3	Panel and backlight enable, PWM	
HDMI	12	Secondary Display: HDMI	DP
CSI0 / PCAM Hi	7	Camera Input: CSI 2 lane / Parallel Camera Input D10:15	
CSI1 / PCAM Lo	10	Camera Input: CSI 4 lane / Parallel Camera Input D0:9	
PCAM Support	6	Parallel Camera support signals	
GBE	12	Gigabit Ethernet	
PCIe	28	3 PCIe x 1 ports with supporting signals	
USB	11	3 ports, one is OTG (client or host); other 2 host only	
SATA	5	1 port (may be boot device)	
SDIO	9	1 port 4 bit	
eMMC	11	1 port 8 bit (may be boot device)	
SPI	10	2 ports (one of the two may be a boot device)	
I2S	13	3 ports plus Audio Master Clock	
SPDIF	2	1 port	
I2C	8	4 ports	
Serial	12	4 ports (two 2 wire and two 4 wire)	
CAN	4	2 ports	
GPIO	12	General Purpose I/O (4 additional GPIO via Strap pins)	
Boot Sel	3	Boot device select pins	
Force Recovery	1	Allow boot media recovery, with Module as USB client	
WDT	1	Watch Dog Timer output	
MISC	12	Power management pins	
RSVD / AFB	20	Reserved / Alternate Function Blocks (AFB)	AFBs
RSVD / EDP_HPD	1	Reserved / Future use for eDP HPD	
RSVD	1	Reserved	
Type Pins	2	Pin straps used to distinguish Camera Usage	
Power	11	10 pins for Module input power ; 1 for RTC	
GND	49	Grounds – circa 15% of total pins	
Pin Total	**314**		

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3 MODULE INTERFACE REQUIRED AND OPTIONAL FEATURES

3.1 Required and Optional Feature Table

Required and optional features for an SMARC Module are summarized in the table below.

" *Shall* "	indicates a mandatory requirement
" ***Should*** "	indicates a recommended but not mandatory requirement
" ***May*** "	indicates a lesser used optional interface
" ***Alternate*** "	indicates an optional interface, implemented on pins shared with another use

Feature	Sub Feature	Requirement	Notes
Parallel LCD	24 bit Parallel RGB interface + Support	***Should***	Default Display (parallel)
LVDS LCD	18 bit single channel	***Should***	Default Display (serial LVDS)
	24 bit single channel – 18 bit compatible	***Should***	
	24 bit single channel – standard color map	***May***	
HDMI	HDMI display interface	***Should***	At least 1 of the 3 display interfaces (Parallel, LVDS or HDMI) ***shall*** be implemented.
	HDMI CEC function	***May***	
DP on HDMI Pins		***May***	
Camera	CSI0 – 2 lane	***Should***	
	CSI1 – 2 lane implementation	***Should***	
	CSI1 – 4 lane implementation	***May***	
	Parallel Camera In – up to 16 bit	***Alternate***	
SDIO	SDIO (4 bit, for SD cards)	***Shall***	***May*** be Carrier boot device
SDMMC	SDMMC (8 bit, eMMC capable)	***May***	***May*** be Carrier boot device
SPI	SPI0	***Shall***	***May*** be Carrier boot device
	SPI1	***Shall***	
I2S	I2S0	***Shall***	
	I2S1	***Should***	
	I2S2	***Should***	
	I2S2 – HDA variant	***May***	
I2C	Power Management	***Shall***	
	General Purpose	***Shall***	
	Camera	***Shall***	
	LCD (Parallel or LVDS) Display I/D	***Shall***	
Serial Ports	SER0 (4 wire)	***Shall***	
	SER1 (2 wire)	***Shall***	
	SER2 (4 wire)	***Should***	
	SER3 (2 wire)	***Should***	

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(Module Interface Required and Optional Features, Continued)

Feature	Sub Feature	Requirement	Note
CAN Bus	CAN0	***May***	
	CAN1	***May***	
USB	USB0 - as USB 2.0 Client	***Shall***	
	USB0 - as USB 2.0 Host / OTG	***May***	
	USB1 - as USB 2.0 Host	***Shall***	
	USB2 – as USB 2.0 Host	***May***	
PCIe	PCIE_A (x1 Gen 1 Root)	***Should***	
	PCIE_B (x1 Gen 1 Root)	***May***	
	PCIE_C (x1 Gen 1 Root)	***May***	
	PCIE_ Target operation	***May***	
	PCIE Gen 2 operation	***May***	
SATA	SATA Gen 1	***Should***	***May*** be Carrier boot device
	SATA Gen 2 operation	***May***	
	SATA Gen 3 operation	***May***	
GBE		***Should***	
SPDIF		***Should***	
Watchdog	WDT Out	***Should***	
GPIO	GPIOs – 12x	***Shall***	
	GPIO interrupt capability – 12x	***Shall***	
	GPIO Camera Support	***Shall*** *(see Note)*	As appropriate for Module Camera implementation
	GPIO5 PWM capability	***Should***	
	GPIO6 Tachin capability	***Should***	
Management	System and power management features	***Shall***	
AFB	AFB functions	***May***	Application specific
Boot Select		***Shall***	
Force Recov		***Should***	
JTAG	JTAG connector on Module	***Should***	Some vendors prefer test point access
RTC		***Should***	***May*** not be needed on some ARM designs. ***Should*** be implemented on X86 designs.

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3.2 Feature Fill Order

Features ***shall*** be filled in a low – to – high order, based on the signal group names. For example, there are three possible USB ports, designated with signal prefixes USB0 to USB2. If a Module design implements only two USB, those would be USB0 and USB1. The PCIe links are designated PCIE_A, PCIE_B and PCIE_C. If only one is implemented, it would be PCIE_A.

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4 SIGNAL DESCRIPTIONS

4.1 Signal Direction and Type Definitions

Direction	Type / Tolerance	Notes
Input		Input to the Module
Output		Output from the Module
Output OD		Open drain output from the Module
Bi-Dir		Bi-directional signal (can be input or output)
Bi-Dir OD		Bi-directional signal; output from the Module is open drain
	VDD_IN	Signal may be exposed to Module input voltage range (3.0 to 5.25V)
	CMOS 1.5V*	CMOS logic input and / or output, 1.5V I/O supply level or tolerance Used for HD Audio. Should be 1.8V signal tolerant.
	CMOS 1.8V	CMOS logic input and / or output, 1.8V I/O supply level or tolerance. Used for majority of SMARC I/O
	CMOS 3.3V	CMOS logic input and / or output, 3.3V I/O supply level or tolerance
	CMOS VDD_JTAG_IO	VDD_JTAG_IO is specific to the Module design. It may be 1.8V, 3.3V, or other value in the 0 to 3.3V range. The JTAG emulator adjusts to the VDD_JTAG_IO level provided by the Module, on the JTAG connector
	GBE MDI	Differential analog signaling for Gigabit Media Dependent Interface
	LVDS AFB	LVDS signaling for AFB – may be PCIe, SATA, USB SS, GBE MDI, MLB or other low voltage high speed differential physical interface
	LVDS DP	LVDS signaling used for DisplayPort devices
	LVDS D-PHY	LVDS signaling used for MIPI CSI camera interfaces
	LVDS LCD	LVDS signaling used for LVDS LCD displays
	LVDS MLB	LVDS signaling used for MOST MLB interface Up to 1.5V CM and 0.5V differential
	LVDS PCIE	LVDS signaling used for PCIE interfaces
	LVDS SATA	LVDS signaling used for SATA interfaces
	TMDS	LVDS signaling used for HDMI display interfaces
	USB	DC coupled differential signaling used for traditional (non- Super-Speed) USB signals
	USB SS	LVDS signaling used for Super Speed USB 3.0
	USB VBUS 5V	5V tolerant input for USB VBUS detection
	10 /100Base-TX	Differential signaling, using MLT-3 (tri level) format for 100 MBit / Sec full duplex Ethernet

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4.2 Display Interfaces

4.2.1 Primary Display – 18 / 24 bit Parallel LCD Data

Signal Name	Direction	Type / Tolerance	Description
LCD_D[16:23]	Output	CMOS 1.8V	8 bit RED color data - 18 bit display implementations leave the two LS bits (D16, D17) not connected
LCD_D[8:15]	Output	CMOS 1.8V	8 bit GRN color data - 18 bit display implementations leave the two LS bits (D8, D9) not connected
LCD_D[0:7]	Output	CMOS 1.8V	8 bit BLU color data - 18 bit display implementations leave the two LS bits (D0, D1) not connected
LCD_PCK	Output	CMOS 1.8V	Pixel clock – display data transitions on the positive clock edge
LCD_DE	Output	CMOS 1.8V	Display Enable – signal is high during the active display line; low otherwise
LCD_HS	Output	CMOS 1.8V	Horizontal Sync – high pulse indicates the start of a new horizontal display line
LCD_VS	Output	CMOS 1.8V	Vertical Synch – high pulse indicates the start of a new display frame

4.2.2 Primary LCD Display Support Signals

The signals in the table below support the Parallel LCD and LVDS LCD interfaces (as these usually are created from the same SOC video source).

Signal Name	Direction	Type / Tolerance	Description
LCD_VDD_EN	Output	CMOS 1.8V	High enables panel VDD
LCD_BKLT_EN	Output	CMOS 1.8V	High enables panel backlight
LCD_BKLT_PWM	Output	CMOS 1.8V	Display backlight PWM control
I2C_LCD_DAT	Bi-Dir OD	CMOS 1.8V	I2C data – to read LCD display EDID EEPROMs
I2C_LCD_CK	Output	CMOS 1.8V	I2C clock – to read LCD display EDID EEPROMs

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4.2.3 Primary Display – 18 / 24 Bit LVDS LCD Single Channel

The Module ***should*** implement an 18 / 24 bit single channel LVDS output stream for the Primary display. This stream is usually created from the parallel RGB data, and usually carries the same display information, but in the serialized LVDS format. Control data (HS, VS, DE) are included in the LVDS stream.

Signal Name	Direction	Type / Tolerance	Description
LVDS[0:3]+ LVDS[0:3]-	Output	LVDS LCD	LVDS LCD data channel differential pairs
LVDS_CK+ LVDS_CK-	Output	LVDS LCD	LVDS LCD differential clock pair

All 18 bit TFT panels use the same LVDS color mapping. Only 3 data pairs (LVDS[0:2] +/-) and the clock pair are needed to drive an 18 bit TFT panel.

Unfortunately, there are two 24 bit LVDS color mappings in the industry:

- Most significant color bits on the 4th LVDS data pair (LVDS[3] +/- here). This is the more common 24 bit mapping. It is not compatible with the 18 bit LVDS color mapping.
- Least significant color bits on the 4th LVDS data pair. This is compatible with the 18 LVDS color mapping.

Modules that implement LVDS ***shall*** implement single channel 18 bit LVDS; ***should*** implement a 24 bit "18 bit compatible" LVDS mapping and ***may*** implement the "MS bit on 4th LVDS pair" mapping.

Details on LVDS color mappings are provided in ***Section 9 Appendix A: LVDS LCD Color*** Mappings***.***

4.2.4 Carrier Board Dual Channel LVDS Support

The current SMARC HW specification does not support dual channel LVDS directly out of the SMARC Module. Version 1.0 of the SMARC specification defined a pin called LCD_DUAL_PCK to support sual channel LVDS implementations on the Carrier. However, with the availability of modern dual channel LVDS transmitters for the Carrier Board such as the Texas Instruments DS90C187 and the Thine THC63LVD827, the Module LCD_DUAL_PCK signal (formerly assigned to Module pin S142) is not necessary and has been deprecated. SMARC Module pin S142 is now defined as a reserved (RSVD) pin.

If the Module supports parallel LCD operation, then it is straightforward to implement dual channel LVDS on the Carrier with either the Texas Instruments DS90C187 or the Thine THC63LVD827. These parts support all flavors of LVDS.

If the Module supports DisplayPort operation (over the Module single channel LVDS pins), then Dual Channel LVDS operation on the Carrier Board may be realized with parts such as the NXP PTN3460.

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4.2.5 eDP / LVDS LCD Pin Sharing

Pins used for LVDS LCD support ***may*** alternatively be used to support an Embedded DisplayPort. The AC coupling required for eDP operation ***shall*** be done off-Module.

LVDS Pin Pairs	LCD Support Pins / Other Pins	eDP Usage	Notes
LVDS0+ LVDS0-		EDP_TX2+ EDP_TX2-	eDP data pair 2
LVDS1+ LVDS1-		EDP_TX1+ EDP_TX1-	eDP data pair 1
LVDS2+ LVDS2-		EDP_TX0+ EDP_TX0-	eDP data pair 0
LVDS3+ LVDS3-		Not used	
LVDS_CK+ LVDS_CK-		EDP_TX3+ EDP_TX3-	eDP data pair 3
	I2C_LCD_CK I2C_LCD_DAT	EDP_AUX+ EDP_AUX-	eDP Auxiliary Channel pair
	LCD_VDD_EN	LCD_VDD_EN	eDP VDD_EN support over EDP_AUX channel is preferable
	LCD_BKLT_EN	LCD_BKLT_EN	eDP BKLT_EN support over EDP_AUX channel is preferable
	LCD_BKLT_PWM	LCD_BKLT_PWM	eDP BKLT_PWM support over EDP_AUX channel is preferable
	RSVD / EDP_HPD	EDP_HPD	eDP Hot Plug Detect pin

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4.2.6 Secondary (HDMI) Display

Signal Name	Direction	Type / Tolerance	Description
HDMI_D[0:2]+ HDMI_D[0:2]-	Output	TMDS	TMDS / HDMI data differential pairs
HDMI_CK+ HDMI_CK-	Output	TMDS	HDMI differential clock output pair
HDMI_HPD	Input	CMOS 1.8V	HDMI Hot Plug Detect input
HDMI_CTRL_DAT	Bi-Dir OD	CMOS 1.8V	I2C data line dedicated to HDMI
HDMI_CTRL_CK	Output OD	CMOS 1.8V	I2C clock line dedicated to HDMI
HDMI_CEC	Bi-Dir	CMOS 1.8V	HDMI Consumer Electronics Control 1 – wire peripheral control interface

HDMI displays uses 5V I2C signaling. The Module HDMI_CTRL_DAT and HDMI_CTRL_CK signals need to be level translated on the Carrier from the Module 1.8V level. A similar consideration applies to the HDMI_HPD signal. There are a number of single chip devices on the market that perform ESD protection and control signal level shifting for HDMI interfaces. The Texas Instruments TPD12S016 is one such device.

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4.2.7 DP Operation Over HDMI

The SMARC HDMI pins may alternatively be used for DisplayPort (DP) operation. This is Module vendor dependent.

DP Use	Direction	DP Description	Coupling / Tolerance	SMARC Signal Name
DP[0]+ DP[0]-	Output	DP Data Pair 0	AC Coupled ***off*** module	HDMI_D[2]+ HDMI_D[2]-
DP[1]+ DP[1]-	Output	DP Data Pair 1	AC Coupled ***off*** module	HDMI_D[1]+ HDMI_D[1]-
DP[2]+ DP[2]-	Output	DP Data Pair 2	AC Coupled ***off*** module	HDMI_D[0]+ HDMI_D[0]-
DP[3]+ DP[3]-	Output	DP Data Pair 3	AC Coupled ***off*** module	HDMI_CK+ HDMI_CK-
DP_HPD	Input	DP Hot Plug Detect input	DC coupled CMOS 1.8V	HDMI_HPD
DP_AUX-	Bi-Dir	DP AUX Channel (- part of pair)	AC Coupled ***on*** module	HDMI_CTRL_DAT
DP_AUX+	Bi-Dir	DP AUX Channel (+ part of pair)	AC Coupled ***on*** module	HDMI_CTRL_CK
AUX_SEL	Input	Pulled to GND on Carrier for DP operation in Dual Mode implementations. Driven to 1.8V on Carrier for HDMI operation. Terminated on Module through 1M resistor to GND.	DC coupled CMOS 1.8V	HDMI_CEC

Dual Mode (HDMI and DisplayPort on the same pins) implementations ***may*** be realized. This is desirable for SOCs that natively implement this capability. With such SOCs, the primary Dual Mode implementation challenge is that the HDMI_CTRL_DAT and HDMI_CTRL_CK lines are DC coupled, but the DP_AUX+ /- pair must be AC coupled. A set of FET switches is usually used to sort this out. The FET gates can be controlled by the AUX_SEL pin function. The HDMI_CEC function is not available in a SMARC Dual Mode HDMI / DisplayPort implementation.

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4.3 Camera Interfaces

A group of pins is defined on the Module to support serial and parallel camera interfaces. The same pins are used for serial and parallel camera data interfaces, and a given design will generally be used with either serial camera(s) or parallel camera(s). There are additionally a number of separate pins defined to support the serial and parallel interfaces.

4.3.1 Camera Configurations

Configuration	CSI0 / PCAM D15:10	CSI1 / PCAM D9:0
Serial	CSI0 - 2 lanes	CSI1 – 2 or 4 lanes
Parallel	Up to 16 bits of Parallel Video In ***May*** be 8, 10, 12 or 16 bit wide input, using PCAM_PXL_CK0 as the Parallel Camera Pixel Clock ***May*** be split into two 8 bit streams, using PCAM_PXL_CK0 for PCAM_D[0:7] and using PCAM_PXL_CK1 for PCAM_D[8:15]. For dual 8 bit streams, a video format with embedded synch signals, such as BT.656, must be used.	
Mixed	CSI0 – 2 lanes	Parallel Video In, over CSI1 pin group Up to 10 bits

4.3.2 Module Camera Type Pins

A pair of pins are defined on the Module to indicate to the Carrier what Camera interface(s) are supported by the Module. Carrier boards that implement parallel camera(s) logic ***shall*** decode these Camera Type pins. Such Carriers ***shall not*** power up a Carrier Camera interface that is incompatible with the Module implementation.

Signal Name	Description
PCAM_ON_CSI0#	***Shall*** be tied to GND on the Module if the Module supports a parallel camera interface on the SMARC CSI0 pin group. ***Shall*** be an open pin on the Module if the Module supports a serial camera interface over the CSI0 pin group. Modules that do not use the CSI0 pin group ***may*** leave the PCAM_CSI0 pin open.
PCAM_ON_CSI1#	***Shall*** be tied to GND on the Module if the Module supports a parallel camera interface on the SMARC CSI1 pin group. ***Shall*** be an open pin on the Module if the Module supports a serial camera interface over the CSI1 pin group. Modules that do not use the CSI1 pin group ***may*** leave the PCAM_CSI1 pin open.

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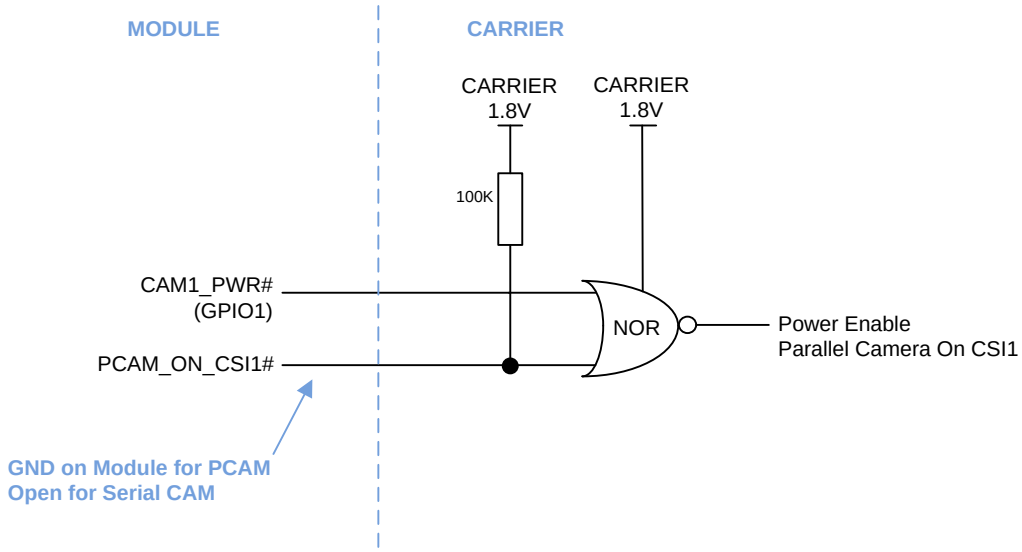
4.3.3 Camera Power Enables and Resets

CAM0 refers to the CSI0 pin group, pin shared with the high order PCAM bits, PCAM_D[10:15].

CAM1 refers to the CSI1 pin group, pin shared with the low order PCAM bits, PCAM_D[0:9].

Signal Name	Direction	Type / Tolerance	GPIO Use	Sanctioned Alternate Uses
GPIO0 / CAM0_PWR#	Bi-Dir	CMOS 1.8V	GPIO0	Camera 0 Power Enable, active low output.
GPIO1 / CAM1_PWR#	Bi-Dir	CMOS 1.8V	GPIO1	Camera 1 Power Enable, active low output
GPIO2 / CAM0_RST#	Bi-Dir	CMOS 1.8V	GPIO2	Camera 0 Reset, active low output
GPIO3 / CAM1_RST#	Bi-Dir	CMOS 1.8V	GPIO3	Camera 1 Reset, active low output

Figure 1 Parallel Camera Power Enable



Carrier boards that implement parallel camera circuit(s) ***shall*** ensure that the parallel camera power is not enabled when there is a Module capability mismatch (e.g. the Module implements a serial camera on the CSI1 pins but the Carrier has a parallel implementation on CSI1, or the Module implements a serial camera on the CSI0 pins but the Carrier implements a wide parallel camera on the CSI0 and CSI1 pins).

The reason for this is that the parallel camera interfaces run at 1.8V or more. The CSI interfaces are low voltage differential pairs. The voltage tolerance of many SOC CSI interfaces extends to about 1.8V. To ensure that there is no mis-matched Module damage potential, Carrier boards ***shall*** implement a parallel camera power enable scheme as per or equivalent to the one shown in the figure above.

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4.3.4 Camera I2C Support

The I2C_CAM_ port is intended to support serial and parallel cameras. Most contemporary cameras with I2C support allow a choice of two I2C address ranges.

Signal Name	Direction	Type / Tolerance	Description
I2C_CAM_DAT	Bi-Dir OD	CMOS 1.8V	Serial / Parallel camera support link - I2C data
I2C_CAM_CK	Bi-Dir OD	CMOS 1.8V	Serial / Parallel camera support link - I2C clock

4.3.5 Serial Camera In - CSI0

Signal Name	Direction	Type / Tolerance	Description
CSI0_D[0:1]+ CSI0_D[0:1]-	Input	LVDS D-PHY	CSI0 differential data inputs Pin shared with parallel PCAM D12 – D15
CSI0_CK+ CSI0_CK-	Input	LVDS D-PHY	CSI0 differential clock inputs Pin shared with parallel PCAM D10 – D11
CAM_MCK	Output	CMOS 1.8V	Master clock output for CSI camera support (***may*** be used for CSI0 and / or CSI1)

4.3.6 Serial Camera In – CSI1

Signal Name	Direction	Type / Tolerance	Description
CSI1_D[0:3]+ CSI1_D[0:3]-	Input	LVDS D-PHY	CSI1 differential data inputs Pin shared with parallel PCAM D2 – D9
CSI1_CK+ CSI1_CK-	Input	LVDS D-PHY	CSI0 differential clock inputs Pin shared with parallel PCAM D0 – D1

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4.3.7 Parallel Camera Input – Low Order 10 Bits

Signal Name	Direction	Type / Tolerance	Description
PCAM_D[0:9]	Input	CMOS 1.8V	Parallel camera input data, bits 0 -9 Pin shared with CSI1 serial camera interface
PCAM_PXL_CK0	Input	CMOS 1.8V	Parallel camera primary pixel clock input
PCAM_VSYNC	Input	CMOS 1.8V	Parallel camera Vertical Sync input
PCAM_HSYNC	Input	CMOS 1.8V	Parallel camera Horizontal Sync input
PCAM_DE	Input	CMOS 1.8V	Parallel camera Data Enable input
PCAM_MCK	Output	CMOS 1.8V	Parallel camera Master Clock output
GPIO7 / PCAM_FLD	Input	CMOS 1.8V	Parallel camera Field input

4.3.8 Parallel Camera Input – High Order 6 Bits

Signal Name	Direction	Type / Tolerance	Description
PCAM_D[10:15]	Input	CMOS 1.8V	Parallel camera input data, bits 10-15 Pin shared with CSI0 interface

4.3.9 Parallel Camera Input – 2nd Pixel Clock

Some SOCs allow their 16 bit video input port to be broken up into to independent 8 bit ports. To allow this SOC feature to be used, a 2nd PCAM pixel clock ***may*** be provided. An 8 bit video input format with embedded synch signals, such as ITU-BT.656, must be used in this case, along with the two available pixel clocks.

Signal Name	Direction	Type / Tolerance	Description
PCAM_PXL_CK1	Input	CMOS 1.8V	Parallel camera secondary pixel clock input – 2nd video parallel port (8 bit format with embedded synchs only)

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4.4 SDIO / SDMMC Interfaces

4.4.1 SDIO Card (4 bit) Interface

The Carrier SDIO Card ***may*** be selected as the Boot Device – see ***Section 4.19 Boot Select.***

Signal Name	Direction	Type / Tolerance	Description
SDIO_D[0:3]	Bi-Dir	CMOS 3.3V	4 bit data path
SDIO_CMD	Bi-Dir	CMOS 3.3V	Command line
SDIO_CK	Output	CMOS 3.3V	Clock
SDIO_WP	Input	CMOS 3.3V	Write Protect
SDIO_CD#	Input	CMOS 3.3V	Card Detect
SDIO_PWR_EN	Output	CMOS 3.3V	SD card power enable

Note: SD Cards are not typically available with a 1.8V I/O voltage. The Module SD Card I/O level is specified as 3.3V and not 1.8V.

4.4.2 eMMC (8 bit) Interface

The Module pin definition allows for an 8 bit eMMC interface. However, with most SOCs, there will only be a single eMMC interface available from the SOC. If the SOC eMMC path is used for an on-Module boot device, then the interface ***may not*** be available to the Carrier.

If the SOC eMMC interface is not used on-Module, it ***may*** be available off-Module. In that case, Carrier eMMC Interface ***may*** be selected as the Boot Device – see ***Section 4.19 Boot Select.***

Signal Name	Direction	Type / Tolerance	Description
SDMMC_D[0:7]	Bi-Dir	CMOS 1.8V	8 bit data path (***may*** be used for 4 and 1 bit wide eMMC devices as well)
SDMMC_CMD	Bi-Dir	CMOS 1.8V	Command line
SDMMC_CK	Output	CMOS 1.8V	Clock
SDMMC_RST#	Output	CMOS 1.8V	Reset signal to eMMC device

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4.5 SPI Interfaces

4.5.1 SPI0

The Carrier SPI0 device ***may*** be selected as the Boot Device – see ***Section 4.19 Boot Select.***

Signal Name	Direction	Type / Tolerance	Description
SPI0_CS0#	Output	CMOS 1.8V	SPI0 Master Chip Select 0 output Use to select Carrier SPI boot device
SPI0_CS1#	Output	CMOS 1.8V	SPI0 Master Chip Select 1 output
SPI0_CK	Output	CMOS 1.8V	SPI0 Master Clock output
SPI0_DIN	Input	CMOS 1.8V	SPI0 Master Data input (input to CPU, output from SPI device)
SPI0_DO	Output	CMOS 1.8V	SPI0 Master Data output (output from CPU, input to SPI device)

4.5.2 SPI1

Signal Name	Direction	Type / Tolerance	Description
SPI1_CS0#	Output	CMOS 1.8V	SPI1 Master Chip Select 0 output
SPI1_CS1#	Output	CMOS 1.8V	SPI1 Master Chip Select 1 output
SPI1_CK	Output	CMOS 1.8V	SPI1 Master Clock output
SPI1_DIN	Input	CMOS 1.8V	SPI1 Master Data input (input to CPU, output from SPI device)
SPI1_DO	Output	CMOS 1.8V	SPI1 Master Data output (output from CPU, input to SPI device)

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4.6 I2S Interfaces

Three I2S interfaces are defined. These are typically used for digital audio I/O and other modest bandwidth functions. A common audio master clock signal is also defined.

Signal Name	Direction	Type / Tolerance	Description
I2S[0:2]_LRCK	Bi-Dir	CMOS 1.8V	Left& Right audio synchronization clock
I2S[0:2]_SDOUT	Output	CMOS 1.8V	Digital audio Output
I2S[0:2]_SDIN	Input	CMOS 1.8V	Digital audio Input
I2S[0:2]_CK	Bi-Dir	CMOS 1.8V	Digital audio clock
AUDIO_MCK	Output	CMOS 1.8V	Master clock output to Audio codecs

4.7 HDA Interface

One of the three I2S channels, I2S2, ***may*** alternatively be used to implement a HDA (High Definition Audio) channel:

Signal Name	Direction	Type / Tolerance	Description
HDA_SYNC (I2S2_LRCK)	Bi-Dir	CMOS 1.5V*	Left& Right audio synchronization clock / HDA sync
HDA_SDO (I2S2_SDOUT)	Output	CMOS 1.5V*	I2S Digital audio Output / High Definition Audio data out
HDA_SDI (I2S2_SDIN)	Input	CMOS 1.5V*	I2S Digital audio Input / High Definition Audio data in
HDA_CK (I2S2_CK)	Bi-Dir	CMOS 1.5V*	I2S Digital audio clock/ High Definition Audio clock
GPIO4 / HDA_RST#	Output	CMOS 1.8V	HDA reset output (by means of GPIO4)

Note: per the HD Audio specification, HD Audio may be run at either 1.5V or 3.3V. SMARC requires 1.5V HD Audio signaling. The SMARC HD Audio pins are shared with the I2S2 pins, which are defied to be 1.8V. This specification ignores the discrepancy between the 1.5V and 1.8V signaling, as the chance of damage in mis-matched systems is negligible.

ARM SOCs generally run I2S audio and will likely use 1.8V signaling. X86 SOCs generally run 1.5V signal levels on the HD Audio interface.

Not all HD Audio CODECs accept 1.5V signaling. One that does is the Cirrus CS4207. IDT also offers 1.5V HD Audio CODECs.

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4.8 SPDIF

Signal Name	Direction	Type / Tolerance	Description
SPDIF_OUT	Output	CMOS 1.8V	Digital Audio Output
SPDIF_IN	Input	CMOS 1.8V	Digital Audio Input

4.9 I2C Interfaces

The Module supports five I2C interfaces, per the following table. Except for the LCD and HDMI Module I2C interfaces, the I2C ports ***should*** be multi-master capable. Data rates of 100 kHz and 400 kHz ***should*** be supported.

I2C Port	Primary Purpose	Alternate Use	I/O Voltage Level
I2C_PM	Power Management support	System configuration management	CMOS 1.8V
I2C_CAM	Camera support	General Purpose	CMOS 1.8V
I2C_GP	General purpose use		CMOS 1.8V
I2C_LCD	LCD display support (for parallel and LVDS LCD)	General Purpose	CMOS 1.8V
HDMI_CTRL	HDMI control		CMOS 1.8V

All I2C interfaces but the I2C_GP interface are described in the section served by that I2C link (LCD, HDMI, Camera Interface, etc). The I2C_GP Module interface consists of the following two pins:

Signal Name	Direction	Type / Tolerance	Description
I2C_GP_CK	Bi-Dir OD	CMOS 1.8V	I2C General Purpose clock signal
I2C_GP_DAT	Bi-Dir OD	CMOS 1.8V	I2C General Purpose data signal

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4.10 Asynchronous Serial Ports

Module pins for up to four asynchronous serial ports are defined. The ports are designated SER0 – SER3. Ports SER0 and SER2 are 4 wire ports (2 data lines and 2 handshake lines). Ports SER1 and SER3 are 2 wire ports (data only).

Signal Name	Direction	Type / Tolerance	Description
SER[0:3]_TX	Output	CMOS 1.8V	Asynchronous serial port data out
SER[0:3]_RX	Input	CMOS 1.8V	Asynchronous serial port data in
SER[0]_RTS#	Output	CMOS 1.8V	Request to Send handshake line for SER0
SER[0]_CTS#	Input	CMOS 1.8V	Clear to Send handshake line for SER0
SER[2]_RTS#	Output	CMOS 1.8V	Request to Send handshake line for SER2
SER[2]_CTS#	Input	CMOS 1.8V	Clear to Send handshake line for SER2

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4.11 CAN Bus

4.11.1 CAN0 Data

Signal Name	Direction	Type / Tolerance	Description
CAN0_TX	Output	CMOS 1.8V	CAN0 Transmit output
CAN0_RX	Input	CMOS 1.8V	CAN0 Receive input

4.11.2 CAN1 Data

Signal Name	Direction	Type / Tolerance	Description
CAN1_TX	Output	CMOS 1.8V	CAN1 Transmit output
CAN1_RX	Input	CMOS 1.8V	CAN1 Receive input

4.11.3 CAN Bus Error Signals

If the Module supports CAN0 operation, then CAN0 bus error condition signaling ***should*** be supported on the Module GPIO8 pin. This is an active low input to the Module from the CAN bus transceiver.

If the Module supports CAN1 operation, then CAN1 bus error condition signaling ***should*** be supported on the Module GPIO9 pin. This is an active low input to the Module from the CAN bus transceiver.

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4.12 USB Interfaces

4.12.1 USB0

The USB0 port ***shall*** be available as a USB 2.0 client. It ***may*** also be available as an OTG port (and, by extension, as a host), or as a host (some SOCs allow a USB port to be configured as client or host, but do not support full OTG functionality).

Signal Name	Direction	Type / Tolerance	Description
USB0+ USB0-	Bi-Dir	USB	Differential USB0 data pair.
USB0_EN_OC#	Bi-Dir OD	CMOS 3.3V	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up ***shall*** be present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.12.4 ***USBx_EN_OC# Discussion*** below.
USB0_VBUS_DET	Input	USB VBUS 5V	USB host power detection, when this port is used as a device.
USB0_OTG_ID	Input	CMOS 3.3V	USB OTG ID input, active high.

4.12.2 USB1

The USB1 port ***shall*** be available as a USB 2.0 host.

Signal Name	Direction	Type / Tolerance	Description
USB1+ USB1-	Bi-Dir	USB	Differential USB1 data pair.
USB1_EN_OC#	Bi-Dir OD	CMOS 3.3V	Pulled low by Module OD driver to disable USB1 power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up ***shall*** be present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.12.4 ***USBx_EN_OC# Discussion*** below.

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4.12.3 USB2

The USB2 port ***may*** be implemented. If implemented, USB2 ***shall*** be a host port.

Signal Name	Direction	Type / Tolerance	Description
USB2+ USB2-	Bi-Dir	USB	Differential USB2 data pair.
USB2_EN_OC#	Bi-Dir OD	CMOS 3.3V	Pulled low by Module OD driver to disable USB2 power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up ***shall*** be present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.12.4 ***USBx_EN_OC# Discussion*** below.

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4.12.4 USBx_EN_OC# Discussion

The Module USBx_EN_OC# pins (where 'x' is 0,1 or 2 for use with USB0, USB1 or USB2) are multi-function Module pins, with a pull-up to a 3.3V rail on the Module, an OD driver on the Module, and, if the OC# (over-current) monitoring function is implemented on the Carrier, an OD driver on the Carrier. The use is as follows:

1) On the Carrier board, for external plug-in USB peripherals (USB memory sticks, cameras, keyboards, mice, etc.) USB power distribution is typically handled by USB power switches such as the Texas Instruments TPS2052B or the Micrel MIC2026-1 or similar devices. The Carrier implementation is more straightforward if the Carrier USB power switches have active–high power enables and active low open drain OC# outputs (as the TI and Micrel devices referenced do). The USB power switch Enable and OC# pins for a given USB channel are tied together on the Carrier. The USB power switch enable pin must function with a low input current. The TI and Micrel devices referenced above require 1 microampere or less, at a 3.3V enable voltage level.

2) The Module drives USBx_EN_OC# low to disable the power delivery to the USBx device.

3) The Module floats USBx_EN_OC# to enable power delivery. The line is pulled to 3.3V by the Module pull-up, enabling the Carrier board USB power switch.

4) If there is a USB over-current condition, the Carrier board USB power switch drives the USBx_EN_OC# line low. This removes the over-current condition (by disabling the USB switch enable input), and allows Module software to detect the over-current condition.

5) The Module software ***should*** look for a falling edge interrupt on USBx_EN_OC#, while the port is enabled, to detect the OC# condition. The OC# condition will not last long, as the USB power switch is disabled when the switch IC detects the OC# condition.

6) If the USB power to the port is disabled (USBx_EN_OC# is driven low by the Module) then the Module software must be aware that the port is disabled, and the low input value on the port does not indicate an over-current condition (because the port power is disabled).

7) If the USB power to the port is disabled, then the Module ***may*** remove the 3.3V pull-up voltage to the USBx_EN_OC# node, to save the current drain through the pull-up resistor. This is optional and Module design dependent.

Carrier Board USB peripherals that are not removable often do ***not*** make use of USB power switches with current limiting and over-current detection. It is usually deemed un-necessary for non-removable devices. In these cases, the USBx_EN_OC# pins may be left unused, or they may be used as USBx power enables, without making use of the over-current detect Module input feature.

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4.13 PCI Express

The Module ***may*** implement up to three PCIe x1 links, designated PCIe Links A, B, C. The links ***may*** be PCIe Gen 1, 2 or 3, as the Module chip or chipset allows.

The Module PCIe links are primarily PCIe Root Complexes. If the chipset allows it, the PCIe link(s) ***may*** alternatively be configured as a PCIe target(s). This is Module vendor specific.

4.13.1 PCIe_Link A

Modules ***should*** implement the PCIe Link A port.

Signal Name	Direction	Type / Tolerance	Description
PCIE_A_TX+ PCIE_A_TX-	Output	LVDS PCIe	Differential PCIe Link A transmit data pair 0 Series coupling caps ***shall*** be on the Module Caps ***should*** be 0402 package 0.1uF
PCIE_A_RX+ PCIE_A_RX-	Input	LVDS PCIe	Differential PCIe Link A receive data pair 0 No coupling caps on Module
PCIE_A_REFCK+ PCIE_A_REFCK-	Output	LVDS PCIe	Differential PCIe Link A reference clock output DC coupled
PCIE_A_CKREQ#	Input	CMOS 3.3V	PCIe Port A clock request input Pulled up or terminated on Module
PCIE_A_RST#	Output	CMOS 3.3V	PCIe Port A reset output
PCIE_A_PRSNT#	Input	CMOS 3.3V	PCIe Port A present input Pulled up or terminated on Module

4.13.2 PCIe_Link B

Modules ***may*** implement the PCIe Link B port (if the Link A port is also implemented).

Signal Name	Direction	Type / Tolerance	Description
PCIE_B_TX+ PCIE_B_TX-	Output	LVDS PCIe	Differential PCIe Link B transmit data pair 0 Series coupling caps ***shall*** be on the Module Caps ***should*** be 0402 package 0.1uF
PCIE_B_RX+ PCIE_B_RX-	Input	LVDS PCIe	Differential PCIe Link B receive data pair 0 No coupling caps on Module
PCIE_B_REFCK+ PCIE_B_REFCK-	Output	LVDS PCIe	Differential PCIe Link B reference clock output DC coupled
PCIE_B_CKREQ#	Input	CMOS 3.3V	PCIe Port B clock request input Pulled up or terminated on Module
PCIE_B_RST#	Output	CMOS 3.3V	PCIe Port B reset output, active low
PCIE_B_PRSNT#	Input	CMOS 3.3V	PCIe Port B present input Pulled up or terminated on Module

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4.13.3 PCIe_Link C

Modules ***may*** implement the PCIe Link C port (if the Link B port is also implemented).

Signal Name	Direction	Type / Tolerance	Description
PCIE_C_TX+ PCIE_C_TX-	Output	LVDS PCIe	Differential PCIe Link C transmit data pair 0 Series coupling caps ***shall*** be on the Module Caps ***should*** be 0402 package 0.1uF
PCIE_C_RX+ PCIE_C_RX-	Input	LVDS PCIe	Differential PCIe Link C receive data pair 0 No coupling caps on Module
PCIE_C_REFCK+ PCIE_C_REFCK-	Output	LVDS PCIe	Differential PCIe Link C reference clock output DC coupled
PCIE_C_CKREQ#	Input	CMOS 3.3V	PCIe Port C clock request input Pulled up or terminated on Module
PCIE_C_RST#	Output	CMOS 3.3V	PCIe Port C reset output
PCIE_C_PRSNT#	Input	CMOS 3.3V	PCIe Port C present input Pulled up or terminated on Module

4.13.4 PCIe Wake

Signal Name	Direction	Type / Tolerance	Description
PCIE_WAKE#	Input	CMOS 3.3V	PCIe wake up interrupt to host – common to PCIe links A, B, C – pulled up or terminated on Module

4.14 SATA

The Module definition allows for one SATA port. The port ***may*** be SATA Gen 1, 2 or 3 as the Module chip or chipset allows.

The Carrier SATA device ***may*** be selected as the Boot Device – see ***Section 4.19***

.

Signal Name	Direction	Type / Tolerance	Description
SATA_TX+ SATA_TX-	Output	SATA	Differential SATA 0 transmit data Pair 0402 series coupling caps ***shall*** be on Module
SATA_RX+ SATA_RX-	Input	SATA	Differential SATA 0 transmit data 0402 series coupling caps ***shall*** be on Module
SATA_ACT#	Output OD	CMOS 3.3V Tolerance	Active low SATA activity indicator If implemented, ***shall*** be able to sink 24mA or more Carrier LED current

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4.15 GBE

Signal Name	Direction	Type / Tolerance	Description
GBE_MDI0+ GBE_MDI0-	Bi-Dir	GBE MDI	Bi-directional transmit/receive pair 0 to magnetics (Media Dependent Interface)
GBE_MDI1+ GBE_MDI1-	Bi-Dir	GBE MDI	Bi-directional transmit/receive pair 1 to magnetics (Media Dependent Interface)
GBE_MDI2+ GBE_MDI2-	Bi-Dir	GBE MDI	Bi-directional transmit/receive pair 2 to magnetics (Media Dependent Interface)
GBE_MDI3+ GBE_MDI3-	Bi-Dir	GBE MDI	Bi-directional transmit/receive pair 3 to magnetics (Media Dependent Interface)
GBE_LINK100#	Output OD	CMOS 3.3V Tolerance	Link Speed Indication LED for 100Mbps ***Shall*** be able to sink 24mA or more Carrier LED current
GBE_LINK1000#	Output OD	CMOS 3.3V Tolerance	Link Speed Indication LED for 1000Mbps ***Shall*** be able to sink 24mA or more Carrier LED current
GBE_LINK_ACT#	Output OD	CMOS 3.3V Tolerance	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity ***Shall*** be able to sink 24mA or more Carrier LED current
GBE_CTREF	Output	Reference Voltage	Center-Tap reference voltage for GBE0 Carrier board Ethernet magnetic (if required by the Module GBE PHY)

4.16 Watchdog

Signal Name	Direction	Type / Tolerance	Description
WDT_TIME_OUT#	Output	CMOS 1.8V	Watch-Dog-Timer Output

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4.17 GPIO

Twelve Module pins are allocated for GPIO (general purpose input / output) use. All pins ***should*** be capable of bi-directional operation. A preferred direction of operation is assigned, with half of them (GPIO0 – GPIO5) recommended for use as outputs and the remainder (GPIO6 – GPIO11) as inputs.

At Module power-up, the state of the GPIO pins ***may not*** be defined, and ***may*** briefly be configured in the "wrong" state, before boot loader code corrects them. Carrier designers ***should*** be aware of this and plan accordingly. Module designers ***should*** generally choose pins that are tri-stated or are inputs during power up and reset, but this ***may not*** always be the case.

All GPIO pins ***should*** be weakly pulled up to 1.8V. If the pull-ups are implemented as discrete resistors, or resistor packs, a value of 470K ***should*** be used. SOC internal pull-up / current source features ***may*** be used instead of external resistors.

All GPIO pins ***shall*** be capable of generating interrupts. The interrupt characteristics (edge or level sensitivity, polarity) are generally configurable in the SOC register set.

Signal Name	Direction	Preferred Direction	Type / Tolerance	GPIO Use	Sanctioned Alternate Uses
GPIO0 / CAM0_PWR#	Bi-Dir	Output	CMOS 1.8V	GPIO0	Camera 0 Power Enable, active low output
GPIO1 / CAM1_PWR#	Bi-Dir	Output	CMOS 1.8V	GPIO1	Camera 1 Power Enable, active low output
GPIO2 / CAM0_RST#	Bi-Dir	Output	CMOS 1.8V	GPIO2	Camera 0 Reset, active low output
GPIO3 / CAM1_RST#	Bi-Dir	Output	CMOS 1.8V	GPIO3	Camera 1 Reset, active low output
GPIO4 / HDA_RST#	Bi-Dir	Output	CMOS 1.8V	GPIO4	HD Audio Reset, active low output
GPIO5 / PWM_OUT	Bi-Dir	Output	CMOS 1.8V	GPIO5	PWM output
GPIO6 / TACHIN	Bi-Dir	Input	CMOS 1.8V	GPIO6	Tachometer input (used with the GPIO5 PWM)
GPIO7 / PCAM_FLD	Bi-Dir	Input	CMOS 1.8V	GPIO7	PCAM_FLD (Field) signal input
GPIO8 / CAN0_ERR#	Bi-Dir	Input	CMOS 1.8V	GPIO8	CAN0 Error signal, active low input
GPIO9 / CAN1_ERR#	Bi-Dir	Input	CMOS 1.8V	GPIO9	CAN1 Error signal, active low input
GPIO10	Bi-Dir	Input	CMOS 1.8V	GPIO10	
GPIO11	Bi-Dir	Input	CMOS 1.8V	GPIO11	

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4.18 Management Pins

The input pins listed in this table are all active low and are meant to be driven by OD (open drain) devices on the Carrier. The Carrier either floats the line or drives it to GND. No Carrier pull-ups are needed. The pull-up functions are performed on the Module. The voltage rail that these lines are pulled to on the Module varies, depending on the design, and may be anywhere from 1.8V to 5.25V.

Switches to GND ***may*** be used instead of OD drivers for lines such as PWR_BTN# and RESET_IN#.

Signal Name	Direction	Type / Tolerance	Description
VIN_PWR_BAD#	Input	CMOS VDD_IN	Power bad indication from Carrier board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) ***shall not*** be enabled while this signal is held low by the Carrier. Pulled up on Module. Driven by OD part on Carrier.
CARRIER_PWR_ON	Output	CMOS 1.8V	Carrier board circuits (apart from power management and power path circuits) ***should not*** be powered up until the Module asserts the CARRIER_PWR_ON signal.
CARRIER_STBY#	Output	CMOS 1.8V	The Module ***shall*** drive this signal low when the system is in a standby power state
RESET_OUT#	Output	CMOS 1.8V	General purpose reset output to Carrier board.
RESET_IN#	Input	CMOS 1.8V	Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise. Pulled up on Module. Driven by OD part on Carrier.
POWER_BTN#	Input	CMOS 1.8V	Power-button input from Carrier board. Carrier to float the line in in-active state. Active low, level sensitive. ***Should*** be de-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.
SLEEP#	Input	CMOS 1.8V	Sleep indicator from Carrier board. ***May*** be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. ***Should*** be de-bounced on the Module. Pulled up on Module. Driven by OD part on Carrier.
LID#	Input	CMOS 1.8V	Lid open/close indication to Module. Low indicates lid closure (which system ***may*** use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. ***Should*** be de-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.

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Signal Name	Direction	Type / Tolerance	Description
BATLOW#	Input	CMOS 1.8V	Battery low indication to Module. Carrier to float the line in in-active state. Pulled up on Module. Driven by OD part on Carrier.
I2C_PM_DAT	Bi-Dir OD	CMOS 1.8V	Power management I2C bus data.
I2C_PM_CK	Bi-Dir OD	CMOS 1.8V	Power management I2C bus clock.
CHARGING#	Input	CMOS 1.8V	Held low by Carrier during battery charging. Carrier to float the line when charge is complete. Pulled up on Module. Driven by OD part on Carrier.
CHARGER_PRSNT#	Input	CMOS 1.8V	Held low by Carrier if DC input for battery charger is present. Pulled up on Module. Driven by OD part on Carrier.
TEST#	Input	CMOS 1.8V	Held low by Carrier to invoke Module vendor specific test function(s). Pulled up on Module. Driven by OD part on Carrier.

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4.19 Boot Select

Three Module pins allow the Carrier board user to select from eight possible boot devices. Three are Module devices, and four are Carrier devices, and one is a remote device. The pins ***shall*** be weakly pulled up on the Module and the pin states decoded by Module logic. The Carrier ***shall*** either leave the Module pin Not Connected ("Float" in the table below) or ***shall*** pull the pin to GND, per the second table below.

A "Force Recovery" provision exists, per the pin description below.

Signal Name	Direction	Type / Tolerance	Description
BOOT_SEL[0:2]#	Input	CMOS 1.8V	Input straps determine the Module boot device. Pulled up on Module. Driven by OD part on Carrier.
FORCE_RECOV#	Input	CMOS 1.8V	Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked. Pulled high on the Module. For SOCs that do not implement a USB based Force Recovery functions, then a low on the Module FORCE_RECOV# pin ***may*** invoke the SOC native Force Recovery mode – such as over a Serial Port. Pulled up on Module. Driven by OD part on Carrier.

	Carrier Connection			Boot Source
	BOOT_SEL2#	BOOT_SEL1#	BOOT_SEL0#	
0	GND	GND	GND	Carrier SATA
1	GND	GND	Float	Carrier SD Card
2	GND	Float	GND	Carrier eMMC Flash
3	GND	Float	Float	Carrier SPI
4	Float	GND	GND	Module device (NAND, NOR) – vendor specific
5	Float	GND	Float	Remote boot (GBE, serial) – vendor specific
6	Float	Float	GND	Module eMMC Flash
7	Float	Float	Float	Module SPI

Note: the boot sources shown above are Module options, and ***may not*** be available on all Module designs.

The definition of "boot" is left to the Module designer. Some designs may literally implement some or all of the table above, such that the first off-SOC code fetches come from the devices listed above. Alternatively, some designs may always fetch the first few off-SOC instructions from a fixed device, likely a SPI Flash EEPROM, and then re-direct the execution to another device per the table above.

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4.20 Alternate Function Block

The Alternate Function Block is a set of 20 signal pins that are set aside for application and vendor specific use. The AFB pins ***may*** be defined in a future version of this specification for certain standard uses. For this version of the SMARC specification, the AFB pins are reserved pins.

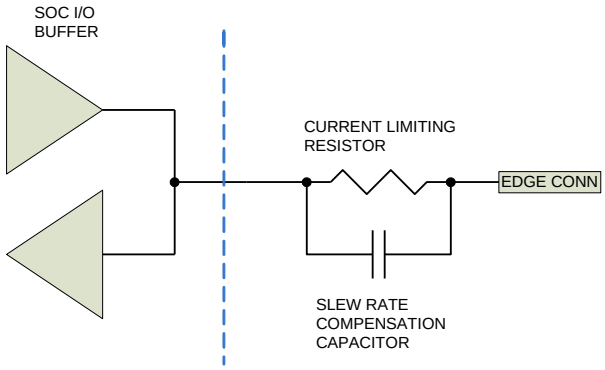
For application specific and vendor specific uses, the AFB pins are segregated into four categories, evident in the table below. The groupings serve to impose some order on the ways the pins are used by applications, lessening the chance of damage if Modules and Carriers are mis-matched. Nonetheless, users must be aware of what the respective Module and Carrier AFB functions are, and take care that they match up suitably.

Some application specific use models for the AFB are outlined in ***Section 10 Appendix B: Alternate Function Block Use Models.***

Signal Name	Direction	Type / Tolerance	Description
AFB0_OUT	Output	CMOS 1.8V	General purpose AFB output
AFB1_OUT	Output	CMOS 1.8V	General purpose AFB output
AFB2_OUT	Output	CMOS 1.8V	General purpose AFB output
AFB3_IN	Input	CMOS 1.8V	General purpose AFB input
AFB4_IN	Input	CMOS 1.8V	General purpose AFB input
AFB5_IN	Input	CMOS 1.8V	General purpose AFB input
AFB6_PTIO	Bi-Dir	Protected CMOS 1.8V	General purpose AFB I/O
AFB7_PTIO	Bi-Dir	Protected CMOS 1.8V	General purpose AFB I/O
AFB8_PTIO	Bi-Dir	Protected CMOS 1.8V	General purpose AFB I/O
AFB9_PTIO	Bi-Dir	Protected CMOS 1.8V	General purpose AFB I/O
AFB_DIFF0+ AFB_DIFF0-	Output or Bi-Dir	LVDS AFB	High speed pair for data transmit out of Module, or BiDir data
AFB_DIFF1+ AFB_DIFF1-	Input or Bi-Dir	LVDS AFB	High speed pair for data received into Module, or BiDir data
AFB_DIFF2+ AFB_DIFF2-	Output or Bi-Dir	LVDS AFB	High speed pair for data transmit out of Module, or BiDir data
AFB_DIFF3+ AFB_DIFF3-	Input or Bi-Dir	LVDS AFB	High speed pair for data received into Module, or BiDir data
AFB_DIFF4+ AFB_DIFF4-	Bi-Dir	LVDS AFB	High speed pair for data into or out of Module

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Figure 2 AFB Protected I/O Sketch



The suggested component values for the protection scheme above are 200 ohms for the Current Limiting Resistor and 100 nF for the Slew Rate Compensation Capacitor.

Modules that implement functions on the AFB_PTIO pins ***shall*** protect the pins such that they can withstand an indefinite short to GND or 1.8V. A protection scheme per the above ***should*** be used.

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4.21 IO Levels

4.21.1 Default I/O 1.8V

In the interest of minimizing system power, the majority of SMARC I/O is at a 1.8V level. Most SOCs used for SMARC systems are optimized for 1.8V I/O. Recall that the power required to charge and discharge the pin capacitance of a target IC is proportional to the **square** of the I/O voltage.

4.21.2 Signals At 3.3V

A few SMARC interfaces run at 3.3V to interface with industry standard devices on the Carrier that run at 3.3V. Such interfaces include the SD Card signals (SDIO_ prefix); the USBx_EN_OC# signals (x = 0,1,2); the USB0_OTG_ID signals; the PCIE_x support signals (x = A, B, C; support includes PCIE_x_CKREQ#, _RST# and _PRSNT#); the PCIE_WAKE# signal; the SATA_ACT# signal and the GBE_LINK_ signals.

4.21.3 Signals At 5V

The USB0_VBUS_DET signal is 5V tolerant.

4.21.4 Deprecation From Spec V1.0

In SMARC HW Specification V1.0, the VDD_IO pins were defined as optionally being either 1.8V or 3.3V. A SMARC pin, S158, was dedicated as a VDD_IO voltage flag pin. For 1.8V VDD_IO, the V1.0 specification ties S158 to GND.

The 3.3V option is deprecated this version, VDD_IO is set to 1.8V and S158 is a GND pin.

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4.22 Power and GND

Signal Name	Type / Tolerance	Use
VDD_IN	Power In	Module power input voltage - 3.0V min to 5.25V max
GND	Ground	Module signal and power return, and GND reference
VDD_RTC	Power In Power Out (when charging a Super Cap)	Low current RTC circuit backup power – 3.0V nominal May be sourced from a Carrier based Lithium cell or Super Cap. See ***Section 7.3 RTC Voltage Rail*** for an important safety note on the implementation of lithium backup batteries.

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4.23 JTAG

A CPU JTAG interface ***may*** be implemented on the Module, using a small form factor R/A SMT connector. The JTAG pins are used to allow test equipment and circuit emulators to have access to the Module CPU. The pin-out shown below ***may*** be used:

JTAG Conn Pin Number	Signal Name	Direction	Type / Tolerance	Description
1	VDD_JTAG_IO	Power	Power	JTAG I/O Voltage (sourced by Module)
2	JTAG_TRST#	Input	CMOS VDD_JTAG_IO	JTAG Reset, active low
3	JTAG_TMS	Input	CMOS VDD_JTAG_IO	JTAG mode select
4	JTAG_TDO	Output	CMOS VDD_JTAG_IO	JATG data out
5	JTAG_TDI	Input	CMOS VDD_JTAG_IO	JTAG data in
6	JTAG_TCK	Input	CMOS VDD_JTAG_IO	JTAG clock
7	JTAG_RTCK	Input	CMOS VDD_JTAG_IO	JTAG return clock
8	GND			
9	MFG_MODE#	Input	CMOS VDD_JTAG_IO	Pulled low to allow in-circuit SPI ROM update
10	GND			

The Module JTAG connector ***should*** be implemented with a JST SH series 1mm pitch R/A wire mount header (JST SM10B-SRSS-TB).

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4.24 Module Terminations

4.24.1 Module Input Terminations - General

Except as noted in the tables in the following two sub-sections, all Module inputs ***shall*** be terminated such that if the interface is used or not used, the proper pull up or pull down resistor or other termination mechanism is on the Module, either as a component on the PCB or as part of an IC used on the Module. If the Carrier Board does not use a particular interface, it ***shall*** be possible to leave the Module pin Not Connected on the Carrier. ***Except*** as noted below, pull-up resistors on the Carrier board for Module inputs are generally not required and ***should*** be avoided. They can cause Carrier to Module leakage problems.

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4.24.2 Module Terminations – Specific Recommendations

The Module signals listed below ***shall*** be terminated on the Module. The terminations ***should*** follow the guidance given in the table below, although the final decision on specific component values and types is left to the Module designer.

Signal Name	Series Termination (On Module)	Parallel Termination (On Module)	Notes
GPIOx		470K pull-ups to 1.8V	SOC internal pull-ups ***may*** be used.
HDMI_CTRL_DAT		100K pull-up to 1.8V	Carrier pull-up required
HDMI_CTRL_CK		100K pull-up to 1.8V	Carrier pull-up required
HDMI_CEC		100K pull-up to 1.8V	Carrier pull-up required
I2C_CAM_DAT		2.2K pull-up to 1.8V	
I2C_CAM_CK		2.2K pull-up to 1.8V	
I2C_GP_DAT		2.2K pull-up to 1.8V	
I2C_GP_CK		2.2K pull-up to 1.8V	
I2C_LCD_DAT		2.2K pull-up to 1.8V	
I2C_LCD_CK		2.2K pull-up to 1.8V	
I2C_PM_DAT		2.2K pull-up to 1.8V	
I2C_PM_CK		2.2K pull-up to 1.8V	
PCIE_A_TX+	0.1 uF 0402 capacitor		
PCIE_A_TX-	0.1 uF 0402 capacitor		
PCIE_B_TX+	0.1 uF 0402 capacitor		
PCIE_B_TX-	0.1 uF 0402 capacitor		
PCIE_C_TX+	0.1 uF 0402 capacitor		
PCIE_C_TX-	0.1 uF 0402 capacitor		
SATA0_TX+	0.1 uF 0402 capacitor		
SATA0_TX-	0.1 uF 0402 capacitor		
SATA0_RX+	0.1 uF 0402 capacitor		
SATA0_RX-	0.1 uF 0402 capacitor		
SDIO_CD#		10K pull-up to 3.3V	
SDIO_WP		10K pull-up to 3.3V	
USBx_EN_OC#		10K pull-up to 3.3V or a switched 3.3V rail on the Module	x is ‘0’ ‘1’ or ‘2’ Switched 3.3V: if a USB channel is not used, then the USBx_EN_OC# pull-up rail ***may*** be held at GND to prevent leakage currents.
All Other Inputs			All other inputs should be weakly terminated to their inactive states.

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4.25 Carrier / Off-Module Terminations

The following Carrier terminations are required, if the relevant interface is used. If unused, the SMARC Module pins may be left un-connected.

Module Signal Group Name	Carrier Series Termination	Carrier Parallel Termination	Notes
GBE MDI	Magnetics module appropriate for 10/100/1000 GBE transceivers	Secondary side center tap terminations appropriate for Gigabit Ethernet implementations	
GBE_LINK (GBE status LED sinks)		If used, current limiting resistors and diodes to pulled to a positive supply rail	The open drain GBE status signals, GBE_LINK100#, GBE_LINK1000# and GBE_LINK_ACT#, if used, need Carrier based current limiting resistors and LEDs. The LED may be integrated into a Carrier RJ45 jack. A resistor of 68 ohms, and a LED with the anode tied to Carrier 3.3V, is typical.
HDMI_CTRL_DAT HDMI_CTRL_CK HDMI_CEC		Pull-ups to 1.8V on each of these lines is required on the Carrier. The pull-ups may be part of an integrated HDMI ESD protection and control-line level shift device, such as the Texas Instruments TPD12S016. If discrete Carrier pull-ups are used, they should be 10K.	
LVDS LCD		100 ohm resistive termination across the differential pairs at the endpoint of the signal path, usually on the display assembly	
PCIE_x_RX	Series coupling caps near the TX pins of the Carrier board PCIe device		x is ‘A’ ‘B’ or ‘C’

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5 MODULE PIN-OUT MAP

5.1 Module Pin-Out

P-Pin	Primary (Top) Side	S-Pin	Secondary (Bottom) Side
		S1	PCAM_VSYNC
P1	PCAM_PXL_CK1	S2	PCAM_HSYNC
P2	GND	S3	GND
P3	CSI1_CK+ / PCAM_D0	S4	PCAM_PXL_CK0
P4	CSI1_CK- / PCAM_D1	S5	I2C_CAM_CK
P5	PCAM_DE	S6	CAM_MCK
P6	PCAM_MCK	S7	I2C_CAM_DAT
P7	CSI1_D0+ / PCAM_D2	S8	CSI0_CK+ / PCAM_D10
P8	CSI1_D0- / PCAM_D3	S9	CSI0_CK- / PCAM_D11
P9	GND	S10	GND
P10	CSI1_D1+ / PCAM_D4	S11	CSI0_D0+ / PCAM_D12
P11	CSI1_D1- / PCAM_D5	S12	CSI0_D0- / PCAM_D13
P12	GND	S13	GND
P13	CSI1_D2+ / PCAM_D6	S14	CSI0_D1+ / PCAM_D14
P14	CSI1_D2- / PCAM_D7	S15	CSI0_D1- / PCAM_D15
P15	GND	S16	GND
P16	CSI1_D3+ / PCAM_D8	S17	AFB0_OUT
P17	CSI1_D3- / PCAM_D9	S18	AFB1_OUT
P18	GND	S19	AFB2_OUT
P19	GBE_MDI3-	S20	AFB3_IN
P20	GBE_MDI3+	S21	AFB4_IN
P21	GBE_LINK100#	S22	AFB5_IN
P22	GBE_LINK1000#	S23	AFB6_PTIO
P23	GBE_MDI2-	S24	AFB7_PTIO
P24	GBE_MDI2+	S25	GND
P25	GBE_LINK_ACT#	S26	SDMMC_D0
P26	GBE_MDI1-	S27	SDMMC_D1
P27	GBE_MDI1+	S28	SDMMC_D2
P28	GBE_CTREF	S29	SDMMC_D3
P29	GBE_MDI0-	S30	SDMMC_D4
P30	GBE_MDI0+	S31	SDMMC_D5
P31	SPI0_CS1#	S32	SDMMC_D6
P32	GND	S33	SDMMC_D7
P33	SDIO_WP	S34	GND
P34	SDIO_CMD	S35	SDMMC_CK
P35	SDIO_CD#	S36	SDMMC_CMD
P36	SDIO_CK	S37	SDMMC_RST#
P37	SDIO_PWR_EN	S38	AUDIO_MCK

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P-Pin	Primary (Top) Side	S-Pin	Secondary (Bottom) Side
P38	GND	S39	I2S0_LRCK
P39	SDIO_D0	S40	I2S0_SDOUT
P40	SDIO_D1	S41	I2S0_SDIN
P41	SDIO_D2	S42	I2S0_CK
P42	SDIO_D3	S43	I2S1_LRCK
P43	SPI0_CS0#	S44	I2S1_SDOUT
P44	SPI0_CK	S45	I2S1_SDIN
P45	SPI0_DIN	S46	I2S1_CK
P46	SPI0_DO	S47	GND
P47	GND	S48	I2C_GP_CK
P48	SATA_TX+	S49	I2C_GP_DAT
P49	SATA_TX-	S50	I2S2_LRCK
P50	GND	S51	I2S2_SDOUT
P51	SATA_RX+	S52	I2S2_SDIN
P52	SATA_RX-	S53	I2S2_CK
P53	GND	S54	SATA_ACT#
P54	SPI1_CS0#	S55	AFB8_PTIO
P55	SPI1_CS1#	S56	AFB9_PTIO
P56	SPI1_CK	S57	PCAM_ON_CSI0#
P57	SPI1_DIN	S58	PCAM_ON_CSI1#
P58	SPI1_DO	S59	SPDIF_OUT
P59	GND	S60	SPDIF_IN
P60	USB0+	S61	GND
P61	USB0-	S62	AFB_DIFF0+
P62	USB0_EN_OC#	S63	AFB_DIFF0-
P63	USB0_VBUS_DET	S64	GND
P64	USB0_OTG_ID	S65	AFB_DIFF1+
P65	USB1+	S66	AFB_DIFF1-
P66	USB1-	S67	GND
P67	USB1_EN_OC#	S68	AFB_DIFF2+
P68	GND	S69	AFB_DIFF2-
P69	USB2+	S70	GND
P70	USB2-	S71	AFB_DIFF3+
P71	USB2_EN_OC#	S72	AFB_DIFF3-
P72	PCIE_C_PRSNT#	S73	GND
P73	PCIE_B_PRSNT#	S74	AFB_DIFF4+
P74	PCIE_A_PRSNT#	S75	AFB_DIFF4-
	<Key>		*<Key>*
P75	PCIE_A_RST#	S76	PCIE_B_RST#
P76	PCIE_C_CKREQ#	S77	PCIE_C_RST#
P77	PCIE_B_CKREQ#	S78	PCIE_C_RX+
P78	PCIE_A_CKREQ#	S79	PCIE_C_RX-
P79	GND	S80	GND
P80	PCIE_C_REFCK+	S81	PCIE_C_TX+

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P-Pin	Primary (Top) Side	S-Pin	Secondary (Bottom) Side
P81	PCIE_C_REFCK-	S82	PCIE_C_TX-
P82	GND	S83	GND
P83	PCIE_A_REFCK+	S84	PCIE_B_REFCK+
P84	PCIE_A_REFCK-	S85	PCIE_B_REFCK-
P85	GND	S86	GND
P86	PCIE_A_RX+	S87	PCIE_B_RX+
P87	PCIE_A_RX-	S88	PCIE_B_RX-
P88	GND	S89	GND
P89	PCIE_A_TX+	S90	PCIE_B_TX+
P90	PCIE_A_TX-	S91	PCIE_B_TX-
P91	GND	S92	GND
P92	HDMI_D2+	S93	LCD_D0
P93	HDMI_D2-	S94	LCD_D1
P94	GND	S95	LCD_D2
P95	HDMI_D1+	S96	LCD_D3
P96	HDMI_D1-	S97	LCD_D4
P97	GND	S98	LCD_D5
P98	HDMI_D0+	S99	LCD_D6
P99	HDMI_D0-	S100	LCD_D7
P100	GND	S101	GND
P101	HDMI_CK+	S102	LCD_D8
P102	HDMI_CK-	S103	LCD_D9
P103	GND	S104	LCD_D10
P104	HDMI_HPD	S105	LCD_D11
P105	HDMI_CTRL_CK	S106	LCD_D12
P106	HDMI_CTRL_DAT	S107	LCD_D13
P107	HDMI_CEC	S108	LCD_D14
P108	GPIO0 / CAM0_PWR#	S109	LCD_D15
P109	GPIO1 / CAM1_PWR#	S110	GND
P110	GPIO2 / CAM0_RST#	S111	LCD_D16
P111	GPIO3 / CAM1_RST#	S112	LCD_D17
P112	GPIO4 / HDA_RST#	S113	LCD_D18
P113	GPIO5 / PWM_OUT	S114	LCD_D19
P114	GPIO6 / TACHIN	S115	LCD_D20
P115	GPIO7 / PCAM_FLD	S116	LCD_D21
P116	GPIO8 / CAN0_ERR#	S117	LCD_D22
P117	GPIO9 / CAN1_ERR#	S118	LCD_D23
P118	GPIO10	S119	GND
P119	GPIO11	S120	LCD_DE
P120	GND	S121	LCD_VS
P121	I2C_PM_CK	S122	LCD_HS
P122	I2C_PM_DAT	S123	LCD_PCK
P123	BOOT_SEL0#	S124	GND
P124	BOOT_SEL1#	S125	LVDS0+

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P-Pin	Primary (Top) Side	S-Pin	Secondary (Bottom) Side
P125	BOOT_SEL2#	S126	LVDS0-
P126	RESET_OUT#	S127	LCD_BKLT_EN
P127	RESET_IN#	S128	LVDS1+
P128	POWER_BTN#	S129	LVDS1-
P129	SER0_TX	S130	GND
P130	SER0_RX	S131	LVDS2+
P131	SER0_RTS#	S132	LVDS2-
P132	SER0_CTS#	S133	LCD_VDD_EN
P133	GND	S134	LVDS_CK+
P134	SER1_TX	S135	LVDS_CK-
P135	SER1_RX	S136	GND
P136	SER2_TX	S137	LVDS3+
P137	SER2_RX	S138	LVDS3-
P138	SER2_RTS#	S139	I2C_LCD_CK
P139	SER2_CTS#	S140	I2C_LCD_DAT
P140	SER3_TX	S141	LCD_BKLT_PWM
P141	SER3_RX	S142	RSVD
P142	GND	S143	GND
P143	CAN0_TX	S144	RSVD / EDP_HPD
P144	CAN0_RX	S145	WDT_TIME_OUT#
P145	CAN1_TX	S146	PCIE_WAKE#
P146	CAN1_RX	S147	VDD_RTC
P147	VDD_IN	S148	LID#
P148	VDD_IN	S149	SLEEP#
P149	VDD_IN	S150	VIN_PWR_BAD#
P150	VDD_IN	S151	CHARGING#
P151	VDD_IN	S152	CHARGER_PRSNT#
P152	VDD_IN	S153	CARRIER_STBY#
P153	VDD_IN	S154	CARRIER_PWR_ON
P154	VDD_IN	S155	FORCE_RECOV#
P155	VDD_IN	S156	BATLOW#
P156	VDD_IN	S157	TEST#
		S158	GND

Notes:

1) SMARC HW Specification V1.1 showed pin S142 as LCD_DUAL_PCK.
2) SMARC HW Specification V1.1 showed pin S158 as VDD_IO_SEL#.

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6 MECHANICAL DEFINITIONS

6.1 Carrier Connector

The Carrier board connector is a 314 pin 0.5mm pitch right angle part designed for use with 1.2mm thick mating PCBs with the appropriate edge finger pattern. The connector is commonly used for MXM3 graphics cards. The SMARC Module uses the connector in a way quite different from the MXM3 usage.

Vendor	Vendor P/N	Stack Height	Body Height	Contact Plating	Pin Style	Body Color	Notes
Foxconn	AS0B821-S43B - *H	1.5mm	4.3mm	Flash	Std	Black	
Foxconn	AS0B821-S43N - *H	1.5mm	4.3mm	Flash	Std	Ivory	
Foxconn	AS0B826-S43B - *H	1.5mm	4.3mm	10 u-in	Std	Black	
Foxconn	AS0B826-S43N - *H	1.5mm	4.3mm	10 u-in	Std	Ivory	
Lotes	AAA-MXM-008-P04_A	1.5mm	4.3mm	Flash	Std	Tan	
Lotes	AAA-MXM-008-P03	1.5mm	4.3mm	15 u-in	Std	Tan	
Speedtech	B35P101-02111-H	1.56mm	4.0mm	Flash	Std	Black	
Speedtech	B35P101-02011-H	1.56mm	4.0mm	Flash	Std	Tan	
Speedtech	B35P101-02112-H	1.56mm	4.0mm	10 u-in	Std	Black	
Speedtech	B35P101-02012-H	1.56mm	4.0mm	10 u-in	Std	Tan	
Speedtech	B35P101-02113-H	1.56mm	4.0mm	15 u-in	Std	Black	
Speedtech	B35P101-02013-H	1.56mm	4.0mm	15 u-in	Std	Tan	
Aces	91781-314 2 8-001	2.7mm	5.2mm	3 u-in	Std	Black	
Foxconn	AS0B821-S55B - *H	2.7mm	5.5mm	Flash	Std	Black	
Foxconn	AS0B821-S55N - *H	2.7mm	5.5mm	Flash	Std	Ivory	
Foxconn	AS0B826-S55B - *H	2.7mm	5.5mm	10 u-in	Std	Black	
Foxconn	AS0B826-S55N - *H	2.7mm	5.5mm	10 u-in	Std	Ivory	
Speedtech	B35P101-02121-H	2.76mm	5.2mm	Flash	Std	Black	
Speedtech	B35P101-02021-H	2.76mm	5.2mm	Flash	Std	Tan	
Speedtech	B35P101-02122-H	2.76mm	5.2mm	10 u-in	Std	Black	
Speedtech	B35P101-02022-H	2.76mm	5.2mm	10 u-in	Std	Tan	
Speedtech	B35P101-02123-H	2.76mm	5.2mm	15 u-in	Std	Black	
Speedtech	B35P101-02023-H	2.76mm	5.2mm	15 u-in	Std	Tan	
Foxconn	AS0B821-S78B - *H	5.0mm	7.8mm	Flash	Std	Black	
Foxconn	AS0B821-S78N - *H	5.0mm	7.8mm	Flash	Std	Ivory	
Foxconn	AS0B826-S78B - *H	5.0mm	7.8mm	10 u-in	Std	Black	
Foxconn	AS0B826-S78N - *H	5.0mm	7.8mm	10 u-in	Std	Ivory	
Yamaichi	CN113-314-2001	5.0mm	7.8mm	0.3 u-meter	Std	Black	Automotive Grade

Other, taller stack heights may be available from these and other vendors. Stack heights as tall as 11mm are shown on the Aces web site.

Note: many of the vendor drawings for the connectors listed above show a PCB footprint pattern for use with an MXM3 graphics card. This footprint, and the associated pin numbering, is not suitable for SMARC use. The MXM3 standard gangs large groups of pins together to provide ~80W capable power paths needed for X86 graphics cards. The SMARC module “ungangs” these pins to allow more signal pins. Footprint and pin numbering information for application of this 314 pin connector to SMARC is given in the sections below.

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Note: JAE (Japan Aviation Electronics) manufactures an MXM3 connector with JAE part number MM70. This connector, unfortunately, is not quite suited for SMARC use as JAE omits 4 of the 314 pins that SMARC systems use. The 4 missing pins are:

- P146 (CAN1_RX)
- P147 (VDD_IN)
- S148 (LID#)
- S149 (SLEEP#)

If the above 4 signals are not needed in a given application, then the MM70 connector could be used if necessary. Of course omitting 1 of the 10 VDD_IN pins slightly de-rates the maximum amount of power that may be brought in.

6.2 Module and Carrier Connector Pin Numbering Convention

The Module pins are designated as P1 – P156 on the Module Primary (Top) side, and S1 – S158 on the Module Secondary (Bottom) side. There is a total of 314 pins on the Module. The connector is sometimes identified as a 321 pin connector, but 7 pins are lost to the key (4 on the primary side and 3 on secondary side).

The Secondary (Bottom) side faces the Carrier board when a normal or standard Carrier connector is used. Some connector vendors offer “reverse” pin-out connectors, which effectively flip the Module over such that the Module Primary side would face the Carrier board.

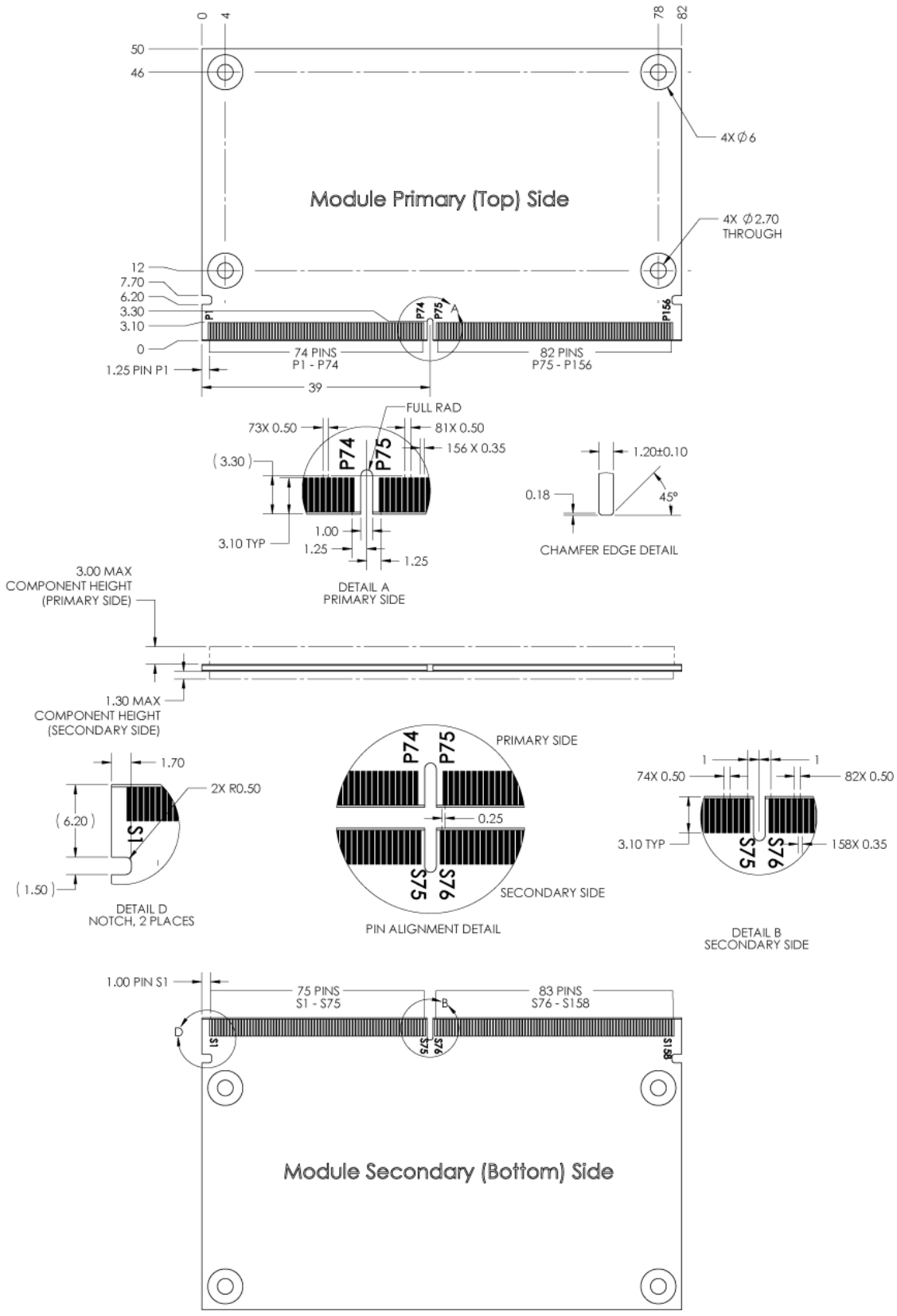
The SMARC Module pins are deliberately numbered as P1 – P156 and S1 – S158 for clarity and to differentiate the SMARC Module from MXM3 graphics modules, which use the same connector but use the pins for very different functions. MXM3 cards and MXM3 baseboard connectors use different pin numbering scheme.

6.3 Module Outline – 82mm x 50mm Module

The figure on the following page details the 82mm x 50mm Module mechanical attributes, including the pin numbering and edge finger pattern.

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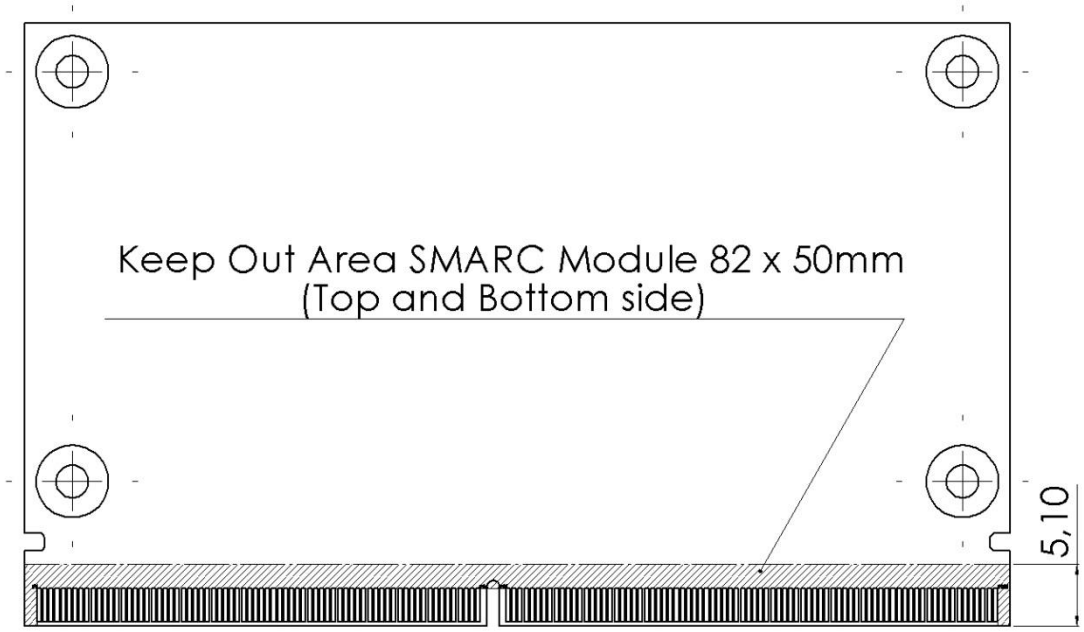
Figure 3 82mm x 50mm Module Outline



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It is recommended that Module components be kept away from the edge fingers, on the top and bottom sides, per the following figure:

Figure 4 Module Edge Finger Keep Out Area (82mm x 50mm Module)

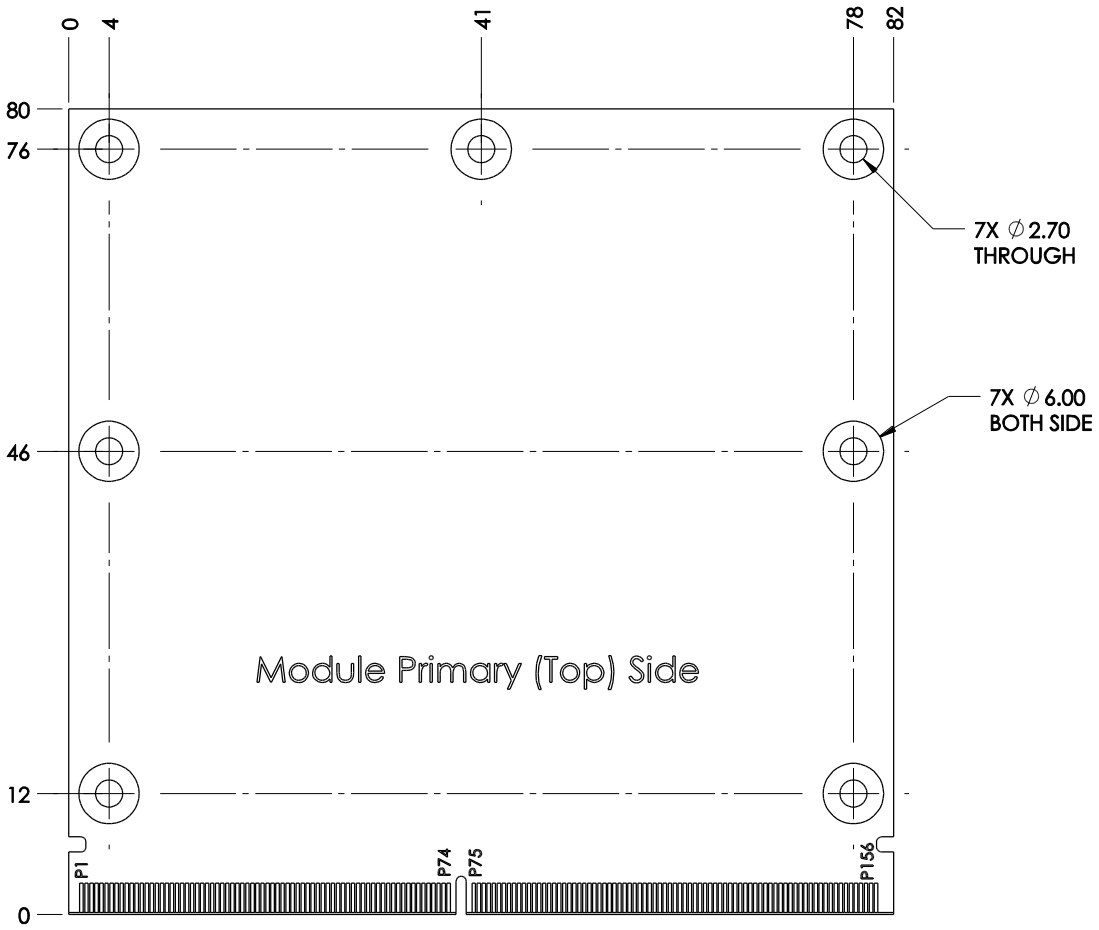


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6.4 Module Outline – 82mm x 80mm Module

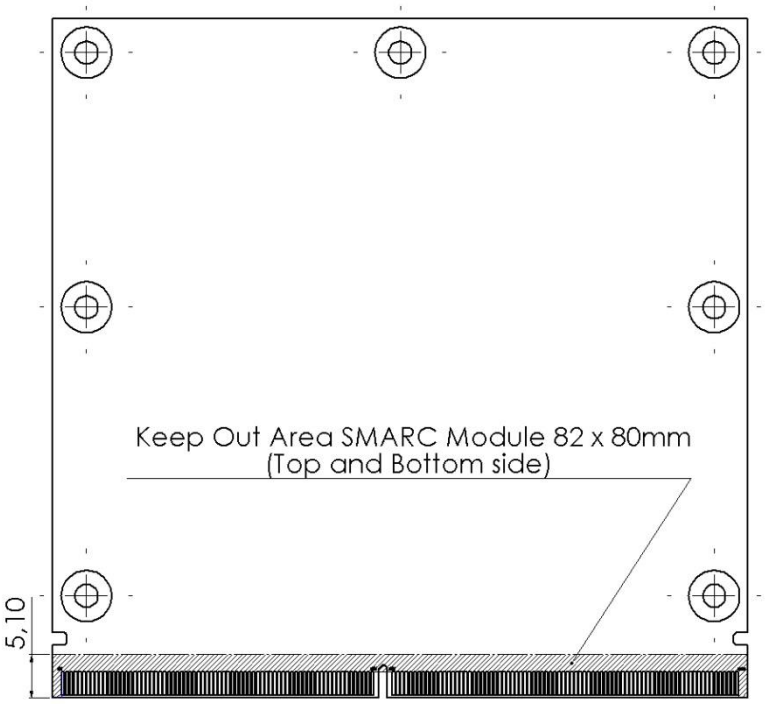
The 82mm x 80mm Module is shown in the figure below. The PCB edge finger pattern and spacing details relative to the board edges and lower mounting holes are the same as for the 82mm x 50mm case, and are not repeated here.

Figure 5 82mm x 80mm Module Outline



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Figure 6 Module Edge Finger Keep Out Area (82mm x 80mm Module)



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6.5 Module 'Z' Height Considerations

Note from ***Figure 3 82mm x 50mm Module Outline*** above that the component height on the Module is restricted to a maximum component height of 3mm on the Module Primary (Top) side and to 1.3mm on the Module Secondary (Bottom) side.

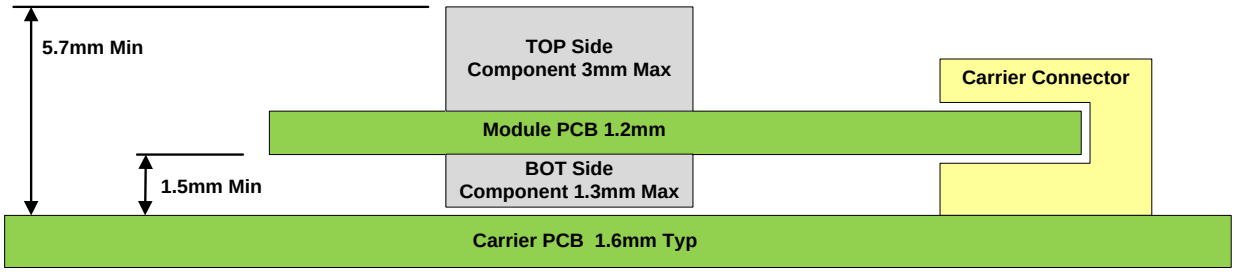
The 1.3mm Secondary side component height restriction allows the Module to be used with 1.5mm stack-height Carrier connectors. When used with 1.5mm stack height connectors, the 'Z' height profile from Carrier board Top side to tallest Module component is 5.7mm.

When a 1.5mm stack height Carrier board connector is used, there ***shall not*** be components on the Carrier board Top side in the Module region. Additionally, when 1.5mm stack height connectors are used, there ***should not*** be PCB traces on the Carrier top side in the Module shadow. This is to prevent possible problems with metallic Module heat sink attachment hardware that may protrude through the Module.

If Carrier board components are required in this region, then the Carrier components must be on the Carrier Bottom side, or a taller Module – to – Carrier connector may be used. Stack heights of 2.7mm, 3mm, 5mm and up are available.

Not shown in the figure below are any thermal dissipation components (heat sinks, heat spreaders, etc) nor is fastening hardware (standoffs, spacers, screws, washers, etc) shown. The dimensions of those components must of course be considered in a system design.

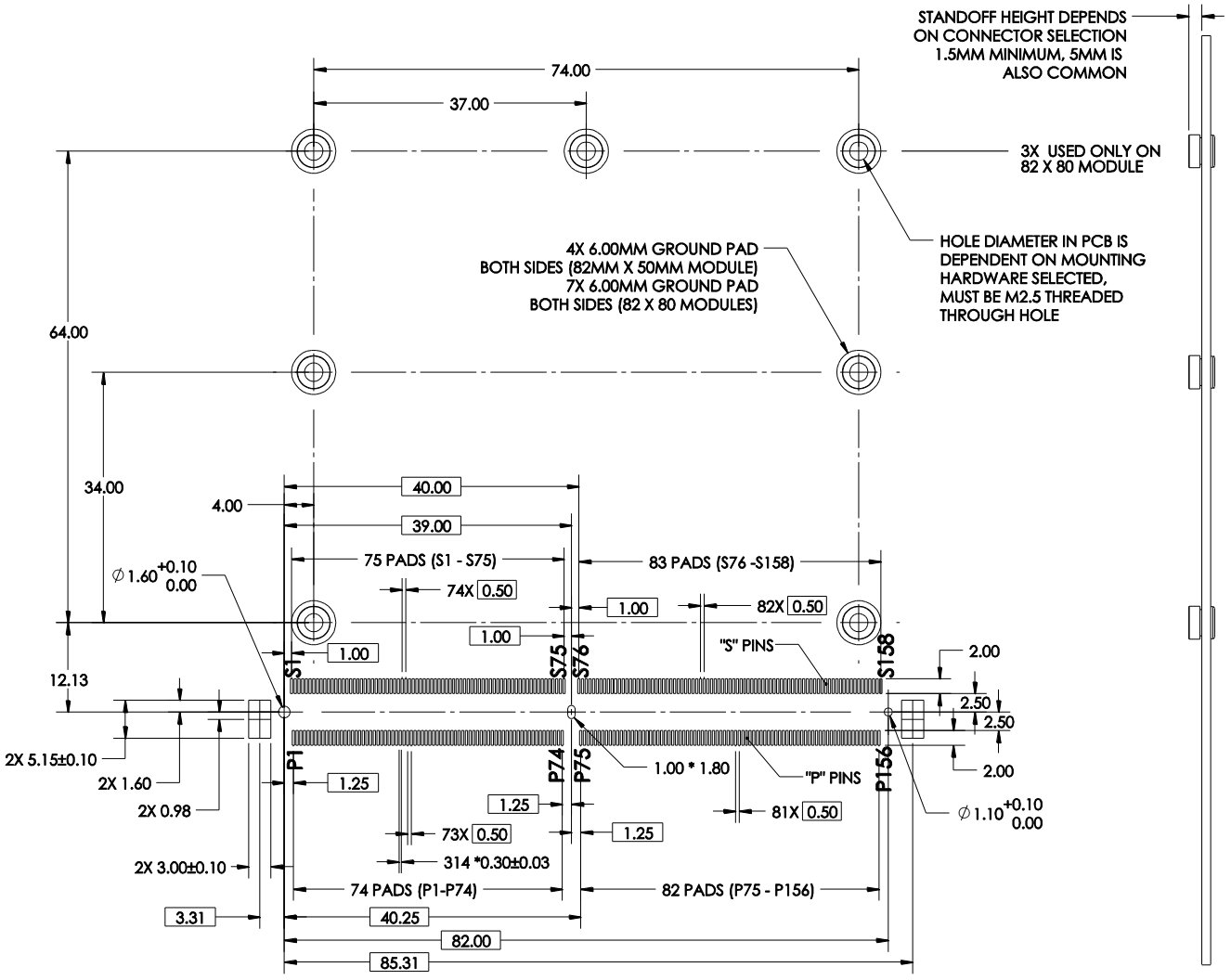
Figure 7 Module Minimum 'Z' Height



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6.6 Carrier Board Connector PCB Footprint

Figure 8 Carrier Board Connector PCB Footprint



Note: the pin numbering shown here is different from the pin numbering used in an MXM3 application. In an SMARC application, all 314 pins of the connector are used individually. The MXM3 power ganging is not used.

Note: the hole diameter for the 4 holes (82mm x 50mm Module) or 7 holes (82mm x 80mm Module) depends on the spacer hardware selection. See the section below for more information on this.

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6.7 Module and Carrier Board Mounting Holes – GND Connection

It ***shall*** be possible to tie all Module and Carrier board mounting holes to GND. The holes ***should*** be tied directly to the GND planes, although Module and Carrier designers ***may*** optionally make the mounting hole GND connections through passive parts, allowing the mounting holes to be isolated from GND if they feel it necessary.

6.8 Carrier Board Standoffs

Standoffs secured to the Carrier board are expected. The standoffs are to be used with M2.5 hardware. Most implementations will use Carrier board standoffs that have M2.5 threads (as opposed to clearance holes). A short M2.5 screw and washer, inserted from the Module top side, secures the Module to the Carrier board threaded standoff.

The SMARC connector board–to–board stack heights that are available may result in the use of non-standard spacer lengths. The board-to-board stack heights available include 1.5mm, 2.7mm and 5mm. Of these three, only the spacer for the 5mm stack would likely be a standard length.

Penn Engineering and Manufacturing (PEM) (**www.pemnet.com**) makes surface mount spacers with M2.5 internal threads. The product line is called SMTSO (“surface mount technology stand offs”). The shortest standard length offered is 2mm. A custom part with 1.5mm standoff length, M2.5 internal thread, and 5.56mm standoff OD is available from PEM. The PEM part number provided to Kontron for this is YSMTSO-2712-ET. The Carrier PCB requires a 4.22mm hole and 6.2mm pad to accept these parts.

Other vendors such as RAF Electronic Hardware (**www.rafhdwe.com**) offer M2.5 compatible swaged standoffs. Swaged standoffs require the use of a press and anvil at the CM. Their use is common in the industry. The standoff OD and Carrier PCB hole size requirements are different from the PEM SMTSO standoffs described above.

6.9 Thermal Attachment Points

Attachment points for thermal heat sinks and thermal dissipaters, if needed, are Module design dependent. Thermal hardware ***should*** be attached to the Module using attachment points other than the Module mounting holes (4 mounting holes for the 82mm x 50mm and 7 mounting holes for the 82mm x 80mm Module). The Module mounting holes ***should*** be clear for securing the Module to the Carrier.

Having thermal attachment points separate from the Module mounting holes allows the thermal solution to be shipped with the Module, attached to the Module with thermal interface materials applied, and avoids the disassembly of the thermal interface materials when the end-user places the Module into their system. The Module mounting holes ***may*** be used as supplemental thermal attachment points.

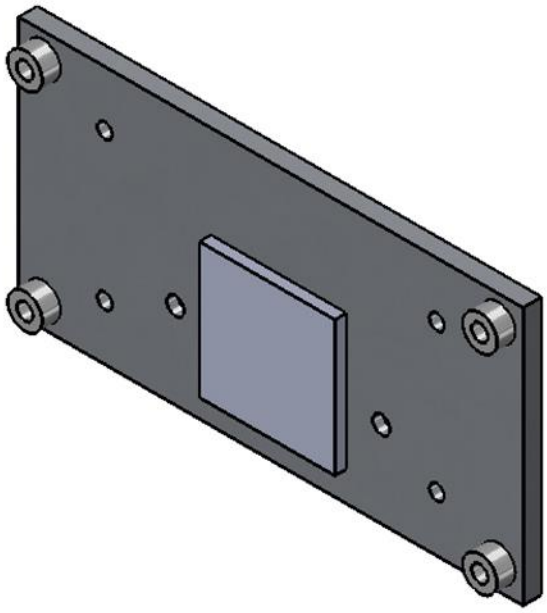
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6.10 Heat Spreader – 82mm x 50mm Module

A standard heat-spreader plate for use with the SMARC 82mm x 50mm form factor is described below. A standard heat spreader plate definition allows the customer to use a Module from multiple vendors, and the details of the thermal interface to the Module ICs – which can be tricky - becomes the Module designer's problem.

The heat spreader plate is sized at 82mm x 42mm x 3mm, and sits 3mm above the SMARC Module. The heat spreader plate 'Y' dimension is deliberately set at 42mm and not 50mm, to allow the plate to clear the SMARC MXM3 connector. The plate is shown in the figures below.

Figure 9 Heat Spreader Isometric View



The internal square in the figure above is a thermally conductive and mechanically compliant Thermal Interface Material (or "TIM"). The exact X-Y position and Z thickness details of the TIM vary from design to design.

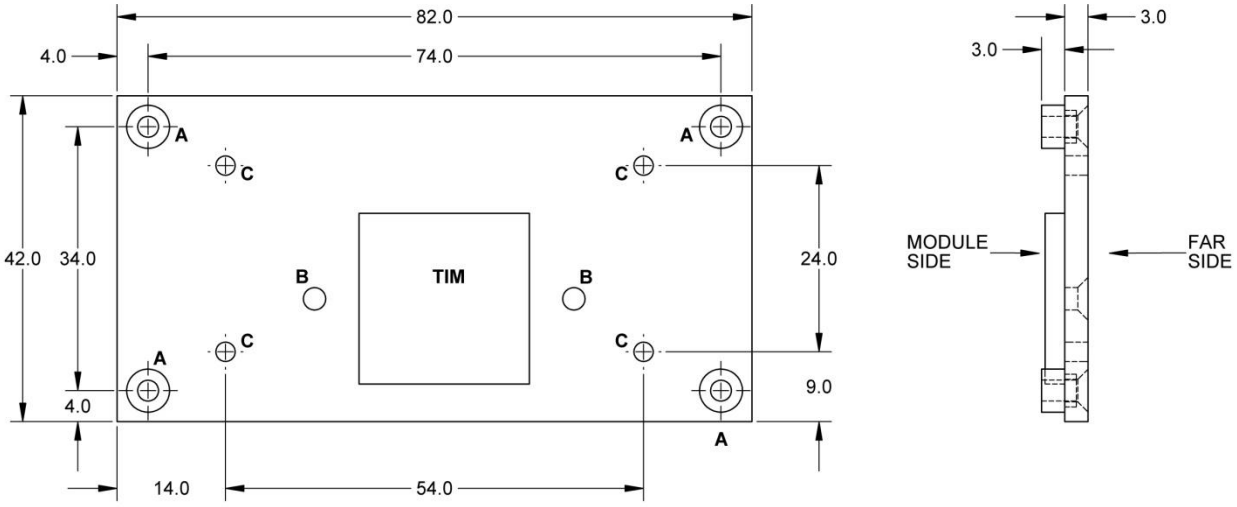
The two holes immediately adjacent to the TIM serve to secure the PCB in the SOC area and compress the TIM.

The four interior holes that are further from the center allow a heat sink to be attached to the heat spreader plate, or they can be used to secure the heat spreader plate to a chassis wall that serves as a heat sink.

Dimensions and further details may be found in the figure on the following page.

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Figure 10 Heat Spreader Plan View

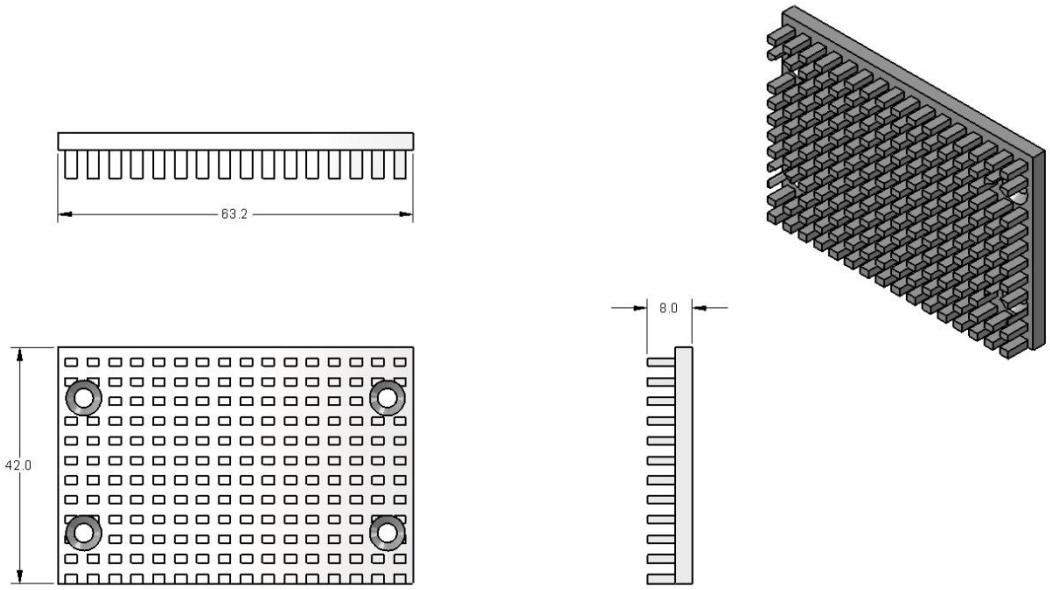


Dimensions in the figure above are in millimeters. “TIM” stands for “Thermal Interface Material”. The TIM takes up the small gap between the SOC top and the Module - facing side of the heat spreader.

Hole Reference	Description	Size
A	SMARC Module corner mounting holes Spacing determined by SMARC specification for 82mm x 50mm Modules. Typically these holes have 3mm length press fit or swaged clearance standoffs on the Module side. These holes are typically countersunk on the far side of the plate, to allow the heat spreader plate to be flush with a secondary heat sink.	Hole size depends on standoffs used. Standoff diameter must be compatible with SMARC Module mounting hole pad and hole size (6.0mm pads, 2.7mm holes on the Module). The holes and standoffs are for use with M2.5 screw hardware. The far side of these holes are counter-sunk to allow the attachment screw to be flush with the far side heat spreader surface.
B	Design – specific attachment points. The X-Y position, size and finish details of these holes may vary between designs.	Varies, design dependent The far side of these holes are counter-sunk to allow the attachment screw to be flush with the far side heat spreader surface.
C	Fixed location holes to allow the attachment of a heat sink to the heat spreader, or to allow the heat spreader to be secured to a chassis wall that can serve as a heat sink.	M3 threaded holes

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Figure 11 Heat Sink Attachment Option



This figure shows an optional heat sink that can be added on to the heat spreader plate. Some situations may require a taller heat sink and / or one with an embedded fan. The four holes in the heat sink above are used with M3 flat head screws. The screws engage the 'C' holes in the heat spreader plate in Figure 2 on the previous page. A relatively large, thin TIM is required between the heat spreader plate "Far Side" and the flat surface of the heat sink.

The heat sink Y dimension matches the 42mm Y dimension of the heat spreader plate. The X dimension of the heat sink is less, at 63.2 mm, than the 82 mm length of the heat spreader plate. This is to allow the heat sink to clear the four Module corner holes (the 'A' holes in Figure 2). The heat sink Z dimension can vary according to the thermal situation at hand.

Alternatively, the system enclosure wall may be used as the heat sink. In this case, the heat spreader plate is secured to the enclosure wall via the four 'C' holes shown in Figure 2 on the previous page. A large, thin TIM is then required between the heat spreader plate "Far Side" and the enclosure wall.

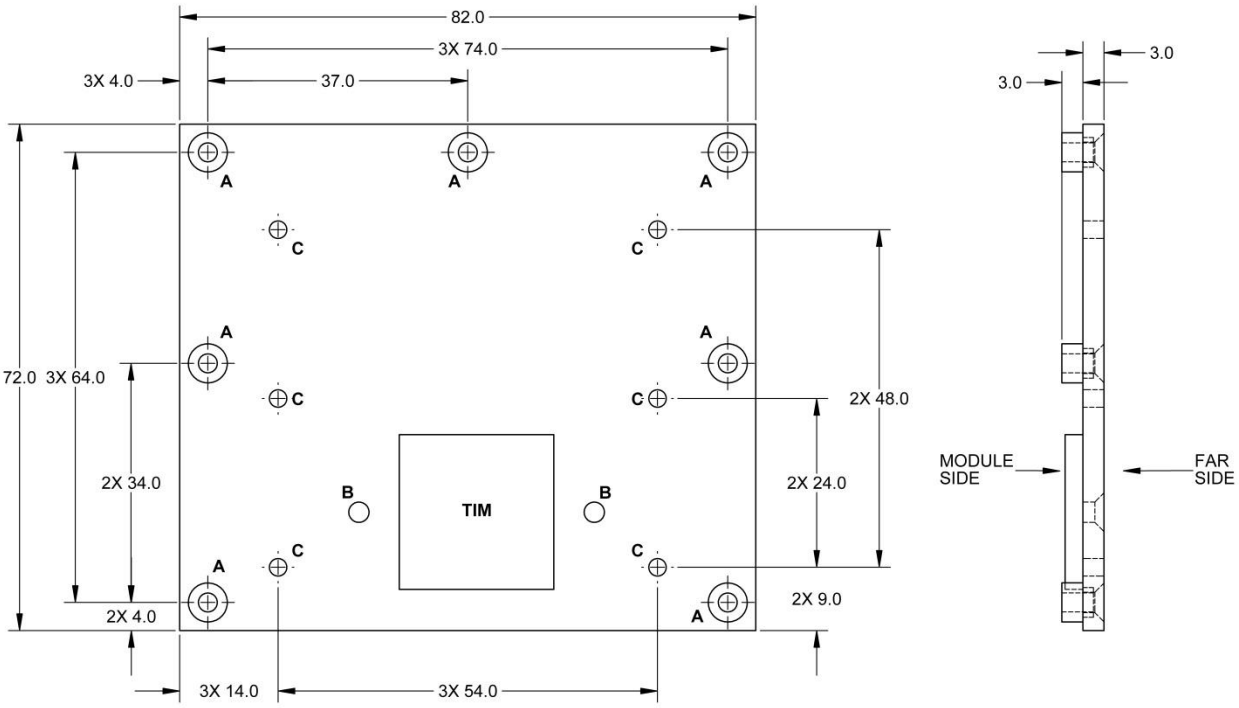
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6.11 Heat Spreader – 82mm x 80mm Module

The heat spreader for an 82mm x 80mm Module is similar to the heat spreader for the 82mm x 50mm Module, but is extended upward by 30mm and appropriate additional holes are provided. The ‘A’ and ‘C’ hole drill details are the same as the ‘A’ and ‘C’ holes on the heat spreader for the 82mm x 50mm Module.

The TIM and the B holes are not fixed, and may be in locations other than what is shown in the figure.

Figure 12 Heat Spreader - 82mm x 80mm Module



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7 MODULE POWER

7.1 Input Voltage / Main Power Rail

The Module input power voltage is brought in on the ten VDD_IN pins and returned through the numerous GND pins on the connector.

A Module ***shall*** withstand an indefinite exposure to an applied VDD_IN that may vary over the 3.0V to 5.25V range, without damage.

A Module ***should*** operate over the entire VDD_IN range of 3.0V to 5.25V.

Modules that use higher wattage SOCs ***may*** be designed to operate with a fixed 5V supply (4.75V to 5.25V).

Modules that are designed for rock-bottom cost and that use low power SOCs ***may*** be designed to operate with a fixed 3.3V supply (3.1V to 3.4V). They ***shall not*** be damaged in any way by exposure to the allowable VDD_IN range of 3.0 to 5.25V.

Ten pins are allocated to VDD_IN. The connector pin current rating is 0.5A per pin. This works out to 5A total for the 10 pins. At the lowest allowed Module input voltage of 3.0V, this would allow up to 15W of electrical power to be brought in (with no de-rating on the connector current capability). With a 40% connector current de-rating, up to 9W may be brought in at 3.0V.

If the fixed 5V input option is used, then 25W may be brought in over the 10 power pins (no de-rating). With a 40% connector de-rating, 15W are allowed to be brought in at 5V

As a practical matter, ARM most Module designs are expected to be 6W or less. X86 designs are expected to be in the 5W to 12W range, depending on the CPU SKU.

7.2 No Separate Standby Voltage

There is no separate voltage rail for standby power, other than the very low current (optional) RTC voltage rail. All Module operating and standby power comes from the single set of VDD_IN pins. This suits battery power sources well, and is also easy to use with non-battery sources.

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7.3 RTC Voltage Rail

RTC backup power ***may*** brought in on the VDD_RTC rail. The RTC consumption is typically 15 microA or less. The allowable VDD_RTC voltage range ***shall*** be 2.0V to 3.25V. The VDD_RTC rail ***may*** be sourced from a Carrier based Lithium cell or Super Cap, or it ***may*** be left open if the RTC backup functions are not required. The Module ***shall*** be able to boot without an external VDD_RTC voltage source.

Important: Lithium cells must be protected against charging by reverse currents, with a series Schottky diode and resistor. It is impractical to have the series diode on the Module, as this complicates the use of Super Caps (they need to be charged, over the Module VDD_RTC pin).

Lithium cells, if used, ***shall*** be protected against charging by a Carrier Schottky diode. The diode is placed in series with the positive battery terminal. The diode anode is on the battery side, and the cathode on the Module VDD_RTC side.

Note that if a Super cap is used, current may flow out of the Module VDD_RTC rail to charge the Super Cap.

7.4 Power Sequencing

The Module signal CARRIER_PWR_ON exists to ensure that the Module is powered before the main body of Carrier circuits (those outside the power and power control path on the Carrier). The main body of Carrier board circuits ***should not*** be powered until the Module asserts the CARRIER_PWR_ON signal as a high. Module hardware ***should*** assert CARRIER_PWR_ON when all Module supplies necessary for Module booting are up. The Module ***should*** continue to assert signal CARRIER_RESET_OUT# after the release of CARRIER_PWR_ON, for a period sufficient to allow Carrier power circuits to come up.

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7.5 System Power Domains

It is useful to describe an SMARC system as being divided into a hierarchy of three power domains:

1) Battery Charger power domain
2) SMARC Module power domain
3) Carrier Circuits power domain

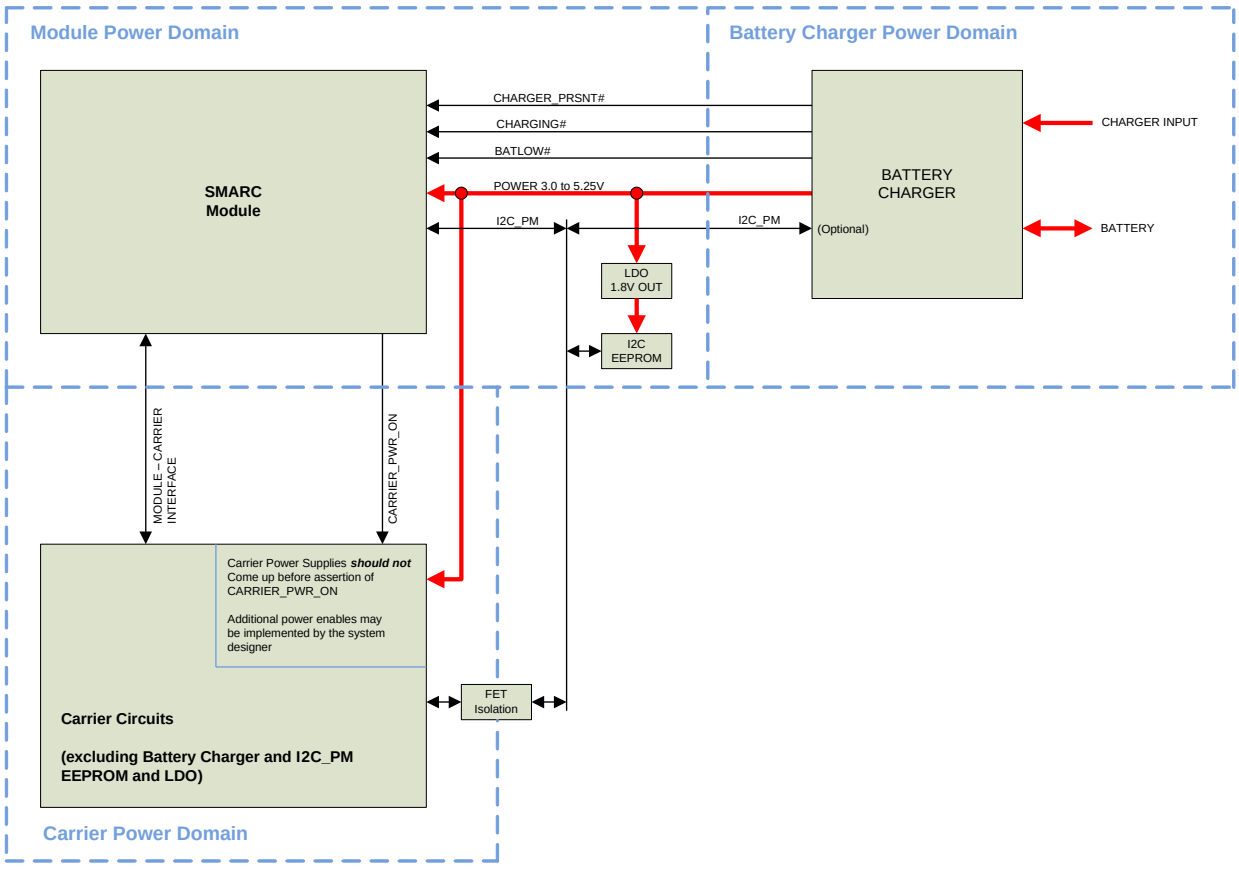
The Battery Charger domain includes circuits that are active whenever either charger input power and / or battery power are available. These circuits may include power supply supervisor(s), battery chargers, fuel gauges and, depending on the battery configuration, switching power section(s) to step down a high incoming battery voltage.

The SMARC Module domain includes the SMARC module and ***may*** include a serial EEPROM on the Carrier, connected to the I2C_PM I2C bus in the Module power domain, allowing Module software to read Carrier board parameters.

The Carrier Circuits domain includes “every thing else” (and does not include items from the Battery Charger and Module domain, even though they may be mounted on the Carrier).

This is illustrated in the figure below. Note: not shown in the figure is the additional, optional, fine grain power control that the Module may exert on the Carrier board, using design specific I/O. The power control I/O may be implemented via I2C I/O expanders (e.g. Texas Instruments TCA9554 or TC7408), or by other means.

Figure 13 System Power Domains



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8 MODULE AND CARRIER SERIAL EEPROMS

SMARC Modules ***shall*** include an I2C serial EEPROM on the Module I2C_PM bus. The device used ***should*** be an Atmel 24C32 or equivalent. The device ***shall*** operate at 1.8V. The Module serial EEPROM ***should*** be placed at I2C slave addresses A2 A1 A0 set to 0 (I2C slave address 50 hex, 7 bit address format or A0 / A1 hex, 8 bit format) (recall that for I2C EEPROMs, address bits A6 A5 A4 A3 are set to binary 0101 convention).

The Module serial EEPROM is intended to retain Module parameter information, including a Module serial number. The Module serial EEPROM data structure ***should*** conform to the ***PICMG® EEEP Embedded EEPROM Specification***.

SMARC Carriers ***may*** include an I2C serial EEPROM on the I2C_PM bus, in the Module power domain. The device used ***should*** be an Atmel 24C32 or equivalent. The device ***shall*** operate at 1.8V. The Carrier serial EEPROM ***should*** be placed with I2C slave addresses A2 A1 A0 set to binary 111 (I2C slave address 57 hex, 7 bit address format or AE / AF hex, 8 bit format).

The Carrier serial EEPROM is intended to retain Carrier parameter information. The Carrier serial EEPROM data structure ***should*** conform to the ***PICMG® EEEP Embedded EEPROM Specification***.

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9 APPENDIX A: LVDS LCD COLOR MAPPINGS

LVDS LCD Color Mappings

For flat panel use, parallel LCD data and control information (Red, green and blue color data; Display Enable, Vertical Synch, Horizontal Synch) are commonly serialized onto a set of LVDS differential pairs. The information is packed into frames that are 7 bits long. For 18 bit color depths, the data and control information utilize three LVDS channels (18 data bits + 3 control bits = 21 bits; hence 3 channels with 7 bit frames) plus a clock pair. For 24 bit color depths, four LVDS channels are used (24 data bits + 3 control bits + 1 unused bit = 28 bits, or 4 x 7) plus a clock pair.

The LVDS clock is transmitted as a separate LVDS pair. The LVDS clock period is 7 times longer than the pixel clock period. The LVDS clock edges are off from the 7 bit frame boundaries by 2 pixel periods.

Unfortunately, there are two different 24 bit color mappings in use. The more common one, sometimes referred to as “24 bit standard color mapping”, is not compatible with 18 bit panels, as it places the most significant RGB color data on the 4th LVDS data pair – the pair that is not used on 18 bit panels. There is a less common “24 bit / 18 bit compatible” mapping that puts the least significant color bits of the 24 bit set onto the 4th LVDS pair.

Some panels have pin straps that allow the user to select which color mapping is to be used.

The color mappings are summarized in the table below. The table includes a reference to a Texas Instruments LVDS transmitter, the SN75LVDS83B, showing the transmitter input pin names that TI lists in their sheet.

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Single Channel LVDS LCD Color Mappings – General Information

LVDS Channel	Transmit Bit Order	18 bit Standard	24 Bit Standard	24 Bit / 18 Bit Compatible	SN75LVDS83B Pin Name
0	1	G0	G0	G2	D7
	2	R5	R5	R7	D6
	3	R4	R4	R6	D4
	4	R3	R3	R5	D3
	5	R2	R2	R4	D2
	6	R1	R1	R3	D1
	7	R0	R0	R2	D0
1	1	B1	B1	B3	D18
	2	B0	B0	B2	D15
	3	G5	G5	G7	D14
	4	G4	G4	G6	D13
	5	G3	G3	G5	D12
	6	G2	G2	G4	D9
	7	G1	G1	G3	D8
2	1	DE	DE	DE	D26
	2	VS	VS	VS	D25
	3	HS	HS	HS	D24
	4	B5	B5	B7	D22
	5	B4	B4	B6	D21
	6	B3	B3	B5	D20
	7	B2	B2	B4	D19
3	1	<not used>	<not used>	<not used>	D23
	2	<not used>	B7	B1	D17
	3	<not used>	B6	B0	D16
	4	<not used>	G7	G1	D11
	5	<not used>	G6	G0	D10
	6	<not used>	R7	R1	D5
	7	<not used>	R6	R0	D27

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Single Channel LVDS LCD 24 Bit Standard Color Mapping – Carrier Connections

LVDS Channel	Transmit Bit Order	24 Bit Colors	Module Pin Name	SN75LVDS83B Pin Name
0	1	G0	LCD_D[8]	D7
	2	R5	LCD_D[21]	D6
	3	R4	LCD_D[20]	D4
	4	R3	LCD_D[19]	D3
	5	R2	LCD_D[18]	D2
	6	R1	LCD_D[17]	D1
	7	R0	LCD_D[16]	D0
1	1	B1	LCD_D[1]	D18
	2	B0	LCD_D[0]	D15
	3	G5	LCD_D[13]	D14
	4	G4	LCD_D[12]	D13
	5	G3	LCD_D[11]	D12
	6	G2	LCD_D[10]	D9
	7	G1	LCD_D[9]	D8
2	1	DE	LCD_DE	D26
	2	VS	LCD_VS	D25
	3	HS	LCD_HS	D24
	4	B5	LCD_D[5]	D22
	5	B4	LCD_D[4]	D21
	6	B3	LCD_D[3]	D20
	7	B2	LCD_D[2]	D19
3	1	<not used>	<not used>	D23
	2	B7	LCD_D[7]	D17
	3	B6	LCD_D[6]	D16
	4	G7	LCD_D[15]	D11
	5	G6	LCD_D[14]	D10
	6	R7	LCD_D[23]	D5
	7	R6	LCD_D[22]	D27

For a 24 bit standard color map single channel LVDS implementation, connect the Module pins to the Carrier board LVDS transmitter input pins as shown in the table above.

The LVDS transmitter clock input (pin name CLKIN on the TI SN75LVDS83B) ***should*** be driven by the Module parallel LCD interface pixel clock: the Module LCD_PCK pin.

Some LVDS transmitters, including the SN75LVDS83B, have a pin allowing the user to select which edge of the pixel clock is to be used to latch the data coming in to the LVDS transmitter. In most cases, this pin should be set for a rising edge clock latching. A resistor or jumper option allowing either edge to be used is recommended.

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Dual Channel LVDS LCD 24 Bit Standard Color Mapping – Carrier Connections

Dual channel LVDS implementations are used to drive high resolution panels (generally, panel resolutions of 1280 x 1024 and above). In a dual channel implementation, the parallel pixel data is fed to a pair of LVDS transmitters. The pair of transmitters form two sets of LVDS streams (“dual channel”). The first set has the odd pixel information and the second set has the even pixel information. By convention, the upper left most pixel on a display is “odd”, the next one on the line is “even”, and so on.

A 24 bit dual channel LVDS implementation comprises 10 differential pairs: 4 pairs for odd pixel and control data; 1 pair for the LVDS clock for the odd data; 4 pairs for the even pixel data and control data, and 1 pair for the even LVDS clock.

The data is clocked into the pair of Carrier Board LVDS transmitters by Module signal LCD_DUAL_PCK. The rising edge of this clock is used to latch the odd pixels, and the falling edge for the even pixels,

The same 18 / 24 bit color mapping considerations described earlier in this document apply to dual channel displays. However, as dual channel displays are higher end products, they tend to be 24 bit devices, usually with the standard 24 bit color mapping.

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10 APPENDIX B: ALTERNATE FUNCTION BLOCK USE MODELS

10.1 Alternate Function Block: MOST Media Local Bus MLB-150 Use

The MOST Media Local Bus is used in the automotive industry for infotainment. MLB-150 is the high speed, differential version of the standard. An SMARC AFB implementation ***may*** be realized per the tables below.

Signal Name	Direction	Type	Description	AFB Mapping
MLB_CK+ MLB_CK-	Output	LVDS MLB	MOST Bus MediaLB Clock differential pair	AFB_DIFF2+ AFB_DIFF2-
MLB_DAT+ MLB_DAT-	Bi-Dir	LVDS MLB	MOST Bus MediaLB Data differential pair	AFB_DIFF3+ AFB_DIFF3-
MLB_SIG+ MLB_SIG-	Bi-Dir	LVDS MLB	MOST Bus MediaLB Signal differential pair	AFB_DIFF4+ AFB_DIFF4-
MLB_RST#	Output	Protected CMOS 1.8V	Low level to reset MLB	AFB8_PTIO
MLB_PWRDN#	Output	Protected CMOS 1.8V	Low level for MLB Power down	AFB9_PTIO

.

An I2C interface is needed for MOST bus support. The Module I2C_GP port ***may*** be used.

Signal Name	Direction	Type	Description
I2C_GP_DAT I2C_GP_CK	Bi-Dir OD	CMOS 1.8V	General purpose I2C may be used for MOST support.

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10.2 Alternate Function Block: Dual GBE Use

The magnetics referred to in the table below are based on the Carrier board.

Signal Name	Direction	Type	Description	AFB Mapping
GBE_1_MDI0+ GBE_1_MDI0-	Bi-Dir	GBE MDI	Bi-directional transmit/receive pair 0 to magnetics (Media Dependent Interface) for AFB 2nd GBE	AFB_DIFF0+ AFB_DIFF0-
GBE_1_MDI1+ GBE_1_MDI1-	Bi-Dir	GBE MDI	Bi-directional transmit/receive pair 1 to magnetics (Media Dependent Interface) for AFB 2nd GBE	AFB_DIFF1+ AFB_DIFF1-
GBE_1_MDI2+ GBE_1_MDI2-	Bi-Dir	GBE MDI	Bi-directional transmit/receive pair 2 to magnetics (Media Dependent Interface) for AFB 2nd GBE	AFB_DIFF2+ AFB_DIFF2-
GBE_1_MDI3+ GBE_1_MDI3-	Bi-Dir	GBE MDI	Bi-directional transmit/receive pair 3 to magnetics (Media Dependent Interface) for AFB 2nd GBE	AFB_DIFF3+ AFB_DIFF3-
GBE_1_ CTREF	Output	Ref Voltage	Central-Tap reference voltage for Carrier board Ethernet magnetic for AFB 2nd GBE	AFB0_OUT
GBE_1_ LINK100#	Output OD	CMOS 3.3V Tolerant	Link Speed Indication LED for 100Mbps for AFB 2nd GBE	AFB6_PTIO
GBE_1_LINK1000#	Output OD	CMOS 3.3V Tolerant	Link Speed Indication LED for 1000Mbps for AFB 2nd GBE	AFB7_PTIO
GBE_1_LINK#_ACT	Output OD	CMOS 3.3V Tolerant	Link / Activity Indication LED for AFB 2nd GBE Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity	AFB8_PTIO

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10.3 Alternate Function Block: Industrial Network Use

The Alternate Function Block ***may*** be used to implement Industrial Network features. Industrial Networks are optimized for real-time control of industrial systems, and include features such as Real Time Ethernet channels and Fieldbus implementations.

Ethernet magnetic are implemented on the Carrier board.

Signal Name	Direction	Type	Description	AFB Mapping
RTE0_TXD+ RTE0_TXD-	Output	10 /100Base-TX	Real Time Ethernet 0 MDI transmit data pair	AFB_DIFF0+ AFB_DIFF0-
RTE0_RXD+ RTE0_RXD-	Input	10 /100Base-TX	Real Time Ethernet 0 MDI receive data pair	AFB_DIFF1+ AFB_DIFF1-
RTE1_TXD+ RTE1_TXD-	Output	10 /100Base-TX	Real Time Ethernet 1 MDI transmit data pair	AFB_DIFF2+ AFB_DIFF2-
RTE1_RXD+ RTE1_RXD-	Input	10 /100Base-TX	Real Time Ethernet 1 MDI receive data pair	AFB_DIFF3+ AFB_DIFF3-
RTE_SYNC_0	Output	CMOS 1.8V	Real Time Ethernet synchronization signal 0	AFB0_OUT
RTE_SYNC_1	Output	CMOS 1.8V	Real Time Ethernet synchronization signal 1	AFB1_OUT
RTE0_LINK#	Output	CMOS	Real Time Ethernet link indication channel 0	AFB6_PTIO
RTE0_ACT#	Output	CMOS	Real Time Ethernet activity indication channel 0	AFB7_PTIO
RTE1_LINK#	Output	CMOS	Real Time Ethernet link indication channel 1	AFB8_PTIO
RTE1_ACT#	Output	CMOS	Real Time Ethernet activity indication channel 1	AFB9_PTIO
FB_TXD	Output	CMOS 1.8V	Fieldbus transmit data	AFB2_OUT
FB_RXD	Input	CMOS 1.8V	Fieldbus receive data	AFB3_IN
FB_IO0	Bi-Dir	CMOS 1.8V	Fieldbus control 0; network dependent. Used as a transmitter enable output or as a failure input signal.	AFB4_IN
FB_IO1	Bi-Dir	CMOS 1.8V	Fieldbus control 1. Reserved	AFB5_IN

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Real Time Ethernet and Fieldbus implementations typically use a number of LEDs to indicate the system status. Four SMARC GPIOs are selected to support such LEDs. The LED usage conventions vary by the Fieldbus type, and are not covered in this document.

Signal Name	Direction	Type	Description	GPIO Mapping
FB_LED0_G#	Output	CMOS 1.8V	Communication status 0 Used to drive green LED	GPIO0
FB_LED0_R#	Output	CMOS 1.8V	Communication status 0 Used to drive red LED	GPIO1
FB_LED1_G#	Output	CMOS 1.8V	Communication status 1 Used to drive green LED	GPIO2
FB_LED1_R#	Output	CMOS 1.8V	Communication status 1 Used to drive red LED	GPIO3

A Fieldbus bus implementation ***may*** need additional I/Os, address switches, or status LEDs. These ***may*** be realized on the Carrier board using I2C bus peripheral devices. The Module I2C_GP port ***may*** be used to support this.

Signal Name	Direction	Type	Description
I2C_GP_DAT I2C_GP_CK	Bi-Dir OD	CMOS 1.8V	General purpose I2C may be used for MOST support.

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10.4 Alternate Function Block: Intel Bay Trail Use

The following table outlines the recommended mapping of SMARC AFB pins for Intel Bay Trail use.

AFB Signal	Type / Dir	SMARC Standard Use	SMARC with Intel Bay Trail	Notes
AFB0_OUT	Out	Reserved	Intel SOC PMC_SLP_S3#	Intel sleep state status S3: suspend to RAM
AFB1_OUT	Out	Reserved	Intel SOC PMC_SLP_S4#	Intel sleep state status S3: suspend to disk
AFB2_OUT	Out	Reserved	Intel SOC PMC_SUS_STAT#	Intel Suspend Status signal
AFB3_IN	In	Reserved		
AFB4_IN	In	Reserved		
AFB5_IN	In	Reserved		
AFB6_PTIO	Protected Bi-Dir	Reserved	EN_OC# for USB SS on AFB	USB 3 port power enable and overcurrent
AFB7_PTIO	Protected Bi-Dir	Reserved	PCU_SMB_ALERT#	SM Bus Alert# (interrupt) signal
AFB8_PTIO	Protected Bi-Dir	Reserved		
AFB9_PTIO	Protected Bi-Dir	Reserved		
AFB_DIFF0+ AFB_DIFF0-	HS Pair Out or Bi-Dir	Reserved	Intel SOC USB3_TXP Intel SOC USB3_TXN	These Super Speed pairs and USB 2 pair form a single USB 3 port. Coupling caps for USB 3 TX and RX pairs are ***off***-Module.
AFB_DIFF1+ AFB_DIFF1-	HS Pair In or Bi-Dir	Reserved	Intel SOC USB3_RXP Intel SOC USB3_RXN	
AFB_DIFF2+ AFB_DIFF2-	HS Pair Out or Bi-Dir	Reserved	Intel SOC USB_DP0 Intel SOC USB_DN0	
AFB_DIFF3+ AFB_DIFF3-	HS Pair In or Bi-Dir	Reserved	Intel SATA1_TXP Intel SATA1_TXN	Coupling caps are ***on***-Module
AFB_DIFF4+ AFB_DIFF4-	HS Pair In, Out or Bi-Dir	Reserved	Intel SATA1_RXP Intel SATA1_RXN	Coupling caps are ***on***-Module

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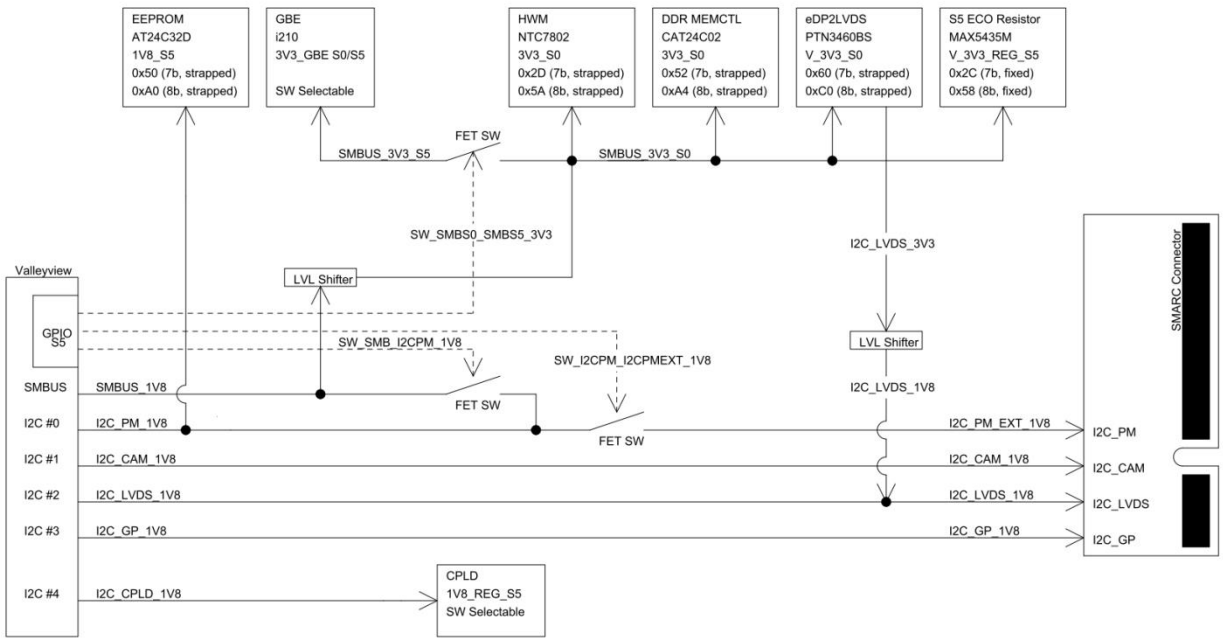
10.4.1 Additional SMARC to Intel Bay Trail Mapping Recommendations: I2C

The Intel Bay Trail SOC has seven I2C ports, designated I2C0 through I2C6 by Intel. Additionally, there is an SM Bus, which is an I2C superset and has I2C compatibility modes. A recommended mapping of Intel I2C ports to SMARC I2C ports is shown in the figure below. Intel ports I2C5 and I2C6 are not used.

The peripheral blocks at the top of the figure are from a specific design and may be regarded as for illustration only in this context. They are not part of the SMARC specification.

The SMARC I2C_PM bus and the x86 SM Bus serve similar functions, and the recommendation is to merge them on SMARC designs, as shown in the figure.

Figure 14 SMARC I2C Intel Bay Trail I2C Mapping Recommendation



The SMARC I2C_PM bus is meant as a power management bus. It may be active whenever the system has power (including the S5 “soft off” and S6 “deep soft off” states). The SOC connection should not drag down the SMARC I2C_PM bus (labeled I2C_PM_EXT_1V8 in the figure above – the FET switch should be open when the SOC is in the S6 state).

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10.5 Alternate Function Block Summary Comparisons

Alternate Function Block – Possible Uses Comparison Chart

AFB Signal	Type / Dir	USB 3.0	MOST / MLB	Dual GBE	Industrial Network	DSI	Intel Bay Trail
AFB0_OUT	Out			GBE_1_CTREF	RTE_SYNC_0		Intel SOC PMC_SLP_S3#
AFB1_OUT	Out				RTE_SYNC_1		Intel SOC PMC_SLP_S4#
AFB2_OUT	Out				FB_TXD		Intel SOC PMC_SUS_STAT#
AFB3_IN	In				FB_RXD		
AFB4_IN	In				FB_IO0 (Bi-Dir)		
AFB5_IN	In				FB_IO1 (Bi-Dir)		
AFB6_PTIO	Protected Bi-Dir			GBE_1_LINK100#	RTE0_LINK#		EN_OC# for USB SS on AFB
AFB7_PTIO	Protected Bi-Dir			GBE_1_LINK1000#	RTE0_ACT#		PCU_SMB_ALERT#
AFB8_PTIO	Protected Bi-Dir		MLB_RST#	GBE_1_LINK_ACT#	RTE1_LINK#		
AFB9_PTIO	Protected Bi-Dir		MLB_PWRDN#		RTE1_ACT#		
AFB_DIFF0+ AFB_DIFF0-	HS Pair Out or Bi-Dir	USB1_SSTX0+ USB1_SSTX0-		GBE_1_MDIO+ GBE_1_MDIO-	RTE0_TXD+ RTE0_TXD-		Intel SOC USB3_TXP Intel SOC USB3_TXN
AFB_DIFF1+ AFB_DIFF1-	HS Pair In or Bi-Dir	USB1_SSRX0+ USB1_SSRX0-		GBE_1_MDI1+ GBE_1_MDI1-	RTE0_RXD+ RTE0_RXD-		Intel SOC USB3_RXP Intel SOC USB3_RXN
AFB_DIFF2+ AFB_DIFF2-	HS Pair Out or Bi-Dir	USB2_SSTX0+ USB2_SSTX0-	MOST_MLB_CK+ MOST_MLB_CK-	GBE_1_MDI2+ GBE_1_NDI2-	RTE1_TXD+ RTE1_TXD-	DSI_CK+ DSI_CK-	Intel SOC USB_DP0 Intel SOC USB_DN0
AFB_DIFF3+ AFB_DIFF3-	HS Pair In or Bi-Dir	USB2_SSRX0+ USB2_SSRX0-	MOST_MLB_DAT+ MOST_MLB_DAT-	GBE_1_MDI3+ GBE_1_MDI3-	RTE1_RXD+ RTE1_RXD-	DSI_D0+ DSI_D0-	Intel SATA1_TXP Intel SATA1_TXN
AFB_DIFF4+ AFB_DIFF4-	HS Pair In, Out or Bi-Dir		MOST_MLB_SIG+ MOST_MLB_SIG-			DSI_D1+ DSI_D1-	Intel SATA1_RXP Intel SATA1_RXN

Please refer to the individual AFB interface sections above for details such as coupling cap locations.

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11 APPENDIX C: DOCUMENT CHANGES

11.1 SMARC HW Specification Changes V1.0 to V1.1

Section Ref	Change Description
Various	Sections and Section Numbers that existed in V1.0 still exist in V1.1x
Various	Figure Numbers have changed as one Figure was removed and four Figures were added
Various	Version changed to V1.1x with Feb 4, 2014 date mark
	Copyright © notice changed to 2014
TOC	Table of Contents updated
TOF	Table of Figures updated
Various	VDD_IO references all changed to 1.8V
2.3	Pin Group Summary updated
3.1	Required and Optional Features Table updated • RTC added to table • DP over HDMI pins added to table
4.1	Signal Direction and Type Definitions updated: • VDD_IO reference removed • Previous VDD_IO references change to 1.8V • CMOS 1.5V* Type added for HD Audio
4.2.4	Carrier Board Dual Channel LVD Support section re-written • References to LCD_DUAL_PCK removed • Former Figure 1 removed • Text updated
4.2.7	Expanded this section, described DP operation over HDMI pins
4.3.3	Former Figure 2 (now Figure 1) changed VDD_IO reference to CARRIER 1.8V
4.5.1	Added text to indicate that SPI0_CS0# signals should be used to select Carrier SPI boot device
4.7	HDA Interface • Type / Tolerance changed to CMOS 1.5V* • New text added
4.21	Section renamed to 4.21 I/O Levels • Table removed • Text re-written to describe the various voltage levels used
4.24.2	Module Terminations • Table revised • SDIO_WP added • SDIO_CD# added
5.1	Module Pin-Out • Signal LCD_DUAL_PCK (pin S142) removed. Pin S142 now marked as RSVD. • Signal VDD_IO_SEL# (pin S158) was removed. Pin S158 now listed as GND
6.1	Added note about JAE MM70 connector
6.3	Added figure from Adlink on recommended edge finger keep out area for 82mm x 50mm Modules
6.4	Added figure from Adlink on recommended edge finger keep out area for 82mm x 80mm Modules
6.10	New Section: Heat Spreader – 82mm x 50mm Module • Three Figures added
6.11	New Section: Heat Spreader – 82mm x 80mm Module • New Figure added

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Section Ref	Change Description
7.1	Input Voltage / Main Power Rail • Section re-written • 5V fixed option described • 3.3V fixed option described
7.3 and Various	Clarified that RTC is optional
10.4	Added new Section 10.4 (old 10.4 becomes 10.5). New section outlines use of SMARC AFB with Intel Bay Trail
10.4.1	Added section with additional Intel Bay Trail recommendations on I2C Mappings
10.5	Old section 10.4 becomes 10.5. Updated AFB use case comparison table to include Intel Bay Trail.

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