CoreModule® 740
Single Board Computer
Reference Manual

P/N 50-1Z046-1010

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Notice Page

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REVISION HISTORY

Revision	Reason for Change	Date
1000	Initial Release	July/10
1010	Revised I/O Paddle Board in App. B; removed JP1 jumper header; removed U13 temp monitor; added BIOS Setup settings to ch. 4; added simplified pin out tables to ch 3	May/11

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Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

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Chapter 1 About This Manual

Purpose of this Manual

This manual is for designers of systems based on the CoreModule™ 740 single board computer (SBC). This manual contains information that permits designers to create an embedded system based on specific design requirements.

Information provided in this reference manual includes:

- Product Overview
- Hardware Specifications
- BIOS Setup information
- Technical Support Contact Information

Information not provided in this reference manual includes:

- Detailed chip specifications
- Internal component operation
- Internal registers or signal operations
- Bus or signal timing for industry standard busses and signals
- Pinout definitions for industry standard interfaces

References

The following list of references may help you successfully complete your custom design.

Specifications

- PC/104 Specification, Revision 2.5, November, 2003
- PC/104-Plus Specification, Revision 2.0, November, 2003

  For latest revision of the PC/104 specifications, contact the PC/104 Consortium, at:

  Web site: http://www.pc104.org
- PCI 2.2 Compliant Specifications, Revision 2.2, December 18, 1998

  For latest revision of the PCI specifications, contact the PCI Special Interest Group at:

  Web site: http://www.pcisig.com
- AMI BIOS Core 8 User's Guide

  Data sheet: http://www.ami.com/support/doc/MAN-EZP-80.pdf

Chip Specifications

The following integrated circuits (ICs) are used in the CoreModule 740 single board computer:

- Intel® Corporation and the N450 processor

  Web site:

  http://www.intel.com/products/processor/atom/techdocs.htm
- Intel and the ICH8-M chip, used for the I/O Hub (Southbridge)

  Data sheet:

  http://www.intel.com/assets/pdf/datasheet/313056.pdf

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- SMSC and the Super I/O SCH3112I-NU chip used for the Super I/O controller

  Data sheet:

  http://www.smsc.com/media/Downloads_Public/Data_Briefs/311xdb.pdf

- Maxim Integrated Products and the MAX213ECAI+ RS-232 Serial Port transceiver

  Web site:

  http://www.maxim-ic.com/quick_view2.cfm/qv_pk/1047

- Integrated Technology Express, Inc. and the PCI-to-ISA bridge, IT8888G-L

  Web site: http://www.iteusa.com or http://www.ite.com.tw

NOTE	If you are unable to locate the datasheets using the links provided, go to the manufacturer's web site where you can perform a search using the chip datasheet number or name listed, including the extension (htm for web page, pdf for files name, etc.)

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Chapter 2 Product Overview

This introduction presents general information about the PC/104 architecture and the CoreModule 740 single board computer (SBC). After reading this chapter you should understand:

- PC/104 architecture
- Product description
- CoreModule 740 features
- Major components (ICs)
- Headers and Connectors
- Specifications

PC/104 Architecture

The PC/104 architecture affords a great deal of flexibility in system design. You can build a simple system using only a CoreModule 740, an input/output device connected to the serial or parallel ports, and an IDE storage device connected to the IDE port. To expand a simple CoreModule system, simply add self-stacking PC/104 and PC/104-Plus expansion boards to provide additional capabilities, such as:

- Additional serial and parallel ports
- Analog or high-speed digital I/O
    - Data Acquisition (Analog In/Out)
    - USB 2.0 expansion modules
    - IEEE 1394 (FireWire) expansion modules
    - Standard VGA video output

PC/104 or PC/104-Plus expansion modules can be stacked with the CoreModule 740 avoiding the need for large, expensive card cages and backplanes. The PC/104-Plus expansion modules can be mounted directly to the PC/104 and PC/104-Plus connectors of the CoreModule 740. PC/104-compliant modules can be stacked with an inter-board spacing of ~0.66 inches, so that a 3-module system fits in a 3.6" x 3.8" x 2.4" space. See Figure 2-1.

One or more MiniModule products or other PC/104 modules can be installed on the CoreModule expansion connectors, so that the expansion modules fit within the CoreModule outline dimensions. Most MiniModule products have stackthrough connectors compatible with the PC/104-Plus Version 2.0 specification. Several modules can be stacked on the CoreModule headers. Each additional module increases the thickness of the package by ~17mm (0.66"). See Figure 2-1.

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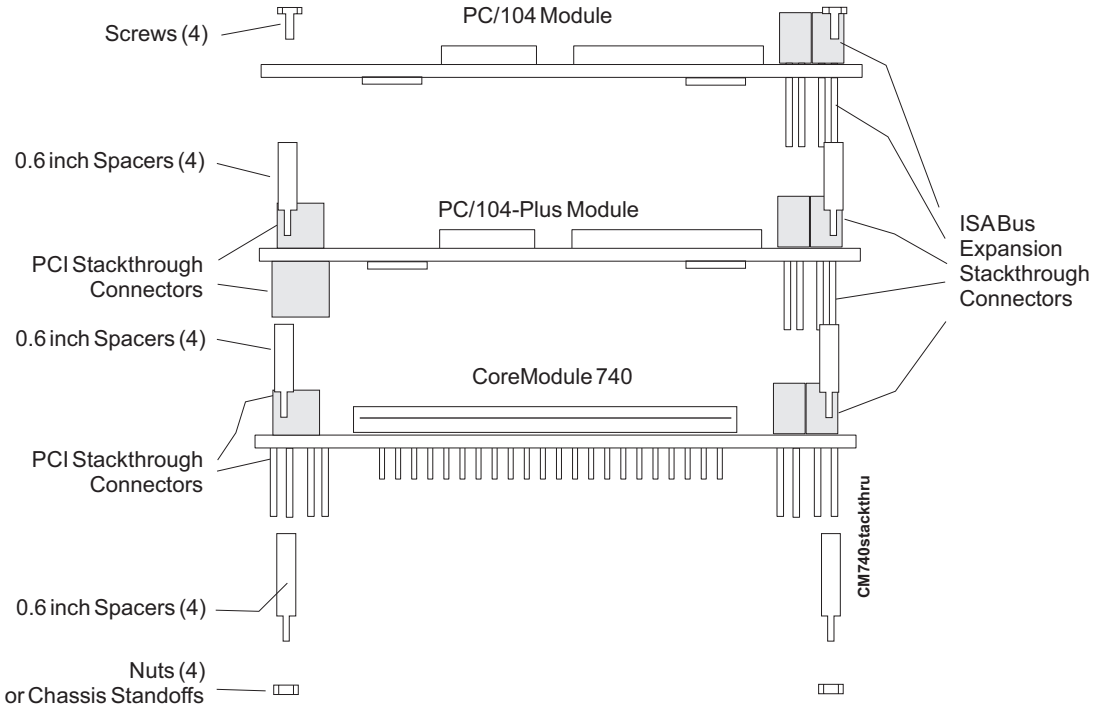


Figure 2-1. Stacking PC/104-Plus Modules with the CoreModule 740

Product Description

The CoreModule 740 SBC is an exceptionally high integration, high performance, Intel® Atom™ N450 processor based system compatible with the PC/104 standard. This rugged and high quality single-board system contains all the component subsystems of an ATX motherboard plus the equivalent of several PCI expansion boards.

The Intel Atom N400 series CPUs integrate processor cores with Graphics and Memory Hubs (GMHs), providing low-power, high-performance processors, memory controllers for up to 512MB of onboard SDRAM memory, and graphics controllers which provide LVDS and VGA signals for most LCD video panels.

The ICH8-M chipset provides controllers for the I/O Hub (Southbridge) featuring two USB ports, one Ultra DMA 33/66/100 IDE port supporting two IDE devices, and one PCI port. The CoreModule 740 provides legacy interfaces through the SMSC SCH3112I-NU Super I/O featuring two serial ports, one parallel port, PS/2 keyboard and mouse ports, and one floppy port.

The CoreModule 740 can be expanded through the PCI expansion bus using the PC/104 and PC/104-Plus connectors for additional system functions. This bus offers compact, self-stacking, modular expandability. The PC/104 bus is an embedded system version of the signal set provided on a desktop PC's ISA bus. The PC/104-Plus bus includes this signal set plus additional signals implementing a PCI bus, available on a 120-pin (4 rows of 30 pins) PCI expansion bus connector. This PCI bus operates at a clock speed of 33MHz.

The CoreModule 740 is particularly well suited to either embedded or portable applications and meets the size, power consumption, temperature range, quality, and reliability demands of embedded system applications. It can be stacked with ADLINK MiniModules™ or other PC/104-compliant expansion modules, or it can be used as a powerful computing engine. The CoreModule 740 requires a single +5V AT power source.

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Module Features

- CPU
  - Provides 166MHz Intel Atom N450 processor core
  - DMI (Direct Media Interface) with 1 GB/s of bandwidth in each direction
  - Enhanced SpeedStep® technology
  - On die 512-kB, 8-way L2 cache
- Memory
  - 512MB standard SDRAM soldered on the board
  - 667MHz Clock Speed
- Interface Buses
  - PC/104 and PC/104-Plus Interfaces
  - PC/104 bus speeds up to 8MHz (16-bit ISA Bus)
  - PC/104-Plus bus speed at 33MHz (32-bit PCI Bus)
  - PCI 2.2 compliant
- Utility Interfaces (2)
  - Provide IDE port
    - Supports two enhanced IDE devices
    - Supports single master mode
    - Supports Ultra DMA 100/66/33 in master mode
    - Supports ATAPI and DVD peripherals
    - Supports IDE native and ATA compatibility modes
  - Provide floppy drive port
    - Supports one floppy drive
    - Supports all standard PC/AT formats: 360kB, 1.2MB, 720kB, 1.44MB, 2.88MB
  - Provide PS/2 Keyboard and PS/2 Mouse ports
  - Provide parallel printer port with IEEE standard 1284 protocols, and EPP, ECP outputs
  - Provide two RS-232 serial ports with full handshaking
  - Provide two 2.0 USB ports
    - Provides one root USB hub
    - Provides two USB ports
    - Supports USB V2.0
  - Support external reset switch
  - Support standard external 8Ω speaker interface
  - Support HDD Activity LED
  - Support external battery for Real Time Clock operation

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- Video Interface (VGA/LVDS)
  - Supports VGA (1400 x 1050 bpp at 60Hz) with 32MB SMA (Shared Memory Area)
  - 18-bit flat panel outputs (LVDS)
  - Supports LVDS (1280 X 800)
- Miscellaneous
  - Battery-less boot
  - Oops! Jumper support
  - Serial Console support
  - Watchdog Timer
  - Logo Screen (Splash)

Block Diagram

Figure 2-2 shows the functional components of the module.

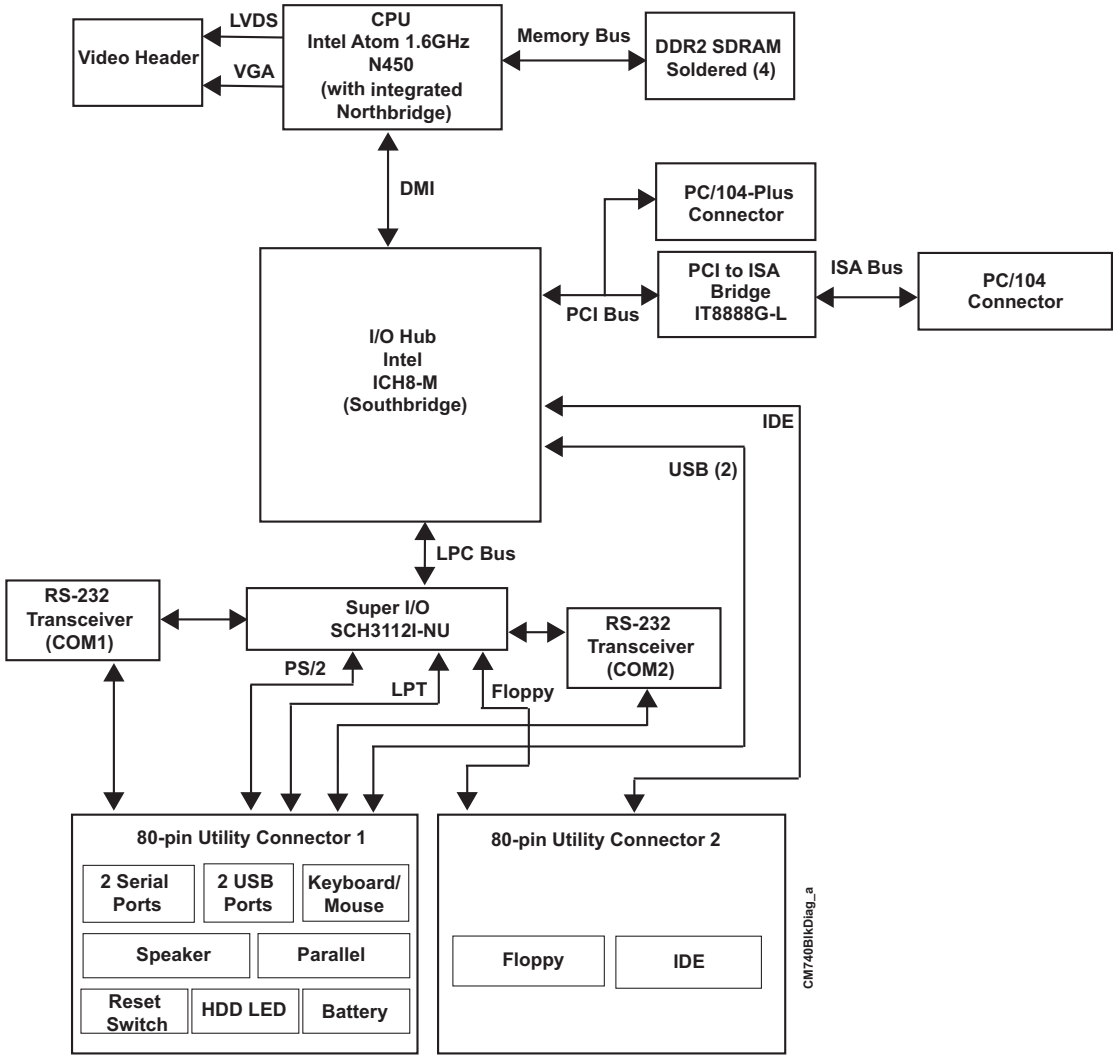


Figure 2-2. Functional Block Diagram

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Major Components (ICs)

Table 2-1 lists the major ICs, including a brief description of each, on the CoreModule 740. Figures 2-3 and 2-4 show the locations of the major ICs.

Table 2-1. Major Component Descriptions and Functions

Chip Type	Mfg.	Model	Description	Function
CPU (U1)	Intel	Atom N450	Central Processing Unit	Integrated processor core and Northbridge (memory and video)
I/O Hub (U2)	Intel	82801HBM ICH8-M	Southbridge functions (provides some of standard I/O functions)	I/O functions
PCI-to-ISA Bridge (U8 - on bottom side) [see Figure 2-4]	ITE	ITE8888G-L	PCI-to-ISA interface	ISA bus support
Super I/O Hub (U9 - on bottom side) [see Figure 2-4]	SMSC	SCH3112I-NU	Super I/O controller provides remaining standard I/O functions	I/O functions
RS-232 Transceiver (U11 - on bottom side) [see Figure 2-4]	Maxim*	MAX213ECAI+*	RS232 Transceiver for COM1	Serial Port Transceiver
RS-232 Transceiver (U12 - on bottom side) [see Figure 2-4]	Maxim*	MAX213ECAI+*	RS232 Transceiver for COM2	Serial Port Transceiver
Soldered Memory (U27)	Elpida*	EDE1116AEBG-8E-F*	SDRAM 1	128MB DDR2 memory
Soldered Memory (U28 - on bottom side) [see Figure 2-4]	Elpida*	EDE1116AEBG-8E-F*	SDRAM 2	128MB DDR2 memory
Soldered Memory (U29)	Elpida*	EDE1116AEBG-8E-F*	SDRAM 3	128MB DDR2 memory
Soldered Memory (U30) - on bottom side [see Figure 2-4]	Elpida*	EDE1116AEBG-8E-F*	SDRAM 4	128MB DDR2 memory

Note: *Subject to change in model or manufacturer.

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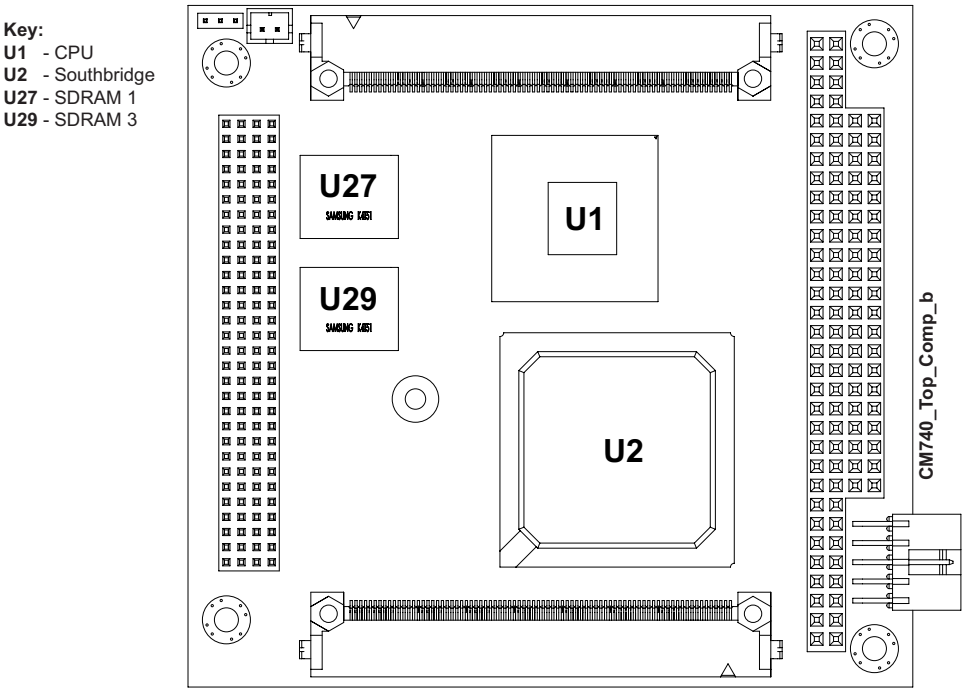


Figure 2-3. Component Locations (Top Side)

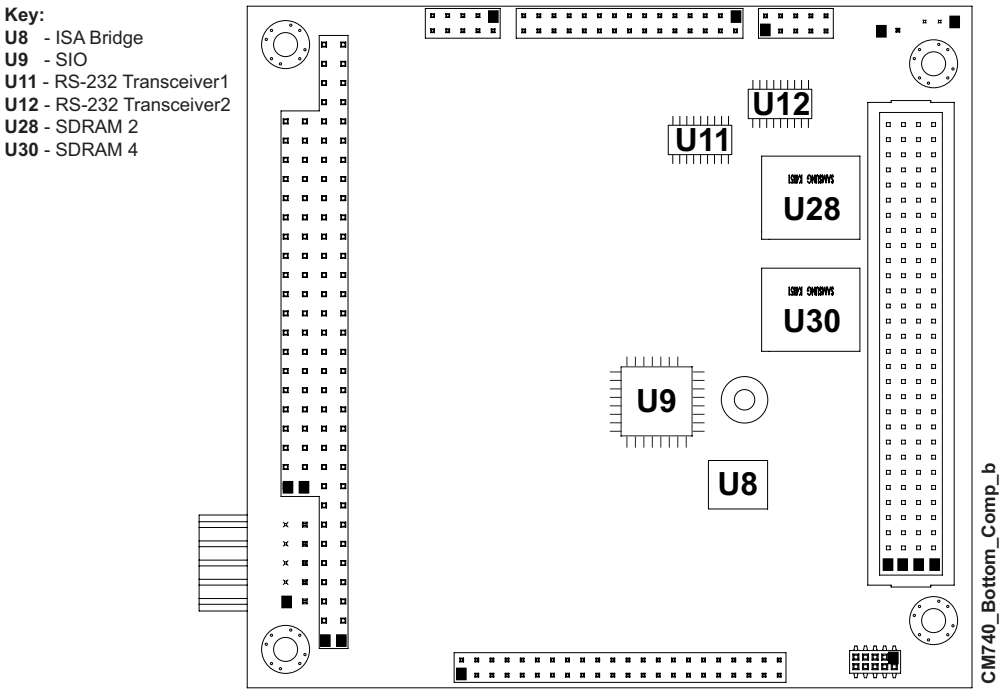


Figure 2-4. Component Locations (Bottom Side)

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Header and Connector Definitions

Table 2-2 describes the headers and connectors of the CoreModule 740 shown in Figures 2-6 and 2-7.

Table 2-2. Module Header and Connector Descriptions

Header #	Board Access	Description
J1 A, B, C, D – PC/104-Plus	Top/Bottom	120-pin, 0.079" (2mm) connector used for PC/104-Plus signals
J2 A, B, C, D – PC/104	Top/Bottom	104-pin, connector used for PC/104 signals
J4 – Utility 2	Top	80-pin, 0.025" (0.635mm) High-Density connector used for Floppy and IDE signals
J5 – Utility 1	Top	80-pin, 0.025" (0.635mm) High-Density connector used for Serial, Parallel, USB 1 & 2, Keyboard and Mouse, Speaker, Reset Switch, HDD Activity LED, and Battery
J6 – Fan	Top	2-pin, 0.079" (2mm) header used for System Fan signals
J7 – Power	Top	10-pin, 0.100" (2.54mm), right-angle, shrouded header used for external power connection
J8 – N/P	Bottom	Not Populated
J9 – N/P	Bottom	Not Populated
J10 – Video	Bottom; see Figure 2-7	30-pin, 0.079" (2mm) header used for LVDS and VGA video signals
J11 – N/P	Bottom	Not Populated
J12 – N/S	Bottom; see Figure 2-7	Not Supported

NOTE The pinout tables in Chapter 3 of this manual identify pin sequence using the following methods: A 30-pin header with two rows of pins, using odd/even numbering, where pin 2 is directly across from pin 1, is noted as 30-pin, 2 rows, odd/even (1, 2). Alternately, a 30-pin connector using consecutive numbering, where pin 11 is directly across from pin 1, is noted in this way: 30-pin, 2 rows, consecutive (1, 11). The second number in the parenthesis is always directly across from pin 1. See Figure 2-5.

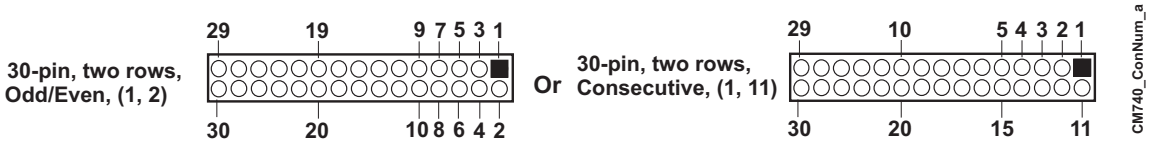


Figure 2-5. Connector Pin Identifications

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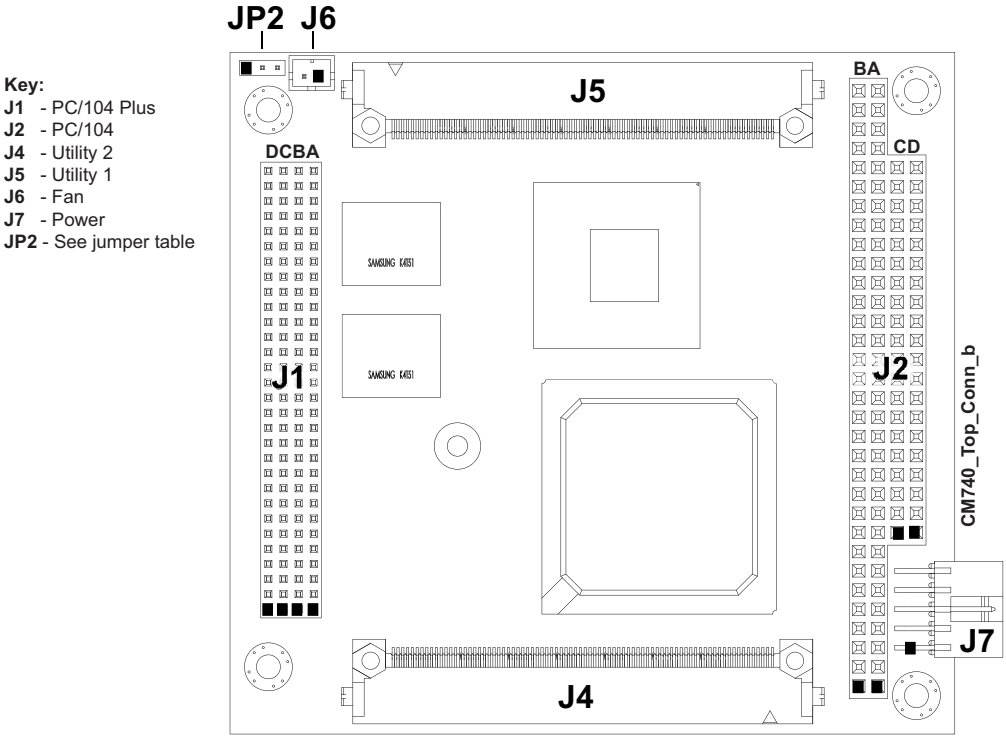


Figure 2-6. Header and Connector Locations (Top Side)

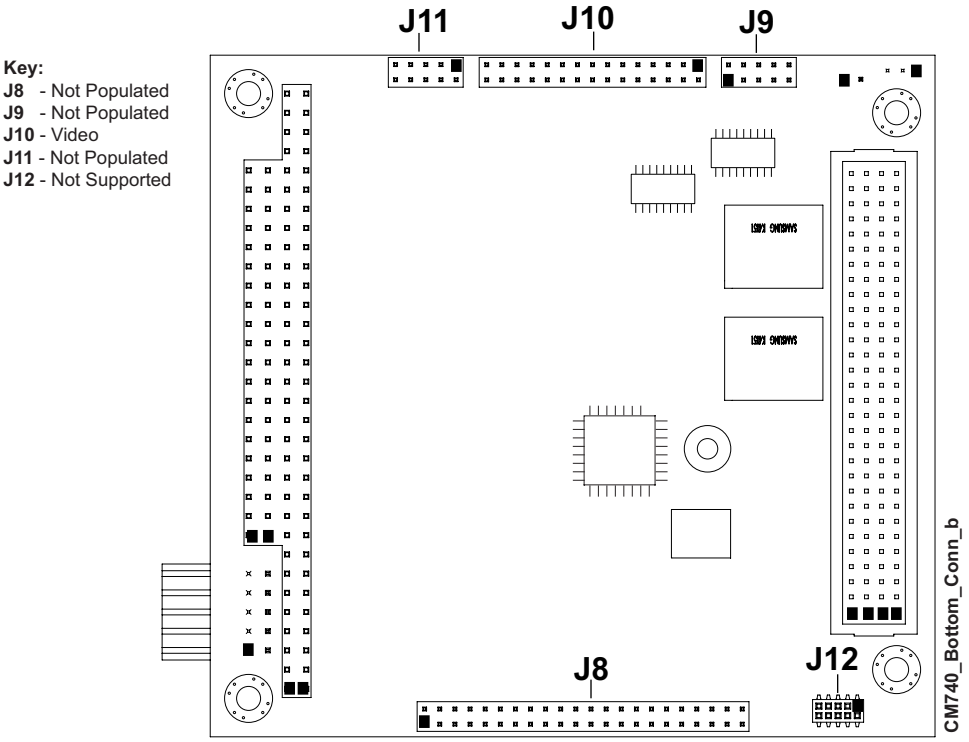


Figure 2-7. Header and Connector Locations (Bottom Side)

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Jumper Header Definition

Table 2-3 describes the jumper header shown in Figure 2-8. All jumper headers provide 0.079" (2mm) pitch.

Table 2-3. Jumper Settings

Jumper Header	Installed	Removed/Enabled
JP2 – LVDS Voltage Selection	Enable +3.3V (1-2) **(Default)**	Enable +5V (2-3)

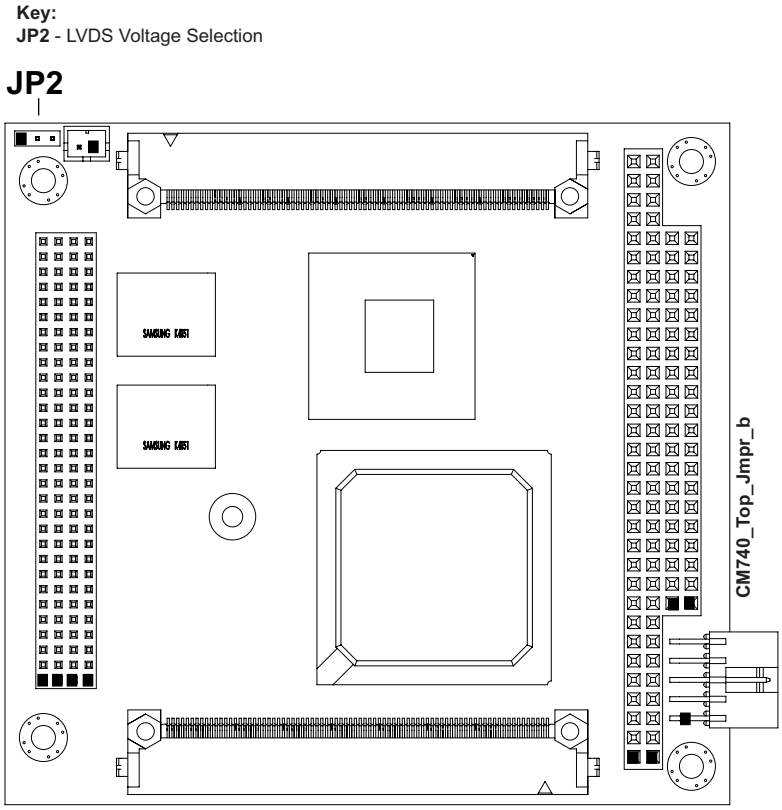


Figure 2-8. Jumper Header Locations (Top Side)

Specifications

Physical Specifications

Table 2-4 gives the physical dimensions of the module.

Table 2-4. Weight and Footprint Dimensions

Item	Dimension
Weight	0.12 kg (0.25 lbs)
Height (overall)	11.05 mm (0.435 inches)
Board thickness	2.362 mm (0.093 inches)
Width	90.169 mm (3.55 inches)
Length	95.884 mm (3.775 inches)

NOTE Overall height is measured from the upper board surface to the highest permanent component (PC/104 bus connector) on the upper board surface. This measurement does not include the heatsink, which can vary. The heatsink could increase this dimension.

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Mechanical Specifications

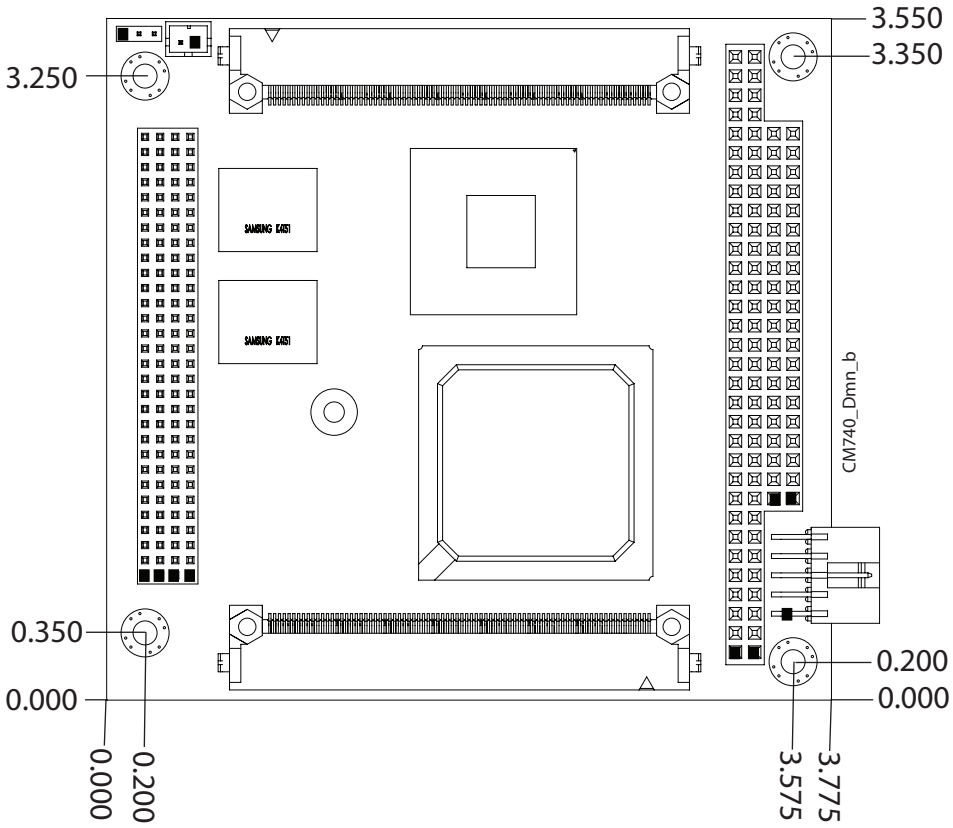


Figure 2-9. Mechanical Overview (Top Side)

NOTE	All dimensions are given in inches. Pin 1 is shown as a black square on headers and connectors. Black squares on right-angle headers indicate pin 2 in top-side views and pin 1 in bottom-side views.

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Power Specifications

Table 2-5 provides the power requirements for the CoreModule 740.

Table 2-5. Power Supply Requirements

Parameter	1.6GHz Characteristics
Input Type	Regulated DC voltage
In-rush Voltage & Current (Max)	7.16A (35.80W)
Typical Idle Voltage & Current	1.28A (6.42W)
BIT Voltage & Current	1.78A (8.92W)

Operating configurations:

- In-rush operating configuration includes Intel Atom N450 CPU, video, 512MB built-in SDRAM, and power.
- Idle operating configuration includes In-rush configuration as well as connected I/O board, one external PATA HDD (primary master), one external IDE CD-ROM (Primary Slave), one external floppy drive, one PS/2 keyboard, and one PS/2 mouse.
- BIT (Burn-In-Test) operating configuration includes Idle configuration as well as one USB Compact Flash reader with 64MB Compact Flash, one USB flash thumb drive, one LPT loop back, and two serial loop backs.

Environmental Specifications

Table 2-6 provides the most efficient operating and storage condition ranges required for this module.

Table 2-6. Environmental Requirements

Parameter	Conditions
Temperature	
Operating	–20 to +70 C (–4 to +158 F)
Extended (Optional)	–40 to +85 C (–40 to +185 F)
Storage	–55 to +85 C (–67 to +185 F)
Humidity	
Operating	5% to 90% relative humidity, non-condensing
Non-operating	5% to 95% relative humidity, non-condensing

Thermal/Cooling Requirements

The CPU is the primary source of heat on the board. The CoreModule 740 is designed to operate at the maximum speed of the CPU and requires a heatsink (provided).

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Chapter 3 Hardware

Overview

This chapter discusses the chips and connectors of the module features in the following order:

- Memory Map
- Interrupt Channel Assignments
- I/O Address Map
- Utility 1 Interface
  - Serial 1 & 2 Interfaces
  - Parallel Interface
  - USB 1 & 2 Interfaces
  - Mouse
  - Keyboard
  - Speaker
  - Reset Switch
  - HDD Activity LED
  - Battery
- Utility 2 Interface
  - Floppy Interface
  - IDE Signals
- Video Interface
  - VGA
  - LVDS
- System Fan
- Power Interface
- Miscellaneous
  - Time of Day/RTC
  - Oops! Jumper
  - Serial Console
  - Watchdog Timer

NOTE ADLINK Technology, Inc. supports only the features/options tested and listed in this manual. The main chips used in the CoreModule 740 may provide more features or options than are listed for the CoreModule 740, but some of these features/options are not supported on the module and will not function as specified in the chip documentation.

The pinout tables only of non-standard headers and connectors are included in this chapter. This chapter does not include pinout tables for standard headers and connectors such as PC/104 and PC/104-Plus.

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Interrupt Channel Assignments

The interrupt channel assignments are shown in Table 3-1.

Table 3-1. Interrupt Channel Assignments

Device vs IRQ No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timer	X															
Keyboard		X														
Secondary Cascade			X													
COM1				O	D											
COM2				D	O											
Floppy							D									
Parallel						O		D								
RTC									X							
IDE															D	
Math Coprocessor														X		
PS/2 Mouse													X			
PCI INTA	Automatically Assigned															
PCI INTB	Automatically Assigned															
PCI INTC	Automatically Assigned															
PCI INTD	Automatically Assigned															
USB	Automatically Assigned															
Video	Automatically Assigned															

Legend: D = Default, O = Optional, X = Fixed

NOTE The IRQs for USB and Video are automatically assigned by the BIOS Plug and Play logic. Local IRQs assigned during initialization can not be used by external devices.

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Memory Map

The following table provides the common PC/AT memory allocations. These are DOS-level addresses. The OS typically hides these physical addresses by way of memory management. Memory below 000500h is used by the BIOS.

Table 3-2. Memory Map

Base Address			Function
00000000h	-	0009FFFFh	Conventional Memory
000A0000h	-	000AFFFFh	Graphics Memory
000B0000h	-	000B7FFFh	Mono Text Memory
000B8000h	-	000BFFFFh	Color Text Memory
000C0000h	-	000CFFFFh	Standard Video BIOS
000D0000h	-	000DFFFFh	Reserved for Extended BIOS
000E0000h	-	000EFFFFh	Extended System BIOS Area
000F0000h	-	000FFFFFh	System BIOS Area (Storage and RAM Shadowing)
00100000h	-	04000000h	Extended Memory (If onboard VGA is enabled, then the amount of memory assigned is subtracted from extended memory.)
FFF80000h	-	FFFFFFFFh	System Flash

I/O Address Map

Table 3-3 shows the I/O address map. These are DOS-level addresses. The OS typically hides these physical addresses by way of memory management.

Table 3-3. I/O Address Map

Address (hex)	Subsystem
0000-000F	Primary DMA Controller
0020-0021	Master Interrupt Controller
0040-0043	Programmable Interrupt Timer (Clock/Timer)
0060	Keyboard Controller
0061	NMI, Speaker Control
0063	NMI Controller
0064	Keyboard Controller
0065	NMI Controller
0067	NMI Controller
0070-007F	CMOS RAM, NMI Mask Reg, RT Clock
0080	System reserved
0081-0083	DMA Page Registers
0084-0086	System reserved
0087	DMA Page Register
0088	System reserved
0089-008B	DMA Page Registers
008C-008E	System reserved
008F	DMA Page Register

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Table 3-3. I/O Address Map (Continued)

0090-0091	System reserved
0092	Fast A20 gate and CPU reset
0093-009F	System reserved
00A0-00A1	Slave Interrupt Controller
00A2-00BF	System reserved
00C0-00DF	Slave DMA Controller #2
00E0-00EF	System reserved
00F0-00FF	Math Coprocessor
01F0-01F7	IDE Hard Disk Controller
0200-0240h	Mapped to ISA
0240-0260h	Mapped to ISA
0279h	Mapped to ISA
02F8-02FF	Serial Port 2 (COM2)
0300-0340h	Mapped to ISA
0340-0360h	Mapped to ISA
0378-037F	Parallel Port (Standard and EPP)
03B0-03BB	Video (monochrome)
03C0-03DF	Video (VGA)
03F0-03F5	Floppy Disk Controller
03F6	IDE Hard Disk Controller
03F7	Floppy Disk Controller
03F8-03FF	Serial Port 1 (COM1)
04D0-04D1	Edge/Level Trigger PIC
0778-077F	Parallel Port (ECP Extensions) (Port 378+400)
0A79h	Mapped to ISA
0CF8-0CFF	PCI Configuration Registers
0CF9	Reset Control Register

NOTE 0279h and 0A79h are the ISA PnP ports used by the BIOS and an OS that supports this feature to recognize ISA PnP (Plug and Play) cards.

The Intel I/O hub ICH-8 (ICH-6 or later) does not support ISA DMA.

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Utility 1 Interface

The CoreModule 740 provides two utility interface connectors. Both interfaces, Utility 1 (J5) and Utility 2 (J4), use identical 80-pin connectors. This section describes the Utility 1, J5 interface, which supports the features listed in the following bullets. Table 3-8 provides a complete list of the Utility 1 connector interface signals. Tables 3-4 through 3-7 provide simplified pin signal descriptions of each specific interface on the Utility 1 connector.

- Serial interface
- Parallel interface
- USB interface
- Mouse and Keyboard interfaces
- Speaker interface
- Reset Switch interface
- HDD Activity LED interface
- Battery interface

Serial Interface

The two serial port signals are provided through the 80-pin Utility 1 connector (J5) and support the following features:

- Both ports are 16550 compatible
- Programmable word length, stop bits and parity
- 16-bit programmable baud rate and Interrupt generator
- Loop-back mode
- Two 16-bit FIFOs and two DMA handshake lines
- Serial 1 and 2 (COM 1 and COM 2) support RS-232

Table 3-4. Simplified Serial Interface (Ports 1 & 2) Pin Signal Descriptions (J5)

J5 Pin #	Signal	DB25 Pin #	DB9 Pin #	Description
1	DCD1*	8	1	Data Carrier Detect 1 – Indicates external modem is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR1 as part of the DTR1/DSR1 handshake.
3	DSR1*	6	6	Data Set Ready 1 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR1 for overall readiness to communicate.
5	RXD1	3	2	Serial Port Receive Data 1 Input – This line is typically held at a logic 1 (mark) when no data is being transmitted, and is held “Off” for a brief interval after an “On” to “Off” transition on the RTS1 line to allow the transmission to complete.
7	RTS1*	4	7	Request To Send 1 – Indicates serial port is ready to transmit data. Used as hardware handshake with CTS1 for low level flow control.

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Table 3-4. Simplified Serial Interface (Ports 1 & 2) Pin Signal Descriptions (J5) (Continued)

J5 Pin #	Signal	DB25 Pin #	DB9 Pin #	Description
9	TXD1	2	3	Serial Port Transmit Data 1 Output – This line is typically held to a logic 1 when no data is being sent. Typically, a logic 0 (On) must be present on RTS1, CTS1, DSR1, and DTR1 before data can be transmitted on this line.
11	CTS1*	5	8	Clear To Send 1 – Indicates external serial communication device is ready to receive data. Used as hardware handshake with RTS1 for low level flow control.
13	DTR1*	20	4	Data Terminal Ready 1 – Indicates port is powered, initialized, and ready. Used as hardware handshake with DSR1 for overall readiness to communicate.
15	RI1*	22	9	Ring Indicator 1 – Indicates external modem is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
17	GND	7	5	Digital Ground
19	NC	NC	NC	Not Connected
21	DCD2*	8	1	Data Carrier Detect 2 – Indicates external modem is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR2 as part of the DTR2/DSR2 handshake.
23	DSR2*	6	6	Data Set Ready 2 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR2 for overall readiness to communicate.
25	RXD2	3	2	Serial Port Receive Data 2 Input – This line is typically held at a logic 1 (mark) when no data is being transmitted, and is held “Off” for a brief interval after an “On” to “Off” transition on the RTS2 line to allow the transmission to complete.
27	RTS2*	4	7	Request To Send 2 – Indicates serial port is ready to transmit data. Used as hardware handshake with CTS2 for low level flow control.
29	TXD2	2	3	Serial Port Transmit Data 2 Output – This line is typically held to a logic 1 when no data is being sent. Typically, a logic 0 (On) must be present on RTS2, CTS2, DSR2, and DTR2 before transmitting data on this line.
31	CTS2*	5	8	Clear To Send 2 – Indicates external serial communication device is ready to receive data. Used as hardware handshake with RTS2 for low level flow control.
33	DTR2*	20	4	Data Terminal Ready 2 – Indicates port is powered, initialized, and ready. Used as hardware handshake with DSR2 for overall readiness to communicate.
35	RI2*	22	9	Ring Indicator 2 – Indicates external modem is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
37	GND	7	5	Digital Ground
39	TXD2_ TTL	NC	NC	Serial Transmit Data 2 – Serial port 2 TTL transmit data output signal (jumpered to pin 3 DB9 connector on I/O Board).

Note: The shaded table cells denote power or ground. The * symbol indicates the signal is Active Low.

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Parallel Interface

The parallel port interface supports standard parallel, Bi-directional, ECP and EPP protocols. The Super I/O chip (SCH3112I-NU) provides the parallel port interface signals to support Standard Printer Port (SPP), Enhanced Parallel Port (EPP), and Enhanced Capabilities Port (ECP) protocols.

Table 3-5. Simplified Parallel Interface (SPP) Pin Signal Descriptions (J5)

J5 Pin #	Signal	DB25 Pin #	Description
2	Strobe*	1	Strobe* – This output signal is used to strobe data into the printer. I/O pin in ECP/EPP mode.
6	PD0	2	Parallel Port Data 0 – This pin (0 to 7) provides a parallel port data signal and is the LSB of printer data.
10	PD1	3	Parallel Port Data 1 – Refer to pin 6 (J5) for more information.
14	PD2	4	Parallel Port Data 2 – Refer to pin 6 (J5) for more information.
18	PD3	5	Parallel Port Data 3 – Refer to pin 6 (J5) for more information.
22	PD4	6	Parallel Port Data 4 – Refer to pin 6 (J5) for more information.
26	PD5	7	Parallel Port Data 5 – Refer to pin 6 (J5) for more information.
30	PD6	8	Parallel Port Data 6 – Refer to pin 6 (J5) for more information.
34	PD7	9	Parallel Port Data 7 – This pin (0 to 7) provides a parallel port data signal and is the MSB of printer data.
38	ACK*	10	Acknowledge * – This is a status input signal from the printer. A Low State indicates it has received the data and is ready to accept new data.
42	BUSY	11	Busy – This is a status input signal from the printer. A high state indicates the printer is not ready to accept data.
46	PE	12	Paper End – This is a status input signal from the printer. A high state indicates it is out of paper.
50	SLCT	13	Select – This is a status output signal from the printer. A high state indicates it is selected and powered on.
4	AFD*	14	Auto Feed * – This is a output signal from the printer to automatically feed one line after each line is printed.
8	ERR*	15	Error – This is a status output signal from the printer. A low state indicates an error condition on the printer.
12	INIT*	16	Initialize * – This signal initializes the printer. Output in standard mode, I/O in ECP/EPP mode.
16	SLCTIN	17	Select In – This output signal is used to select the printer. I/O pin in ECP/EPP mode.
20, 24, 28, 32, 36, 40, 44, 48	GND	18-25	Digital Ground

Note: The shaded table cells denote power or ground. The * symbol indicates the signal is Active Low.

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USB Interface

The CoreModule 740 supports one root USB (Universal Serial Bus) hub and two functional USB ports (USB1 and USB2 on J5).

Features implemented in the USB port include the following:

- USB v2.0 and legacy v1.1 compatible
- Integrated physical layer transceivers
- Over current detection status on both USB ports (I/O Hub function)
- No over current fuses located on the CoreModule 740

Table 3-6. Simplified USB Interface Pin Signal Descriptions (J5)

J5 Pin #	Signal	Description
41	USBOC0	USB Port 0 Over Current Protection – Port is disabled if this input is low. Direct inputs are provided for over current protection.
43	USBPWR0	USB Port 0 power
45	USBPN	Universal Serial Bus Port 0 Data Negative Polarity
47	USBPP	Universal Serial Bus Port 0 Data Positive Polarity
49	GND	USB Port ground
51	USBOC1	USB Port 1 Over Current Protection – Port is disabled if this input is low. Direct inputs are provided for over current protection.
53	USBPWR1	USB Port 0 power
55	USBPN	Universal Serial Bus Port 1 Data Negative Polarity
57	USBPP	Universal Serial Bus Port 1 Data Positive Polarity
59	GND	USB Port ground

Note: The shaded table cells denote power or ground.

Keyboard and Mouse Interfaces

The signal lines for a PS/2 keyboard and mouse are provided through the Utility 1 interface (J5).

Speaker

The speaker signal provides sufficient signal strength to drive a 1W 8 Ω “Beep” speaker through the Utility interface at an audible level. The speaker signal is driven from an on-board amplifier and the ICH8-M.

Reset Switch

The Utility 1 header provides the signal for an external reset button, which allows the user to re-boot the system.

HDD Activity LED

This indicator signal is fed to pin 69 of the Utility 1 connector to allow for an external LED to indicate IDE activity.

Battery Interface

An external battery input connection is provided through the Utility 1 interface to provide an external battery for the CMOS RAM and the RTC (Real Time Clock).

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Table 3-7. Simplified Keyboard, Mouse, and Miscellaneous Interface Pin Signal Descriptions (J5)

J5 Pin #	Signal	Description
61	MOU Data	Mouse Data
63	MOU Clk	Mouse Clock
65	GND	Ground
67	MOU Pwr	Mouse Power (+5V)
62	SPKR+	Speaker + Output
64	GND	Ground
66	RESET SW	Reset Switch
68	KBD SW	Keyboard switch – Not used
70	KBD Data	Keyboard Data
72	KBD Clk	Keyboard Clock
74	GND	Digital Ground
76	KBD PWR	Keyboard power (+5V)
78	BATV+	External Backup Battery +
80	BATV-	External Backup Battery Return -

Note: The shaded table cells denote power or ground.

Utility 1 Pin Signals

Table 3-8 lists the signals and their descriptions for the Utility 1 interface which provides a right-angle, 80-pin connector with 0.025" (0.635mm) pin pitch.

Table 3-8. Complete Utility 1 Interface Pin Signals (J5)

Pin #	Signal	Description
1	DCD1*	Serial Data Carrier Detect 1 – Indicates external serial device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this is driven by DTR1 as part of the DTR/DSR handshake.
2	PP_ STRB*	Parallel Port Strobe – This is an output signal used to strobe data into the printer. I/O pin in ECP/EPP mode.
3	DSR1*	Serial Data Set Ready 1 – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR1 for overall readiness.
4	PP_AFD*	Parallel Auto Feed – This is a request signal into the printer to automatically feed one line after each line is printed.
5	RXD1	Serial Receive Data 1– Serial port 1 receive data in.
6	PD0	Parallel Data 0 – This signal provides parallel data to the printer.
7	RTS1*	Serial Request To Send 1 – Indicates port is ready to transmit data. Used as hardware handshake with CTS1 for low level flow control.
8	PP_ERR*	Parallel Error – This is a status output signal from the printer. A Low State indicates an error condition on the printer.
9	TXD1	Serial Transmit Data 1 – Serial port 1 transmit data out.
10	PD1	Parallel Data 1 – This signal provides parallel data to the printer.
11	CTS1*	Serial Clear To Send 1 – Indicates external serial device is ready to receive data. Used as hardware handshake with RTS1 for low level flow control.

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Table 3-8. Complete Utility 1 Interface Pin Signals (J5) (Continued)

12	PP_INIT*	Parallel Initialize – This signal is used to initialize printer. Output in standard mode, I/O in ECP/EPP mode.
13	DTR1*	Serial Data Terminal Ready 1 – Indicates port is powered, initialized, and ready. Used as hardware handshake with DSR1 for overall readiness to communicate.
14	PD2	Parallel Port Data 2 – This signal provides parallel data to the printer.
15	RI1*	Serial Ring Indicator 1 – Indicates external modem is detecting a ring condition. Software initiates operation to answer and open communication channel.
16	PP_SLIN*	Parallel Select In – This output signal is used to select the printer. I/O pin in ECP/EPP mode.
17	GND1	Ground 1 (Serial)
18	PD3	Parallel Data 3 – This signal provides parallel data to the printer.
19	NC	Not Connected
20	GND2	Ground 2 (Parallel)
21	DCD2*	Serial Data Carrier Detect 2 – Indicates external serial device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this is driven by DTR2 as part of the DTR2/DSR2 handshake.
22	PD4	Parallel Data 4 – This signal provides parallel data to the printer.
23	DSR2*	Serial Data Set Ready 2 – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR2 for overall readiness.
24	GND3	Ground 3 (Parallel)
25	RXD2	Serial Receive Data 2 – Serial port 2 receive data in.
26	PD5	Parallel Data 5 – This signal provides parallel data to the printer.
27	RTS2*	Serial Request To Send 2 – Indicates port is ready to transmit data. Used as hardware handshake with CTS2 for low level flow control.
28	GND4	Ground 4 (Parallel)
29	TXD2	Serial Transmit Data 2 – Serial port 2 transmit data out.
30	PD6	Parallel Port Data 6 – This signal provides parallel data to the printer.
31	CTS2*	Serial Clear To Send 2 – Indicates external serial device is ready to receive data. Used as hardware handshake with RTS2 for low level flow control.
32	GND5	Ground 5 (Parallel)
33	DTR2*	Serial Data Terminal Ready 2 – Indicates port is powered, initialized, and ready. Used as hardware handshake with DSR2 for overall readiness to communicate.
34	PD7	Parallel Port Data 7 – This signal provides parallel data to the printer.
35	RI2*	Serial Ring Indicator 2 – Indicates external serial device is detecting a ring condition. Software initiates operation to answer and open communication channel.
36	GND6	Ground 6 (Parallel)
37	GND7	Ground 7 (Serial)
38	PP_ACK*	Parallel Acknowledge – This is a status output signal from the printer. A low state indicates it has received the data and is ready to accept new data.
39	TXD2_TTL	Serial Transmit Data 2 – Serial port 2 TTL transmit data output signal, jumpered to pin-3 on DB9 connector on I/O Interface Board.
40	GND8	Ground 8 (Parallel)

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Table 3-8. Complete Utility 1 Interface Pin Signals (J5) (Continued)

41	USB_OC0*	USB 0 Over Current Protection – Port is disabled if this input is low. Direct inputs are provided for over current protection.
42	PP_BUSY	Parallel Printer Busy – This is a status output signal from the printer. A high state indicates the printer is not ready to accept data.
43	USBPwr0	+5 volts +/-5% (USB0 Power)
44	GND9	Ground 9 (Parallel)
45	USBP0-	USB Port 0 Negative Polarity
46	PP_PE	Parallel Paper End – This is a status output signal from the printer. A high state indicates it is out of paper.
47	USBP0+	USB Port 0 Positive Polarity
48	GND10	Ground 10 (USB)
49	GND11	Ground 11 (USB)
50	PP_SLCT	Parallel Select – This is a status output signal from the printer. A high state indicates it is selected and powered on.
51	USB_OC1*	USB 1 Over Current Protection – Port is disabled if this input is low. Direct inputs are provided for over current protection.
52	FIRMode	IR Function Mode Select – Tied to ground through 10k ohm resistor.
53	USBPwr1	+5 volts +/-5% (USB1 Power)
54	NC	Not Connected
55	USBP1-	USB Port 1 Negative Polarity
56	GND12	Ground 12 (USB)
57	USBP1+	USB Port 1 Positive Polarity
58	IRTX	Not Connected
59	GND 13	Ground 13 (USB)
60	IRRX	Not Connected
61	MDATA	Mouse Data
62	SPKR	Speaker – Signal for external PC “Beep” speaker.
63	MSCK	Mouse Clock
64	GND14	Ground 14 (Mouse)
65	GND15	Ground 15 (Mouse)
66	ResetSW	Reset Switch – Accepts external reset signal (momentarily grounding this pin.)
67	MSPwr	+5 volts +/-5% (Mouse Power)
68	KBSW	Not Connected
69	HDACT	IDE Hard Drive Active – Signal for external HDD activity LED.
70	KBDT	Keyboard Data
71	ExtSMI	Not Connected
72	KBCK	Keyboard Clock
73	NC	Not Connected
74	GND16	Ground 16 (Keyboard)
75	NC	Not Connected
76	KBPwr	Keyboard Power
77	NC	Not Connected -12V

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Table 3-8. Complete Utility 1 Interface Pin Signals (J5) (Continued)

78	BATV+	External Backup Battery Positive – External positive battery terminal.
79	NC	Not Connected -5V
80	BATV-	External Backup Battery Negative – External battery ground.

Note: The shaded table cells denote power or ground. The * symbol indicates the signal is Active Low.

Utility 2 Interface

This section describes the Utility 2, J4 interface, which supports the features in the following bullets. Table 3-11 provides a complete list of the Utility 2 connector pin signals. Tables 3-9 through 3-10 provide simplified pin signal descriptions of each specific interface on the Utility 2 connector.

- Floppy Drive Interface
- IDE Interface

Floppy Drive Interface

The Super I/O chip (SCH3112I-NU) provides the floppy controller and supports one floppy drive.

Table 3-9. Simplified Floppy Drive Interface Pin Signal Descriptions (J4)

J4 Pin #	Signal	Floppy Cable	Description
3	DRVEN0*	2	Drive (Floppy) Density Select 0 – This signal indicates a low (250/300 kbps) or high (500 kbps) data rate has been selected.
54	NC	4	Not connected
11	KEY	6	Key – Not connected
15	INDEX*	8	Index –Detects when the head is positioned over the beginning of track 0.
19	MTR0*	10	Motor Control 0 – Select motor on drive 0
23	NP	12	Not Provided (Drive Select 1)
27	DS0*	14	Drive Select 0 – Select drive 0
31	NP	16	Not Provided (Motor Control 1)
35	DIR*	18	Direction – Direction of head movement (0 = inward motion, 1 = outward motion).
39	STEP*	20	Step – Low pulse for each track-to-track movement of the head.
43	WDATA*	22	Write Data – Encoded data to the drive for write operations.
47	WGATE*	24	Write Gate – Signal to the drive to enable current flow in the write head.
51	TRK0*	26	Track 0 – Detects when head is positioned over track 0.

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Table 3-9. Simplified Floppy Drive Interface Pin Signal Descriptions (J4) (Continued)

J4 Pin #	Signal	Floppy Cable	Description
55	WRTPRT*	28	Write Protect – Senses when diskette is write protected.
59	RDATA*	30	Read Data – Raw serial bit stream from the drive for read operations.
63	HDSEL*	32	Head Select – Selects the side for Read/Write operations (0 = side 1, 1 = side 0)
67	DSKCHG*	34	Disk Change – Senses the drive door is open or the diskette has been changed since the last drive selection.
1, 5, 9, 13, 17, 21, 25, 29, 33, 37, 41, 45, 49, 53, 57, 61, 65	GND	1-33 (all odd)	Digital Ground

Note: The shaded table cells denote power or ground. The * symbol indicates the signal is Active Low.

IDE Interface

The ICH8-M I/O Hub (82801HBM) provides the IDE controller and supports two IDE drives.

Table 3-10. Simplified IDE Interface Pin Signal Descriptions (J4)

J4 Pin #	Signal	IDE Cable	Description
2	HD_RST*	1	Reset – Low active hardware reset
6	IDE_PDD7	3	Primary Disk Data 7
8	IDE_PDD8	4	Primary Disk Data 8
10	IDE_PDD6	5	Primary Disk Data 6
12	IDE_PDD9	6	Primary Disk Data 9
14	IDE_PDD5	7	Primary Disk Data 5
16	IDE_PDD10	8	Primary Disk Data 10
18	IDE_PDD4	9	Primary Disk Data 4
20	IDE_PDD11	10	Primary Disk Data 11
22	IDE_PDD3	11	Primary Disk Data 3
24	IDE_PDD12	12	Primary Disk Data 12
26	IDE_PDD2	13	Primary Disk Data 2
28	IDE_PDD13	14	Primary Disk Data 13

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Table 3-10. Simplified IDE Interface Pin Signal Descriptions (J4) (Continued)

J4 Pin #	Signal	IDE Cable	Description
30	IDE_PDD1	15	Primary Disk Data 1
32	IDE_PDD14	16	Primary Disk Data 14
34	IDE_PDD0	17	Primary Disk Data 0
36	IDE_PDD15	18	Primary Disk Data 15
40	NC	20	Not Connected (HD_Key)
42	IDE_DRQ	21	Primary Disk DMA Request
46	IDE_IOW*	23	Primary Disk Write Strobe
50	IDE_IOR*	25	Primary Disk Read Strobe
54	IDE_IORDY	27	Primary Disk I/O DMA Channel Ready
56	IDE_ALE	28	Address Latch Enable
58	IDE_DAK	29	Primary Disk DMA Channel Acknowledge
62	IDE_IRQ14	31	Primary Disk Interrupt Request 14
64	IDE_IOCS16*	32	I/O Chip Select 16
66	IDE_PDA1	33	Primary Disk Address 1
68	IDE_CABLID	34	Cable ID
70	IDE_PDA0	35	Primary Disk Address 0
72	IDE_PDA2	36	Primary Disk Address 2
74	IDE_PDCS0*	37	Primary Disk Chip Select Drive 0
76	IDE_PDCS1*	39	Primary Disk Chip Select Drive 1
4, 38, 44, 48, 52, 60, 80	GND	2, 19, 22, 24, 26, 30, 40	Digital Ground

Note: The shaded table cells denote power or ground. The * symbol indicates the signal is Active Low.

Utility 2 Pin Signals

Table 3-11 lists the signals and their descriptions for the Utility 2 interface which provides a right-angle, 80-pin connector with 0.025" (0.635mm) pin pitch.

Table 3-11. Complete Utility 2 Interface Pin Signals (J4)

Pin #	Signal	Description
1	GND8	Floppy Ground
2	HD_RST*	Reset – Low active hardware reset
3	FDD_DEN	Floppy Density Select
4	GND3	IDE Ground
5	GND9	Floppy Ground
6	IDE_PDD7	Primary Disk Data 7
7	NC	Not Connected
8	IDE_PDD8	Primary Disk Data 8
9	GND10	Floppy Ground

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Table 3-11. Complete Utility 2 Interface Pin Signals (J4) (Continued)

10	IDE_PDD6	Primary Disk Data 6
11	FPY_KEY	Not Connected
12	IDE_PDD9	Primary Disk Data 9
13	GND11	Floppy Ground
14	IDE_PDD5	Primary Disk Data 5
15	FDD_INDX*	Floppy Index – Detects the drive head is positioned over the track 0
16	IDE_PDD10	Primary Disk Data 10
17	GND12	Floppy Ground
18	IDE_PDD4	Primary Disk Data 4
19	FDD_MTR0	Floppy Motor Control 0 – Selects drive motor 0
20	IDE_PDD11	Primary Disk Data 11
21	GND13	Floppy Ground
22	IDE_PDD3	Primary Disk Data 3
23	NC	Not Connected
24	IDE_PDD12	Primary Disk Data 12
25	GND14	Floppy Ground
26	IDE_PDD2	Primary Disk Data 2
27	FDD_DS0	Floppy Drive Select 0 – Selects drive 0
28	IDE_PDD13	Primary Disk Data 13
29	GND15	Floppy Ground
30	IDE_PDD1	Primary Disk Data 1
31	NC	Not Connected
32	IDE_PDD14	Primary Disk Data 14
33	GND16	Floppy Ground
34	IDE_PDD0	Primary Disk Data 0
35	FDD_DIR*	Floppy Direction – Direction of head movement (0 = inward motion, 1 = outward motion)
36	IDE_PDD15	Primary Disk Data 15
37	GND17	Floppy Ground
38	GND1	IDE Ground
39	FDD_STEP*	Floppy Step – Low pulse for each track-to-track movement of the head
40	HD_KEY	Not Connected
41	GND18	Floppy Ground
42	IDE_PDDREQ	Primary DMA Channel Request – Used for DMA transfers between host and drive (direction of transfer controlled by PIOR* and PIOW*). Used in asynchronous mode with PDACK*. Drive asserts PDREQ when ready to transfer or receive data.
43	FDD_WDATA	Floppy Write Data – Encoded data to the drive for write operations
44	GND2	IDE Ground
45	GND19	Floppy Ground

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Table 3-11. Complete Utility 2 Interface Pin Signals (J4) (Continued)

46	IDE_PDIOW*	Primary I/O Write Strobe – Strobe signal for write functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
47	FDD_WGATE*	Floppy Write Gate – Signal to the drive to enable current flow in the write head
48	GND7	IDE Ground
49	GND20	Floppy Ground
50	IDE_PDIOR*	Primary I/O Read Strobe – Strobe signal for read functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
51	FDD_TRK0*	Floppy Track 0 – Senses the head is positioned over track 0
52	GND6	IDE Ground
53	GND21	Floppy Ground
54	IDE_PDIORDY	Primary I/O DMA Channel Ready – When negated extends the host transfer cycle of any host register access when the drive is not ready to respond to a data transfer request. High impedance if asserted.
55	FDD_WPRT*	Floppy Write Protect – Senses the diskette is write protected
56	ALE	Address Latch Enable – This signal is used to latch the LA23 to LA17 signals or decodes of these signals. Addresses are latched on the falling edge of BALE. It is forced high during DMA cycles. When used with AENx, it indicates a valid processor or DMA address.
57	GND22	Floppy Ground
58	IDE_PDDACK*	Primary DMA Channel Acknowledge – Used by the host to acknowledge data has been accepted or data is available. Used in response to PDREQ asserted.
59	FDD_DATA*	Floppy Read Data – Raw serial bit stream from the drive for read operations
60	GND4	IDE Ground
61	GND23	Floppy Ground
62	IDE_IRQ14	Primary Interrupt Request 14 – Asserted by drive when it has a pending interrupt (PIO transfer of data to or from the drive to host.)
63	FDD_HDSEL*	Floppy Head Select – Selects the side for Read/Write operations (0 = side 1, 1 = side 0)
64	IOCS16*	I/O Chip Select 16 – This signal is driven low by an I/O slave device to indicate it is capable of performing a 16-bit I/O data transfer. This signal is driven from a decode of the SA15 to SA0 address lines.
65	GND24	Floppy Ground
66	IDE_PDA1	Primary Disk Address 1 – Used to indicate which byte in the ATA command block or control block is being accessed
67	FDD_DSKCHG*	Floppy Disk Change – Senses the drive door is open or the diskette has been changed since the last drive selection
68	IDE_CABLID	Cable ID – Used for slave and master negotiation and for 40 and 80 pin IDE cable selection
69	NC	Not Connected
70	IDE_PDA0	Primary Disk Address 0 – Used to indicate which byte in the ATA command block or control block is being accessed

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Table 3-11. Complete Utility 2 Interface Pin Signals (J4) (Continued)

71	NC	Not Connected
72	IDE_PDA2	Primary Disk Address 2 – Used to indicate which byte in the ATA command block or control block is being accessed
73	NC	Not Connected
74	IDE_PDCS0*	Primary Chip Select Drive 0 – Used to select the host-accessible Command Block Register for Drive 0
75	NC	Not Connected
76	IDE_PDCS1*	Primary Chip Select Drive 1 – Used to select the host-accessible Command Block Register for Drive 1
77	NC	Not Connected
78	HDACT	Primary IDE Drive Activity LED – Used to drive an external IDE activity LED, indicating drive activity
79	NC	Not Connected
80	GND5	IDE Ground

Note: The shaded table cells denote power or ground. The * symbol indicates the signal is Active Low.

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Video (VGA/LVDS) Interface

The CPU provides the graphics control and video signals to the traditional glass CRT monitors and LCD flat panel displays. The chip features are listed below:

VGA features:

- Supports a maximum resolution of 1400 x 1050 at 60Hz
- Provides 2D registers for added color, depth, resolution, and hardware acceleration
- Provides integrated 3 x 8-bit DAC with R, G, and B signals to the monitor

LVDS features:

- Integrated single LVDS channel supporting resolution up to 1280 x 800 or 1366 x 768
- Supports 1 x 18 data format
- Supports transmit clock frequency ranges from 25 MHz to 112 MHz

Table 3-12 lists the pin signals of the video (LVDS/VGA) header, which provides 30 pins, 2 rows, odd/even pin sequence (1, 2) with 0.079" (2mm) pitch.

Table 3-12. Video Interface Pin Signals (J10)

Pin #	Signal	Description
1	GPI1	GPIO 1
2	GPI2	GPIO 2
3	GND	Ground
4	VCC_LVDS_CONN	JP2 determines LVDS voltage on pin (+3.3V or +5V)
5	LA_CLK_P	LVDS Clock Positive
6	LA_CLK_N	LVDS Clock Negative
7	LA_DAT2_P	LVDS DATA Positive Line 2
8	LA_DAT2_N	LVDS DATA Negative Line 2
9	LA_DAT1_P	LVDS DATA Positive Line 1
10	LA_DAT1_N	LVDS DATA Negative Line 1
11	LA_DAT0_P	LVDS DATA Positive Line 0
12	LA_DAT0_N	LVDS DATA Negative Line 0
13	LBKLT_CTL	Panel Backlight Control
14	LVDD_EN	Enable Panel Power
15	LDDC_CLK	Display Data Channel Clock
16	LDDC_DATA	Display Data Channel Data
17	LBKLT_EN	Enable Backlight Inverter
18	NC	Not Connected
19	CON_DAC_SDA	Digital to Analog Converter DDC (Display Data Channel) - Data
20	CON_DAC_SCL	Digital to Analog Converter DDC (Display Data Channel) - Clock
21	CON_DAC_RED	Digital to Analog Converter – Red Output to the CRT
22	RED_RETURN	VGA Ground for Red Output
23	CON_DAC_GREEN	Digital to Analog Converter – Green Output to the CRT
24	GREEN_RETURN	VGA Ground for Green Output
25	CON_DAC_BLUE	Digital to Analog Converter – Blue Output to the CRT
26	BLUE_RETURN	VGA Ground for Blue Output
27	CRT_HSYNC	Horizontal Sync – Digital Horizontal Sync Output to the CRT

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Table 3-12. Video Interface Pin Signals (J10) (Continued)

Pin #	Signal	Description
28	GND VGA	VGA Ground
29	CRT_VSYNC	Vertical Sync – Digital Vertical Sync Output to the CRT
30	VCC_CON_DAC	+5V Power and Ground for Digital to Analog Converter

Note: The shaded table cells denote power or ground. The * symbol indicates the signal is Active Low.

System Fan

Table 3-13 lists the pin signals of the optional System Fan header, which provides 2 pins with 0.079" (2mm) pitch.

Table 3-13. Optional System Fan Pin Signals (J6)

Pin #	Signal	Description
1	VCC	+5.0 volts DC +/- 5%
2	GND	Ground

Note: The shaded table cells denote power or ground.

Power Interface

The CoreModule 740 requires one +5 volt DC power source and provides a 10-pin, shrouded header with 2 rows, odd/even pin sequence (1, 2), and 0.100" (2.54mm) pitch. If the +5VDC power drops below ~4.65V, a low voltage reset is triggered, resetting the system.

The power input header (J7) supplies the following voltage and ground directly to the module:

- 5.0VDC +/- 5%

Table 3-14. Power Interface Pin Signals (J7)

Pin	Signal	Descriptions
1	GND	Ground
2	+5V	+5 Volts
3	GND	Ground
4	+12V	+12 Volts routed to PC/104 and PC/104-Plus connectors
5	GND	Ground
6	+3.3V_PCI	+3.3 Volts routed to PCI
7	GND	Ground
8	+5V	+5 Volts
9	GND	Ground
10	+5V	+5 Volts

Note: The shaded table cells denote power or ground.

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Miscellaneous

Real Time Clock (RTC)

The CoreModule 740 contains a Real Time Clock (RTC). The RTC can be backed up with a battery. If the battery is not present, the board BIOS has a battery-less boot option to complete the boot process.

Oops! Jumper (BIOS Recovery)

The Oops! jumper function is provided in the event the BIOS settings you have selected prevent you from booting the system. By using the Oops! jumper you can prevent the current BIOS settings in flash from being loaded, allowing you to re-load default settings.

Use a jumper to connect the DTR pin (4) to the RI pin (9) on Serial Port 1 (COM 1) prior to boot-up to prevent the present BIOS settings from loading. After booting with the Oops! jumper in place, remove the Oops! jumper and return to BIOS Setup. You must now load factory defaults by selecting *Load Optimal Defaults* from the *Exit* menu. Then select *Save Changes and Exit* to reboot the system. Now you can modify the default settings to your desired values. Ensure you save the changes before rebooting the system.

To convert a standard DB9 connector to an Oops! jumper, short together the DTR (4) and RI (9) pins on the front of the connector as shown in Figure 3-1 on the Serial Port 1 DB9 connector.

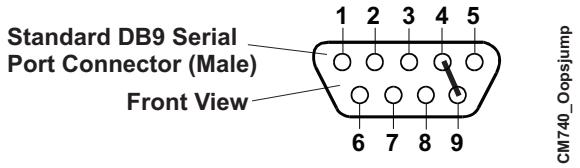


Figure 3-1. Oops! Jumper Serial Port (DB9)

Serial Console

The CoreModule 740 BIOS supports the serial console (or console redirection) feature. This I/O function is provided by an ANSI-compatible serial terminal, or the equivalent terminal emulation software running on another system. This can be very useful when setting up the BIOS on a production line for systems that are not connected to a keyboard and display.

Serial Console Setup

The serial console feature is implemented by entering the serial console settings in BIOS Setup Utility and connecting the appropriate serial cable (a standard null modem serial cable or “Hot Cable”) between one of the serial ports (serial 1 or 2), and the serial terminal or a PC with communications software.

Hot (Serial) Cable

To convert a standard serial cable to a “Hot Cable”, certain pins must be shorted together at the Serial port connector or on the DB9 connector. Short together the RTS (7) and RI (9) pins on either serial port DB9 connector as shown in Figure 3-2.

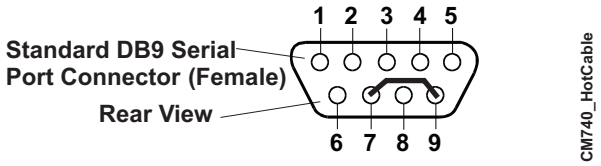


Figure 3-2. Serial Console Jumper

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Watchdog Timer

The Watchdog Timer (WDT) restarts the system if a mishap occurs, ensuring proper start-up after the interruption. Possible problems include failure to boot properly, the application software's loss of control, failure of an interface device, unexpected conditions on the bus, or other hardware or software malfunctions.

The WDT (watchdog timer) can be used both during the boot process and during normal system operation.

- During the Boot process – If the operating system fails to boot in the time interval set in the BIOS, the system will reset.

  Enable the WDT using *Boot Settings Configuration* of the Boot menu in BIOS Setup. Set the WDT for a time-out interval in seconds, between 1 and 255, in one-second increments in the Boot Setting Configuration screen. Ensure you allow enough time for the boot process to complete and for the OS to boot. The OS or application must tickle the WDT as soon as it comes up. This can be done by accessing the hardware directly or through a BIOS call.

- During System Operation – An application can set up the WDT hardware through a BIOS call, or by accessing the hardware directly. Some ADLINK Board Support Packages provide an API interface to the WDT. The application must tickle the WDT in the time set when the WDT is initialized or the system will be reset. You can use a BIOS call to tickle the WDT or access the hardware directly.

  The BIOS implements interrupt 15 function 0C3h to manipulate the WDT.

- Watchdog Code examples – ADLINK has provided source code examples on the CoreModule 740 Support Software QuickDrive illustrating how to control the WDT. The code examples can be easily copied to your development environment to compile and test the examples, or make any desired changes before compiling. Refer to the WDT Readme file on the CoreModule 740 Support Software QuickDrive.

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Chapter 4 BIOS Setup

Introduction

This section assumes the user is familiar with general BIOS Setup and does not attempt to describe the BIOS functions. Refer to "BIOS Setup Menus " on page 39 in this chapter for a map of the BIOS Setup settings. If ADLINK has added to or modified any of the standard BIOS functions, these functions will be described.

Entering BIOS Setup (VGA Display)

To access BIOS Setup using a VGA display for the CoreModule 740:

1. Turn on the VGA monitor and the power supply to the CoreModule 740.
2. Start Setup by pressing the [Del] key when the following message appears on the boot screen.

```
Press DEL to run Setup
```

> **NOTE** If the setting for *Quick Boot* is [Enabled], you may not see this prompt appear on screen. If this happens, press the <Del> key early in the boot sequence to enter BIOS Setup.

3. Follow the instructions on the right side of the screen to navigate through the selections and modify any settings.

Entering BIOS Setup (Remote Access)

This section describes how to enable the Remote Access in VGA mode and enter the BIOS setup through a serial terminal or PC.

1. Turn on the power supply to the CoreModule 740 and enter the BIOS Setup Utility in VGA mode.
2. Set the BIOS feature *Remote Access Configuration* to [Enable] under the **Advanced** menu.
3. Accept the default options or make your own selections for the balance of the Remote Access fields and record your settings.
4. Ensure you select the type of remote serial terminal you will be using and record your selection.
5. Select *Save Changes and Exit* and then shut down the CoreModule 740.
6. Connect the remote serial terminal (or the PC with communications software) to the COM port you selected and recorded earlier in the BIOS Setup Utility.
7. Turn on the remote serial terminal or PC and set it to the settings you selected in the BIOS Setup Utility.

   The default settings for the CoreModule 740 are:

   - COM1
   - 115200
   - 8 bits
   - 1 stop bit
   - no parity
   - no flow control
   - [Always] for *Redirection After BIOS POST*
8. Restore power to the CoreModule 740 and look for the screen prompt shown below.

```
Press <space bar> to update BIOS
```


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9. Press the F4 key to enter Setup (early in the boot sequence if *Quick Boot* is set to [Enabled].)

   If *Quick Boot* is set to [Enabled], you may never see the screen prompt.

10. Use the <Enter> key to select the screen menus listed in the Opening BIOS screen.

> **NOTE** The serial console port is not hardware protected. Diagnostic software that probes hardware addresses may cause a loss or failure of the serial console functions.

PCI-ISA Bridge Mapping

The CoreModule 740 supports ISA bus based modules with an on-board PCI-ISA bridge. The PCI-ISA bridge optionally maps the IRQs to ISA based modules.

The CoreModule 740 system BIOS, maps the above resources based on information provided in the BIOS Setup screens. By default, IRQs to be mapped to ISA modules must be explicitly specified by the user in the BIOS Setup screens.

The IRQs are mapped with the “PCIPnP/IRQx” fields in BIOS setup (where x specifies the IRQ number.) The IRQs 3, 4, 5, 7, 9, 10, 11, 14, and 15 can be mapped to ISA based modules by changing the default setting for these IRQs from “Available” to “Reserved”.

OEM Logo Utility

The CoreModule 740 BIOS supports a graphical logo utility, which can be customized by the user and displayed when enabled through the BIOS Setup Utility. The graphical image can be a company logo or any custom image the user wants to display during the boot process. The custom image can be displayed as the first image on screen and remain there while the OS boots, depending on the options selected in BIOS Setup.

Logo Image Requirements

The user’s image may be customized with any image editing tool, and the system will automatically convert the image into an acceptable format to the tools (files and utilities) provided by ADLINK. The CoreModule 740 OEM Logo utility supports the following image formats:

- Bitmap image
  - 16-Color, 640x480 pixels
  - 256-Color, 640x480 pixels
- JPG image
  - 16-Color, 640x480 pixels
- PCX image
  - 256-Color, 640x480 pixels
- A file size no larger than 64kB

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BIOS Setup Menus

This section provides illustrations of the six main setup screens in the CoreModule 740 BIOS Setup Utility. Below each illustration is a bulleted list of the screen's submenus and setting selections. The setting selections are presented in brackets after each submenu or menu item and the optimal default settings are presented in bold. For more detailed definitions of the BIOS settings, refer to the AMIBIOS8 manual: http://www.ami.com/support/doc/MAN-EZP-80.pdf

Table 4-1. BIOS Setup Menus

BIOS Setup Utility Menu	Item/Topic
Main	Date and Time
Advanced	CPU, IDE, USB, Chipset, Video Function, Super IO, PCI PnP, Remote Access, Watchdog Timer
Power	Power Management (APM) and Resume Power conditions
Boot	Boot up Settings, Boot Order, Removable Drives
Security	Setting or changing Passwords, Boot Sector Virus Protection
Exit	Exiting with or without changing settings, Loading Optimal or Failsafe conditions

BIOS Main Setup Screen

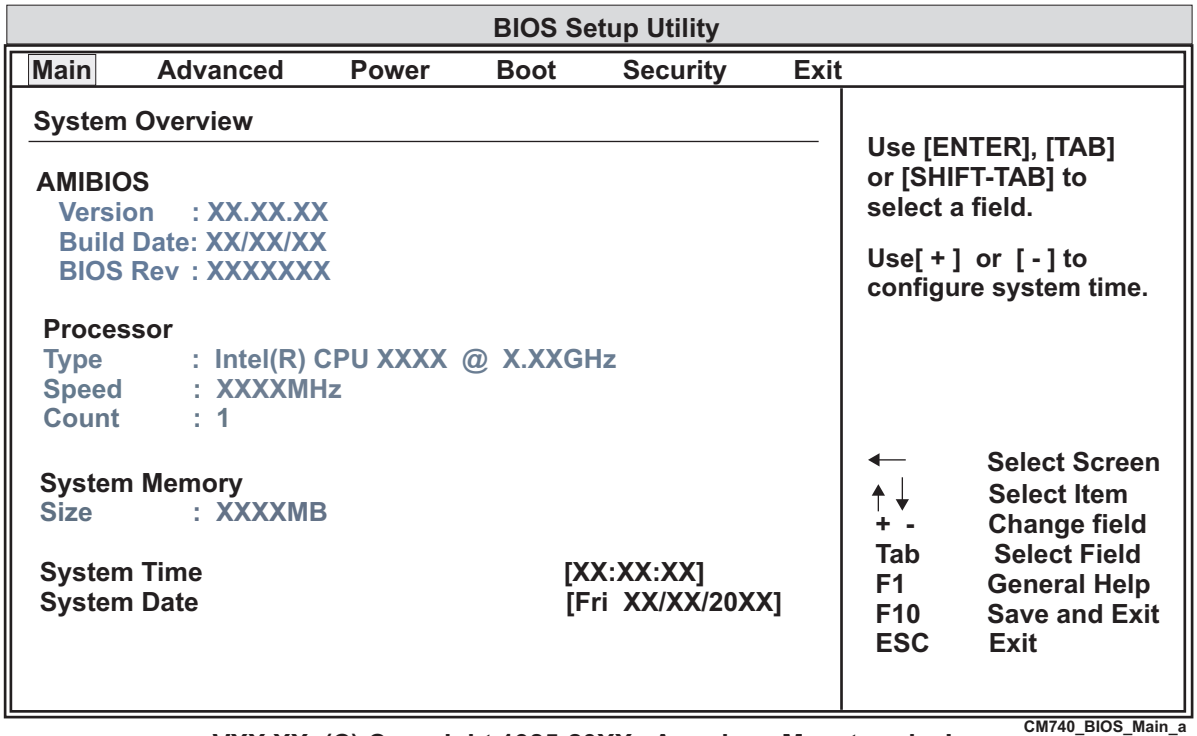


Figure 4-1. BIOS Main Setup Screen

- **Date & Time**
  - System Time (hh:mm:ss) – This is a 24-hour clock setting in hours, minutes, and seconds.
  - System Date (day of week, mm:dd:yyyy) – This field requires the alpha-numeric entry of the day of week, day of the month, calendar month, and all 4 digits of the year, indicating the century plus year (*Fri XX/XX/20XX*).

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BIOS Advanced Setup Screen

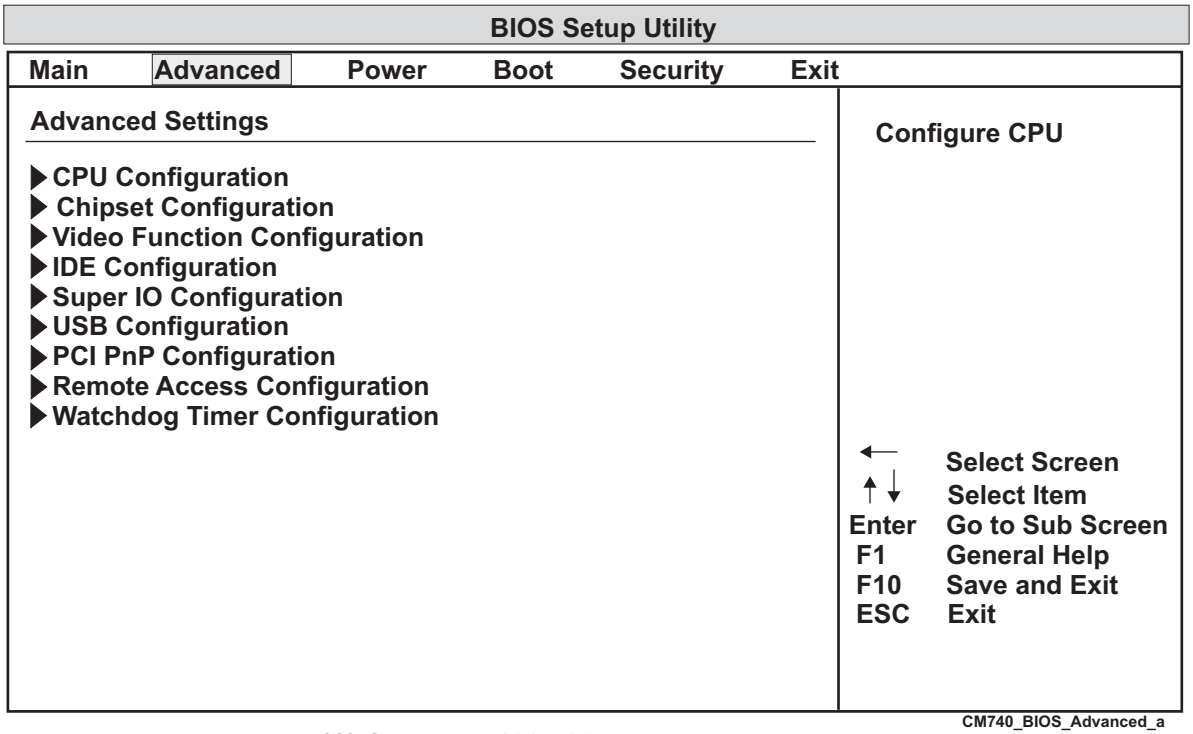


Figure 4-2. BIOS Advanced Setup Screen

- **CPU Configuration**
  - Manufacture: Intel
  - Brand String: Intel® Atom processor X.XXGHz
  - Frequency: X.XXGHz
  - FSB Speed: XXXMHz
  - Cache L1: XXkB
  - Cache L2: XXXXkB
  - Ratio Actual Value: XX
  - Max CPUID Limit [**Disabled**; Enabled]
  - Execute - Disable Bit Capability [Disabled; **Enabled**]
  - Hyper Threading Technology [Disabled; **Enabled**]
  - Intel (R) Speed Step (TM) Technology [Disabled; **Enabled**] - (Available only on the N450 model)
  - Intel (R) C-State Technology [Disabled; **Enabled**]
  - Enhanced C-States [Disabled; **Enabled**]
- **Chipset Configuration**
  - North Bridge Chipset Configuration
    - PCIMMIO Allocation: XGB to XXXXMB
    - DRAM Frequency [**Auto**; Max MHz]
    - Configure DRAM Timing by SPD [**Enabled**; Disabled]

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- South Bridge Chipset Configuration
  - SMBUS Controller [**Enabled**; Disabled]

- **Video Function Configuration**
  - Initiate Graphic Adapter [**PCI/IGD**; IGD]
  - Internal Graphics Mode Select [**Enabled, 8MB**]
  - DVMT Mode Select [**DVMT Mode**; Fixed Mode]
    - DVMT/Fixed Memory [128MB; **256MB**; Maximum DVMT]
  - Boot Display Device [CRT; LVDS; **CRT + LVDS**]
  - Flat Panel Type [640x480; **800x600**; 1024x768; 1280x800; 1366x768]
  - Spread Spectrum Clock [**Disabled**; Enabled]
- **IDE Configuration**
  - ATA/IDE Configuration [Disabled; **Enabled**]
  - Primary IDE Master [Not Detected]
  - Primary IDE Slave [Not Detected]
- **Super IO Configuration**
  - OnBoard Floppy Controller [**Enabled**; Disabled]
  - Serial Port1 Address [Disabled; **3F8**; 3E8; 2E8]
    - Serial Port1 IRQ [3; **4**; 10; 11]
  - Serial Port2 Address [Disabled; **2F8**; 3E8; 2E8]
    - Serial Port2 IRQ [**3**; 4; 10; 11]
  - Parallel Port Address [Disabled; **378**; 278; 3BC]
    - Parallel Port Mode [**Normal**; SPP (Bi-Dir); EPP + SPP; ECP; ECP + EPP]
    - Parallel Port IRQ [IRQ5; **IRQ7**]
  - Floppy A [**Disabled**; 360 KB 51/4"; 1.2 MB 51/4"; 720 KB 31/2"; 1.44 MB 31/2"; 2.88 MB 31/2"]
- **USB Configuration**
  - Module Version - X.XX.X - XX.X
  - USB Devices Enabled: None
  - USB Functions [Disabled; 2 USB Ports; **4 USB Ports**]
  - USB 2.0 Controller [**Enabled**; Disabled]
  - Legacy USB Support [Disabled; **Enabled**; Auto]
  - USB 2.0 Controller Mode [FullSpeed; **HiSpeed**]
  - BIOS EHCI Hand-Off [Disabled; **Enabled**]
- **PCI/PnP Configuration**
  - Clear NVRAM [**No**; Yes]
  - PCI Latency Timer [32; **64**; 96; 128; 160; 192; 224; 248]
  - Palette Snooping [**Disabled**; Enabled]
  - IRQ3 [**Available**; Reserved]
  - IRQ4 [**Available**; Reserved]
  - IRQ5 [**Available**; Reserved]

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- IRQ7 [**Available**; Reserved]
- IRQ9 [**Available**; Reserved]
- IRQ10 [**Available**; Reserved]
- IRQ11 [**Available**; Reserved]
- IRQ14 [**Available**; Reserved]
- IRQ15 [**Available**; Reserved]
- Reserved Memory Size [**Disabled**; 16k; 32k; 64k]

- **Remote Access Configuration**
  - Remote Access [**Hot Cable**; Enabled]
  - Serial Port Number [**COM1**; COM2]
    - Base Address, IRQ [**3F8h, 4**]
  - Serial Port mode [**115200 8, n, 1**; 57600 8, n, 1; 38400 8, n, 1; 19200 8, n, 1; 09600 8, n, 1]
  - Flow Control [**None**; Hardware; Software]
  - Redirection After BIOS POST [Disabled; Boot Loader; **Always**]
  - Terminal Type [**ANSI**; VT100; VT-UTF8]
  - VT-VTF8 Combo Key Support [Disabled; **Enabled**]
  - Sredir Memory Display Delay [**No Delay**; Delay 1 Sec; Delay 2 Sec; Delay 4 Sec]
- **Watchdog Timer Configuration**
  - Watchdog Timer [**Disabled**; Enabled]

BIOS Power Management Setup Screen

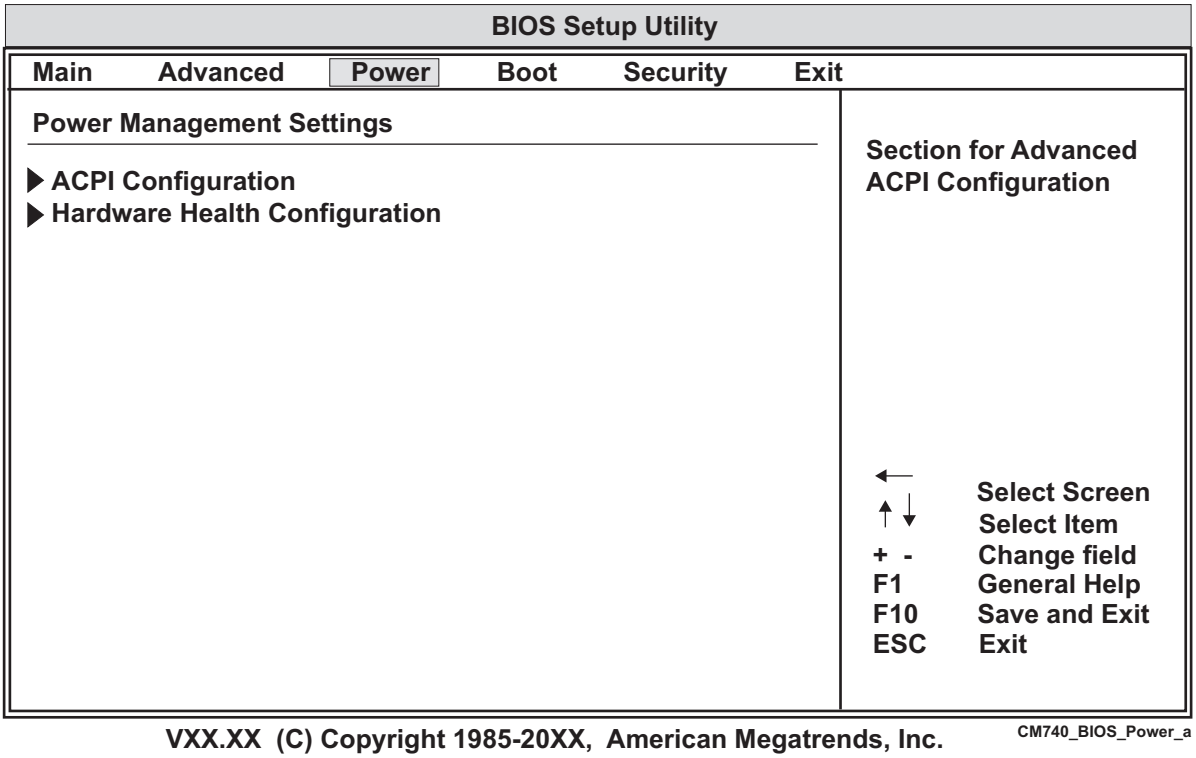


Figure 4-3. Power Management Setup Screen

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- **Power Management Settings**
  - ACPI Configuration
    - ACPI Version Features [ACPI v1.0; **ACPI v2.0**; ACPI v3.0]
    - ACPI APIC Support [Disabled; **Enabled**]
    - APIC ACPI SCI IRQ [**Disabled**; Enabled]
    - High Performance Event Timer [Disabled; **Enabled**]
    - HPET Memory Address [**FED00000h**; FED01000h; FED02000h; FED03000h]
  - Hardware Health Configuration
    - CPU Temperature XX°C / XXX°F

BIOS Boot Setup Screen

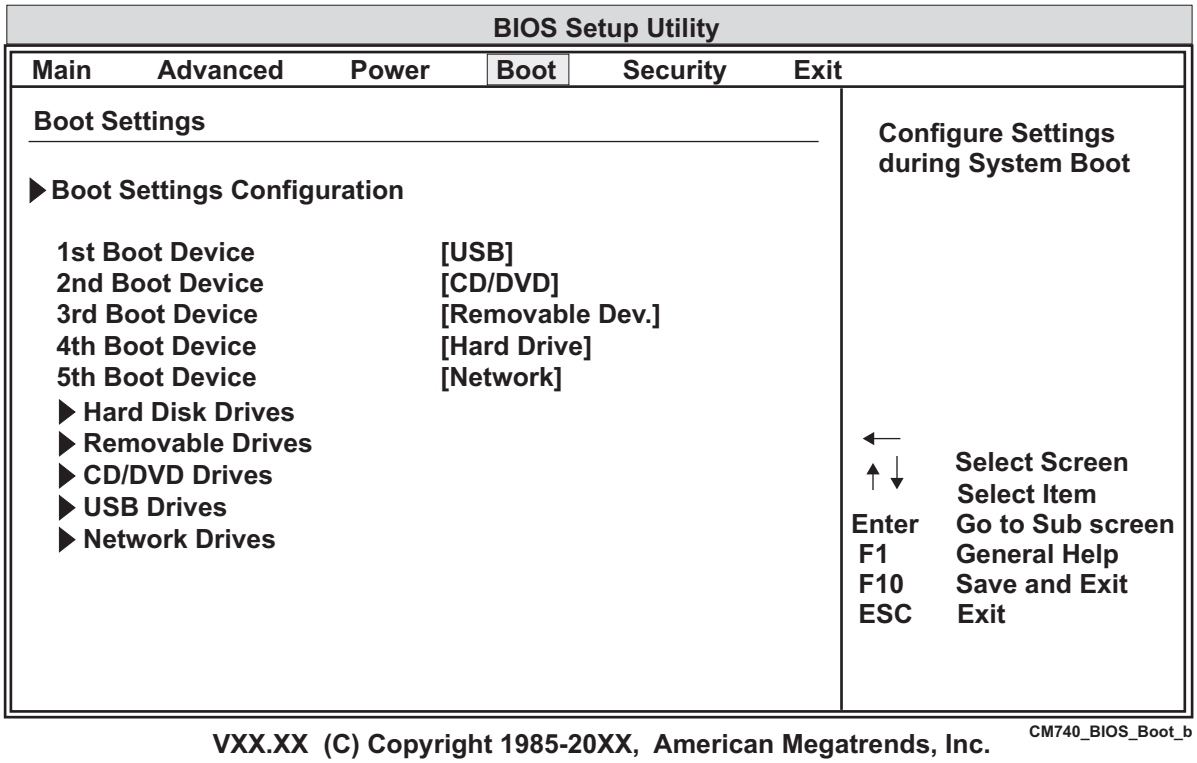


Figure 4-4. BIOS Boot Setup Screen

- **Boot Settings**
  - Boot Settings Configuration
    - Quick Boot [Disabled; **Enabled**]
    - Quiet Boot [**Disabled**; Enabled]
    - AddOn ROM Display Mode [**Force BIOS**; Keep Current]
    - Bootup Num-Lock [Off; **On**]
    - PS/2 Mouse Support [Disabled; Enabled; **Auto**]
    - Wait for 'F1' If Error [Disabled; **Enabled**]
    - Hit 'DEL' Message Display [Disabled; **Enabled**]
    - Interrupt 19 Capture [**Disabled**; Enabled]

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- 1st Boot Device [**Removable Dev**; CD/DVD; Hard Drive; USB; Network; Disabled]
- 2nd Boot Device [Removable Dev; **CD/DVD**; Hard Drive; USB; Network; Disabled]
- 3rd Boot Device [Removable Dev; CD/DVD; **Hard Drive**; USB; Network; Disabled]
- 4th Boot Device [Removable Dev; CD/DVD; Hard Drive; **USB**; Network; Disabled]
- 5th Boot Device [Removable Dev; CD/DVD; Hard Drive; USB; **Network**; Disabled]
- Hard Disk Drives
  - 1st Drive [**SATA: SM-XGB NANDri**; Disabled]
- Removable Drives
  - 1st Drive [Not Installed]
- CD/DVD Drives
  - 1st Drive [Not Installed]
- USB Drives
  - 1st Drive [Not Installed]
- Network drives
  - 1st Drive [Not Installed]

BIOS Security Setup Screen

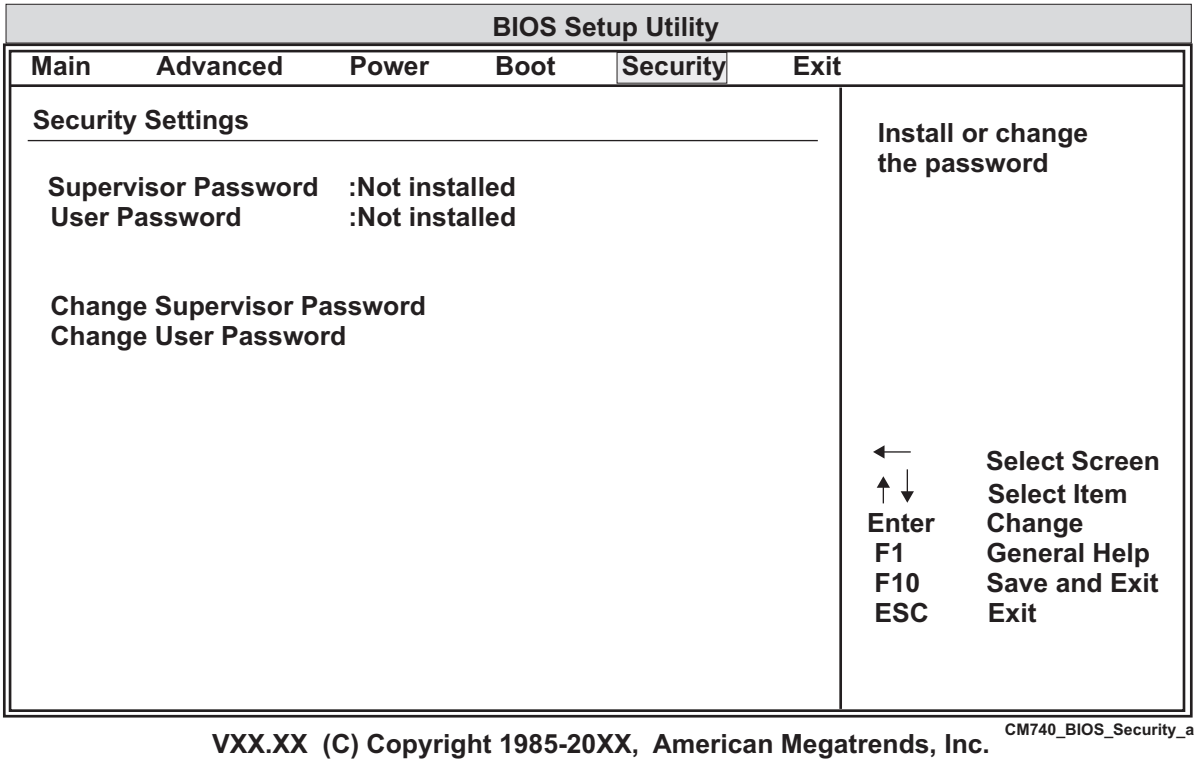


Figure 4-5. BIOS Security Setup Screen

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- **Security Settings**
  - Supervisor Password [Not Installed]
  - User Password [Not Installed]
  - Change Supervisor Password [Enter New Password]
  - Change User Password [Enter New Password]

BIOS Exit Setup Screen

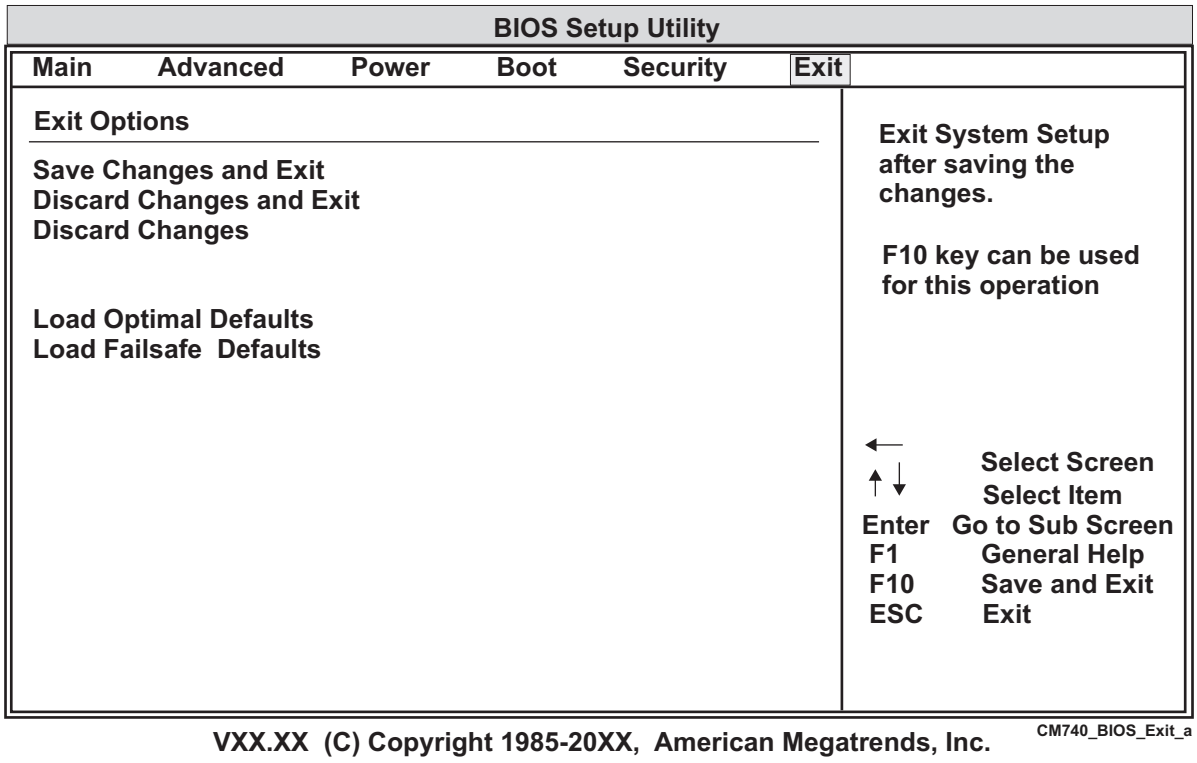


Figure 4-6. BIOS Exit Setup Screen

- **Exit Options**
  - Save Changes and Exit (F10 key can be used for this operation.)
  - Discard Changes and Exit (ESC key can be used for this operation.)
  - Discard Changes (F7 key can be used for this operation.)
  - Load Optimal Defaults (F9 key can be used for this operation.)
  - Load Failsafe Defaults (F8 key can be used for this operation.)

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Appendix A Technical Support

ADLINK Technology, Inc. provides a number of methods for contacting Technical Support listed below in Table A-1. Requests for support through the Ask an Expert are given the highest priority, and usually will be addressed within one working day.

- ADLINK's Ask an Expert – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the Ampro By ADLINK web page at http://www.adlinktech.com/AAE/. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online if you wish to use the Ask a Question feature.

  ADLINK strongly suggests that you register with the web site. By creating a profile on the ADLINK web site, you will have a portal page called "My ADLINK" unique to you with access to exclusive services and account information.

- Personal Assistance – You may also request personal assistance by creating an Ask an Expert account and then going to the Ask a Question feature. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request, you must log in to go to My Stuff area where you can check status, update your request, and access other features.

- Download Service – This service is also free and available 24 hours a day at http://www.adlinktech.com. For certain downloads such as technical documents and software, you must register online before you can log in to this service.

Table A-1. Technical Support Contact Information

Method	Contact Information
Ask an Expert	http://www.adlinktech.com/AAE/
Web Site	http://www.adlinktech.com
Standard Mail	Contact us should you require any service or assistance. **ADLINK Technology, Inc.** Address: 9F, No.166 Jian Yi Road, Zhonghe District New Taipei City 235, Taiwan 新北市中和區建一路 166 號 9 樓 Tel: +886-2-8226-5877 Fax: +886-2-8226-5717 Email: service@adlinktech.com **Ampro ADLINK Technology, Inc.** Address: 5215 Hellyer Avenue, #110, San Jose, CA 95138, USA Tel: +1-408-360-0200 Toll Free: +1-800-966-5200 (USA only) Fax: +1-408-360-0222 Email: info@adlinktech.com **ADLINK Technology (China) Co., Ltd.** Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203) 300 Fang Chun Rd., Zhangjiang Hi-Tech Park, Pudong New Area, Shanghai, 201203 China Tel: +86-21-5132-8988 Fax: +86-21-5132-3588 Email: market@adlinktech.com

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Table A-1. Technical Support Contact Information (Continued)

	ADLINK Technology Beijing Address: 北京市海淀区上地东路 1 号盈创动力大厦 E 座 801 室(100085) Rm. 801, Power Creative E, No. 1, B/D Shang Di East Rd., Beijing, 100085 China Tel: +86-10-5885-8666 Fax: +86-10-5885-8625 Email: market@adlinktech.com **ADLINK Technology Shenzhen** Address: 深圳市南山区科技园南区高新南七道 数字技术园 A1 栋 2 楼 C 区 (518057) 2F, C Block, Bldg. A1, Cyber-Tech Zone, Gao Xin Ave. Sec. 7, High-Tech Industrial Park S., Shenzhen, 518054 China Tel: +86-755-2643-4858 Fax: +86-755-2664-6353 Email: market@adlinktech.com **ADLINK Technology (Europe) GmbH** Address: Nord Carree 3, 40477 Duesseldorf, Germany Tel: +49-211-495-5552 Fax: +49-211-495-5557 Email: emea@adlinktech.com **ADLINK Technology, Inc. (French Liaison Office)** Address: 15 rue Emile Baudot, 91300 Massy CEDEX, France Tel: +33 (0) 1 60 12 35 66 Fax: +33 (0) 1 60 12 35 66 Email: france@adlinktech.com **ADLINK Technology Japan Corporation** Address: 〒101-0045 東京都千代田区神田鍛冶町 3-7-4 KANDA374 ビル 4F KANDA374 Bldg. 4F, 3-7-4 Kanda Kajicho, Chiyoda-ku, Tokyo 101-0045, Japan Tel: +81-3-4455-3722 Fax: +81-3-5209-6013 Email: japan@adlinktech.com **ADLINK Technology, Inc. (Korean Liaison Office)** Address: 서울시 서초구 서초동 1506-25 한도 B/D 2 층 2F, Hando B/D, 1506-25, Seocho-Dong, Seocho-Gu, Seoul 137-070, Korea Tel: +82-2-2057-0565 Fax: +82-2-2057-0563 Email: korea@adlinktech.com **ADLINK Technology Singapore Pte. Ltd.** Address: 84 Genting Lane #07-02A, Cityneon Design Centre, Singapore 349584 Tel: +65-6844-2261 Fax: +65-6844-2263 Email: singapore@adlinktech.com **ADLINK Technology Singapore Pte. Ltd. (Indian Liaison Office)** Address: No. 1357, "Anupama", Sri Aurobindo Marg, 9th Cross, JP Nagar Phase I, Bangalore - 560078, India Tel: +91-80-65605817 Fax: +91-80-22443548 Email: india@adlinktech.com

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Appendix B I/O Interface Board Description

Overview

The I/O Interface Board provides the connections for the keyboard, mouse, two USB ports, and all the standard input/output connections for the floppy/parallel port and serial ports. The I/O Interface Board also provides an auxiliary battery connection, PC speaker, and a reset switch.

I/O Interface Board Layout

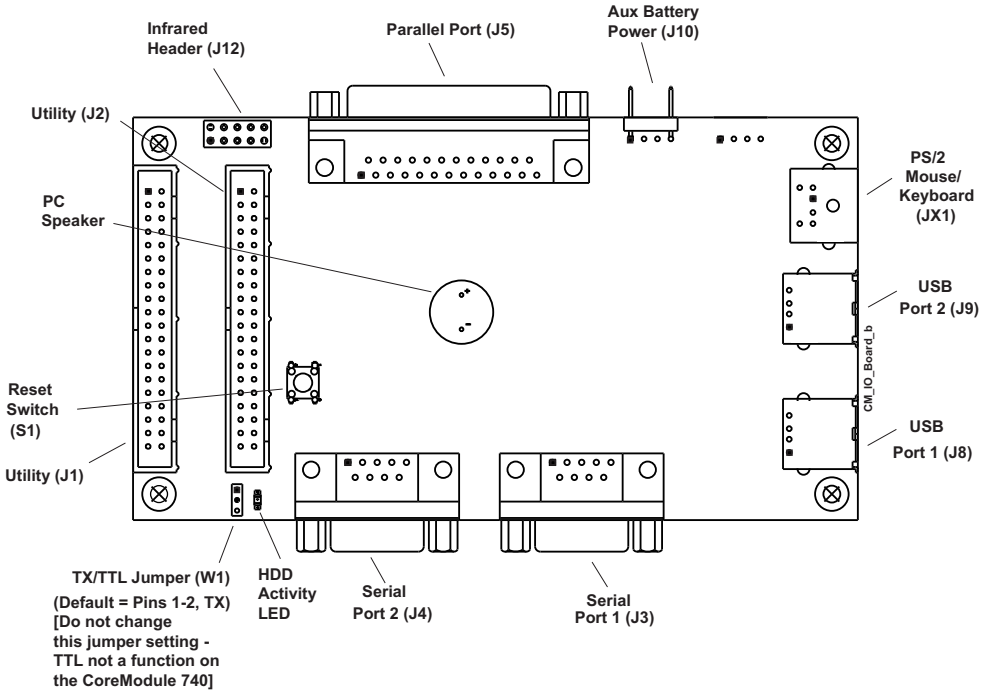


Figure B-1. I/O Interface Board Connectors (Top view)

NOTE	If you need more information concerning the I/O Interface Board than is provided in this Appendix, refer to the CoreModule 740 QuickDrive for a schematic, BOM, and AVL.

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I/O Interface Board Connectors and Headers

The following tables define the pin signals of all the non-standard connectors and headers on the I/O Interface Board. This appendix does not define industry-standard connectors on the board such as parallel, DB9 serial, PS2 mouse and keyboard, and USB.

> **NOTE** The CoreModule 740 does not support the Infrared header (J12) shown in Figure B-1.

Table B-1 lists the signals and their descriptions for the J1 Utility interface, which provides a shrouded 40-pin header with odd/even (1, 2) pin sequence. The third column in this table denotes the corresponding pins from the J5 header on the CoreModule 740.

Table B-1. Utility Interface Pin Signals (J1)

Pin #	Signal	From J5 Pin #	Description
1	DCD1*	J5-1	Serial Data Carrier Detect 1 – Indicates external modem is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR1 as part of the DTR1/DSR1 handshake.
2	DSR1*	J5-3	Serial Data Set Ready 1 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR1 for overall readiness to communicate.
3	RXD1	J5-5	Serial Receive Data 1 Input – This line is typically held at a logic 1 (mark) when no data is being transmitted, and is held “Off” for a brief interval after an “On” to “Off” transition on the RTS1 line to allow the transmission to complete.
4	RTS1*	J5-7	Serial Request To Send 1 – Indicates serial port is ready to transmit data. Used as hardware handshake with CTS1 for low level flow control.
5	TXD1	J5-9	Serial Transmit Data 1 Output – This line is typically held to a logic 1 when no data is being sent. Typically, a logic 0 (On) must be present on RTS1, CTS1, DSR1, and DTR1 before data can be transmitted on this line.
6	CTS1*	J5-11	Serial Clear To Send 1 – Indicates external serial communication device is ready to receive data. Used as hardware handshake with RTS1 for low level flow control.
7	DTR1*	J5-13	Serial Data Terminal Ready 1 – Indicates port is powered, initialized, and ready. Used as hardware handshake with DSR1 for overall readiness to communicate.
8	RI1*	J5-15	Serial Ring Indicator 1 – Indicates external modem is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
9	GND	J5-17	Digital Ground
10	NC	J5-19	Not Connected
11	DCD2*	J5-21	Serial Data Carrier Detect 2 – Indicates external modem is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR2 as part of the DTR2/DSR2 handshake.

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Table B-1. Utility Interface Pin Signals (J1) (Continued)

12	DSR2*	J5-23	Serial Data Set Ready 2 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR2 for overall readiness to communicate.
13	RXD2	J5-25	Serial Receive Data 2 Input – This line is typically held at a logic 1 (mark) when no data is being transmitted, and is held "Off" for a brief interval after an "On" to "Off" transition on the RTS2 line to allow the transmission to complete.
14	RTS2*	J5-27	Serial Request To Send 2 – Indicates serial port is ready to transmit data. Used as hardware handshake with CTS2 for low level flow control.
15	TXD2	J5-29	Serial Transmit Data 2 Output – This line is typically held to a logic 1 when no data is being sent. Typically, a logic 0 (On) must be present on RTS1, CTS1, DSR1, and DTR1 before transmitting data on this line.
16	CTS2*	J5-31	Serial Clear To Send 2 – Indicates external serial communication device is ready to receive data. Used as hardware handshake with RTS2 for low level flow control.
17	DTR2*	J5-33	Serial Data Terminal Ready 2 – Indicates port is powered, initialized, and ready. Used as hardware handshake with DSR2 for overall readiness to communicate.
18	RI2*	J5-35	Serial Ring Indicator 2 – Indicates external modem is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
19	GND	J5-37	Digital Ground
20	TXD2_ TTL (NF)	J5-39	Serial Port 2 Transmit TTL – Places TTL TX signals on pin 3 of the Serial Port 2 (J4) when jumper (W1) on I/O Interface Board is set to pins 2-3. (NF = No function at the CoreModule 740.)
21	USB_ OC0*	J5-41	USB0 Over Current Protection – The voltage network monitors power and disables port if this input is low. Direct power input through fuse on I/O Interface Board provides over current protection.
22	USB PWR0	J5-43	USB Port 0 power (+5V +/-5%)
23	USB P0-	J5-45	Universal Serial Bus Port 0 Data –
24	USB P0+	J5-47	Universal Serial Bus Port 0 Data +
25	GND	J5-49	USB Ground
26	USB_OC1*	J5-51	USB1 Over Current Protection – The voltage network monitors power and disables port if this input is low. Direct power input through fuse on I/O Interface Board provides over current protection.
27	USB PWR1	J5-53	USB Port 1 power (+5V +/-5%)
28	USB P1-	J5-55	Universal Serial Bus Port 1 Data –
29	USB P1+	J5-57	Universal Serial Bus Port 1 Data +
30	GND	J5-59	USB Ground
31	MS Dta	J5-61	Mouse Data
32	MS Clk	J5-63	Mouse Clock
33	GND	J5-65	Ground
34	MS Pwr	J5-67	Mouse Power (+5V +/-5%)

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Table B-1. Utility Interface Pin Signals (J1) (Continued)

35	HD Act	J5-69	IDE Hard Drive Activity – Front panel HD activity signal to LEDs
36	NC	J5-71	Not Connected (External SMI)
37	NC	J5-73	Not Connected (RS485 Transmit/Receive Data –)
38	NC	J5-75	Not Connected (RS485 Transmit/Receive Data +)
39	NC	J5-77	Not Connected (External –12V input)
40	NC	J5-79	Not Connected (External –5V input)

Note: The shaded table cells denote power or ground. NC = Not Connected at the CoreModule 740. The * symbol indicates the signal is Active Low.

Table B-2 lists the signals and their descriptions for the J2 Utility interface, which provides a shrouded 40-pin header with odd/even (1, 2) pin sequence. The third column in this table denotes the corresponding pins from the J5 header on the CoreModule 740.

Table B-2. Utility Interface Pin Signals (J2)

Pin #	Signal	From J5 Pin #	Description
1	STB*	J5-2	Strobe* – Output used to strobe data into the printer. I/O pin in ECP/EPP mode.
2	AFD*	J5-4	Auto Feed – This is a Request signal sent to the printer to automatically feed one line after each line is printed.
3	PD0	J5-6	Parallel Data 0 – These signals (0 to 7) provide the parallel port data to the printer.
4	ERR*	J5-8	Parallel Error – This is a Status output signal from the printer. A Low State indicates an error condition on the printer.
5	PD1	J5-10	Parallel Data 1 – Refer to PD0, pin 3, for more information.
6	Init*	J5-12	Parallel Initialize – This signal used to Initialize printer. Output in standard mode, I/O in ECP/EPP mode.
7	PD2	J5-14	Parallel Data 2 – Refer to PD0, pin 3, for more information.
8	SLIn*	J5-16	Parallel Select In – This signal used to select the printer. I/O pin in ECP/EPP mode.
9	PD3	J5-18	Parallel Data 3 – Refer to PD0, pin 3, for more information.
10	GND	J5-20	Ground
11	PD4	J5-22	Parallel Data 4 – Refer to PD0, pin 3, for more information.
12	GND	J5-24	Ground
13	PD5	J5-26	Parallel Data 5 – Refer to PD0, pin 3, for more information.
14	GND	J5-28	Ground
15	PD6	J5-30	Parallel Data 6 – Refer to PD0, pin 3, for more information.
16	GND	J5-32	Ground
17	PD7	J5-34	Parallel Data 7 – Refer to PD0, pin 3, for more information.
18	GND	J5-36	Ground
19	ACK*	J5-38	Parallel Acknowledge – This is a Status output signal from the printer. A Low State indicates it has received the data and is ready to accept new data.
20	GND	J5-40	Ground

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Table B-2. Utility Interface Pin Signals (J2) (Continued)

21	BSY	J5-42	Parallel Busy – This is a Status output signal from the printer. A High State indicates the printer is not ready to accept data.
22	GND	J5-44	Ground
23	PE	J5-46	Parallel Paper End – This is a Status output signal from the printer. A High State indicates it is out of paper.
24	GND	J5-48	Ground
25	Slct	J5-50	Parallel Select – This is a Status output signal from the printer. A High State indicates it is powered on.
26	IR FIRM	J5-52	IR Function Mode Select – Disabled (Terminated with 10k ohm resistor to ground on CoreModule 740.)
27	NC	J5-54	Not connected
28	GND	J5-56	Signal Ground
29	IR TXD	J5-58	IR Transmit Data (HPSIR or ASKIR)
30	IR RXD	J5-60	IR Receive Data (HPSIR or ASKIR)
31	SPKR+	J5-62	Speaker + drive signal
32	GND	J5-64	Speaker return
33	RST SW	J5-66	Reset Switch
34	KB SW	J5-68	Not Connected (Keyboard switch)
35	KB DTA	J5-70	Keyboard Data signal
36	KB CLK	J5-72	Keyboard Clock signal
37	GND	J5-74	Digital Ground
38	KB PWR	J5-76	Keyboard power (+5V +/-5%)
39	BATV+	J5-78	External Backup Battery +
40	BATV-	J5-80	External Backup Battery Return -

Note: The shaded table cells denote power or ground. NC = Not Connected at the CoreModule 740. The * symbol indicates the signal is Active Low.

Table B-3 lists the signals and their descriptions for the Auxiliary Battery interface which provides a right-angle, single row, 4-pin header (with two pins removed.) The third column in this table denotes the corresponding pins from the on-board J2 header.

Table B-3. Auxiliary Battery Interface Pin Signals (J10)

Pin #	Signal	From On-Board Connector & Pin #	Description
1	BATV+	J2-39	External Backup Battery +
2	NC	NA	Not connected
3	NC	NA	Not connected
4	BATV-	J2-40	External Backup Battery Return -

Note: The shaded table cells denote power or ground.

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