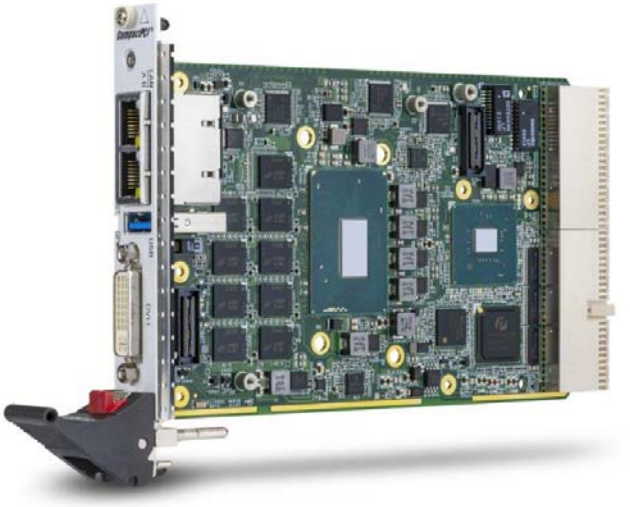
cPCI-3520 Series

Performance 3U CompactPCI® Processor Blade
Intel® Xeon® E, 8th/9th Gen Intel® Core™

User's Manual



Manual Rev.:	1.0
Revision Date:	May 5, 2022
Part No:	50M-00036-1000

LEADING EDGE COMPUTING

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Revision History

Revision	Release Date	Description of Change(s)
1.0	2022-05-05	Initial release

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Preface

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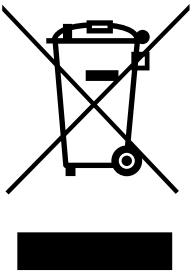
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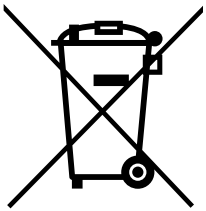
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Product names mentioned herein are used for identification purposes only and may be trademarks and/or registered trademarks of their respective companies.

Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

NOTE: Additional information, aids, and tips that help users perform tasks.

CAUTION: Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

WARNING: Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

1.1 Overview

The ADLINK cPCI-3520 Series is a 3U CompactPCI® processor blade with soldered DDR4-2666 ECC memory up to 32GB. The ADLINK cPCI-3520 features the Intel® Xeon® E, 8th/9th Gen Intel® Core™ processor with Mobile Intel® CM246 Chipset.

The cPCI-3520 Series is a 3U CompactPCI blade available in single-slot (4HP), dual-slot (8HP) or triple-slot (12HP) width form factors with various daughter boards to provide a broad range of I/O requirements. Faceplate I/O in the single-slot (4HP) version includes 1x DVI-I, 2x GbE and 1x USB 3.0 port (these I/O are common to all versions). Faceplate I/O in the dual-slot (8HP) version includes additional 2x USB 2.0, 1x COM, 1x KB/MS and Line-in/Line-out on the cPCI-3520D or additional 2x DisplayPorts, 1x COM in RJ-45 connector, 1x KB/MS and 1x additional USB 2.0 port on the cPCI-3520G. Two more dual-slot options are the cPCI-3520L with additional 2x GbE, 1x COM and 2x USB and the cPCI-3520M with one 100-pin high density connector supporting additional 2x DVI-D, 2x USB 2.0, 2x COM, 2x KB/MS and Line-in/Line-out ports.

Graphics support is integrated on the CPU and allows 3 independent displays on the faceplate by selecting the cPCI-3520G with additional 2x DisplayPorts. Storage includes a CFast slot, mSATA socket or a 32GB onboard SSD and 2.5" SATA drive on the layer 2 daughter board (cPCI-3520D/L/M/P). One optional PCI 32-bit/66MHz PMC site or PCIe x1 XMC site is available on the 8HP or 12HP versions (cPCI-3520S or cPCI-3520P).

Rear I/O signals to J2 include 4x PCIe x1, 3x SATA 3 Gb/s, and 3x USB 2.0. 3x GPIO and SMBus signals are also routed to the J2 connector. The optional Rear Transition Module (RTM) provides 3x SATA, 2x GbE, 2x USB, 1x COM (Tx/Rx), and 1x VGA port.

The cPCI-3520 is a high performance solution for factory automation and other industrial applications that require superior data transfer capability and advanced computing power. The ADLINK cPCI-3520 provides high manageability, supports Satellite mode operation as a standalone blade in peripheral slots, and IPMI for

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system health monitoring. A GbE port on the faceplate supports Intel® AMT 9.0 for remote monitoring.

1.2 Features

- 3U CompactPCI blade in 4HP, 8HP or 12HP width form factor
- Intel® Xeon® E, 8th/9th Gen Intel® Core™ Processor
- Graphics and memory controllers integrated in processor
- Dual channel DDR4-2666 soldered SDRAM with ECC, up to 32GB
- 32-bit, 33/66MHz CompactPCI Interface based on PCI specifications, universal V(I/O)
- Supports Satellite mode operation as a standalone blade in peripheral slots
- Optional 32-bit/66MHz PMC or PCIe x1 XMC site
- Supports IPMI for system health monitoring
- DVI-I port on front with VGA switchable to rear I/O by BIOS setting
- Additional two DisplayPorts on layer 2 daughter board (cPCI-3520G)
- Supports 3 independent displays
- Two PCIe Gigabit Ethernet egress ports
- Two additional PCIe Gigabit Ethernet Controllers routed to RTM (cPCI-R3P00)
- Additional two Gigabit Ethernet ports on 80mm RTM (cPCI-R3P00T)
- Line-in and Line-out ports on faceplate (cPCI-3520D)
- CFast or mSATA socket for SATA interface storage
- Optional onboard SSD for SATA interface storage (shares space with CFast socket)
- 2.5" SATA connector on 8HP/12HP versions at 6 Gb/s (cPCI-3520D/G/M/L/P)

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1.3 Model Number Decoder

Blades

cPCI-EX 3520 D / 9850HL / 32G / S32

(A) (B) (C) (D) (E)

(A) Operating Temperature Code

- **Blank** = -20°C to +70°C
- EX= -40°C to +85°C (for CPUs with TDP 25W only)

(B) Configuration Code

- **Blank** = Single slot width with CFast socket, 1x DVI-I, 1x USB 3.0, 2x GbE
- **D** = Dual slot width with CFast socket, 1x DVI-I, 1x USB 3.0, 2x GbE on layer 1; 2x USB 2.0, COM (RS-232/422/485), PS/2 KB/MS, Line-in, Line-out ports and 2.5" SATA drive space on layer 2
- **G** = Dual slot width with CFast socket, 1x DVI-I, 1x USB 3.0, 2x GbE on layer 1; 2x DisplayPort, RJ-45 COM (RS-232/422/485), PS/2 KB/MS, USB 2.0 ports, onboard SATA connector and 2.5" SATA drive space on layer 2
- **L** = Dual slot width with CFast socket, 1x DVI-I, 1x USB 3.0, 2x GbE on layer 1; 2x GbE, 1x DB-9 COM (RS-232/422/485), 1x USB 2.0 on faceplate, and 2.5" SATA drive space on layer 2
- **M** = Dual slot width with CFast socket, 1x DVI-I, 1x USB 3.0, 2x GbE on layer 1; 1x 100-pin high density connector supports, 2x DVI-D, 2x USB 2.0, 2x COM (RS-232/422/485), 1x KB/MS, audio and 2.5" SATA drive space on layer 2
- **P** =Triple slot width with CFast socket, 1x DVI-I, 1x USB 3.0, 2x GbE on layer 1; 2x USB 2.0, COM (RS-232/422/485), PS/2 KB/MS, Line-in, Line-out ports and 2.5" SATA drive space on layer 2; PMC/XMC site on layer 3
- **S** = Dual slot width with CFast socket, 1x DVI-I, 1x USB 3.0, 2x GbE on layer 1; PMC/XMC site on layer 2
- **T** = Dual slot width with CFast socket, 1x DVI-I, 1x USB 3.0, 2x GbE via RJ45 on layer 1; 2x GbE via M12, 1x DB-9 COM (RS-232/422/485), 1x onboard USB 2.0 port and 2.5" SATA drive space on layer 2

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(C) CPU Code

- **2276ML**= 6-core Intel® Xeon® E-2276ML w/ ECC
- **9850HL** = 6-core Intel® Core™ i7-9850HL
- **8400HL** = 4-core Intel® Core™ i5-8400H
- **9100HL**= 4-core Intel® Core™ i3-9100HL w/ ECC

(D) Memory Size Code

- **M8** = 8GB DDR3L-2666 soldered SDRAM
- **M16** = 2x 8GB DDR3L-2666 soldered SDRAM
- **M32** = 2x 16GB DDR4-2666 soldered SDRAM

(E) Storage Board Code

- **Blank** = Default with CFast socket
- **MS** = Equipped with mSATA socket
- **S32** = Onboard soldered 32GB SSD

RTMs

cPCI- R3P00 T

(A)

(A) Model Code

- Blank = dual slot width, 50mm depth 3U RTM with 2x COM, 2x USB, 3x SATA, VGA, 2x GbE (switched from front CPU blade)
- T = dual slot width, 80mm depth 3U RTM with 2x COM, 2x USB, 3x SATA, VGA, 2x GbE (independent from front CPU blade)

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1.4 Package Contents

The cPCI-3520 is packaged with the following components. If any of the following items are missing or damaged, retain the shipping carton and packing material and contact the dealer for inspection. Please obtain authorization before returning any product to ADLINK. The packing contents of cPCI-3520 Series non-standard configurations will vary depending on customer requests.

Processor Blade

- The cPCI-3520 Series Processor Blade
  - CPU and memory specifications will differ depending on options selected
  - Thermal module is assembled on the board
- Y-cable for PS/2 combo port (cPCI-3520D/P only)
- 2.5" SATA drive installation kit (cPCI-3520D/G/L/M/P only)
- RJ-45 to DB-9 COM adapter cable (cPCI-3520G version only)
- DisplayPort to DVI adapter cable (cPCI-3520G version only)l


NOTE:

No I/O cables are included with the cPCI-3520M version.


NOTE:

The contents of non-standard cPCI-3520 configurations may vary depending on the customer's requirements.

Rear Transition Module

- cPCI-R3P00 or cPCI-R3P00T RTM

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Blade Optional Accessories

- 2.5” SATA drive installation kit (P/N 58-00176-0000)
- Y-cable for PS/2 combo port (P/N 30-01016-2000)
- RJ-45 to DB-9 COM adapter cable (P/N 30-01020-0200)
- DisplayPort to DVI adapter cable (P/N 30-01120-0000)
- DisplayPort to VGA adapter cable (P/N 30-01119-0000)
- DisplayPort to HDMI adapter cable (P/N 30-01121-0000)
- USB 3.0 Type A male-to-female extension cable (P/N: 30-01175-0000)
- SCSI 100-pin IO cable: 2x DVI-D female, 2x DB9 male, 2x USB female, 2x PS/2 female, 2x audio jack (available by request)



This product must be protected from static discharge and physical shock. Never remove any of the components except at a static-free workstation. Use the anti-static bag shipped with the product when putting the board on a surface. Wear an anti-static wrist strap properly grounded on one of the system's ESD ground jacks when installing or servicing system components.

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2 Specifications

2.1 cPCI-3520 Processor Blade Specifications

CompactPCI® Standards	• PICMG® 2.0 CompactPCI® Rev. 3.0 • PICMG® 2.9 System Management Rev. 1.0 (IPMI v1.5)
Mechanical	• Standard 3U CompactPCI® • Board size: 100mm x 160mm • Single slot (4HP, 20.32mm); Dual slot (8HP, 40.64mm); Triple slot (12HP, 60.96 mm) • CompactPCI® with HM type J1 connector, UHM type J2 connector
Processor	• 6-core Intel® Xeon® E-2276ME Processor 2.8GHz, 4.5GHz Turbo, 12M cache, 45W (35W by cTDP) • 6-core Intel® Xeon® E-2276ML Processor 2GHz, 4.2GHz Turbo, 12M cache, 25W • 6-core Intel® Core™ i7-9850HE Processor 2.7GHz, 4.4GHz Turbo, 9M cache, 45W (35W by cTDP) • 6-core Intel® Core™ i7-9850HL Processor 1.9GHz, 4.1GHz Turbo, 9M cache, 25W • 4-core Intel® Core™ i5-8400H Processor 2.5GHz, 4.2GHz Turbo, 8M cache, 45W (35W by cTDP) • 4-core Intel® Core™ i3-9100HL Processor 1.6GHz, 2.9GHz Turbo, 6M cache, 25W • Passive heatsink
Chipset	• Mobile Intel® CM246 Chipset
Memory	• Dual channel DDR4-2666 SDRAM ECC soldered, up to 32GB • DRAM configuration 32GB/16GB/8GB
CompactPCI Bus	• PCI 32-bit 33/66MHz; 3.3V, 5V universal V(IO) • Supports operation in system slot as master or in peripheral slot as standalone blade without connectivity to CompactPCI bus (Satellite mode)
Gigabit Ethernet	• One PCIe x1 Intel® I219LM GbE PHY and three PCIe x1 Intel® Ethernet Controllers I210IT • Two egress 10/100/1000BASE-T ports on faceplate, one supporting Intel® AMT by I219LM • Two egress 10/100/1000BASE-T ports routed to rear transition module • Two additional egress 10/100/1000BASE-T ports on faceplate (cPCI-3520L and cPCI-3520T)

Table 2-1: cPCI-3520 Processor Blade Specifications

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Graphics	• Integrated on Intel® Core™ processor • DVI-I port on faceplate, VGA switchable to J2 (RTM) by BIOS setting • Analog monitor support up to QXGA 2048x1536 @75Hz, 32-bit • Two DisplayPorts on faceplate with resolution up to 2560x1440 @60Hz (cPCI-3520G only) • Up to three independent displays
USB	Front: • 4HP: 1x USB 3.1 Gen2 Type A port • 8HP: Up to two USB 2.0 on riser card • (cPCI-3520D/P: 1x USB 3.1 Gen2 + 2x USB 2.0) • (cPCI-3520G: 1x USB 3.1 Gen2 + 1x USB 2.0) • (cPCI-3520L: 1x USB 3.1 Gen2 + 1x USB 2.0) Rear: • Up to 3x USB2.0
Serial Ports	Front: • 4HP: no serial port • 8HP: 1x RS-232/422/485 • One RS-232/422/485 serial port on 8HP faceplate (cPCI-3520D/L/P: 1x DB-9 COM, cPCI-3520G: 1x RJ-45 COM) • Additional RS-232 10-pin header on layer-2 board (cPCI-3520G only) Rear: • 1x Tx/Rx to J2
PMC/XMC	One 32-bit/66MHz PMC site or PCIe x1 XMC site if PMC/XMC daughter board is installed
Audio	Line-in/Line-out on faceplate by Realtek ALC262 High Definition Audio codec (cPCI-3520D only)
GPIO	3x GPIO signals from chipset: GPP_E0, GPP_E1 and GPP_E2
TPM	TPM 2.0
Storage Interfaces[1]	• CFast or mSATA socket on daughter board • Optional onboard SSD on daughter board • One SATA 6Gb/s direct connector for 2.5" SATA drive (8HP/12HP version only)
BIOS	• AMI® UEFI BIOS, SPI flash memory
OS Compatibility	• Microsoft Windows 10 IOT Enterprise 64-bit • VxWorks 7.0 • Other OS support upon request

Table 2-1: cPCI-3520 Processor Blade Specifications

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Environmental	• Operating Temperature (with forced air flow)[2]: Standard: -20°C to 70°C Extreme temperature: -40°C to +85°C • Storage Temperature: -50°C to 100°C • Humidity: 95% @60°C non-condensing • Shock: 20G peak-to-peak, 11ms duration, non-operating • Vibration[3]: 2Grms, 5-500Hz, each axis, operating (w/o hard drive)
Safety & EMI	• CE/FCC
Faceplate I/O	**4HP cPCI-3520** • 1x USB 3.0 ports • 2x 10/100/1000BASE-T Ethernet ports • 1x DVI-I port **8HP cPCI-3520D** • 1x USB 3.0 ports • 2x 10/100/1000BASE-T Ethernet ports • 1x DVI-I port • 2x USB 2.0 ports • DB-9 RS-232/422/485/485+ port • PS/2 Keyboard/Mouse combo port • Line-in and Line-out port **8HP cPCI-3520G** • 1x USB 3.0 ports • 2x 10/100/1000BASE-T Ethernet ports • 1x DVI-I port • 2x DisplayPort • 1x USB 2.0 ports • RJ-45 RS-232/422/485 port • PS/2 Keyboard/ Mouse combo port **8HP cPCI-3520L** • 1x USB 3.0 ports • 1x DVI-I port • 4x 10/100/1000BASE-T Ethernet ports • 1x USB 2.0 ports • DB-9 RS-232/422/485 port **8HP cPCI-3520M** • 1x USB 3.0 ports • 1x DVI-I port • 2x 10/100/1000BASE-T Ethernet ports • 1x 100-pin connector supports 2x DVI-D, Line-in/Line-out, 2x USB 2.0, 2x RS-232/422/485 COM, 1x KB/MS

Table 2-1: cPCI-3520 Processor Blade Specifications

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Faceplate I/O (cont'd)	**8HP cPCI-3520S** • 1x USB 3.0 ports • 2x 10/100/1000BASE-T Ethernet ports • 1x DVI-I port • PMC/XMC site
	8HP cPCI-3520T • 1x USB 3.0 ports • 1x DVI-I port • 4x 10/100/1000BASE-T Ethernet ports (2x RJ-45, 2x M12) • DB-9 RS-232/422/485 port
	12HP cPCI-3520P • 1x USB 3.0 ports • 2x 10/100/1000BASE-T Ethernet ports • 1x DVI-I port • 2x USB 2.0 ports • DB-9 RS-232/422/485/485+ port • PS/2 Keyboard/Mouse combo port • Line-in and Line-out port • PMC/XMC site

Table 2-1: cPCI-3520 Processor Blade Specifications

1. The storage device limits the operational vibration tolerance. When the application requires higher specification for anti-vibration, it is recommended to use a flash storage device.
2. ADLINK-certified thermal design. The thermal performance is dependent on the chassis cooling design. Sufficient forced air-flow is required. Temperature limits of optional mass storage devices may also affect the thermal specification.

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2.2 cPCI-R3P00(T) RTM Specifications

Mechanical	Board Size • cPCI-R3P00: 100mm x 50mm • cPCI-R3P00T: 100mm x 80mm Dual-slot (8HP, 40.64mm) (optional single slot upon request)
Gigabit Ethernet	• cPCI-R3P00: Two GbE ports switched from cPCI-3520 2x Intel® Ethernet Controllers I210 • cPCI-R3P00T: Two GbE ports from independent Intel® 82580DB GbE controller
Serial Ports	• Two serial ports on I/O panel from pin header • One port converted from USB supporting RS-232/422/485 • One port provides Tx, Rx signals only
Storage Interfaces	• Three 7-pin Serial ATA ports
Faceplate I/O	• 2x USB 2.0 ports • 2x 10/100/1000BASE-T Ethernet ports • Analog DB-15 VGA port • 2x COM ports

Table 2-2: cPCI-R3P00(T) RTM Specifications


NOTE:

Specifications are subject to change without prior notice.

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2.3 Block Diagrams

cPCI-3520 Processor Blade

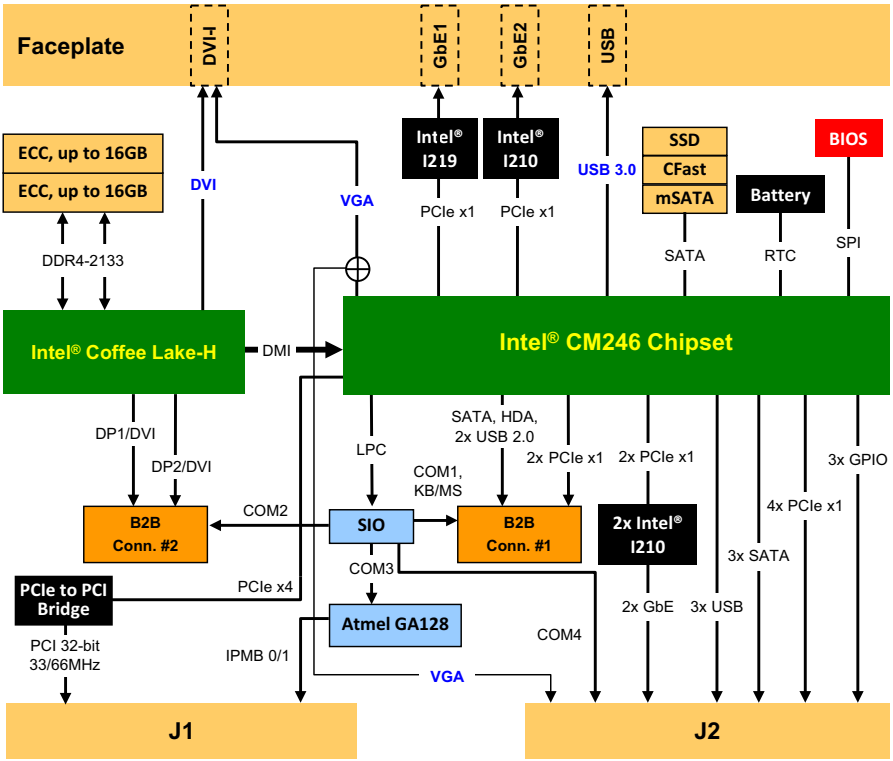


Figure 2-1: cPCI-3520 Processor Blade Functional Block Diagram

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cPCI-3520D Daughter Board (DB-3610L2)

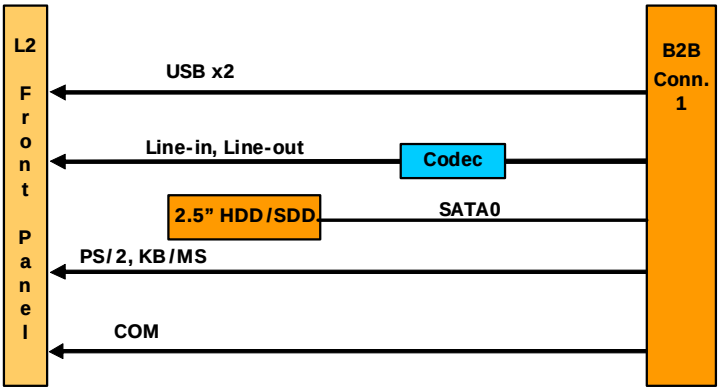


Figure 2-2: cPCI-3520D Daughter Board Functional Block Diagram

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cPCI-3520G Daughter Board (DB-3970L2)

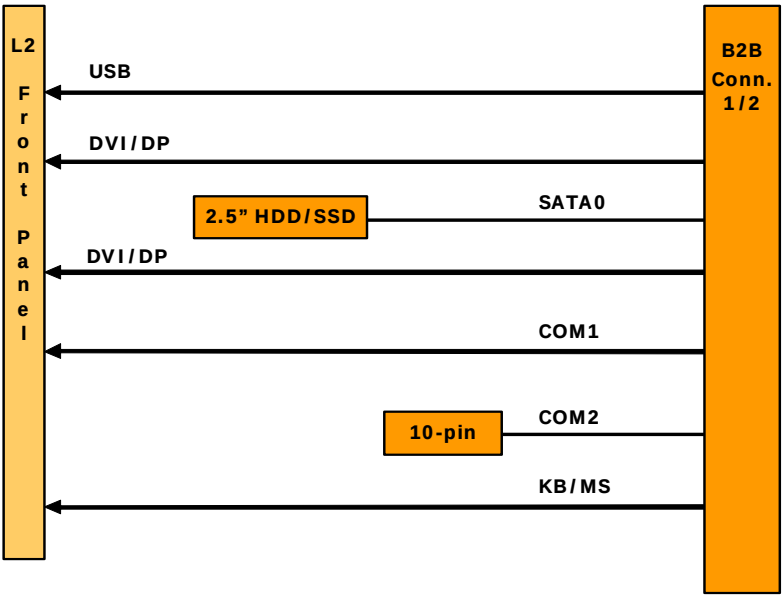


Figure 2-3: cPCI-3520G Daughter Board Functional Block Diagram

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cPCI-3520L Daughter Board (DB-LAN2-S)

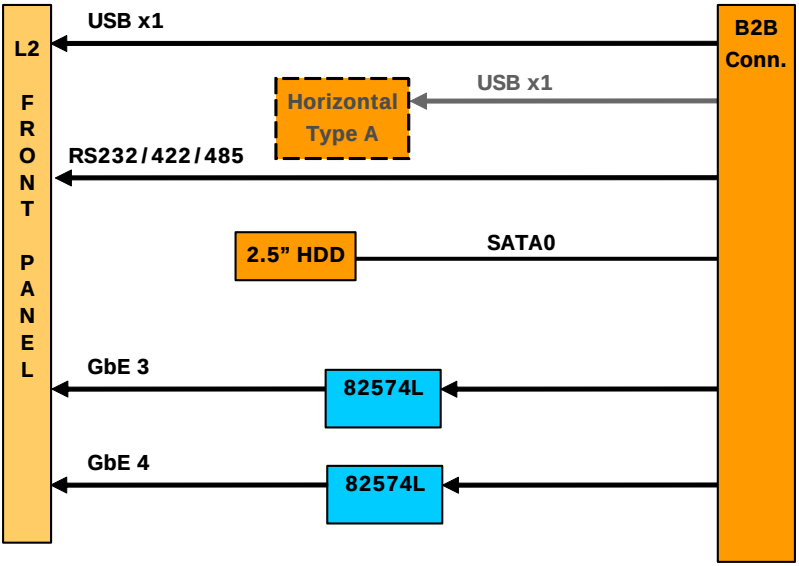


Figure 2-4: cPCI-3520L Daughter Board Functional Block Diagram

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cPCI-3520M Daughter Board (DB-Max)

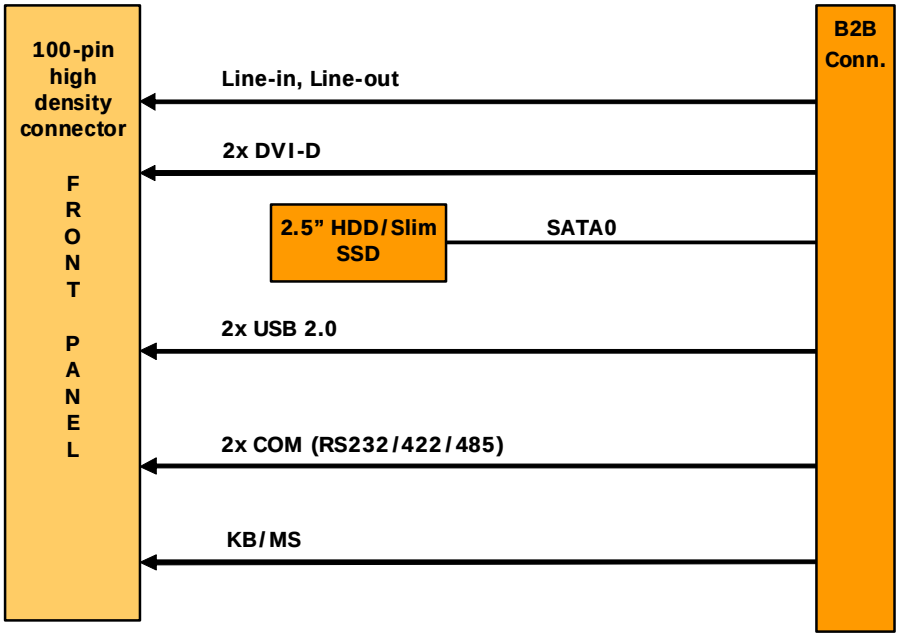


Figure 2-5: cPCI-3520M Daughter Board Functional Block Diagram

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cPCI-R3P00 RTM

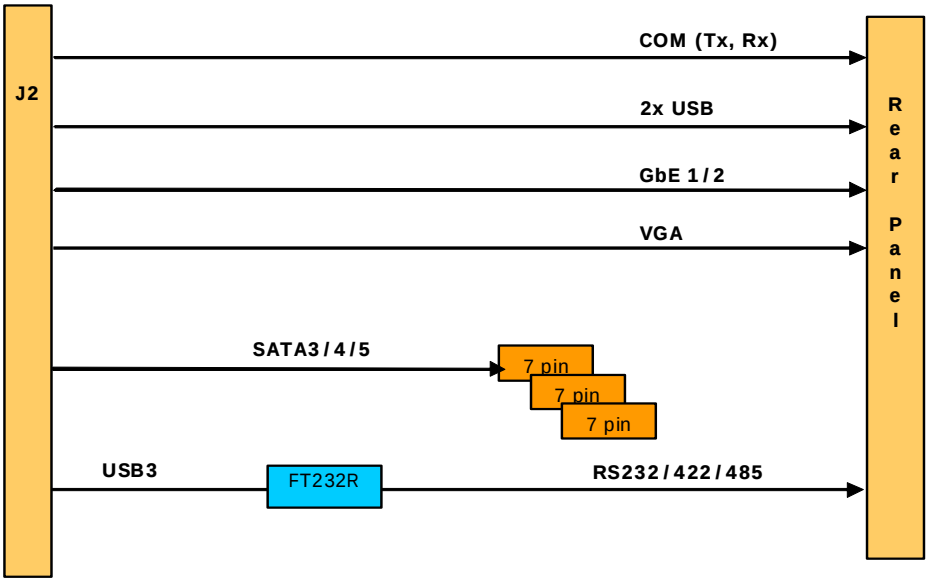


Figure 2-6: cPCI-R3P00 RTM Functional Block Diagram

cPCI-R3P00T RTM

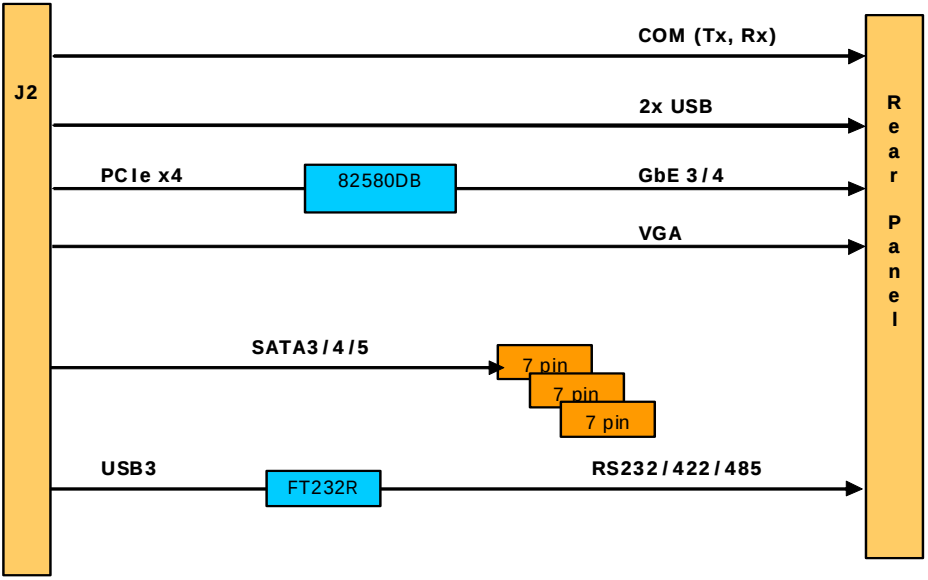


Figure 2-7: cPCI-R3P00T RTM Functional Block Diagram

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2.4 I/O Connectivity Table

Function	cPCI-3520 (4HP)		cPCI-3520D (8HP)		cPCI-3520G (8HP)		cPCI-3520L (8HP)	
	Faceplate	Onboard	Faceplate	Onboard	Faceplate	Onboard	Faceplate	Onboard
GbE	2 (RJ-45)		2 (RJ-45)		2 (RJ-45)		4 (RJ-45)	
USB	1 (3.0)		1 (3.0) 2 (2.0)		1 (3.0) 1 (2.0)		1 (3.0) 1 (2.0)	
COM			1 (DB9)		1 (RJ-45)	1 (10-pin)	1(DB9)	
Display	1 (DVI-I)		1 (DVI-I)		1 (DVI-I) 2 (DP)		1 (DVI-I)	
KB/MS	Y		Y		1			
Storage		1 CFast		1 SATA 1 CFast		1 SATA 1 CFast		1 SATA 1 CFast
Onboard SSD		optional[1]		optional[1]		optional[1]		optional[1]
Audio			Line-in Line-out					
PMC/XM								

Table 2-3: cPCI-3520 I/O Connectivity

1. Available by replacing CFast or mSATA socket adapter board with onboard SSD adapter board.

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Function	cPCI-3520M (8HP)		cPCI-3520S (8HP)		cPCI-3520T (8HP)		cPCI-3520P (12HP)	
	Faceplate	Onboard	Faceplate	Onboard	Faceplate	Onboard	Faceplate	Onboard
GbE	2 (RJ-45)		2 (RJ-45)		2 (RJ-45) 2(M12)		2 (RJ-45)	
USB	1 (3.0) 2 (2.0)		1 (3.0)		1 (3.0)		1 (3.0) 2 (2.0)	
COM	2 (DB9)				1 (DB9)		1 (DB9)	
Display	1 (DVI-I) 2 (DVI-D)		1 (DVI-I)		1 (DVI-I)		1 (DVI-I)	
KB/MS					1		1	
Storage		1 SATA 1 CFast				1 SATA 1 CFast		1 SATA 1 CFast
Onboard SSD		optional[1]				optional[1,2]		
Audio	Line-in Line-out				Line-in Line-out		Line-in Line-out	
PMC/XMC				1		1		1

Table 2-3: cPCI-3520 I/O Connectivity (cont'd)

1. Available by replacing CFast or mSATA socket adapter board with onboard SSD adapter board.
2. When select cPCI-3520T with mSATA daughter board, strongly recommend to pre-installed mSATA module during production.

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Function	R3P00(T) (RTM)	
	Faceplate	Onboard
GbE	2 (RJ-45)[1]	
USB	2 (2.0)	
COM	2 (DB9)	
Display	1 (VGA)[2]	
KB/MS		
Storage		3 SATA
Onboard SSD		
Audio		
PMC/XMC		

Table 2-4: R3P00(T) RTM I/O Connectivity

1. Routed from CPU blade faceplate for cPCI-R3P00; independent of CPU blade for cPCI-R3P00T (GbE controller onboard).
2. VGA switched from faceplate.

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2.5 Power Requirements

In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. **An industrial power supply unit should be able to provide at least twice as much power as the entire system requires of each voltage**. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires of each voltage.

The tolerance of the voltage lines described in the CompactPCI specification (PICMG 2.0 R3.0) is +5%/-3% for 5, 3.3 V and ±5% for ±12V. This specification is for power delivered to each slot and it includes both the power supply and the backplane tolerance.

Voltage	Nominal Value	Tolerance	Max. Ripple (P - P)
5V	+5.0 VDC	+5% / -3%	50 mV
3.3V	+3.3 VDC	+5% / -3%	50 mV
+12V	+12 VDC	+5% / -5%	240 mV
-12V	-12 VDC	+5% / -5%	240 mV
V I/O (PCI I/O Buffer Voltage)	+3.3 VDC or +5 VDC	+5% / -3%	50 mV
GND			

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Power Consumption

This section provides information on the power consumption of cPCI-3520 Series when using the Intel® Core™ i7 and Intel® Xeon® E processors with 32GB DDR4-2666 SO-DIMM memory and 500GB SATA SSD. The cPCI-3520 is powered by +5 V and +3.3V.

Intel® Core™ i7-9850HE			
OS/Mode	**Current 5V**	**Current 3.3V**	**Total Power**
Windows 10 x64 Idle Mode[1]	1.48A	1.72A	13.076W
Windows 10 x64 Typical Mode[2]	7.42A	1.77A	42.941W
Windows 10 x64 Maximum Mode[3]	6.52A	1.76A	38.408W

Intel® Xeon E-2276ML			
OS/Mode	**Current 5V**	**Current 3.3V**	**Total Power**
Windows 10 x64 Idle Mode[1]	2.47A	2.58A	20.86W
Windows 10 x64 Typical Mode[2]	6.34A	2.65A	40.45W
Windows 10 x64 Maximum Mode[3]	6.34A	2.64A	40.41W

Notes:

1. The system set to idle mode and stays idle for 10 minutes.
2. Run BurnInTest™ that includes CPU, memory, video and 2D/3D graphics. Set all test items to 100% loading and run for 10 minutes.
3. Run Intel® Thermal Analysis Tool that includes CPU, graphics and memory. Set all test items to 100% loading and run for 10 minutes.

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3 Functional Description

The following sections describe the cPCI-3520 Series features and functions.

3.1 Processors

The Mobile 8th/9th Generation Intel® Core™ Processor Family, and Intel® Xeon® E Processor are 64-bit, multi-core mobile processor built on 14 nanometer process technology. The processor is designed for a two-chip platform consisting of a processor and chip-set. The platform enables higher performance, lower cost, easier validation, and improved x-y footprint. The processor includes an Integrated Display Engine, Processor Graphics and Integrated Memory Controller.

The cPCI-3520 Series supports Intel® Core™ i7/i5/i3 and Xeon® E processors. The table below lists the general specifications and power ratings of the CPUs supported by the cPCI-3520 Series.

Features	Xeon® E-2276ME	Xeon® E-2276ML	Core™ i7-9850HE	Core™ i7-9850HL	Core™ i5-8400H	Core™ i3-9100HL
Clock	2.8GHz	2.0GHz	2.7GHz	1.9GHz	2.5GHz	1.6GHz
Max. Single Core Turbo Freq.	4.5GHz	4.2GHz	4.4GHz	4.1GHz	4.2GHz	2.9GHz
Last Level Cache	12MB	12MB	9MB	9MB	8MB	6MB
No. of Cores/Threads	6/12	6/12	6/12	6/12	4/8	4/4
Max. Power (TDP[1])	45W	25W	45W	25W	45W	25W
DMI	8 GT/s	8 GT/s	8 GT/s	8 GT/s	8 GT/s	8 GT/s
$T_{junction, MAX}$[2]	100°C	100°C	100°C	100°C	100°C	100°C

1. The highest expected sustainable power while running known power intensive applications. TDP is not the maximum power that the processor can dissipate.
2. The maximum temperature allowed at the processor die.

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Supported Technologies

Features	Xeon® E-2276ME Xeon® E-2276ML Core™ i7- 9850HL Core™ i7- 9850HL Core™ i5- 8400H Core™ i3- 9100HL
Intel® Virtualization Technology for Directed I/O (Intel® VT-d)	Yes
Intel® Virtualization Technology (Intel® VT-x)	Yes
Intel® VT-x with Extended Page Tables (EPT)	Yes
Intel® Hyper-Threading Technology	Yes
Intel® 64 Architecture	Yes
Execute Disable Bit	Yes
Intel® Turbo Boost Technology	2.0
Intel® vPro Technology	Yes
Enhanced Intel SpeedStep® Technology	Yes
Thermal Monitoring Technologies	Yes
Intel® Identity Protection Technology	Yes

Interfaces

- Two channels of DDR4-2666 memory
- Theoretical maximum memory bandwidth of
  - 37.5 GB/s in dual-channel mode assuming 2400 MT/s
  - 41.6 GB/s in dual-channel mode assuming 2666 MT/s
- 64-bit wide channels
- DDR4 I/O voltage of 1.2V
- Standard 4-Gb, 8-Gb technologies and addressing are supported for x8 and x16 devices, 16-Gb technologies and addressing supported for x8 device.
- PCI Express ports are fully-compliant with the PCI Express Base Specification, Revision 3.0.
- 8 GT/s point-to-point DMI interface to Chipset is supported

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3.2 Chipset

The Mobile Intel® C240 Series Chipset provides extensive I/O support. Functions and capabilities include:

- PCI Express Base Specification, Revision 3.0
- ACPI Power Management Logic Support, Revision 4.0a
- Interrupt controller and timer functions
- Integrated Serial ATA host controller 3.2, supports data transfer rates up to 6Gb/s on all ports
- XHCI USB 3.1 Controller
- Integrated 10/100/1000 Gigabit Ethernet MAC with System Defense
- System Management Bus (SMBus) Specification, Version 2.0 with additional support for I2C devices
- Supports Intel® High Definition Audio
- Supports Intel® Rapid Storage Technology
- Supports Intel® Virtualization Technology for Directed I/O
- Integrated Clock Controller
- Analog and Digital Display ports
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support
- Serial Peripheral Interface (SPI) support

3.3 PMC/XMC

The cPCI-3520P/S models support one PMC or XMC site for face-plate I/O expansion. The PMC site provides a maximum 32-bit/66MHz PCI bus link using a Pericom PI7C9X130 PCI-Express-to-PCI bridge and PCI-Express x1 link. The PMC site supports +3.3V signaling only. The XMC site provides a PCI Express x1 lane.

3.4 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology is a feature that allows the processor to opportunistically and automatically run faster than its rated operating core and/or render clock frequency when there is sufficient power headroom, and the product is within specified temper-

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ature and current limits. The Intel Turbo Boost Technology feature is designed to increase performance of both multi-threaded and single-threaded workloads. The processor supports a Turbo mode where the processor can use the thermal capacity associated with package and **run at power levels higher than TDP power for short durations**. This improves the system responsiveness for short, bursty usage conditions.

Turbo Mode availability is independent of the number of active cores; however, the Turbo Mode frequency is dynamic and dependent on the instantaneous application power load, the number of active cores, user configurable settings, operating environment, and system design. If the power, current, or thermal limit is reached, the processor will automatically reduce the frequency to stay with its TDP limit.

3.5 Intel® Hyper-Threading Technology

Intel® Hyper-Threading Technology allows an execution core to function as two logical processors. While some execution resources (such as caches, execution units, and buses) are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled using the BIOS and requires operating system support. Intel recommends enabling Hyper-Threading Technology with Microsoft Windows 7, Vista, and XP, and disabling Hyper-Threading Technology using the BIOS for all previous versions of Windows operating systems.

3.6 Trusted Platform Module

The cPCI-3520 is optionally equipped with an Infineon SLB 9665TT2.0 Trusted Platform Module (TPM). The TPM is a secure controller with added cryptographic functionality to provide users a secure environment in e-commerce transactions and Internet communications.

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The key features the Trusted Platform Module (TPM) offers are:

- Compliant to TPM 2.0 Rev. 01.16
- Pin compatible to SLB9660
- Low Pin Count (LPC) to allow easy system integration
- TCG and Common Criteria certified with EAL4+
- FIPS 140-2 certified FW available via FW update
- Full personalization with Endorsement Key (EK) and EK certificate
- 1280 byte I/O buffer

3.7 Battery

The cPCI-3520 is equipped with a 3.0V "coin cell" lithium battery for the Real Time Clock (RTC). The battery socket is equipped on the storage carrier daughter board. The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. A Rayovac BR2032 is equipped on board by default, and can be optionally equipped with a Gold Capacitor (Panasonic EECS5R5H105).

3.8 Watchdog Timer

The watchdog timer function on the cPCI-3520 is supported by IPMI commands. Please refer to Section 8.2 “Summary of Commands Supported by BMR-AVR-cPCI” on page 111.

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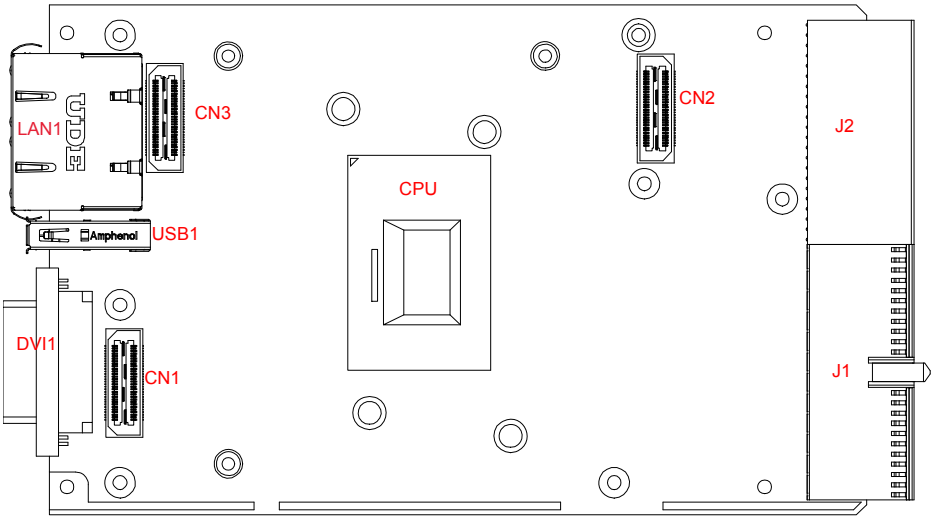
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4 Board Interfaces

This chapter illustrates the board layout, connector pin assignments, and jumper settings to familiarize users with the cPCI-3520 Series.

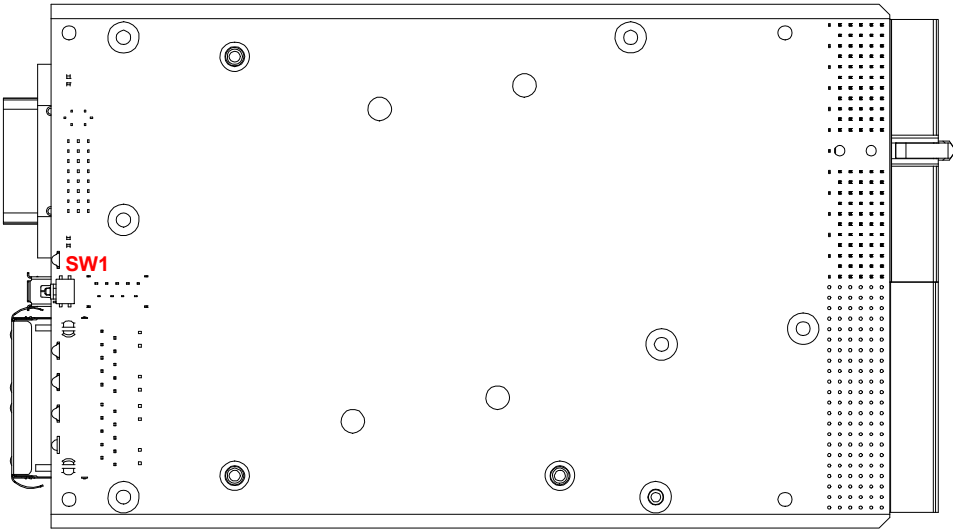
4.1 cPCI-3520 Series Board Layout



CPU	Intel® Core™ Processor	**J1**	CompactPCI connector J1
CN1	Layer-2 daughter board connector	**J2**	CompactPCI connector J2 (UHM/HM)
CN2	Storage daughter board connector	**LAN1**	Dual Ethernet connectors
CN3	cPCI-3520G daughter board connector	**USB1**	USB port
DVI1	DVI connector		

Figure 4-1: cPCI-3520 Series Board Layout (component side)

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SW1	Reset Button

Figure 4-2: cPCI-3520 Series Board Layout (solder side)

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4.2 cPCI-3520 Blade Assembly Layout

This section describes the final assembly layout of the single slot cPCI-3520 Blade.

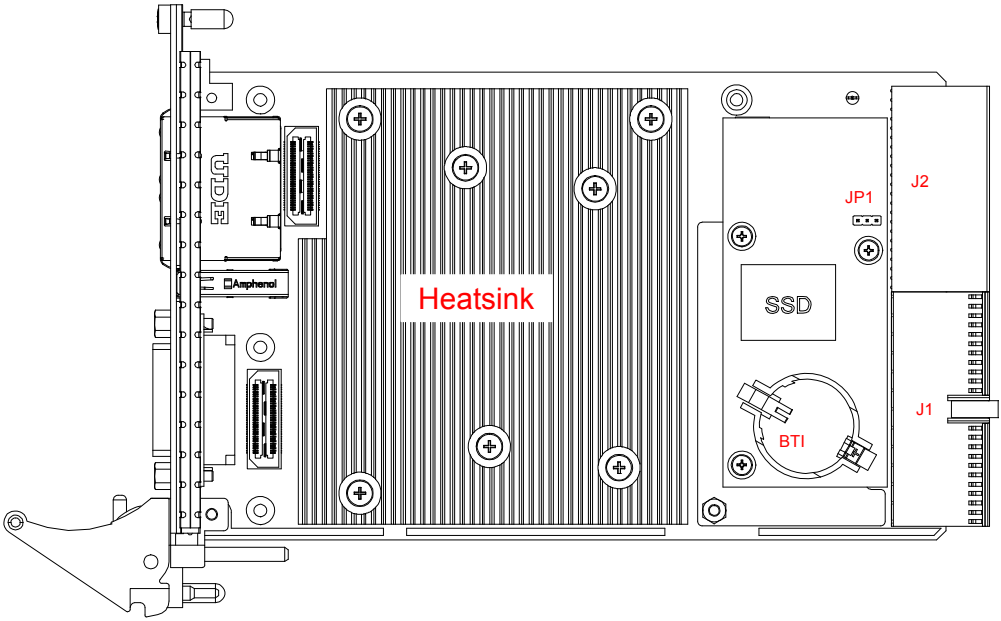


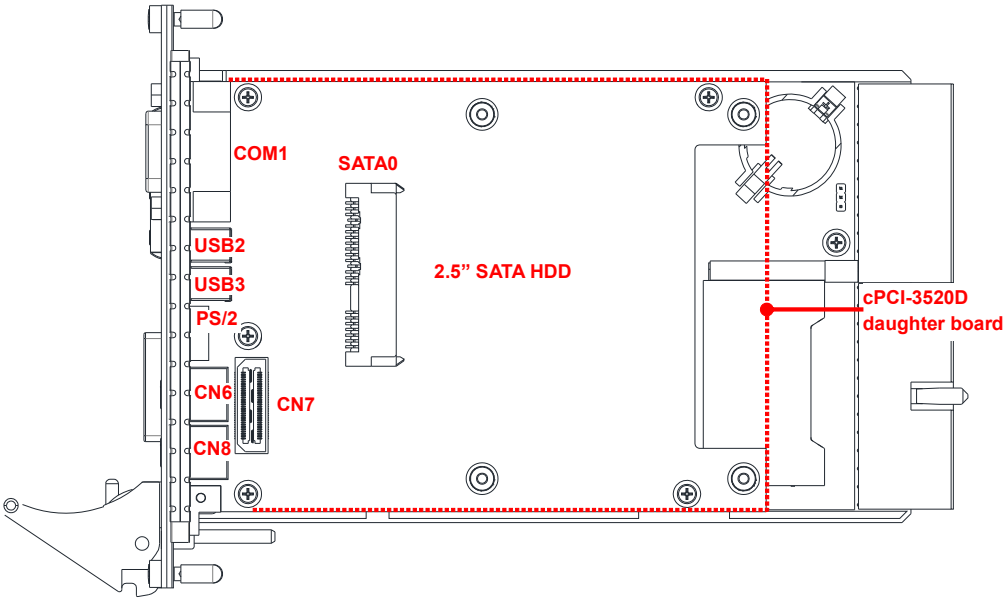
Figure 4-3: cPCI-3520 Blade Assembly Layout

BT1	Battery	**J1**	CompactPCI connector J1
JP1	Clear CMOS jumper	**J2**	CompactPCI connector J2

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4.3 cPCI-3520D Blade Assembly Layout

The dual-slot width cPCI-3520D Blade is comprised of the cPCI-3520 single-slot main board and the cPCI-3520D daughter board to expand I/O connectivity with PS/2, COM, 2x USB ports, Line-in, and Line-out ports .



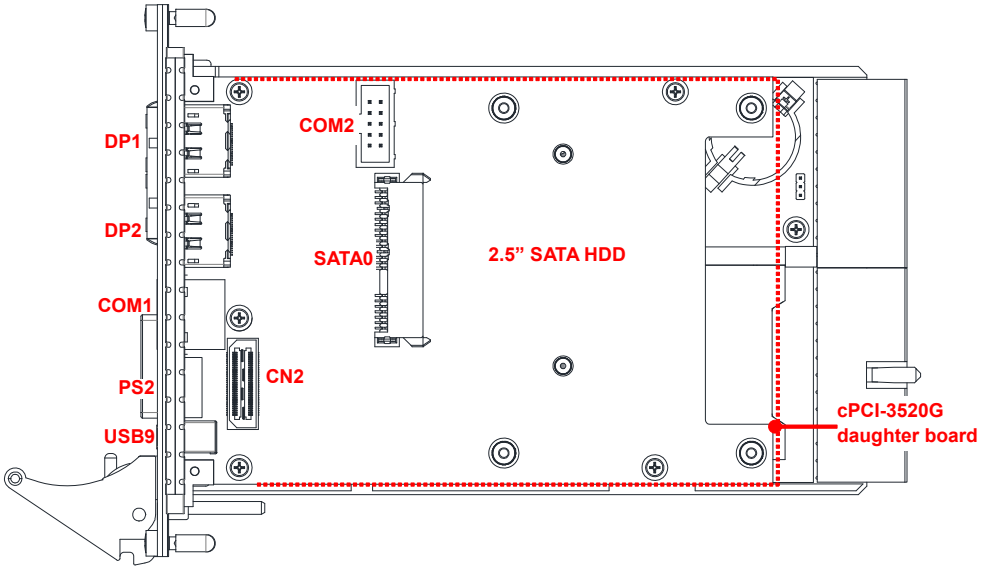
COM1	DB-9 COM port	**CN7**	Layer-2 daughter board connector
USB2/3	USB connectors	**CN6**	Line-in port
PS2	PS/2 KB/Ms combo port	**CN8**	Line-out port
SATA0	22-pin SATA connector		

Figure 4-4: cPCI-3520D Blade Assembly Layout

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4.4 cPCI-3520G Blade Assembly Layout

The dual-slot width cPCI-3520G Blade is comprised of the cPCI-3520 single-slot main board and the cPCI-3520G daughter board to expand I/O connectivity with PS/2, COM, USB ports, and 2x DisplayPorts.



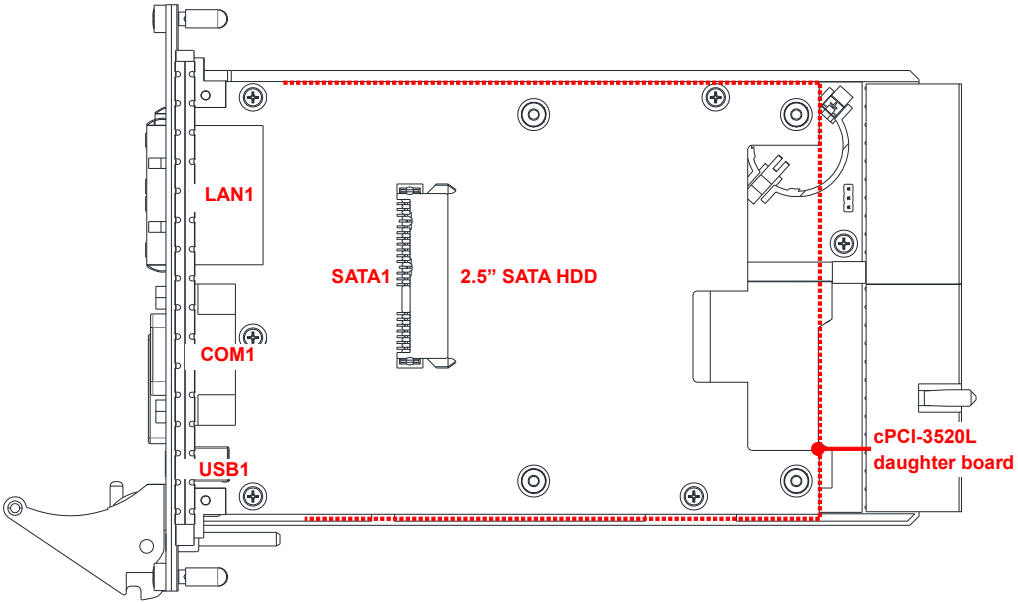
COM1	RJ-45 COM port	**CN2**	Layer-2 daughter board connector
COM2	10-pin COM port	**DP1/2**	DisplayPort connectors
USB9	USB connector	**PS2**	PS/2 KB/MS combo port
SATA0	22-pin SATA connector		

Figure 4-5: cPCI-3520G Blade Assembly Layout

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4.5 cPCI-3520L Blade Assembly Layout

The dual-slot width cPCI-3520L Blade is comprised of the cPCI-3520 single-slot main board and the cPCI-3520L daughter board, expanding I/O connectivity with 2x LAN, COM, USB.



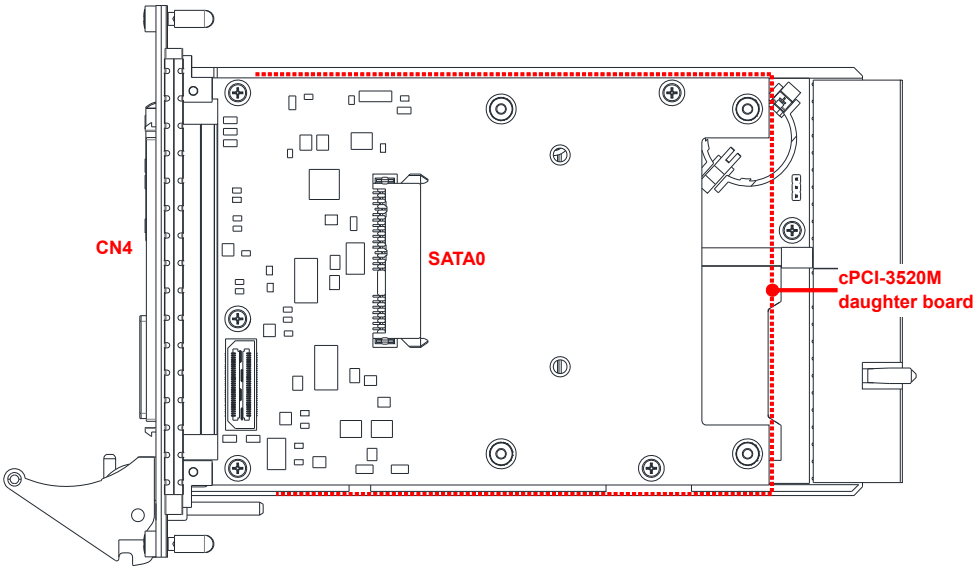
LAN1	GbE RJ-45 ports	**USB1**	USB connector
COM1	DB-9 COM port	**SATA1**	22-pin SATA connector

Figure 4-6: cPCI-3520L Blade Assembly Layout

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4.6 cPCI-3520M Blade Assembly Layout

The dual-slot width cPCI-3520M Blade is comprised of the cPCI-3520 single-slot main board and the cPCI-3520M daughter board, expanding I/O connectivity with a 100-pin high density connector.



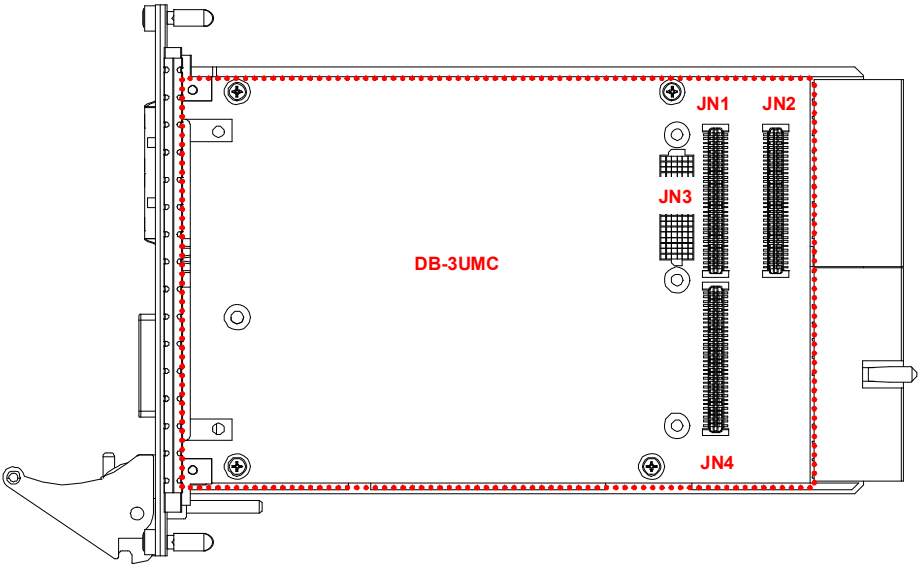
CN4	100-pin high density connector	**SATA0**	22-pin SATA connector

Figure 4-7: cPCI-3520M Blade Assembly Layout

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4.7 cPCI-3520S Blade Assembly Layout

The dual-slot width cPCI-3520S Blade is comprised of the cPCI-3520 single-slot main board and the DB-3UMC riser card, expanding I/O connectivity with a XMC/PMC connector.

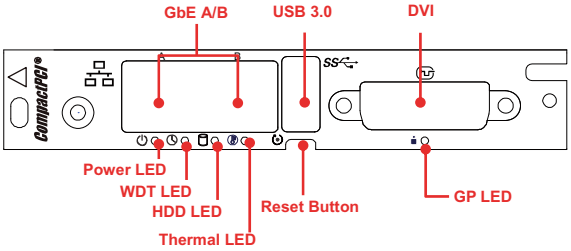


JN3	XMC connector	**JN1/JN2/JN4**	PCM connectors

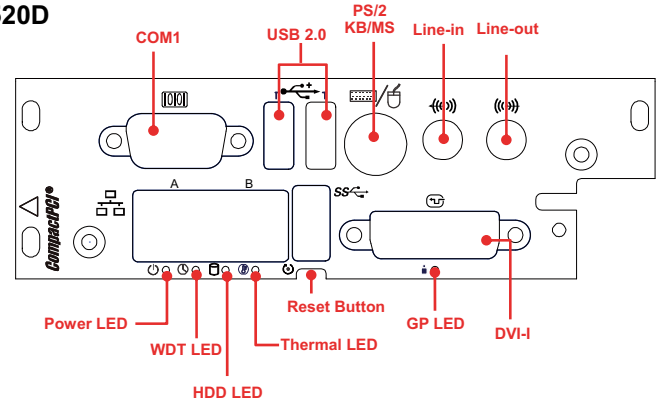
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4.8 cPCI-3520 Series Faceplate Layout

cPCI-3520



cPCI-3520D



cPCI-3520G

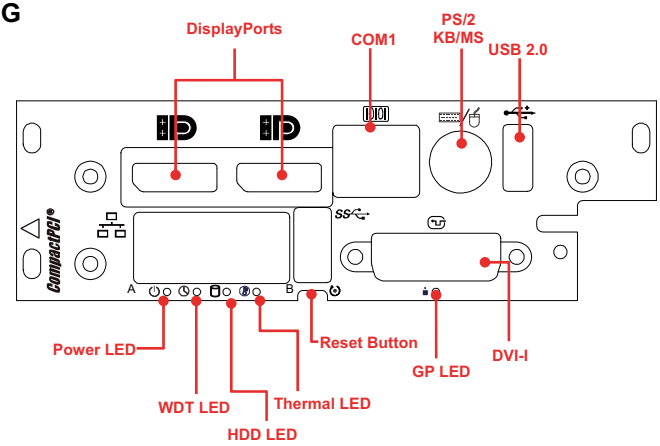
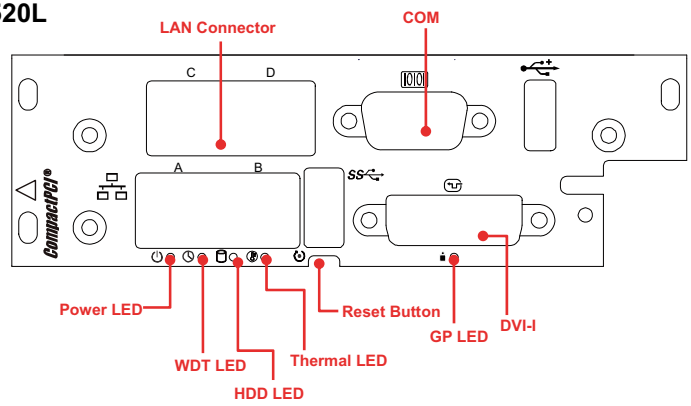


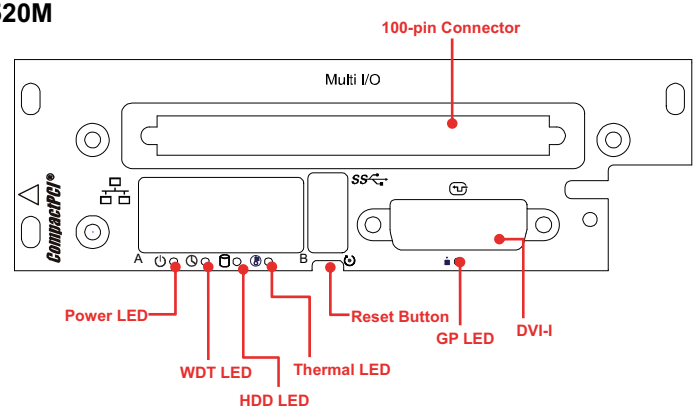
Figure 4-8: cPCI-3520/D/G Faceplate Layout

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cPCI-3520L



cPCI-3520M



cPCI-3520S

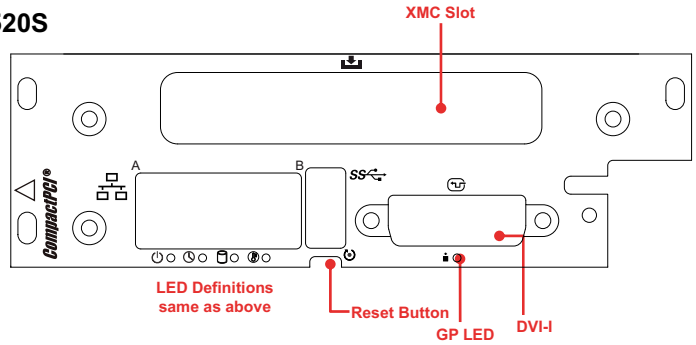


Figure 4-9: cPCI-3520L/M/S Faceplate Layout

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cPCI-3520P: Same faceplate as cPCI-3520D but with XMC/PMC slot on Layer 3.

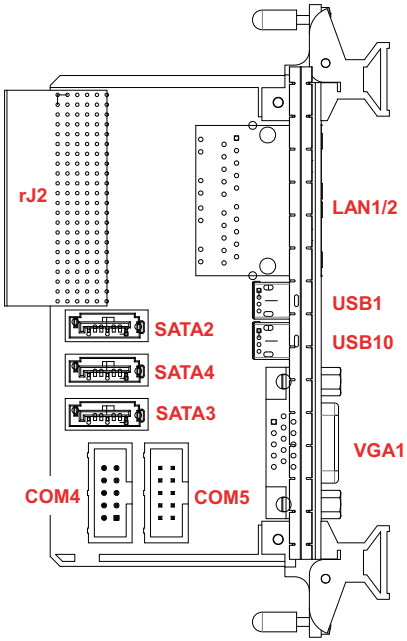
System LEDs

LED	Color	Condition	Indication
Power 	Green/ Red	OFF	System is off
		Red	System Power ready (PWGD)
		Green	Post OK
WDT 	Orange	OFF	No Watchdog event
		Blinking	Watchdog event alert
Drive 	Blue	OFF	No CF/CFast/mSATA/SATA activity
		Blinking	Data read/write in process for CF/CFast/ mSATA/SATA drive
Overheat 	Red	OFF	CPU $T_{junction}$ temperature is under 100ºC
		ON	CPU $T_{junction}$ temperature exceeds 100ºC
GP (General Purpose) 	Yellow	OFF	No activity
		ON/Blinking	Defined by user

Table 4-1: cPCI-3520 Faceplate System LED Descriptions

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4.9 cPCI-R3P00(T) RTM Board Layout



COM5*	RS-232/422/485 port (converted from USB)	**LAN1/2**	Dual Ethernet ports
COM4	RS-232 port (Tx, Rx only)	**VGA1**	VGA port
SATA2/3/4	SATA ports	**USB1/10**	USB ports
rJ2	CompactPCI connector		

(cPCI-R3P00 is 50mm deep and cPCI-R3P00T is 80mm deep)

Figure 4-10: cPCI-R3P00(T) RTM Board Layout

NOTE:

*COM5 is incorrectly labeled COM3 on the A1 vers. PCB silkscreen.

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4.10 cPCI-R3P00(T) RTM Faceplate

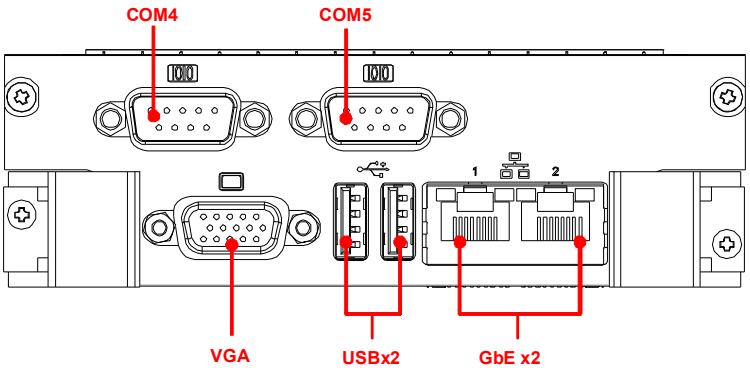


Figure 4-11: cPCI-R3P00(T) RTM Faceplate

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4.11 Connector Pin Assignments

USB 2.0 Connectors

Pin #	Signal Name
1	Vcc
2	UV0-
3	UV0+
4	GND

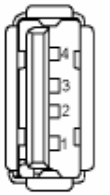
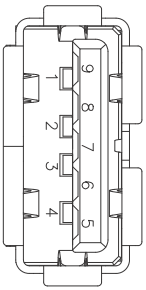


Table 4-2: USB 2.0 Pin Definition

USB 3.0 Connectors

Pin #	Signal Name
1	USB3.0_P5VA
2	USB2_CMAN
3	USB2_CMAP
4	GND
5	USB3A_CMRXN
6	USB3A_CMRXP
7	GND
8	USB3A_CMTXN
9	USB3A_CMTXP



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DB-15 VGA Connector

Signal Name	Pin #	Pin #	Signal Name
Red	1	2	Green
Blue	3	4	N.C.
GND	5	6	GND
GND	7	8	GND
+5V.	9	10	GND
N.C.	11	12	CRTDATA
HSYNC	13	14	VSYNC
CRTCLK	15		

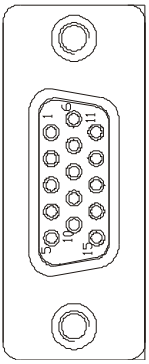


Table 4-3: VGA Pin Definition

DisplayPort Connectors

Pin #	Signal	Pin #	Signal
1	CN_DP0_P	2	Ground
3	CN_DP0_N	4	CN_DP1_P
5	Ground	6	CN_DP1_N
7	CN_DP2_P	8	Ground
9	CN_DP2_N	10	CN_DP3_P
11	Ground	12	CN_DP3_N
13	CN_CAD-L	14	CN_CEC
15	CN_AUX_P	16	Ground
17	CN_AUX_N	18	DDP_HPD
19	Ground	20	P3V3

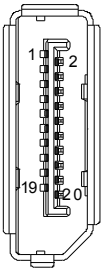
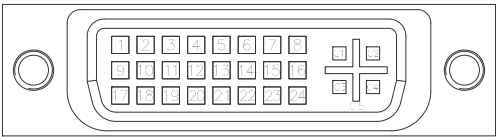


Table 4-4: DisplayPort Pin Definition

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DVI-I Connector



Pin #	Signal	Pin #	Signal
1	TMDS Data2-	16	Hot Plug Detect
2	TMDS Data2+	17	TMDS Data0-
3	GND	18	TMDSData0+
4	NC	19	GND
5	NC	20	NC
6	DDC Clock [SCL]	21	NC
7	DDC Data [SDA]	22	GND
8	Analog vertical sync	23	TMDS Clock +
9	TMDS Data1-	24	TMDS Clock -
10	TMDS Data1+	C1	Analog Red
11	GND	C2	Analog Green
12	NC	C3	Analog Blue
13	NC	C4	Analog Horizontal Sync
14	+5 V Power	C5	Analog GND Return
15	GND		

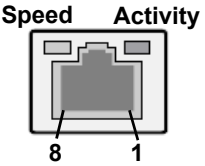
Table 4-5: DVI-I Connector Pin Definition

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RJ-45 Gigabit Ethernet Connectors

Pin #	10BASE-T/ 100BASE-TX	1000BASE-T
1	TX+	LAN_TX0+
2	TX-	LAN_TX0-
3	RX+	LAN_TX1+
4	—	LAN_TX2+
5	—	LAN_TX2-
6	RX-	LAN_TX1-
7	—	LAN_TX3+
8	—	LAN_TX3-

Table 4-6: RJ-45 GbE Pin Definitions



Status		Speed LED (Green/Orange)	Activity LED (Yellow)
Network link is not established or system powered off		OFF	OFF
10 Mbps	Link	OFF	ON
	Active	OFF	Blinking
100 Mbps	Link	Green	ON
	Active	Green	Blinking
1000 Mbps	Link	Orange	ON
	Active	Orange	Blinking

Table 4-7: LAN LED Status Definitions

NOTE: The cPCI-R3P00 RTM LAN LED signals are not passed through from the main board and are not displayed on the face-plate LAN LEDs.

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PS/2 Keyboard/Mouse Connector

Pin #	Signal	Function
1	KBDATA	Keyboard Data
2	MSDATA	Mouse Data
3	GND	Ground
4	+5V	Power
5	KBCLK	Keyboard Clock
6	MSCLK	Mouse Clock

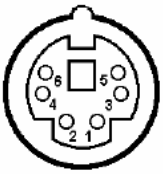


Table 4-8: PS/2 Keyboard/Mouse Pin Definition

cPCI-3520D/P Serial Ports

COM1 Connector (DB-9)

Pin #	RS-232	RS-422	RS-485(+)
1	DCD-L	TXD-	TXD-
2	RXD	TXD+	TXD+
3	TXD	RXD+	—
4	DTR-L	RXD-	—
5	GND	GND	GND
6	DSR-L	—	—
7	RTS-L	—	—
8	CTS-L	—	—
9	RI-L	—	—

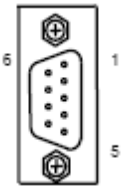


Table 4-9: cPCI-3520D/P COM1 (DB-9) Pin Definition

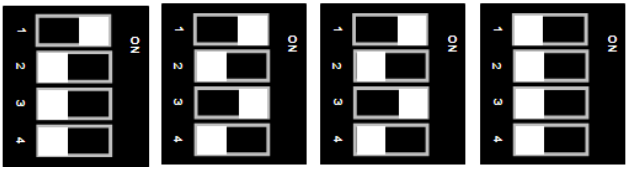
NOTE:

The COM mode setting for cPCI-3520D/P models is set using SW1~SW4. See *"COM1 Mode Selection Switches (SW1-SW4)" on page 49*.

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COM1 Mode Selection Switches (SW1-SW4)

These switches set the cPCI-3520D/P COM1 to RS-232 full modem, RS-422, RS-485, or RS-485+ half-duplex mode. Switches SW1~SW4 are located on the top edge of the cPCI-3520D daughter board. RS-232 full modem is set by default.



SW1 SW2 SW3 SW4

Mode	Pin	SW1	SW2	SW3	SW4
RS-232	1	ON	ON	ON	OFF
	2	OFF	OFF	OFF	OFF
	3	OFF	ON	ON	OFF
	4	OFF	OFF	OFF	OFF
RS-422	1	OFF	OFF	OFF	ON
	2	ON	ON	ON	OFF
	3	OFF	OFF	OFF	ON
	4	OFF	ON	ON	OFF
RS-485	1	OFF	OFF	OFF	ON
	2	OFF	ON	ON	OFF
	3	ON	OFF	OFF	ON
	4	OFF	ON	ON	OFF
RS-485+	1	OFF	OFF	OFF	OFF
	2	OFF	ON	ON	ON
	3	ON	OFF	OFF	OFF
	4	OFF	ON	ON	ON

Table 4-10: cPCI-3520D/P COM1 Mode Selection Switch Settings

NOTE:

The COM mode setting for cPCI-3520D/P models must be set using the SW1~SW4 DIP switches above. The cPCI-3520G COM1/2 Output BIOS setting is only used for cPCI-3520G models.

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cPCI-3520G Serial Ports

COM1 Connector (RJ-45)

Pin #	RS-232	RS-422	RS-485
1	DCD-L	—	—
2	RTS-L	TXD+	TXD+
3	DSR-L	—	—
4	TXD	TXD-	TXD-
5	RXD	RXD-	—
6	Ground	—	—
7	CTS-L	RXD+	—
8	DTR-L	—	—
9	RI-L	—	—

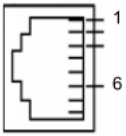


Table 4-11: cPCI-3520G COM1 (RJ-45) Pin Definition


NOTE:

The COM mode settings for cPCI-3520G models are set in the BIOS: see *"Super IO Configuration" on page 90*.

COM1 Connector with DB-9 Adapter

An RJ-45 to DB-9 adapter cable is provided to breakout the COM1 signals.

Pin #	RS-232	RS-422	RS-485
1	DCD-L	—	—
2	RXD	RXD-	—
3	TXD	TXD-	TXD-
4	DSR-L	—	—
5	Ground	—	—
6	DSR-L	—	—
7	RTS-L	TXD+	TXD+
8	CTS-L	RXD+	—
9	—	—	—

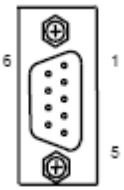


Table 4-12: cPCI-3520G COM1 (DB-9 adapter) Pin Definition

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NOTE:

The cPCI-3520G COM1 RS-422/485 pin definitions are different from the common DB-9 pin definitions. An RS-422/485 DB-9 male-female adapter dongle allows compatibility with common RS-422/485 pin definitions.

RS-422/485 Adapter Dongle for cPCI-3520G

A DB-9 male-female adapter dongle allows compatibility with common RS-422/485 pin definitions

DB-9 (Female) Signal Name	Pin #	DB-9 (Male) Signal Name
NC	1	TXD-
RXD-	2	TXD+
TXD-	3	RXD+
NC	4	RXD-
NC	5	NC
NC	6	NC
TXD+	7	NC
RXD+	8	NC
NC	9	NC

Table 4-13: RS-422/485 Adapter Dongle Pin Definition

COM1 with RS-422/485 Dongle (DB-9)

Pin #	RS-422	RS-485
1	TXD-	TXD-
2	TXD+	TXD+
3	RXD+	—
4	RXD-	—
5	—	—
6	—	—
7	—	—
8	—	—
9	—	—

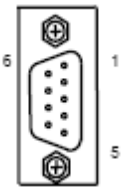


Table 4-14: cPCI-3520G COM1 with RS-422/485 Dongle Pin Definition

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COM2 Pin Header

Pin #	RS-232	RS-422	RS-485
1	DCD-L	—	—
2	DSR-L	—	—
3	RXD	RXD-	—
4	RTS-L	TXD+	TXD+
5	TXD	TXD-	TXD-
6	CTS-L	RXD+	—
7	DTR-L	—	—
8	RI-L	—	—
9	Ground	—	—
10	NC	—	—

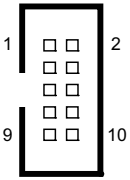


Table 4-15: cPCI-3520G COM2 Pin Header Definition

NOTE:

The COM mode settings for cPCI-3520G models are set in the BIOS: see *"Super IO Configuration" on page 90*.

cPCI-R3P00(T) RTM Serial Ports

COM4 Connector (DB-9))

Pin #	RS-232
1	—
2	RXD
3	TXD
4	—
5	GND
6	—
7	—
8	—
9	—

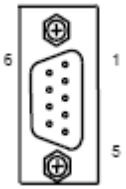


Table 4-16: cPCI-R3P00(T) RTM COM4 Pin Definition

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COM5 Connector (DB-9)

NOTE:

The cPCI-R3P00(T) RTM COM5 RS-422/485 pin definitions are different from the common DB-9 pin definitions. An RS-422/485 DB-9 male-female adapter dongle allows compatibility with common RS-422/485 pin definitions. See *"RS-422/485 Adapter Dongle for cPCI-3520G" on page 51*

Pin #	RS-232	RS-422	RS-485
1	DCD-L	—	—
2	RXD	RXD-	—
3	TXD	TXD-	TXD-
4	DTR-L	—	—
5	GND	—	—
6	DSR-L	—	—
7	RTS-L	TXD+	TXD+
8	CTS-L	RXD+	—
9	RI-L	—	—

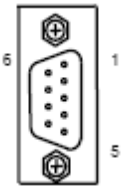


Table 4-17: cPCI-R3P00(T) RTM COM5 Pin Definition

COM5 with RS-422/485 Dongle (DB-9)

Pin #	RS-422	RS-485
1	TXD-	TXD-
2	TXD+	TXD+
3	RXD+	—
4	RXD-	—
5	—	—
6	—	—
7	—	—
8	—	—
9	—	—

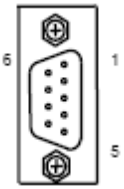


Table 4-18: cPCI-R3P00(T) RTM COM5 with RS-422/485 Dongle Pin Def'n

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cPCI-3520M 100-pin I/O Connector (CN4)

Pin #	Signal	Pin #	Signal
1	GND	2	USB9_CN-N
3	USB9_CN-P	4	GND
5	USB1_CN-N	6	USB1_CN-P
7	GND	8	GND
9	TMDS_I2C_DATA	10	TMDS_I2C_CLK
11	GND	12	TMDSB_DATA2B
13	TMDSB_DATA2	14	GND
15	TMDSB_DATA1B	16	TMDSB_DATA1
17	GND	18	TMDSB_DATA0B
19	TMDSB_DATA0	20	GND
21	TMDSB_CLKB	22	TMDSB_CLK
23	GND	24	P5V_DVI1
25	TMDSB_HPD	26	GND
27	NC	28	NC
29	GND	30	TMDS_I2C_DATA
31	TMDS_I2C_CLK	32	GND
33	TMDSB_DATA2B	34	TMDSB_DATA2
35	GND	36	TMDSB_DATA1B
37	TMDSB_DATA1	38	GND
39	TMDSB_DATA0B	40	TMDSB_DATA0
41	GND	42	TMDSB_CLKB
43	TMDSB_CLK	44	GND
45	P5V_DVI2	46	TMDSB_HPD
47	GND	48	NC
49	NC	50	GND
51	P5V_USB_1_9	52	P5V_USB_1_9
53	P5V_USB_1_9	54	P5V_USB_1_9
55	GND	56	GND
57	GND	58	P5V_KBMS
59	MSCLK_CN	60	MSDATA_CN
61	KBCLK_CN	62	KBDATA_CN

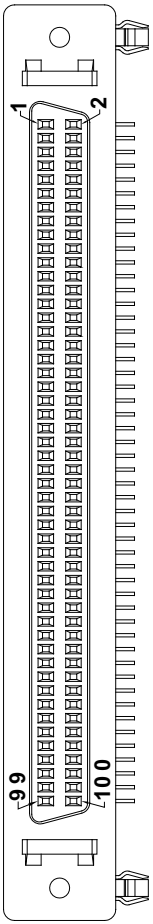


Table 4-19: cPCI-3520M 100-pin I/O Connector Pin Definition

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Pin #	Signal	Pin #	Signal
63	GND	64	GND
65	COM1_RXD_CN	66	COM1_CTS-L_CN
67	GND	68	COM1_TXD_CN
69	COM1_RTS-L_CN	70	GND
71	COM1_DTR-L_CN	72	COM1_DSR-L_CN
73	COM1_DCD-L_CN	74	GND
75	COM2_RXD_CN	76	COM2_CTS-L_CN
77	GND	78	COM2_TXD_CN
79	COM2_RTS-L_CN	80	GND
81	COM2_DTR-L_CN	82	COM2_DSR-L_CN
83	COM2_DCD-L_CN	84	AGND_AU
85	NC	86	NC
87	NC	88	NC
89	NC	90	NC
91	NC	92	AGND_AU
93	L_IN_R	94	L_IN_L
95	L_IN_JD	96	AGND_AU
97	HP_R	98	HP_L
99	HP_JD	100	AGND_AU

Table 4-19: cPCI-3520M 100-pin I/O Connector Pin Definition

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Serial ATA Connectors on RTM (CN4-R, CN5-R)

Pin #	Signal
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND



Table 4-20: Serial ATA Connector on RTM

SATA Conn. on cPCI-3520D/G/M Daughter Board

Pin #	Signal
S1	GND
S2	TX+
S3	TX-
S4	GND
S5	RX-
S6	RX+
S7	GND
P1	NC
P2	NC
P3	NC
P4	GND
P5	GND
P6	GND
P7	5V
P8	5V
P9	5V
P10	GND
P11	NC
P12	GND
P13~P15	NC

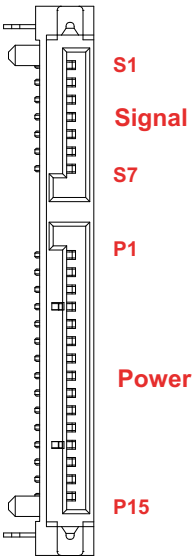


Table 4-21: SATA on cPCI-3520D/G/M Daughter Board Pin Def'n

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

CFast Socket (on CFast carrier board)

Pin #	Signal Name
Ground	S1
SATA_TX-P	S2
SATA_TX-N	S3
Ground	S4
SATA_RX-N	S5
SATA_RX-P	S6
Ground	S7
CFast_CDI	P1
Ground	P2
NC	P3
NC	P4
NC	P5
NC	P6
Ground	P7
CFast_LED1	P8
CFast_LED2	P9
NC	P10
NC	P11
NC	P12
P3V3	P13
P3V3	P14
Ground	P15
Ground	P16
CFast_CDO	P17

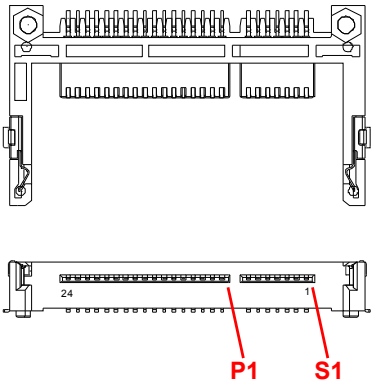


Table 4-22: CFast Socket Pin Definition

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Layer-2 Daughter Board Connector (CN1)

Signal Name	Pin #	Pin #	Signal Name
USB2-N	1	2	-12V
USB2-P	3	4	+12
GND	5	6	GND
USB3-N	7	8	HDA_SDIN0
USB3-P	9	10	HDA_R_SDOUT
GND	11	12	GND
SATA_ICH_RX-N0	13	14	HDA_R_SYNC
SATA_ICH_RX-P0	15	16	HDA_R_BIT_CLK
GND	17	18	GND
SATA_TX-P0	19	20	CK_L2_PCIE1-P
SATA_TX-N0	21	22	CK_L2_PCIE1-N
GND	23	24	GND
PCIE_TXN5	25	26	CK_L2_PCIE2-P
PCIE_TXP5	27	28	CK_L2_PCIE2-N
GND	29	30	GND
PCIE_RXN5	31	32	HDA_R_RST-L
PCIE_RXP5	33	34	SPKR
GND	35	36	L2_PCIE_RST-L
PCIE_RXN4	37	38	NC
PCIE_RXP4	39	40	USB_2_3_OC-L
GND	41	42	COM1_DCD-L
PCIE_TXN4	43	44	COM1_RI-L
PCIE_TXP4	45	46	COM1_CTS-L
GND	47	48	COM1_DTR-L
MSCLK	49	50	COM1_RTS-L
MSDATA	51	52	COM1_DSR-L
KBCLK	53	54	COM1_SOUT
KBCDATA	55	56	COM1_SIN
P5V	57	58	+3.3V
P5V	59	60	+3.3V

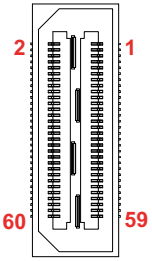


Table 4-23: Layer-2 Daughter Board Connector Pin Definition

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Storage Daughter Board Connector (CN2)

Signal Name	Pin #	Pin #	Signal Name
PCH_SPKR	1	2	CLK33_TPM
SIO_SPKR	3	4	LPC_FRAME-L
GND	5	6	TPM_RST-L
CN_VCC_RTC	7	8	LPC_AD3
GND	9	10	LPC_AD2
NC	11	12	LPC_AD1
NC	13	14	LPC_AD0
NC	15	16	TPM_LPCPD
NC	17	18	PCH_SERIRQ
NC	19	20	TPM_CLKRUN
NC	21	22	TPM_GPIO
NC	23	24	NC
NC	25	26	NC
NC	27	28	NC
NC	29	30	NC
NC	31	32	NC
NC	33	34	NC
NC	35	36	NC
GND	37	38	NC
SATA_PCH_RX-N0	39	40	NC
SATA_PCH_RX-P0	41	42	NC
GND	43	44	NC
SATA_PCH_TX-N0	45	46	NC
SATA_PCH_TX-P0	47	48	NC
GND	49	50	NC
CFast_CDI	51	52	NC
CFast_CDO	53	54	NC
GND	55	56	NC
P5V	57	58	P3V3
P5V	59	60	P3V3

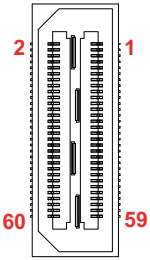


Table 4-24: Storage Daughter Board Connector Pin Definition

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

cPCI-3520G Daughter Board Connector (CN3)

Signal Name	Pin #	Pin #	Signal Name
NC	1	2	RS232_COM2_SEL-L
NC	3	4	COM2_DCD-L
NC	5	6	COM2_RI-L
NC	7	8	COM2_CTS-L
NC	9	10	COM2_DTR-L
NC	11	12	COM2_RTS-L
NC	13	14	COM2_DSR-L
NC	15	16	COM2_SOUT
NC	17	18	COM2_SIN
NC	19	20	NC
NC	21	22	NC
GND	23	24	GND
PCH_DDPD_AUXN	25	26	PCH_DDPC_AUXN
PCH_DDPD_AUXP	27	28	PCH_DDPC_AUXP
GND	29	30	GND
PCH_DDPD_0N	31	32	PCH_DDPC_0N
PCH_DDPD_0P	33	34	PCH_DDPC_0P
GND	35	36	GND
PCH_DDPD_1N	37	38	PCH_DDPC_1N
PCH_DDPD_1P	39	40	PCH_DDPC_1P
GND	41	42	GND
PCH_DDPD_2N	43	44	PCH_DDPC_2N
PCH_DDPD_2P	45	46	PCH_DDPC_2P
GND	47	48	GND
PCH_DDPD_3N	49	50	PCH_DDPC_3N
PCH_DDPD_3P	51	52	PCH_DDPC_3P
GND	53	54	GND
DDPD_CTRLCLK	55	56	DDPC_CTRLCLK
DDPD_CTRLDATA	57	58	DDPC_CTRLDATA
DDPD_HPD	59	60	DDPC_HPD

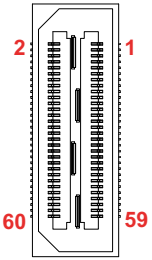


Table 4-25: cPCI-3520G Daughter Board Connector Pin Definition

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

PMC/XMC Daughter Board Connector

(on cPCI-3520D/G daughter board)

Signal Name	Pin #	Pin #	Signal Name
NC	1	2	-12V
NC	3	4	+12V
GND	5	6	GND
NC	7	8	NC
NC	9	10	NC
GND	11	12	GND
NC	13	14	NC
NC	15	16	NC
GND	17	18	GND
NC	19	20	CK_PCIE1_P
NC	21	22	CK_PCIE1_N
GND	23	24	GND
PCIE_TXN2	25	26	CK_PCIE2_P
PCIE_TXP2	27	28	CK_PCIE2_N
GND	29	30	GND
PCIE_R_RXN2	31	32	NC
PCIE_R_RXP2	33	34	NC
GND	35	36	PCIE_RST#
PCIE_R_RXN1	37	38	NC
PCIE_R_RXP1	39	40	NC
GND	41	42	NC
PCIE_TXN4	43	44	NC
PCIE_TXP4	45	46	NC
GND	47	48	NC
NC	49	50	NC
NC	51	52	NC
NC	53	54	NC
NC	55	56	NC
+5V	57	58	+3.3V
+5V	59	60	+3.3V

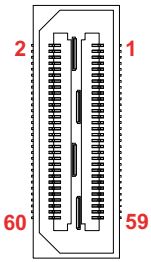


Table 4-26: PMC/XMC Daughter Board Connector Pin Definition

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PMC Connector on PMC/XMC Daughter Board (JN1/2)

Pin#	JN1 Signal	JN2 Signal
1	PMC_TCK	P12V
2	N12V	PMC_TRST-L
3	GND	PMC_TMS
4	PCIX_INTA-L	NC (PMC_TDO)
5	PCIX_INTB-L	PMC_TDI
6	PCIX_INTC-L	GND
7	PMC_MOD-L1	GND
8	P5V	NC
9	PCIX_INTD-L	NC
10	NC	NC
11	GND	PMC_MOD-L2
12	P3V3_PMCAUX	P3V3
13	CLK66_PCIX_PMC	PMC_RST-L
14	GND	PMC_MOD-L3
15	GND	P3V3
16	PCIX_GNT-L0	PMC_MOD-L4
17	PCIX_REQ-L0	PMC_PME-L
18	P5V	GND
19	PMC_VIO	PCIX_AD30
20	PCIX_AD31	PCIX_AD29
21	PCIX_AD28	GND
22	PCIX_AD27	PCIX_AD26
23	PCIX_AD25	PCIX_AD24
24	GND	PCIX_AD23
25	GND	PMC_IDSEL
26	PCIX_CBE-L3	PCIX_AD23
27	PCIX_AD22	P3V3
28	PCIX_AD21	PCIX_AD20
29	PCIX_AD19	PCIX_AD18
30	P5V	GND
31	PCIX_FRAME-L	PCIX_AD16
32	PCIX_AD17	PCIX_CBE-L2

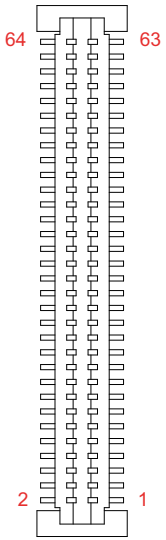


Table 4-27: PMC Connector Pin Definitions

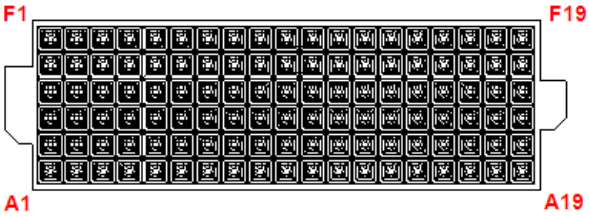
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Pin#	JN1 Signal	JN2 Signal
33	PCIX_FRAME-L	GND
34	GND	NC
35	GND	PCIX_TRDY-L
36	PCIX_IRDY-L	P3V3
37	PCIX_DEVSEL-L	GND
38	P5V	PCIX_STOP-L
39	PCIX_PCIXCAP	PCIX_PERR-L
40	PCIX_LOCK-L	GND
41	NC	P3V3
42	NC	PCIX_SERR-L
43	PCIX_PAR	PCIX_CBE-L1
44	GND	GND
45	PMC_VIO	PCIX_AD14
46	PCIX_AD15	PCIX_AD13
47	PCIX_AD12	PCIX_M66EN
48	PCIX_AD11	PCIX_AD10
49	PCIX_AD9	PCIX_AD8
50	P5V	P3V3
51	GND	PCIX_AD7
52	PCIX_CBE-L0	NC
53	PCIX_AD6	P3V3
54	PCIX_AD5	NC
55	PCIX_AD4	NC
56	GND	GND
57	PMC_VIO	NC
58	PCIX_AD3	NC
59	PCIX_AD2	GND
60	PCIX_AD1	NC
61	PCIX_AD0	PCIX_ACK64-L
62	P5V	P3V3
63	GND	GND
64	PCIX_REQ64-L	NC

Table 4-27: PMC Connector Pin Definitions (cont'd)

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XMC Connector on PMC/XMC Daughter Board (JN3)



Pin#	A	B	C	D	E	F
1	RXP	RXN	3.3V	NC	NC	VPWR
2	GND	GND	Not used	GND	GND	PCIE_RST-L
3	NC	NC	3.3V	NC	NC	VPWR
4	GND	GND	Not used	GND	GND	Not used
5	NC	NC	3.3V	NC	NC	VPWR
6	GND	GND	Not used	GND	GND	+12V
7	NC	NC	3.3V	NC	NC	VPWR
8	GND	GND	Not used	GND	GND	-12V
9	NC	NC	Not used	NC	NC	VPWR
10	GND	GND	Not used	GND	GND	GA0
11	TXP	TXN	Not used	NC	NC	VPWR
12	GND	GND	GA1	GND	GND	Not used
13	NC	NC	3.3V	NC	NC	VPWR
14	GND	GND	GA2	GND	GND	Not used
15	NC	NC	Not used	NC	NC	VPWR
16	GND	GND	Not used	GND	GND	Not used
17	NC	NC	Not used	NC	NC	NC
18	GND	GND	Not used	GND	GND	Not used
19	CK-P	CK-N	Not used	Not used	Not used	Not used

Table 4-28: XMC Connector Pin Definition

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GPIO MMIO Addresses

Pin # on J2	Chipset Signal	DW0 Register Address	DW1 Register Address
GPIO0	GPP_E0	0xFD6B0900	0xFD6B0904
GPIO1	GPP_E1	0xFD6B0910	0xFD6B0914
GPIO2	GPP_E2	0xFD6B0920	0xFD6B0924

Table 4-29: GPIO MMIO Addresses

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CompactPCI J1 Connector

Pin	Z	A	B	C	D	E	F
25	GND	+5V	REQ64#	ENUM#	+3.3V	+5V	GND
24	GND	CPCI_AD1	+5V	CPCI_VIO	CPCI_AD0	ACK64#	GND
23	GND	+3.3V	CPCI_AD4	CPCI_AD3	+5V	CPCI_AD2	GND
22	GND	CPCI_AD7	GND	+3.3V	CPCI_AD6	CPCI_AD5	GND
21	GND	+3.3V	CPCI_AD9	CPCI_AD8	CPCI_M66EN	CPCI_CBE-L0	GND
20	GND	CPCI_AD12	GND	VIO	CPCI_AD11	CPCI_AD10	GND
19	GND	+3.3V	CPCI_AD15	CPCI_AD14	GND	CPCI_AD13	GND
18	GND	CPCI_SERR-L	GND	+3.3V	CPCI_PAR	CPCI_CBE-L1	GND
17	GND	+3.3V	NC	NC	GND	CPCI_PERR-L	GND
16	GND	CPCI_DEVSEL-L	CPCI_PCIXCAP	VIO	CPCI_STOP-L	CPCI_LOCK-L	GND
15	GND	+3.3V	CPCI_FRAME-L	CPCI_IRDY-L	NC	CPCI_TRDY-L	GND
12-14	Key						
11	GND	CPCI_AD18	CPCI_AD17	CPCI_AD16	GND	CPCI_CBE-L2	GND
10	GND	CPCI_AD21	GND	+3.3V	CPCI_AD20	CPCI_AD19	GND
9	GND	CPCI_CBE-L3	NC	CPCI_AD23	GND	CPCI_AD22	GND
8	GND	CPCI_AD26	GND	VIO	CPCI_AD25	CPCI_AD24	GND
7	GND	CPCI_AD30	CPCI_AD29	CPCI_AD28	GND	CPCI_AD27	GND
6	GND	CPCI_REQ-L0	GND	+3.3V	CPCI_CLK0	CPCI_AD31	GND
5	GND	NC	NC	CPCI_RESET-L	GND	CPCI_GNT-L0	GND
4	GND	NC	CPCI_HEALTHY-L	VIO	NC	NC	GND
3	GND	CPCI_IRQA-L	CPCI_IRQB-L	CPCI_IRQC-L	+5V	CPCI_IRQD-L	GND
2	GND	cPCI_TCK-L	+5V	cPCI_TMS-L	NC	cPCI_TDI-L	GND
1	GND	+5V	NC	cPCI_TRST-L	+12V	+5V	GND

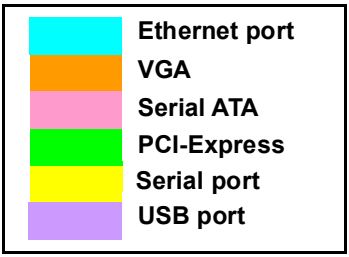
Table 4-30: CompactPCI J1 Connector Pin Definition

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CompactPCI J2 Connector

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	PCI_CLK6	GND	LAN4_MDI1_P	LAN3_MDI3_P	LAN3_MDI1_P	GND
20	GND	PCI_CLK5	GND	LAN4_MDI1_N	LAN3_MDI3_N	LAN3_MDI1_N	GND
19	GND	GND	GND	LAN4_MDI0_P	LAN3_MDI2_P	LAN3_MDI0_P	GND
18	GND	LAN4_MDI3_P	LAN4_MDI2_P	LAN4_MDI0_N	LAN3_MDI2_N	LAN3_MDI0_N	GND
17	GND	LAN4_MDI3_N	LAN4_MDI2_N	J2_RSTJ	CPCI_REQ_L6	CPCI_GNT_L6	GND
16	GND	PCIE4_CLK8_N	PCIE2_CLK6_P	DEGJ	GND	+5V	GND
15	GND	PCIE4_CLK8_P	PCIE2_CLK6_N	FALJ	CPCI_REQ_L5	CPCI_GNT_L5	GND
14	GND	PCIE3_CLK7_N	PCIE1_CLK5_P	PCIE_RST-L	DDC_DAT	+5V	GND
13	GND	PCIE3_CLK7_P	PCIE1_CLK5_N	GPIO2	VGA_HSY	DDC_CLK	GND
12	GND	PCIE4_RXP	GPIO0	GPIO1	VGA_VSY	SATA_RX-P1	GND
11	GND	PCIE4_RXN	PCIE4_TXP	COM3_TX	SATA_TX-P1	SATA_RX-N1	GND
10	GND	PCIE3_RXP	PCIE4_TXN	COM3_RX	SATA_TX-N1	SATA_RX-P2	GND
9	GND	PCIE3_RXN	PCIE3_TXP	USB 2_2P	SATA_TX-P2	SATA_RX-N2	GND
8	GND	PCIE2_RXP	PCIE3_TXN	USB 2_2N	SATA_TX-N2	SATA_RX-P3	GND
7	GND	PCIE2_RXN	PCIE2_TXP	USB 2_3P	SATA_TX-P3	SATA_RX-N3	GND
6	GND	PCIE1_RXP	PCIE2_TXN	USB 2_3N	SATA_TX-N3	RGB_RED	GND
5	GND	PCIE1_RXN	PCIE1_TXP	USB 2_4P	RS232_COM5_SEL-L	RGB_GREEN	GND
4	GND	VIO	PCIE1_TXN	USB 2_4N	USB 2_OC1	RGB_BLUE	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

Table 4-31: CompactPCI J2 Connector Pin Definition

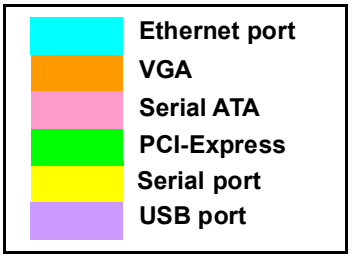


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cPCI-R3P00 rJ2 Connector

Pin	Z	A	B	C	D	E	F
22	GND	NC	NC	NC	NC	NC	GND
21	GND	NC	GND	2_ETH_B+	1_ETH_D+	1_ETH_B+	GND
20	GND	NC	GND	2_ETH_B-	1_ETH_D-	1_ETH_B-	GND
19	GND	GND	GND	2_ETH_A+	1_ETH_C+	1_ETH_A+	GND
18	GND	2_ETH_D+	2_ETH_C+	2_ETH_A-	1_ETH_C-	1_ETH_A-	GND
17	GND	2_ETH_D-	2_ETH_C-	NC	NC	NC	GND
16	GND	NC	NC	NC	GND	+5V	GND
15	GND	NC	NC	NC	NC	NC	GND
14	GND	NC	NC	NC	DDC_DAT	+5V	GND
13	GND	NC	NC	NC	VGA_HSY	DDC_CLK	GND
12	GND	NC	NC	NC	VGA_VSY	2_SATA_RX+	GND
11	GND	NC	NC	COM4_TX	2_SATA_TX+	2_SATA_RX-	GND
10	GND	NC	NC	COM4_RX	2_SATA_TX-	3_SATA_RX+	GND
9	GND	NC	NC	0_USB+	3_SATA_TX+	3_SATA_RX-	GND
8	GND	NC	NC	0_USB-	3_SATA_TX-	4_SATA_RX+	GND
7	GND	NC	NC	1_USB+	4_SATA_TX+	4_SATA_RX-	GND
6	GND	NC	NC	1_USB-	4_SATA_TX-	RGB_RED	GND
5	GND	NC	NC	10_USB+	RS232_COM5_SEL-L	RGB_GREEN	GND
4	GND	NC	NC	10_USB-	USB1_10_OC	RGB_BLUE	GND
3	GND	NC	GND	NC	NC	NC	GND
2	GND	NC	NC	NC	NC	NC	GND
1	GND	NC	GND	NC	NC	NC	GND

Table 4-32: cPCI-R3P00 rJ2 Connector Pin Definition

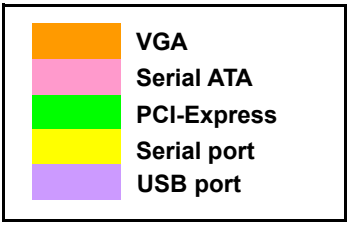


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cPCI-R3P00T rJ2 Connector

Pin	Z	A	B	C	D	E	F
22	GND	NC	NC	NC	NC	NC	GND
21	GND	NC	GND	NC	NC	NC	GND
20	GND	NC	GND	NC	NC	NC	GND
19	GND	GND	GND	NC	NC	NC	GND
18	GND	NC	NC	NC	NC	NC	GND
17	GND	NC	NC	NC	NC	NC	GND
16	GND	4PE_CLK-	2_PE_CLK+	NC	GND	+5V	GND
15	GND	4PE_CLK+	2_PE_CLK-	NC	NC	NC	GND
14	GND	3PE_CLK+	1_PE_CLK+	4_PE_CLKE#	DDC_DAT	+5V	GND
13	GND	3PE_CLK-	1_PE_CLK-	3_PE_CLKE#	VGA_HSY	DDC_CLK	GND
12	GND	4PE_RX00+	1_PE_CLKE#	2_PE_CLKE#	VGA_VSY	2_SATA_RX+	GND
11	GND	4PE_RX00-	4PE_TX00+	COM4_TX	2_SATA_TX+	2_SATA_RX-	GND
10	GND	3PE_RX00+	4PE_TX00-	COM4_RX	2_SATA_TX-	3_SATA_RX+	GND
9	GND	3PE_RX00-	3PE_TX00+	0_USB+	3_SATA_TX+	3_SATA_RX-	GND
8	GND	2PE_RX00+	3PE_TX00-	0_USB-	3_SATA_TX-	4_SATA_RX+	GND
7	GND	2PE_RX00-	2PE_TX00+	1_USB+	4_SATA_TX+	4_SATA_RX-	GND
6	GND	1PE_RX00+	2PE_TX00-	1_USB-	4_SATA_TX-	RGB_RED	GND
5	GND	1PE_RX00-	1PE_TX00+	10_USB+	RS232_COM5_SEL-L	RGB_GREEN	GND
4	GND	NC	1PE_TX00-	10_USB-	USB1_10_OC	RGB_BLUE	GND
3	GND	NC	GND	NC	NC	NC	GND
2	GND	NC	NC	NC	NC	NC	GND
1	GND	NC	GND	NC	NC	NC	GND

Table 4-33: cPCI-R3P00T rJ2 Connector Pin Definition



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4.12 Jumper Settings

XMC VPWR Select Jumper (JPX1)

This jumper is located on the PMC/XMC daughter board near JN1/2 and selects the XMC VPWR setting. 5V is set by default.

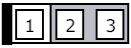
Mode	Connection	JPX1
+5V (Default)	1 – 2	
+12V	2 – 3	

Table 4-34: XMC VPWR Select Jumper Settings

PMC V(I/O) Select Jumper (JPX2)

This jumper is located on the PMC/XMC daughter board near JN1/2 and selects the PMC V(I/O) setting. 3.3V is set by default.

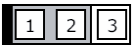
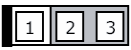
Mode	Connection	JPX2
+5V	1 – 2	
+3.3V (Default)	2 – 3	

Table 4-35: PMC V(I/O) Select Jumper Settings

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5 Getting Started

This chapter describes the following installation procedures for the cPCI-3520 and rear transition module:

- CPU and Heatsink
- 2.5" SATA storage drive
- CFast card
- PCI Mezzanine Card
- Processor blade installation to chassis
- RTM installation to chassis

5.1 CPU and Heatsink

The cPCI-3520 Series come with CPU and heatsink pre-installed. Removal of heatsink/CPU by users is not recommended. Please contact your ADLINK service representative for assistance.

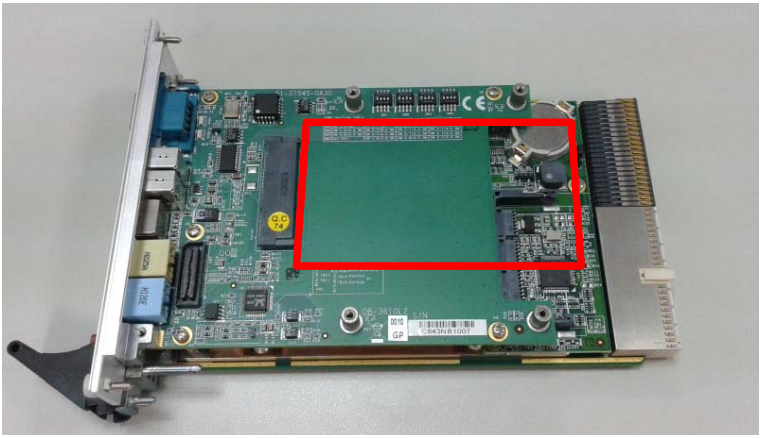
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5.2 SATA Drive Installation

The cPCI-3520D/G/L/M/P 2/3-slot versions provide space to install a slim type 2.5" Serial-ATA storage drive.

Installing a SATA Drive - cPCI-3520D/G/L/M/P

1. A 2.5" SATA drive can be assembled in the location marked as below.



2. 2.Prepare a 2.5" SATA drive and locate the brackets and screws in the accessory kit.



3. Screw the brackets to the 2.5" SATA drive.

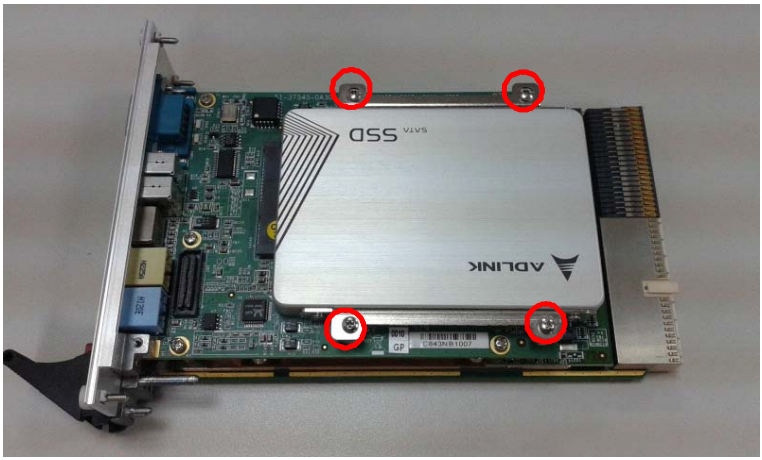


4. Align the drive assembly with the cPCI-3520 and insert it into the onboard SATA connector until it is properly seated.



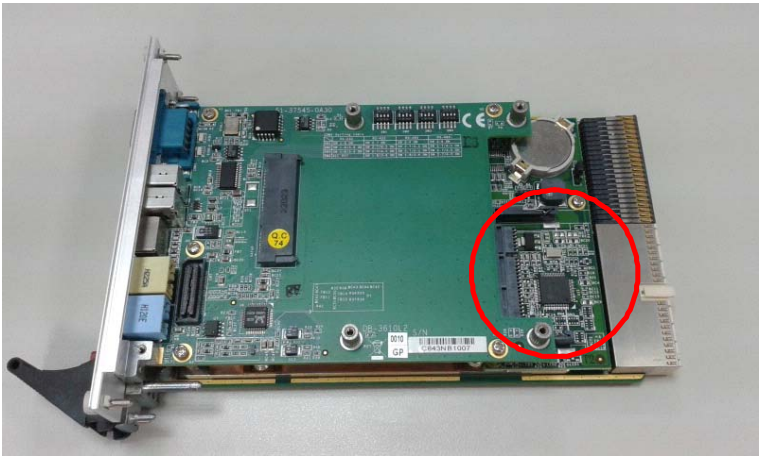
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5. Secure the hard drive assembly to the cPCI-3520 with four M2.5 screws provided.



5.3 Installing a CFast Card

To install a CFast card, locate the CFast connector on the CFAST storage board and insert the card until it is properly seated.



5.4 Installing the cPCI-3520 to the Chassis

The cPCI-3520 may be installed in a system or peripheral slot of a 3U CompactPCI chassis. These instructions are for reference only. Refer to the user guide that comes with the chassis for more information.

1. Be sure to select the correct slot depending on the operational purpose of the module. The system power may now be powered on or off.
2. Remove the blank face cover from the selected slot, if necessary.
3. Press down on the release catches of the cPCI-3520 ejector handles.
4. **Remove the black plastic caps securing the mounting screws to the faceplate.**
5. Align the module's top and bottom edges to the chassis card guides, and then carefully slide the module into the chassis. A slight resistance may be felt when inserting the module. If the resistance it too strong, check if there are bent pins on the backplane or if the board's connector pins are not properly aligned with connectors on the backplane. Then push the board until it is completely flush with the chassis.
6. Push the ejector handles outwards to secure the module in place, and then fasten the screws on the module faceplate.
7. Connect the cables and peripherals to the board, and then turn the chassis on if necessary.

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5.5 RTM Installation - cPCI-R3P00(T)

The installation and removal procedures for a RTM are the same as those for CompactPCI boards. Because they are shorter than front boards, pay careful attention when inserting or removing RTMs.

Refer to previous sections for peripheral connectivity of all I/O ports on the RTM. When installing the cPCI-3520 Series and related RTMs, make sure the RTM is the correct matching model.


NOTE:

You must install the correct RTM to enable functions (I/O interfaces) on the rear panel. Installation of non-compatible RTMs may damage the system board and/or other RTMs.

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6 Driver Installation

The cPCI-3520 drivers are available from the ADLINK website (https://www.adlinktech.com/Products/CompactPCI/3UCompactPCI2_0Blades/cPCI-3520_Series). ADLINK provides validated drivers for Windows 10 64-bit. We recommend using these drivers to ensure compatibility.

6.1 cPCI-3520 Drivers

The following describes the cPCI-3520 driver installation procedures for Windows 10 64-bit. Install the Windows operating system before installing any driver. Most standard I/O device drivers are installed during Windows installation.

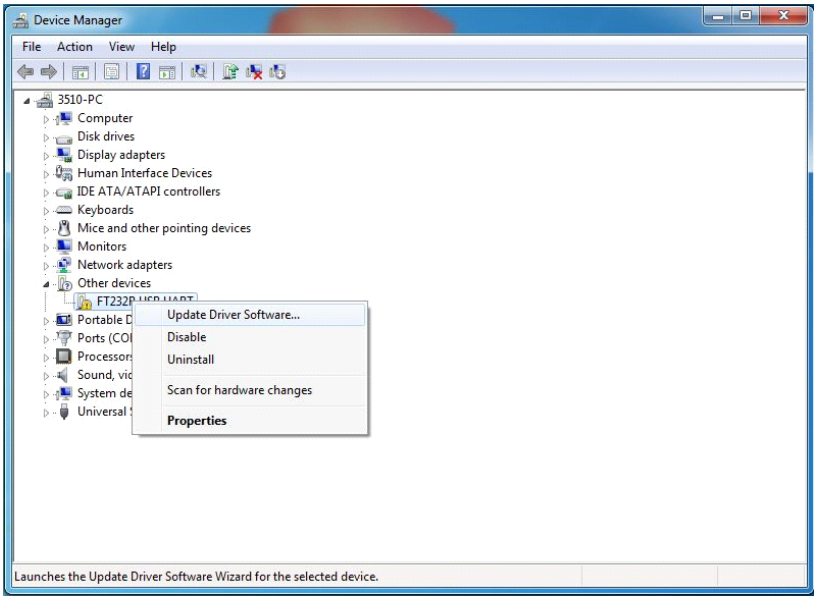
1. Install the **chipset driver** by extracting and running the program in **...\Chipset\Chipset_10.1.18121.8164.zip**.
2. Install the **graphics driver** and utilities by extracting and running the program in **...\Graphics\igfx_win10_100.9466.zip**.
3. Install the **Management Engine (ME) driver** and utilities by extracting and running the program in **...\ME\Intel Management Engine Interface 12.0.34.1425.zip**.
4. Install the **Ethernet Controller driver** by extracting and running the program in **…\Network\PROWinx64.zip**.

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6.2 USB-to-Serial Converter Driver (RTM)

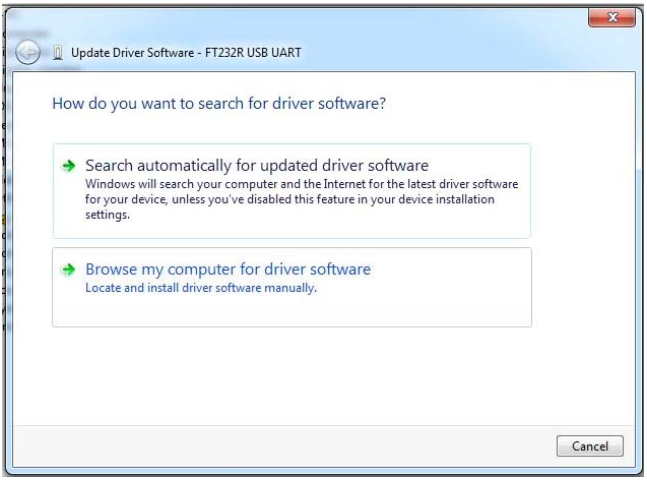
The COM5 serial port on the cPCI-R3P00(T) is converted from the USB3 port by a USB-to-serial converter (see " cPCI-R3P00 RTM" on page 17). To install the driver for the converter, follow the procedure below.

1. Extract the contents of **…\COM\CDM 2.08.28 WHQL Certified-x64.zip**.
2. Open the *Device Manager* and go to *Other Devices.* You will see a "question mark" next to *FT2332R USB UART.* R-click on *FT2332R USB UART* and choose "Update Driver Software…".

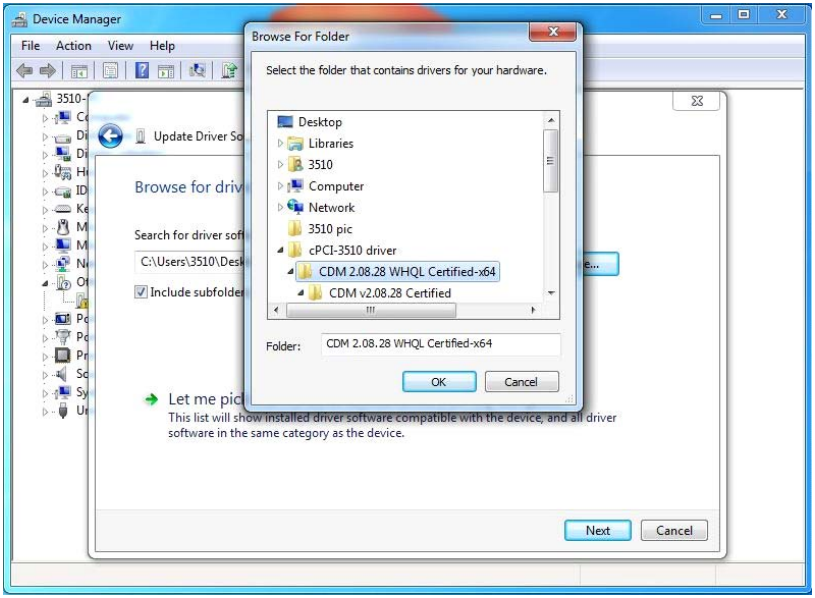


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3. Click “Browse my computer for driver software”.



4. Navigate to the folder where you extracted the contents of the zip file and click “OK”. Click “Next” to install the driver



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7 BIOS Setup Utility

The following chapter describes basic navigation for the AMI EFI BIOS setup utility.

7.1 Starting the BIOS

To enter the setup screen, follow these steps:

1. Power on the motherboard
2. Press the < Delete > key on your keyboard when you see the following text prompt:
   < Press DEL to run Setup >
3. After you press the < Delete > key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu.



In most cases, the < Delete > key is used to invoke the setup screen. There are several cases that use other keys, such as < F1 >, < F2 >, and so on.

Setup Menu

The main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in this user's guide.

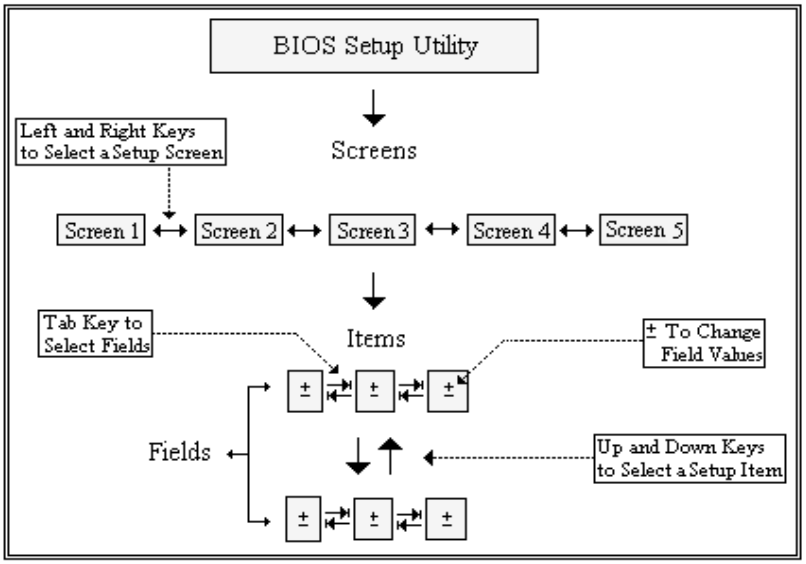
The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed" options cannot be configured, "Blue" options can be.

The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

Navigation

The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process.

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NOTE: There is a hot key legend located in the right frame on most setup screens.

→←	Left/Right. The Left and Right < Arrow > keys allow you to select a setup screen. For example: Main screen, Advanced screen, Chipset screen, and so on.
↑↓	Up/Down The Up and Down < Arrow > keys allow you to select a setup item or sub-screen.
+-	Plus/Minus The Plus and Minus < Arrow > keys allow you to change the field value of a particular setup item. For example: Date and Time.
Tab	The < Tab > key allows you to select setup fields.
ESC	The < Esc > key allows you to discard any changes you have made and exit the Setup. Press the < Esc > key to exit the setup without saving your changes. Press the < Enter > key to discard changes and exit. You can also use the < Arrow > key to select Cancel and then press the < Enter > key to abort this function and return to the previous screen.

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7.2 Main Setup

When you first enter the Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. The Main BIOS Setup menu is shown below.

Main	Advanced	Chipset	Security	Boot	Save & Exit	Server Mgmt
-BIOS Information -System Information -System Date -System Time	-CPU Configuration ► -Power Management ► -USB Configuration ► -AMT Configuration ► -CSM Configuration ► -Super IO Configuration ► -Serial Console Redirection ► -Miscellaneous -Network Stack Configuration ► -Intel ® I210 Gigabit Network Connection – [MAC Address] ► -Intel ® I210 Gigabit Network Connection – [MAC Address] ► -Intel ® I210 Gigabit Network Connection – [MAC Address] ► -Intel ® Ethernet Connection (7) I219-LM – [MAC Address] ►	-System Agent (SA) Configuration ► -PCH-IO Configuration ►	-Administrator Password -User Password -Secure Boot Menu ► -HDD Security Configuration	-Boot Configuration	-Save Options -Boot Override	-BMC Self Test Status -BMC Device ID -BMC Device Revision -BMC Firmware Revision -IPMI Version -BMC Intreface(s) -BMC Support -OS Watchdog Timer

NOTE:

► indicates a submenu
Gray text indicates info only

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7.2.1 BIOS Information

Feature	Options	Description
BIOS Vendor	Info only	American Megatrends
BIOS Version	Info only	Display Core Version
Build Date	Info only	Date the BIOS was built
MRC Version	Info only	Platform MRC Version
GOP Version	Info only	Platform GOP Version
ME FW Version	Info only	Intel Management Engine Version
BIOS Boot Source	Info only	First BIOS

7.2.2 System Information

Feature	Options	Description
Project Name	Info only	Display Project Name
CPU Board Version	Info only	Display CPU Board Version
CPU Brand String	Info only	Display Intel CPU Brand Information
Stepping	Info only	Display CPU Stepping
GT Info	Info only	Display GT info
CPU Frequency	Info only	Display CPU Frequency
Total Memory	Info only	Display Current System installed Memory Size
Memory Frequency	Info only	Display Memory Frequency Information
PCH SKU	Info only	Display PCH Version
Stepping	Info only	Display PCH Stepping

7.2.3 System Date and Time

Feature	Options	Description
System Date	MM/DD/YYYY	Requires the alpha-numeric entry of the day of the week, day of the month, calendar month, and all 4 digits of the year, indicating the century and year (Fri XX/XX/20XX).
System Time	HH/MM/SS	Presented as a 24-hour clock setting in hours, minutes, and seconds.

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7.3 Advanced

This menu contains the settings for most of the user interfaces in the system.

7.3.1 CPU Configuration

Feature	Options	Description
Type	Info only	Manufacturer, model
ID	Info only	Display CPU Information
Microcode Revision	Info only	Display Microcode Revision
Speed	Info only	Display CPU Speed.
L1 Data Cache	Info only	Display L1 Data Cache size
L1 Instruction Cache	Info only	Display L1 Instruction Cache size
L2 Cache	Info only	Display L2 Data Cache size
L3 Cache	Info only	Display L3 Data Cache size
L4 Cache	Info ony	Display L4 Data Cache size
Boot performance mode	Max Battery **Max Non-Turbo Performance** Turbo Perfromance	Select the performance state that the BIOS will set starting from reset vector.
Hyper-Threading	Disabled **Enabled**	Enabled or Disabled Hyper-Threading Technology
Active Processor Cores	**All** 1 2 3 4 5 6 7	Number of cores to enable in each processor package
Intel® SpeedStep™	Disabled **Enabled**	Allows more than two frequency ranges to be supported
Intel® Speed Shift Technology	Disabled **Enabled**	Enable/Disable Intel® Speed Shift Technology support.
Turbo Mode	Disabled **Enabled**	Enable/Disable processor Turbo Mode
Configurable TDP Boot Mode	**Nominal** Deactivate	Configurable TDP Mode as Nominal/Deactivate TDP selection. Deactivate option will set MSR to Nominal and MMIO to Zero
Platform PL1 Enable	**Disabled** Enabled	When a processor thermal sensor trips (either core), the PROCHOT# will be driven. If bi-direction is enabled, external agents can drive PROCHOT# to throttle the processor

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Feature	Options	Description
C state	Disabled **Enabled**	Enable/Disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized.
Package C State Limit	C0/C1 C2 C3 C6 C7 C7S C8 C9 C10 CPU Default **Auto**	Maximum Package C State Limit Setting. CPU Default: Leaves to Factory default value. Auto: Initializes to deepest available Package C State Limit
Active Processor Cores	**All** 1 2 3 4 5	Number of cores to enable in each processor package.
VT-d	Disabled **Enabled**	Enable/Disable VT-d capability
DTS SMM	Disabled **Enabled** Critical Temp Reporting (Out of spec)	Disabled: ACPI thermal management uses EC reported temperature values. Enabled: ACPI thermal management uses DTS SMM mechanism to obtain CPU temperature values. Out of Spec: ACPI Thermal Management uses EC reported temperature values and DTS SMM is used to handle Out of Spec.
Intel Trusted Execution Technology	**Disabled** Enabled	Enable/Disable utilization of additional hardware capabilities provided by Intel® Trusted Execution Technology. Changes require a full power cycle to take effect.

7.3.2 Power Management

Feature	Options	Description
Enable ACPI Auto Configuration	**Disabled** Enabled	Enables or Disables BIOS ACPI Auto Confiuration

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7.3.3 USB Configuration

Feature	Options	Description
USB Module version	Info only	
USB Controllers:	Info only	
USB Devices:	Info only	.
USB Mass Storage Driver Support	Disabled **Enabled**	Enable/Disable USB Mass Storage Driver Support
XHCI Compliance Mode	Enabled **Disabled**	Option to enable Compliance Mode. Default is to disable Compliance Mode. Change to enabled for Complaince Mode testing.
xDCI Support	Enabled **Disabled**	Enable/Disable xDCI (USB OTG device)
USB Port Disable Override	**Disable Link** Select Per-Pin	Select to Enable/Disable the corresponding USB port from reporting a Device Connection to the Controller.

7.3.4 AMT Configuration

Feature	Options	Description
AMT BIOS Features	Disabled **Enabled**	When disabled AMT BIOS Features are no longer supported and user is no longer able to access MEBx Setup. Note: This option does not disable Manageability Features in FW.
MEBx Hotkey Pressed	**Disabled** Enabled	OME Flag Bit 1: Enable automatic MEBx hotkey press.

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7.3.5 CMS Configuration

Feature	Options	Description
CSM Support	**Disabled** Enabled	Enable/Disable CSM Support.
CSM16 Module Version	Info only	
GateA20 Active	**Upon Request** Always	UPON REQUEST - GA20 can be disabled using BIOS services. ALWAYS - do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.
Boot Option filter	**UEFI and Legacy** Legacy only UEFI only	This option controls Legacy/UEFI ROMs priority.
Option ROM execution	Info only	
Network	**Do not launch** Legacy UEFI	Controls the execution of UEFI and Legacy Network OpROM.
Storage	Do not launch **UEFI** Legacy	Controls the execution of UEFI and Legacy Storage OpROM
Video	Do not launch **UEFI** Legacy	Controls the execution of UEFI and Legacy Video OpROM.
Other PCI devices	Do not launch **UEFI** Legacy	Determines OpROM execution policy for devices other than Network, Storage, or Video.

7.3.6 Super IO Configuration

Feature	Options	Description
NCT6106D Super IO Configuration	Info only	
Serial Port 1 Configuration	Submenu	
Serial Port 2 Configuration	Submenu	
Serial Port 3 Configuration	Submenu	
Serial Port 4 Configuration	Submenu	
Serial Port 5 Configuration	Submenu	

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Super IO Configuration > Serial Port 1 Configuration

Feature	Options	Description
Serial Port 1 Configuration	Info only	
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	IO=3F8h; IRQ=4	Fixed configuration of serial port.
Device Mode	**RS232 Mode** RS422/RS485Mode	Change the Serial Port mode.
Change Settings	**Auto** IO=3F8h; IRQ=4; IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;	Select an optimal setting for Super IO Device

Super IO Configuration > Serial Port 2 Configuration

Feature	Options	Description
Serial Port 2 Configuration	Info only	
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	IO=2F8h; IRQ=3	Fixed configuration of serial port.
Device Mode	**RS232 Mode** RS422/RS485 Mode	Change the Serial Port mode.
Change Settings	**Auto** IO=2F8h; IRQ=3; IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;	Select an optimal setting for Super IO Device


NOTE:

Device Mode settings are for cPCI-3520G only. For cPCI-3520D/P models, set the Device Mode using SW1~SW4. See *"COM1 Mode Selection Switches (SW1-SW4)" on page 49.*.

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Super IO Configuration > Serial Port 3 Configuration

Feature	Options	Description
Serial Port 3 Configuration	Info only	
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	IO=3E8h; IRQ=5	Fixed configuration of serial port.
Change Settings	**Auto** IO=3E8h; IRQ=7; IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=2F0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=2E0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;	Select an optimal setting for Super IO Device

Super IO Configuration > Serial Port 4 Configuration

Feature	Options	Description
Serial Port 4 Configuration	Info only	
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	IO=2E8h; IRQ=7	Fixed configuration of serial port.
Change Settings	**Auto** IO=2E8h; IRQ=7; IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=2F0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=2E0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;	Select an optimal setting for Super IO Device

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Super IO Configuration > Serial Port 5 Configuration

Feature	Options	Description
Serial Port 5 Configuration	Info only	
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	IO=2F0h; IRQ=6	Fixed configuration of serial port.
Change Settings	**Auto** IO=2E0h; IRQ=7; IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=2F0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12; IO=2E0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;	Select an optimal setting for Super IO Device

7.3.7 Serial Console Redirection

Feature	Options	Description
Serial Console Redirection	Info only	
COM1~4		
Console Redirection	Enabled **Disabled**	Console Redirection enable or disable
Console Redirection Settings	Submenu	

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Console Redirection Settings

Feature	Options	Description
Console Redirection Settings	Info only	
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7 **8**	Data Bits.
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
VT-UTF8 Combo Key Support	Disabled **Enable**	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.
Recorder Mode	**Disabled** Enable	With this mode enabled only text will be sent. This is to capture Terminal data.
Resolution 100x31	**Disabled** Enable	Enables or disables extended terminal resolution
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.

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7.3.8 Miscellaneous

Feature	Options	Description
Trusted Computing	Submenu	Trusted Computing Settings
NVMe Configuration	Submenu	NVMe Device Options Settings
Power Supply Unit	Emulate AT Mode **ATX Mode**	ATX: OS will turn off system power when shutdown. AT mode will not support S3 & S4 & S5, so it will change Power Loss State to Power On.
Network	**Do not launch** UEFI Legacy	Controls the execution of UEFI Network OpROM
VGA Switch	**Front** RTM	Change the VGA output. Select <Front> or <RTM> output

Trusted Computing

Feature	Options	Description
Security Device Support	**Disabled** Enabled	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.

NVMe Configuration

Feature	Options	Description
NVMe Configuration	Info only	

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7.3.9 Network Stack Configuration

Feature	Options	Description
Network Stack	**Disabled** Enabled	Enable/Disable UEFI network stack.
IPv4 PXE Support	**Disabled** Enabled	Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.
IPv4 HTTP Support	**Disabled** Enabled	Enable/Disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.
IPv6 PXE Support	**Disabled** Enabled	Enable/Disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.
IPv6 HTTP Support	**Disabled** Enabled	Enable/Disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.
IPSEC Certificate	**Enabled**	Support to Enable/Disable IPSEC certificate for Ikev.
PXE boot wait time	**0**	Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.
Media detect count	**1**	Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

7.3.10 Intel I210 Gigabit Network Connection / Ethernet Connection (7) I219-LM [MAC Address]

Feature	Options	Description
NIC Configuration	Submenu	Click to configure the device network device port
UEFI Driver	Info only	
Adpater PBA	Info only	
Device Name	Info only	
Chip Type	Info only	
PCI Device ID	Info only	
PCI Address	Info only	
Link Status	Info only	
MAC Address	Info only	
Virtual MAC Address	Info only	

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NIC Configuration

Feature	Options	Description
Link Speed	**Auto Negotiated** 10 Mbps Half 10 Mbps Full 100 Mbps Half 100 Mbps Full	Specifies the port speed used for the selected boot protocol
Wake On LAN	**Disabled** Enabled	Enables the server to be powered on using an in-band magic packet.

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7.4 Chipset

Feature	Options	Description
System Agent (SA) Configuration	Submenu	System Agent (SA) Parameters
PCH-IO Configuration	Submenu	PCH parameters

7.4.1 System Agent (SA) Configuration

Feature	Options	Description
SA PCIe Code Version	Info only	Displaye SA PCIe code revision
VT-d	Info only	Display VT-d supported or not
Memory Configuration	Submenu	Memory parameters
Graphics Configuration	Submenu	Graphics parameters
PEG Port Configuration	Submenu	PEG port parameters
Above 4GB MMIO BIOS assignment	Enabled **Disabled**	Enable/Disable above 4GB memory mapped BIOS assignment.

Memory Configuration

Feature	Options	Description
Memory RC Version	Info only	Display RC version
Memory Frequency	Info only	Display memory frequency
Memory Voltage	Info only	Display memory voltage
Memory Timings (tCL-tRCD-tRP-tRAS)	Info only	Display memory timing parameters
Channel 0 Slot 0	Info only	Display memory Size
Channel 1 Slot 0	Info only	Display memory Size
Maximum Memory Frequency	**Auto** 1067, 1200…, 5867	Maximum memory frequency selections in MHz. Valid values should match the refclk, i.e. divided by 133 or 100
Max TOLUD	**Dynamic** 1 GB, 1.25GB…3.5GB	Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.

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Graphics Configuration

Feature	Options	Description
Skip Scaning of External Gfx Card	**Disabled** Enabled	If Enabled, it will not scan for External Gfx card on PEG and PCH PCIE ports
Primary Display	**Auto** IGFX PEG PCIe	Select which IGFX/PEG/PCI Graphics device should be Primary Display.
Select PCIe Card	**Auto** Elk Creek 4 PEG Eval	Select the card used on the platform Auto: Skip GPIO based power enable to dGPU Elk Creek 4: dGPU Power Enable = ActiveLow PEG Eval: dGPU Power Enable = ActiveHigh
Internal Graphics	**Auto** Disabled Enabled	Keep IGFX enabled based on the setup options
GTT Size	2MB 4MB **8MB**	Select the GTT Size
Aperture Size	128MB **256MB** 512MB 1024MB 2048MB	Select the Aperture Size Note: Above 4GB MMIO BIOS assignment is automatically enabled when selecting 2048MB aperture. To use this feature, please disable CSM support.
DVMT Pre-Allocated	0M **32M** 64M 4M 8M 12M 16M 20M 24M 28M 32M/F7 36M 40M 44M 48M 52M 56M 60M	Select DVMT 5.0 pre-allocated (fixed) graphics memory size used by the internal graphics device.
DVMT Total Gfx Mem	128M **256M** Max	Select DVMT5.0 total graphics memory used by the internal graphics device.

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PEG Port Configuration

Feature	Options	Description
PEG 0:1:0 / 0:1:1 / 0:1:2 / 0:6:0		
Enable Root Port	Disabled Enabled **Auto**	Enable or disable this root port
Max Link Speed	**Auto** Gen1 Gen2 Gen3	Configure PEG 0:1:0 max speed
PEG0 Slot Power Limit Value	75	Sets the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying this value by the Slot Power Limit Scale. Values 0-255
PEG0/1/2/3 Slot Power Limit Scale	**1.0x** 0.1x 0.01x 0.001x	Select the scale used for the Slot Power Limit Value.
PEG0/1/2/3 Physical Slot Number	1	Set the physical slot number attached to this Port. The number has to be globally unique within the chassis. Values 0-8191
Gen3 RxCTLE Control	Submenu	Gen3 RxCTLE Control per Bundle
PCIe Rx CEM Test Mode	**Disabled** Enabled	Enable/Disable PEG Rx CEM Loopback Mode
PCIe Spread Spectrum Clocking	**Enabled** Disabled	Allows disabling Spread Spectrum Clocking for compliance testing

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Gen3 RxCTLE Control

Feature	Options	Description
Bundle0	**0**	Gen3 RxCTLE setting for Bundle0 (Lane0, Lane1)
Bundle1	**0**	Gen3 RxCTLE setting for Bundle1 (Lane2, Lane3)
Bundle2	**0**	Gen3 RxCTLE setting for Bundle2 (Lane4, Lane5)
Bundle3	**0**	Gen3 RxCTLE setting for Bundle3 (Lane6, Lane7)
Bundle4	**0**	Gen3 RxCTLE setting for Bundle4 (Lane8, Lane9)
Bundle5	**0**	Gen3 RxCTLE setting for Bundle5 (Lane10, Lane11)
Bundle6	**0**	Gen3 RxCTLE setting for Bundle6 (Lane12, Lane13)
Bundle7	**0**	Gen3 RxCTLE setting for Bundle7 (Lane14, Lane15)
PEG10 RxCTLE Override	**Disabled** Enabled	When Enabled, it overrides PEG0 RxCTLE adaptive behaviour
PEG11 RxCTLE Override	**Disabled** Enabled	When Enabled, it overrides PEG1 RxCTLE adaptive behavior
PEG12 RxCTLE Override	**Disabled** Enabled	When Enabled, it overrides PEG2 RxCTLE adaptive behavior
DMI RxCTLE Override	**Disabled** Enabled	When Enabled, it overrides DMI RxCTLE adaptive behavior

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7.4.2 PCH-IO Configuration

Feature	Options	Description
PCI Express Configuraiton	Submenu	Configure Serial IRQ Mode.
SATA And RST Configuration	Submenu	Enable/Disable SMBus Support.
HD Audio Configuration	Submenu	Select the target OS.
PCH LAN Controller	**Enabled** Disabled	Enable/Disable onboard NIC
Wake on LAN for S5 Enable	**Enabled** Disabled	Enable/Disable integrated LAN to wake the system only for S5.
Serial IRQ Mode	Quiet **Continuous**	Configure Serial IRQ Mode
High Precision Timer	**Enabled** Disabled	Enable or Disable the High Precision Event Timer
PCIE PLL SSC	**Auto** 0.1%~2.0%	PCIe PLL SSC percentage. Auto – Keep HW default, no BIOS override. Range is 0.0%-2.0%
SPD Write Disable	**True** False	Enable/Disable setting SPD write disable.

PCIe Express Configuration

Feature	Options	Description
PCIe Configuration	Info only	
PCI Express Clock Gating	Disabled **Enabled**	PCI Express Clock Gating Enable/Disable for each root port
DMI Link ASPM Control	**Disabled** Enabled	The control of Active State Power Management of the DMI Link
PCIE Port assigned to LAN	Read only	
Compliance Test Mode	**Disabled** Enabled	Enable when using Compliance Load Board
PCIe-USB Glitch W/A	**Disabled** Enabled	PCIe-USB Glitch W/A for bad USB device(s) connected behind PCIE/PEG port.
PCIe function swap	Disabled **Enabled**	When Disabled, prevents PCIE root port function swap. If any function other than 0^{th} is enabled, 0^{th} will become visible.
PCIe Express Root Port1~11, 17~20	Submenu	PCI Express Root Port Settings

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PCIe Express Configuration > PCI Express Root PortX

Feature	Options	Description
PCIe Express Root PortX	Disabled **Enabled**	Control the PCI Express Root Port.
Connection Type	Built-in **Slot**	Built-In: a built-in device is connected to this rootport. SlotImplemented bit will be clear. Slot: this rootport connects to user-accessible slot. SlotImplemented bit will be set.
ASPM	**Disable** L0s L1 L0sL1 Auto	Set the ASPM Level: Force L0s – Force all inks to L0s State Auto – BIOS auto configure Disable – Disables ASPM
L1 Substates	Disabled L1.1 **L1.1 & L1.2**	PCI Express L1 substates settings.
Gen3 Eq Phase3 Method	**Hardware** Static Coeff.	PCIe Gens3 Equalization Phase 3 Method
UPTP	Info only	Upstream Port Transmitter Preset
DPTP	Info only	Downstream Port Transmitter Preset
ACS	**Enabled** Disabled	Enable/Disable Access Control Services Extended Capability
PTM	**Enabled** Disabled	Enable/Disable Precision Time Measurement
DPC	**Enabled** Disabled	Enable/Disable Downstream Port Containment
EDPC	**Enabled** Disabled	Enable/Disable Rootport extensions for Downstream Port Containment
URR	Enabled **Disabled**	PCI Express Unsupported Request Reporting Enable/Disable
FER	Enabled **Disabled**	PCI Express Device Fatal Error Reporting Enable/Disable
NFER	Enabled **Disabled**	PCI Express Device Non-Fatal Error Reporting Enable/Disable
CER	Enabled **Disabled**	PCI Express Device Correctable Error Reporting Enable/Disable
CTO	Enabled **Disabled**	PCI Express Completion Timer TO Enable/Disable.
SEFE	Enabled **Disabled**	Root PCI Express System Error on Fatal Error Enable/Disable
SENFE	Enabled **Disabled**	Root PCI Express System Error on Non-Fatal Error Enable/Disable.
SECE	Enabled **Disabled**	Root PCI Express System Error on Correctable Error Enable/Disable

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Feature	Options	Description
PME SCI	**Enabled** Disabled	PCI Express PME SCI Enable/Disable
Hot Plug	Enabled **Disabled**	PCI Express Hot Plug Enable/Disable
Advanced Error Reporting	**Enabled** Disabled	Advanced Error Reporting Enable/Disable
PCIe Speed	**Auto** Gen1 Gen2 Gen3	Configure PCIe Speed
Transmitter Half Swing	**Disabled** Enabled	Transmitter Half Swing Enable/Disable
Detect Timeout	Info only	The number of milliseconds reference code will wait for link to exit Detect State for enabled ports before assuming there is no device and potentially disabling the port.
Extra Bus Reserved	Info only	Extra Bus Reserved (0-7) for bridges behind this Root Bridge
Reserved Memory	Info only	Resreved Memory for this Root Bridge (1-20) MB
Reserved I/O	Info only	Reserved I/O (4K/8K/12K/16K/20K) range for this root bridge
PCH PCIe LTR Configuration		
LTR	**Enabled** Disabled	PCH PCIE Latency Reporting Enable/Disable
Snoop Latency Override	Disabled Manual **Auto**	Snoop Latency Override for PCH PCIE. Disabled: Disable override Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Non Snoop Latency Override	Disabled Manual **Auto**	Non Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Force LTR Override	**Disabled** Enabled	Force LTR Override for PCH PCIE. Disabled: LTR override values will not be forced. Enabled: LTR override values will be forced and LTR messages from the device will be ignored.
LRT Lock	**Disabled** Enabled	PCIE LTR configuration lock

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SATA And RST Configuration

Feature	Options	Description
SATA And RST Configuration	Info only	
SATA Controller(s)	Disabled **Enabled**	
SATA Mode Selection	**AHCI** Intel RST Premium With Intel Optane System Acceleration	Determines how SATA controller(s) operate.
SATA Test Mode	Enabled **Disabled**	Test Mode Enable/Disable (Loop Back)
Software Feature Mask Configuration	Submenu	RST Legacy OROM/RST UEFI driver will refer to the SWFM configuration to enable/disable the storage features.
Aggressive LPM Support	Disabled **Enabled**	Enable PCH to aggressively enter link power state.
SATA Controller Speed	Default Gen1 **Gen2** Gen3	Indicates the maximum speed the SATA controller can support
Serial ATA Port X, X = 0-7	Info only	
Software Preserve	Info only	
Port X	Disabled **Enabled**	Enable or Disable SATA Port.
Hot Plug Capability	**Disabled** Enabled	Designates this port as Hot Pluggable
Configured as eSATA	Info only	
External	**Disabled** Enabled	Marks this port as external
Spin Up Device	**Disabled** Enabled	If enabled for any of ports Staggerred Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
SATA Device Type	**Hard Disk Drive** Solid State Drive	Identify the SATA port is connected to solid state drive or hard disk drive
SATA Port X DevSlp	**Disabled** Enabled	Enable/Disable SATA Port X DevSlp. For DevSlp to work, both hard drive and SATA port need to support DevSlp function, otherwise an unexpected behavior might happen. Please check board design before enabling it.
DTTO Configuration	**Disabled** Enabled	Enable/Disable DITO configuration
DITO Value	Info only	Display DITO value
DM Value	Info only	Display DM value

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HD Audio Configuration

Feature	Options	Description
HD-Audio Support	Disabled **Enabled**	Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled Enabled = HAD will be unconditionally enabled.

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7.5 Security

7.5.1 Password Description

Feature	Options	Description
Administrator Password	Enter password	Set Administrator Password
User Password	Enter password	Set user Password
Secure Boot Menu	Submenu	Customizable Secure Boot settings
HDD Security Configuration	Enter User Password Enter Master Password	Set HDD User Password Set HDD Master Password

Secure Boot Menu

Feature	Options	Description
System Mode	Info only	Show system mode.
Secure Boot	Info only	Show Secure Boot status.
Secure Boot Control	**Disabled** Enabled	Secure Boot activated when platform Key (PK) is enrolled, system mode is User/Deployed, and CSM function is disabled.
Secure Boot Mode	**Standard** Custom	Secure Boot mode options: If Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication.

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7.6 Boot

Feature	Options	Description
Setup Prompt Timeout	1	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
Bootup NumLock State	On **Off**	Select the keyboard NumLock state after system boot.
Quiet Boot	Disabled **Enabled**	Enables or disables Quiet Boot option.
Fast Boot	Disabled **Enabled**	Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.
SATA Support	**Last Boot SATA Devices Only** All SATA Devices	If Last Boot SATA Devices Only, Only last boot SATA device will be available in Post. If All SATA Devices, all SATA devices will be available in OS and Post.
VGA Support	Auto **EFI Driver**	If Auto, only install Legacy OpRom with Legacy OS and logo will NOT be shown during post. EFI driver will still be installed with EFI OS.
USB Support	Disabled **Full Initial** Partial Initial	If Disabled, all USB devices will NOT be available util after OS boot. If Partial Initial, USB Mass Storage and specific USB port/device will NOT be available before OS boot. If Enabled, all USB devices will be available in OS and Post.
PS2 Deivces Support	Disabled **Enabled**	If Disabled, PS2 devices will be skipped.
Network Stack Driver Support	**Disabled** Enabled	If Disabled, Network Stack Driver will be skipped.
Redirection Support	**Disabled** Enabled	If disable, Redirection function will be disabled.
Boot mode select	Legacy **UEFI**	Select boot mode LEGACY/UEFI.
Boot Configuration	Info only	

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7.7 Save & Exit

Feature	Options	Description
Save Changes and Reset	Save changes and reset the system.	Exit system setup after saving the changes.
Discard Changes and Reset	Reset the system without saving any changes.	Exit system setup without saving the changes.
Save Changes and Reset	Reset the system with saving any changes.	Reset the system after saving the changes.
Discard Changes and Reset	Reset the system and discard any changes.	Reset the system after without the changes.
Save Changes		Save Changes done so far to any of the setup options.
Discard Changes		Discard Changes done so far to any of the setup options.
Restore Default		Restore/Load the Default values for all the setup options.
Save as User Default		Save the changes done so far as User Defaults.
Restore User Default		Restore the User Defaults to all the setup options.
UEFI: Built-in EFI Shell		
Launch EFI Shell from filesystem device		

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7.8 Server Mgmt

Feature	Options	Description
BMC Self Test Status	Info only	
BMC Device ID	Info only	
BMC Device Revision	Info only	
BMC Firmware Revision	Info only	
IPMI Version	Info only	
BMC Interface(s)	Info only	
BMC Support	**Enabled** Disabled	Enable/Disable interfaces to communicate with BMC
OS Watchdog Timer	**Disabled** Enabled	If enabled, starts a BIOS timer which can only be shut off by Management Software after the OS loads. Helps determine that the OS successfully loaded or follows the OS Boot Watchdog Timer policy
OS Wtd Timer Timeout	5 minutes **10 minutes** 15 minutes 20 minutes	Configure the length of the OS Boot Watchdog Timer. Not available if OS Boot Watchdog Timer is disabled.
OS Wtd Timer Policy	Do Nothing **Reset** Power Down Power Cycle	Configure how the system should respond if the OS Boot Watchdog Timer expires. Not available if OS Boot Watchdog Timer is disabled.

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8 IPMI User Guide

8.1 Introduction

This chapter is written for those who already have a basic understanding of the newest implementation of the baseboard management controller (BMC) of the Intelligent Platform Management Interface (IPMI) specification rev. 2.0. It also describes the OEM extension IPMI command usages which are not listed in the IPMI specification.

8.2 Summary of Commands Supported by BMR-AVR-cPCI

The table below lists all the commands supported by the BMR-AVR-cPCI.

Command	IPMI Spec	NetFn	CMD	Description (Req'd by PICMG 3.0/2.9)
IPM Device "Global" Commands				
Get Device ID	20.1	App	01h	This command is used to retrieve the Intelligent Device's Hardware Revision, Firmware/ Software Revision, and Sensor and Event Interface Command specification revision information.
Cold Reset	20.2	App	02h	This command directs the Responder to perform a 'Cold Reset' of itself. (Optional/Optional)
Warm Reset	20.3	App	03h	This command directs the Responder to perform a 'Warm Reset' of itself.
Get Self Test Results	20.4	App	04h	This command directs the device to return its Self Test results, if any. (Mandatory/Mandatory)

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Command	IPMI Spec	NetFn	CMD	Description (Req'd by PICMG 3.0/2.9)
Get Device GUID	20.8	App	08h	This command returns a GUID (Globally Unique ID), also referred to as a UUID (Universally Unique IDentifier), for the management controller. (Optional/Optional)
Broadcast "Get Device ID"	20.9	App	01h	This is a broadcast version of the 'Get Device ID' command that is provided for the 'discovery' of Intelligent Devices on the IPMB. (Mandatory/ Mandatory)
IPMI Messaging Support Commands				
Send Message	22.7	App	34h	The *Send Message* command is used for bridging IPMI messages between channels, and between the system management software (SMS) and a given channel. (Optional/ Optional)
BMC Watchdog Timer				
Reset Watchdog Timer	27.5	App	22h	The *Reset Watchdog Timer* command is used for starting and restarting the Watchdog Timer from the initial countdown value that was specified in the *Set Watchdog Timer* command. (Mandatory/Optional)
Set Watchdog Timer	27.6	App	24h	The *Set Watchdog Timer* command is used for initializing and configuring the watchdog timer. The command is also used for stopping the timer. (Mandatory/Optional)
Get Watchdog Timer	27.7	App	25h	This command retrieves the current settings and present countdown of the watchdog timer. (Mandatory/Optional)

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Command	IPMI Spec	NetFn	CMD	Description (Req'd by PICMG 3.0/2.9)
Event Commands				
Set Event Receiver	29.1	S/E	00h	This global command tells a controller where to send Event Messages. (Mandatory/Optional)
Get Event Receiver	29.2	S/E	01h	This global command is used to retrieve the present setting for the Event Receiver Slave Address and LUN. This command is only applicable to management controllers that act as IPMB Event Generators. (Mandatory/Optional)
Platform Event Message	29.3	S/E	02h	This command may be thought of as a request for the BMC to process the event data that the command contains. Typically, the data will be logged to the System Event Log (SEL). (Mandatory/Optional)
Sensor Device Commands				
Get Device SDR Info	35.2	S/E	20h	This command returns general information about the collection of sensors in a Dynamic Sensor Device. (Mandatory/Optional)
Get Device SDR	35.3	S/E	21h	The 'Get Device SDR' command allows SDR information for sensors for a Sensor Device (typically implemented in a satellite management controller) to be returned. (Mandatory/Optional)
Reserve Device SDR Repository	35.4	S/E	22h	This command is used to obtain a *Reservation ID*. (Mandatory/Optional)

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Command	IPMI Spec	NetFn	CMD	Description (Req'd by PICMG 3.0/2.9)
Set Sensor Hysteresis	35.6	S/E	24h	This command provides a mechanism for setting the hysteresis values associated with the thresholds of a sensor that has threshold based event generation. (Optional/Optional)
Get Sensor Hysteresis	35.7	S/E	25h	This command retrieves the present hysteresis values for the specified sensor. (Optional/ Optional)
Set Sensor Threshold	35.8	S/E	26h	This command is used to set the specified threshold for the given sensor. (Optional/Optional)
Get Sensor Threshold	35.9	S/E	27h	This command retrieves the threshold for the given sensor. (Optional/Optional)
Set Sensor Event Enable	35.10	S/E	28h	This command provides the ability to disable or enable Event Message Generation for individual sensor events. The command is also used to enable or disable sensors in their entirety using the *disable scanning* bit. (Optional/Optional)
Get Sensor Event Enable	35.11	S/E	29h	This command returns the enabled/disabled state for Event Message Generation from the selected sensor. The command also returns the enabled/ disabled state for scanning on the sensor. (Optional/Optional)
Get Sensor Event Status	35.13	S/E	2Bh	The Get Sensor Event Status command is provided to support systems where sensor polling is used in addition to, or instead of, Event Messages for event detection. (Optional/Optional)

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Command	IPMI Spec	NetFn	CMD	Description (Req'd by PICMG 3.0/2.9)
Get Sensor Reading	35.14	S/E	2Dh	This command returns the present reading for sensor. The sensor device may return a stored version of a periodically updated reading, or the sensor device may scan to obtain the reading after receiving the request. (Mandatory/Optional)
Get Sensor Type	35.16	S/E	2Fh	This command is used to retrieve the Sensor Type and Event/Reading Type for the specified sensor. (Optional/ Optional)
FRU Device Commands				
Get FRU Inventory Area Info	34.1	Storage	10h	Returns overall the size of the FRU Inventory Area in this device, in bytes. (Mandatory/ Optional)
Read FRU Data	34.2	Storage	11h	The command returns the specified data from the FRU Inventory Info area. (Mandatory/ Optional)
Write FRU Data	34.3	Storage	12h	The command writes the specified byte or word to the FRU Inventory Info area. (Mandatory/Optional)
OEM Commands				
GET BIOS SEL	N/A	0x30	0x39	GET BIOS ROM SELECT (Read Only) 1: BIOS ROM0 2: BIOS ROM1
ME Lock/Unlock	N/A	0x30	0xF8	This command select ME lock or unlock 0: ME Lock 1: ME UnLock

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Command	IPMI Spec	NetFn	CMD	Description (Req'd by PICMG 3.0/2.9)
LED TEST	N/A	0x30	0xF9	This command controls LED status 0:TBD LED ON 1:TBD LED OFF 2:THERMAL LED ON 3:THERMAL LED OFF 4:WDT LED ON 5:WDT LED OFF
BIOS SEL	N/A	0x30	0xFA	BIOS ROM SELECT 0: BIOS ROM0 1: BIOS ROM1
Operating time	N/A	0x30	0xFB	This command reads the Total Ontime Seconds counter. The returned value specifies the total time in seconds the system has been running in S0 state (4 Byte Ready only). Used ipmitool to verify, LSB on the left
Number of power on cycle	N/A	0x30	0xFC	This command reads the Power Cycle Counter. The returned value specifies the number of times the external power supply has been shut down (including standby voltage, 4 Byte Ready only). Used ipmitool to verify, LSB on the left
Monitor reset causes	N/A	0x30	0xFD	This command returns the cause of the last system restart 0:UNKNOWN (In addition to the following options) 1:WDT reset 2:WDT.power down 3:WDT power cycle 4:HW reset 5:IPMC payload reset 6:Chassis reset
Get System Power State	N/A	0x30	0xFE	Get System Power status 0: S0 1: S5
Payload reset	N/A	0x30	0xFF	Payload reset

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8.3 CompactPCI Address Map

Since more than one system may be installed in a single chassis, we allocate each IPMB address based on GA input as peripheral cards. The CompactPCI Peripheral Address Mapping Table is given below.

CompactPCI Peripheral Address Mapping			
Geo. Addr.	**IPMB Addr.**	**Geo. Addr.**	**IPMB Addr.**
0	**Disabled**	16	D0h
1	B0h	17	D2h
2	B2h	18	D4h
3	B4h	19	D6h
4	B6h	20	D8h
5	B8h	21	DAh
6	Bah	22	DCh
7	BCh	23	DEh
8	BEh	24	E0h
9	Coh	25	E2h
10	C4h	26	E4h
11	C6h	27	E6h
12	C8h	28	E8h
13	CAh	29	EAh
14	CCh	30	ECh
15	CEh	**31**	**Disabled**

8.4 Communications with IPMC

Operating systems need to use a serial port to communicate with the IPMC. The resource setting of the serial port must be IO: 0x2F0 and IRQ:6. The communication setting of the serial port must be BaudRate: 115200, DataBit: 8, ParityCheck: None, Stop-Bit: 1, and FlowControl: None. In Windows 10, use “COM5” to communicate with the IPMC.

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8.5 IPMI Sensors List

Sensor Number	Sensor name	Normal Reading	Remark
01h	BMC Watchdog		
06h	3.3V	3.3 V	
03h	5V	5 V	
02h	12V	12 V	
0Fh	CPU Temp	40°C	
0Eh	System Temp	25°C	

8.6 Relevant Documents

Document Title	Revision	Source
Intelligent Platform Management Interface Specification Second Generation v2.0	Document Revision 1.1 October 1, 2013	https://www.intel.com/content/www/us/en/products/docs/servers/ipmi/ipmi-second-gen-interface-spec-v2-rev1-1.html
PICMG 2.9 D1.0 CompactPCI System Management Specification	January 21, 2000	
Intelligent Platform Management Bus Communications Protocol Specification v0.9	Document Revision 0.15 June 24, 1997	Intel Corp. http://www.intel.com/design/servers/ipmi/license_ipmi.htm

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Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

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- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

A Lithium-type battery may be provided for uninterrupted, backup or emergency power.



Risk of explosion if battery is replaced with one of an incorrect type. Dispose of used batteries appropriately.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

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Getting Service

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