cPCI-6210 Series

6U CompactPCI Processor Blade with Quad-Core Intel® Core™ i7

User's Manual



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Revision History

Revision	Release Date	Description of Change(s)
2.00	23/02/2012	Initial release
2.01	26/03/2012	Correct LAN1/2 locations; LAN3/4 signal names in J3/5 pin definitions; LVDS support note
2.02	14/04/2014	Correct SW9 COM1 setting
2.03	13/11/2014	Add PMC slot -12V support note

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Preface

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Using this Manual

Audience and Scope

The cPCI-6210 User's Manual is intended for hardware technicians and systems operators with knowledge of installing, configuring and operating industrial grade CompactPCI modules.

Manual Organization

This manual is organized as follows:

Chapter 1, Overview: Introduces the cPCI-6210, its features, block diagrams, and package contents.

Chapter 2, Specifications: Presents detailed specification information, and power consumption.

Chapter 3, Functional Description: Describes the cPCI-6210's main functions.

Chapter 4, Board Interfaces: Describes the cPCI-6210 board interfaces, pin definitions, and jumper settings.

Chapter 5, Getting Started: Describes the installation instructions of the cPCI-6210.

Chapter 6, Driver Installation: Describes the driver installation procedures.

Chapter 7, Utilities: Describes the Watchdog Timer and Preboot Execution Environment functions.

Chapter 8, BIOS Setup Utility: Describes the AMI EFI BIOS setup utility.

Chapter 9, IPMI User Guide: Provides relevant information for the baseboard management controller (BMC) of the Intelligent Platform Management Interface (IPMI).

Important Safety Instructions: Presents safety instructions all users must follow for the proper setup, installation and usage of equipment and/or software.

Getting Service: Contact information for ADLINK's worldwide offices.

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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.



NOTE:

Additional information, aids, and tips that help users perform tasks.



CAUTION:

Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.



WARNING:

Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Overview

1.1 Introduction

The cPCI-6210 Series is a 6U CompactPCI single board computer in single-slot (4HP) or dual-slot (8HP) width form factor featuring the 2nd generation Intel® Core™ i7/i5 processors in FCPGA988 socket, with both graphics and memory controllers integrated in the processor. The cPCI-6210 supports dual channel DDR3-1066/1333 SDRAM via two SO-DIMM sockets, up to 16GB. Accompanying the processor is the QM67 Platform Controller Hub.

The 4HP cPCI-6210 provides three GbE ports (one switchable to rear for PICMG 2.16 support), three USB ports, DVI-I, dual-mode DisplayPort, RS-232/422/485 port, and PS/2 KB/MS port on front panel, as well as a standard 7-pin SATA connector and SATA 6 Gb/s port (w/ power) for an onboard 2.5" SATA HDD or Solid State Drive. The 8HP cPCI-6210 provides an additional RS-232 port and a 32-bit/66MHz PMC site or PCIe x8 XMC site. The cPCI-6210 supports dual independent displays and the Display-Port can be converted to DVI, HDMI or VGA output using an adapter cable. A selection of optional Rear Transition Modules (RTM) provide additional I/O functionality including GbE, USB, COM, High Definition Audio and storage interfaces (SATA and SAS with RAID 0/1/5/10 support).

For the dense computing requirements, the cPCI-6210 Series supports operation in both a system slot, and in a peripheral slot as a standalone blade. The cPCI-6210 Series is compliant with the PICMG 2.9 specification and supports system management functions based on the Intelligent Platform Management Interface (IPMI) as well as hardware monitoring of physical characteristics such as CPU and system temperature, DC voltages and power status. With the Intel® Active Management Technology (AMT 7.0), users can manage the cPCI-6210 remotely. To address security requirements, the cPCI-6210 supports Trusted Platform Module 1.2 upon request.

The carefully component selection allows the cPCI-6210 to support extreme temperature environments and provide a long life cycle. The cPCI-6210 Series is ideally suited for military, communications and other industrial applications.

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1.2 Features

- 6U CompactPCI blade in 4HP or 8HP width form factor
- Supports 2nd generation Intel® Core™ i7/i5 processors in FCPGA988 socket (Core™ i7-2710QE: 4 cores, 6M cache, 2.10 GHz)
- Graphics and memory controllers integrated in processor
- Dual channel DDR3-1066/1333/1600 SDRAM via two SODIMM sockets, up to 16GB
- 64bit/66MHz CompactPCI Interface based on PCI specifications, universal V(I/O)
- Supports Satellite mode operation as a standalone blade in peripheral slots
- One 32-bit/66MHz PMC or PCIe x8 XMC site on 8HP version
- Supports IPMI v1.5 for system health monitoring
- One Dual-Mode display port on front panel
- One DVI-I port on front panel
- Three PCIe Gigabit Ethernet ports on front panel
- One SATA interface CFast socket
- 2.5" SATA drive onboard at 6 Gb/s
- Compliant with PICMG 2.0, 2.1, 2.9, 2.16 standards
- Optional TPM support
- Intel AMT support for remote management (only available when system is powered on)

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1.3 Block Diagram

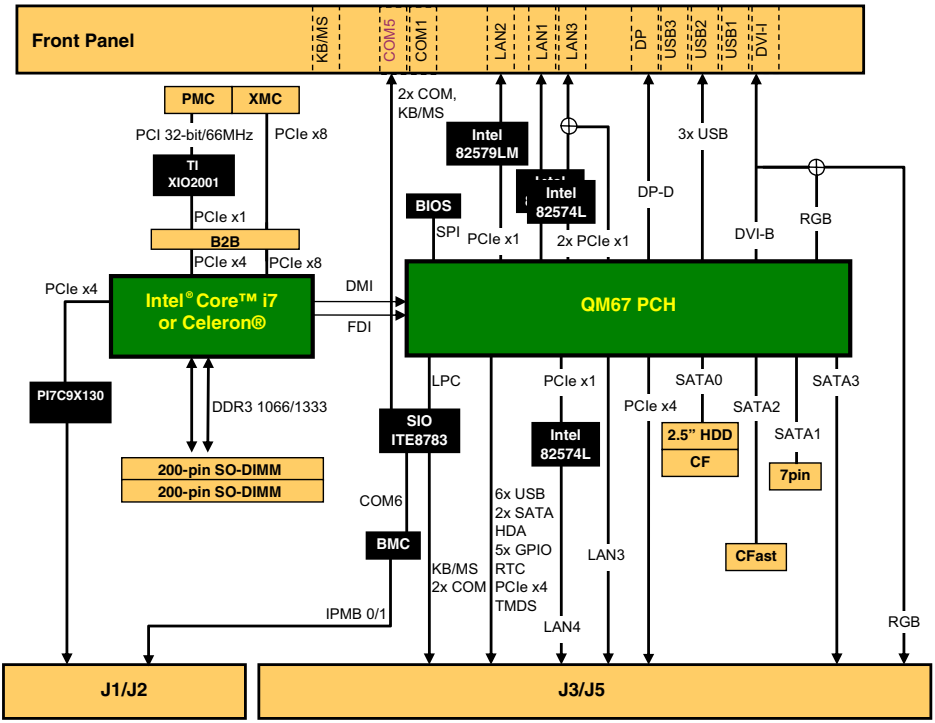


Figure 1-1: cPCI-6210 Series Block Diagram

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1.4 Product List

Products included in the cPCI-6210 Series include:

Processor Blade

- **cPCI-6210:** 4HP width (single-slot) 6U CompactPCI blade featuring single 2nd generation Intel® Core™ i7/i5 processor, dual channel DDR3-1066/1333 SO-DIMM, PS/2 KB/MS, DisplayPort, DVI-I, 3x GbE, 3x USB, COM, SATA ports and CFast socket
- **cPCI-6210D:** 8HP width (dual-slot) 6U CompactPCI blade featuring single 2nd generation Intel® Core™ i7/i5 processor, dual channel DDR3-1066/1333 SO-DIMM, PS/2 KB/MS, DisplayPort, DVI-I, 3x GbE, 3x USB, 2x COM, SATA ports, CFast socket and PMC/XMC site

Rear Transition Modules

- **cPCI-R6002:** 4HP width RTM with DVI-I, 2x COM, 3x USB, 2x GbE, 2x SATA
- **cPCI-R6002D:** 8HP width RTM with DVI-I, 2x COM, 5x USB, 2x GbE, 3x SATA, Mic-in, Line-out, PS/2 KB/MS
- **cPCI-R6100:** 4HP width RTM with 4x GbE, 4x USB, 2x SATA, DVI, VGA, PS/2 KB/MS, CF & SD sockets
- **cPCI-R6110:** 4HP width RTM with 2x GbE, 4x USB, 3x SATA, VGA, PS/2 KB/MS, CF, & SD sockets
- **cPCI-R6200:** 8HP width RTM with 2x GbE, 2x COM, 4x USB, DVI-I, 3x SATA, Mic-in, Line-out, PS/2 KB/MS, 8x SAS
- **cPCI-R6700(D):** 4/8HP width RTM with discrete ATI/AMD E4690 GPU, 2x DVI-I, 2x GbE, 3x USB, 2x COM, KB/MS header, 3x SATA, audio header (8HP version has space for 2.5" SATA drive and PS/2 port on I/O panel)

Adapter Kit

- **DB-CF-SA:** CompactFlash socket kit for cPCI-R6002D & cPCI-R6200 RTMs, including DB-6920CF adapter board, card guide and screws to replace SATA adapter with CompactFlash socket

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1.5 Package Contents

The cPCI-6210 is packaged with the components listed below (RTMs and adapter kits are optional). If any of the items in the contents list are missing or damaged, retain the shipping carton and packing material and contact the dealer for inspection. Please obtain authorization before returning any product to ADLINK. The packing contents of non-standard configurations may vary depending on customer requests.

Processor Blade

- The cPCI-6210 Series Processor Blade
  - CPU and memory specifications will differ depending on options selected
  - Thermal module is assembled onboard
- Y-cable for PS/2 combo port
- 2.5" HDD accessory pack
- DB-9 RS-422/485 converter dongle
- DVI to VGA dongle
- ADLINK All-in-One DVD
- User's manual

Optional Accessories:

- DisplayPort to DVI adapter cable (Part. No. 30-01120-0000)
- DisplayPort to VGA adapter cable (Part. No. 30-01121-0000)
- DisplayPort to HDMI adapter cable (Part No. 30-01119-0000)
- DB-CF-SA: CompactFlash socket kit, including DB-6920CF adapter board, card guide and screws to replace SATA adapter with CompactFlash socket for cPCI-6210, cPCI-R6002D, and cPCI-R6200

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NOTE:

The contents of non-standard cPCI-6210 Series configurations may vary depending on customer requests.



CAUTION:

This product must be protected from static discharge and physical shock. Never remove any of the components except at a static-free workstation. Use the anti-static bag shipped with the product when putting the board on a surface. Wear an anti-static wrist strap properly grounded on one of the system's ESD ground jacks when installing or servicing system components.

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2 Specifications

2.1 cPCI-6210 Specifications

CompactPCI Standard	PICMG® 2.0 CompactPCI® Rev. 3.0 PICMG® 2.1 Hot Swap Specification Rev.2.0 PICMG® 2.9 System Management Bus Rev. 1.0 PICMG® 2.16 Packet Switching Backplane Rev.1.0
Mechanical	Standard 6U CompactPCI®
	Board size: 233.23 mm x 160mm
	cPCI-6210: Single slot (4HP, 20.32mm) width with single slot height heatsink **cPCI-6210D:** Dual slot (8HP, 40.64mm) width with dual slot height heatsink
	CompactPCI® connectors J1, J2, J3 and J5
Processor	2nd Generation Intel® Core™ processors in FCPGA988 socket with passive heatsink • Core™ i7-2710QE, 2.1 GHz, 6MB LLC cache, TDP 45W • Core™ i7-2515E, 2.5 GHz, 3MB LLC cache, TDP 35W • Celeron® B810, 1.6 GHz, 2MB LLC cache, TDP 35W
Chipset	Intel® QM67 Platform Controller Hub (PCH)
Memory	Dual channel DDR3-1066/1333/1600 memory Two SO-DIMM sockets Up to 16GB (dependent on availability of memory modules)
CompactPCI Bus	PCI 64-bit/ 66MHz; 3.3V, 5V universal V(I/O) Supports operation in system slot as master or in peripheral slot as standalone blade without connectivity to CompactPCI bus (Satellite mode)
PMC/XMC	One 32-bit/66MHz PMC site or PCIe x8 XMC site provided by DB-6210L2 riser card (8HP version only)
Graphics	Integrated in Intel® processor One DVI-I port on front panel (digital and analog signals), RGB signal switchable to J3; 2nd DVI port routed to J5 One Dual-mode DisplayPort on front panel and can be converted to DVI/HDMI/VGA via adapter cables, supports resolutions up to 2560x1600 @60Hz Analog support up to QXGA 2048x1536 @75Hz, 32-bit Dual independent display support

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Ethernet	Up to four 10/100/1000BASE-T ports One Intel® 82579LM PHY controller for LAN2 and three PCIe x1 Intel® 82574L GbE controllers for LAN1/3/4 LAN1/2/3 on front panel and LAN3 switchable to J3 for PICMG 2.16 support LAN4 routed to J3 for PICMG 2.16
Serial Ports	Up to four serial ports One RS-232/422/485 serial port[1] on front panel, additional RS-232 port onboard (output to front panel by cable in cPCI-6210D version) Two serial ports routed to rear I/O
USB	Up to three USB 2.0 front panel ports and six ports routed to rear I/O
Audio	High Definition Audio signals routed to rear I/O
TPM	TPM support available on request (Infineon SLB 9635 TT1.2) • Over/Under voltage detection • Low/High frequency sensor/filter • Reset filter • Memory Encryption/Decryption (not available on Ext. Temp. versions)
Faceplate I/O	**4HP: cPCI-6210** 3x USB 2.0 ports 3x 10/100/1000BASE-T Ethernet ports DVI-I port (digital + analog) Dual-mode DisplayPort PS/2 Keyboard/Mouse DB-9 COM port
	8HP: cPCI-6210D 3x USB 2.0 ports 3x 10/100/1000BASE-T Ethernet ports DVI-I port (digital + analog) Dual-mode DisplayPort PS/2 Keyboard/Mouse 2x DB-9 COM ports PMC/XMC slot
Storage Interfaces	• CFast Type I or II socket onboard • Optional CompactFlash socket onboard[2] • One SATA 6 Gb/s direct connector for 2.5" onboard HDD/SDD • One 7-pin SATA 6 Gb/s port onboard for external HDD/SDD

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BIOS	AMI® EFI BIOS 64Mbit SPI flash memory
OS Support	Microsoft Windows XP Professional Microsoft Windows 7 64-bit Red Hat Enterprise Linux 6 64-bit Fedora 14 32-bit Other OS support on request
Operating Temperature[3] (w/ forced airflow)	Standard: 0°C to 60°C Extended Temperature: -40°C to +70°C Extreme Extended Temperature*: -40°C to +85°C (*Core™ i7-2510E or Celeron® B810, 8HP only)
Storage temperature	-40°C to 85°C
Humidity	95% @60°C non-condensing
Shock	15G peak-to-peak, 11ms duration, non-operating
Vibration[4]	Operating: 2Grms. 5 to 500Hz, each axis (without HDD)
Compliance	CE EN55022, FCC Class A

Table 2-1: cPCI-6210 Specifications

Notes:

1. A DB-9-to-DB-9 dongle to convert the cPCI-6210G RS-422/485 pin definitions to common definitions is included in the package (see page 29).
2. The SATA direct connector is removable (DB-6920SAT) and can be replaced with a CompactFlash socket adapter (DB-6920CF). A CompactFlash card and SATA drive cannot be used simultaneously.
3. ADLINK-certified thermal design. The thermal performance is dependent on the chassis cooling design. Sufficient forced air-flow is required (see 2.4 "Thermal Requirements" on page 13). Temperature limit of optional mass storage devices may affect the thermal specification.
4. The storage device limits the operating vibration tolerance. When the application requires a higher specification for anti-vibration, it is recommended to use a flash storage device.


NOTE:

Specifications are subject to change without prior notice.

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2.2 I/O Connectivity

cPCI-6210 Processor Blade

Function	cPCI-6210		cPCI-6210D		RTM[1]
	Faceplate	Board	Faceplate	Board	J3/J5
Gigabit Ethernet	Y x3		Y x3		Y x2[2]
COM	Y		Y x2		Y x2
USB 2.0	Y x3		Y x3		Y x6
DVI-I	Y		Y		Y (DVI-D)
RGB					Y (RGB) [3]
DP	Y		Y		
SATA		Y x2		Y x2	Y x2
CFast		Y		Y	
CF		Y[4]		Y[4]	
PS/2 KB/MS	Y		Y		Y
HDA					Y
LEDs	Y x4		Y x4		
Reset Button	Y		Y		

Table 2-2: cPCI-6210 I/O Connectivity

Notes:

1. Signals are passed through to the RTM. Available functions are dependent on the specific RTM model.
2. LAN3 is switched from front panel
3. Switched from front panel.
4. Available when SATA direct connector (DB-6920SAT) is replaced with a CompactFlash socket adapter (DB-6920CF). A CF card and SATA drive cannot be used simultaneously.

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2.3 Power Requirements

In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. **An industrial power supply unit should be able to provide at least twice as much power as the entire system requires of each voltage**. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.

The tolerance of the voltage lines described in the CompactPCI specification (PICMG 2.0 R3.0) is +5%/ -3% for 5, 3.3 V and ±5% for ±12V. This specification is for power delivered to each slot and it includes both the power supply and the backplane tolerance.

Voltage	Nominal Value	Tolerance	Max. Ripple (P - P)
5V	+5.0 VDC	+5% / -3%	50 mV
3.3V	+3.3 VDC	+5% / -3%	50 mV
+12V	+12 VDC	+5% / -5%	240 mV
-12V	-12 VDC	+5% / -5%	240 mV
V I/O (PCI I/O Buffer Voltage)	+3.3 VDC or +5 VDC	+5% / -3%	50 mV
GND			

Table 2-3: CompactPCI Input Voltage Characteristics

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Power Consumption

This section provides information on the power consumption of the cPCI-6210 Series with different CPUs, 2x 4GB DDR3-1066 SO-DIMM memory and onboard 160GB SATA hard disk. The cPCI-6210 is powered by 5V and 3.3V. Power consumption at 100% CPU usage was measured by running the Intel Thermal Analysis Tool (TAT) and Turbo Boost and Hyper-Threading Technology were enabled.

Intel® Core i7-2710QE			
OS/Mode	**Current 5V**	**Current 3.3v**	**Total Power**
DOS/Idle mode	2.54 A	1.36 A	17.2 W
Windows XP/Idle mode	2.43 A	1.34 A	16.6 W
Windows® XP, CPU 100% Usage	13.56 A	1.36 A	72.3 W

Intel® Core i7-2510E			
OS/Mode	**Current 5v**	**Current 3.3v**	**Total Power**
DOS/Idle mode	2.10 A	1.35 A	15.0 W
Windows XP/Idle mode	1.68 A	1.31 A	12.7 W
Windows® XP, CPU 100% Usage	7.90 A	1.35 A	44.0 W

Intel® Celeron B810			
OS/Mode	**Current 5V**	**Current 3.3v**	**Total Power**
DOS/Idle mode	2.89 A	1.64 A	19.9 W
Windows XP/Idle mode	1.79 A	1.41 A	13.6 W
Windows® XP, CPU 100% Usage	4.25 A	1.46 A	26.1 W



Measurements were made with Intel® Turbo Boost and Hyper-Threading Technology enabled

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2.4 Thermal Requirements

This section provides information on the thermal requirements of the cPCI-6210 Series. Cooling of the board and its components is provided by the thermal module (passive heatsink) and is dependent on sufficient airflow from the chassis.

The amount of thermal energy that can by dissipated from the board is dependent on the ambient air temperature and the airflow rate of the chassis. To provide the user with guidelines for the upper limits of operating conditions for the cPCI-6210, the following sections give information on the maximum ambient air temperature as a function of airflow rate for a given level of power consumption.

Power Dissipation Graphs

The graphs shown below illustrate the level of CPU power dissipation that can be maintained dependent on ambient air temperature and airflow rate. One graph is provided for each CPU supported by the cPCI-6210(D). The curves on each graph indicate the upper limits of operating conditions under which the CPU will not be affected by its thermal management and protection systems at a given percentage of maximum CPU loading.

The CPU's thermal management and protection systems begin to take effect when the CPU temperature exceeds the maximum junction temperature ($T_{j,Max}$=100°C). When the ambient air temperature and airflow rate are in the ranges below the curves on the graphs, the CPU temperature will remain below $T_{j,Max}$ and the CPU will be able to operate at full performance (i.e. not limited by thermal management).

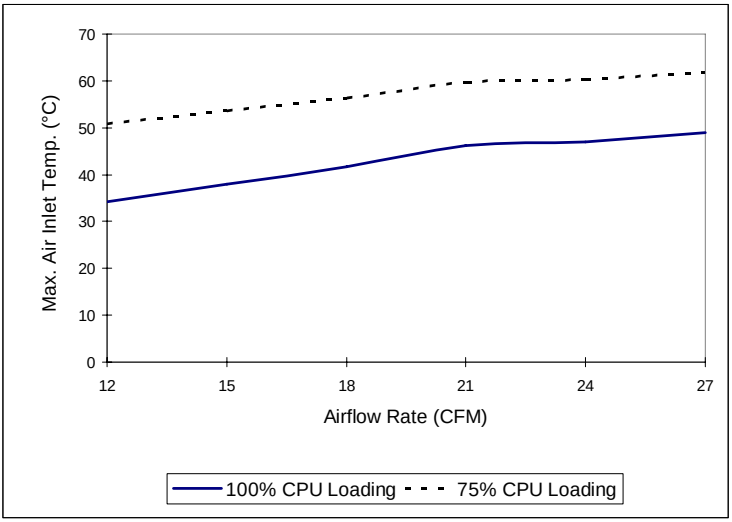
The power dissipation graphs show two curves:

- 100% CPU loading
- 75% CPU loading

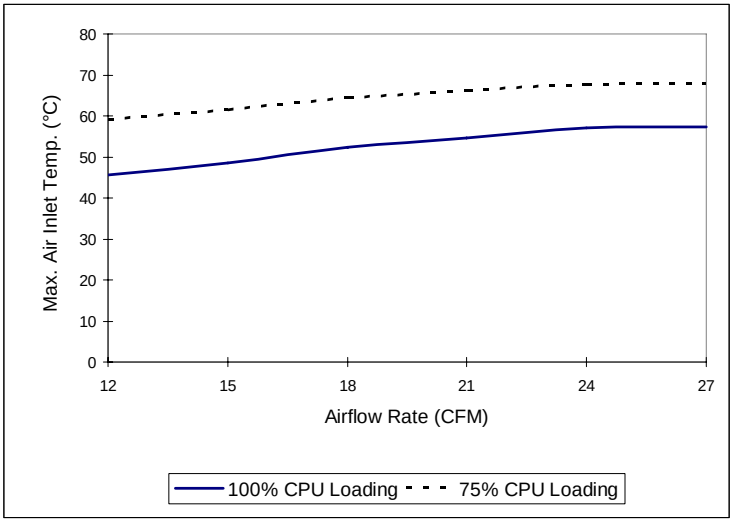
The detailed specifications for each processor can be found in Section 3.1 "Processor" on page 17.

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Intel® Core™ i7-2710QE (cPCI-6210)

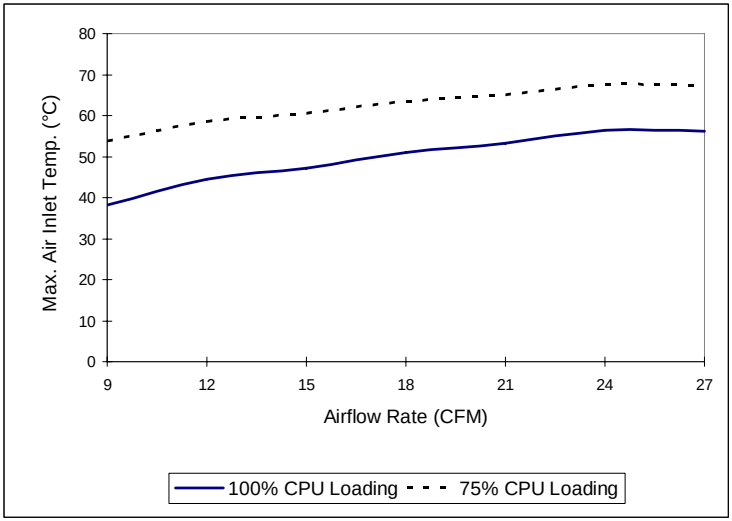


Intel® Core™ i7-2710QE (cPCI-6210D)

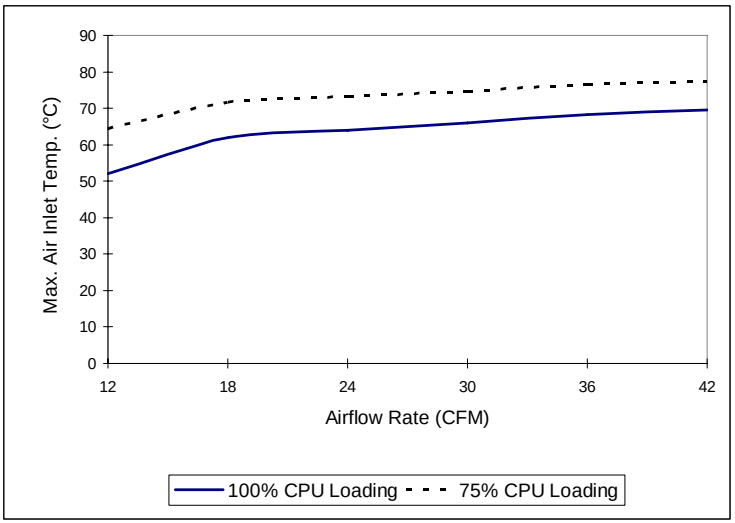


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Intel® Core™ i5-2510E (cPCI-6210)



Intel® Core™ i5-2510E (cPCI-6210D)



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3 Functional Description

The following sections describe the cPCI-6210 Series features and functions.

3.1 Processor

Intel® Core™ i7 Processor

The 2nd Generation Intel® Core™ processor family mobile and Intel® Celeron® processor family mobile are the next generation of 64-bit, multi-core mobile processor built on 32- nanometer process technology. Based on a new micro-architecture, the processor is designed for a two-chip platform. The two-chip platform consists of a processor and Platform Controller Hub (PCH). The platform enables higher performance, lower cost, easier validation, and improved x-y footprint. The processor includes Integrated Display Engine, Processor Graphics and Integrated Memory Controller.

The following table lists the processors supported by the cPCI-6210 Series and their specifications.

Features	Core™ i7-2710QE	Core™ i7-2515E	Celeron® B810
Clock	2.1GHz	2.5GHz	1.6GHz
Max. Single Core Turbo Freq.	3GHz	3.2GHz	N/A
Last Level Cache	6MB	3MB	2MB
No. of Cores/Threads	4/8	2/4	2/2
Max. Power (TDP[1])	45W	35W	35W
$T_{j, Max}$[2]	100°C	100°C	100°C

Notes:

1. The highest expected sustainable power while running known power intensive applications. TDP is not the maximum power that the processor can dissipate.
2. Maximum junction temperature ($T_{j,Max}$). The maximum supported operating temperature.

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Supported Technologies

- Intel® Virtualization Technology for Directed I/O (Intel® VT-d)
- Intel® Virtualization Technology (Intel® VT-x)
- Intel® Hyper-Threading Technology
- Intel® 64 Architecture
- Execute Disable Bit
- Intel® Turbo Boost Technology

Interfaces

- Two channels of DDR3 memory with a maximum of one SO-DIMM per channel
- Memory DDR3 data transfer rates of 1066 MT/s, 1333 MT/s, and 1600 MT/s
- 64-bit wide channels
- DDR3 I/O Voltage of 1.5 V
- 1Gb, 2Gb, and 4Gb DDR3 DRAM technologies are supported for x8 and x16 devices
  - Using 4Gb device technologies, the largest memory capacity possible is 16 GB, assuming dual-channel mode with two x8, dual-ranked, un-buffered, non-ECC, SO-DIMM memory configuration.
- The PCI Express port(s) are fully-compliant with the PCI Express Base Specification, Revision 2.0.
- 5 GT/s point-to-point DMI interface to PCH is supported
- The Processor Graphics contains a refresh of the sixth generation graphics core
- enabling substantial gains in performance and lower power consumption.
- DX10.1, DX10, DX9 support
- OGL 3.0 support
- FDI carries display traffic from the Processor Graphics in the processor to the legacy display connectors in the PCH

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3.2 Chipset

Mobile Intel® QM67 Express Chipset

The cPCI-6210 Series is equipped with the Mobile Intel® QM67 Express Chipset, also referred to as PCH (Platform Controller Hub), to provide extensive I/O support. Functions and capabilities include:

- PCI Express Base Specification, Revision 2.0 support for up to eight ports with transfer rate up to 5 GT/s
- ACPI Power Management Logic Support, Revision 4.0a
- Enhanced DMA controller, interrupt controller, and timer functions
- Integrated Serial ATA host controllers with independent DMA operation on up to six ports
- USB host interface with two EHCI high-speed USB 2.0 Host controllers and two rate matching hubs provide support for up to fourteen USB 2.0 ports
- Integrated 10/100/1000 Gigabit Ethernet MAC with System Defense
- System Management Bus (SMBus) Specification, Version 2.0 with additional support for I2C devices
- Supports Intel® High Definition Audio
- Supports Intel® Rapid Storage Technology
- Supports Intel® Virtualization Technology for Directed I/O
- Integrated Clock Controller
- Analog and Digital Display ports
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support
- Serial Peripheral Interface (SPI) support

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3.3 PMC/XMC

The cPCI-6210D Series supports one PMC or XMC site for front panel I/O expansion. The PMC site provides a maximum 32-bit/66MHz PCI bus link using a TI XIO2001 PCIe-to-PCI bridge and PCIe x1 link. The PMC site supports +3.3V and 5V signaling. The XMC site provides a x8 PCIe lane.

3.4 Intel® Turbo Boost Technology

Intel Turbo Boost Technology is a feature that allows the processor to opportunistically and automatically run faster than its rated operating core and/or render clock frequency when there is sufficient power headroom, and the product is within specified temperature and current limits. The Intel Turbo Boost Technology feature is designed to increase performance of both multi-threaded and single-threaded workloads. The processor supports a Turbo mode where the processor can use the thermal capacity associated with package and **run at power levels higher than TDP power for short durations**. This improves the system responsiveness for short, bursty usage conditions.

Turbo Mode availability is independent of the number of active cores; however, the Turbo Mode frequency is dynamic and dependent on the instantaneous application power load, the number of active cores, user configurable settings, operating environment, and system design. If the power, current, or thermal limit is reached, the processor will automatically reduce the frequency to stay with its TDP limit.

3.5 Intel® Hyper-Threading Technology

Intel® Hyper-Threading Technology allows an execution core to function as two logical processors. While some execution resources (such as caches, execution units, and buses) are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled using the BIOS and requires operating system support. Intel recommends enabling Hyper-Threading Technology with Microsoft Windows 7, Vista, and XP, and disabling Hyper-Threading Technology using the BIOS for all previous versions of Windows operating systems.

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3.6 Trusted Platform Module

Upon request, the cPCI-6210 supports the Infineon SLB 9635 TT 1.2 Trusted Platform Module (TPM), a security controller with cryptographic functionality that provides users a secure environment in e-commerce transactions and Internet communications.

The key features the TPM provides are:

- Hardware hash accelerator for SHA-1 algorithm.
- Advanced Crypto Engine (ACE) for asymmetric key operations (up to 2048-bit key length) to make hardware protection.
- Tick counter to extend the time required to decipher the key.

In addition to an encryption key created by the user, the TPM also provides security features to protect the TPM itself:

- Over/Under-voltage detection to monitor the system stability. If the voltage fluctuates dramatically, this function can block the data transfer and lock the chip.
- Low/High frequency sensor to detect the IC clock frequency. If the frequency fluctuates dramatically, this function can block the data transfer and lock the chip.
- Reset filter to filter reset signal in order to break the time set by tick counter is received.
- Memory encryption to protect memory.
- Physical shield in the IC to protect the die from intruding or hacking by matching the data transferred on the 2 layer metal shield on the IC. If the data is not matched, the IC may be blocked.



The TPM does not support operation below 0ºC. Below this temperature, the system may not boot. As a result, the Extended Temperature versions of the cPCI-6210 are not available with TPM.

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3.7 Battery

The cPCI-6210 is equipped with a 3.0V "coin cell" lithium battery for the Real Time Clock (RTC). The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. A Rayovac BR2032 with -40°C to +85°C operating temperature support is equipped on board by default

3.8 Intel® Active Management Technology

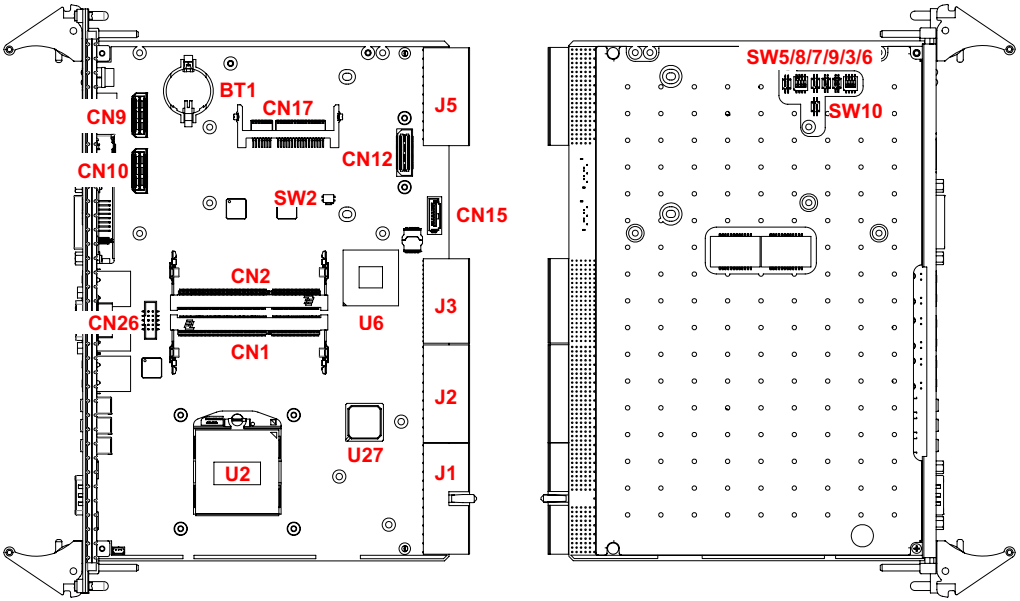
Intel® Active Management Technology (Intel® AMT) is a hardware based technology for remotely managing and securing PCs out-of-band. Intel® AMT includes hardware-based remote management, security, power-management, and remote-configuration features. Intel® AMT allows remote access to a system when traditional techniques and methods are not available.

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4 Board Interfaces

This chapter describes the board layout, connector pin assignments, and jumper settings of the cPCI-6210 Series.

4.1 cPCI-6210(D) Series Board Layout



U2	CPU	**CN15**	SATA port (7-pin)
U6	QM67 PCH	**CN17**	CFast socket
U27	PCIe-to-PCI Bridge	**CN26**	COM5 box header
CN1/2	DDR3 SO-DIMM sockets	**BT1**	RTC Battery
CN9/10	DB-6210L2 connectors (cPCI-6210D only)	**J1-5**	CompactPCI connectors
		SW2	Clear CMOS Switch
CN12	DB-6920SAT connector	**SW3~10**	DIP Switches

Figure 4-1: cPCI-6210(D) Series Board Layout

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4.2 cPCI-6210D Assembly Layout

The dual-slot width cPCI-6210D is comprised of the cPCI-6210 single-slot main board and the DB-6210L2 riser card to provide a PMX/XMC site

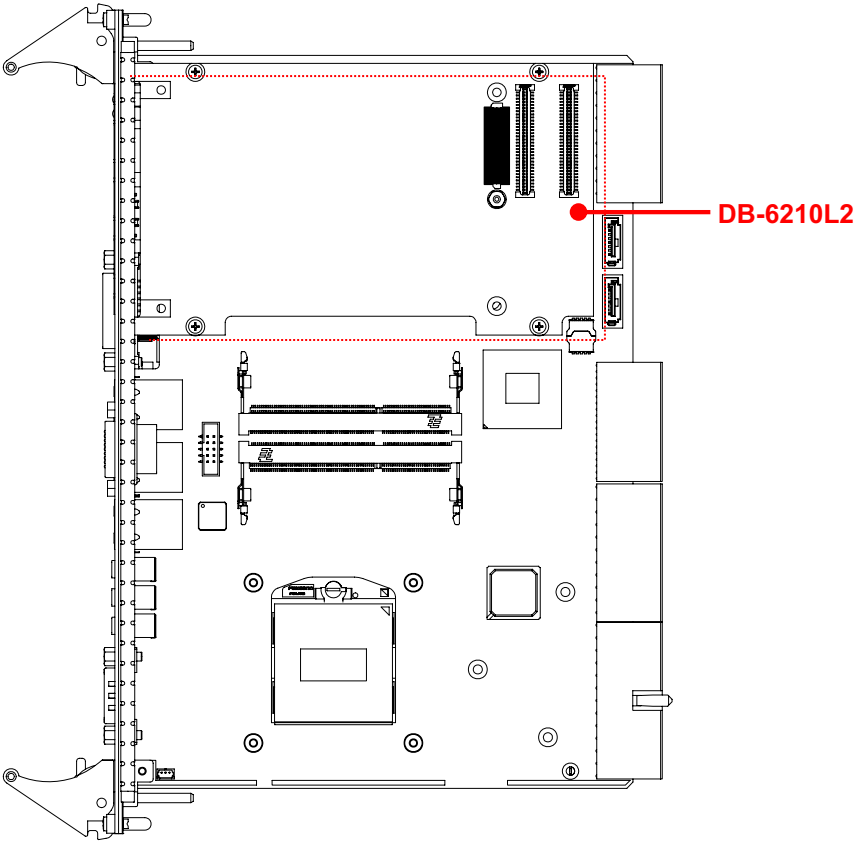
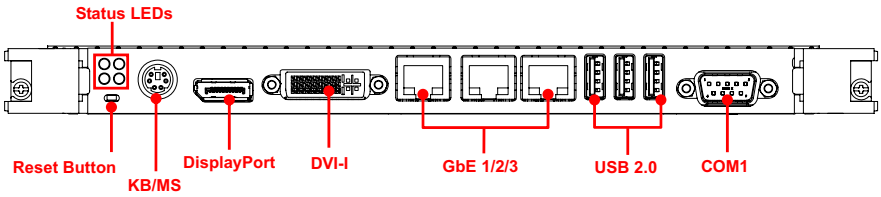


Figure 4-2: cPCI-6210D Assembly Layout

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4.3 cPCI-6210(D) Front Panel

cPCI-6210



cPCI-6210D

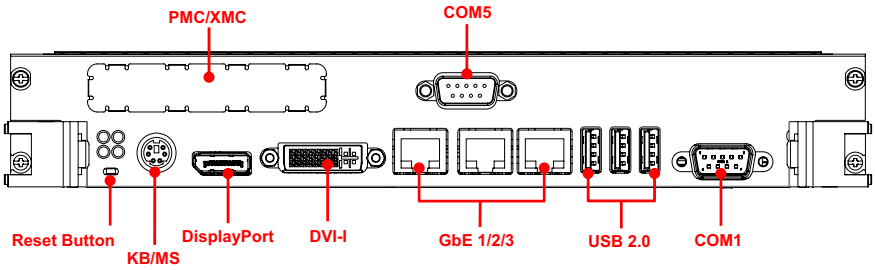
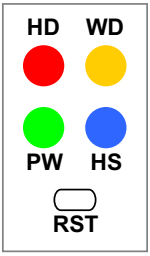


Figure 4-3: cPCI-6210(D) Front Panel Layout

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Status LEDs



LED	Color	Condition	Indication
Power (PW)	Green	Off	System is off
		On	System is on
Hot Swap (HS)	Blue	Off	Handles closed, System is on
		Fast Blink	Preparing to shut down system (LED: 0.1s on, 0.9s off)
		On	Handles open and blade ready to be removed
		Slow Blink[1]	Voltages out of tolerance: 3.3V, 5V, 12V, 1.5V over ±5% (LED: 2s on, 1s off)
HDD (HD)	Red	Off	No drive activity
		Blinking	SATA HDD, CFast, CF data read/write in process
WDT (WD)	Amber	Off	No Watchdog event
		On/Blinking	Watchdog event alert (activity dependent on WDT programming)

Table 4-1: cPCI-6210 Front Panel Status LED Descriptions

1. Disabled by default. See “OemSetBlueLEDLongBlinking” on page 116.

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4.4 Connector Pin Assignments

Refer to "cPCI-6210(D) Series Board Layout" on page 23 and "cPCI-6210(D) Front Panel Layout" on page 25 for connector locations

USB Connectors

Pin #	Signal Name
1	Vcc
2	UV0-
3	UV0+
4	GND

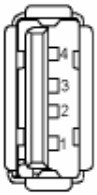
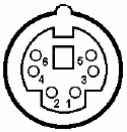


Table 4-2: USB Connector Pin Definition

PS/2 Keyboard/Mouse Port

Pin #	Signal	Function
1	KBDAT	Keyboard Data
2	MSDAT	Mouse Data
3	GND	Ground
4	+5V	Power
5	KBCLK	Keyboard Clock
6	MSCLK	Mouse Clock



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RJ-45 Gigabit Ethernet Connectors

Pin #	10BASE-T/ 100BASE-TX	1000BASE-T
1	TX+	LAN_TX0+
2	TX-	LAN_TX0-
3	RX+	LAN_TX1+
4	--	LAN_TX2+
5	--	LAN_TX2-
6	RX-	LAN_TX1-
7	--	LAN_TX3+
8	--	LAN_TX3+

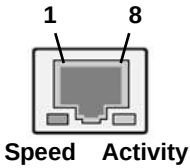


Table 4-3: GbE Connector Pin Definitions

Status		Speed LED (Green/Amber)	Activity LED (Amber)
Network link is not established or system powered off		OFF	OFF
10 Mbps	Link	OFF	ON
	Active	OFF	Blinking
100 Mbps	Link	Green	ON
	Active	Green	Blinking
1000 Mbps	Link	Amber	ON
	Active	Amber	Blinking

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COM1 Connector (DB-9)

Pin #	RS-232	RS-422	RS-485
1	DCD-L	—	—
2	RXD	RXD-	—
3	TXD	TXD-	TXD-
4	DSR-L	—	—
5	Ground	—	—
6	DSR-L	—	—
7	RTS-L	TXD+	TXD+
8	CTS-L	RXD+	—
9	—	—	—

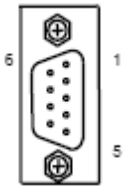


Table 4-4: COM1 Connector Pin Definition

NOTE: The COM1 RS-422/485 pin definitions are different from the common DB-9 pin definitions. An RS-422/485 DB-9 male-female adapter dongle is provided to allow compatibility with common RS-422/485 pin definitions.

RS-422/485 Adapter Dongle

A DB-9 male-female adapter dongle is provided to allow compatibility with common RS-422/485 pin definitions

DB-9 (Female) Signal Name	Pin #	DB-9 (Male) Signal Name
NC	1	TXD-
RXD-	2	TXD+
TXD-	3	RXD+
NC	4	RXD-
NC	5	NC
NC	6	NC
TXD+	7	NC
RXD+	8	NC
NC	9	NC

Table 4-5: RS-422/485 Adapter Dongle Pin Definition

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COM1 Connector with RS-422/485 Dongle (DB-9)

Pin #	RS-422	RS-485
1	TXD-	TXD-
2	TXD+	TXD+
3	RXD+	—
4	RXD-	—
5	—	—
6	—	—
7	—	—
8	—	—
9	—	—

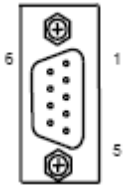


Table 4-6: COM1 Connector with RS-422/485 Dongle Pin Definition

COM5 Box Header

Pin #	RS-232
1	DCD-L
2	DSR-L
3	RXD
4	RTS-L
5	TXD
6	CTS-L
7	DTR-L
8	RI-L
9	Ground
10	NC

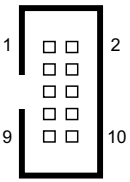


Table 4-7: COM5 Box Header Definition

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COM5 Connector (DB-9)

Pin #	RS-232
1	DCD-L
2	RXD
3	TXD
4	DSR-L
5	Ground
6	DSR-L
7	RTS-L
8	CTS-L
9	RI-L

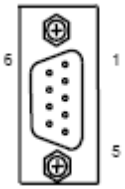
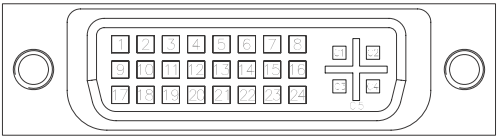


Table 4-8: COM5 Connector Pin Definition

NOTE: The COM5 DB-9 front panel connector is only available on the cPCI-6210D (8HP) version.

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DVI-I Connector



Pin #	Signal	Pin #	Signal
1	TMDS Data2-	16	Hot Plug Detect
2	TMDS Data2+	17	TMDS Data0-
3	GND	18	TMDSData0+
4	NC	19	GND
5	NC	20	NC
6	DDC Clock [SCL]	21	NC
7	DDC Data [SDA]	22	GND
8	Analog vertical sync	23	TMDS Clock +
9	TMDS Data1-	24	TMDS Clock -
10	TMDS Data1+	C1	Analog Red
11	GND	C2	Analog Green
12	NC	C3	Analog Blue
13	NC	C4	Analog Horizontal Sync
14	+5 V Power	C5	Analog GND Return
15	GND		

Table 4-9: DVI-I Connector Pin Definition

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DisplayPort Connector

Pin #	Signal	Pin #	Signal
1	CN_DP0_P	2	Ground
3	CN_DP0_N	4	CN_DP1_P
5	Ground	6	CN_DP1_N
7	CN_DP2_P	8	Ground
9	CN_DP2_N	10	CN_DP3_P
11	Ground	12	CN_DP3_N
13	CN_CAD-L	14	CN_CEC
15	CN_AUX_P	16	Ground
17	CN_AUX_N	18	DDP_HPD
19	Ground	20	P3V3

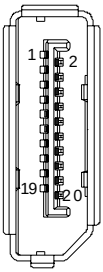


Table 4-10: DisplayPort Pin Definition

Serial ATA Connector (CN15)

Pin #	Signal
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

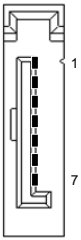


Table 4-11: Serial ATA Connector Pin Definition

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CFast Socket (CN17)

Pin #	Signal Name
Ground	S1
SATA_TX-P	S2
SATA_TX-N	S3
Ground	S4
SATA_RX-N	S5
SATA_RX-P	S6
Ground	S7
CFast_CDI	P1
Ground	P2
NC	P3
NC	P4
NC	P5
NC	P6
Ground	P7
CFast_LED1	P8
CFast_LED2	P9
NC	P10
NC	P11
NC	P12
P3V3	P13
P3V3	P14
Ground	P15
Ground	P16
CFast_CDO	P17

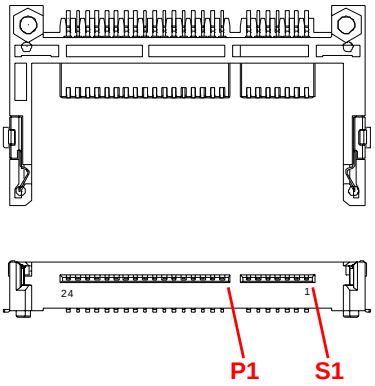


Table 4-12: CFast Socket Pin Definition

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Serial ATA Connector on DB-6920SAT

Pin #	Signal
S1	GND
S2	TX+
S3	TX-
S4	GND
S5	RX-
S6	RX+
S7	GND
P1	NC
P2	NC
P3	NC
P4	GND
P5	GND
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P7	5V
P8	5V
P9	5V
P10	GND
P11	NC
P12	GND
P13~P15	NC

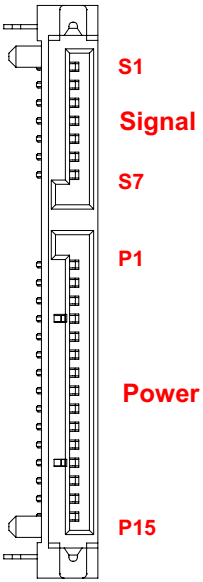


Table 4-13: DB-6920SAT SATA Connector Pin Definition

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DB-6920SAT Connector (CN12)

Signal Name	Pin #	Pin #	Signal Name
GND	1	2	GND
GND	3	4	GND
GND	5	6	GND
GND	7	8	GND
GND	9	10	GND
GND	11	12	GND
GND	13	14	GND
GND	15	16	GND
GND	17	18	GND
GND	19	20	GND
GND	21	22	GND
GND	23	24	GND
GND	25	26	GND
GND	27	28	GND
GND	29	30	GND
P3V3	31	32	P5V
P3V3	33	34	P5V
P3V3	35	36	P5V
P3V3	37	38	P5V
P1V8	39	40	12V
P1V8	41	42	12V
P1V8	43	44	12V
GND	45	46	GND
GND	47	48	SATA-TXN0
GND	49	50	SATA-TXP0
SATA-RXN0	51	52	GND
SATA-RXP0	53	54	GND
GND	55	56	RESET#
GND	57	58	GND
GND	59	60	GND

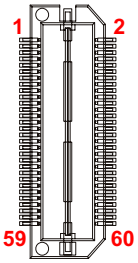


Table 4-14: DB-6920SAT Connector Pin Definition

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PMC Connectors on DB-6210L2 (JN1, JN2)

Pin#	JN1 Signal	JN2 Signal
1	PMC_TCK	P12V
2	N12V*	PMC_TRST-L
3	GND	PMC_TMS
4	PCIX_INTA-L	NC (PMC_TDO)
5	PCIX_INTB-L	PMC_TDI
6	PCIX_INTC-L	GND
7	PMC_MOD-L1	GND
8	P5V	NC
9	PCIX_INTD-L	NC
10	NC	NC
11	GND	PMC_MOD-L2
12	P3V3_PMCAUX	P3V3
13	CLK66_PCIX_PMC	PMC_RST-L
14	GND	PMC_MOD-L3
15	GND	P3V3
16	PCIX_GNT-L0	PMC_MOD-L4
17	PCIX_REQ-L0	PMC_PME-L
18	P5V	GND
19	PMC_VIO	PCIX_AD30
20	PCIX_AD31	PCIX_AD29
21	PCIX_AD28	GND
22	PCIX_AD27	PCIX_AD26
23	PCIX_AD25	PCIX_AD24
24	GND	PCIX_AD23
25	GND	PMC_IDSEL
26	PCIX_CBE-L3	PCIX_AD23
27	PCIX_AD22	P3V3
28	PCIX_AD21	PCIX_AD20
29	PCIX_AD19	PCIX_AD18
30	P5V	GND
31	PCIX_FRAME-L	PCIX_AD16
32	PCIX_AD17	PCIX_CBE-L2

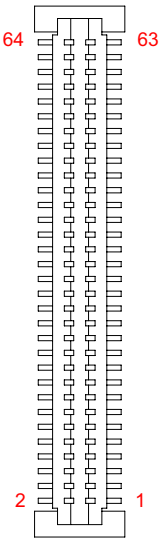


Table 4-15: PMC Connector Pin Definitions

***Note:** -12V signal not supported on JN1 pin 2. Contact ADLINK for more information.

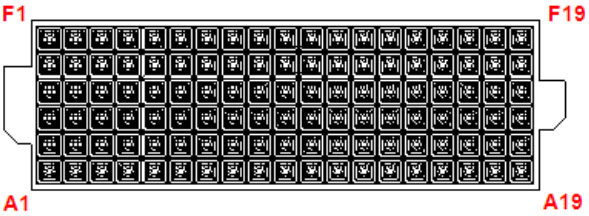
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Pin#	JN1 Signal	JN2 Signal
33	PCIX_FRAME-L	GND
34	GND	NC
35	GND	PCIX_TRDY-L
36	PCIX_IRDY-L	P3V3
37	PCIX_DEVSEL-L	GND
38	P5V	PCIX_STOP-L
39	PCIX_PCIXCAP	PCIX_PERR-L
40	PCIX_LOCK-L	GND
41	NC	P3V3
42	NC	PCIX_SERR-L
43	PCIX_PAR	PCIX_CBE-L1
44	GND	GND
45	PMC_VIO	PCIX_AD14
46	PCIX_AD15	PCIX_AD13
47	PCIX_AD12	PCIX_M66EN
48	PCIX_AD11	PCIX_AD10
49	PCIX_AD9	PCIX_AD8
50	P5V	P3V3
51	GND	PCIX_AD7
52	PCIX_CBE-L0	NC
53	PCIX_AD6	P3V3
54	PCIX_AD5	NC
55	PCIX_AD4	NC
56	GND	GND
57	PMC_VIO	NC
58	PCIX_AD3	NC
59	PCIX_AD2	GND
60	PCIX_AD1	NC
61	PCIX_AD0	PCIX_ACK64-L
62	P5V	P3V3
63	GND	GND
64	PCIX_REQ64-L	NC

Table 4-15: PMC Connector Pin Definitions (cont'd)

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XMC Connector on DB-6210L2



Pin#	A	B	C	D	E	F
1	RXP	RXN	3.3V	NC	NC	VPWR
2	GND	GND	Not used	GND	GND	PCIE_RST-L
3	NC	NC	3.3V	NC	NC	VPWR
4	GND	GND	Not used	GND	GND	Not used
5	NC	NC	3.3V	NC	NC	VPWR
6	GND	GND	Not used	GND	GND	+12V
7	NC	NC	3.3V	NC	NC	VPWR
8	GND	GND	Not used	GND	GND	-12V
9	NC	NC	Not used	NC	NC	VPWR
10	GND	GND	Not used	GND	GND	GA0
11	TXP	TXN	Not used	NC	NC	VPWR
12	GND	GND	GA1	GND	GND	Not used
13	NC	NC	3.3V	NC	NC	VPWR
14	GND	GND	GA2	GND	GND	Not used
15	NC	NC	Not used	NC	NC	VPWR
16	GND	GND	Not used	GND	GND	Not used
17	NC	NC	Not used	NC	NC	NC
18	GND	GND	Not used	GND	GND	Not used
19	CK-P	CK-N	Not used	Not used	Not used	Not used

Table 4-16: XMC Connector Pin Definition

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DB-6210L2 Connector (CN9)

Signal Name	Pin #	Pin #	Signal Name
GND	2	1	GND
PCIE_A_RXP0	4	3	PCIE_A_TXP0
PCIE_A_RXN0	6	5	PCIE_A_TXN0
GND	8	7	GND
PCIE_A_RXP1	10	9	PCIE_A_TXP1
PCIE_A_RXN1	12	11	PCIE_A_TXN1
GND	14	13	GND
PCIE_A_RXP2	16	15	PCIE_A_TXP2
PCIE_A_RXN2	18	17	PCIE_A_TXN2
GND	20	19	GND
PCIE_A_RXP3	22	21	PCIE_A_TXP3
PCIE_A_RXN3	24	23	PCIE_A_TXN3
GND	26	25	GND
CLK-P	28	27	PCIE_RST-L
CLK-N	30	29	GND
GND	32	31	SML_DAT
XMC1_RST-L	34	33	SML_CLK
+12V	36	35	P5V_STB
+12V	38	37	P5V_STB
+12V	40	39	-12V
+5V	42	41	-12V
+5V	44	43	+3.3V
+5V	46	45	+3.3V
+5V	48	47	+3.3V
+5V	50	49	+3.3V
+5V	52	51	+3.3V
+5V	54	53	+3.3V
+5V	56	55	+3.3V
+5V	58	57	+3.3V
+5V	60	59	+3.3V

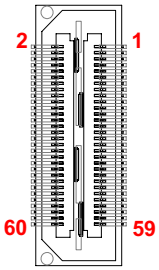


Table 4-17: DB-6210L2 Connector (CN9) Pin Definition

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DB-6210L2 Connector (CN10)

Signal Name	Pin #	Pin #	Signal Name
GND	2	1	GND
PCIE_B_RXP0	4	3	PCIE_B_TXP0
PCIE_B_RXN0	6	5	PCIE_B_TXN0
GND	8	7	GND
PCIE_B_RXP1	10	9	PCIE_B_TXP1
PCIE_B_RXN1	12	11	PCIE_B_TXN1
GND	14	13	GND
PCIE_B_RXP2	16	15	PCIE_B_TXP2
PCIE_B_RXN2	18	17	PCIE_B_TXN2
GND	20	19	GND
PCIE_B_RXP3	22	21	PCIE_B_TXP3
PCIE_B_RXN3	24	23	PCIE_B_TXN3
GND	26	25	GND
PCIE_B_RXP4	28	27	PCIE_B_TXP4
PCIE_B_RXN4	30	29	PCIE_B_TXN4
GND	32	31	GND
PCIE_B_RXP5	34	33	PCIE_B_TXP5
PCIE_B_RXN5	36	35	PCIE_B_TXN5
GND	38	37	GND
PCIE_B_RXP6	40	39	PCIE_B_TXP6
PCIE_B_RXN6	42	41	PCIE_B_TXN6
GND	44	43	GND
PCIE_B_RXP7	46	45	PCIE_B_TXP7
PCIE_B_RXN7	48	47	PCIE_B_TXN7
GND	50	49	GND
XMC_PCIE-P	52	51	+3.3V
XMC-PCIE-N	54	53	+3.3V
GND	56	55	+3.3V
+12V	58	57	+3.3V
+12V	60	59	+3.3V

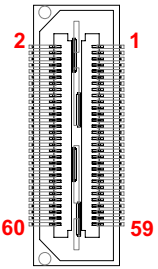


Table 4-18: DB-6210L2 Connector (CN10) Pin Definition

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CompactPCI J1 Connector Pin Assignment

Pin	Z	A	B	C	D	E	F
25	GND	+5V	REQ64#	ENUM#	+3.3V	+5V	GND
24	GND	AD1	+5V	V(I/O)	AD0	ACK64#	GND
23	GND	P3V3	CPCI_AD4	CPCI_AD3	P5V	CPCI_AD2	GND
22	GND	CPCI_AD7	GND	P3V3	CPCI_AD6	CPCI_AD5	GND
21	GND	P3V3	CPCI_AD9	CPCI_AD8	CPCI_M66EN	CPCI_CBE-L0	GND
20	GND	CPCI_AD12	GND	VIO	CPCI_AD11	CPCI_AD10	GND
19	GND	P3V3	CPCI_AD15	CPCI_AD14	GND	CPCI_AD13	GND
18	GND	CPCI_SERR-L	GND	P3V3	CPCI_PAR	CPCI_CBE-L1	GND
17	GND	P3V3	IPMB_CLK	IPMB_DAT	GND	CPCI_PERR-L	GND
16	GND	CPCI_DEVSEL-L	GND	VIO	CPCI_STOP-L	CPCI_LOCK-L	GND
15	GND	P3V3	CPCI_FRAME-L	CPCI_IRDY-L	NC	CPCI_TRDY-L	GND
12-14	GND	Key Area					Key
11	GND	CPCI_AD18	CPCI_AD17	CPCI_AD16	GND	CPCI_CBE-L2	GND
10	GND	CPCI_AD21	GND	P3V3	CPCI_AD20	CPCI_AD19	GND
9	GND	CPCI_CBE-L3	NC	CPCI_AD23	GND	CPCI_AD22	GND
8	GND	CPCI_AD26	GND	VIO	CPCI_AD25	CPCI_AD24	GND
7	GND	CPCI_AD30	CPCI_AD29	CPCI_AD28	GND	CPCI_AD27	GND
6	GND	CPCI_REQ-L0	GND	P3V3	CPCI_CLK0	CPCI_AD31	GND
5	GND	NC	NC	CPCI_RESET-L	GND	CPCI_GNT-L0	GND
4	GND	P5V_IPMB	CPCI_HEALTHY-L	VIO	NC	NC	GND
3	GND	CPCI_IRQA-L	CPCI_IRQB-L	CPCI_IRQC-L	P5V	CPCI_IRQD-L	GND
2	GND	cPCI_TCK-L	P5V	cPCI_TMS-L	NC	cPCI_TDI-L	GND
1	GND	P5V	N12V	cPCI_TRST-L	P12V	P5V	GND

Table 4-19: CompactPCI J1 Connector Pin Definition

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CompactPCI J2 Connector Pin Assignment

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	NC	NC	NC	GND
20	GND	CLK5	GND	NC	GND	NC	GND
19	GND	GND	GND	NC	NC	NC	GND
18	GND	NC	NC	NC	GND	NC	GND
17	GND	NC	GND	RSTBTN#	REQ6#	GNT6#	GND
16	GND	NC	NC	DEG#	GND	NC	GND
15	GND	NC	GND	FAL#	REQ5#	GNT5#	GND
14	GND	AD35	AD34	AD33	GND	AD32	GND
13	GND	AD38	GND	V(I/O)	AD37	AD36	GND
12	GND	AD42	AD41	AD40	GND	AD39	GND
11	GND	AD45	GND	V(I/O)	AD44	AD43	GND
10	GND	AD49	AD48	AD47	GND	AD46	GND
9	GND	AD52	GND	V(I/O)	AD51	AD50	GND
8	GND	AD56	AD55	AD54	GND	AD53	GND
7	GND	AD59	GND	V(I/O)	AD58	AD57	GND
6	GND	AD63	AD62	AD61	GND	AD60	GND
5	GND	CBE5#	GND	V(I/O)	CBE4#	PAR64	GND
4	GND	V(I/O)	NC	CBE7#	GND	CBE6#	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

Table 4-20: CompactPCI J2 Connector Pin Definition

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CompactPCI J3 Pin Assignment

Pin	Z	A	B	C	D	E	F
19	GND	P5V	P5V	P12V	P5V	P5V	GND
18	GND	LAN3_D0+	LAN3_D0-	GND	LAN3_D2+	LAN3_D2-	GND
17	GND	LAN3_D1+	LAN3_D1-	GND	LAN3_D3+	LAN3_D3-	GND
16	GND	LAN4_D0+	LAN4_D0-	GND	LAN4_D2+	LAN4_D2-	GND
15	GND	LAN4_D1+	LAN4_D1-	GND	LAN4_D3+	LAN4_D3-	GND
14	GND	USB-OC4#	USB-OC5#	USB-OC6#	USB-OC7#	USB-OC8#	GND
13	GND	USB-P7+	USB-P7-	GND	USB-P8+	USB-P8-	GND
12	GND	USB-P5+	USB-P5-	GND	USB-P6+	USB-P6-	GND
11	GND	USB-P3+	USB-P3-	GND	USB-P4+	USB-P4-	GND
10	GND	USB-OC3#	RGB-DDCCLK	RGB-DDCDAT	RGB-HSYNC	RGB-VSYNC	GND
9	GND	COM3-CTS#	COM3-RI#	RGB-BLUE	RGB-RED	RGB-GREEN	GND
8	GND	COM3-RX	COM3-TX	COM3-DTR#	COM3-DSR#	COM3-RTS#	GND
7	GND	COM4-TX	COM4-RX	COM3-DCD#	IPMB_CLK	IPMB_DAT	GND
6	GND	SATA-RX4+	SATA-RX4-	GND	SATA-RX3+	SATA-RX3-	GND
5	GND	GND	GND	NC	GND	GND	GND
4	GND	SATA-TX4+	SATA-TX4-	GND	SATA-TX3+	SATA-TX3-	GND
3	GND	KBDATA	KBCLK	NC	MSDATA	MSCLK	GND
2	GND	HDA_SDIN1	HDA_SDIN2	NC	HDA_DOCK_EN#	HDA_DOCK_RST#	GND
1	GND	HDA_RST#	HDA_SYNC	HDA_BIT_CLK	HDA_SDOUT	HDA_SDIN0	GND

Table 4-21: CompactPCI J3 Connector Pin Definition



High Definition audio
Keyboard/Mouse
Serial ATA
Serial ports
USB ports
Ethernet ports
RGB

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CompactPCI J5 Pin Assignment

Pin	Z	A	B	C	D	E	F
22	GND	NC	LAN4_LINK_ACT#	+3.3V	LAN3_LINK_ACT#	+3.3V	GND
21	GND	LVDS_DATA2-	LVDS_DATA2+	GND	LVDS_CLK-	LVDS_CLD+	GND
20	GND	LVDS_DATA0-	LVDS_DATA0+	GND	LVDS_DATA1-	LVDS_DATA1+	GND
19	GND	DSKCHG#	HDSEL#	NC	RDATA#	WRPORT#	GND
18	GND	TRK0#	WGATE#	DETECT#	WDATA#	STEP#	GND
17	GND	DIR#	NC	GPIO8	DRVA#	NC	GND
16	GND	MTR0#	INDEX#	GPIO7	NC	DENSEL#	GND
15	GND	NC	NC	GPIO6	SATA-RX5+	SATA-RX5-	GND
14	GND	NC	NC	GND	SATA-TX5+	SATA-TX5-	GND
13	GND	LAN4_100#	LAN3_100#	NC	LAN3_1G#	LAN4_1G#	GND
12	GND	DVI_DATA	DVI_CLK	DVI_HTPLG	NC	NC	GND
11	GND	TDC2+	TDC2-	GND	TLC+	TLC-	GND
10	GND	TDC0+	TDC0-	GND	TDC1+	TDC1-	GND
9	GND	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GND
8	GND	LVDS_DATA3-	LVDS_DATA3+	NC	LVDS_CLK	LVDS_DATA	GND
7	GND	GND	GND	RTC	GND	GND	GND
6	GND	PCIE-CLK+	PCIE-CLK-	GND	RESET#	NC	GND
5	GND	GND	GND	GND	GND	GND	GND
4	GND	PCIE-TX3+	PCIE-TX3-	GND	PCIE-RX3+	PCIE-RX3-	GND
3	GND	PCIE-TX2+	PCIE-TX2-	GND	PCIE-RX2+	PCIE-RX2-	GND
2	GND	PCIE-TX1+	PCIE-TX1-	GND	PCIE-RX1+	PCIE-RX1-	GND
1	GND	PCIE-TX0+	PCIE-TX0-	GND	PCIE-RX0+	PCIE-RX0-	GND

Table 4-22: CompactPCI J5 Connector Pin Definition

PCI-Express x4
GPIO
DVI
Ethernet port
LVDS*
Serial ATA
Floppy

NOTE:

*LVDS function is not supported by default BIOS. Please contact ADLINK if you require LVDS support.

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4.5 Switch and Jumper Settings

Refer to “cPCI-6210(D) Series Board Layout” on page 23 for switch locations.

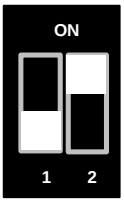
Load BIOS Default Switch (SW2)

Press switch SW2 to load the default BIOS settings.



Front/Rear VGA/LAN Selection Switch (SW3)

Switch SW3 sets the VGA and LAN3 outputs to the front panel or to the rear panel of the RTM. The default VGA and LAN3 outputs are set to the front panel.



Switch Pin	1	Mode
1	ON	Rear VGA output
	OFF	Front VGA output
2	ON	Front LAN3 output
	OFF	Rear LAN3 output

Table 4-23: Front/Rear VGA Selection Switch Settings

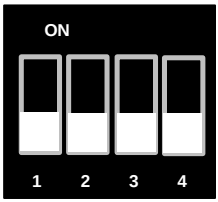
SW5 & SW7 (Debug use only)

The switches SW5 & SW7 are for debugging purposes and should be left in the default settings. The default setting of SW5 is all OFF; the default setting of SW7 is Pin 1 OFF and Pin 2 ON.

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Mode Switch (SW6)

Switch SW6 is a multi purpose switch that allows users to define the board operating mode. Four pins independently control the mode setting. All are set to OFF by default.



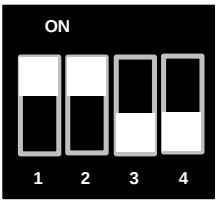
Pin#	Status	Description
1	OFF	Not used.
	ON	Not used.
2	OFF	When the system does not include a CMM (Chassis Management Module), set this pin to OFF to allow IPMI to run in "without CMM mode".
	ON	When the system includes a CMM, set this pin to ON to allow IPMI to run in "with CMM mode".
3	OFF	For debugging purposes. Do not change the default setting (OFF).
4	OFF	The cPCI-6210 power on/off is state is controlled by the ejector handle state.
	ON	Force the ejector handle state to "closed".

Table 4-24: Mode Switch Settings

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COM1/Debug Switch (SW8)

Switch SW8 sets the COM1 serial port as a standard RS-232 serial port or as an IPMI debugging port.

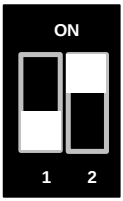


Mode	1	2	3	4
RS-232 COM port (default)	ON	ON	OFF	OFF
IPMI debugging port	OFF	OFF	ON	ON

Table 4-25: COM1/Debug Switch Settings

COM1 Mode Selection Switches (SW9,SW10)

Switch SW9 sets the COM1 serial port to RS-232 or RS-422/485 mode and SW10 sets COM1 to RS-422 or RS-485 mode. When the SW9 is set to RS-232 mode, SW10 has no function.



Mode	1	2
RS-232 (default)	Not Used	ON
RS-422/485	Not Used	OFF

Table 4-26: COM1 Mode Selection Switch SW9 Settings

Mode	1	2
RS-485	Not Used	ON
RS-422	Not Used	OFF

Table 4-27: COM1 Mode Selection Switch SW10 Settings

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5 Getting Started

This chapter describes the installation of the following components to the cPCI-6210 and rear transition modules:

- CFast card
- CompactFlash card
- 2.5” SATA hard drive
- PMC/XMC module installation

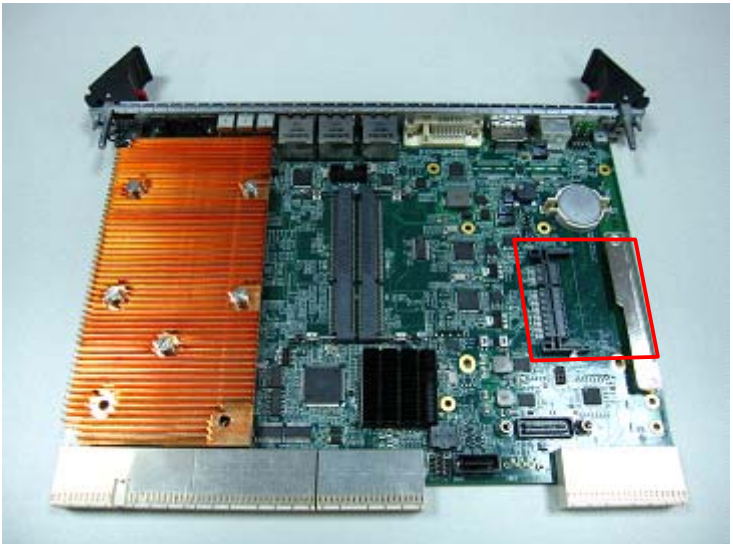
5.1 CPU and Heatsink

The cPCI-6210 Series comes with CPU and heatsink pre-installed. Removal of heatsink/CPU by users is not recommended. Please contact your ADLINK service representative for assistance.

5.2 CFast Card Installation

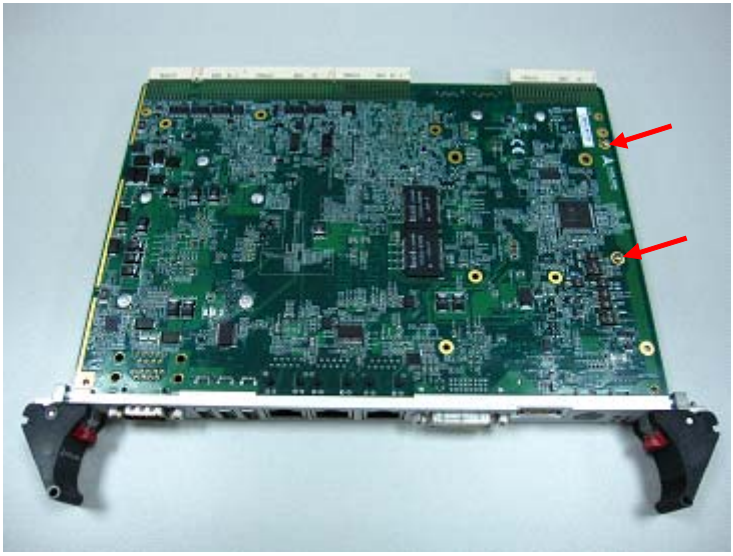
Installing a CFast card – cPCI-6210

1. A CFast card can be installed in the location indicated below.

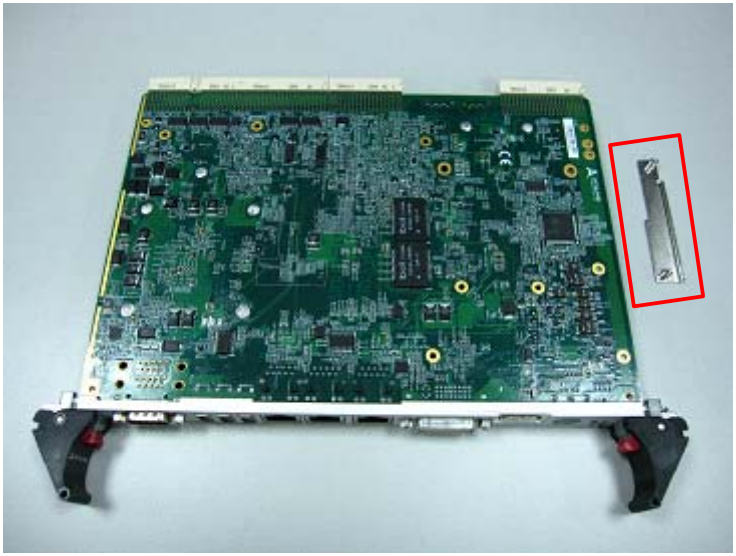


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2. Turn the board over (solder side up) and remove the two screws securing the CFast card retention bracket as indicated below.



3. Remove the CFast card retention bracket from the board.



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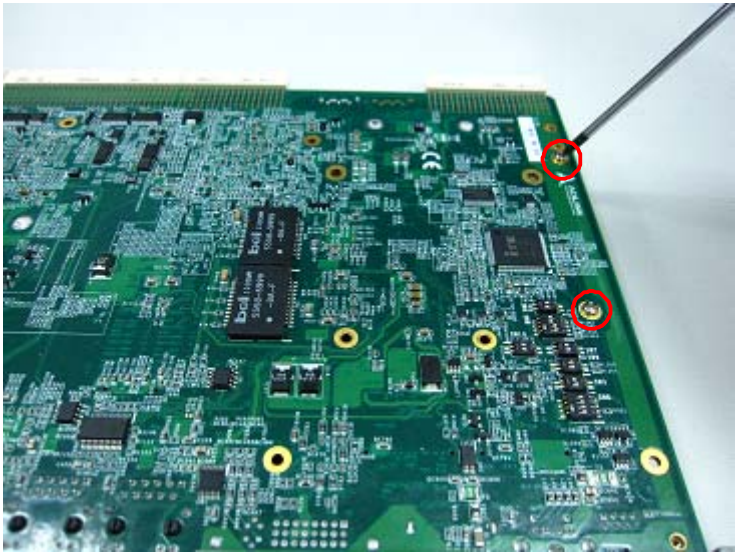
4. Turn the board over (component side up), then align and insert the CFast card into the slot until it is properly seated.



5. Align the CFast card retention bracket with the screw holes as indicated.



6. Turn the board over (solder side up) and secure CFast card retention bracket to the board with two screws.



7. The CFast card installation is now complete.

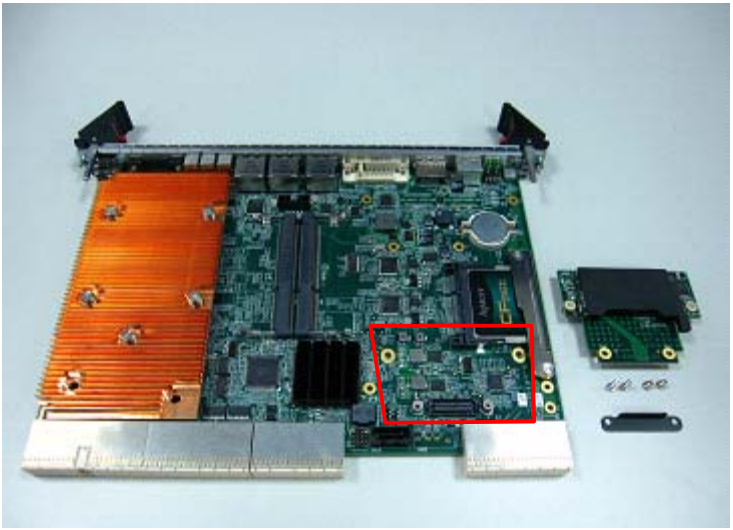


5.3 CompactFlash Card Installation

A CompactFlash card can be installed on the cPCI-6210 Series using the DB-6920CF CompactFlash adapter (ordering code "DB-CF-SA"). Note that the CompactFlash adapter occupies the same space as the 2.5” SATA drive and both cannot be installed at the same time.

Installing a CF card – cPCI-6210

1. Locate the DB-6920CF CompactFlash adapter, CF retention bracket and four screws in the CompactFlash kit DB-CF-SA. The CompactFlash adapter can be installed on the location indicated below.

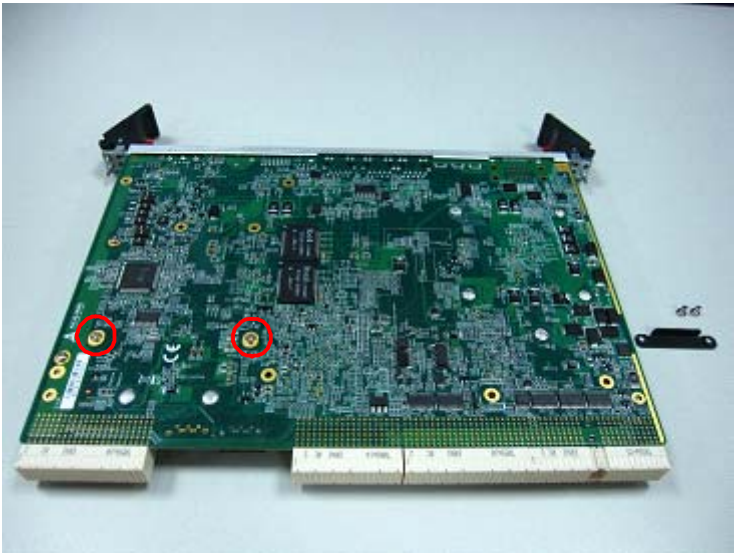


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2. Align the CompactFlash adapter with the onboard SATA connector (CN12) and press down firmly until it is properly seated.

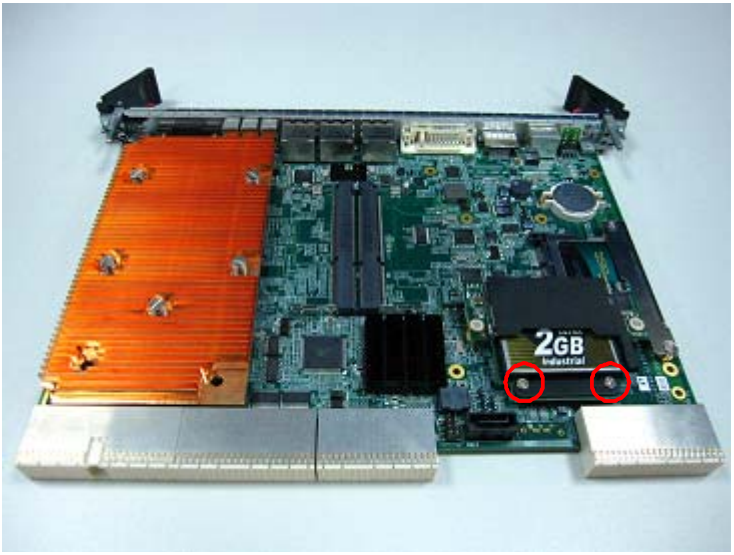


3. Turn the board over (solder side down) and secure adapter with two screws as shown.



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4. Turn the board over (component side up) and insert a CompactFlash card into the slot on the adapter. Install the CF retention bracket with two screws as shown.



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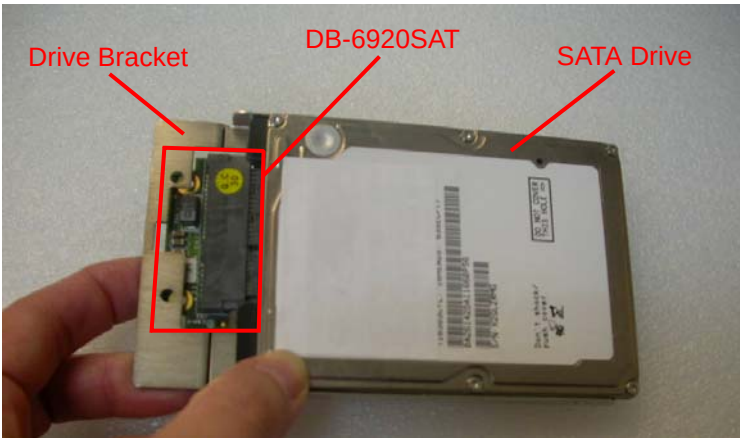
5.4 2.5” SATA Drive Installation

The cPCI-6210D provides space to install a slim type 2.5” SATA drive.

Installing a SATA Drive

1. Locate the DB-6920SAT daughter board in the package contents and connect it to 2.5” slim type drive. Mount the SATA drive onto the bracket as shown.





CAUTION:

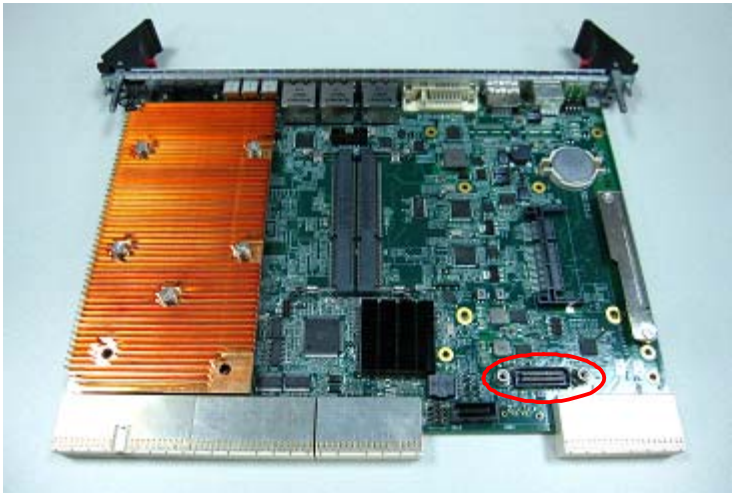
Make sure the adapter board is under the drive bracket to avoid damaging the SATA drive connectors.

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2. Secure the SATA drive onto the bracket with the four screws provided in the package. This unit is now referred to as the “drive assembly”.



3. Locate the board-to-board SATA connector (CN12) on the cPCI-6210 as indicated below.



NOTE: To install the drive assembly on the cPCI-6210D, the DB-6210L2 must first be removed as described in Step 1 of “Installing a PMC/XMC Module” on page 60

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4. Align the drive assembly so that the connector on the DB-6920SAT mates with the board-to-board connector (CN12) on the cPCI-6210 as shown. Press down on the DB-6920SAT until it is properly seated.



5. Secure the top side of the drive assembly with two screws shown as below. Turn the board over (solder side up) to continue securing the drive assembly.



CAUTION:

Support the hard drive assembly to avoid damaging the SATA connectors when turning the board over to proceed with Step 6.

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6. Secure the bottom side of the drive assembly with four screws shown as below.



7. The SATA drive installation is now complete.

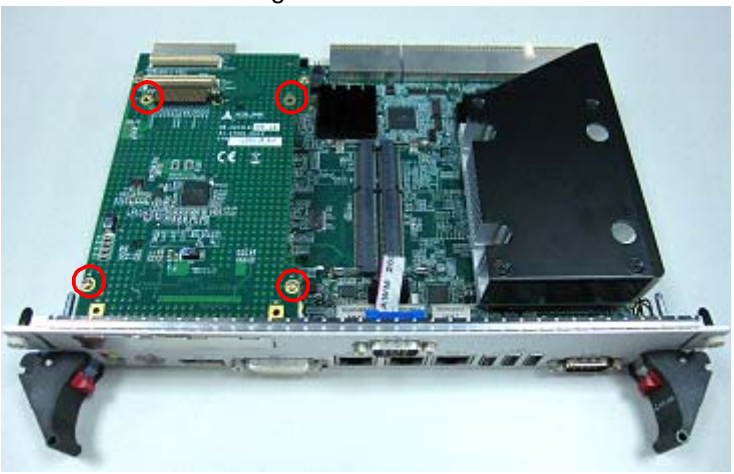


5.5 PMC/XMC Module Installation

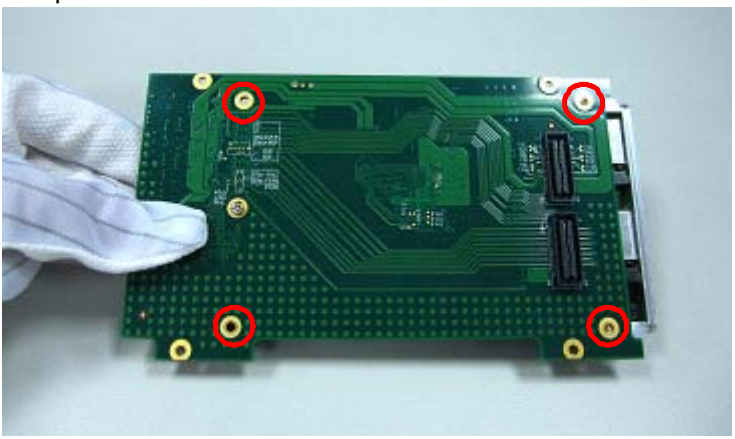
The 8HP width cPCI-6210D provides space to install a PMC or XMC module.

Installing a PMC/XMC Module

1. Remove the four screws indicated below to disassemble the DB-6210L2 daughter board from the cPCI-6210D.



2. Mount the PMC/XMC module to the DB-6210L2 and secure it using four screws provided by PMC/XMC supplier from the solder side of the DB-6210L2.



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3. Mount the PMC/XMC assembly onto the cPCI-6210D and secure the PMC/XMC assembly with the four screws removed in Step 1 as shown below.





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6 Driver Installation

The cPCI-6210 drivers can be found on the ADLINK All-In-One DVD at **X:\cPCI\cPCI-6210** or from the ADLINK website (**http://www.adlinktech.com**). ADLINK provides validated drivers for Windows XP Professional and Windows 7. We recommend using these drivers to ensure compatibility. The VxWorks BSP can be downloaded from the cPCI- 6210 product page on the ADLINK website.

6.1 Driver Installation Procedure

The following describes the driver installation procedures for Windows XP.

1. Install the Windows operating system before installing any driver. Most standard I/O device drivers are installed during Windows installation.

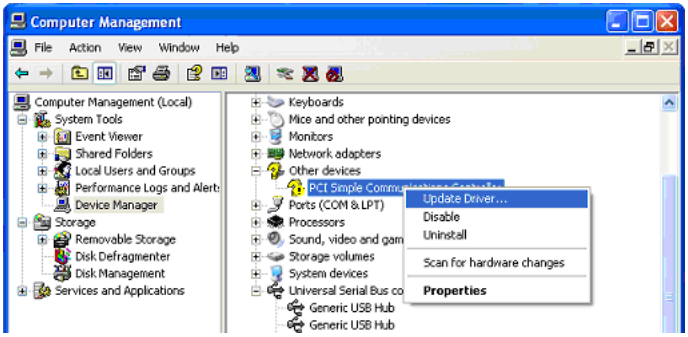

NOTE:

In order to enable AHCI mode, you must pre-install the Intel® Rapid Storage Technology driver using the F6 installation method described in the file **F6Readme.txt**, located here: **…\AHCI\Intel RST Driver Files_F6 Install_ 32bit_10.1.0.1008.zip** (not required for Windows 7).

2. Install the **chipset driver** by extracting and running the program in **...\Chipset\Intel_Chipset_Device_Software _AllOS_9.2.0.1015.zip**.
3. Install the Microsoft .NET Framework utilities (required for the graphics utility) by extracting and running the program in **...\Chipset\Microsoft_Net_Framework_v3.5_SP1.zip.**
4. Install the **graphics driver** and utilities by extracting and running the program in **...\Graphics\Intel_HD_Graphics _Family_WinXP_6.14.10.5313.zip**.
5. Install the **LAN drivers** by extracting and running the program in **…\LAN\Intel_82574L_Gigabit_Network_WINXP _11.4.7.0.zip**.
6. Install the **Intel Rapid Storage Technology Utility** by extracting and running the program in **…\AHCI\ Intel_Rapid_Storage_Technology_10.1.0.1008.zip**.

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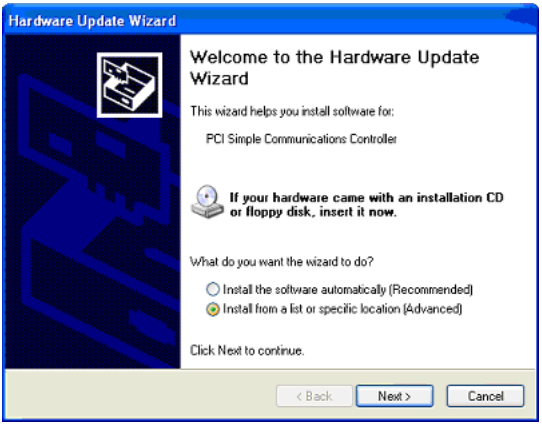
7. Install the **TPM driver** by extracting and running the program in **…\TPM\Infineon_Trusted_Platform_Module_2.1.1.0.zip**.
8. Install the **audio driver** and utilities by extracting and running the program in **…\Audio\RealTek_High_Definition_Audio _WINXP_5.10.0.6029.zip**.
9. Install the **Intel® Management Engine Interface driver** by following the steps below:
   - ▷ R-click on *My Computer*, select *Manage*, and open the *Device Manager*.
   - ▷ Under *Other Devices* you will see a "question mark" next to *PCI Simple Communication Controller.* R-click on *PCI Simple Communication Controller* and click on *Update Driver* to start the *Hardware Update Wizard*.



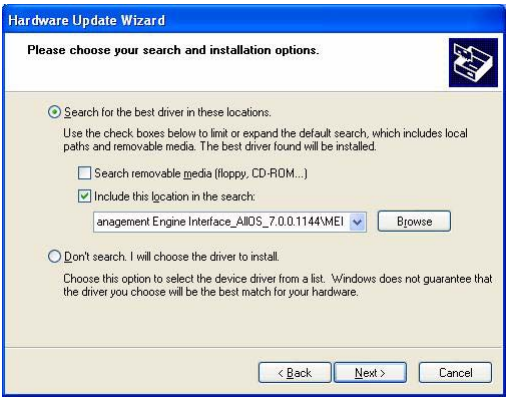
   - ▷ When asked to let Windows Update search for software, select "*No, not at this time*" and click *Next*.

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▷ Select "*Install from a list or specific location (Advanced)*" and click *Next*.



▷ Extract the contents of **…\cPCI-6210\Chipset\Intel_Management_Engine_Interface_AllOS_7.0.0.1144.zip**. Select "*Search for the best driver in these locations*" and "*Include this location in the search*". Click *Browse* and navigate to the folder "MEI" where you extracted the contents of the zip file, and then click *OK*. Click *Next* to continue.



▷ When driver installation has completed, click *Finish* to close the wizard.

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7 Utilities

7.1 Watchdog Timer

This section describes the operation of the cPCI-6210's watchdog timer (WDT). The primary function of the WDT is to monitor the cPCI-6210's operation and to reset the system if a software application fails to function as programmed. The following WDT functions may be controlled using a software application:

- enabling and disabling
- reloading timeout value

The cPCI-6210 custom WDT circuit is implemented using the internal IO of the ITE Super I/O IT8783 which is at address 2Eh of LPC. The basic functions of the WDT include:

- Starting the timer countdown
- Enabling or disabling WDT
- Enabling or disabling WDT countdown LED ON
- Reloading the timeout value to keep the watchdog from timing out
- Setting the range of the timeout period from 1 to 15300 seconds or minutes
- Sending a RESET signal to the system when the watchdog times out

Using the Watchdog in an Application

The following section describes using the WDT functions in an application. The WDT reset function is explained in the previous section. This can be controlled through the registers in the cPCI-6210's Super I/O.

An application using the reset feature enables the watchdog function, sets the count-down period, and reloads the timeout value periodically to keep it from resetting the system. If the timer count-down value is not reloaded, the watchdog resets the system hardware after its counter reaches zero.

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For a detailed programming sample, refer to the sample code provided on the ADLINK All-In-One CD. You can find it in the following directory: **X:\cPCI\cPCI-6210\WDT**.

Sample Code

The sample program written in C shown below offers an interactive way to test the Watchdog Timer under DOS.

```
#include<stdio.h>
#include<dos.h>

#define IT8783_ID1 0x87
#define IT8783_ID2 0x83

static unsigned int IT8783_ioPort = 0x2e;

//Check index port
void Enter_IT8783_Config(unsigned int flag)
{
        if(flag) IT8783_ioPort = 0x4e;

        switch(IT8783_ioPort)
        {
                case 0x2E:  //Address port = 0x2E, enter
     keys = 0x87, 0x01, 0x55, 0x55
                        outportb(0x2E, 0x87);
                        outportb(0x2E, 0x01);
                        outportb(0x2E, 0x55);
                        outportb(0x2E, 0x55);
                        break;
                case 0x4E:  //Address port = 0x4E, enter
     keys = 0x87, 0x01, 0x55, 0xAA
                        outportb(0x4E, 0x87);
                        outportb(0x4E, 0x01);
                        outportb(0x4E, 0x55);
                        outportb(0x4E, 0xAA);
                        break;
                default:
                        break;
           }
}
```

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```
//Exit index port
void Exit_IT8783_Config(unsigned int flag)
{
        if(flag) IT8783_ioPort = 0x4e;

        outportb(IT8783_ioPort, 0x02);
        outportb(IT8783_ioPort+1, 0x02);
}

//Check chip
void Get_IT8783_ID(unsigned int &ID1, unsigned int &ID2)
{
        outportb(IT8783_ioPort, 0x20);
        ID1 = inportb(IT8783_ioPort+1);
        outportb(IT8783_ioPort, 0x21);
        ID2 = inportb(IT8783_ioPort+1);
}

//WDT and LED program
void IT8783_3_WDTRun(unsigned int count_value, unsigned
     int PLEDflag)           //for cPCI-6510
{
        unsigned long tempCount;
        unsigned int registerValue;


        outportb(IT8783_ioPort, 0x07);
       outportb(IT8783_ioPort+1, 0x07);        // Device
     7

        outportb(IT8783_ioPort, 0xf8);
        outportb(IT8783_ioPort+1, 0x00);        // PLED
     mapping to nothing, disable PLED function

        if(PLEDflag == 1)
        {
                outportb(IT8783_ioPort, 0x2D);
                registerValue = inportb(IT8783_ioPort +
     1);
                registerValue |= 0x01;       // set
     Pin109 is GPIO function GP60
                outportb(IT8783_ioPort+1, registerValue);
```

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```
            outportb(IT8783_ioPort, 0xC5);
            registerValue = inportb(IT8783_ioPort +
1);
            registerValue &= 0xfe;      // set GP60
is alternate function
           outportb(IT8783_ioPort+1, registerValue);

            outportb(IT8783_ioPort, 0xCD);
            registerValue = inportb(IT8783_ioPort +
1);
            registerValue |= 0x01;          // set
GP60 is output
           outportb(IT8783_ioPort+1, registerValue);

            outportb(IT8783_ioPort, 0xf8);
            outportb(IT8783_ioPort+1, 0x30);        /
/ PLED mapping to GP60

            outportb(IT8783_ioPort, 0xf9);
            registerValue = inportb(IT8783_ioPort +
1);
            registerValue |= 0x02;
            registerValue &= 0xfb;
           outportb(IT8783_ioPort+1, registerValue);
   }
   outportb(IT8783_ioPort, 0x71);
   registerValue = inportb(IT8783_ioPort + 1);
   registerValue |= 0xD0;                   // set
Mouse & Keyboard interrupt Enable
   outportb(IT8783_ioPort+1, registerValue);

   outportb(IT8783_ioPort, 0x73);
   outportb(IT8783_ioPort+1, count_value); // set
WDT count LSB
   tempCount = tempCount >> 8;
   outportb(IT8783_ioPort, 0x74);
   outportb(IT8783_ioPort+1, count_value); // set
WDT count MSB

   if(count_value >= 60)
   {
            outportb(IT8783_ioPort, 0x72);
            registerValue = inportb(IT8783_ioPort+1);
```

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```
                registerValue &= 0x8f;
               registerValue |= 0x10; //enable WDT output
        through PowerOK!
                outportb(IT8783_ioPort+1, registerValue);
        // set WDT count is minute

                tempCount = count_value / 60;
                if((count_value%60) > 30)
                        tempCount++;
                if(tempCount > 65535)
                        tempCount = 65535;
                printf("WDT timeout in %d minutes.\n",
        tempCount);
           }
           else
           {
                outportb(IT8783_ioPort, 0x72);
                registerValue = inportb(IT8783_ioPort+1);
                registerValue |= 0x80;

                tempCount = count_value;
                if(tempCount != 0)
                {
                        printf("WDT timeout in %d
        seconds.\n", tempCount);
                        registerValue |= 0x40; //Enable
        WDT output through KBRST
                }
                else
                {
                        printf("WDT is Disabled.\n");
                        registerValue &= 0xbf; //Disable
        WDT output through KBRST
                }

               outportb(IT8783_ioPort+1, registerValue);
        // set WDT count is second
           }

}
```

7.2 Using the Trusted Platform Module

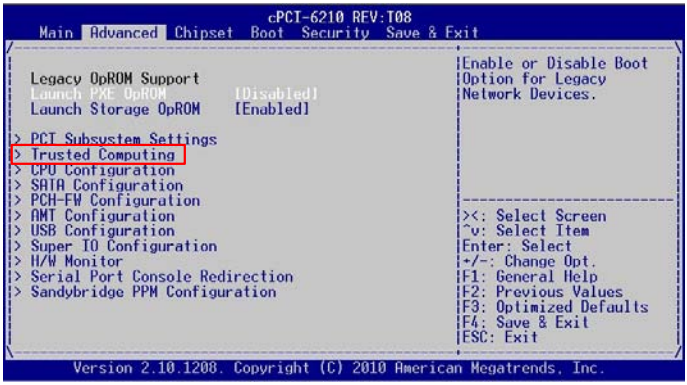
This section describes the operation of the cPCI-6210's Trusted Platform Module (TPM).

Enabling TPM in BIOS

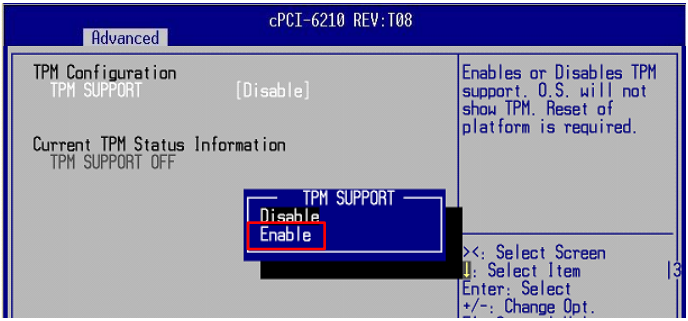
The TPM is set to "Disabled" by default. Users wishing to use the TPM must first enable it in BIOS as follows:

NOTE: TPM is not supported by default. If you require TPM for your application, please contact your sales representative to order a model that supports TPM.

1. Under the "Advanced" section in BIOS, choose "Trusted Computing".

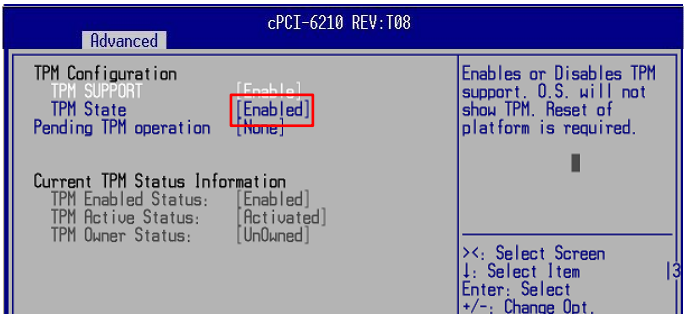


2. Set "TPM Support" to Enabled.



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3. Set "TPM State" Enabled. Save settings and exit BIOS.



Using the TPM Utility

A utility for managing the TPM settings, the Infineon Security Platform Settings Tool, is provided with the TPM driver located on the All-In-One DVD in the following directory: X:\cPCI\cPCI-6210\TPM. Make sure you have installed the TPM driver as described in 6.1 Driver Installation Procedure on page 63.

1. After the driver is installed, click on *Start* > *Programs* > *Infineon Security Platform Solution* > *Manage Security Platform* to run the utility.



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2. The Infineon Security Platform Settings Tool is shown in the screen capture below.



3. Click on the "User Settings" tab, then follow the on screen instructions to build a security platform.



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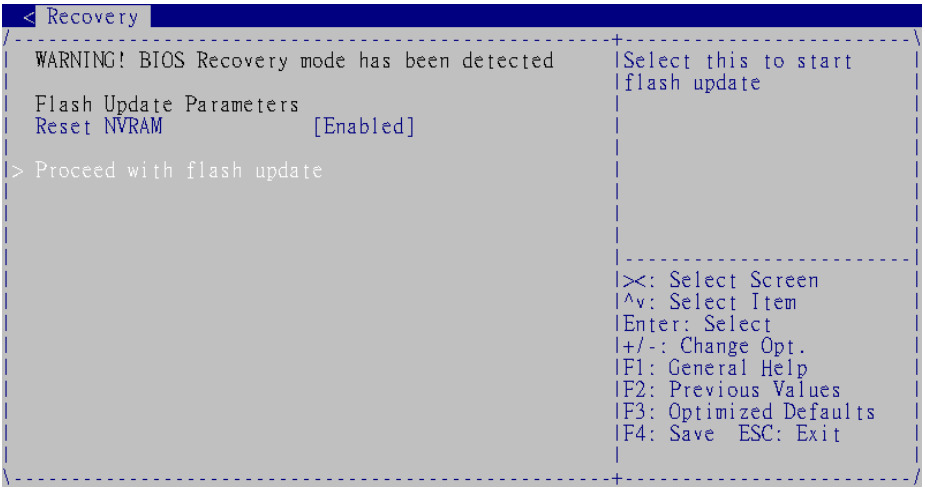
4. Prepare a removable media to store important passwords and data and follow the on screen instructions.



7.3 BIOS Recovery

The cPCI-6210 Series features AMI® EFI BIOS with BIOS recovery. If the BIOS becomes corrupted and you are unable to boot your system, the system will sound 4 beeps. Follow the instructions below to re-flash the BIOS and recover the system.

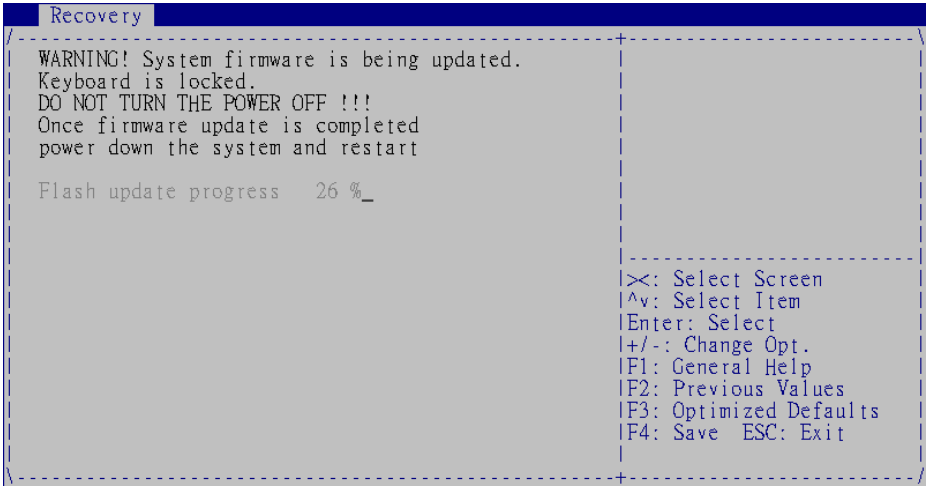
1. Download the BIOS recovery file "**C6210000.ROM**" from the product website at:
   www.adlinktech.com/PD/web/PD_detail.php?cKind=&pid=1013
2. Prepare a bootable USB flash drive and copy the recovery file "C6210000.ROM" to the root directory.
3. Insert the USB flash drive into the cPCI-6210 and power up the system.
4. The system will sound 4 beeps to indicate boot failure, and then it will sound 2 beeps to indicate it is entering Recovery Mode. You will see the screen below:



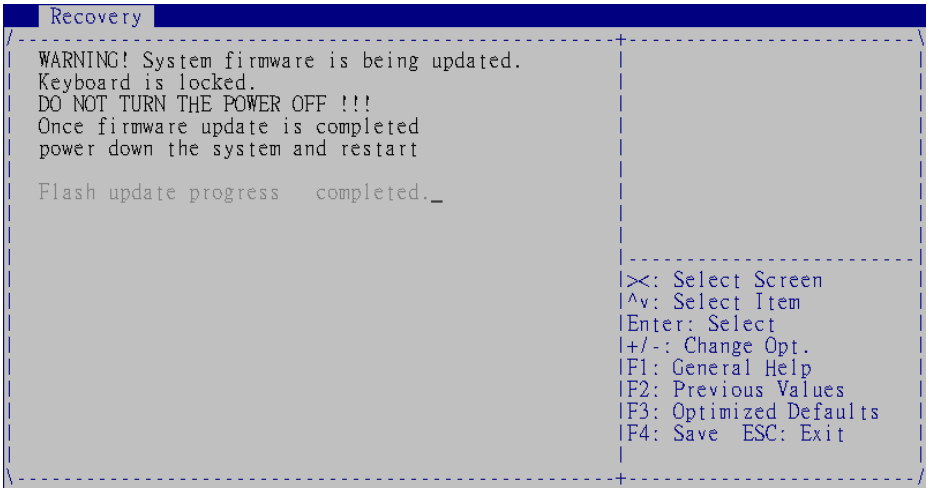
5. Select "Proceed with flash update" and press **Enter**.

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6. During the BIOS recovery process, you will see the following:



7. After the flash update is completed, power down the system and restart. The system should now boot up normally.



NOTE: After BIOS recovery, follow the instructions in *Section 7.4* or *Section 7.5* to restore your original BIOS version.

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7.4 BIOS Update - DOS Method

Follow the instructions below to update the BIOS or restore a previous BIOS version using a DOS bootable storage device.

1. Download the required BIOS file from the product website: **www.adlinktech.com/PD/web/PD_detail.php?cKind=&pid=1013**
2. Prepare a DOS bootable floppy disk or USB flash drive and unzip the contents of the BIOS file to the disk
3. Boot the system using the floppy disk or USB drive prepared above and run the file **pBIOS.bat**
4. Restart the system (if requested)

7.5 BIOS Update - ADLINK BIOS Updater Method

The ADLINK BIOS updater is a BIOS flash application embedded in the EFI firmware volume. With the ADLINK BIOS updater, you can update the system BIOS without first having to enter an operating system (e.g. MS-DOS or Windows). To access the ADLINK BIOS updater, **press the <F9> key during POST**. The new BIOS file can be saved to any storage device that has been formatted with the FAT12/16/32 file system (e.g. hard drive, USB flash drive).

Updating the BIOS

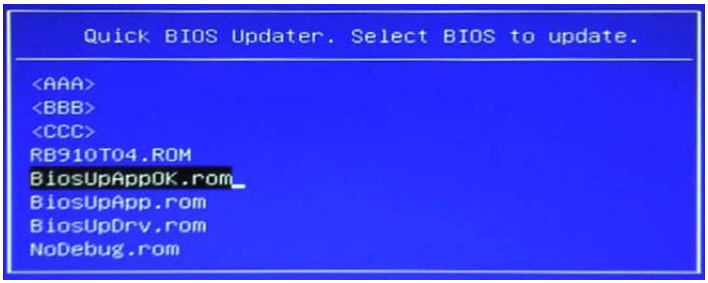
The following procedure assumes that you have saved the new BIOS ROM file to a USB flash drive.

1. Insert the USB flash drive containing the new BIOS file into the USB target system. Boot up the system and press the <F9> key during POST to enter the BIOS Updater. You will be presented with a menu of storage devices. Select the USB flash drive with the new BIOS file using the up or down arrow keys and press <Enter>. (In the example screen capture below, only one storage device has been detected.)

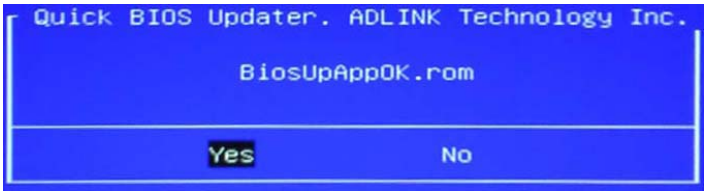


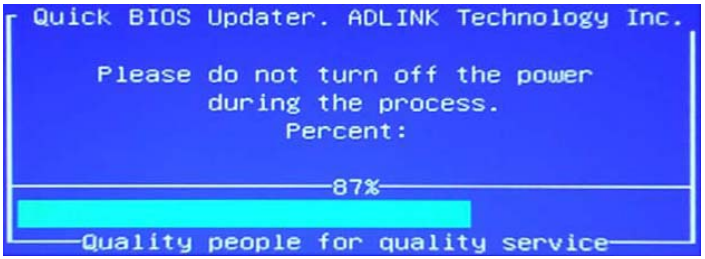
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2. The BIOS Updater will display the contents of the selected storage device. Navigate to the desired BIOS ROM file and press <Enter>. If the file has been saved in a subdirectory, select the subdirectory and press <Enter> to view its contents.



3. After you have selected the desired BIOS ROM file, the BIOS Updater will ask you to confirm that you wish to update the BIOS on your target system. Select "Yes" and press <Enter> to begin the BIOS update. The progress of the BIOS update will be displayed on screen.



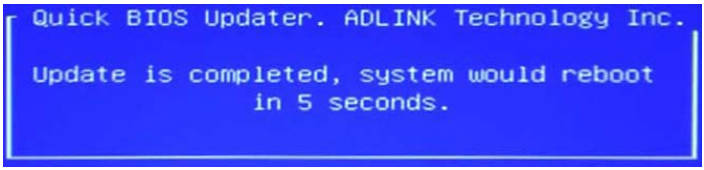


CAUTION:

Do not turn off or restart the system while the system is reading/updating the BIOS.
Do not remove the USB flash drive or hard drive while the system is updating the BIOS.

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4. After the update process is complete, system will automatically reboot.



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8 BIOS Setup Utility

The following chapter describes basic navigation for the AMIBIOS®8 BIOS setup utility.

8.1 Starting the BIOS

To enter the setup screen, follow these steps:

1. Power on the motherboard
2. Press the < Delete > key on your keyboard when you see the following text prompt:
   < Press DEL to run Setup >
3. After you press the < Delete > key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu.



Note: In most cases, the < Delete > key is used to invoke the setup screen. There are several cases that use other keys, such as < F1 >, < F2 >, and so on.

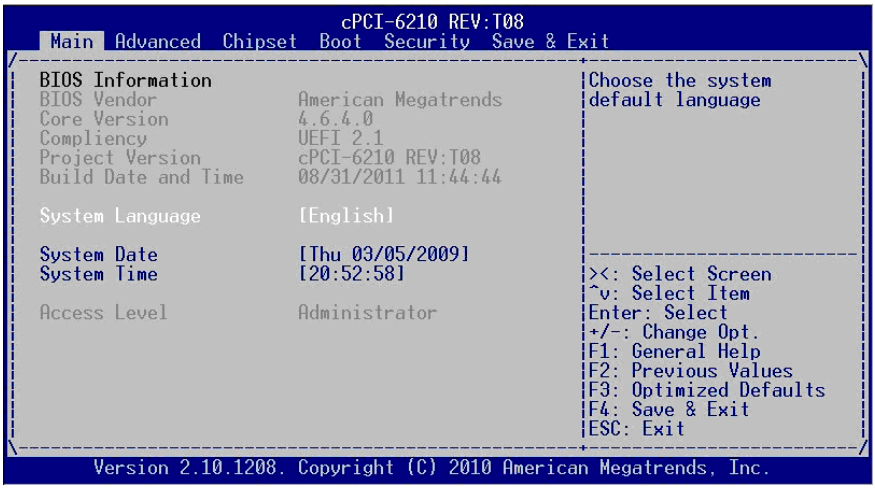
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Setup Menu

The main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in this user's guide.

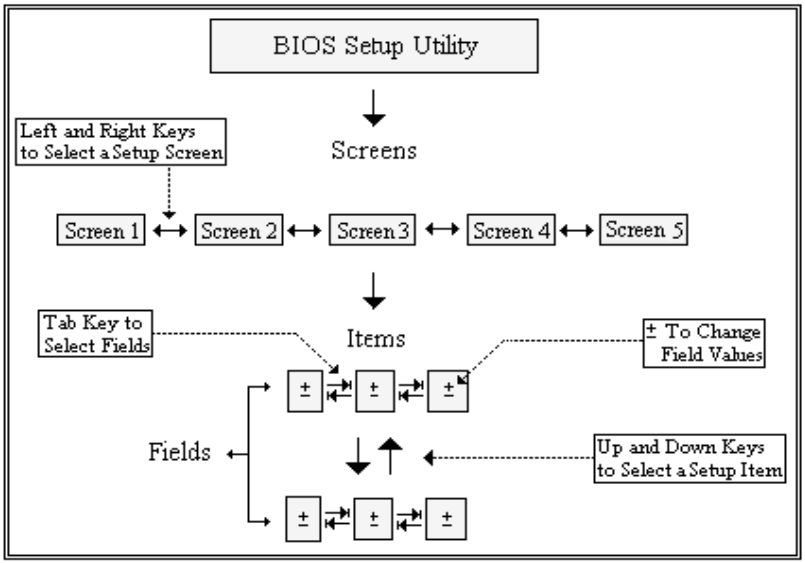
The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed" options cannot be configured, "Blue" options can be.

The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.



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Navigation



Note: There is a hot key legend located in the right frame on most setup screens.

Keyboard Commands

Enter Selects the highlighted option or submenu.

< > The *Left* and *Right* "Arrow" keys allow you to select a setup screen.

^ v The *Up* and *Down* "Arrow" keys allow you to select a setup screen.

+ - The *Plus* and *Minus* keys allow you to change the field value of a particular setup item.

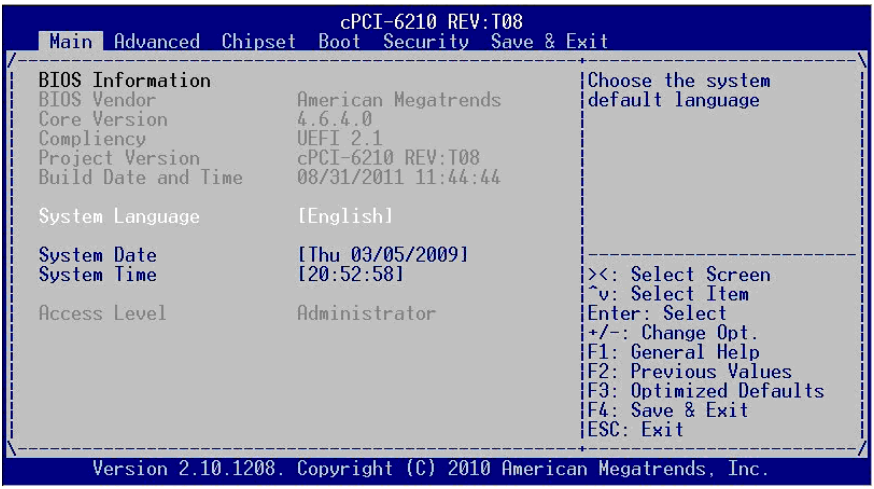
Tab Moves the cursor to the next configurable item or to the next field.

Esc The *Esc* key allows you to discard any changes you have made and exit the Setup menu. Press the *Esc* key to exit the Setup menu without saving your changes. Press the *Enter* key to discard changes and exit. You can also use the "Arrow" keys to select Cancel and then press the *Enter* key to abort this function and return to the previous screen.

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8.2 Main Setup

When you first enter the Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



System & Board Info

BIOS Vendor

Displays the BIOS vendor.

Core Version

Displays the BIOS core version.

Project Version

Displays the current BIOS revision.

Build Data

Displays the BIOS build data.

System Language

Displays the system default language (English only).

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System Time/System Date

Use this option to change the system time and date. Highlight System Time or System Date using the < Arrow > keys. Enter new values using the keyboard. Press the < Tab > key or the < Arrow > keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

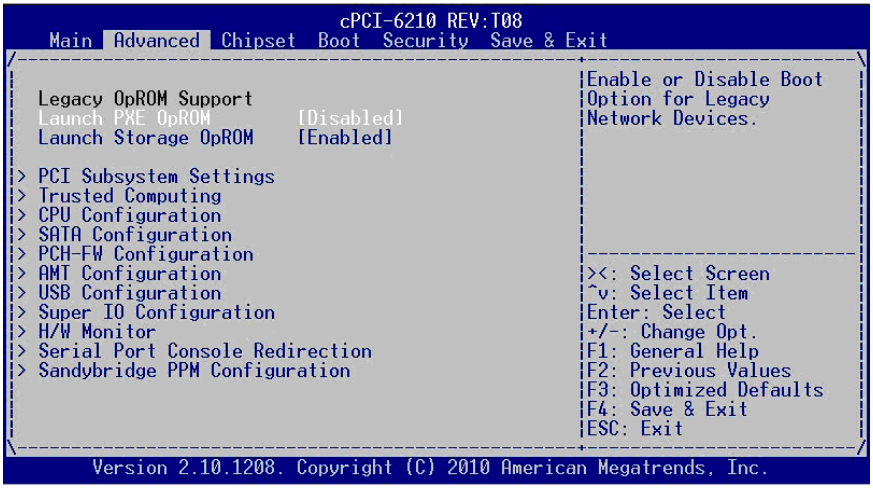
Note: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

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8.3 Advanced BIOS Setup

Select the Advanced tab from the setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as SuperIO Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the < Arrow > keys. The Advanced BIOS Setup screen is shown below.

The sub menus are described on the following pages.



Launch PXE OpROM

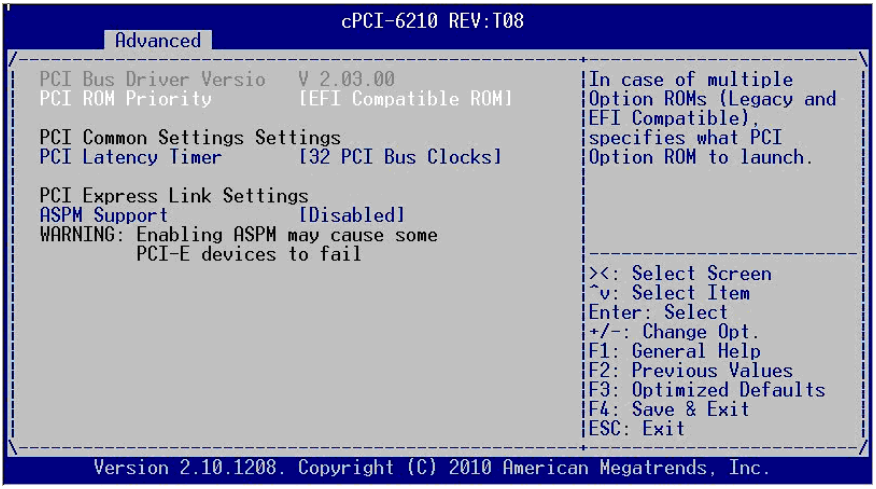
Boot option for legacy network devices. Options: Enabled, Disabled.

Launch Storage OpROM

Boot option for legacy mass storage devices with Option ROM. Options: Enabled/Disabled.

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8.3.1 PCI Subsystem Settings



PCI Latency Timer

Value to be programmed into PCI Latency Timer Register. Options: 32 PCI Bus Clocks, 64 PCI Bus Clocks, 96 PCI Bus Clocks, 128 PCI Bus Clocks, 160 PCI Bus Clocks, 192 PCI Bus Clocks, 224 PCI Bus Clocks, 248 PCI Bus Clocks.

ASPM Support

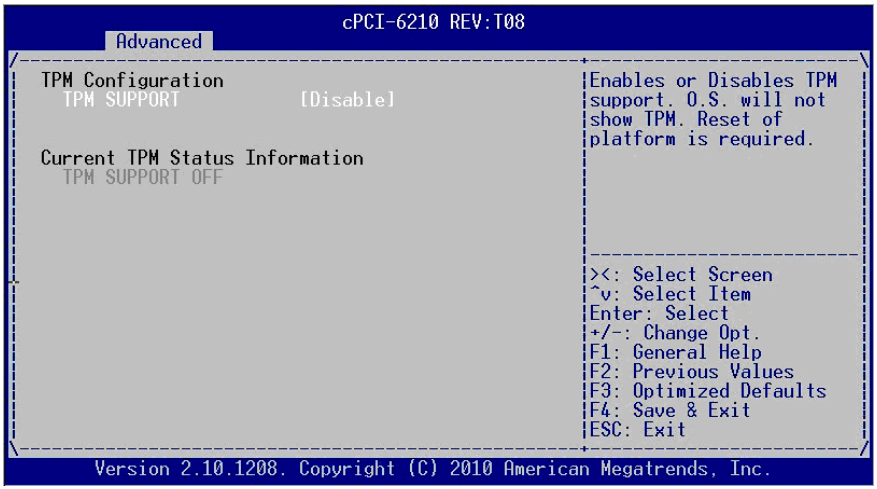
Set the ASPM (Active State Power Management) level. Options:

- **Disabled:** Disable ASPM
- **Auto:** BIOS auto configure
- **Force L0:** Force all links to L0 State

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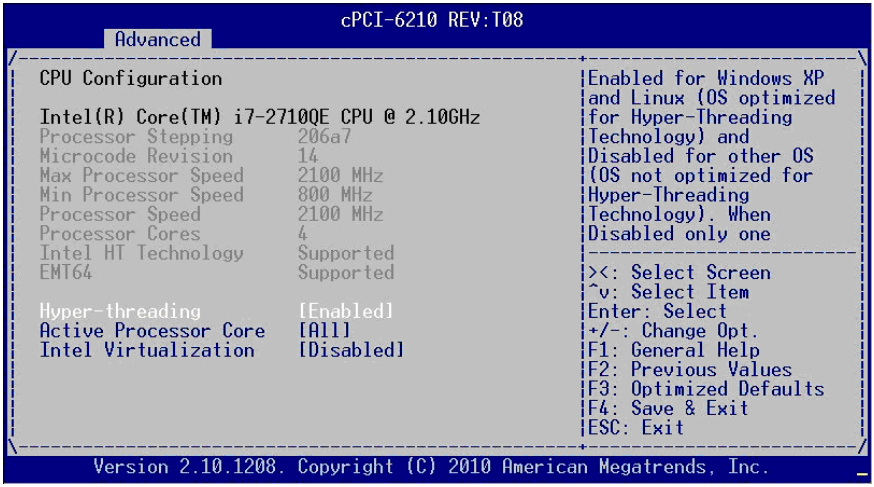
8.3.2 Trusted Computing

Trusted computing is an industry standard to make personal computers more secure through a dedicated hardware chip, called a Trusted Platform Module (TPM). This option allows you to enable or disable the TPM support.



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8.3.3 CPU Configuration



Hyper-Threading

Enables/disables Hyper-Threading Technology.

Active Processor Cores

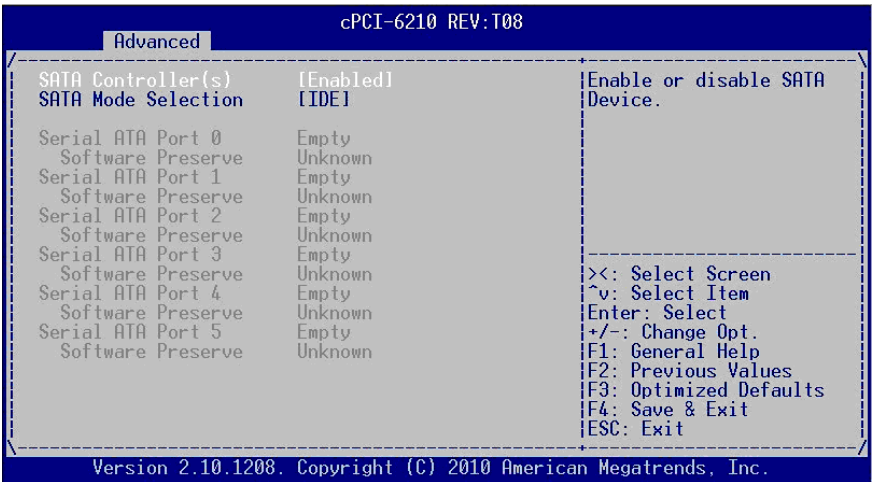
Number of cores to enable in each processor package. Options: All, 1, 2.

Intel Virtualization

Enables/disables Intel Virtualization Technology.

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8.3.4 SATA Configuration



SATA Controllers

This item specifies enables/disables the SATA Controllers.

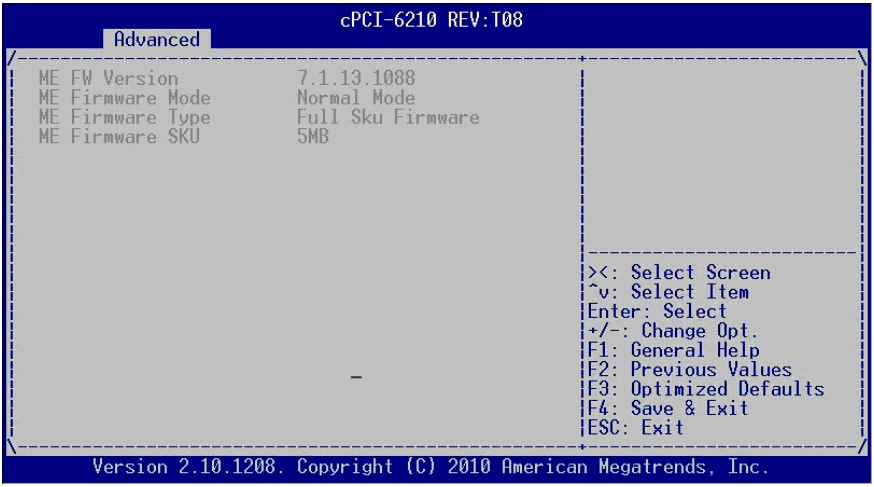
SATA Mode

The SATA interface can be configured as a legacy IDE, RAID and AHCI mode.

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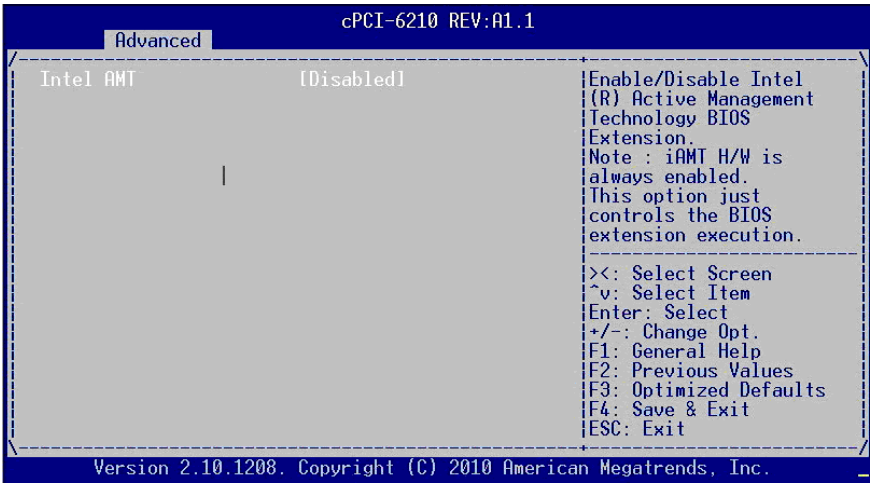
8.3.5 PCH-FW Configuration

The setup screen reports “Management Engine Technology Parameters” information.



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8.3.6 AMT Configuration

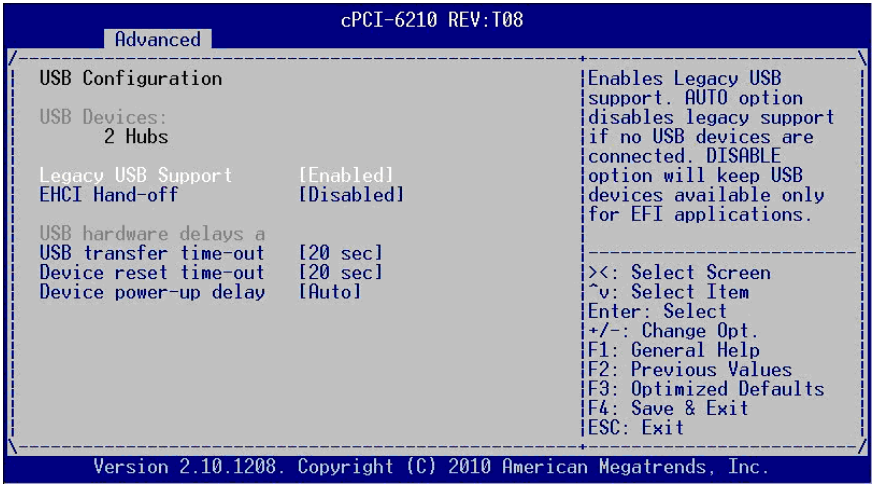


Intel AMT

Enable/Disable the Intel® Active Management Technology BIOS extension.

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8.3.7 USB Configuration



Legacy USB Support

Legacy USB Support refers to USB mouse and keyboard support. Normally if this option is not enabled, any attached USB mouse or keyboard will not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB device (such as mouse or keyboard) can function even when there is no USB driver loaded on the system (e.g. during boot and while using DOS). Set this value to enable or disable the Legacy USB Support.

EHCI Hand-off

This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by the EHCI driver. Options: Enable, Disable.

USB transfer time-out

This item sets the time-out value for Control, Bulk and Interrupt transfers.

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Device Reset Timeout

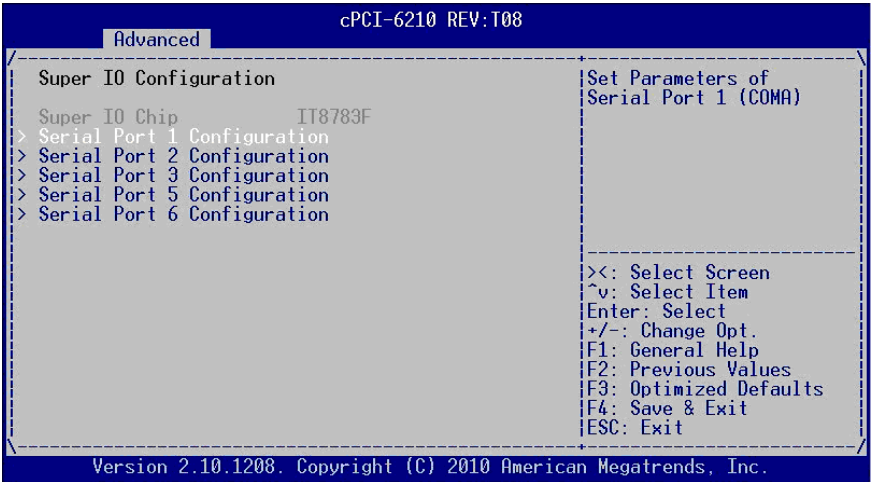
USB mass storage device Start Unit command timeout.

Device Power-up Delay

Maximum time the device will take before it properly reports itself to the Host Controller. "Auto" uses these default values: for a Root port it is 100ms, for a Hub port the delay is taken from the Hub descriptor.

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8.3.8 Super IO Configuration

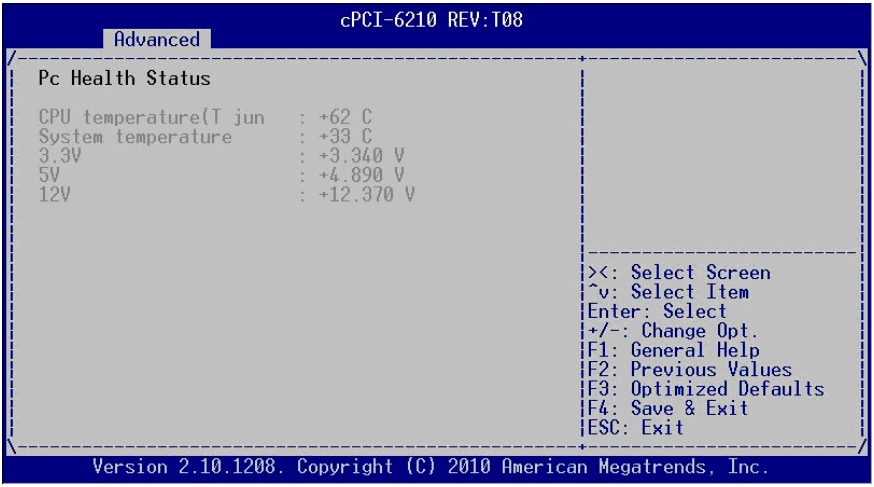


Serial Port 1/2/3/5/6 Configuration

Each sub-menu allows you to Enable/Disable and set the parameters of Serial Ports 1, 2 (RTM), 3 (RTM), 5 (Front Panel), 6 (IPMI).

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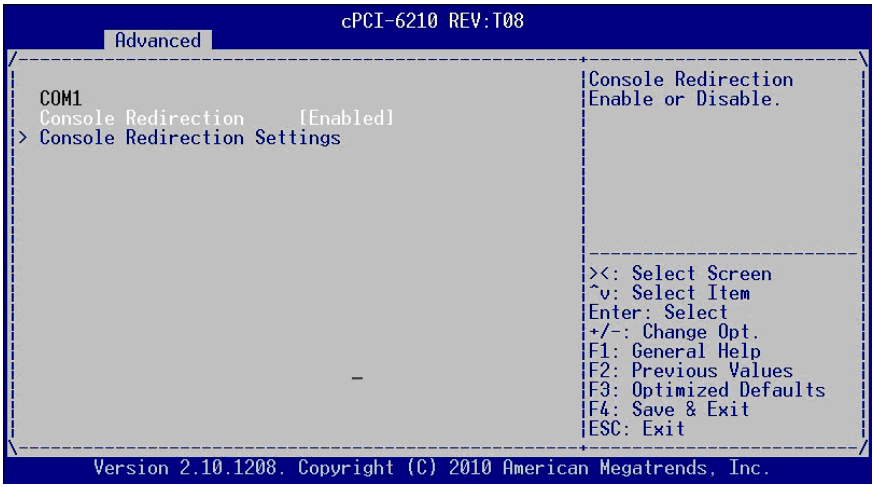
8.3.9 H/W Monitor



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8.3.10 Serial Port Console Redirection

The settings specify how the host computer and the remote computer will exchange data. Both computers should have the same or compatible settings.

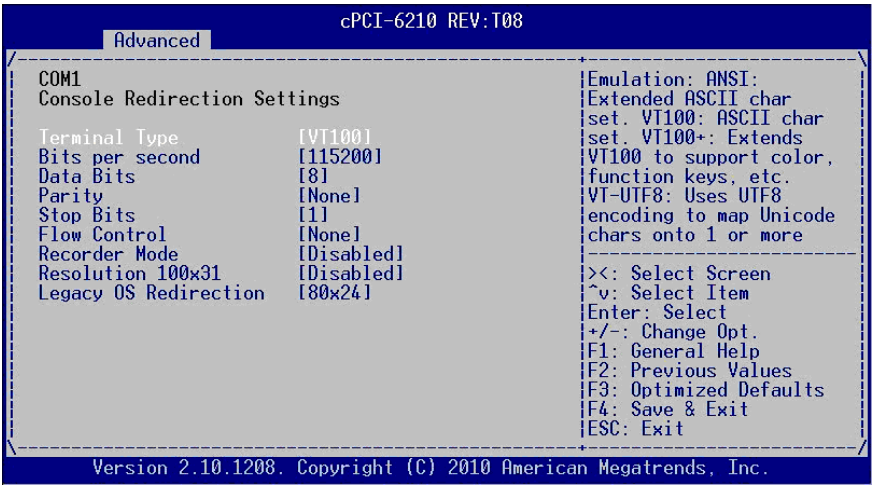


Console Redirection

Enable or disable Console Redirection.

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Console Redirection Settings



Terminal Type

VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. Options: VT100, VT100+, VT-UTF8, ASNI.

Bits per Second

Select the bit rate (bits/second) you want the serial port to use for console redirection. Options: 115200, 57600, 19200, 9600.

Data Bits

Select the data bits you want the serial port to use for console redirection. Set this value to 7 or 8.

Parity

Set this option to select Parity for console redirection. The settings for this value are None, Even, Odd, Mark, Space.

Stop Bits

Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit.

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Communication with slow devices may require more than 1 stop bit. Set this value to 1 or 2.

Flow Control

Set this option to select Flow Control for console redirection. The settings for this value are Noneand Hardware RTS/CTS. Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals. Software flow control uses start/stop ASCII chars, which slows down the data flow and can be problematic if binary data is being sent.

Recorder Mode

When enabled, only text will be sent. This is to capture terminal data.

Resolution 100x31

Enables or disables extended terminal resolution.

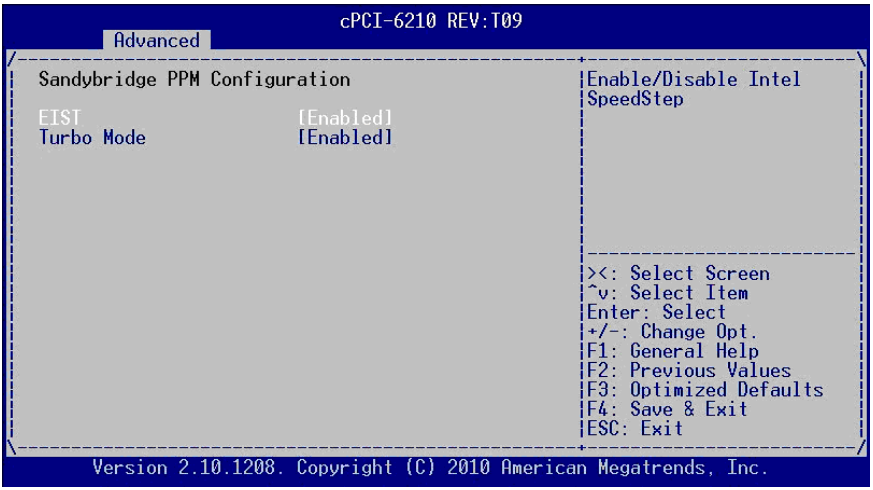
Legacy OS Redirection Resolution

In legacy OSes, the number of rows and columns supported by redirection. The settings for this value are: 80x24, 80x25.

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8.3.11 Sandy Bridge PPM Configuration

(Processor Power Management)



EIST

Enables/disables Enhanced Intel SpeedStep® Technology (EIST)

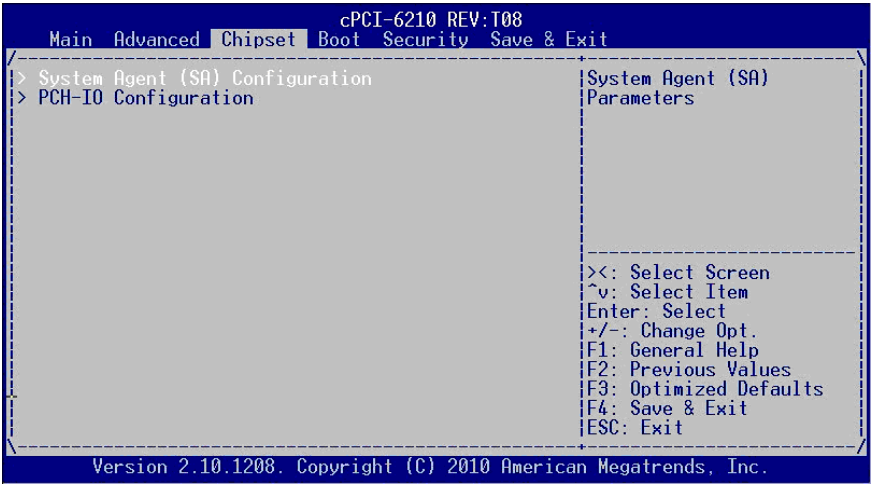
Turbo Mode

Enables/disables Turbo Mode.

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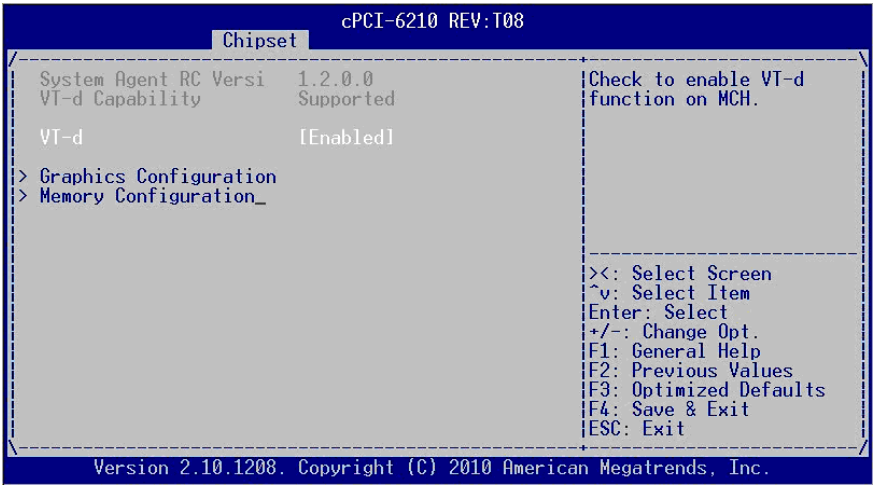
8.4 Chipset Configuration

Select the Chipset tab from the setup screen to enter the Chipset BIOS Setup screen. You can select any of Chipset BIOS Setup options by highlighting it using the < Arrow > keys. The Chipset BIOS Setup screen is shown below.



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8.4.1 System Agent (SA) Configuratio



VT-d

Enables/disables Intel® Virtualization Technology for Directed I/O (VT-d).

Graphics Configuration



Primary Display

Allows you to select which graphics controller to use as the primary boot device. Options: Auto, IGFX, PEG, PCI.

Internal Graphics

Allows you to select enable/disable.the internal graphics. Options: Auto, Enabled or Disabled

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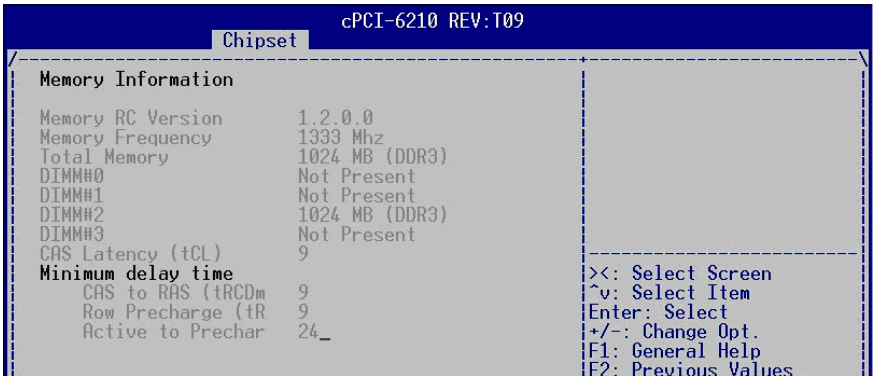
DVMT Pre-Allocated

Select DVMT 5.0 Pre-Allocated Graphics Memory size (fixed) used by the internal graphics device.

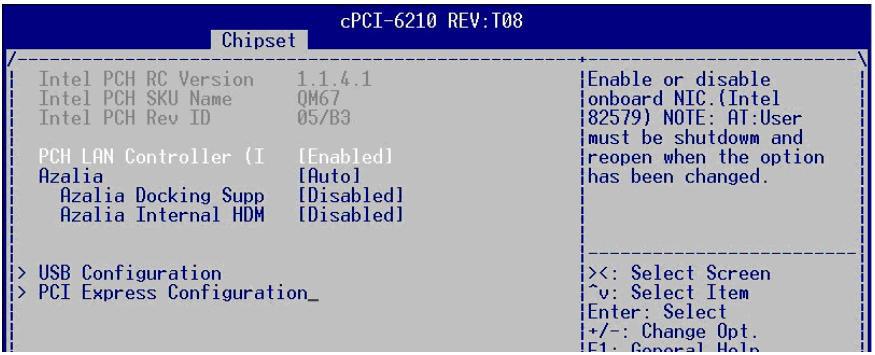
DVMT Total Gfx Mem

Select DVMT5.0 Total Graphic Memory size used by internal graphics device. Options: 128MB, 256MB, Maximum.

Memory Information



PCH-IO Configuration



PCH LAN Controller

Enable or disable onboard NIC (Intel 82579). Note: In AT Mode, system must be shutdown and restarted when this option has been changed.

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Azalia HD Audio

The onboard HDA Controller. Set this value to Enabled, Disabled, Auto (enabled if present, disabled otherwise).

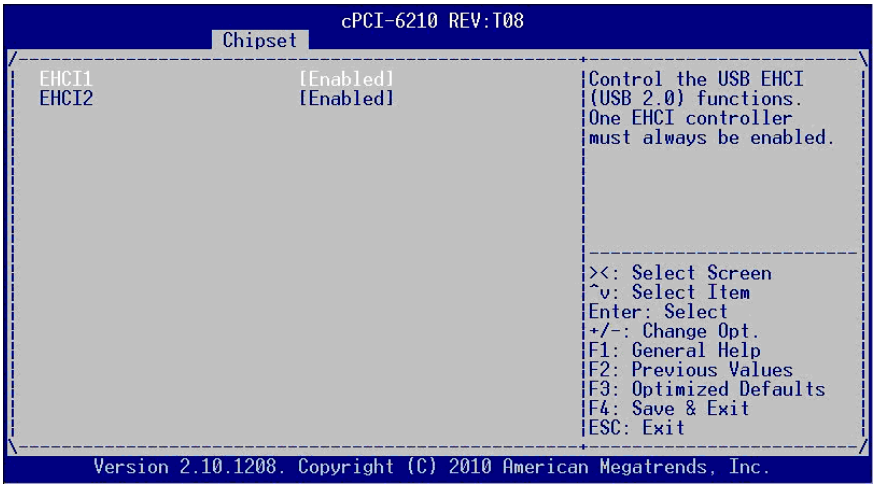
Azalia Docking Support

Enable or disable Azalia Docking Support of Audio Controller.

Azalia Internal HDMI Codec

Enable or disable internal HDMI codec for Azalia.

USB Configuration



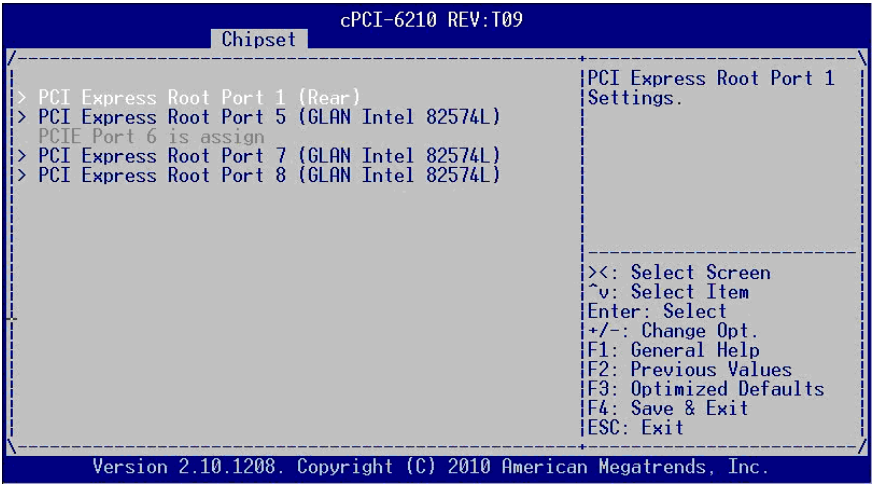
EHCI1/2 Controller 1

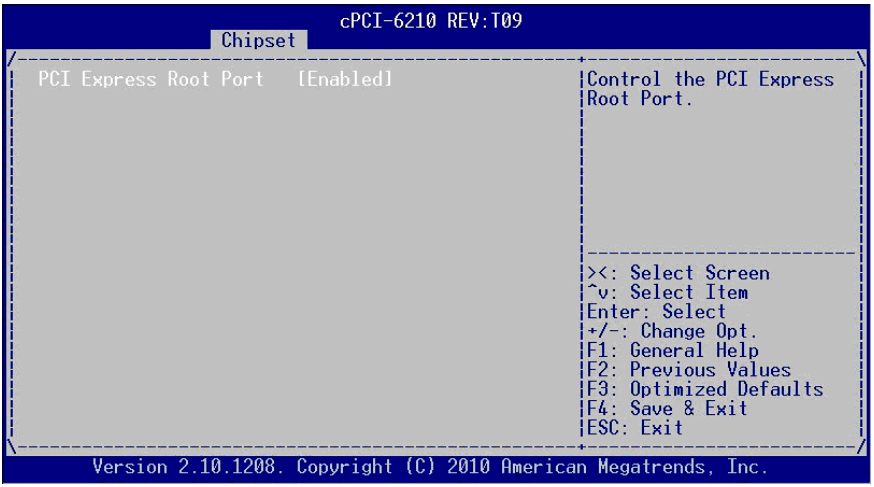
USB 2.0 (EHCI) support. Set this value to Enable/Disable.

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PCI Express Configuration

Use these submenus to enable/disable PCI Express Root Port 1 (Rear), PCI Express Root Port 5 /7/8 (GbE Intel 82574L).

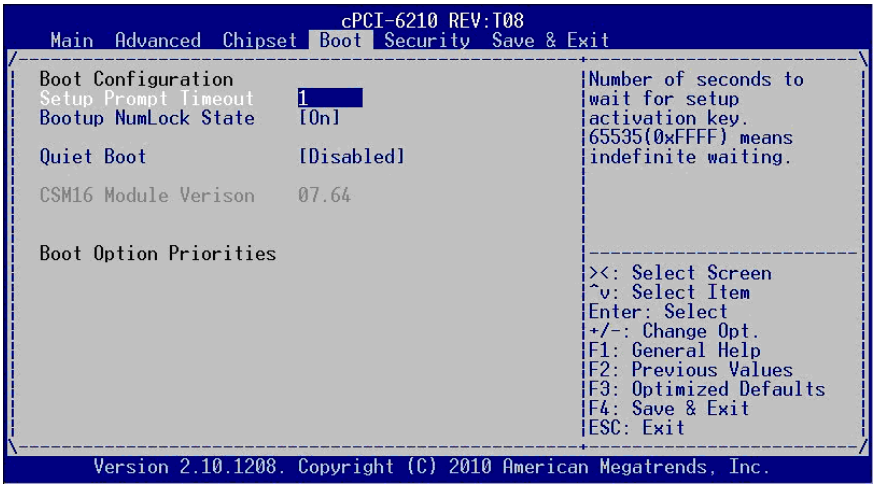




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8.5 Boot Configuration

Select the Boot tab from the setup screen to enter the Boot Configuration screen. You can select any of the items in the left frame of the screen to go to the sub menu for that item. You can display a Boot Configuration option by highlighting it using the < Arrow > keys. The Boot Configuration screen is shown below:



Setup Prompt Timeout

Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting. Use the <+> and <-> keys to change the value of the selected option.

Bootup Num-Lock

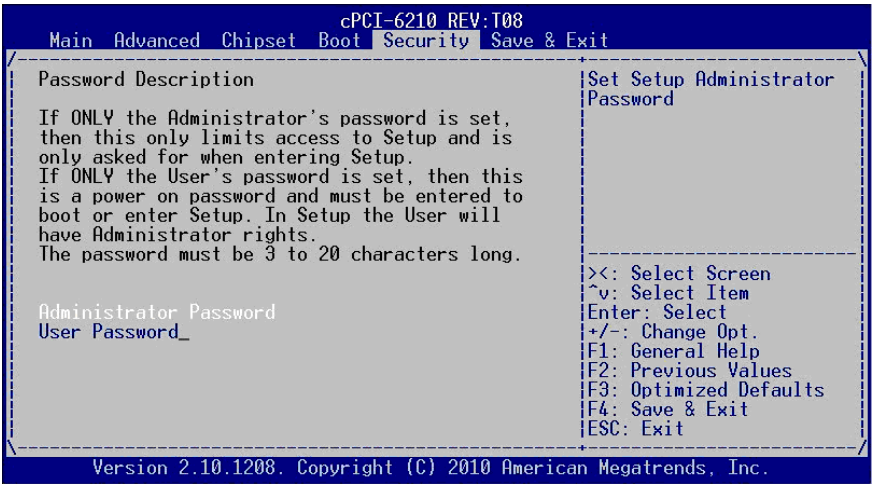
This option sets the Num Lock status when the system is powered on. Setting it to On will turn on the Num Lock key when the system is booted up. Setting it to Off will not enable the Num Lock key on bootup.

Quiet Boot

When this feature is **enabled**, the BIOS will hide normal POST messages during the boot-up sequence. When it is **disabled**, the BIOS will display the normal POST messages.

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8.6 Security Setup



Administrator Password

Use this option to set a password for administrators with full control of the BIOS setup utility.

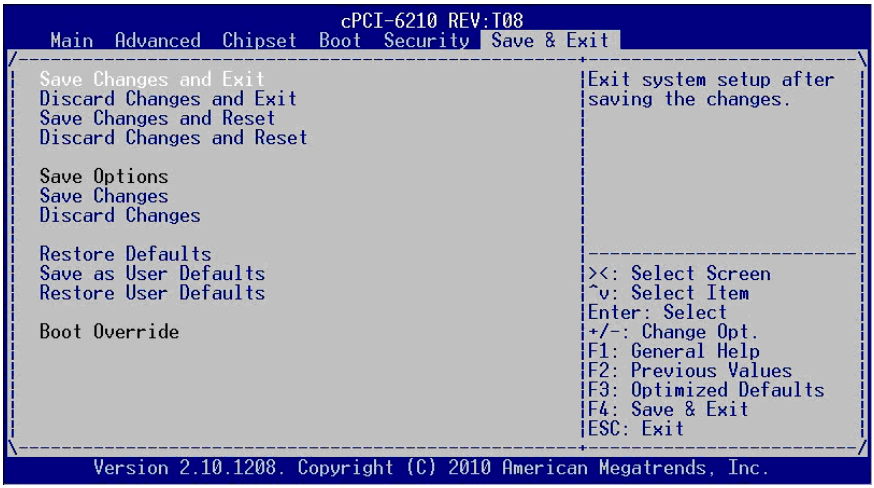
User Password

Use this option to set a password for users with limited access to the BIOS setup utility.

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8.7 Save & Exit

Select the Save & Exit tab from the setup screen to enter the Save & Exit setup screen. You can display a Save & Exit BIOS setup option by highlighting it using the < Arrow > keys. The Save & Exit BIOS setup screen is shown below.



Save Changes and Exit

When you have completed the system configuration changes, select this option to leave Setup and reboot the computer so the new system configuration parameters can take effect.

Discard Changes and Exit

Select this option to quit Setup without making any permanent changes to the system configuration.

Save Changes and Reset

Reset the system after saving the changes.

Discard Changes and Reset

Reset the system without saving any changes.

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Save Changes

Save changes made so far to any of the setup options.

Discard Changes

Discard changes made so far to any of the setup options.

Restore Defaults

Restore/Load Defaults values for all the setup options.

Save as User Defaults

Save changes made so far as User Defaults.

Restore User Defaults

Restore the User Defaults to all setup options

Boot Override

Use the up/down arrow keys to highlight a boot device to immediately exit the BIOS Setup and boot from the selected device.

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9 IPMI User Guide

9.1 Introduction

This chapter is written for those who already have a basic understanding of the newest implementation of the baseboard management controller (BMC) of the Intelligent Platform Management Interface (IPMI) specification rev. 2.0. It also describes the OEM extension IPMI command usages which are not listed in the IPMI specification.

9.2 Summary of Commands Supported by BMR-AVR-cPCI

The table below lists all the commands supported by the IPMC. The right most column indicates if a particular command is mandatory or optional for PICMG 3.0/2.9.

Command	IPMI Spec	NetFn	CMD	Description (Required by PICMG 3.0/2.9)
IPM Device "Global" Commands				
Get Device ID	20.1	App	01h	This command is used to retrieve the Intelligent Device's Hardware Revision, Firmware/Software Revision, and Sensor and Event Interface Command specification revision information.
Cold Reset	20.2	App	02h	This command directs the Responder to perform a 'Cold Reset' of itself. (Optional/Optional)
Warm Reset	20.3	App	03h	This command directs the Responder to perform a 'Warm Reset' of itself.
Get Self Test Results	20.4	App	04h	This command directs the device to return its Self Test results, if any. (Mandatory/Mandatory)

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Command	IPMI Spec	NetFn	CMD	Description (Required by PICMG 3.0/2.9)
Get Device GUID	20.8	App	08h	This command returns a GUID (Globally Unique ID), also referred to as a UUID (Universally Unique IDentifier), for the management controller. (Optional/Optional)
Broadcast "Get Device ID"	20.9	App	01h	This is a broadcast version of the 'Get Device ID' command that is provided for the 'discovery' of Intelligent Devices on the IPMB. (Mandatory/Mandatory)
IPMI Messaging Support Commands				
Send Message	22.7	App	34h	The *Send Message* command is used for bridging IPMI messages between channels, and between the system management software (SMS) and a given channel. (Optional/Optional)
BMC Watchdog Timer				
Reset Watchdog Timer	27.5	App	22h	The *Reset Watchdog Timer* command is used for starting and restarting the Watchdog Timer from the initial countdown value that was specified in the *Set Watchdog Timer* command. (Mandatory/Optional)
Set Watchdog Timer	27.6	App	24h	The *Set Watchdog Timer* command is used for initializing and configuring the watchdog timer. The command is also used for stopping the timer. (Mandatory/Optional)
Get Watchdog Timer	27.7	App	25h	This command retrieves the current settings and present countdown of the watchdog timer. (Mandatory/Optional)
Event Commands				
Set Event Receiver	29.1	S/E	00h	This global command tells a controller where to send Event Messages. (Mandatory/Optional)

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Command	IPMI Spec	NetFn	CMD	Description (Required by PICMG 3.0/2.9)
Get Event Receiver	29.2	S/E	01h	This global command is used to retrieve the present setting for the Event Receiver Slave Address and LUN. This command is only applicable to management controllers that act as IPMB Event Generators. (Mandatory/Optional)
Platform Event Message	29.3	S/E	02h	This command may be thought of as a request for the BMC to process the event data that the command contains. Typically, the data will be logged to the System Event Log (SEL). (Mandatory/Optional)
Sensor Device Commands				
Get Device SDR Info	35.2	S/E	20h	This command returns general information about the collection of sensors in a Dynamic Sensor Device. (Mandatory/Optional)
Get Device SDR	35.3	S/E	21h	The 'Get Device SDR' command allows SDR information for sensors for a Sensor Device (typically implemented in a satellite management controller) to be returned. (Mandatory/Optional)
Reserve Device SDR Repository	35.4	S/E	22h	This command is used to obtain a *Reservation ID*. (Mandatory/Optional)
Set Sensor Hysteresis	35.6	S/E	24h	This command provides a mechanism for setting the hysteresis values associated with the thresholds of a sensor that has threshold based event generation. (Optional/Optional)
Get Sensor Hysteresis	35.7	S/E	25h	This command retrieves the present hysteresis values for the specified sensor. (Optional/Optional)
Set Sensor Threshold	35.8	S/E	26h	This command is used to set the specified threshold for the given sensor. (Optional/Optional)
Get Sensor Threshold	35.9	S/E	27h	This command retrieves the threshold for the given sensor. (Optional/Optional)

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Command	IPMI Spec	NetFn	CMD	Description (Required by PICMG 3.0/2.9)
Set Sensor Event Enable	35.10	S/E	28h	This command provides the ability to disable or enable Event Message Generation for individual sensor events. The command is also used to enable or disable sensors in their entirety using the *disable scanning* bit. (Optional/Optional)
Get Sensor Event Enable	35.11	S/E	29h	This command returns the enabled/ disabled state for Event Message Generation from the selected sensor. The command also returns the enabled/ disabled state for scanning on the sensor. (Optional/Optional)
Get Sensor Event Status	35.13	S/E	2Bh	The Get Sensor Event Status command is provided to support systems where sensor polling is used in addition to, or instead of, Event Messages for event detection. (Optional/Optional)
Get Sensor Reading	35.14	S/E	2Dh	This command returns the present reading for sensor. The sensor device may return a stored version of a periodically updated reading, or the sensor device may scan to obtain the reading after receiving the request. (Mandatory/Optional)
Get Sensor Type	35.16	S/E	2Fh	This command is used to assign the Sensor Type and Event/Reading Type to a specified sensor. (Optional/Optional)
FRU Device Commands				
Get FRU Inventory Area Info	34.1	Storage	10h	Returns overall the size of the FRU Inventory Area in this device, in bytes. (Mandatory/Optional)
Read FRU Data	34.2	Storage	11h	The command returns the specified data from the FRU Inventory Info area. (Mandatory/Optional)
Write FRU Data	34.3	Storage	12h	The command writes the specified byte or word to the FRU Inventory Info area. (Mandatory/Optional)

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9.3 OEM Commands Summary Table

Command	NetFn Code	Cmd Code
OemShowRevision	OEM (C0h)	12h
OemRescanGaInput	OEM (C0h)	22h
OemTestFunction	OEM (C0h)	30h
OemSetBlueLEDLongBlinking	OEM (C0h)	31h
OemReportGeoAddress	OEM (C0h)	F0h
OemEnableSmbus	OEM (C0h)	F2h
OemDisableSmbus	OEM (C0h)	F3h
OemDispDebugVariable	OEM (C0h)	F4h
OemResetHost	OEM (C0h)	F5h
OemPowerOff	OEM (C0h)	F6h
OemPowerOn	OEM (C0h)	F7h

OemShowRevision

This command is used to show the current information of the firmware including the firmware revision, the product ID, and additional features.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	12h	OEM defined command
Response	0	Complete Code	00h means OK
	1	A5h	Internal check byte. Always A5h
	2	*Firmware Rev	'V' in ASCII code for verification
	3	*Firmware Rev	Revision info high byte
	4	*Firmware Rev	Revision info low byte
	5	*Product ID	'P' in ASCII code for verification
	6	*Product ID	Product info high byte
	7	*Product ID	Product info low byte
	8	*Special info	'S' in ASCII code for verification
	9	*Special info	Addition info byte
	10	5Ah	Internal check byte. Always 5Ah

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OemRescanGaInput

This command is used to rescan the geo-address input pins and reset the IPMB address according to the input value.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	22h	OEM defined command
Response	0	Complete Code	00h means OK
	1	New IPMB address	New IPMB address value

OemTestFunction

Internal test purposes only.

OemSetBlueLEDLongBlinking

This command is used to enable or disable the slow blink of the blue HotSwap LED when a voltage is detected to be over ±5% out of range for five seconds (see Table 4-1 on page 22). This function is set to enabled by default.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	31h	OEM defined command
	2	00h or 01h	00h: disable slow blink capability 01h: enable slow blink capability
Response	0	Complete Code	00h means OK

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OemReportGeoAddress

This command can report the IPMB address, the GA pin input status, and the event forwarding control value.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F0h	OEM defined command
Response	0	Complete Code	00h means OK
	1	IPMB address	IPMB address value
	2	GA value	GA pin input status
	3	Control value	Current control value of event forwarding

OemEnableSmbus

This command is used to turn on the I2C bus when it is off during boot up process. Usually BIOS will perform this command after booting in boards with ServerWorks chipset.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F2h	OEM defined command
Response	0	Complete Code	00h means OK

OemDisableSmbus

This command is used to shut down I2C bus access.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F3h	OEM defined command
Response	0	Complete Code	00h means OK

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OemDispDebugVariable

This command can report up to 5 interval values for debug purposes. For developers only.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F4h	OEM defined command
Response	0	Complete Code	00h means OK
	1	*Debug variable 1	
	2	*Debug variable 2	
	3	*Debug variable 3	
	4	*Debug variable 4	
	5	*Debug variable 5	

OemResetHost

This command is implemented to control the system's status if rebooting is required. Operators can control the system remotely.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F5h	OEM defined command
Response	0	Complete Code	00h means OK

OemPowerOff

This command is implemented to control the system's status if power-off is required. Operators can control the system remotely.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F6h	OEM defined command
Response	0	Complete Code	00h means OK

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OemPowerOn

This command is implemented to control the system's status if power-on is required. Operators can control the system remotely.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F7h	OEM defined command
Response	0	Complete Code	00h means OK

9.4 CompactPCI Address Map

Since more than one system may be installed in a single chassis, we allocate each IPMB address based on GA input as peripheral cards. The CompactPCI Peripheral Address Mapping Table is given below.

CompactPCI Peripheral Address Mapping			
Geo. Addr.	**IPMB Addr.**	**Geo. Addr.**	**IPMB Addr.**
0	**Disabled**	16	D0h
1	B0h	17	D2h
2	B2h	18	D4h
3	B4h	19	D6h
4	B6h	20	D8h
5	B8h	21	DAh
6	Bah	22	DCh
7	BCh	23	DEh
8	BEh	24	E0h
9	Coh	25	E2h
10	C4h	26	E4h
11	C6h	27	E6h
12	C8h	28	E8h
13	CAh	29	EAh
14	CCh	30	ECh
15	CEh	**31**	**Disabled**

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9.5 Communications with IPMC

Operating systems need to use a serial port to communicate with the IPMC. The resource setting of the serial port must be IO: 0x2F0 and IRQ: 7. The communication setting of the serial port must be BaudRate: 9600, DataBit: 8, ParityCheck: None, StopBit: 1, and FlowControl: None. In Windows XP, use "COM6" to communicate with the IPMC.

9.6 IPMI Sensors List

Sensor Number	Sensor name	Normal Reading	Sensor Reading Value of IPMI Get Sensor Reading Command
01h	BMC Watchdog		Timeout action: 000b = no action 001b = Hard Reset 000b = Power Down 011b = Power Cycle 100b - 111b = reserved
02h	3.3V	3.3 V	Raw data of 3.3V sensor
03h	5V	5 V	Raw data of 5.0V sensor
04h	12V	12 V	Raw data of 12.0V sensor
05h	CPU Temp	40ºC	Raw data of CPU Temp sensor
06h	SYSTEM Temp	25ºC	Raw data of SYSTEM Temp sensor

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9.7 Relevant Documents

Document Title	Revision	Source
Intelligent Platform Management Interface Specification v2.0	Document Revision 1.0 February 12, 2004	Intel Corp. http://www.intel.com/design/servers/ipmi/spec.htm
PICMG 2.9 D1.0 CompactPCI System Management Specification	January 21, 2000	
Intelligent Platform Management Bus Communications Protocol Specification v0.9	Document Revision 0.15 June 24, 1997	Intel Corp. http://www.intel.com/design/servers/ipmi/license_ipmi.htm

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Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

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- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

A Lithium-type battery may be provided for uninterrupted, backup or emergency power.



Risk of explosion if battery is replaced with one of an incorrect type. Dispose of used batteries appropriately.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

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