Users Guide

for
ADLINK Technology

cPCI-6240

Network Processor Base Board

IXP2400 based 6U, PICMG 2.16, *CompactPCI* Board

Revision 1.01

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Revision History

Revision	Description	Date
1.0	Initial Release	04/03/2004
1.01	Minor corrections for spelling and RedBoot flash write information	04/26/2004

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Overview

The cPCI-6240 is an Intel ® IXP2400 based PICMG® 2.16 compliant Network Processor Board. Dual PMC sites are provided to support PTMC and control plane processing PMC modules. An on-board Ethernet switch provides flexibility in the routing of packets to and from the network processor, front panel, and PICMG 2.16 interface.

This board, in conjunction with ADLINK Technology Framer-Mapper PTMC cards (Quad OC-3 or Single OC-12), provide an ideal solution for the conversion of SONET ATM, or Packet-over-Sonet (PoS) to IP (Gigabit Ethernet). The cPCI-6240 is designed to meet the needs of network access and edge applications for wireless and broadband markets including BSC/RNC/MSC, CMTS, DSLAM, FTTx, NG-DLC, etc. The cPCI-6240 delivers ultimate performance in multi-service switch and layer 4-7 applications including firewall, IDS, and load balancing, etc.

Features

- PICMG 2.0 R3.0 CompactPCI Core Specification
- PICMG 2.16 R1.0 CompactPCI Packet Switched Backplane Specification
- PICMG 2.1 R2.0 CompactPCI Hot Swap
- PICMG 2.9 R1.0 CompactPCI System Management Specification
- PICMG 2.15 R1.0 PCI Telecom Mezzanine/Carrier Card Specification
- 600MHz Intel® IXP2400 Network Processor
- 512 Mbytes DDR DRAM ECC protected (SO-DIMM)
- 4 Mbytes QDR SRAM ECC on-board
- 16 Mbytes FLASH EPROM on-board
- Serial Debug Port with Front or rear I/O access
- 64 Bit, 66MHz CompactPCI Bus Interface
- PTMC Site
- PrPMC Site
- Onboard Gigabit Ethernet Switch for maximum flexibility
- Dual Front Panel 10/100/1000Mbit Ethernet Ports
- Dual PICMG 2.16 10/100/1000Mbit Ethernet support
- Additional Dual Rear I/O 10/100/1000Mbit Ethernet Ports for transition module
- VxWorks Tornado 2.2 and LINUX board support package

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Block Diagram

The following is a block diagram of the CPCI-6240 IXP2400 based network processor board.

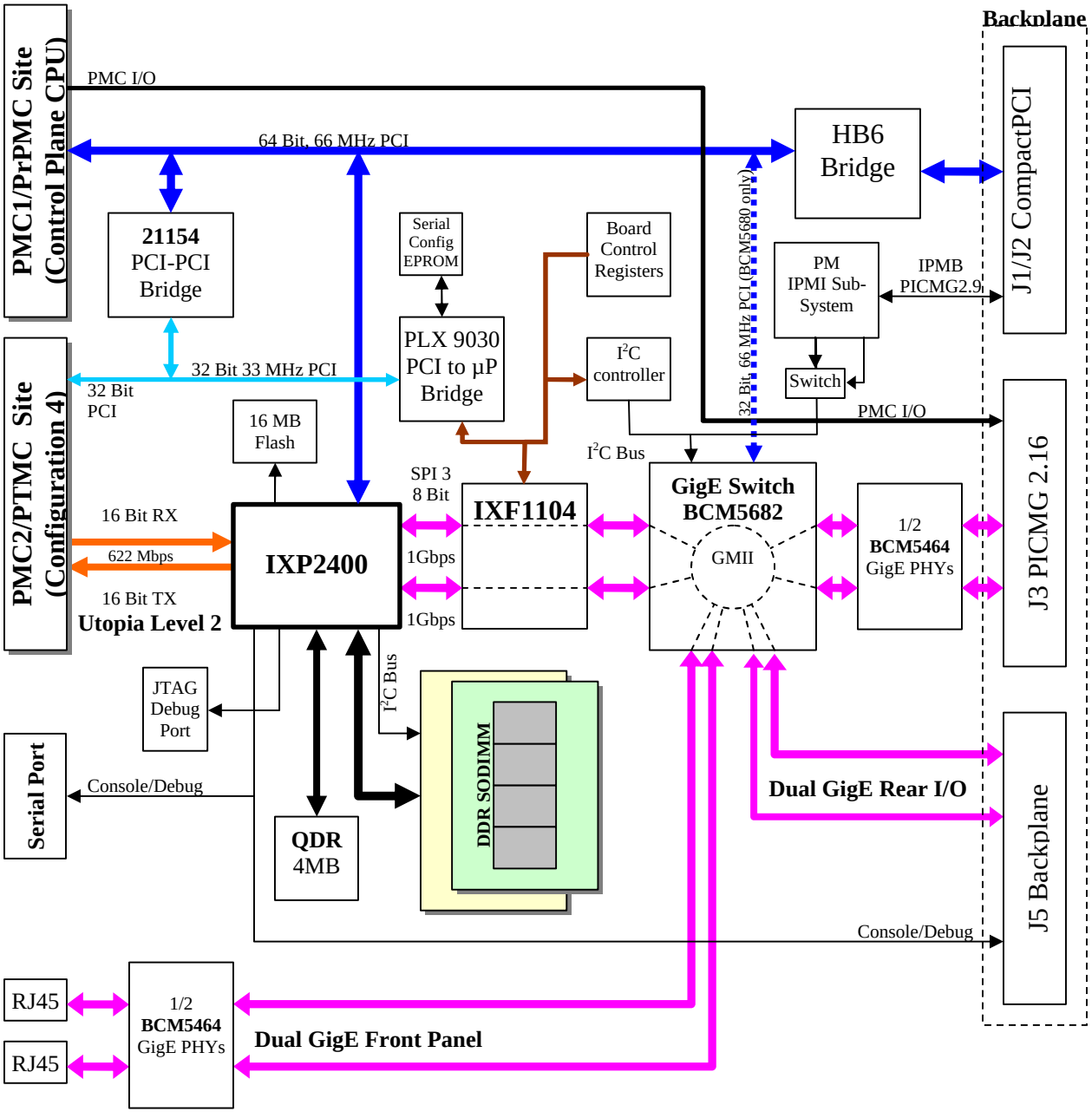
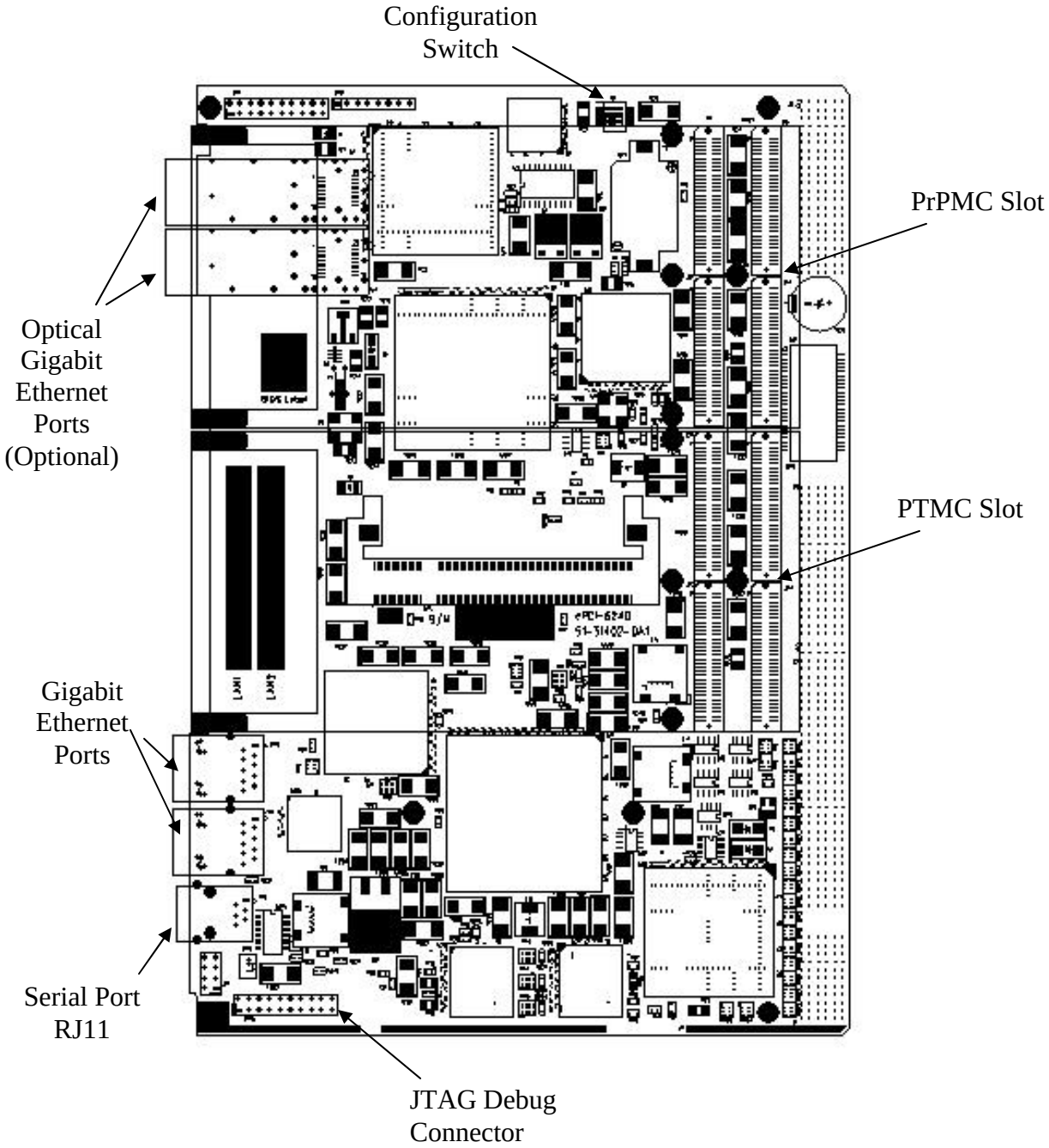


Figure 1

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Board Layout

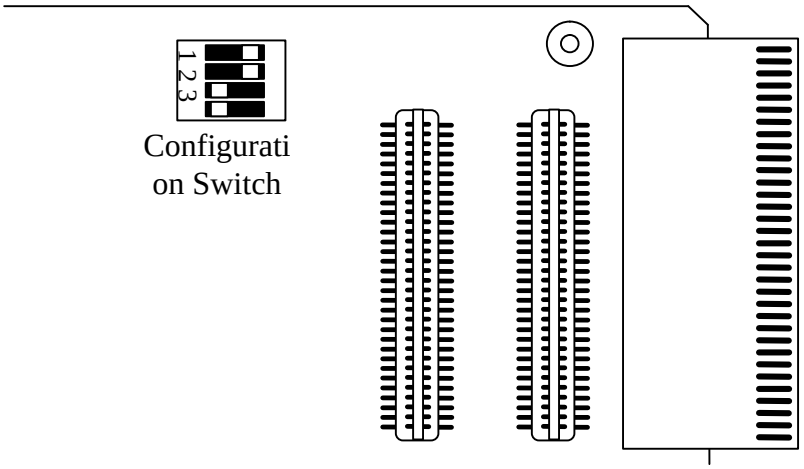
Below is a drawing of the CPCI-6240 board showing the position of connectors and the configuration switch.



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Configuration Switch Settings

There is an on-board configuration switch that is used to configure the board. The following table shows the possible options that can be set.



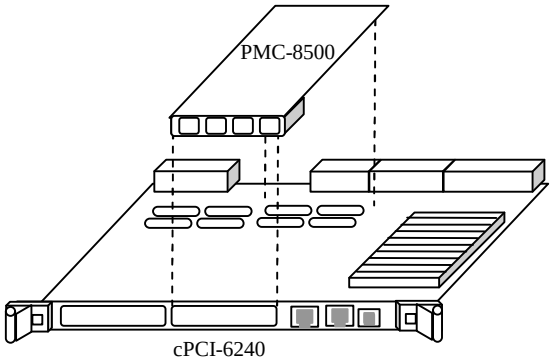
Switch Settings

Switch Position	Function	Description
1	User Configuration	This switch can be read by application code to provide a user configuration option.
2	User Configuration	This switch can be read by application code to provide a user configuration option.
3	PrPMC Monarch Enable	This switch is used to enable the Processor PMC monarch mode. In normal operation this switch should be OFF. If a PrPMC card is used, this switch can be set to ON to allow the PrPMC to become the PCI host. Note that if a PrPMC is the PCI host it must perform PCI configuration and interrupt handling. The IXP2400's XSCALE core will no longer perform these functions.
4	CPCI Chassis Reset Isolation	This switch is used to isolate the CPCI-6240 card RESET# from the CompactPCI bus. If the switch is set to OFF, resets on the CompactPCI bus will not affect the card. If the switch is ON, a CompactPCI reset occurrence will also reset the CPCI-6240 card. This switch should be OFF in chassis that do not have a PCI bus such as PICMG 2.16 only systems.

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PMC-8500 Installation

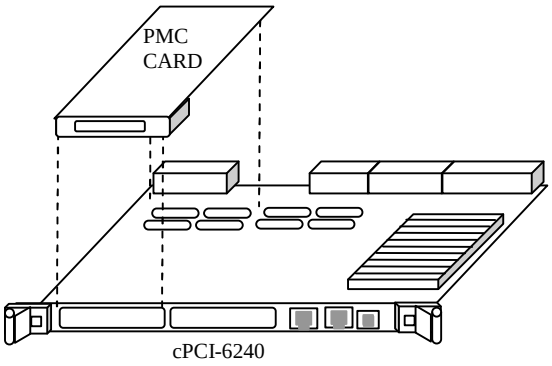
If a PMC-8500 is to be used, it must be installed in the PMC2/PTMC site as shown below.



Note: This site may also be used for standard PMC cards as long as the card is 32 bits with no rear I/O connections.

PMC/PrPMC Installation

Any standard PMC or PrPMC card may be installed into the PMC1 site as shown below.



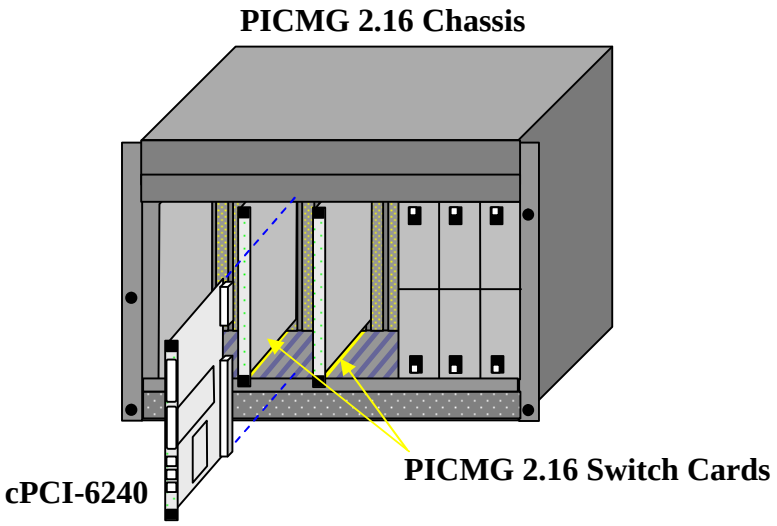
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Chassis Installation

The CPCI-6240 is a peripheral card and can be installed into any standard CompactPCI or PICMG2.16 peripheral slot. When installing the card into a chassis, make sure that the card is seated correctly and the card ejector latches are fully engaged. If the bottom ejector latch is not engaged the card will not boot.

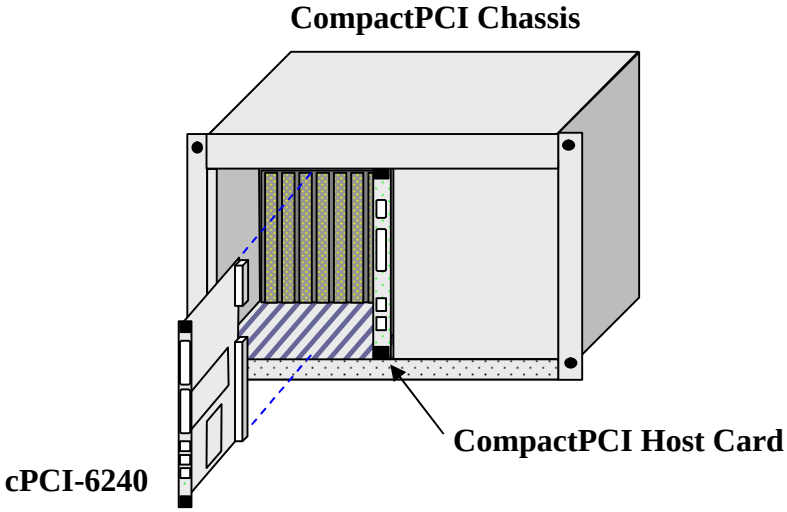
PICMG 2.16 Compatible Chassis Installation

The cPCI-6240 card can be installed into any node slot of a compatible PICMG 2.16 chassis.



Standard CompactPCI Chassis Installation

The cPCI-6240 card can be installed into any peripheral slot of a compatible CompactPCI chassis.



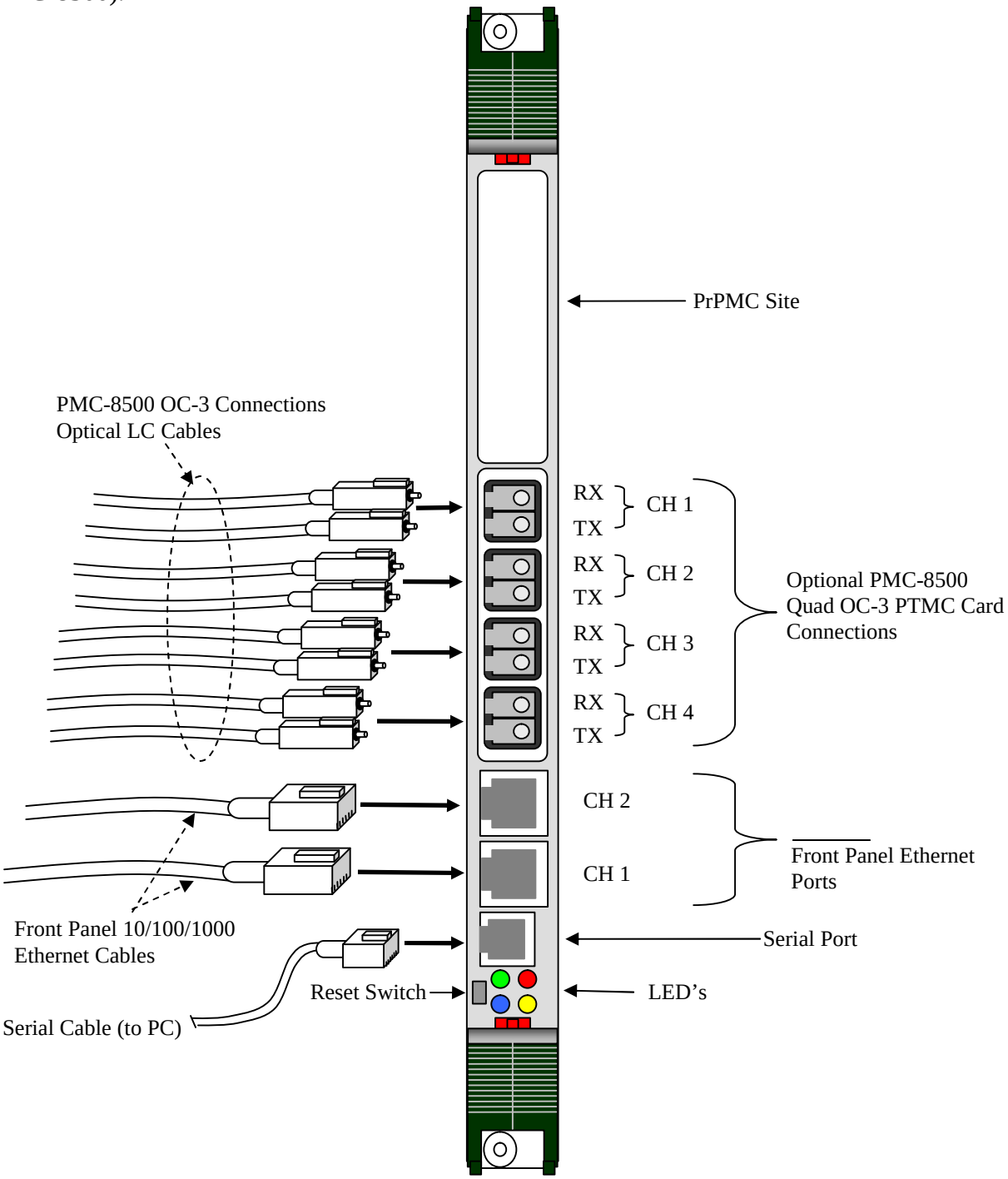
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Front Panel Connections

This section describes the test cable connections for both the cPCI-6240-1 and cPCI-6240-2 versions of the board.

CPCI 6240-1 Cables

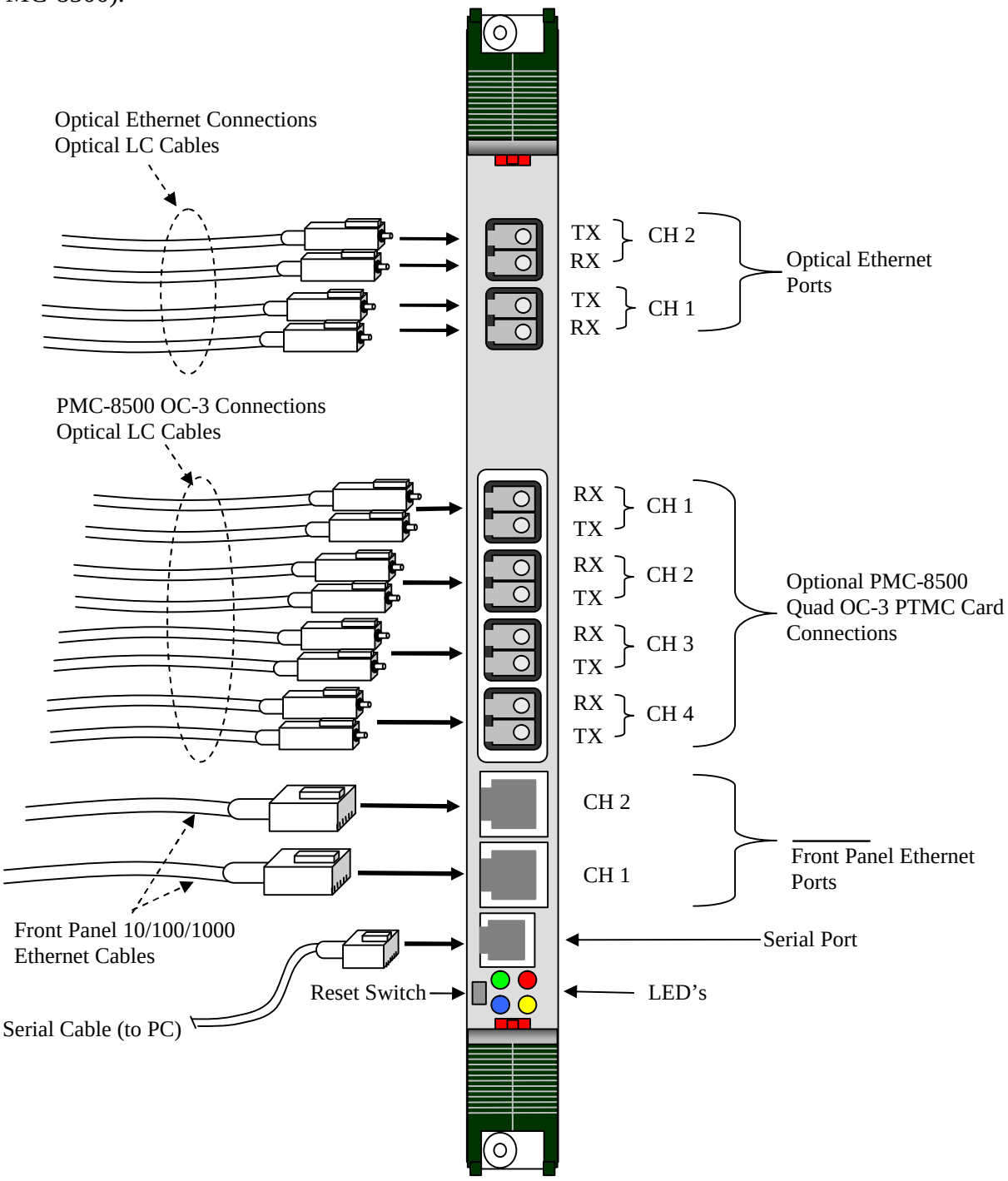
Below is a diagram showing cable connections to the cPCI-6240-1 card (including the PMC-8500).



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CPCI 6240-1 Cables

Below is a diagram showing cable connections to the cPCI-6240-2 card (including the PMC-8500).

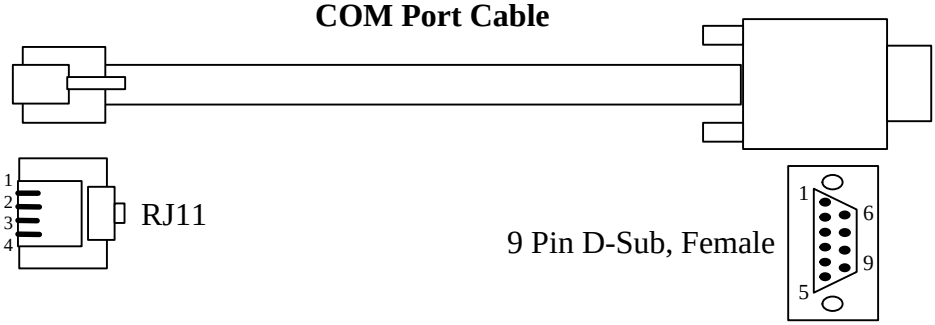


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Serial Cable

To initially use the card and develop applications you will need a serial cable. The serial cable required for use with standard COM ports is shown below. It is an RJ11 to female DB9 converter. This cable connects the CPCI-6240's serial port (RJ11 connector J15), to a standard PC's COM port.

COM Port Cable

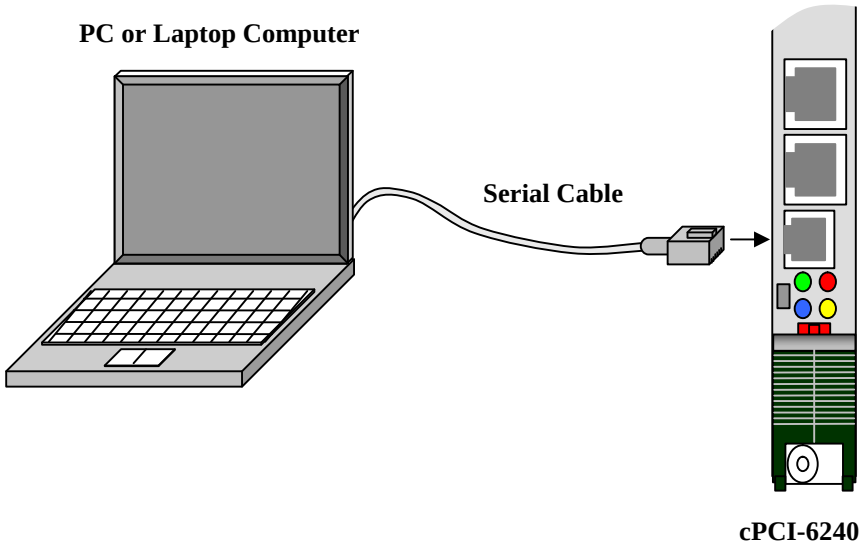


RJ11 6 Pin	RJ11 4 Pin	9 Pin D-Sub Pin#	9 Pin D-Sub Pin#
1		(Not Used)	Chassis Ground
2	1	3	TX
3	2	2	RX
4	3	5	Ground
5	4	(Not Used)	Ground
6		(Not Used)	Ground

Note: This table shows the connections using either a 6 pin or 4 pin, RJ11 connector.

Serial Cable Connection

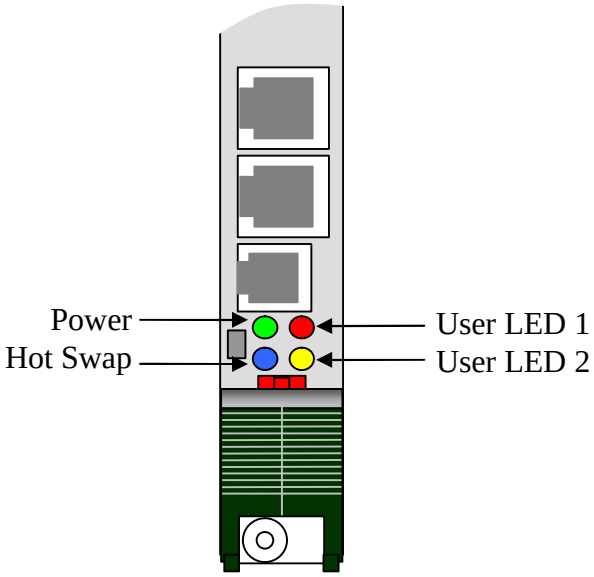
A serial cable is connected from the computers serial port (COM 1 or COM 2) to the serial interface of the cPCI-6240 card.



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Front Panel LED's

Below is a diagram showing the front panel LEDs.



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Boot Monitor Firmware Development

Generally, the RedBoot monitor will not need to be changed by the user. If the RedBoot monitor does need to be modified, the following tools are required.

CYGWIN Tools:
- cygwin, GNUPro (010827).
- BASH Shell
- GNU version of MAKE

Diagnostics Program Firmware Development

Normally the Diagnostics will not be changed by the user, however the Diagnostics module can be used as an example for Direct Program and Utility development.

CYGWIN Tools:
- Cygwin, GNUPro (010827).
- GNU version of MAKE

Intel IXP2400 SDK (µcode development)

Direct Program Development

Programs and utilities can be coded and loaded into flash prom and executed under the RedBoot Monitor.

CYGWIN Tools:
- Cygwin, GNUPro (010827).
- GNU version of MAKE

Intel IXP2400 SDK (µcode development)

VxWorks Application Development

To develop VxWorks based applications the following software is required.

Tornado 2.2/VxWorks 5.5 for XScale
CPCI-6240 Drivers and Documentation
PMC-8500 PTMC (IXF6012) Driver and Documentation
Intel IXP2400 SDK (µcode development)

Linux Application Development

TBA

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Firmware

This chapter contains the following sections which describe these major firmware capabilities on the CPCI-6240:

• Boot Monitor
• Diagnostics
• WindRiver* VxWorks* Board Support Package (BSP)

Serial Port Access to the CPCI-6240

To connect the CPCI-6240 to the development platform Host system, perform the following steps:

1. Connect the CPCI-6240 serial port to your development host serial port.

2. Run a terminal emulation program such as HyperTerminal for Microsoft* Windows systems or minicom for Linux systems, and configure it for VT100 emulation with communications settings of no flow control and no parity bits, 8 data bits, 1 stop bit, a baud rate of 115200.

3. Reset or power-up the CPCI-6240 card. At this time you should see the redboot monitor program start with the following information displayed.

```
 Testing Xscale Scratchpad memory... PASS
 Testing I2C Interface... PASS
 Testing SDRAM memory... PASS
Scrubbing SDRAM
Found IXP2400 Rev. B0
Core clock frequency is 600 MHZ
+
RedBoot(tm) bootstrap and debug environment, version R1.24 - built
13:14:02, Jul  26 2003

Platform: ADLINK cPCI-6240 (XScale) PRE-RELEASE FOR EVALUATION
PURPOSES ONLY Copyright (C) 2000, 2001, Red Hat, Inc.

SDRAM(256M): 0x00000000 - 0x20000000, 0x00200000 - 0x0ffdf000
available SRAM Channel 0(4M): 0x80000000 - 0x80400000 No SRAM found
on channel 1
FLASH(16M): 0xc4000000 - 0xc5000000, 128 blocks of 0x00020000 bytes
each.
RedBoot>
```

Binary Images

The following are the binary images (with filenames in parentheses) burned into the flash memory at time of this version's shipment:

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• The Boot Monitor (RedBoot)
• The VxWorks bootrom: the boot loader for VxWorks (bootrom)
• The Diagnostics application (diag)
• A RAM based ROMable version of VxWorks* for Serial Connections (vxWorks_rom.bin) where *ROMable* refers to the ability to load and re-load into flash ROM a designated binary.

Boot Monitor

Getting Started with Boot Monitor

The Boot Monitor is based on RedBoot*, which is an acronym for **"R**ed Hat* **E**mbedded **D**ebug and **Boot**strap." RedBoot is the standard embedded system debugging and bootstrap environment from Red Hat.

The Boot Monitor provides a complete bootstrap environment for a range of embedded operating systems, such as VxWorks*, and includes facilities such as network and serial downloading. It also provides a simple flash memory file system for maintaining boot images.

The Boot Monitor provides a wide set of tools for downloading and executing programs on target system, as well as tools for manipulating the target system's environment. It can be used for both product development (debug support) and for end product deployment (flash memory and network booting).

Here are some highlights of Boot Monitor's capabilities:

• Boot scripting support
• A simple Command Line Interface (CLI) for Boot Monitor configuration and management which is accessible via the serial (terminal) connection.
• Attribute configuration which provides user control of such aspects as system time and date
• A default flash memory image to boot from, as well as a default fail-safe image, a static IP address, etc.
• X/YModem support for image download via serial connections
• Power-On Self-Test (POST)

You can use the Boot Monitor program as generalized system debugging and bootstrap-controlling software for any operating system.

Installing the Boot Monitor

The Boot Monitor runs from the target platform's flash memory boot sector or boot ROM; it is designed to load when the system is initially powered on. The Boot Monitor image can be programmed either into flash memory *in situ* or into the flash memory (or ROM) using a device programmer. Once installed, user-specific configuration options can be applied, using the `fconfig` command. See details below.

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User Interface

The Boot Monitor provides a command line user interface (CLI). You can access this interface via the serial port on the platform unit. The Boot Monitor CLI is also accessible using the telnet access protocol using an Intel 82559 based PMC Network Interface Controller. By default, the Boot Monitor runs telnet on TCP port 9000, but this is user-configurable.

> Caution: On Windows machines, the telnet console may not work properly. This seems to be a problem with the Windows implementation. Intel recommends that you use a Linux telnet console instead if telnet is your preferred communication protocol.

Command Line Interface Via Network Interface

The Boot Monitor CLI can only be accessed via a network connections when using an Intel 82559 based PMC Network Interface Controller card. If the PMC site is being used for another device the serial port must be used for CLI access.

Target Network Configuration

Each node in a networked system must have a unique address. Since the network support in Boot Monitor is based on TCP/IP, this address is an IP (Internet Protocol) address. There are two ways for a system to learn its IP address. First, it can be stored locally on the platform; this is known as having a *static IP addres*s. Second, the system can use the network itself to discover its IP address; this is known as a *dynamic IP addres*s. The Boot Monitor supports this dynamic IP address mode by use of the BOOTP, a subset of the Dynamic Host Control Protocol (DHCP). In this case, Boot Monitor asks the network (actually a generic server on the network) for an IP address to use.

> Note: The Boot Monitor only supports BOOTP.

Use the fconfig command to set the IP address type; this choice is stored in flash memory. The Boot Monitor only queries the flash memory configuration information at reset, so to make any changes effective requires restarting the platform.

Use the fconfig -l (list) command to display the currently set value for the IP address type which is indicated by the activation of BOOTP.

Here is an example of the Boot Monitor fconfig -l command, showing the network addressing values:

```
RedBoot> fconfig –l
Run script at boot: false
Use BOOTP for network configuration: false
Local IP address: 192.168.1.29
Master’s Local IP address: 10.3.31.19
Slave’s Local IP address: 10.3.31.20
```


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```
Default server IP address: 192.168.1.101
connection port: 9000
Network debug at boot time: false
```

If the selection for Use BOOTP for network configuration had been true, these IP addresses would be determined at boot time via the BOOTP protocol. In this case, the Use BOOTP for network configuration value has been set false and the board has been configured with a static IP address listed as the Local IP address. The default server IP address specifies which network node to communicate with for TFTP service. Note that this address can be overridden directly using TFTP commands.

The Boot Monitor supports incoming commands via the serial ports or the network port. This port number is the TCP port that Boot Monitor uses to accept incoming connections; these connections can be used for generic Boot Monitor commands. In particular, it is possible to communicate with the Boot Monitor via the telnet protocol. The Boot Monitor cannot communicate with machines on different subnets **because it does not support routing**.

Boot Monitor Commands

The Boot Monitor implements all the commands provided by the RedBoot software. For a full description of command usage and examples, please refer to the RedBoot User Guide set available at www.redhat.com.

The following is a list of the available commands and their syntax:

alias name [value]
Manages aliases kept in flash memory

cache [ON | OFF]
Manages machine caches

dump -b <location> [-l <length>]
Displays (hex dump) a range of memory

fis {commands}
Manages flash memory images using a set of {commands}.

fconfig [-i] [-l] [-n] [-f] | nickname [value]
Manages configuration kept in flash memory

go [-w <timeout>] [entry]
Executes code at a specified location

help [<topic>]
Provides Help by listing all commands or specific to <topic>

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load [-r] [-v] [-d] [-h <host>] [-m {TFTP | xyzMODEM}] [-b <base_address>] <file_name>
Loads a file

ping [-v] [-n <count>] [-t <timeout>] [-i <IP_addr] -h <IP_addr>
Performs a network connectivity test

reset
Resets the system

Version
Displays the RedBoot version information

Rebuilding the Boot Monitor

In normal circumstances it is only necessary to rebuild the Boot Monitor if it has been modified, for example, if you have extended the command set or applied patches.
To rebuild the Boot Monitor:

1. Make sure your PATH environment variable is properly set to find GNU compiler and linker.

2. Open a Cygwin bash shell window.

3. Go to the Boot Monitor directory.

4. Issue the command
`./RUNIT.sh`

Table . Files Created During a Boot Monitor Rebuild

`build/install/bin/redboot.elf`	This is the complete version of Boot Monitor, represented in ELF format. It is most useful for testing with tools such as embedded ICE, or other debug tools.
`build/install/bin/redboot.srec`	This version has been converted to Motorola* S-record format.
`build/install/bin/redboot.list`	Disassembly of RedBoot.elf file.
`build/install/bin/redboot.bin`	This version has been flattened, that is, all formatting information has been removed, leaving only the raw image to be placed in ROM or flash.

Once complete, the redboot.bin file can be used to update the flash EEPROM.

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Updating the Boot Monitor

The Boot Monitor normally runs from flash memory or in ROM. In the case of flash, it is possible to update Boot Monitor, that is, replace it with a newer version. This process is complicated because the Boot Monitor is running from the same flash memory which is being updated.

The following sections describe in detail this outline of the steps needed for updating Boot Monitor:

• Start the Boot Monitor from flash.

• Load a different version of Boot Monitor in RAM.

• Update the primary Boot Monitor flash memory image.

• Reboot and run Boot Monitor from flash.

For this process, it is assumed that the target is connected to a host system and that there is some sort of serial connection available for the Boot Monitor CLI.

Start the Boot Monitor from Flash

To start Boot Monitor, reset the platform.

Loading a Different Version of Boot Monitor into RAM

You can use the serial port connection to load the image into SDRAM. The following examples use serial communication.

Caution: The values listed in the following procedure are the standard defaults for loading into RAM, not examples. You must use them as stated.

To load a different (upgrade) version of Boot Monitor using a serial connection:

1. Launch the HyperTerminal program.

2. Using the serial connection, load the image into the target's SDRAM using this command:

```
load -r -v -b 0x400000 -m y
```

3. Select Transfer and choose the Send File command from its menu.

4. When the Send File dialog appears, browse to the filename of the image file and then select the YModem protocol and click Send to transfer the image.

To load a different (upgrade) version of Boot Monitor using Ethernet port:

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1. Verify that a TFTP server is running on the host machine (contains all the necessary binaries), which is within the same subnet as the IXDP2400 platform.

2. Load the image into the target's SDRAM using this command:

```
load -r -v -b 0x400000 –m tftp redboot.bin
```

Updating the Primary Boot Monitor Flash Memory Image

1. Issue the command

```
fis write -f 0xc4000000 -b 0x400000 -l 0x40000
```

2. Answer yes to all by questions by pressing “y”.

Rebooting the Run Boot Monitor from the Flash Memory

Once the image has been successfully written into the flash, simply reboot the target (platform) and the new version of Boot Monitor is loaded.

Diagnostics Program

The requirements of the CPCI-6240 diagnostics are as follows:

• The diagnostics distribution source/binary

• Red Hat* (GnuPro) distribution

• Serial port access to the target Network Processor Units (NPUs)

Building the Diagnostics Binary

To build the diagnostics program binary:

1. Checkout the source files for the diagnostics program from the Diagnostics distribution into a directory (for example, `diagnostics`).

2. Install the Cygwin* for Microsoft* Windows* application and the Cygwin compiler for Intel® XScale™ technology.

3. At the highest level where the diagnostics reside, modify the file makefile.inc and set the environmental variable `TOPDIR` equal to the path where the diagnostics reside.

4. Within Cygwin, go to the diagnostics directory.

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5. Run the command make to create the diag.elf, diag.srec, diag.bin, and diag.list files in the same directory.

Note: The file diag.list provides the information and layout of these images.

Burning-in and Loading the Flash Memory via the Boot Monitor

Here are the steps:

1. Launch the HyperTerminal program.

2. Load the diagnostics image into the target's SDRAM using the `load` command.

3. Select Transfer and choose Send File from its menu.

4. When the Send File dialog appears, browse to the filename of the image file and then choose the YModem protocol.

5. Click Send to transfer the image.

6. Program the image into flash memory using the fis create command.

For example, to load the image via the serial port using Ymodem access use these commands:

```
RedBoot> load diag.bin -r -b 0x400000 -m y
RedBoot> fis create -b 0x400000 -l 0xc0000 -r 0x300000 -e 0x300000 diag
```

7. To load and execute diag use these commands:

```
RedBoot> fis load diag
RedBoot> go
```

Starting Diagnostics

To start the Diagnostics from the Boot Monitor run the following commands.

```
RedBoot> fis load diag
RedBoot> go
```

The following information is displayed:

```
Found IXP2400 Rev. B0
SRAM Channel 0: 0x80000000 - 0x80400000
No SRAM found on channel 1
16M flash found, 128 regions
Enabling FIQ and IRQ in CPSR
Enabling Data cache
```


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```
cPCI-6240 Board Diagnostics ver. 0.5, 11:43:24, Sep  3 2003
NPU Speed:600 Mhz
DRAM:256 Mb,
SRAM:4 Mb; Ch0: 4 Mb, Ch1: 0 Mb,
Running as Master NPU.
Single Flash.
DIAG>
```


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Using Diagnostics

Once the diagnostics application boots and the `MASTER_DIAG>` prompt appears, run the diagnostics commands.

The Diagnostic Command Set

To view the diagnostic commands with a simple definition, issue the "?", or "help" command and the following help display will appear:

```
DIAG> help

Access Commands:
blockcopy.....copy memory block          c[bwd].......change memory
contents
cfg[rw][bwd]..PCI config access          fill.........fill memory with
pattern
i2cread.......Read an I2C device
mem[rw][bwd]..PCI memory access          p[bwd].......print memory
contents
viewlog.......view entries in log        wrv..........Write-Read-Verify
memory

Kernel Commands:
don...........dcache enable              doff.........dcache off
ion...........icache enable              ioff.........icache off
setbaud.......set serial baud rate       tf...........set DIAG test
flags

Utility Commands:
?.............display this help screen   banner.......Print banner
exit..........Exit Diagnostics           h(elp).......display this help
screen
sethoe........Set Halt On Error          setverbose...Set verbose level
t(est)........Run DIAG test

Note: additional help is available on the above commands,
for help on each command type 'h command<cr>'.

DIAG>
```

DIAG Command "`blockcopy`"

This command is ised to copy a block of memory from one location to another.

DIAG Command "`c[bwd]`"

This command is used to edit memory.

DIAG Command "`cfg[rw][bwd]`"

This command is not functional at this time.

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DIAG Command "fill"

This command is used to fill a memory block with a specific value.

DIAG Command "mem[rw][bwd]"

This command is not functional at this time.

DIAG Command "p[bwd]"

This command is used to dump or display a section of memory.

DIAG Command "viewlog"

This command is not functional at this time.

DIAG Command "wrv"

This command is used to write and read verify a section of memory.

Kernel Commands:

DIAG Command "don"

This command is used to set the data cache on.

DIAG Command "doff"

This command is used to set the data cache off.

DIAG Command "ion"

This command is used to set the Instruction cache on.

DIAG Command "ioff"

This command is used to set the Instruction cache off.

DIAG Command "setbaud"

This command is used to re-set the serial port baud rate.

DIAG Command "tf"

This command is used to enable or disable specific tests when running the "**t all**" diagnostics command.

Utility Commands:

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DIAG Command "?"

This command will display the diagnostic help information.

DIAG Command "banner"

This command will display the diagnostics start-up information.

DIAG Command "exit"

This command will cause the diagnostics to quit and exit back to the redboot monitor.

DIAG Command "h(elp)"

This command will display the diagnostic help information.

DIAG Command "sethoe"

This command will set or reset the Holt On Error flag for the "**t all**" diagnostics command.

DIAG Command **"setverbose"**

This command is not functional at this time.

DIAG Command "t(est)"

This command is used to run a suite of tests on different functions of the CCPCI-6240 card.

```
 DIAG Test Help Screen:

all            (tests the system with tests that are enabled by tflags)
flash         (tests the flash lock capability)
gpio          (tests the GPIO registers and some selected pins)
hb6           (tests and programs EEPROM configuration of the HB6)
mac           (tests IXF1104 internal and external loopbacks)
mem           (tests QDR and DDR memory through multiple tests)
pci           (tests some of the PCI functionalities)
plx           (tests PLX9030, checks and programs configuration)
ptmc          (tests PTMC internal and external loopbacks)
sf            (tests some MSF registers and switch fabric functions)
sloop         (tests MAC and PTMC (Super Loop-back)
timers        (tests the capability of the timers (interrupt driven))
uart          (tests UART's read/write functionality)
ueng          (tests microengine's generic functionality)
xscale        (tests XScale's Interrupts and Scratchpad)
6240-1        (tests all functions of the -01 version of the board
6240-2        (tests all functions of the -02 version of the board
emi           (Puts traffic on all external ports for EMI tests
```


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VxWorks BSP

The following is required to boot the Intel ® IXDP2400 Advanced Development Platform with the VxWorks Operating System.

- The CPCI6240 BSP
- Tornado* 2.2

Building the VxWorks BSP

Note: **If you are re-compiling** the Board Support Package, verify these settings:

a) For vxworks_rom.bin (serial): SINGLE_BOOTROM is defined to 0, the BSP VTS defines are not included, SERIAL_DEBUG defined, and INCLUDE_FLASH is **not** defined in `config.h`.

b) For vxworks (downloadable VxWorks image): SINGLE_BOOTROM is defined to 1, BSP VTS includes are included, and SERIAL_DEBUG is **not** defined in `config.h`.

Building Using the Command Line Interface

1. Issue these two commands at the command prompt:
`cd /Tornado/target/config/cpci6240_be make <`*`target_image`***`>`**
where the <*target image*> could be:

- vxworks_rom.bin the RAM-based ROM image
- vxworks.st_rom.bin the standalone ROM image
- bootrom.bin the bootloader
- vxworks the downloadable VxWorks application

When the build is completed, the *target_image* is generated in the BSP directory.

Burning VxWorks into Flash Memory

Use the flash memory utility available in the Boot Monitor to burn-in the target image file onto the flash memory of the IXMB2400 Base Card. This image can be vxworks_rom.bin, vxworks.st_rom.bin, or bootrom.bin.

To burn an image into flash:

1. Build the image `vxworks_rom.bin`, `vxworks.st_rom.bin`, or `bootrom.bin`.

2. Boot the system with Boot Monitor with the serial port connected to a HyperTerminal session running on a Windows host. When the Redboot prompt appears, enter the following command and press Enter:

```
load -r -b 0x400000 -m y
```

3. Click the Send icon and a dialogue window appears.

4. Enter the file name (or use **Browse** to locate it) of the VxWorks image to be downloaded and select the Ymodem protocol.

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5. Click **Send** to transmit the file.

6. After the serial download is completed, use one of these commands to burn-in the vxworks image into flash:

a. If the image is vxworks_rom.bin:

```
fis create -b 0x400000 -l 0x100000 -e 0x1e018000 -r 0x1e010000 vxworks
```

or

b. If the image is vxworks.st_rom:

```
fis create -b 0x400000 -l 0x100000 -e 0x1f008000 -r 0x1f000000 vxworks
```

Loading VxWorks

1. After the flash memory programming is completed, load VxWorks:

```
fis load -w vxworks
```

2. If the image is `vxworks_rom.bin` or `vxworks.st_rom`, launch VxWorks with this command **`go`**

Using VxWorks

In the VxWorks configuration procedure that follows, the following assumptions are made:

- You have identified a system from which you can load a VxWorks image.
- You have installed the CPCI6240 BSP.
- Your host PC's COM port is connected to the CPCI-6240 System with a serial cable.
- You have installed Tornado* 2.2 with Intel® XScale™ core support on your host PC.

Using VxWorks as your development environment involves three general processes which are listed here and described in the following sections.

1. **Boot VxWorks on to the CPCI-6240 system**.
The VxWorks image is loaded into the CPCI-6240 System and system is rebooted. You can use the HyperTerminal* program as a status window. The Boot Monitor screen will display **WDB READY**. This indicates you are now ready to attach to the Tornado server.

2. **Configure the target server**.
The VxWorks Target server must be configured on the Host PC so that the Tornado* System can communicate over the serial connection. Use 115200 baud.

3. **Load the VxWorks application program**.
Load the VxWorks application program via the serial port.

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Appendix A Connector Pinouts

CompactPCI Connector Pinouts

CompactPCI J1

Row #	A	B	C	D	E	F
25	VCC	REQ64#	ENUM#	VCC3	VCC	GND
24	AD[1]	VCC	VIO	AD[0]	ACK64#	GND
23	VCC3	AD[4]	AD[3]	VCC	AD[2]	GND
22	AD[7]	GND	VCC3	AD[6]	AD[5]	GND
21	VCC3	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	AD[12]	GND	VIO	AD[11]	AD[10]	GND
19	VCC3	AD[15]	AD[14]	GND	AD[13]	GND
18	SERR#	GND	VCC3	PAR	C/BE[1]#	GND
17	VCC3	IPMB_CLK	IPMB_DAT	GND	PERR#	GND
16	DEVSEL#	PCIXCAP	VIO	STOP#	LOCK#	GND
15	VCC3	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
KEY						
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	AD[21]	GND	VCC3	AD[20]	AD[19]	GND
9	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	AD[26]	GND	VIO	AD[25]	AD[24]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	REQ0#	PCI_PRESENT#	VCC3	CLK	AD[31]	GND
5	BRSV	BRSV	RST#	GND	GNT0#	GND
4	IPMB_PWR	HLTY#	VIO	RSV	RSV	GND
3	PCIIRQ8#	PCIIRQ9#	PCIIRQ10#	VCC	PCIIRQ11#	GND
2	TCK	VCC	TMS	TDO	TDI	GND
1	VCC	-12V	TRST#	+12V	VCC	GND

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CompactPCI J2

Row #	A	B	C	D	E	F
22	GA4	GA3	GA2	GA1	GA0	GND
21	CLK6	GND	RSV	RSV	RSV	GND
20	CLK5	GND	RSV	GND	RSV	GND
19	RSV	GND	ICMB_SDA	ICMB_SCL	ICMB_ALERT#	GND
18	BRSV	BRSV	BRSV	GND	BRSV	GND
17	BRSV	GND	PRST#	REQ6#	GNT6#	GND
16	BRSV	BRSV	DEG#	GND	BRSV	GND
15	BRSV	GND	FAL#	REQ5#	GNT5#	GND
14	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	AD[38]	GND	VIO	AD[37]	AD[36]	GND
12	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	AD[45]	GND	VIO	AD[44]	AD[43]	GND
10	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	AD[52]	GND	VIO	AD[51]	AD[50]	GND
8	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	AD[59]	GND	VIO	AD[58]	AD[57]	GND
6	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	C/BE[5]#	GND	VIO	C/BE[4]#	PAR64	GND
4	VIO	BRSV	C/BE[7]#	GND	C/BE[6]#	GND
3	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

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CompactPCI J3

Row#	A	B	C	D	E	F
19	**GND**	**+12**	**GND**	**-12V**	**GND**	GND
18	LPa_DA0+	LPa_DA0-	**GND**	LPa_DC0+	LPa_DC0-	GND
17	LPa_DB0+	LPa_DB0-	**GND**	LPa_DD0+	LPa_DD0-	GND
16	LPb_DA1+	LPb_DA1-	**GND**	LPb_DC1+	LPb_DC1-	GND
15	LPb_DB1+	LPb_DB1-	**GND**	LPb_DD1+	LPb_DD1-	GND
14	**+3.3V**	**+3.3V**	**+3.3V**	**+5V**	**+5V**	GND
13	PMCIO5	PMCIO4	PMCIO3	PMCIO2	PMCIO1	GND
12	PMCIO10	PMCIO9	PMCIO8	PMCIO7	PMCIO6	GND
11	PMCIO15	PMCIO14	PMCIO13	PMCIO12	PMCIO11	GND
10	PMCIO20	PMCIO19	PMCIO18	PMCIO17	PMCIO16	GND
9	PMCIO25	PMCIO24	PMCIO23	PMCIO22	PMCIO21	GND
8	PMCIO30	PMCIO29	PMCIO28	PMCIO27	PMCIO26	GND
7	PMCIO35	PMCIO34	PMCIO33	PMCIO32	PMCIO31	GND
6	PMCIO40	PMCIO39	PMCIO38	PMCIO37	PMCIO36	GND
5	PMCIO45	PMCIO44	PMCIO43	PMCIO42	PMCIO41	GND
4	PMCIO50	PMCIO49	PMCIO48	PMCIO47	PMCIO46	GND
3	PMCIO55	PMCIO54	PMCIO53	PMCIO52	PMCIO51	GND
2	PMCIO60	PMCIO59	PMCIO58	PMCIO57	PMCIO56	GND
1	VIO	PMCIO64	PMCIO63	PMCIO62	PMCIO61	GND

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CompactPCI J5

Row#	A	B	C	D	E	F
22	GND	CLK0 GRX1	GND	GND	CLK1 GRX1	GND
21	GND	GND	GND	GND	GND	GND
20	GND			GMII1 RX1	GMII1 RX0	GND
19	GND	GMII1 RX5	GMII1 RX4	GMII1 RX3	GMII1 RX2	GND
18	GND	GMII1 RX9	GMII1 RX8	GMII1 RX7	GMII1 RX6	GND
17	GND	GMII1 TX8	GMII1 TX9	GMII1 CRS	GMII1 COL	GND
16	GND	GMII1 TX4	GMII1 TX5	GMII1 TX6	GMII1 TX7	GND
15	GND	GMII1 TX0	GMII1 TX1	GMII1 TX2	GMII1 TX3	GND
14	GND	GND	GND	GND	GND	GND
13	Serial RX	Serial TX		GND	CLK GTX1	GND
12	GND	GND	GND	GND	GND	GND
11	GND	CLK_GTX_0	GND	+5V	+5V	GND
10	GND	GND	GND	GMII0 TX9	GMII0 TX4	GND
9	GND	GMII0 TX3	GMII0 TX2	GMII0 TX1	GMII0 TX0	GND
8	GND	GMII0 TX8	GMII0 TX7	GMII0 TX6	GMII0 TX5	GND
7	GND	GMII0 RX1	GMII0 RX0	GMII0 COL	GMII0 CRS	GND
6	GND	GMII0 RX6	GMII0 RX5	GMII0 RX4	GMII0 RX3	GND
5	GND	GMII0 RX8	GMII0 RX2	GMII0 RX7	GMII0 RX9	GND
4	GND	GND	GND	GND	GND	GND
3	GND	CLK1 GRX0	GND	GND	CLK0 GRX0	GND
2	GND	GND	GND	+12V	GND	GND
1	+3.3V	+3.3V	+3.3V	SDA	SCK	GND

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PMC PrPMC J11 & J12

J11 pin assignment				J12 pin assignment			
Signal	**Pin**	**Pin**	**Signal**	**Signal**	**Pin**	**Pin**	**Signal**
TCK	1	2	-12V	+12V	1	2	TRST#
GND	3	4	PCIIRQ2#	TMS	3	4	RESERVED
PCIIRQ3#	5	6	PCIIRQ2#	TDI	5	6	GND
BUSMODE1#	7	8	+5V	GND	7	8	RESERVED
PCIIRQ3#	9	10	RESERVED	RESERVED	9	10	RESERVED
GND	11	12	+3.3V	BUSMODE2	11	12	+3.3V
CLOCK	13	14	GND	PCIREST#	13	14	BUSMODE3#
GND	15	16	GNT1#	+3.3V	15	16	BUSMODE4#
REQ1#	17	18	+5V	PME#	17	18	GND
PMCVIO	19	20	AD[31]	AD[30]	19	20	AD[29]
AD[28]	21	22	AD[27]	GND	21	22	AD[26]
AD[25]	23	24	GND	AD[24]	23	24	+3.3V
GND	25	26	C/BEJ[3]#	IDSEL_AD18	25	26	AD[23]
AD[22]	27	28	AD[21]	+3.3V	27	28	AD[20]
AD[19]	29	30	+5V	AD[18]	29	30	GND
PMCVIO	31	32	AD[17]	AD[16]	31	32	C/BEJ[2]#
FRAME#	33	34	GND	GND	33	34	RESERVED
GND	35	36	IRDY#	TRDY#	35	36	+3.3V
DEVSEL#	37	38	+5V	GND	37	38	STOP#
GND	39	40	LCOK#	PERR#	39	40	GND
RESERVED	41	42	RESERVED	+3.3V	41	42	SERR#
PAR	43	44	GND	C/BEJ1	43	44	GND
PMCVIO	45	46	AD[15]	AD[14]	45	46	AD13
AD[12]	47	48	AD[11]	M66EN	47	48	AD10
AD[9]	49	50	+5V	AD[8]	49	50	+3.3V
GND	51	52	C/BEJ[0]#	AD[7]	51	52	RESERVED
AD[6]	53	54	AD[5]	+3.3V	53	54	RESERVED
AD[4]	55	56	GND	RESERVED	55	56	GND
PMCVIO	57	58	AD[3]	RESERVED	57	58	RESERVED
AD[2]	59	60	AD[1]	GND	59	60	RESERVED
AD[0]	61	62	+5V	ACK64#	61	62	GND
GND	63	64	REQ64 #	GND	63	64	RESERVED

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PMC PrPMC J13 & J14

J13 pin assignment				J14 pin assignment			
Signal	**Pin**	**Pin**	**Signal**	**Signal**	**Pin**	**Pin**	**Signal**
RESERVED	1	2	GND	PMCIO01	1	2	PMCIO02
GND	3	4	C/BEJ[7]#	PMCIO03	3	4	PMCIO04
C/BEJ[6]#	5	6	C/BEJ[5]#	PMCIO05	5	6	PMCIO06
C/BEJ[4]#	7	8	GND	PMCIO07	7	8	PMCIO08
PMCVIO	9	10	PAR64	PMCIO09	9	10	PMCIO10
AD[63]	11	12	AD[62]	PMCIO11	11	12	PMCIO12
AD[61]	13	14	GND	PMCIO13	13	14	PMCIO14
GND	15	16	AD[60]	PMCIO15	15	16	PMCIO16
AD[59]	17	18	AD[58]	PMCIO17	17	18	PMCIO18
AD[57]	19	20	GND	PMCIO19	19	20	PMCIO20
PMCVIO	21	22	AD[56]	PMCIO21	21	22	PMCIO22
AD[55]	23	24	AD[54]	PMCIO23	23	24	PMCIO24
AD[53]	25	26	GND	PMCIO25	25	26	PMCIO26
GND	27	28	AD[52]	PMCIO27	27	28	PMCIO28
AD[51]	29	30	AD[50]	PMCIO29	29	30	PMCIO30
AD[49]	31	32	GND	PMCIO31	31	32	PMCIO32
GND	33	34	AD[48]	PMCIO33	33	34	PMCIO34
AD[47]	35	36	AD[46]	PMCIO35	35	36	PMCIO36
AD[45]	37	38	GND	PMCIO37	37	38	PMCIO38
PMCVIO	39	40	AD[44]	PMCIO39	39	40	PMCIO40
AD[43]	41	42	AD[42]	PMCIO41	41	42	PMCIO42
AD[41]	43	44	GND	PMCIO43	43	44	PMCIO44
GND	45	46	AD[40]	PMCIO45	45	46	PMCIO46
AD[39]	47	48	AD[38]	PMCIO47	47	48	PMCIO48
AD[37]	49	50	GND	PMCIO49	49	50	PMCIO50
GND	51	52	AD[36]	PMCIO51	51	52	PMCIO52
AD[35]	53	54	AD[34]	PMCIO53	53	54	PMCIO54
AD[33]	55	56	GND	PMCIO55	55	56	PMCIO56
PMCVIO	57	58	AD[32]	PMCIO57	57	58	PMCIO58
RESERVED	59	60	RESERVED	PMCIO59	59	60	PMCIO60
RESERVED	61	62	GND	PMCIO61	61	62	PMCIO62
GND	63	64	RESERVED	PMCIO63	63	64	PMCIO64

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PMC2 / PTMC Site

PMC PTMC J21 & J22

J21 pin assignment				J22 pin assignment			
Signal	**Pin**	**Pin**	**Signal**	**Signal**	**Pin**	**Pin**	**Signal**
TCK	1	2	-12V	+12V	1	2	TRST#
GND	3	4	PCIIRQ4#	TMS	3	4	RESERVED
PCIIRQ5#	5	6	PCIIRQ4#	TDI	5	6	GND
BUSMODE1#	7	8	+5V	GND	7	8	RESERVED
PCIIRQ5#	9	10	RESERVED	RESERVED	9	10	RESERVED
GND	11	12	+3.3V	BUSMODE2	11	12	+3.3V
CLOCK	13	14	GND	PCIREST#	13	14	BUSMODE3#
GND	15	16	GNT2#	+3.3V	15	16	BUSMODE4#
REQ2#	17	18	+5V	PME#	17	18	GND
PMCVIO	19	20	AD[31]	AD[30]	19	20	AD[29]
AD[28]	21	22	AD[27]	GND	21	22	AD[26]
AD[25]	23	24	GND	AD[24]	23	24	+3.3V
GND	25	26	C/BEJ[3]#	IDSEL_AD19	25	26	AD[23]
AD[22]	27	28	AD[21]	+3.3V	27	28	AD[20]
AD[19]	29	30	+5V	AD[18]	29	30	GND
PMCVIO	31	32	AD[17]	AD[16]	31	32	C/BEJ[2]#
FRAME#	33	34	GND	GND	33	34	RESERVED
GND	35	36	IRDY#	TRDY#	35	36	+3.3V
DEVSEL#	37	38	+5V	GND	37	38	STOP#
GND	39	40	LCOK#	PERR#	39	40	GND
RESERVED	41	42	RESERVED	+3.3V	41	42	SERR#
PAR	43	44	GND	C/BEJ1	43	44	GND
PMCVIO	45	46	AD[15]	AD[14]	45	46	AD13
AD[12]	47	48	AD[11]	M66EN	47	48	AD10
AD[9]	49	50	+5V	AD[8]	49	50	+3.3V
GND	51	52	C/BEJ[0]#	AD[7]	51	52	RESERVED
AD[6]	53	54	AD[5]	+3.3V	53	54	RESERVED
AD[4]	55	56	GND	RESERVED	55	56	GND
PMCVIO	57	58	AD[3]	RESERVED	57	58	RESERVED
AD[2]	59	60	AD[1]	GND	59	60	RESERVED
AD[0]	61	62	+5V	ACK64#	61	62	GND
GND	63	64	REQ64 #	GND	63	64	RESERVED

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PTMC J23 & J24

J23 pin assignment				J24 pin assignment			
Signal	**Pin**	**Pin**	**Signal**	**Signal**	**Pin**	**Pin**	**Signal**
TXSOC	1	2	GND		1	2	GND
GND	3	4		GND	3	4	
	5	6			5	6	
RXADR3	7	8	GND		7	8	
PTID2	9	10	PTGNDZ		9	10	
PTGNDZ	11	12			11	12	
	13	14	GND		13	14	GND
GND	15	16	RXENB#	GND	15	16	REOP
TXADR3	17	18		TEOP	17	18	RMOD
TXADR2	19	20	GND	TMOD	19	20	GND
PTID0	21	22	TXENB#	GND	21	22	RERR
PTGNDZ	23	24	RXADR2	TERR	23	24	RXCLAV3
TXCLK	25	26	GND	TXCLAV3	25	26	GND
GND	27	28	TXADR1	GND	27	28	RXCLAV2
TXADR0	29	30	RXADR1	TXCLAV2	29	30	RXCLAV1
TXPRTY	31	32	GND	TXCLAV1	31	32	GND
GND	33	34	RXADR0	GND	33	34	RVAL
TXD7	35	36	RXPRTY	PTPA	35	36	PRPA
TXD6	37	38	GND	STPA	37	38	GND
PTENB#	39	40	RXD7	GND	39	40	RXD15
PTGNDZ	41	42	RXD6	TXD15	41	42	RXD14
RXCLK	43	44	GND	TXD14	43	44	GND
GND	45	46	RXD5	GND	45	46	RXD13
TXD5	47	48	RXD4	TXD13	47	48	RXD12
TXD4	49	50	GND	TXD12	49	50	GND
GND	51	52	RXD3	GND	51	52	RXD11
TXD3	53	54	RXD2	TXD11	53	54	RXD10
TXD2	55	56	GND	TXD10	55	56	GND
PTID1	57	58	RXD1	GND	57	58	RXD9
TXD1	59	60	RXD0	TXD9	59	60	RXD8
TXD0	61	62	GND	TXD8	61	62	GND
GND	63	64	RxSOC	GND	63	64	

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DDR SODOMM Connector

Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
1	VREF	2	VREF	101	A9	102	A8
3	VSS	4	VSS	103	VSS	104	VSS
5	DQ0	6	DQ4	105	A7	106	A6
7	DQ1	8	DQ5	107	A5	108	A4
9	VDD	10	VDD	109	A3	110	A2
11	DQS0	12	DM0	111	A1	112	A0
13	DQ2	14	DQ6	113	VDD	114	VDD
15	VSS	16	VSS	115	A10/AP	116	BA1
17	DQ3	18	DQ7	117	BA0	118	RAS
19	DQ8	20	DQ12	119	WE	120	CAS
21	VDD	22	VDD	121	S0	122	S1
23	DQ9	24	DQ13	123	NC(A13)	124	NC
25	DQS1	26	DM1	125	VSS	126	VSS
27	VSS	28	VSS	127	DQ32	128	DQ36
29	DQ10	30	DQ14	129	DQ33	130	DQ37
31	DQ11	32	DQ15	131	VDD	132	VDD
33	VDD	34	VDD	133	DQS4	134	DM4
35	CK0	36	VDD	135	DQ34	136	DQ38
37	CK0	38	VSS	137	VSS	138	VSS
39	VSS	40	VSS	139	DQ35	140	DQ39
41	DQ16	42	DQ20	141	DQ40	142	DQ44
43	DQ17	44	DQ21	143	VDD	144	VDD
45	VDD	46	VDD	145	DQ41	146	DQ45
47	DQS2	48	DM2	147	DQS5	148	DM5
49	DQ18	50	DQ22	149	VSS	150	VSS
51	VSS	52	VSS	151	DQ42	152	DQ46
53	DQ19	54	DQ23	153	DQ43	154	DQ47
55	DQ24	56	DQ28	155	VDD	156	VDD
57	VDD	58	VDD	157	VDD	158	CK1
59	DQ25	60	DQ29	159	VSS	160	CK1
61	DQS3	62	DM3	161	VSS	162	VSS
63	VSS	64	VSS	163	DQ48	164	DQ52
65	DQ26	66	DQ30	165	DQ49	166	DQ53
67	DQ27	68	DQ31	167	VDD	168	VDD
69	VDD	70	VDD	169	DQS6	170	DM6
71	CB0	72	CB4	171	DQ50	172	DQ54
73	CB1	74	CB5	173	VSS	174	VSS
75	VSS	76	VSS	175	DQ51	176	DQ55
77	DQS8	78	DM8	177	DQ56	178	DQ60
79	CB2	80	CB6	179	VDD	180	VDD
81	VDD	82	VDD	181	DQ57	182	DQ61
83	CB3	84	CB7	183	DQS7	184	DM7
85	NC	86	(RESET)	185	VSS	186	VSS
87	VSS	88	VSS	187	DQ58	188	DQ62
89	CK2	90	VSS	189	DQ59	190	DQ63
91	CK2	92	VDD	191	VDD	192	VDD
93	VDD	94	VDD	193	SDA	194	SA0
95	CKE1	96	CKE0	195	SCL	196	SA1
97	NC	98	NC	197	VDDSPD	198	SA2
99	A12	100	A11	199	VDDID	200	NC

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IXP2400 JTAG Debug Connector

Pin	Signal	Pin	Signal
1	+3.3V	2	+3.3V
3	IXP2400 TRST#	4	GND
5	IXP2400 TDI	6	GND
7	IXP2400 TMS	8	GND
9	IXP2400 TCK	10	GND
11	GND	12	GND
13	IXP2400 TDO	14	GND
15	RESET	16	GND
17	N/C	18	GND
19	N/C	20	GND

Zircon JTAG Debug Connector

Pin	Signal	Pin	Signal
1	IPMI +3.3V	2	IPMI +3.3V
3	ZIRCON TRST#	4	GND
5	ZIRCON TDI	6	GND
7	ZIRCON TMS	8	GND
9	ZIRCON TCK	10	GND
11	GND	12	GND
13	ZIRCON TDO	14	GND
15	ZIRCON RESET	16	GND
17	N/C	18	GND
19	N/C	20	GND

Front Panel Connectors

RJ11 Serial Port Connector J15

Pin#	Signal
1	Chassis Ground
2	RS232 TX
3	RS232 RX
4	Ground
5	Ground
6	Ground

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RJ45 Gigabit Ethernet Port 1, CN3

Pin#	Signal
1	Data A +
2	Data A -
3	Data B +
4	Data B -
5	Data C +
6	Data C -
7	Data D +
8	Data D -

RJ45 Gigabit Ethernet Port 2, CN4

Pin#	Signal
1	Data A +
2	Data A -
3	Data B +
4	Data B -
5	Data C +
6	Data C -
7	Data D +
8	Data D -

End Of Document

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