cPCI-6530BL Series

Performance 6U CompactPCI®
Intel® Core™ i7/i5 Processor Blade

User's Manual



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Revision History

Revision	Release Date	Description of Change(s)
1.0	July 12, 2018	Initial release

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Preface

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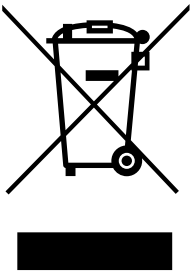
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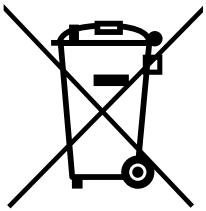
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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

NOTE: Additional information, aids, and tips that help users perform tasks.

CAUTION: Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

WARNING: Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

1.1 Overview

The ADLINK cPCI-6530BL Series is a 6U CompactPCI® processor blade with soldered DDR3L-1600 ECC memory up to 16GB and DDR3L-1600 ECC socket type memory up to 16GB. The ADLINK cPCI-6530BL features an Intel® Core™ i7/i5 processor with Mobile Intel® QM87 Express Chipset.

The cPCI-6530BL Series is a 6U CompactPCI blade in single-slot (4HP) width form factor. Front panel I/O for the cPCI-6530BLV includes 1x DVI-I, 2x GbE and 2x USB 3.0 ports, 1x USB 2.0 port, 1x RJ-45 COM port and 1x PCI/XMC slot. The cPCI-6530BL front panel includes 2x GbE and 1x USB 3.0 port and 1x USB 2.0 port and 2x PMC/XMC slots.

Graphics support is integrated on the CPU and supports 3 independent displays when mated with selected rear transition modules (cPCI-R6700 and cPCI-R6500). Storage for both cPCI-6530BLV and cPCI-6530BL versions includes an mSATA slot and a SATA 7-pin connector. The cPCI-6530BLV supports an additional SATA connector to support onboard 2.5" SATA drive or CFast adapter.

For expansion, both cPCI-6530BL and cPCI-6530BLV are equipped with one 64-bit/33, 66,133MHz PMC site or one PCIe x8 Gen 2 XMC site with rear I/O. The cPCI-6530BL is equipped with one additional PMC/XMC slot supporting PCI 64-bit/33,66,133MHz PMC site or one PCIe x8 Gen 2 XMC site.

Rear I/O signals to RTM include 2x GbE by Intel I210 LAN controllers, 1x DVI-I, 1x PCIe x4 (configurable to 4x PCIe x1), 3x SATA 3 Gb/s, and 6x USB 2.0., 5x GPIO, high definition audio, KB/MS, and 2x serial ports (one supports Tx/Rx only). The PMC/XMC signals on the cPCI-6530BL can also be routed to RTM.

The cPCI-6530BL Series offers outstanding performance provided by 5th generation Intel® Core™ processor family, and is an ideal solution for military, aerospace, transportation and other industrial applications that require best value per watt computing power. The ADLINK cPCI-6530BL Series provides higher flexibility, supporting operation in peripheral slots with CompactPCI bus communication

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(Universal mode) and as a standalone computer if there is no CPU blade in the host slot. Internet remote manageability includes IPMI for system health monitoring over Internet and a GbE port on the faceplate supports Intel® AMT 9.0 for remote monitoring.

1.2 Features

- 6U CompactPCI blade in 4HP width form factor
- Intel® Core™ i7-5850EQ Processor (4 cores, 8 threads, 6M cache, 2.7/3.4 GHz) and Mobile Intel® QM87 Express Chipset
- Graphics and memory controllers integrated in processor
- One channel DDR3L soldered onboard memory with ECC up to 16GB and one channel DDR3L ECC socket memory up to 16GB (total 32GB). When equipped with 8GB onboard memory, the frequency is 1600MHz; when equipped with 16GB onboard memory, the frequency is reduced to 1067MHz.
- 64bit/66MHz CompactPCI Interface based on PCI specifications, universal V(I/O)
- Supports Universal mode operation as a slave in peripheral slots and operation as a standalone computer if no CPU blade in host slot
- One 64-bit/33,66,133MHz PMC or PCIe x8 Gen2 XMC site on cPCI-6530BLV with rear I/O; one additional PMC/XMC site on cPCI-6530BL
- Supports IPMI over LAN for system health monitoring
- DVI-I port on front panel, additional DVI-I and eDP routed to rear
- Two PCIe Gigabit Ethernet egress ports supported by Intel LAN controller on front panel, one supports Intel® AMT 9.0 by Intel® Ethernet Controller I210 (PHY)
- Two additional PCIe Gigabit Ethernet by Intel® Ethernet Controller I210 routed to J2 (PICMG 2.16 compliant)
- Additional two Gigabit Ethernet ports with selected rear transition module (cPCI-R6100 Series)
- High definition audio routed to RTM
- Onboard mSATA for SATA interface storage
- Optional onboard 2.5" SATA SSD or CFast storage on cPCI-6530BLV
- Optional Atmel AT97SC3204 TPM support

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1.3 Package Contents

The cPCI-6530BL is packaged with the following components. If any of the following items are missing or damaged, retain the shipping carton and packing material and contact the dealer for inspection. Please obtain authorization before returning any product to ADLINK. The packing contents of cPCI-6530BL Series non-standard configurations will vary depending on customer requests.

CPU module

- The cPCI-6530BL Series Processor Blade
  - CPU and memory specifications will differ depending on options selected
  - Thermal module is assembled on the board
- RJ-45 to DB-9 COM adapter cable (cPCI-6530BLV)
- 2.5” SATA drive accessory pack (cPCI-6530BLV)
- mSATA accessory pack

Rear Transition Module

- Dependent on the module selected

Optional Accessories

- DB-CFAST adapter board for CFast card assembly (Part No. 91-37572-010E)



The contents of non-standard cPCI-6530BL configurations may vary depending on the customer’s requirements.



This product must be protected from static discharge and physical shock. Never remove any of the components except at a static-free workstation. Use the anti-static bag shipped with the product when putting the board on a surface. Wear an anti-static wrist strap properly grounded on one of the system's ESD ground jacks when installing or servicing system components.

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2 Specifications

2.1 cPCI-6530BL Processor Blade Specifications

CompactPCI® Standards	• PICMG® 2.0 CompactPCI® Rev. 3.0 • PICMG® 2.1 Hot Swap Specification Rev. 2.0 • PICMG® 2.9 System Management Rev. 1.0 • PICMG® 2.16 Packet Switching Backplane Rev. 1.0
Mechanical	• Standard 6U CompactPCI® • Board size: 233mm x 160mm • Single slot (4HP, 20.32mm) • CompactPCI® connectors: J1, J2, J3, J4, J5
Processor	• uFC-BGA quad-core Intel® Core™ i7-5850EQ processor, 2.7/3.4GHz, 6MB L3 cache, 47/37W by cTDP, Intel® Iris Pro Graphics 6200 • uFC-BGA quad-core Intel® Core™ i7-5700EQ processor, 2.6/3.4GHz, 6MB L3 cache, 47/37W by cTDP • Passive heatsink
Chipset	• Mobile Intel® QM87 Express Chipset
Memory	• Dual channel DDR3L ECC memory, max. support 32GB • One channel DDR3L soldered onboard memory with ECC up to 16GB • One channel DDR3L ECC socket memory up to 16GB • When equipped with 8GB onboard memory, the frequency is 1600MHz; when equipped with 16GB onboard memory, the frequency is reduced to 1067MHz
CompactPCI Bus	• PCI 64-bit/66MHz; 3.3V, 5V universal V I/O • Supports operation in system slot as master or in peripheral slot with connectivity to CompactPCI bus (Universal mode) • Supports operation in peripheral slot as standalone CPU board when no host blade in host slot
Gigabit Ethernet	• One PCIe x1 Intel® I217 GbE PHY and three PCIe x1 Intel® I210 Gigabit Ethernet controllers • Two egress 10/100/1000BASE-T ports on front panel, one supporting Intel® AMT 9.0 by I217 controller • Two egress 10/100/1000BASE-T ports routed to rear transition module

Table 2-1: cPCI-6530BL Processor Blade Specifications

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Graphics	• Intel® Core™ i7-5850EQ: Intel® Iris Pro Graphics 6200 • Intel® Core™ i7-5700EQ: Intel® HD Graphics 4600 • One DVI-I port on front panel, one DVI, eDP routed to J3 & J5 (RTM) • Up to three independent display with selected rear transition module (cPCI-R6700 & cPCI-R6500)
Serial Ports	• Up to three serial ports • One RS-232/422/485 serial port on front panel (cPCI-6530BLV) • Up to two RS-232 COM port routed to RTM
USB 2.0	• One USB 2.0 port on front panel • Up to six USB 2.0 ports routed to rear transition module
USB 3.0	• One USB 3.0 for cPCI-6530BL version, additional one USB 3.0 for cPCI-6530BLV version
PMC/XMC	• One 64-bit/33,66,133 MHz PMC site or PCIe x8 Gen 2 XMC site for cPCI-6530BLV version with rear I/O • Two 64-bit/33,66,133 MHz PMC sites or PCIe x8 Gen 2 XMC sites on cPCI-6530BL version
Audio	• High definition audio routed to rear
TPM	Atmel AT97SC3204 TPM (upon request) supporting: • Over/Under voltage detection • Low/High frequency sensor/filter • Reset filter • Memory encryption/decryption
Storage Interfaces[1]	• One mSATA slot • One onboard 2.5” SATA connector supporting SATA 6Gb/s drive on cPCI-6530BLV • Optional CFast socket by adapter board on cPCI-6530BL (space shared with 2.5” SATA drive) • One SATA 7-pin 3Gb/s connector onboard • Three SATA 3Gb/s channels routed to RTM
BIOS	• AMI® EFI BIOS, 64Mbit SPI flash memory, supports Configurable TDP (can be set as Nominal and Down)

Table 2-1: cPCI-6530BL Processor Blade Specifications

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Faceplate I/O	cPCI-6530BLV (4HP) • 2x 10/100/1000BASE-T Ethernet ports • 1x DVI-I port • 2x USB 3.0 ports • 1x USB 2.0 port • 1x RJ-45 serial port • 1x PMC/XMC slot cPCI-6530BL (4HP) • 2x 10/100/1000BASE-T Ethernet ports • 1x USB 3.0 ports • 1x USB 2.0 port • 2x PMC/XMC slots
OS Compatibility	• Microsoft Windows 7 32/64-bit • Microsoft Windows 8 32/64-bit • Red Hat Enterprise Linux 6.4, 64-bit • Fedora 14, 32-bit • VxWorks 6.9 • Other OS support upon request
Environmental	• Operating Temperature (with forced air flow)[2]: Standard: -20°C to +70°C Extreme temperature: -40°C to +85°C (for Intel® Core™ 5850EQ and Core™ i7-5700EQ processor with cTDP down to 37W and forced air flow) • Storage Temperature: -50°C to 100°C • Humidity: 95% @60°C non-condensing • Shock: 20G peak-to-peak, 11ms duration, non-operating • Vibration[3]: 2Grms, 5-500Hz, each axis, operating (w/o hard drive)
EMI	• CE EN55022 • FCC Class A

Table 2-1: cPCI-6530BL Processor Blade Specifications

1. The storage device limits the operational vibration tolerance. When the application requires higher specification for anti-vibration, it is recommended to use a flash storage device.
2. ADLINK-certified thermal design. The thermal performance is dependent on the chassis cooling design. Sufficient forced air-flow is required. Temperature limits of optional mass storage devices may also affect the thermal specification.

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2.2 Block Diagrams

cPCI-6530BL Blade

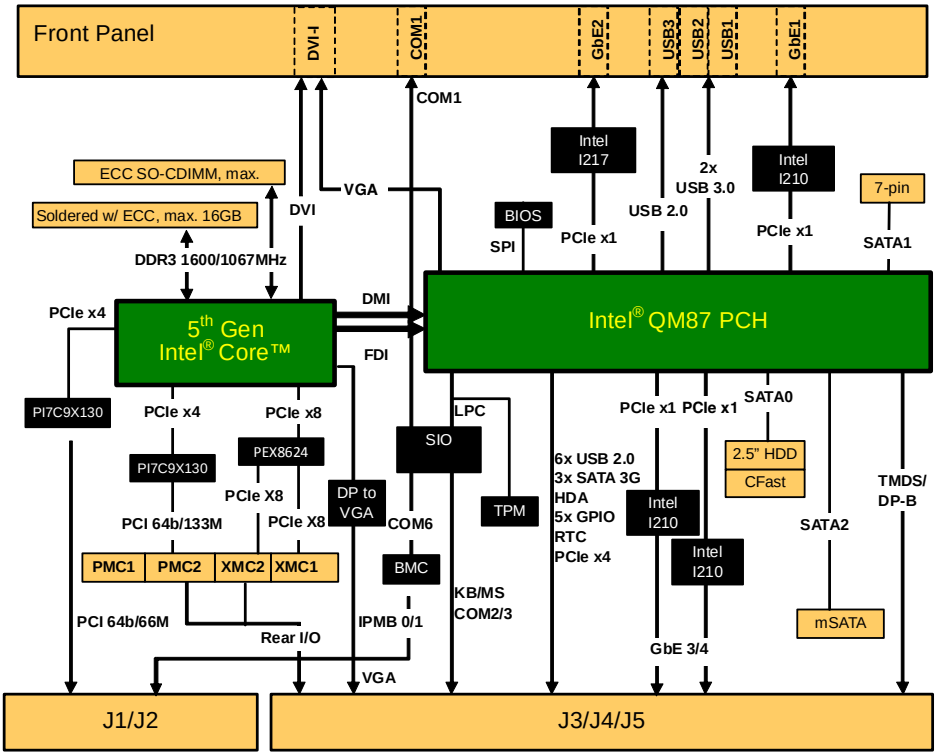


Figure 2-1: cPCI-6530BL Blade Functional Block Diagram

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2.3 I/O Connectivity Table

Function	cPCI-6530BLV (4HP)		cPCI-6530BL (4HP)	
	Faceplate	Onboard	Faceplate	Onboard
Gigabit Ethernet	Y x2	–	Y x2	–
COM	Y (RJ-45)	–	–	–
USB 3.0	Y x2	–	Y x1	–
USB 2.0	Y x1	–	Y x1	–
DVI-I	Y	–	–	–
Serial ATA	–	Y x2 (one for 2.5” drive & one 7-pin SATA connector)	–	Y x1 (7-pin SATA connector)
CFast	–	Y (space shared with 2.5” SATA drive)	–	–
mSATA	–	Y x1	–	Y x1
PMC/XMC	–	Y x1	–	Y x2
LED	Y x5	–	Y x5	–
Reset Button	Y	–	Y	–

Table 2-2: cPCI-6530BL I/O Connectivity

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2.4 Power Requirements

In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. **An industrial power supply unit should be able to provide at least twice as much power as the entire system requires of each voltage**. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires of each voltage.

The tolerance of the voltage lines described in the CompactPCI specification (PICMG 2.0 R3.0) is +5%/-3% for 5, 3.3 V and ±5% for ±12V. This specification is for power delivered to each slot and it includes both the power supply and the backplane tolerance.

Voltage	Nominal Value	Tolerance	Max. Ripple (P - P)
5V	+5.0 VDC	+5% / -3%	50 mV
3.3V	+3.3 VDC	+5% / -3%	50 mV
+12V	+12 VDC	+5% / -5%	240 mV
-12V	-12 VDC	+5% / -5%	240 mV
V I/O (PCI I/O Buffer Voltage)	+3.3 VDC or +5 VDC	+5% / -3%	50 mV
GND			

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Power Consumption

This section provides information on the power consumption of cPCI-6530BL Series when using the Intel® Core™ i7 processors with 8GB DDR3L-1600 ECC soldered memory and 8GB DDR3L-1600 socket memory module. Storage device is used with ADLINK ASD26-MLC32G-CT 32GB SATA SSD. The cPCI-6530BL is powered by 5V and 3.3V. Power consumption at 100% CPU stress was measured using the Intel Thermal Analysis Tool 4.3 (TAT).

Intel® Core™i7-5850EQ (BIOS EIST enabled, cTDP nominal)			
OS/Mode	**Current 5V**	**Current 3.3V**	**Total Power**
Windows 7, Idle mode	4.82 A	2.48 A	32.28 W
Windows 7, CPU 100% stress	12.87 A	2.65 A	73.06 W
Windows 7, BurnIn Test system stress	13.14 A	2.58 A	74.21 W

Intel® Core™i7-5700EQ (BIOS EIST enabled, cTDP nominal)			
OS/Mode	**Current 5V**	**Current 3.3V**	**Total Power**
Windows 7, Idle mode	4.59 A	2.38 A	30.80 W
Windows 7, CPU 100% stress	11.40 A	2.43 A	65.02 W
Windows 7, BurnIn Test system stress	12.10 A	2.41 A	68.45 W

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3 Functional Description

The following sections describe the cPCI-6530BL Series features and functions.

3.1 Processors

The Mobile 5th Generation Intel® Core™ Processor Family are state of the art, 64-bit, multi-core mobile processor built on 22 nanometer process technology. Based on a new micro-architecture, the processor is designed for a two-chip platform. The two-chip platform consists of a processor and Platform Controller Hub (PCH). The platform enables higher performance, lower cost, easier validation, and improved x-y footprint. The processor includes an Integrated Display Engine, Processor Graphics and Integrated Memory Controller.

The cPCI-6530BL Series supports Intel® Core™ i7/i5 processors. The table below lists the general specifications and power ratings of the CPUs supported by the cPCI-6530BL Series.

Features	Core™ i7-5850EQ	Core™ i5-5700EQ
Clock	2.7 GHz	2.6 GHz
Max. Single Core Turbo Freq.	3.4 GHz	3.4 GHz
Last Level Cache	6MB SmartCache	6MB SmartCache
No. of Core(s)	4	4
Max. Power (TDP[1])	47/37W adjusted by cTDP	47/37W adjustable by cTDP
DMI	5 GT/s DMI	5 GT/s DMI
$T_{junction, MAX}$[2]	105C	105C

1. The highest expected sustainable power while running known power intensive applications. TDP is not the maximum power that the processor can dissipate.
2. The maximum supported operating temperature.

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Supported Technologies

Features	Core™ i7-5850EQ	Core™ i5-5700EQ
Intel® Virtualization Technology for Directed I/O (Intel® VT-d)	Yes	Yes
Intel® Virtualization Technology (Intel® VT-x)	Yes	Yes
Intel® VT-x with Extended Page Tables (EPT)	Yes	Yes
Intel® Hyper-Threading Technology	Yes	Yes
Intel® 64 Architecture	Yes	Yes
Execute Disable Bit	Yes	Yes
Intel® Turbo Boost Technology	2.0	2.0
Intel® vPro Technology	Yes	Yes
Enhanced Intel SpeedStep® Technology	Yes	Yes
Thermal Monitoring Technologies	Yes	Yes
Intel® Identity Protection Technology	Yes	Yes

Interfaces

- Two channels of DDR3L-1600 memory
- DDR3 memory data transfer rate of 1600 MT/s
- 64-bit wide channels
- DDR3L I/O voltage of 1.35V
- 4Gb and 8Gb DDR3 DRAM technologies are supported for x8 and x16 devices (using 8Gb device technologies, the largest memory capacity possible is 16GB, assuming dual-channel mode with x8, dual-ranked ECC SDRAM; frequency is reduced to 1067MHz when equipped with 16GB onboard soldered memory)
- PCI Express ports are fully-compliant with the PCI Express Base Specification, Revision 2.0.
- 5 GT/s point-to-point DMI interface to PCH is supported

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Graphics

The Intel® Graphics Engine is integrated in the processor enabling substantial gains in performance and lower power consumption.

- Intel® Core™ i7-5850EQ: Intel® Iris Pro Graphics 6200
- Intel® Core™ i7-5700EQ: Intel® HD Graphics 4600
- DX11.2 support
- OpenGL 4.3 support
- Graphics Base Frequency: 400 MHz
- Graphics Max Dynamic Frequency: 1 GHz
- Supports Intel® InTru™ 3D Technology
- FDI carries display traffic from the Processor Graphics in the processor to the legacy display connectors in the PCH

3.2 Chipset

The Mobile Intel® QM87 Express Chipset provides extensive I/O support. Functions and capabilities include:

- The QM87 PCH provides extensive I/O support, functions and capabilities including:
- PCI Express Base Specification, Revision 2.0 support for up to eight ports with transfers up to 5 GT/s
- ACPI Power Management Logic Support, Revision 4.0a
- Enhanced DMA controller, interrupt controller, and timer functions
- Integrated Serial ATA host controllers with independent DMA operation on up to six ports
- USB host interface with two EHCI high-speed USB 2.0 Host controllers and two rate matching hubs provide support for up to fourteen USB 2.0 ports
- Integrated 10/100/1000 Gigabit Ethernet MAC with System Defense
- System Management Bus (SMBus) Specification, Version 2.0 with additional support for I2C devices
- Supports Intel® High Definition Audio

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- Supports Intel® Rapid Storage Technology
- Supports Intel® Virtualization Technology for Directed I/O
- Integrated Clock Controller
- Analog and Digital Display ports
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support
- Serial Peripheral Interface (SPI) support

3.3 PMC/XMC

The cPCI-6530BL(V) models support max two PMC or XMC sites for front panel I/O expansion. The PMC site provides a maximum 64-bit/33,66,133 MHz PCI bus link using a Pericom PI7C9X130 PCI-Express-to-PCI bridge and PCI-Express x4 link. The PMC sites support +3.3V signaling only. The XMC sites provide PCI-Express x8 lanes which are supported by a PCIe x8 Switch.

3.4 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology is a feature that allows the processor to opportunistically and automatically run faster than its rated operating core and/or render clock frequency when there is sufficient power headroom, and the product is within specified temperature and current limits. The Intel Turbo Boost Technology feature is designed to increase performance of both multi-threaded and single-threaded workloads. The processor supports a Turbo mode where the processor can use the thermal capacity associated with package and **run at power levels higher than TDP power for short durations**. This improves the system responsiveness for short, bursty usage conditions.

Turbo Mode availability is independent of the number of active cores; however, the Turbo Mode frequency is dynamic and dependent on the instantaneous application power load, the number of active cores, user configurable settings, operating environment, and system design. If the power, current, or thermal limit is reached, the processor will automatically reduce the frequency to stay with its TDP limit.

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3.5 Intel® Hyper-Threading Technology

Intel® Hyper-Threading Technology allows an execution core to function as two logical processors. While some execution resources (such as caches, execution units, and buses) are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled using the BIOS and requires operating system support. Intel recommends enabling Hyper-Threading Technology with Microsoft Windows 7, and disabling Hyper-Threading Technology using the BIOS for all previous versions of Windows operating systems.

3.6 Trusted Platform Module

The cPCI-6530BL integrates an Atmel AT97SC3204 Trusted Platform Module (TPM). The TPM is a secure controller with added cryptographic functionality to provide users a secure environment in e-commerce transactions and Internet communications.

The key features Trusted Platform Module (TPM) offers are:

- Fully compliant to the Trusted Computing Group (TCG) Trusted Platform Module (TPM) version 1.2 specification
- Hardware hash accelerator for SHA-1 algorithm
- Advanced Crypto Engine (ACE) for asymmetric key operations(up to 2048-bit key length) to make hardware protection.
- Tick counter to extend the time required to decipher the key
- In addition to encryption key created by user. it also provide some security features to protect the integrated circuit itself:
- Over/Under-voltage detection to monitor the system stability. If the voltage fluctuates dramatically, this function can block the data transfer and lock the chip.
- Low/High frequency sensor to detect the IC clock frequency. If the frequency fluctuates dramatically, this function can block the data transfer and lock the chip.
- Reset filter to filter reset signal in order to break the time set by tick counter is received
- Memory encryption to protect memory

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- Physical shield in the IC to protect the die from intruding or hacking by matching the data transferred on the 2 layer metal shield on the IC. If the data is not matched, the IC may be blocked.

3.7 Battery

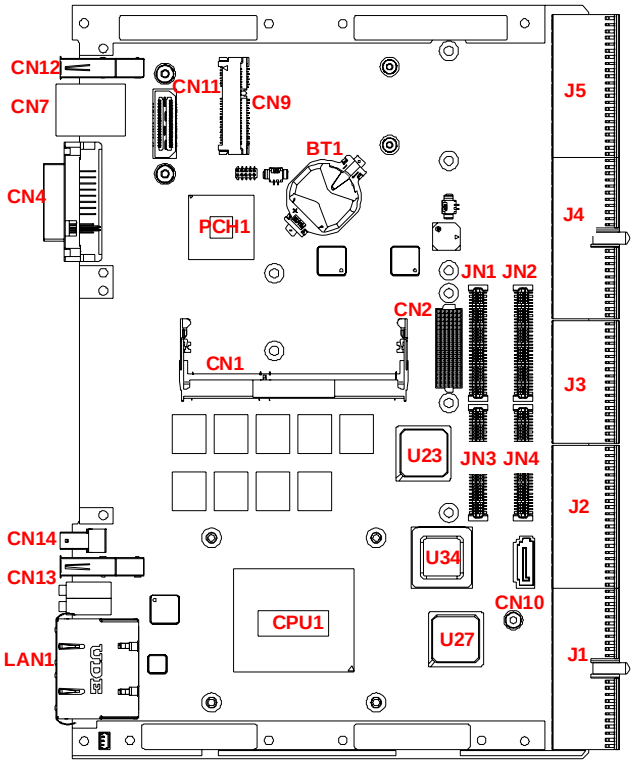
The cPCI-6530BL is equipped with a 3.0V "coin cell" lithium battery for the Real Time Clock (RTC). The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. A Rayovac BR2032 is equipped on board by default.

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4 Board Interfaces

This chapter illustrates the board layout, connector pin assignments, and jumper settings to familiarize users with the cPCI-6530BL Series.

4.1 cPCI-6530BLV Board Layout

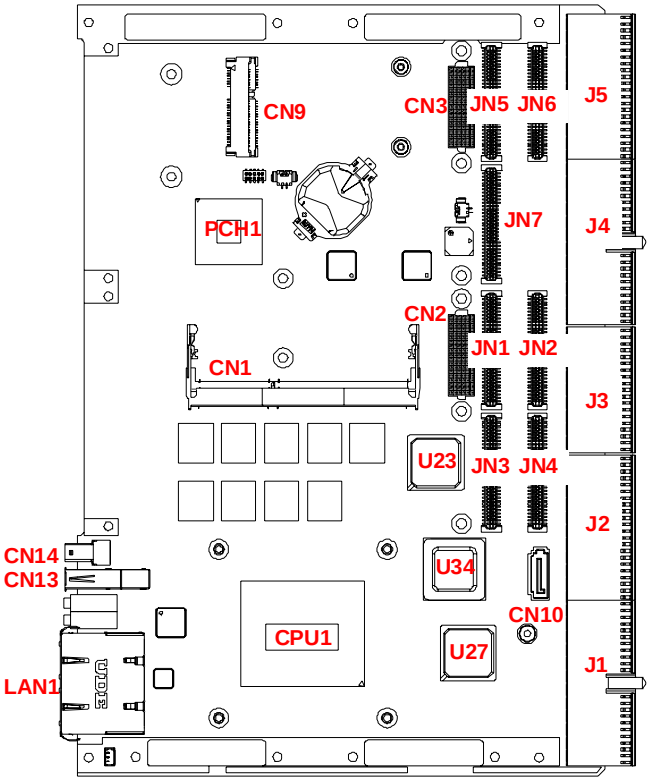


CPU	Intel® Core™ Processor	**J1-J5**	CompactPCI connectors
PCH1	Intel® QM87 PCH	**LAN1**	Dual Ethernet connectors
CN1	Memory socket	**CN9**	mSATA connector
CN2	XMC connector	**CN10**	SATA 7-pin connector
CN4	DVI-I connector	**CN11**	SATA board-to-board conn.
CN7	COM port in RJ-45 conn.	**CN12/13**	USB 3.0 connector
BT1	Battery socket	**CN14**	USB 2.0 connector
U34	PCe Switch PEX8624-BB50BI	**JN1/2/3/4**	PMC connectors
U23/27	Pericom PI7C9X130	**U23/27**	Pericom PI7C9X130

Figure 4-1: cPCI-6530BLV Series Board Layout

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4.2 cPCI-6530BL Board Layout



CPU	Intel® Core™ Processor	**J1-J5**	CompactPCI connectors
PCH1	Intel® QM87 PCH	**LAN1**	Dual Ethernet connectors
CN1	Memory socket	**CN9**	mSATA connector
CN2/3	XMC connectors	**CN10**	SATA 7-pin connector
CN13	USB 3.0 connector	**U34**	PCe Switch PEX8624-BB50BI
CN14	USB 2.0 connector	**U23/27**	Pericom PI7C9X130
BT1	Battery socket	**JN1~7**	PMC connectors

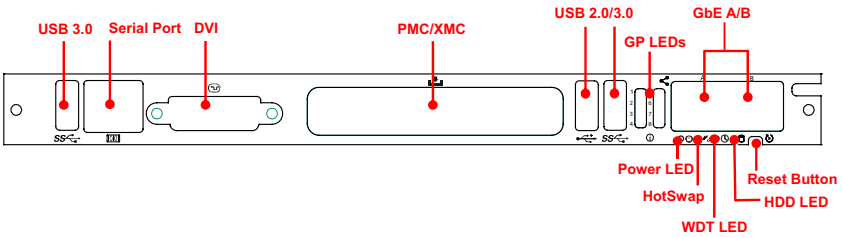
Figure 4-2: cPCI-6530BL Series Board Layout

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4.3 cPCI-6530BL Series Front Panel

Front Panel Layout

cPCI-6530BLV



cPCI-6530BL

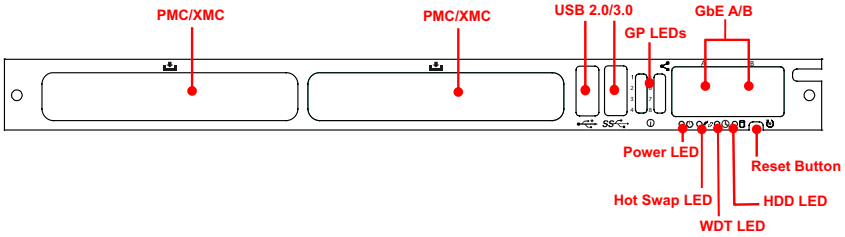


Figure 4-3: cPCI-6530BL Series Front Panel Layout

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System LEDs

LED	Color	Condition	Indication
Power 	Green/ Red	OFF	System is off
		Red	System Power ready (PWGD)
		Green	Post OK
WDT 	Orange	OFF	No Watchdog event
		Blinking	Watchdog event alert
HDD 	Blue	OFF	No CF/CFast/SATA HDD activity
		Blinking	Data read/write in process for CF/CFast/ SATA HDD
Hot Swap 	Blue	Off	Handles closed, system is on
		Fast Blink	Preparing to shut down system (LED: 0.1s on, 0.9s off.)
		On	Handles open and blade ready to be removed
		Slow Blink	Voltages out of tolerance: 3.3V, 5V, 12V, 1.5V over ±5% (LED: 2s on, 1s off)

Table 4-1: cPCI-6530BL Front Panel System LED Descriptions

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General Purpose LEDs

The eight GP LEDs on the front panel display port 80h POST codes in hexadecimal during boot up. Users can use the POST codes to identify issues during the BIOS POST process. For example, if the Bit7 > Bit0 output is “01110101”, then the port 80h output is “75h” (See “Checkpoints & Beep Codes” on page 107).

Each LED indicates a corresponding bit of the port 80h POST code. Refer to the figure and table below.

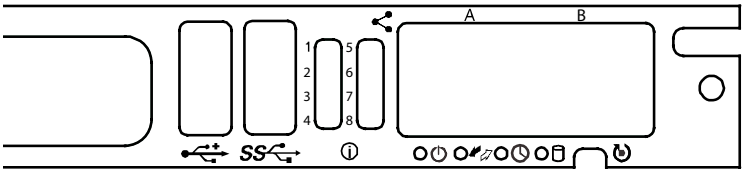


Figure 4-4: cPCI-6530BL Series LED Labels

LED 1	Port 80h bit4
LED 2	Port 80h bit5
LED 3	Port 80h bit6
LED 4	Port 80h bit7
LED 5	Port 80h bit0
LED 6	Port 80h bit1
LED 7	Port 80h bit2
LED 8	Port 80h bit3

For assistance using the GP LEDs, please log in to: **http://askanexpert.adlinktech.com**.

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4.4 Connector Pin Assignments

USB 2.0 Connectors

Pin #	Signal Name
1	Vcc
2	UV0-
3	UV0+
4	GND

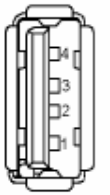
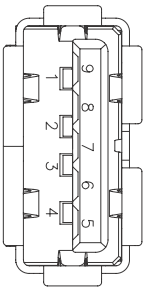


Table 4-2: USB 2.0 Pin Definition

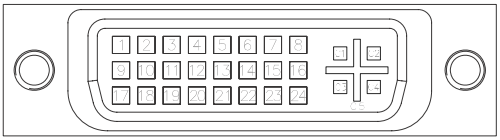
USB 3.0 Connectors

Pin #	Signal Name
1	USB3.0_P5VA
2	USB2_CMAN
3	USB2_CMAP
4	GND
5	USB3A_CMRXN
6	USB3A_CMRXP
7	GND
8	USB3A_CMTXN
9	USB3A_CMTXP



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DVI-I Connector



Pin #	Signal	Pin #	Signal
1	TMDS Data2-	16	Hot Plug Detect
2	TMDS Data2+	17	TMDS Data0-
3	GND	18	TMDSData0+
4	NC	19	GND
5	NC	20	NC
6	DDC Clock [SCL]	21	NC
7	DDC Data [SDA]	22	GND
8	Analog vertical sync	23	TMDS Clock +
9	TMDS Data1-	24	TMDS Clock -
10	TMDS Data1+	C1	Analog Red
11	GND	C2	Analog Green
12	NC	C3	Analog Blue
13	NC	C4	Analog Horizontal Sync
14	+5 V Power	C5	Analog GND Return
15	GND		

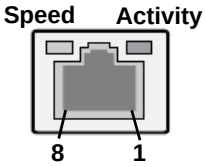
Table 4-3: DVI-I Connector Pin Definition

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RJ-45 Gigabit Ethernet Connectors

Pin #	10BASE-T/ 100BASE-TX	1000BASE-T
1	TX+	LAN_TX0+
2	TX-	LAN_TX0-
3	RX+	LAN_TX1+
4	—	LAN_TX2+
5	—	LAN_TX2-
6	RX-	LAN_TX1-
7	—	LAN_TX3+
8	—	LAN_TX3-

Table 4-4: RJ-45 GbE Pin Definitions



Status		Speed LED (Green/Orange)	Activity LED (Yellow)
Network link is not established or system powered off		OFF	OFF
10 Mbps	Link	OFF	ON
	Active	OFF	Blinking
100 Mbps	Link	Green	ON
	Active	Green	Blinking
1000 Mbps	Link	Orange	ON
	Active	Orange	Blinking

Table 4-5: LAN LED Status Definitions

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COM (RJ-45)

Pin #	RS-232	RS-422	RS-485
1	DCD#	TX-	Data-
2	RTS#	—	—
3	DSR#	—	—
4	TXD	RX+	—
5	RXD	TX+	Data+
6	GND	—	—
7	CTS#	—	—
8	DTR#L	RX-	—

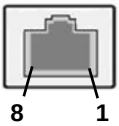


Table 4-6: Front Panel COM Pin Definitions

COM RJ-45 to DB-9 Cable

Pin #	RS-232	RS-422	RS-485
1	DCD#	TX-	Data-
2	RXD	TX+	Data+
3	TXD	RX+	—
4	DTR#L	RX-	—
5	GND	—	—
6	DSR#	—	—
7	RTS#	—	—
8	CTS#	—	—
9	—	—	—

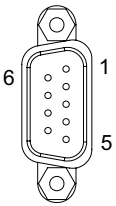


Table 4-7: COM RJ-45 to DB-9 Cable Pin Definitions

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Serial ATA 7-pin Connector (CN10)

Pin #	Signal
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

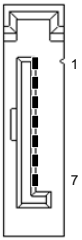


Table 4-8: Serial ATA 7-pin Connector Pin Definition

Serial ATA Connector with Power

Pin #	Signal
S1	GND
S2	TX+
S3	TX-
S4	GND
S5	RX-
S6	RX+
S7	GND
P1	NC
P2	NC
P3	NC
P4	GND
P5	GND
P6	GND
P7	5V
P8	5V
P9	5V
P10	GND
P11	NC
P12	GND
P13~P15	NC

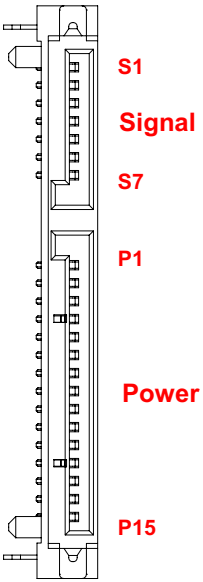
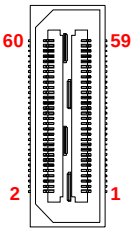


Table 4-9: Serial ATA Connector with power Pin Definition

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SATA Board-to-Board Connector (CN11)



Signal Name	Pin #	Pin #	Signal Name
GND	1	2	GND
GND	3	4	GND
GND	5	6	GND
GND	7	8	GND
GND	9	10	GND
GND	11	12	GND
GND	13	14	GND
GND	15	16	GND
GND	17	18	GND
GND	19	20	GND
GND	21	22	GND
GND	23	24	GND
GND	25	26	GND
GND	27	28	GND
GND	29	30	GND
+3.3V	31	32	+5V
+3.3V	33	34	+5V
+3.3V	35	36	+5V
+3.3V	37	38	+5V
NC	39	40	+12V
CFAST_CDI	41	42	+12V
CFAST_CDO	43	44	+12V
GND	45	46	GND
GND	47	48	SATA_TXN0
GND	49	50	SATA_TXP0
SATA_RXN0	51	52	GND
SATA_RXP0	53	54	GND
GND	55	56	NC
GND	57	58	GND
GND	59	60	GND

Table 4-10: SATA Board-to-Board Connector Pin Definition

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CFast Socket (on optional DB-CFAST)

Pin #	Signal Name
Ground	S1
SATA_TX-P	S2
SATA_TX-N	S3
Ground	S4
SATA_RX-N	S5
SATA_RX-P	S6
Ground	S7
CFast_CDI	P1
Ground	P2
NC	P3
NC	P4
NC	P5
NC	P6
Ground	P7
CFast_LED1	P8
CFast_LED2	P9
NC	P10
NC	P11
NC	P12
+3.3V	P13
+3.3V	P14
Ground	P15
Ground	P16
CFast_CDO	P17

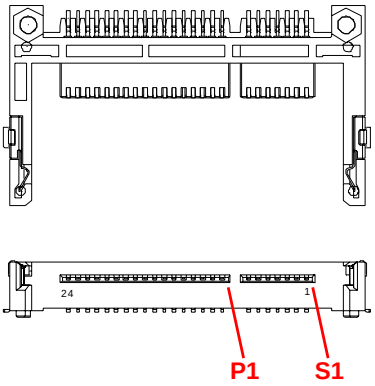
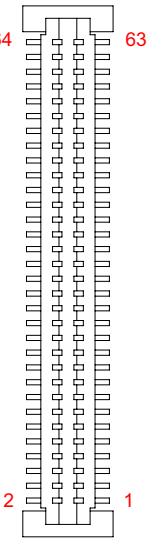


Table 4-11: CFast Socket Pin Definition

PMC Connector (JN1/5, JN2/6, JN3/7, JN4)

Pin#	JN1/5 Signal	JN2/6 Signal	JN3/7 Signal	JN4 Signal
1	PMC_TCK	+12V	NC	PIO1
2	-12V*	PMC_TRST-L	GND	PIO2
3	GND	PMC_TMS	GND	PIO3
4	PCIX_INTA-L	NC (PMC_TDO)	PCIX_CBE-L7	PIO4
5	PCIX_INTB-L	PMC_TDI	PCIX_CBE-L6	PIO5
6	PCIX_INTC-L	GND	PCIX_CBE-L5	PIO6
7	PMC_MOD-L1	GND	PCIX_CBE-L4	PIO7
8	+5V	NC	GND	PIO8
9	PCIX_INTD-L	NC	PMC_VIO	PIO9
10	NC	NC	PCIX_PAR64	PIO10
11	GND	PMC_MOD-L2	PCIX_AD63	PIO11
12	+3.3V AUX	+3.3V	PCIX_AD62	PIO12
13	CLK66_PCIX_PMC	PMC_RST-L	PCIX_AD61	PIO13
14	GND	PMC_MOD-L3	GND	PIO14
15	GND	+3.3V	GND	PIO15
16	PCIX_GNT-L0	PMC_MOD-L4	PCIX_AD60	PIO16
17	PCIX_REQ-L0	PMC_PME-L	PCIX_AD59	PIO17
18	+5V	GND	PCIX_AD58	PIO18
19	PMC_VIO	PCIX_AD30	PCIX_AD57	PIO19
20	PCIX_AD31	PCIX_AD29	GND	PIO20
21	PCIX_AD28	GND	GND	PIO21
22	PCIX_AD27	PCIX_AD26	PCIX_AD56	PIO22
23	PCIX_AD25	PCIX_AD24	PCIX_AD55	PIO23
24	GND	PCIX_AD23	PCIX_AD54	PIO24
25	GND	PMC_IDSEL	PCIX_AD53	PIO25
26	PCIX_CBE-L3	PCIX_AD23	GND	PIO26
27	PCIX_AD22	+3.3V	GND	PIO27
28	PCIX_AD21	PCIX_AD20	PCIX_AD52	PIO28
29	PCIX_AD19	PCIX_AD18	PCIX_AD51	PIO29
30	+5V	GND	PCIX_AD50	PIO30
31	PCIX_FRAME-L	PCIX_AD16	PCIX_AD49	PIO31



***Note:** -12V signal not supported on JN1 pin 2. Contact ADLINK for more information.

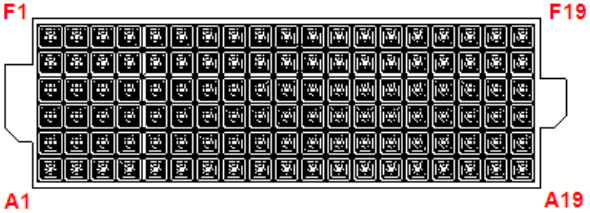
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Pin#	JN1/5 Signal	JN2/6 Signal	JN3/7 Signal	JN4 Signal
32	PCIX_AD17	PCIX_CBE-L2	GND	PIO32
33	PCIX_FRAME-L	GND	GND	PIO33
34	GND	NC	PCIX_AD48	PIO34
35	GND	PCIX_TRDY-L	PCIX_AD47	PIO35
36	PCIX_IRDY-L	+3.3V	PCIX_AD46	PIO36
37	PCIX_DEVSEL-L	GND	PCIX_AD45	PIO37
38	+5V	PCIX_STOP-L	GND	PIO38
39	PCIX_PCIXCAP	PCIX_PERR-L	GND	PIO39
40	PCIX_LOCK-L	GND	PCIX_AD44	PIO40
41	NC	+3.3V	PCIX_AD43	PIO41
42	NC	PCIX_SERR-L	PCIX_AD42	PIO42
43	PCIX_PAR	PCIX_CBE-L1	PCIX_AD41	PIO43
44	GND	GND	GND	PIO44
45	PMC_VIO	PCIX_AD14	GND	PIO45
46	PCIX_AD15	PCIX_AD13	PCIX_AD40	PIO46
47	PCIX_AD12	PCIX_M66EN	PCIX_AD39	PIO47
48	PCIX_AD11	PCIX_AD10	PCIX_AD38	PIO48
49	PCIX_AD9	PCIX_AD8	PCIX_AD37	PIO49
50	+5V	+3.3V	GND	PIO50
51	GND	PCIX_AD7	GND	PIO51
52	PCIX_CBE-L0	NC	PCIX_AD36	PIO52
53	PCIX_AD6	+3.3V	PCIX_AD35	PIO53
54	PCIX_AD5	NC	PCIX_AD34	PIO54
55	PCIX_AD4	NC	PCIX_AD33	PIO55
56	GND	GND	GND	PIO56
57	PMC_VIO	NC	GND	PIO57
58	PCIX_AD3	NC	PCIX_AD32	PIO58
59	PCIX_AD2	GND	NC	PIO59
60	PCIX_AD1	NC	NC	PIO60
61	PCIX_AD0	PCIX_ACK64-L	NC	PIO61
62	+5V	+3.3V	GND	PIO62
63	GND	GND	GND	PIO63
64	PCIX_REQ64-L	NC	NC	PIO64

Table 4-12: PMC Connector Pin Definitions

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XMC1 Connector (CN2)

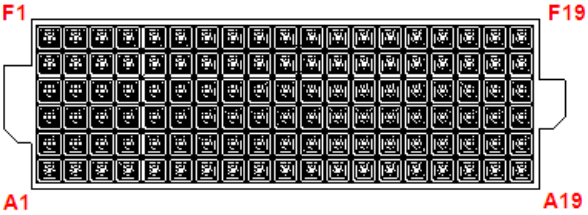


Pin#	A	B	C	D	E	F
1	PCIE_XMC1_RXP0	PCIE_XMC1_RXN0	P3V3_PSU	PCIE_XMC1_RXP1	PCIE_XMC1_RXN1	XMC1_VPWR
2	GND	GND	XMC_TRST-L	GND	GND	PLTRST_XMC1-L
3	PCIE_XMC1_RXP2	PCIE_XMC1_RXN2	P3V3_PSU	PCIE_XMC1_RXP3	PCIE_XMC1_RXN3	XMC1_VPWR
4	GND	GND	XMC1_TCK	GND	GND	XMC1_RST-L
5	PCIE_XMC1_RXP4	PCIE_XMC1_RXN4	P3V3_PSU	PCIE_XMC1_RXP5	PCIE_XMC1_RXN5	XMC1_VPWR
6	GND	GND	XMC1_TMS	GND	GND	P12V
7	PCIE_XMC1_RXP6	PCIE_XMC1_RXN6	PSVS_PSU	PCIE_XMC1_RXP7	PCIE_XMC1_RXN7	XMC1_VPWR
8	GND	GND	XMC1_TD1	GND	GND	NC
9	NC	NC	NC	NC	NC	XMC1_VPWR
10	GND	GND	NC	GND	GND	XMC1_GA0
11	PCIE_XMC1_TXP0	PCIE1_XMC1_TXN0	NC	PCIE1_XMC1_TXP1	PCIE1_XMC1_TXN1	XMC1_VPWR
12	GND	GND	XMC1_GA1	GND	GND	GND
13	PCIE_XMC1_TXP2	PCIE_XMC1_TXN2	PSVS_PSU	PCIE_XMC1_TXP3	PCIE_XMC1_TXN3	XMC1_VPWR
14	GND	GND	XMC1_GA2	GND	GND	XMC1_DAT
15	PCIE_XMC1_TXP4	PCIE_XMC1_TXN4	NC	PCIE_XMC1_TXP5	PCIE_XMC1_TXN5	XMC1_VPWR
16	GND	GND	NC	GND	GND	XMC1_CLK
17	PCIE_XMC1_TXP6	PCIE_XMC1_TXN6	NC	PCIE_XMC1_TXP7	PCIE_XMC1_TXN7	NC
18	GND	GND	NC	GND	GND	NC
19	CLK_XMC1-P	CLK_XMC1-N	NC	PCIE_WAKE-L	P3V3_PSU	NC

Table 4-13: XMC1 Connector Pin Definition

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XMC2 Connector (CN3)



Pin#	A	B	C	D	E	F
1	PCIE_XMC2_RXP0	PCIE_XMC2_RXN0	P3V3_PSU	PCIE_XMC2_RXP1	PCIE_XMC2_RXN1	XMC2_VPWR
2	GND	GND	XMC_TRST-L	GND	GND	PLTRST_XMC2-L
3	PCIE_XMC2_RXP2	PCIE_XMC2_RXN2	P3V3_PSU	PCIE_XMC2_RXP3	PCIE_XMC2_RXN3	XMC2_VPWR
4	GND	GND	XMC2_TCK	GND	GND	XMC2_RST-L
5	PCIE_XMC2_RXP4	PCIE_XMC2_RXN4	P3V3_PSU	PCIE_XMC2_RXP5	PCIE_XMC2_RXN5	XMC2_VPWR
6	GND	GND	XMC2_TMS	GND	GND	P12V
7	PCIE_XMC2_RXP6	PCIE_XMC2_RXN6	PSVS_PSU	PCIE_XMC2_RXP7	PCIE_XMC2_RXN7	XMC2_VPWR
8	GND	GND	XMC2_TD1	GND	GND	NC
9	NC	NC	NC	NC	NC	XMC2_VPWR
10	GND	GND	NC	GND	GND	XMC2_GA0
11	PCIE_XMC2_TXP0	PCIE_XMC2_TXN0	NC	PCIE_XMC2_TXP1	PCIE_XMC2_TXN1	XMC2_VPWR
12	GND	GND	XMC2_GA1	GND	GND	GND
13	PCIE_XMC2_TXP2	PCIE_XMC1_TXN2	PSVS_PSU	PCIE_XMC1_TXP3	PCIE_XMC1_TXN3	XMC2_VPWR
14	GND	GND	XMC2_GA2	GND	GND	XMC2_DAT
15	PCIE_XM2_TXP4	PCIE_XMC2_TXN4	NC	PCIE_XMC2_TXP5	PCIE_XMC2_TXN5	XMC2_VPWR
16	GND	GND	NC	GND	GND	XMC2_CLK
17	PCIE_XMC2_TXP6	PCIE_XMC2_TXN6	NC	PCIE_XMC2_TXP7	PCIE_XMC2_TXN7	NC
18	GND	GND	NC	GND	GND	NC
19	CLK_XMC2-P	CLK_XMC2-N	NC	PCIE_WAKE-L	P3V3_PSU	NC

Table 4-14: XMC2 Connector Pin Definition

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CompactPCI J1 Connector

Pin	Z	A	B	C	D	E	F
25	GND	+5V	CPCI_REQ64-L	CPCI_ENUM-L	+3.3V	+5V	GND
24	GND	CPCI_AD1	+5V	CPCI_VIO	CPCI_AD0	CPCI_ACK64-L	GND
23	GND	+3.3V	CPCI_AD4	CPCI_AD3	+5V	CPCI_AD2	GND
22	GND	CPCI_AD7	GND	+3.3V	CPCI_AD6	CPCI_AD5	GND
21	GND	+3.3V	CPCI_AD9	CPCI_AD8	CPCI_M66EN	CPCI_CBE-L0	GND
20	GND	CPCI_AD12	GND	CPCI_VIO	CPCI_AD11	CPCI_AD10	GND
19	GND	+3.3V	CPCI_AD15	CPCI_AD14	GND	CPCI_AD13	GND
18	GND	CPCI_SERR-L	GND	+3.3V	CPCI_PAR	CPCI_CBE-L1	GND
17	GND	+3.3V	IPMCB_CLK	IPMB_DAT	GND	CPCI_PERR-L	GND
16	GND	CPCI_DEVSEL-L	GND	CPCI_VIO	CPCI_STOP-L	CPCI_LOCK-L	GND
15	GND	+3.3V	CPCI_FRAME-L	CPCI_IRDY-L	CPCI_BDSEL-L	CPCI_TRDY-L	GND
12-14	Key						
11	GND	CPCI_AD18	CPCI_AD17	CPCI_AD16	GND	CPCI_CBE-L2	GND
10	GND	CPCI_AD21	GND	+3.3V	CPCI_AD20	CPCI_AD19	GND
9	GND	CPCI_CBE-L3	CPCI_IDSEL	CPCI_AD23	GND	CPCI_AD22	GND
8	GND	CPCI_AD26	GND	CPCI_VIO	CPCI_AD25	CPCI_AD24	GND
7	GND	CPCI_AD30	CPCI_AD29	CPCI_AD28	GND	CPCI_AD27	GND
6	GND	CPCI_VIO	CPCI_PRESENT-L	+3.3V	CPCI_CLK0	CPCI_AD31	GND
5	GND	NC	NC	CPCI_RST-L	GND	CPCI_VIO	GND
4	GND	+5V_IPMB	IPMC_HEALTHY-L	CPCI_VIO	NC	NC	GND
3	GND	CPCI_INTA-L	CPCI_INTB-L	CPCI_INTC-L	+5V	CPCI_INTD-L	GND
2	GND	NC	+5V	NC	NC	NC	GND
1	GND	+5V	-12V	NC	+12V	+5V	GND

Table 4-15: CompactPCI J1 Connector Pin Definition

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CompactPCI J2 Connector

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CPCI_CLK6	GND	NC	NC	NC	GND
20	GND	CPCI_CLK5	GND	NC	GND	NC	GND
19	GND	GND	GND	GND	IPMB_DAT	IPMB_CLK	GND
18	GND	NC	NC	NC	GND	NC	GND
17	GND	NC	GND	J2_RST-L	CPCI_REQ-L6	CPCI_GNT-L6	GND
16	GND	NC	NC	CPCI_DEG-L	GND	NC	GND
15	GND	NC	GND	CPCI_FAL-L	CPCI_REQ-L5	CPCI_GNT-L5	GND
14	GND	CPCI_AD35	CPCI_AD34	CPCI_AD33	GND	CPCI_AD32	GND
13	GND	CPCI_AD38	GND	CPCI_VIO	CPCI_AD37	CPCI_AD36	GND
12	GND	CPCI_AD42	CPCI_AD41	CPCI_AD40	GND	CPCI_AD39	GND
11	GND	CPCI_AD45	GND	CPCI_VIO	CPCI_AD44	CPCI_AD43	GND
10	GND	CPCI_AD49	CPCI_AD48	CPCI_AD47	GND	CPCI_AD46	GND
9	GND	CPCI_AD52	GND	CPCI_VIO	CPCI_AD51	CPCI_AD50	GND
8	GND	CPCI_AD56	CPCI_AD55	CPCI_AD54	GND	CPCI_AD53	GND
7	GND	CPCI_AD59	GND	CPCI_VIO	CPCI_AD58	CPCI_AD57	GND
6	GND	CPCI_AD63	CPCI_AD62	CPCI_AD61	GND	CPCI_AD60	GND
5	GND	CPCI_CBE-L5	CPCI_DEV64-L	CPCI_VIO	CPCI_CBE-L4	CPCI_PAR64	GND
4	GND	CPCI_VIO	NC	CPCI_CBE-L7	GND	CPCI_CBE-L6	GND
3	GND	CPCI_CLK4	GND	CPCI_GNT-L3	CPCI_REQ-L4	CPCI_GNT-L4	GND
2	GND	CPCI_CLK2	CPCI_CLK3	SYSEN-L	CPCI_GNT-L2	CPCI_REQ-L3	GND
1	GND	CPCI_CLK1	GND	CPCI_REQ-L1	CPCI_GNT-L1	CPCI_REQ-L2	GND

Table 4-16: CompactPCI J2 Connector Pin Definition

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CompactPCI J3 Connector

Pin	Z	A	B	C	D	E	F
19	GND	+5V	+5V	+12V	+5V	+5V	GND
18	GND	LAN3_TXDP0	LAN3_TXDN0	GND	LAN3_TXDP2	LAN3_TXDN2	GND
17	GND	LAN3_TXDP1	LAN3_TXDN1	GND	LAN3_TXDP3	LAN3_TXDN3	GND
16	GND	LAN4_TXDP0	LAN4_TXDN0	GND	LAN4_TXDP2	LAN4_TXDN2	GND
15	GND	LAN4_TXDP1	LAN4_TXDN1	GND	LAN4_TXDP3	LAN4_TXDN3	GND
14	GND	USB_OC45-L	USB_OC6	USB_OC7	USB_OC8	USB_OC9	GND
13	GND	USB8-P	USB8-N	GND	USB9-P	USB9-N	GND
12	GND	USB6-P	USB6-N	GND	USB7-P	USB7-N	GND
11	GND	USB4-P	USB4-N	GND	USB5-P	USB5-N	GND
10	GND	USB_OC45-L	CRT_DDC_CLK	CRT_DDC_DATA	CRT_HSYNC	CRT_VSYNC	GND
9	GND	COM2_CTS-L	COM2_RI-L	CRT_BLUE	CRT_RED	CRT_GREEN	GND
8	GND	COM2_RX	COM2_TX	COM2_DTR-L	COM2_DSR-L	COM2_RTS-L	GND
7	GND	COM3_TX	COM3_RX	COM2_DCD-L	IPMB_CLK	IPMB_DAT	GND
6	GND	SATA_RXP1	SATA_RXN1	GND	SATA_RXP0	SATA_RXN0	GND
5	GND	GND	GND	NC	GND	GND	GND
4	GND	SATA_TXP1	SATA_TXN1	GND	SATA_TXP0	SATA_TXN0	GND
3	GND	KBDATA	KBCLK	NC	MSDATA	MSCLK	GND
2	GND	AUD_SDIN1	AUD_SDIN2	NC	AUD_DOCK_EN-L	AUD_DOCK_RST-L	GND
1	GND	AUD_RST-L	AUD_SYNC	AUD_BIT_CLK	AUD_SDOUT	AUD_SDIN0	GND

Table 4-17: CompactPCI J3 Connector Pin Definition

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CompactPCI J4 Connector

Pin	Z	A	B	C	D	E	F
25	GND	PMC IO:P1	PMC IO:N1	NC	PMC IO:P2	PMC IO:N2	GND
24	GND	PMC IO:P3	PMC IO:N3	NC	PMC IO:P4	PMC IO:N4	GND
23	GND	NC	NC	NC	NC	NC	GND
22	GND	PMC IO:P5	PMC IO:N5	NC	PMC IO:P6	PMC IO:N6	GND
21	GND	PMC IO:P7	PMC IO:N7	NC	PMC IO:P8	PMC IO:N8	GND
20	GND	NC	NC	NC	NC	NC	GND
19	GND	PMC IO:17	PMC IO:19	NC	PMC IO:18	PMC IO:20	GND
18	GND	PMC IO:21	PMC IO:23	NC	PMC IO:22	PMC IO:24	GND
17	GND	NC	NC	NC	NC	NC	GND
16	GND	PMC IO:25	PMC IO:27	NC	PMC IO:26	PMC IO:28	GND
15	GND	PMC IO:29	PMC IO:31	NC	PMC IO:30	PMC IO:32	GND
12-14	GND	Key Area					Key
11	GND	PMC IO:33	PMC IO:35	NC	PMC IO:34	PMC IO:36	GND
10	GND	PMC IO:37	PMC IO:39	NC	PMC IO:38	PMC IO:40	GND
9	GND	NC	NC	NC	NC	NC	GND
8	GND	PMC IO:41	PMC IO:43	NC	PMC IO:42	PMC IO:44	GND
7	GND	PMC IO:45	PMC IO:47	NC	PMC IO:46	PMC IO:48	GND
6	GND	NC	NC	NC	NC	NC	GND
5	GND	PMC IO:49	PMC IO:51	NC	PMC IO:50	PMC IO:52	GND
4	GND	PMC IO:53	PMC IO:55	NC	PMC IO:54	PMC IO:56	GND
3	GND	NC	NC	NC	NC	NC	GND
2	GND	PMC IO:57	PMC IO:59	NC	PMC IO:58	PMC IO:60	GND
1	GND	PMC IO:61	PMC IO:63	NC	PMC IO:62	PMC IO:64	GND

Table 4-18: CompactPCI J4 Connector Pin Definition

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CompactPCI J5 Connector

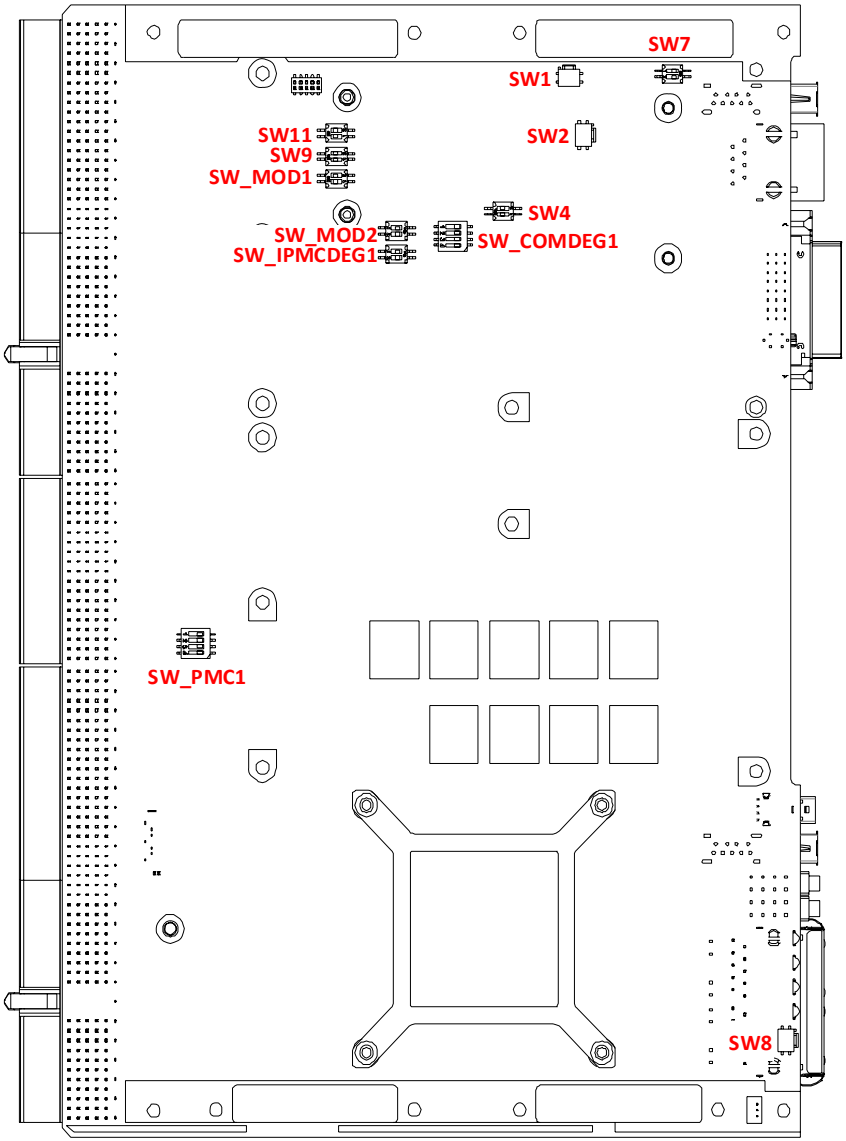
Pin	Z	A	B	C	D	E	F
22	GND	PWRLED-L	LAN4_LED_ACT-L	NC	LAN3_LED_ACT-L	NC	GND
21	GND	EDP_TX_P1	EDP_TX_N1	GND	NC	NC	GND
20	GND	EDP_TX_P0	EDP_TX_N0	GND	NC	NC	GND
19	GND	GND	GND	GND	EDP_AUX_P	EDP_AUX_N	GND
18	GND	NC	NC	GND	NC	NC	GND
17	GND	NC	NC	GND	NC	NC	GND
16	GND	GND	GND	EDP_HPD	GND	GND	GND
15	GND	NC	NC	GND	SATA_RXP2	SATA_RXN2	GND
14	GND	NC	NC	GND	SATA-TXP2	SATA-TXN2	GND
13	GND	LAN4_LED_100-L	LAN3_LED_100-L	NC	LAN3_LED_1000-L	LAN4_LED_1000-L	GND
12	GND	DVI_SDA_RTM	DVI_SCL_RTM	DVI_HPD_RTM	NC	NC	GND
11	GND	TMDSC_DATA2_P	TMDSC_DATA2_N	GND	TMDSC_CLK_P	TMDSC_CLK_N	GND
10	GND	TMDSC_DATA0_P	TMDSC_DATA0_N	GND	TMDSC_DATA1_P	TMDSC_DATA1_N	GND
9	GND	REAR_GPIO1	REAR_GPIO2	REAR_GPIO3	REAR_GPIO4	REAR_GPIO5	GND
8	GND	USB3_TX_5P	USB3_TX_5N	GND	USB3_RX_5P	USB3_RX_5N	GND
7	GND	GND	GND	BAT_RTM	GND	GND	GND
6	GND	CLK_REAR-P	CLK_REAR-N	GND	PLTRST_REAR-L	SATALED-L	GND
5	GND	GND	GND	GND	GND	GND	GND
4	GND	PCIE_TX8-P	PCIE_TX8-N	GND	PCIE_RX8-P	PCIE_RX8-N	GND
3	GND	PCIE_TX7-P	PCIE_TX7-N	GND	PCIE_RX7-P	PCIE_RX7-N	GND
2	GND	PCIE_TX6-P	PCIE_TX6-N	GND	PCIE_RX6-P	PCIE_RX6-N	GND
1	GND	PCIE_TX5-P	PCIE_TX5-N	GND	PCIE_RX5-P	PCIE_RX5-N	GND

Table 4-19: CompactPCI J5 Connector Pin Definition

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4.5 Switches and Buttons

Solder Side



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Figure 4-5: Solder-side switch and button locations

Component Side

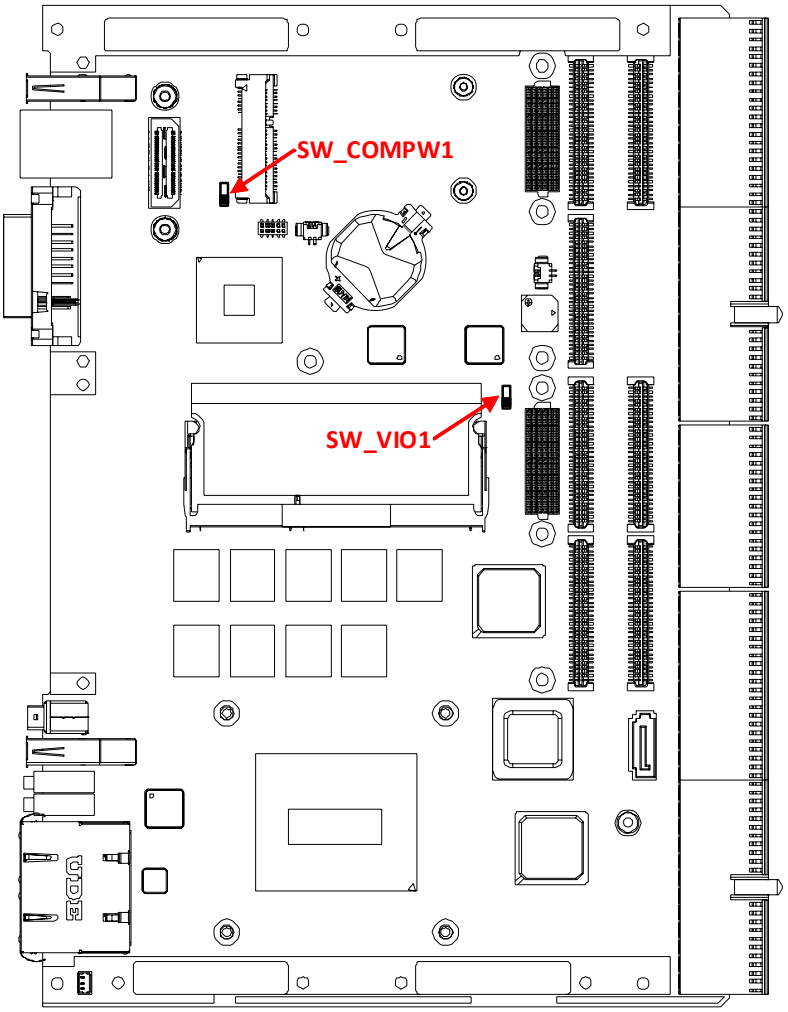
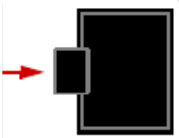


Figure 4-6: Component-side switch locations

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System Reset Button (SW8)

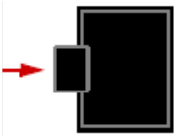
The cPCI-6530BL has a system reset button on the front panel. See “cPCI-6530BL Series Front Panel” on page 21 for the button location.



The following switches are located on the solder side. See Figure 4-4 above for their locations.

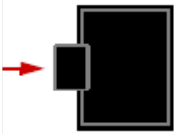
RTC Reset Button (SW1)

Press switch SW1 to clear CMOS.



Load BIOS Default Button (SW2)

Press switch SW2 to load the default BIOS settings.

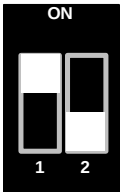


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Serial Port Setting (SW7)

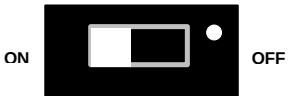
Sets the mode of the COM port on the front panel.

Mode	1	2
RS-232 (default)	ON	OFF
RS-422	ON	ON
RS-485	OFF	ON



PMC VIO Function (SW_VIO1)

Pin	Function
OFF	5V
ON	3.3V (Default)

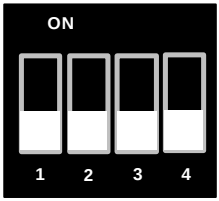


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PMC Clock Settings (SW_PMC1)

Switch SW_PMC1 allows the user to force the PCI bus to lower bandwidth and clock settings. All are set to OFF by default to support PCI-X mode up to 64-bit/133MHz maximum with the bandwidth and clock determined by the PCI device attached. For SKUs with two PMC slots, both slots will have the same clock settings.

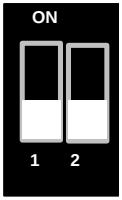
Pin	On	Off
1	Force the PCI bandwidth to 32-bit	Auto Negotiation
2	Force the PCI clock to PCI 66MHz	
3	Force the PCI bus to PCI mode (no PCI-X mode support)	
4	Force the PCI clock to PCI-X 100MHz	



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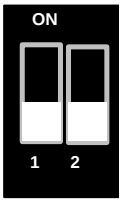
Debug Switches (SW4/9/11, SW_IPMCDEG1/SW_MOD2)

Switches SW4/9/11, SW_IPMCDEG1 and SW_MOD2 are for debugging purposes and should be left in the default settings (all OFF).



Debug Switch (SW_MOD1)

Switch SW_MOD1 is for debugging purposes and should be left in the default settings (all OFF).

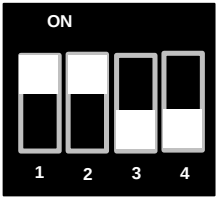


NOTE: On the CT-6530BL Conduction Cooled Blade, the SW_MOD1 default settings are 1 OFF, 2 ON.

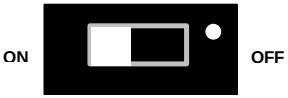
COM Debug Switches (SW_COMDEG1, SW_COMPW1)

Switch **SW_COMDEG1** is set 1, 2 ON and 3, 4 OFF by default to set the front panel RJ-45 COM (CN7) serial port as a standard RS-232 serial port. The setting can be changed to use CN7 as an IPMI debugging port. Leave on default settings unless instructed by ADLINK.

SW_COMDEG1	Function
1, 2 ON, 3, 4 OFF	Normal COM (Default)
1, 2 OFF, 3, 4 ON	IPMI Debug



Switch **SW_COMPW1** is set ON by default. Leave on default settings unless instructed by ADLINK.



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5 Getting Started

This chapter describes the following installation procedures for the cPCI-6530BL and rear transition module:

- CPU and Heatsink
- mSATA module
- 2.5” SATA hard drive
- PMC/XMC module installation

5.1 CPU and Heatsink

The cPCI-6530BL Series come with CPU and heatsink pre-installed. Removal of heatsink/CPU by users is not recommended. Please contact your ADLINK service representative for assistance.

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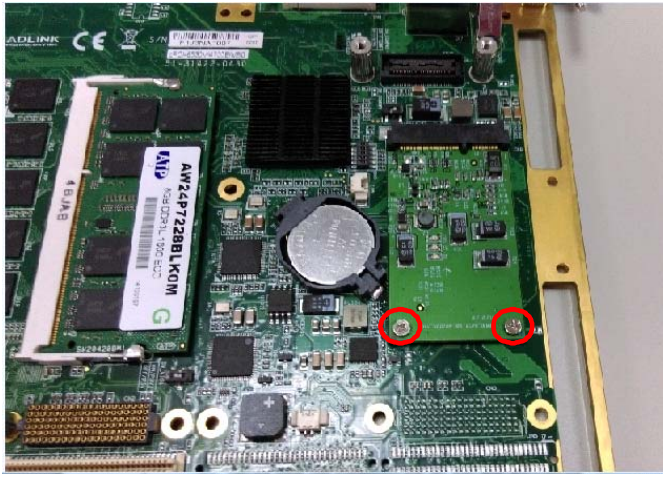
5.2 mSATA Module Installation

The cPCI-6530BLV provides space to install a mSATA module. Follow the instructions below to install a mSATA module to the cPCI-6530BL.

1. An mSATA module can be installed in the location marked as below.



2. Insert the mSATA module into the mSATA slot and secure it with two screws as shown below.



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5.3 2.5" SATA Drive Installation

The cPCI-6530BLV provides space to install a 2.5” SATA drive.

1. Locate the screws and 2.5” SATA drive bracket in the accessory pack.



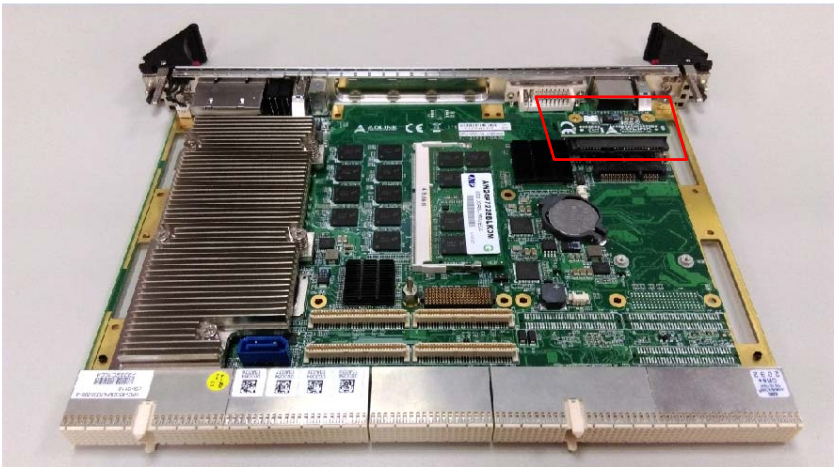
2. Secure the drive to the bracket by fastening the four screws provided as shown below.



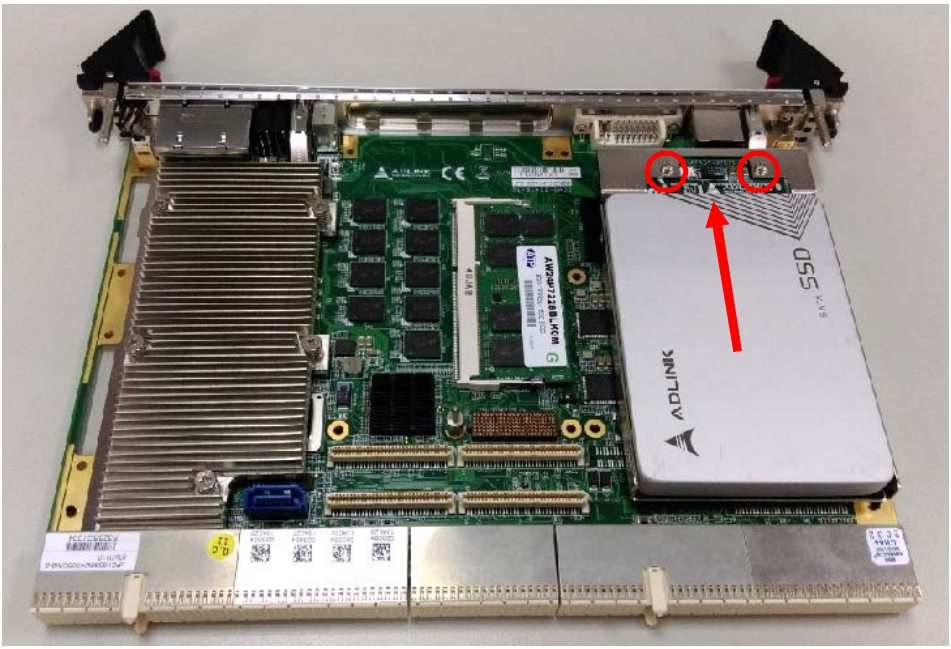
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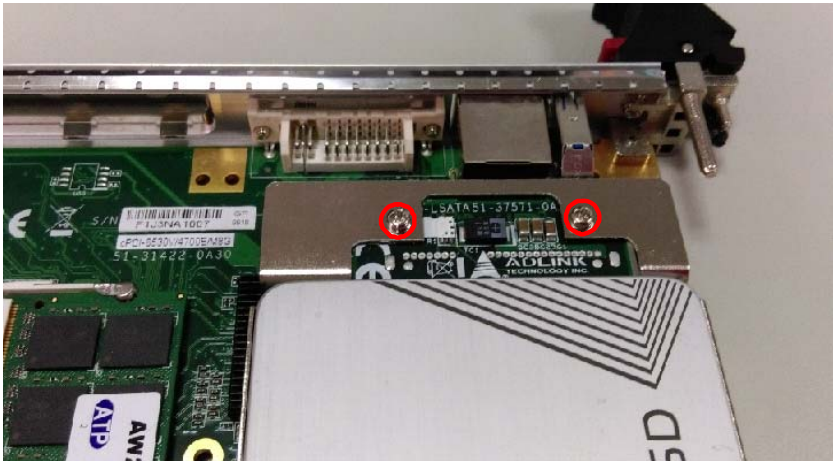
3. Find the SATA adapter board (DB-LSATA) in the accessory pack. Align the adapter board with the onboard SATA connector (CN11).





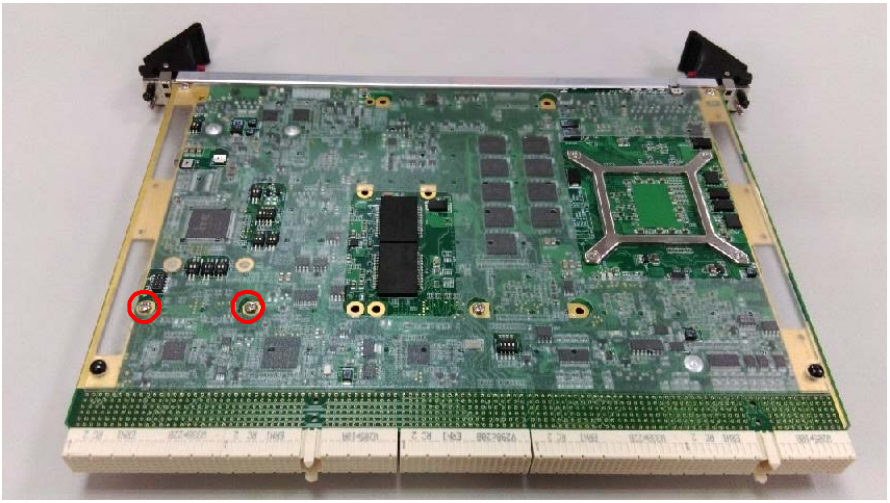
4. Align the drive assembly as shown below and insert it into the onboard SATA connector until it is properly seated. Secure the drive assembly to the blade with two screws circled below.





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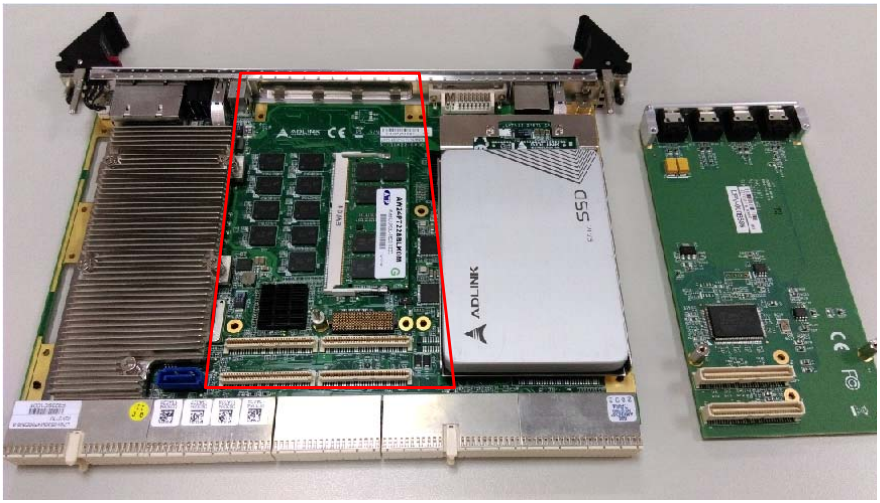
5. Turn the blade over and secure with two screws as marked below to complete the SATA drive installation.



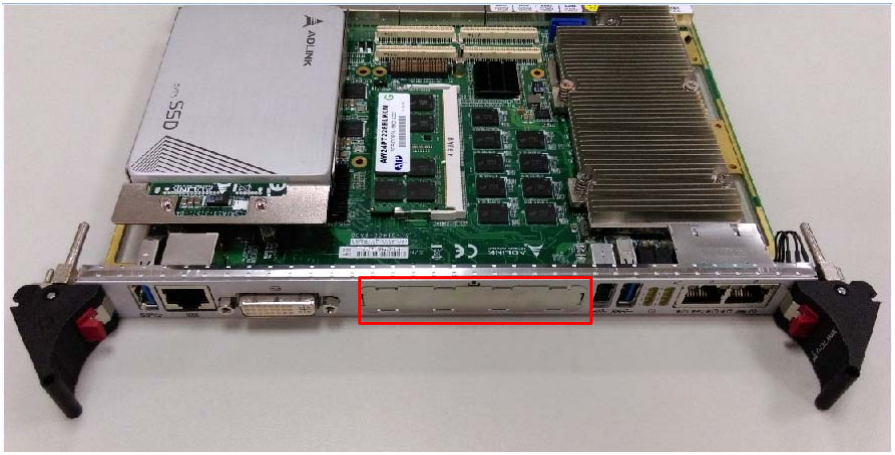
5.4 PMC/XMC Installation

The cPCI-6530BL series provides space to install PMC or XMC module(s). The cPCI-6530BL provides 2 PMC/XMC sites and the cPCI-6530BLV has 1 PMC/XMC site. The instructions below show the cPCI-6530BLV. The same procedure is used to install a second module in the cPCI-6530BL's second PMC/XMC site.

1. The cPCI-6530BLV's single PMC/XMC slot is shown below.

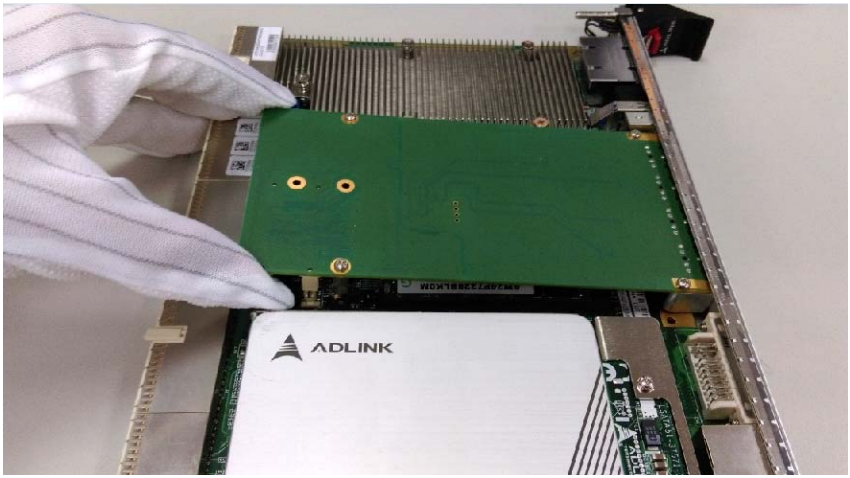


2. Remove the PMC filler plate on the front panel.

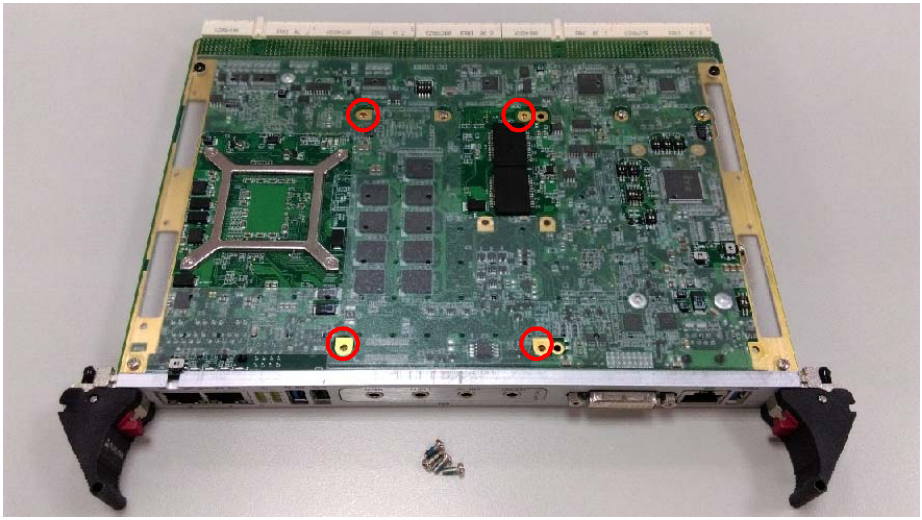


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3. Align the connectors on the PMC/XMC module to the PMC/XMC connectors on cPCI-6530BL(V) blade. Press down to secure the PMC/XMC module to the cPCI-6530BL(V).



4. Secure four screws provided by the PMC/XMC module supplier to the solder side of the cPCI-6530BL(V) blade to complete the installation of the PMC/XMC module.



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5.5 Installing the cPCI-6530BL to the Chassis

The cPCI-6530BL may be installed in a system or peripheral slot of a 6U CompactPCI chassis. These instructions are for reference only. Refer to the user guide that comes with the chassis for more information.

1. Be sure to select the correct slot depending on the operational purpose of the module. The system power may now be powered on or off.
2. Remove the blank face cover from the selected slot, if necessary.
3. Press down on the release catches of the cPCI-6530BL ejector handles.
4. **Remove the black plastic caps securing the mounting screws to the front panel.**
5. Align the module's top and bottom edges to the chassis card guides, and then carefully slide the module into the chassis. A slight resistance may be felt when inserting the module. If the resistance it too strong, check if there are bent pins on the backplane or if the board's connector pins are not properly aligned with connectors on the backplane. Then push the board until it is completely flush with the chassis.
6. Push the ejector handles outwards to secure the module in place, and then fasten the screws on the module front panel.
7. Connect the cables and peripherals to the board, and then turn the chassis on if necessary.

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6 Driver Installation

The cPCI-6530BL drivers are available from the ADLINK All-In-One DVD at **X:\cPCI\cPCI-6530BL**, or from the ADLINK website (**http://www.adlinktech.com**). ADLINK provides validated drivers for Windows 7 and Windows 8. We recommend using these drivers to ensure compatibility. The VxWorks BSP can be downloaded from the cPCI-6530BL product page on the ADLINK website

6.1 cPCI-6530BL Drivers

The following describes the cPCI-6530BL driver installation procedures for Windows 7.

1. Install the Windows operating system before installing any driver. Most standard I/O device drivers are installed during Windows installation.
2. Install the **chipset driver** by extracting and running the program in **...\Chipset\Intel_Chipset_Device_Software_All OS_9.4.0.1012.zip**.
3. Install the **graphics driver** and utilities by extracting and running the program in **...\Graphics\Intel_HD_Graphics_4600_ Win7_32bit_9.18.10.3220.zip**.
4. Install the **LAN drivers** by extracting and running the program in **…\LAN\Intel_I210_Gigabit_Network_connection_Win7 32bit_12.4.36.0.zip**.
5. Install the **Intel Rapid Storage Technology Utility** by extracting and running the program in **…\AHCI\Intel_Rapid_ Storage_Technology_32bit_and_64bit_12.5.0.1040.zip**.
6. Install the USB 3.0 driver by extracting and running the program in **…\USB\Intel_USB_3.0_xHC_Driver_AllOS_ 2.0.0.102.zip**.
7. Install the **audio driver** and utilities by extracting and running the program in **…\Audio\Realtek_High Definition Audio_ Win7_32_6.0.1.6873.zip**.

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8. Install the **Intel® Management Engine Interface driver** for Intel® AMT support by extracting and running the program in**...\Chipset\Intel_Managerment_Engine_Interface _9.0.0.1209.zip**.

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7 Utilities

7.1 Watchdog Timer

This section describes the operation of the cPCI-6530BL's watch dog timer (WDT). The primary function of the WDT is to monitor the cPCI-6530BL operation and to reset the system if a software application fails to function as programmed. The following WDT functions may be controlled using a software application:

- enabling and disabling
- reloading timeout value

The cPCI-6530BL custom WDT circuit is implemented using the internal IO of the ITE Super I/O IT8783 which is at 2Eh of LPC. The basic functions of the WDT include:

- Starting the timer countdown.
- Enabling or disabling WDT.
- Enable or disable WDT countdown LED ON.
- Reloading the timeout value to keep the watch dog from timing out.
- Setting the range of the timeout period from 1 to 15300 seconds.
- Sending a RESET signal to system when the watch dog times out

Using the Watchdog in an Application

The following section describes the WDT functions in an application. The WDT reset function is explained in the previous section. This can be controlled through the registers in the cPCI-6530BL Super I/O.

An application using the reset feature enables the watchdog function, sets the count-down period, and reloads the timeout value periodically to keep it from resetting the system. If the timer countdown value is not reloaded, the watchdog resets the system hardware after its counter reaches zero.

For a detailed programming sample, refer to the sample code provided in the ADLINK All-In-One CD. You may find this in the following directory: X:\cPCI\cPCI-6530BL\WDT.

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Sample Code

```
#include<stdio.h>
#include<dos.h>

#define IT8783_ID1 0x87
#define IT8783_ID2 0x83

static unsigned int IT8783_ioPort = 0x2e;

//Check index port
void Enter_IT8783_Config(unsigned int flag)
{
   if(flag) IT8783_ioPort = 0x4e;

   switch(IT8783_ioPort)
   {
        case 0x2E:  //Address port = 0x2E, enter
   keys = 0x87, 0x01, 0x55, 0x55
             outportb(0x2E, 0x87);
             outportb(0x2E, 0x01);
             outportb(0x2E, 0x55);
             outportb(0x2E, 0x55);
             break;
        case 0x4E:  //Address port = 0x4E, enter
   keys = 0x87, 0x01, 0x55, 0xAA
             outportb(0x4E, 0x87);
             outportb(0x4E, 0x01);
             outportb(0x4E, 0x55);
             outportb(0x4E, 0xAA);
             break;
        default:
             break;
      }
}

//Exit index port
void Exit_IT8783_Config(unsigned int flag)
{
   if(flag) IT8783_ioPort = 0x4e;

   outportb(IT8783_ioPort, 0x02);
```

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```
   outportb(IT8783_ioPort+1, 0x02);
}

//Check chip
void Get_IT8783_ID(unsigned int &ID1, unsigned int
   &ID2)
{
   outportb(IT8783_ioPort, 0x20);
   ID1 = inportb(IT8783_ioPort+1);
   outportb(IT8783_ioPort, 0x21);
   ID2 = inportb(IT8783_ioPort+1);
}

//WDT and LED program
void IT8783_3_WDTRun(unsigned int count_value,
   unsigned int PLEDflag)   //for cPCI-6530BL
{
   unsigned long tempCount;
   unsigned int registerValue;


   outportb(IT8783_ioPort, 0x07);
   outportb(IT8783_ioPort+1, 0x07);// Device 7

   outportb(IT8783_ioPort, 0xf8);
   outportb(IT8783_ioPort+1, 0x00);// PLED mapping
   to nothing, disable PLED function

   if(PLEDflag == 1)
   {
        outportb(IT8783_ioPort, 0x2D);
        registerValue = inportb(IT8783_ioPort + 1);
        registerValue |= 0x01;       // set Pin109
   is GPIO function GP60
        outportb(IT8783_ioPort+1, registerValue);

        outportb(IT8783_ioPort, 0xC5);
        registerValue = inportb(IT8783_ioPort + 1);
        registerValue &= 0xfe;      // set GP60 is
   alternate function
        outportb(IT8783_ioPort+1, registerValue);
```

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```
        outportb(IT8783_ioPort, 0xCD);
        registerValue = inportb(IT8783_ioPort + 1);
        registerValue |= 0x01;  // set GP60 is
output
        outportb(IT8783_ioPort+1, registerValue);

        outportb(IT8783_ioPort, 0xf8);
        outportb(IT8783_ioPort+1, 0x30);// PLED
mapping to GP60

        outportb(IT8783_ioPort, 0xf9);
        registerValue = inportb(IT8783_ioPort + 1);
        registerValue |= 0x02;
        registerValue &= 0xfb;
        outportb(IT8783_ioPort+1, registerValue);
}
outportb(IT8783_ioPort, 0x71);
registerValue = inportb(IT8783_ioPort + 1);
registerValue |= 0xD0;  // set Mouse & Keyboard
interrupt Enable
outportb(IT8783_ioPort+1, registerValue);

outportb(IT8783_ioPort, 0x73);
outportb(IT8783_ioPort+1, count_value); // set
WDT count LSB
tempCount = tempCount >> 8;
outportb(IT8783_ioPort, 0x74);
outportb(IT8783_ioPort+1, count_value); // set
WDT count MSB

if(count_value >= 60)
{
        outportb(IT8783_ioPort, 0x72);
        registerValue = inportb(IT8783_ioPort+1);
        registerValue &= 0x8f;
        registerValue |= 0x10; //enable WDT output
through PowerOK!
        outportb(IT8783_ioPort+1, registerValue); //
set WDT count is minute

        tempCount = count_value / 60;
        if((count_value%60) > 30)
```

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```
                tempCount++;
           if(tempCount > 65535)
                tempCount = 65535;
           printf("WDT timeout in %d minutes.\n",
      tempCount);
      }
      else
      {
           outportb(IT8783_ioPort, 0x72);
           registerValue = inportb(IT8783_ioPort+1);
           registerValue |= 0x80;

           tempCount = count_value;
           if(tempCount != 0)
           {
                printf("WDT timeout in %d seconds.\n",
      tempCount);
                registerValue |= 0x40; //Enable WDT
      output through KBRST
           }
           else
           {
                printf("WDT is Disabled.\n");
                registerValue &= 0xbf; //Disable WDT
      output through KBRST
           }

           outportb(IT8783_ioPort+1, registerValue); //
      set WDT count is second
      }

}
```

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8 BIOS Setup Utility

The following chapter describes basic navigation for the AMI EFI BIOS setup utility.

8.1 Starting the BIOS

To enter the setup screen, follow these steps:

1. Power on the motherboard
2. Press the < Delete > key on your keyboard when you see the following text prompt:
   < Press DEL to run Setup >
3. After you press the < Delete > key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu.



Note: In most cases, the < Delete > key is used to invoke the setup screen. There are several cases that use other keys, such as < F1 >, < F2 >, and so on.

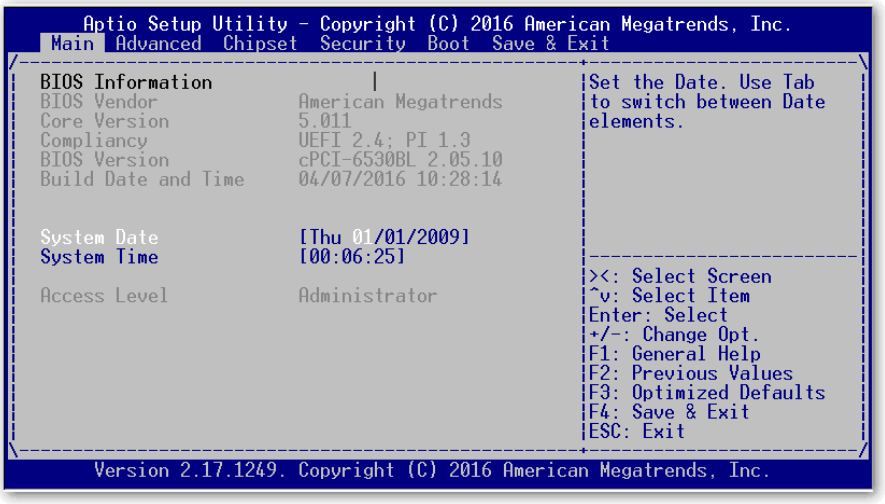
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Setup Menu

The main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in this user's guide.

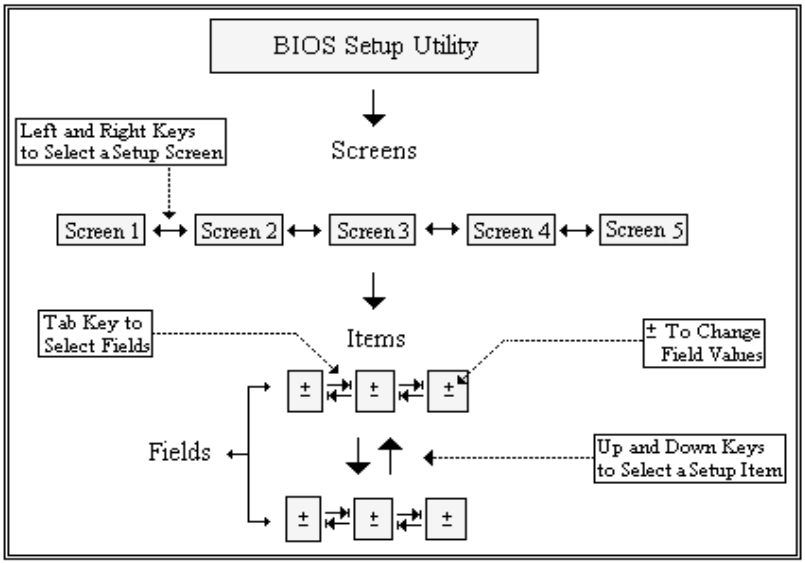
The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed" options cannot be configured, "Blue" options can be.

The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.



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Navigation



Note: There is a hot key legend located in the right frame on most setup screens.

Keyboard Commands

< > The *Left* and *Right* "Arrow" keys allow you to select a setup screen.

^ v The *Up* and *Down* "Arrow" keys allow you to select a setup screen.

+ - The *Plus* and *Minus* keys allow you to change the field value of a particular setup item.

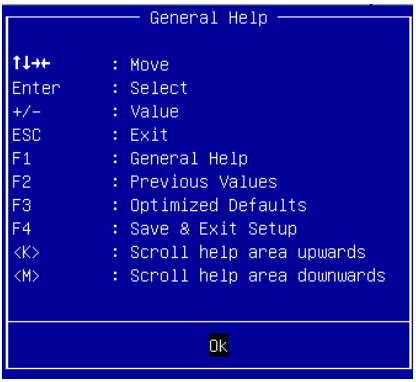
Tab Moves the cursor to the next configurable item or to the next field.

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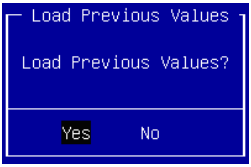
Hotkey Descriptions

Enter The < Enter > key allows you to display or change the setup option listed for a particular setup item. The < Enter > key can also allow you to display the setup sub-screens.

F1 The < F1 > key allows you to display the General Help screen. Press the < F1 > key to open the General Help screen.



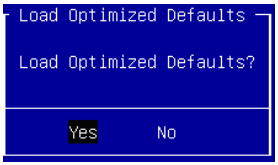
F2 The < F2 > key on your keyboard is the previous values key. It is not displayed on the key legend by default. To set the previous values settings of the BIOS, press the < F2 > key on your keyboard. It is located on the upper row of a standard 101 keyboard. The previous values settings allow the motherboard to boot up with the least amount of options set. This can lessen the probability of conflicting settings.



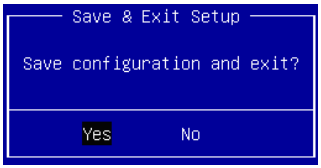
F3 The < F3 > key on your keyboard is the optimized defaults key. To set the optimized defaults settings of the BIOS, press the < F3 > key on your keyboard. It is located on the upper row of a standard 101 keyboard. The optimized defaults settings allow the motherboard to boot up with the optimized defaults of options set. This can lessen the probability of

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conflicting settings.

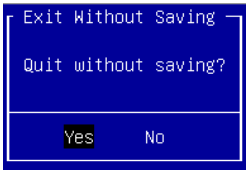


F4 The < F4 > key allows you to save any changes you have made and exit Setup. Press the < F10 > key to save your changes. The following screen will appear:



Press the < Enter > key to save the configuration and exit. You can also use the < Arrow > key to select Cancel and then press the < Enter > key to abort this function and return to the previous screen.

ESC The < Esc > key allows you to discard any changes you have made and exit the Setup. Press the < Esc > key to exit the setup without saving your changes. The following screen will appear:

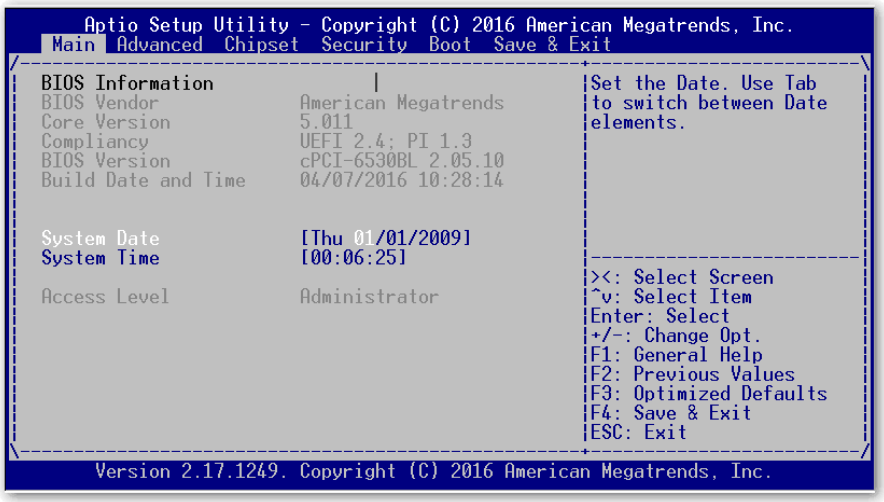


Press the < Enter > key to discard changes and exit. You can also use the < Arrow > key to select Cancel and then press the < Enter > key to abort this function and return to the previous screen.

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8.2 Main Setup

When you first enter the Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



System & Board Info

BIOS Vendor

Displays the BIOS vendor.

Core Version

Displays the BIOS core version.

Project Version

Displays the current BIOS revision.

Build Data

Displays the BIOS build data.

System Language

Displays the system default language (English only).

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System Time/System Date

Use this option to change the system time and date. Highlight System Time or System Date using the < Arrow > keys. Enter new values using the keyboard. Press the < Tab > key or the < Arrow > keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

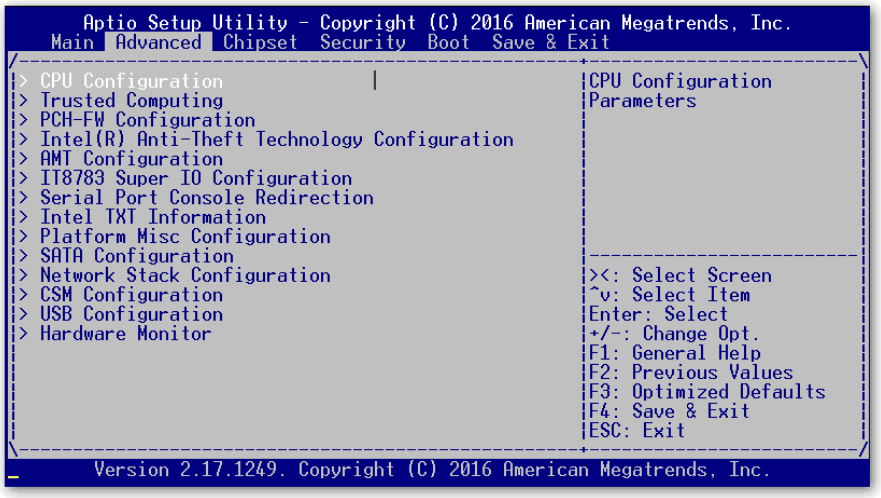
Note: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

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8.3 Advanced BIOS Setup

Select the Advanced tab from the setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as SuperIO Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the < Arrow > keys. The Advanced BIOS Setup screen is shown below.

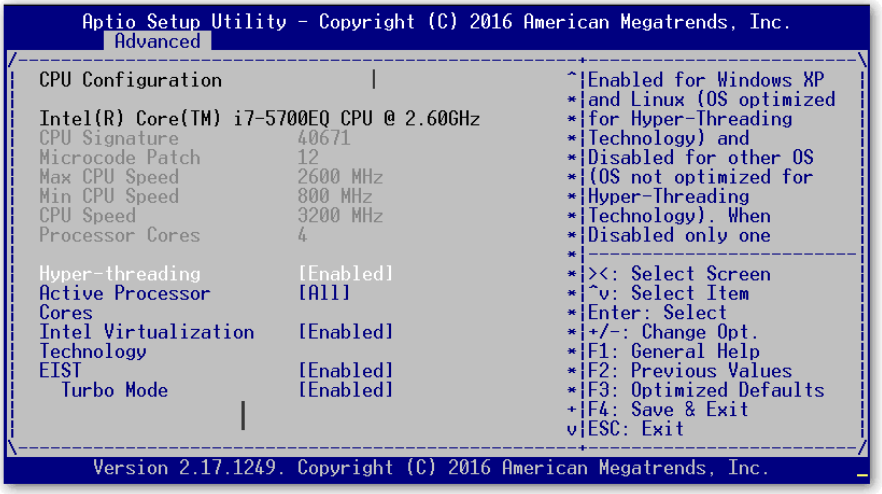
The sub menus are described on the following pages.



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8.3.1 CPU Configuration

You can use this screen to select options for the CPU Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the CPU Configuration screen is shown below.



Hyper-Threading

- **Enabled:** for Windows and Linux (OS optimized for Hyper-Threading Technology).
- **Disabled:** for other OS (OS not optimized for Hyper-Threading Technology).

Intel Virtualization Technology

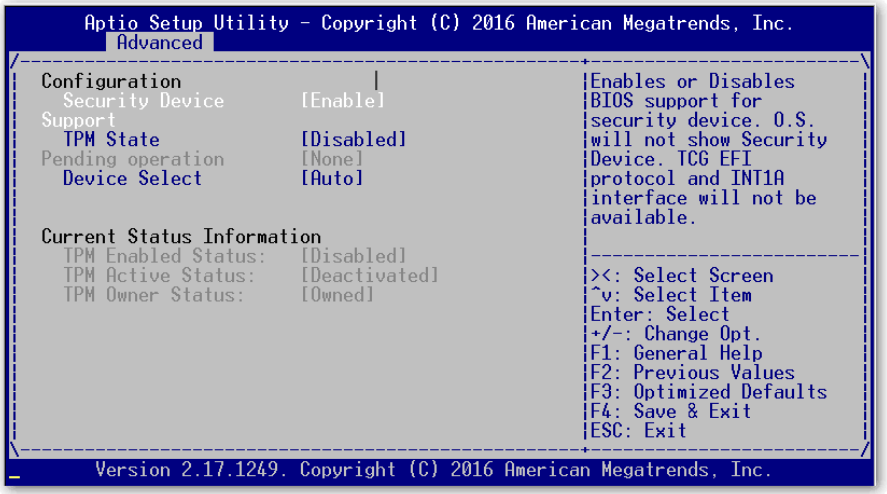
When Enabled, a VMM can utilize the additional hardware capability provided by Vanderpool Technology. Set this value to Enabled/Disabled.

- **EIST:** Set this value to Enabled/Disabled
- **Turbo Mode:** Set this value to Enabled/Disabled.

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8.3.2 Trusted Computing

Trusted Computing is an industry standard to make personal computers more secure through a dedicated hardware chip, called a Trusted Platform Module (TPM). This option allows you to enable or disable the TPM support.



Security Device Support

OS will not show TPM. Reset of platform is required. Set this value to Enabled/Disabled.

TPM State

Determine whether TPM state change requires Password Authentication. Set this value to Enabled/Disabled.

Pending TPM operation

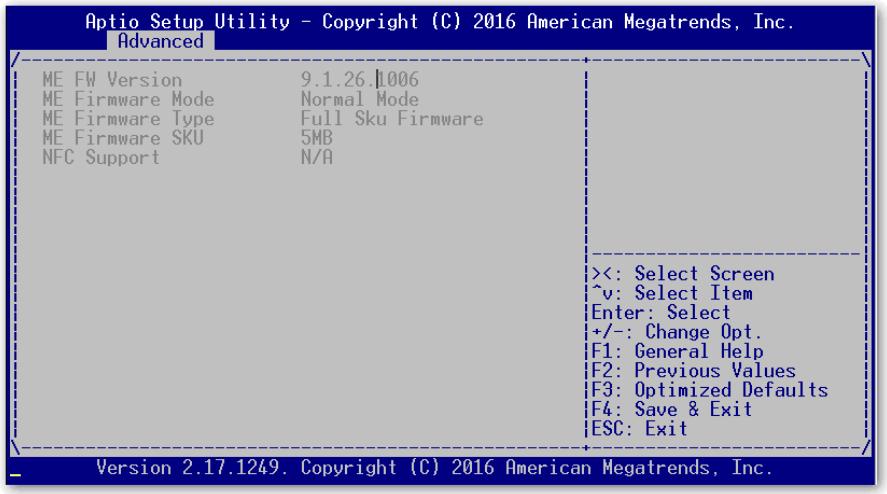
Schedule TPM operation. The settings for this value are Enable, Disable and Clear.

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8.3.3 PCH-FW Configuration

Intel TXT(LT) Configuration

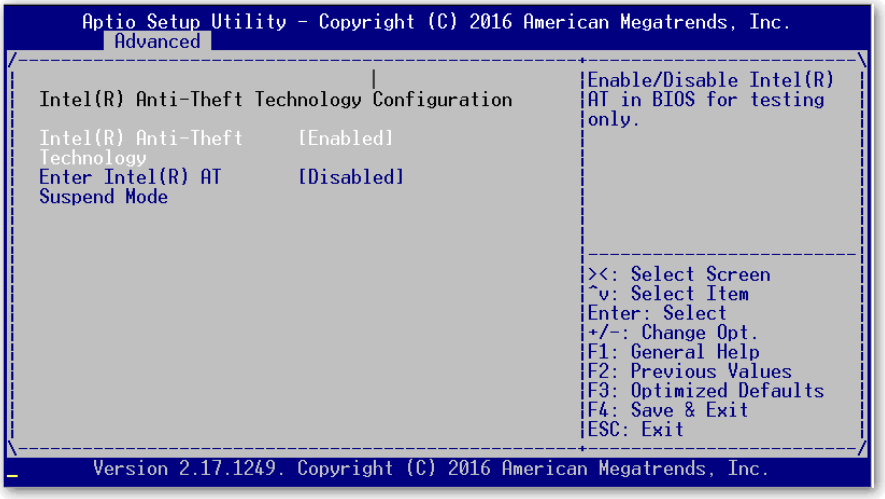
You can use this screen to view ME related information. For example, ME FW Version, ME Firmware Mode, ME Firmware Type, ME Firmware SKU..etc. An example of the ME screen is shown below.



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8.3.4 Intel Anti-Theft Technology Configuration

You can use this screen to select options for the Intel AT Configuration Settings. An example of the Intel AT Configuration screen is shown below.



Intel Anti-Theft Technology

Set this value to Enabled/Disabled.

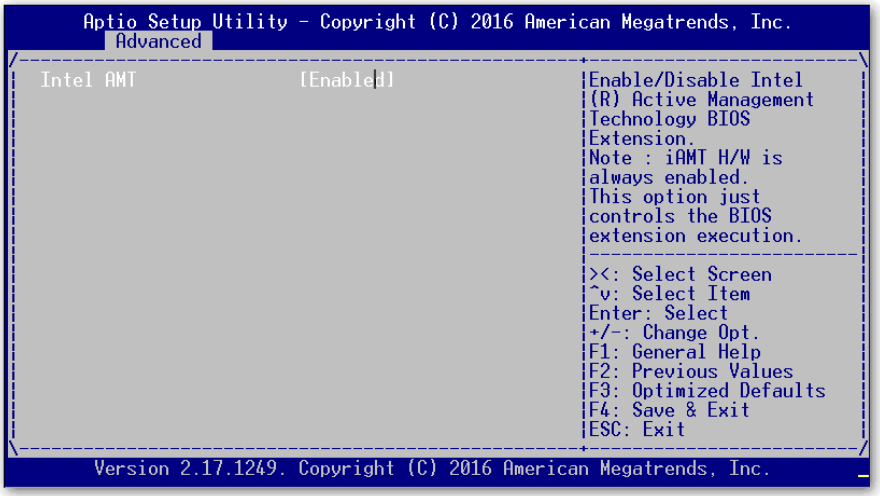
Enter Intel® AT Suspend Mode

Request that the platform enter Intel® AT Suspend Mode.

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8.3.5 AMT Configuration

You can use this screen to select options for the AMT settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option.



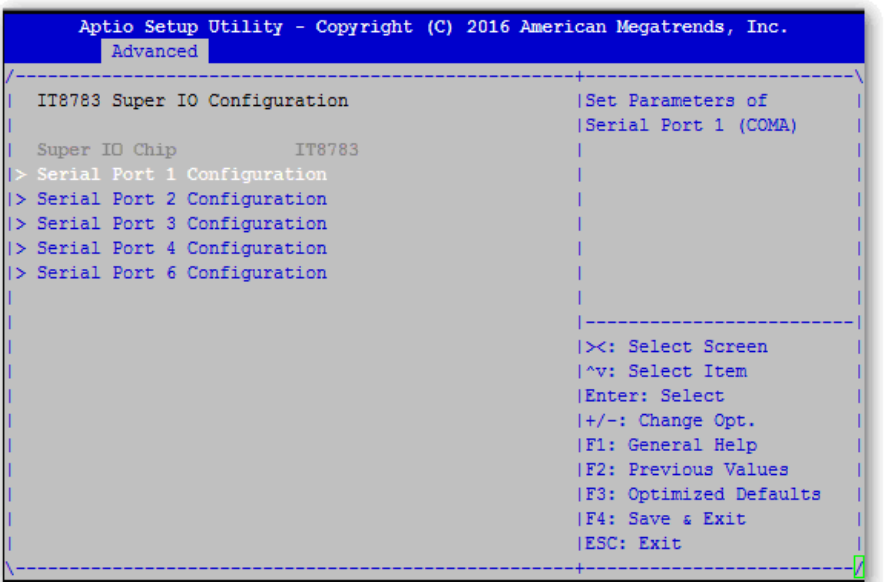
Intel AMT

Intel AMT feature. Set this value to Enabled/Disabled.

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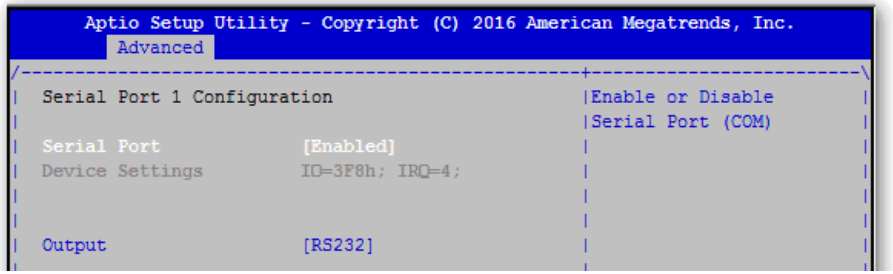
8.3.6 IT8783 Super IO Configuration

You can use this screen to select options for the serial port console redirection settings. An example of the Serial Port Console Redirection screen is shown below.



Serial Port 1,2,3,4,6 Configuration

Set Parameters of Serial Port 1,2,3,4,6 (COM 1,2,3,4,6). Serial port 4 is for SOL, Port 6 is IPMI interface. Set this value to Enabled/Disabled. The screen is shown below.



Serial Port

Select current COM port Disable or Enable of serial port 1,2,3,(COM1,2,3,4,). Set this value to Enable or Disable.

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8.3.7 Serial Port Console Redirection

You can use this screen to select options for the serial port console redirection settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the Serial Port Console Redirection screen is shown below.



Console Redirection

Set this value to Enabled/Disabled.

Console Redirection Settings

The settings specify how the host computer and the remote computer will exchange data. Both computers should have the same or compatible settings. The screen is shown below.

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Terminal Type

VT100+ is the preferred terminal type for out-of-band management. Configuration options: VT100, VT100+, VT-UTF8, ANSI.

Bits per second

Select the bits per second you want the serial port to use for console redirection. The options are 115200, 57600, 38400, 19200, 9600.

Data Bits

Select the data bits you want the serial port to use for console redirection. Set this value to 7, 8.

Parity

Set this option to select Parity for console redirection. The settings for this value are None, Even, Odd, Mark, Space.

Stop Bits

Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit.

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Communication with slow devices may require more than 1 stop bit. Set this value to 1 and 2.

Flow Control

Set this option to select Flow Control for console redirection. The settings for this value are None, Hardware RTS/CTS.

VT-UTF8 Combo Key Support

Enables VT-UTF8 combination key support for ANSI/VT100 terminals.Set this value to Enabled/Disabled.

Recorder Mode

When this mode is enabled, only text will be sent. This is to capture terminal data. Set this value to Enabled/Disabled.

Resolution 100x31

Set this option to extended terminal resolution. Set this value to Enabled/Disabled.

Legacy OS Redirection

On legacy OS, the number of rows and columns supported for redirection. Set this value to 80x24, 80x25.

Putty Key Pad

Select FunctionKey and KeyPad on Putty. Set this value to VT100, LINUX, XTERMR6, SCO, ESCN, VT400.

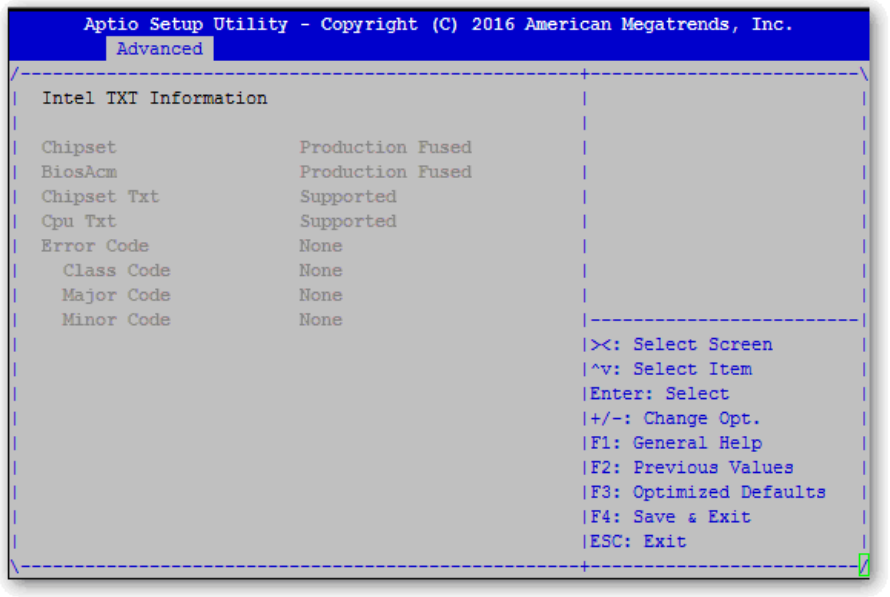
Redirection After BIOS POST

These Settings specify that if BootLoader is selected, then Legacy Console Redirection is disabled before booting into a Legacy OS. The default value is Always Enable, which means Legacy Console Redirection is enabled for Legacy OS.

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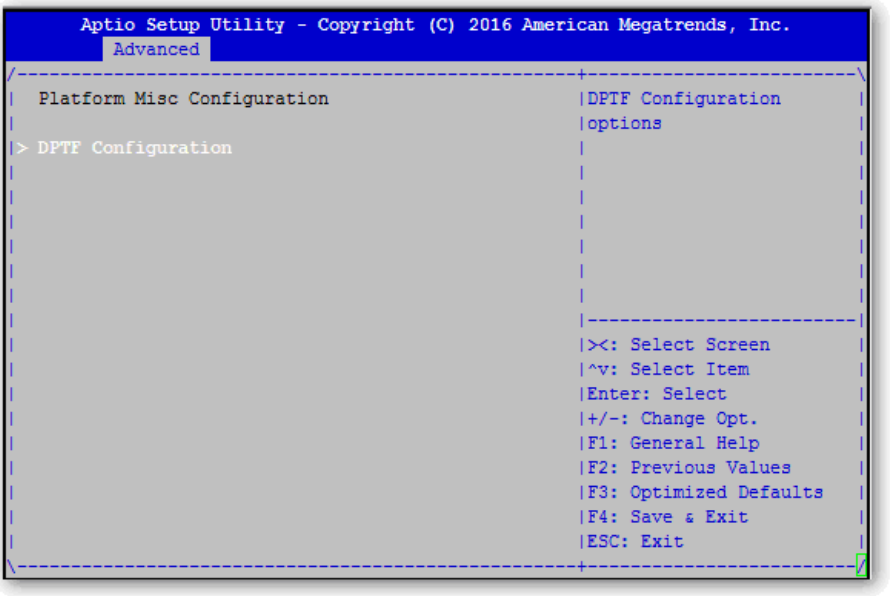
8.3.8 Intel TXT Information

You can use this screen to view Intel TXT information.

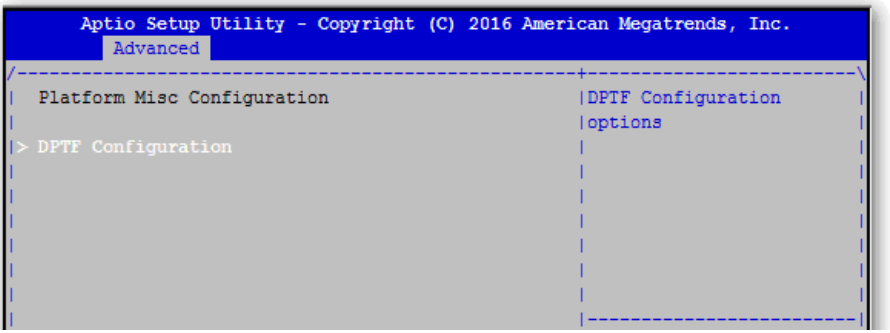


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8.3.9 Platform Misc Configuration



DPTF Configuration



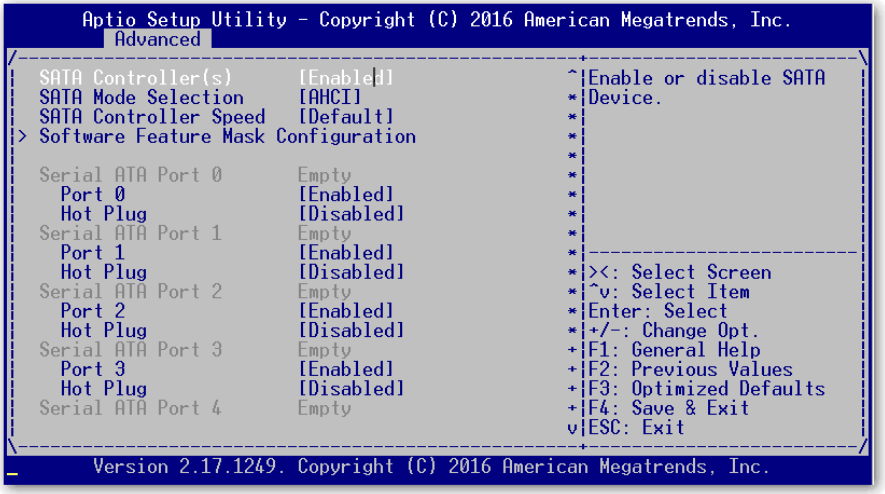
DPTF

Enable/Disable Intel® Dynamic Platform Thermal Framework.

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8.3.10 SATA Configuration

You can use this screen to select options for the SATA Configuration Settings. An example of the SATA Configuration screen is shown below.



SATA Controller(s)

Enable or disable SATA device.

SATA Mode Selection

The SATA can be configured as a legacy IDE, RAID and AHCI mode.

SATA Port 0-4

Display SATA device name string. Set this value to Enabled/Disabled.

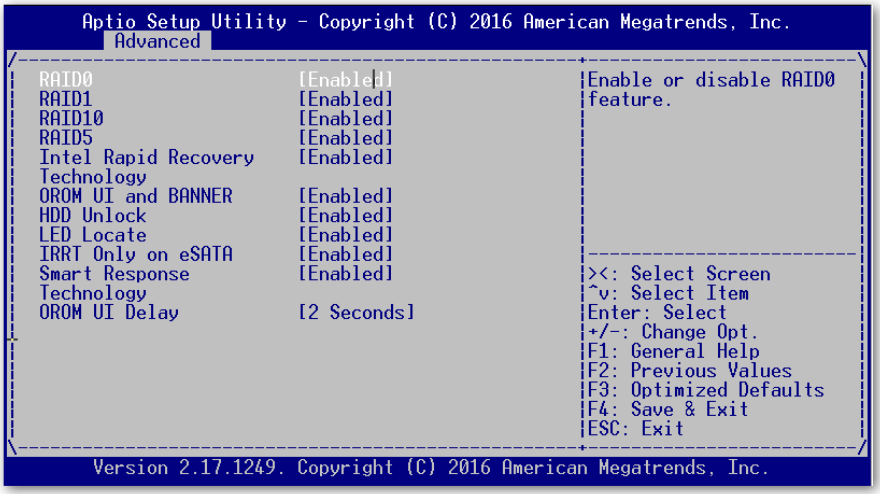
Hot Plug

Appears when SATA mode is AHCI. SATA port Hot Plug support. Set this value to Enabled/Disabled.

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Software Feature Mask Configuration

RAID OROM/RST driver will refer to the SWFM configuration to enable or disable the storage features.



RAID0-5

Enable or disable RAID0-5 feature.

Intel Rapid Recovery Technology

Enable or disable Intel Rapid Recovery Technology.

OROM UI and Banner

If enabled, the OROM UI is shown. Otherwise, no OROM banner or information will be displayed if all disks and RAID volumes are Normal.

HDD Unlock

If enabled, the HDD password unlock in the OS is enabled.

LED Locate

If enabled, the LED/SGPIO hardware is attached and ping to locate feature is enabled on the OS.

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IRRT Only on eSATA

If enabled, then only IRRT volumes can span internal and eSATA drives. If disabled, then any RAID volume can span internal and eSATA drives.

Smart Response Technology

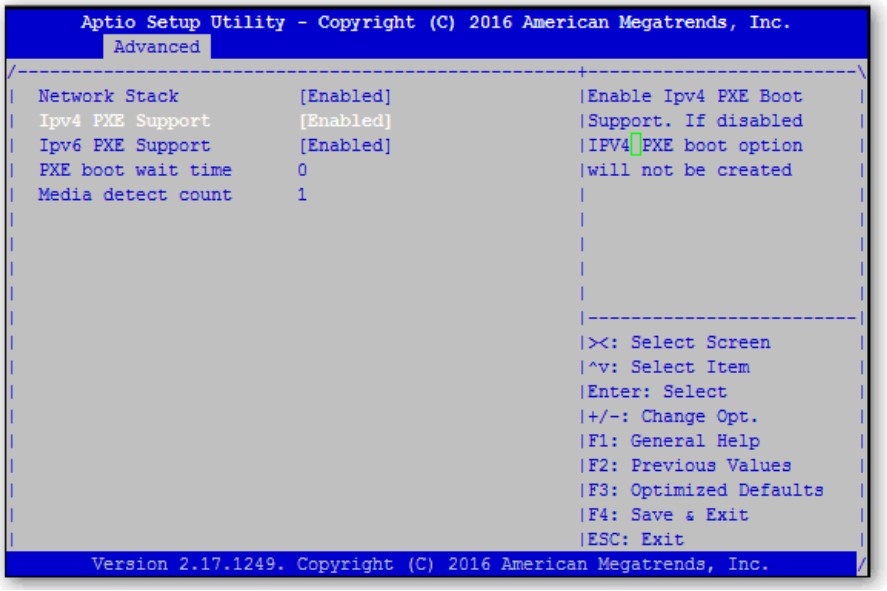
Enable or disable Smart Response Technology.

OROM UI Delay

If enabled, indicates the delay of the OROM UI Splash Screen under normal status.

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8.3.11 Network Stack Configuration



Network Stack

Enable/Disable UEFI Network Stack.

IPv4 PXE Support

Enable IPv4 PXE Boot Support. If disabled, the IPv4 PXE boot option will not be created.

IPv6 PXE Support

Enable IPv6 PXE Boot Support. If disabled, the IPv6 PXE boot option will not be created.

PXE Boot Wait Time

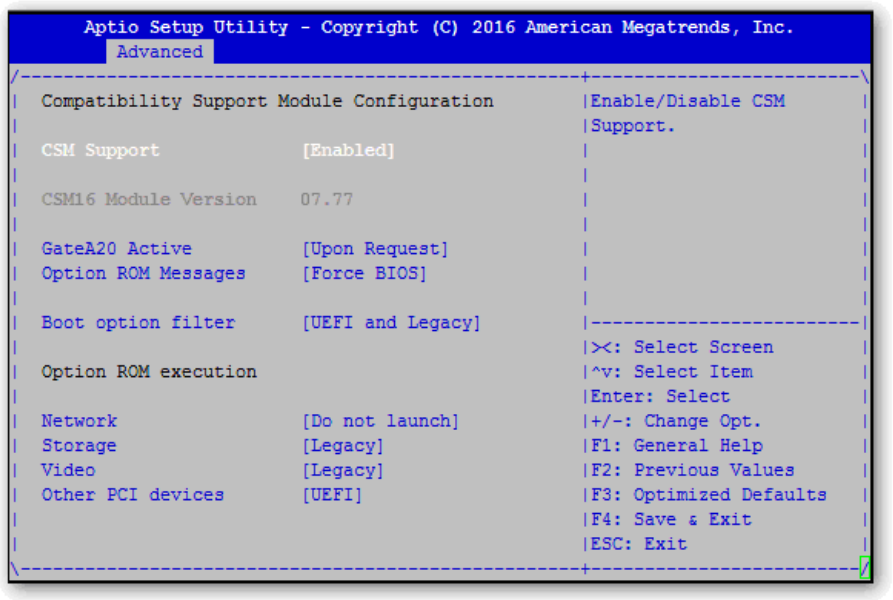
Wait time to press ESC key to abort PXE boot.

Media detect count

Number of times the presence of media will be checked.

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8.3.12 CSM Configuration



CSM Support

Enable/Disable CSM Support.

GateA20 Active

Upon Request: GA20 can be disabled using BIOS services. Always: do not allow disabling of GA20; this option is useful when any RT code is executed above 1MB.

Option ROM Messages

Set the display mode for Option ROM.

Boot Option Filter

This option controls Legacy/UEFI ROM priority. Set this value to UEFI and Legacy, Legacy only, UEFI only.

Network

Controls the execution of UEFI and Legacy PXE OpROM. Set this value to Do not launch, Legacy, UEFI.

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Storage

Controls the execution of UEFI and Legacy PXE OpROM. Set this value to Do not launch, Legacy, UEFI.

Video

Controls the execution of UEFI and Legacy PXE OpROM. Set this value to Do not launch, Legacy, UEFI.

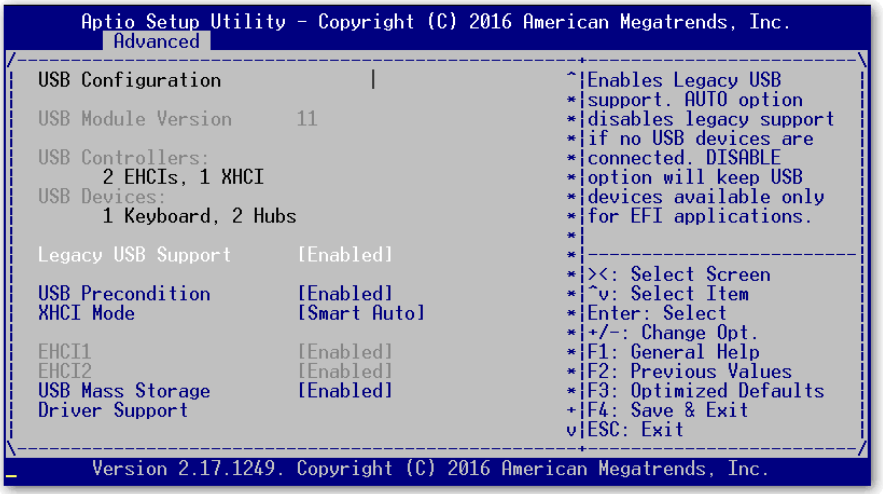
Other PCI Devices

Determines OpROM execution policy for devices other than Network, Storage, or Video. Set this value to Disable, Legacy, UEFI.

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8.3.13 USB Configuration

You can use this screen to select options for the USB Configuration. Use the up and down < Arrow > keys to select an item. The screen is shown below.



Legacy USB Support

Enables legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications. Set this value to Enabled/Disabled/Auto.

USB Precondition

Enable/Disable precondition work on USB host controller and root ports for faster enumeration.

XHCI Mode

Set the mode of operation of the xHCI controller.

EHCI1/EHCI2

Controls the USB EHCI (USB 2.0) functions. One EHCI controller must always be enabled.

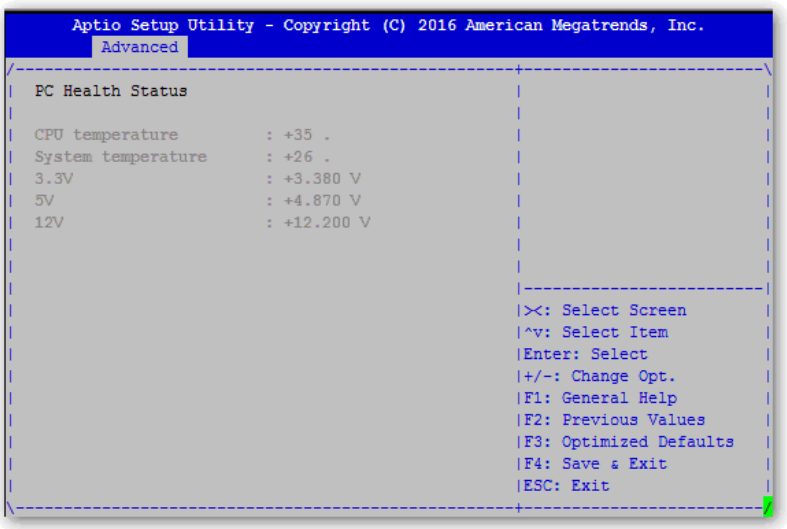
USB Mass Storage Driver Support

Enable/Disable USB Mass Storage Driver Support.

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8.3.14 Hardware Monitor

This option displays the current status of all of the monitored hardware devices/components such as voltages and temperatures.



CPU Temperature

Displays current CPU temperature.

System Temperature

Displays current system temperature.

3.3V

Displays current system 3.3V voltage.

5V

Displays current system 5V voltage.

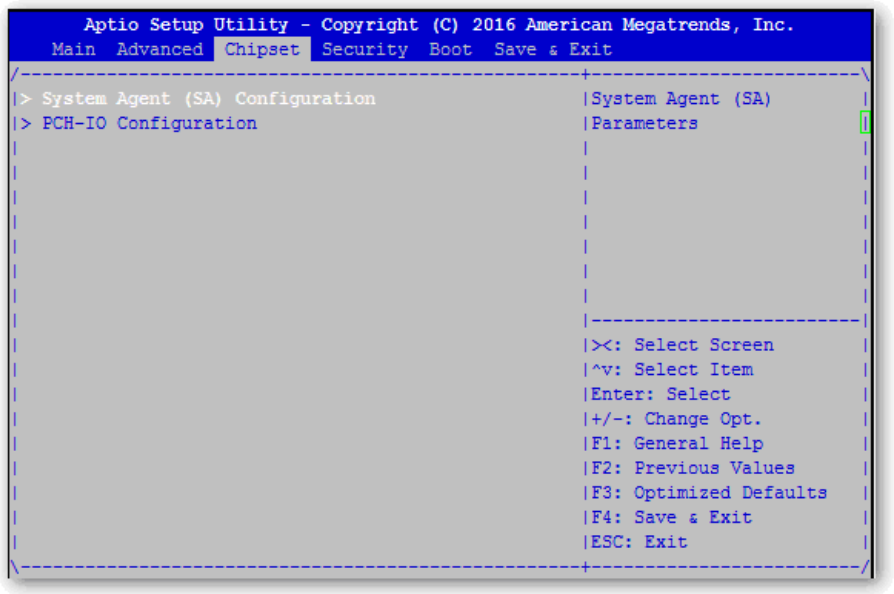
12V

Displays current system 12V voltage.

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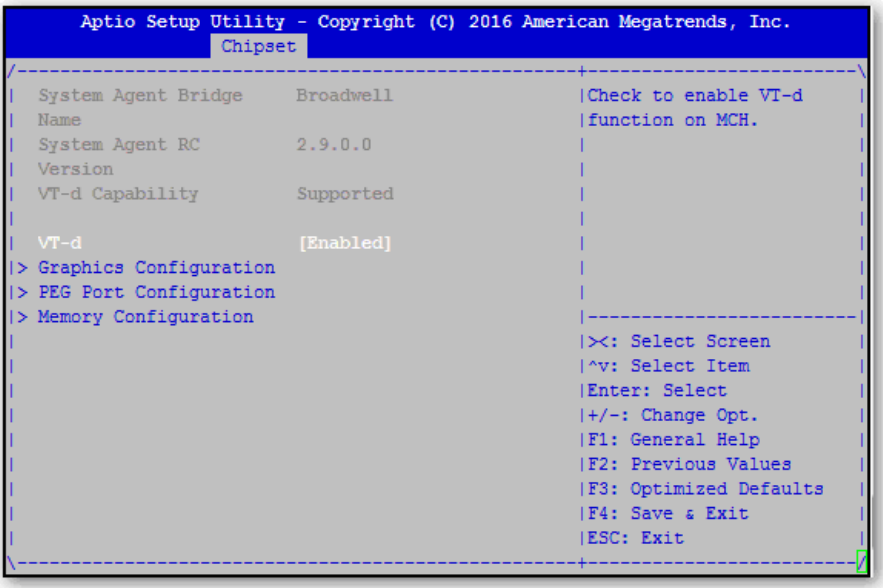
8.4 Chipset Setup

Select the Chipset tab from the setup screen to enter the Chipset BIOS Setup screen. You can select any of Chipset BIOS Setup options by highlighting it using the < Arrow > keys. The Chipset BIOS Setup screen is shown below.



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8.4.1 System Agent (SA) Configuration

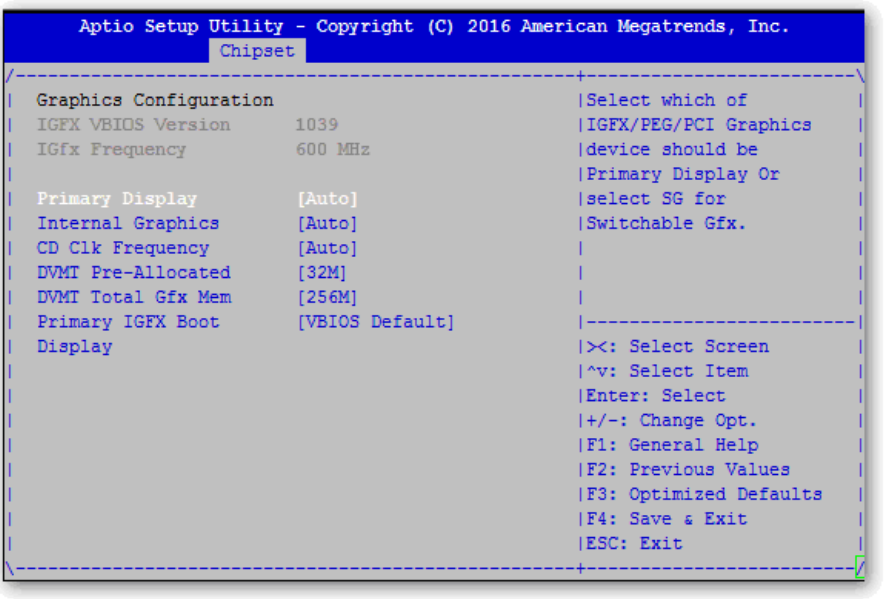


VT-d

The Intel Virtualization Technology for Directed I/O. Set this value to Enabled/Disabled.

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Graphics Configuration



Primary Display

Select which graphics device should be the primary display. Set this value to Auto, IGFX, PCI.

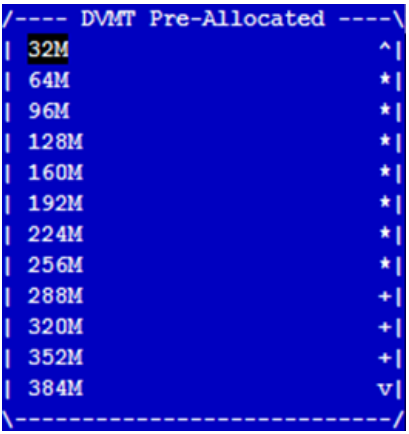
Internal Graphics

Keep IGD enabled based on the setup options. Set this value to Auto, Enabled, Disabled.

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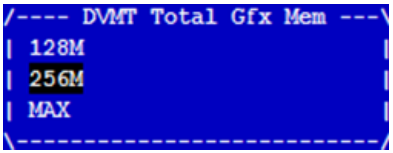
DVMT Pre-Allocated

Select DVMT 5.0 Pre-Allocated (fixed) graphics memory size used by the internal graphics device. Configuration options as below:



DVMT Total Gfx Memory

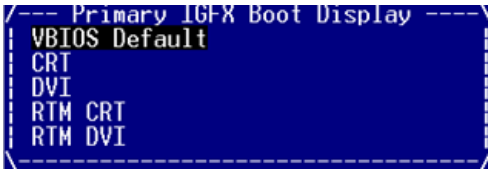
Select DVMT 5.0 total graphic memory size used by the internal graphics device. Configuration options as below:



Primary IGFX Boot Display

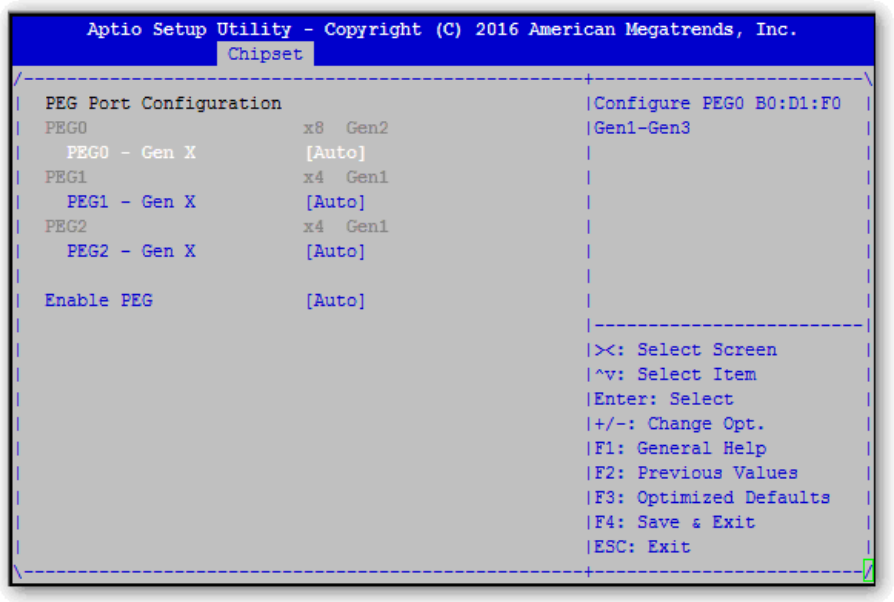
Select Boot Video Device during POST

- ▷ VBIOS Default: auto-detect video device by vBIOS.
- ▷ CRT/DVI/RTM CRT/RTM DVI: force to boot with selected video device.



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PEG Port Configuration



PEG0 - Gen X

XMC PEG (PEX8624, PCIe x8): Bus:0 Device:1 Function:0

Available options: Auto, Gen1, Gen2, Gen3

PEG1 - Gen X

PMC PEG (PI7C9X130 PCIe x4): Bus:0 Device:1 Function:1

Available options: Auto, Gen1, Gen2, Gen3

PEG2 - Gen X

J1/J2 PEG (PI7C9X130 PCIe x4): Bus:0 Device:1 Function:2

Available options: Auto, Gen1, Gen2, Gen3

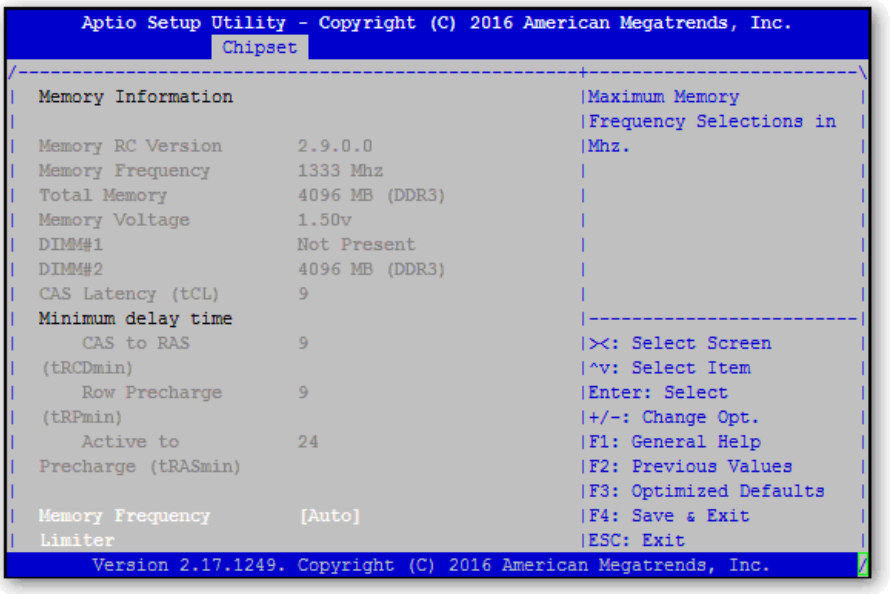
Enable PEG

Enable or disable the PEG port.

Available options: Auto, Gen1, Gen2, Gen3

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Memory Configuration

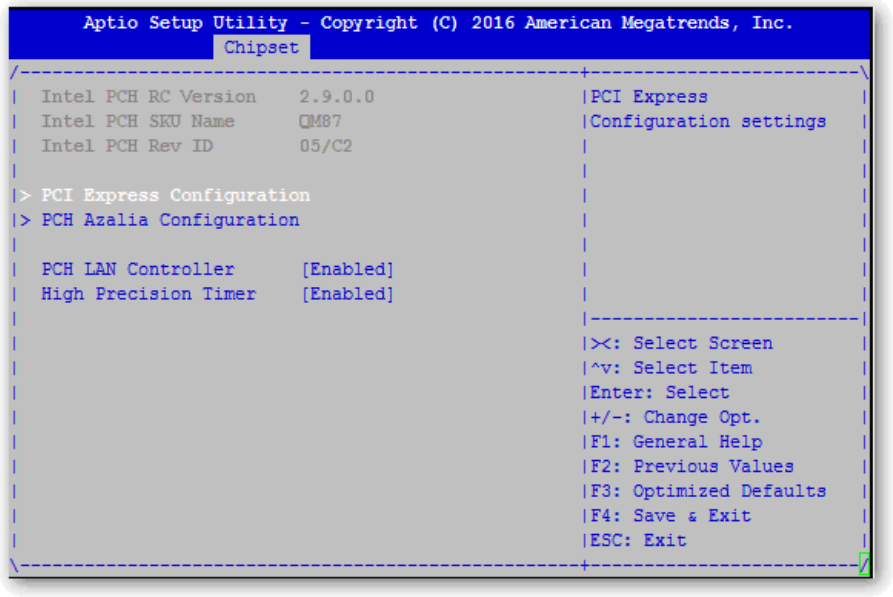


Memory Frequency Limiter

Maximum memory frequency selections in MHz.

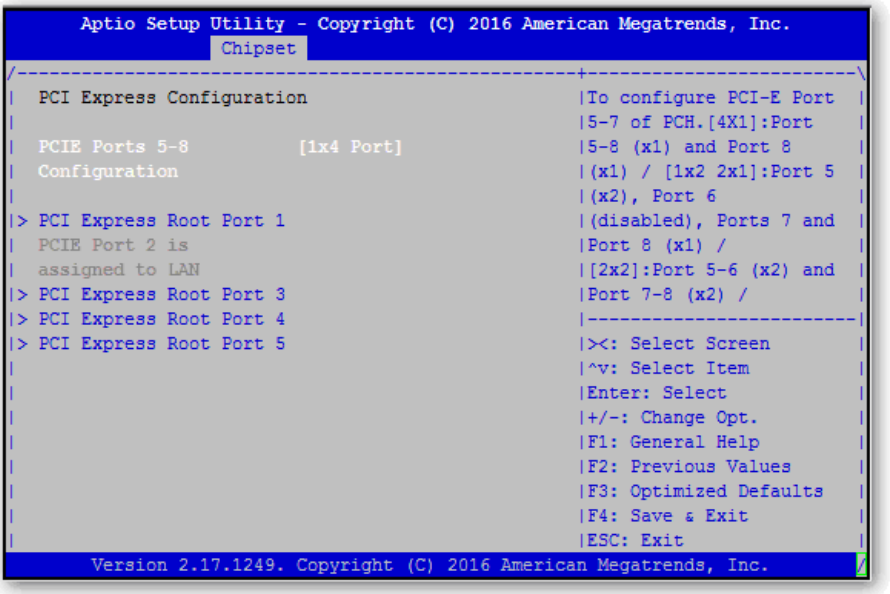
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8.4.2 PCH-IO Configuration



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PCI Express Configuration

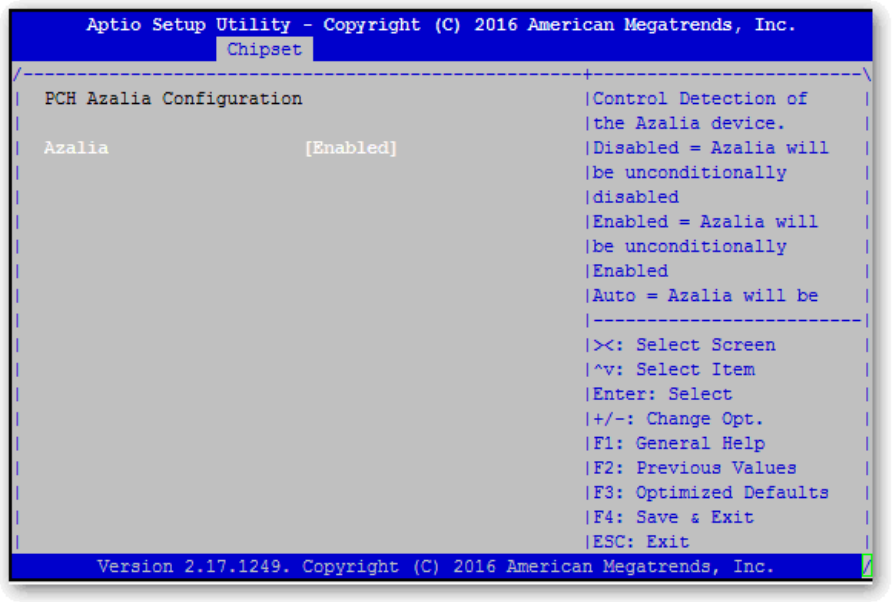


PCI Express Root Port 5-8

Configuration the PCI Express Root Ports 5-8

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PCH Azalia Configuration



Azaila

Enable/Disable the Azalia device.

- ▷ **Disabled:** Azalia will be unconditionally disabled
- ▷ **Enabled:** Azalia will be unconditionally Enabled
- ▷ **Auto:** Azalia will be enabled if present, disabled otherwise.

PCH LAN Controller

Enable/Disable the PCH LAN Controller.

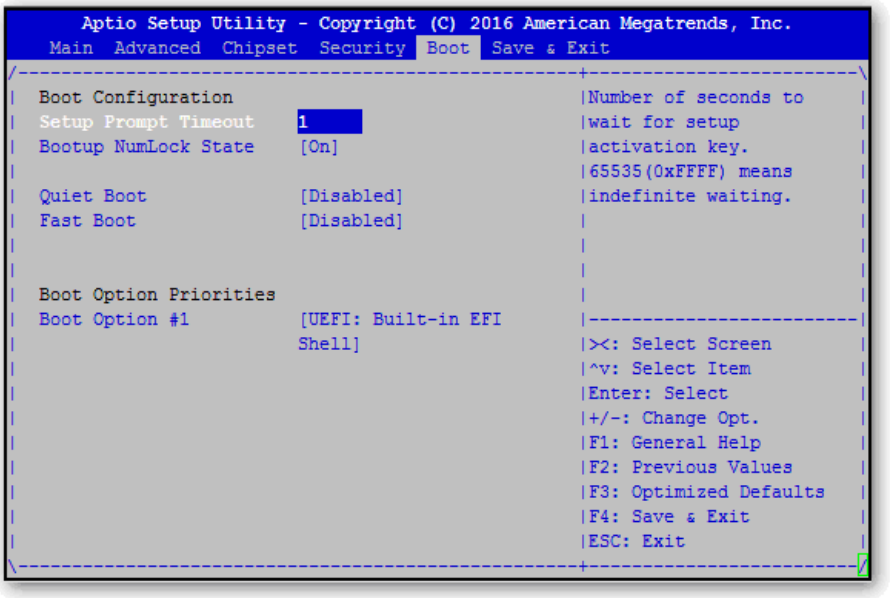
High Precision Timer

Enable/Disable the High Precision Event Timer.

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8.5 Boot Settings

Select the Boot tab from the setup screen to enter the Boot BIOS Setup screen. You can select any of the items in the left frame of the screen, such as Boot Device Priority, to go to the sub menu for that item. You can display a Boot BIOS Setup option by highlighting it using the < Arrow > keys. The Boot Settings screen is shown below:



Quiet Boot

- **Disabled** - Set this value to allow the computer system to display the POST messages.
- **Enabled** - Set this value to allow the computer system to display the OEM logo.

Fast Boot

Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options. Set this value to Enabled/Disabled.

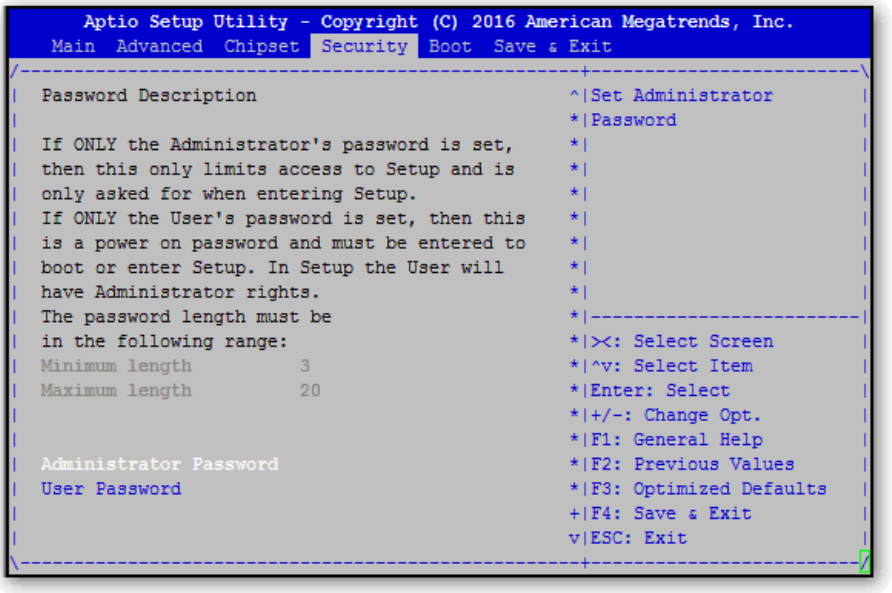
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Set Boot Priority

Set Boot Option #1 ~2 boot priority.

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8.6 Security Setup



Administrator, User Password

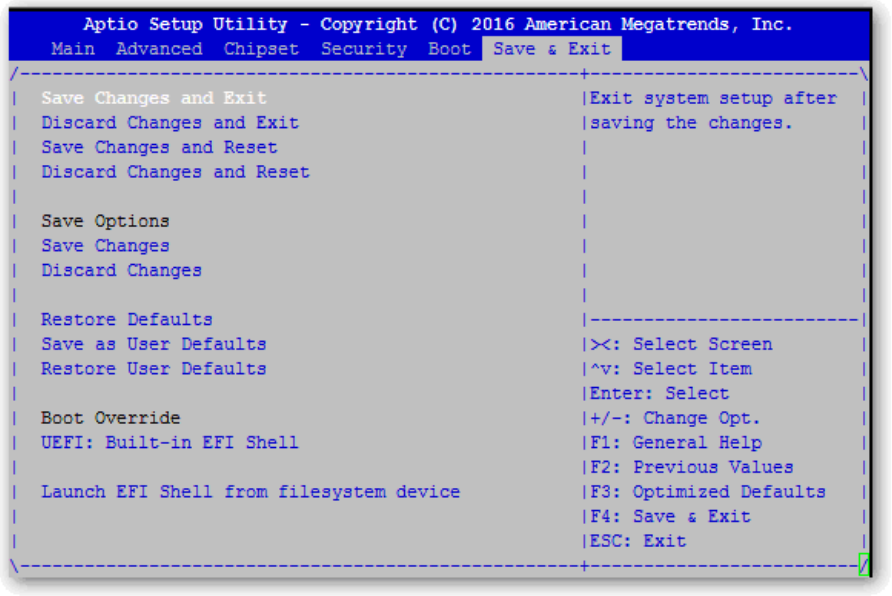
If only the administrator's password is set, then this only limits access to setup and is only asked for when entering setup.

If only the user's password is set, then this is a power on password and must be entered to boot or enter setup. In setup the user will have administrator rights.

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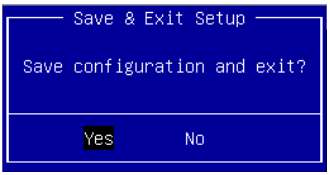
8.7 Save & Exit Menu

Select the Save & Exit tab from the setup screen to enter the Save & Exit BIOS Setup screen. You can display an Exit BIOS Setup option by highlighting it using the < Arrow > keys. The Save & Exit BIOS Setup screen is shown below.



Save Changes and Exit

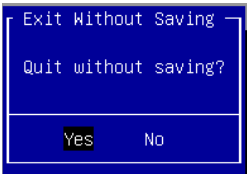
Exit the system after saving the changes.



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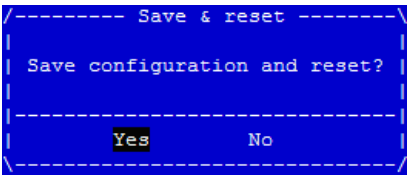
Discard Changes and Exit

Exit system setup without saving any changes.



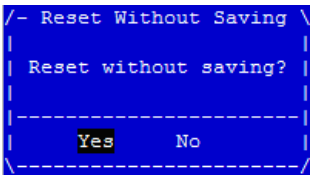
Save Changes and Reset

Reset the system after saving the changes.



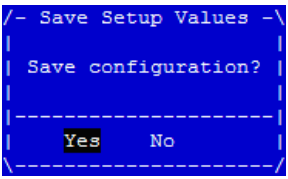
Discard Changes and Reset

Reset system setup without saving any changes.



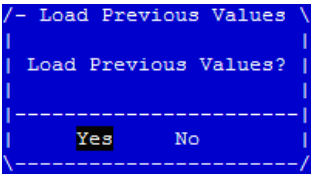
Save Changes

Save changes done so far to any of the setup options.



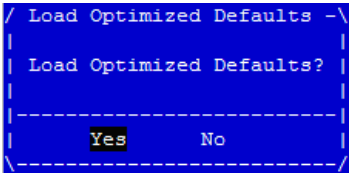
Discard Changes

Discard changes done so far to any of the setup options.



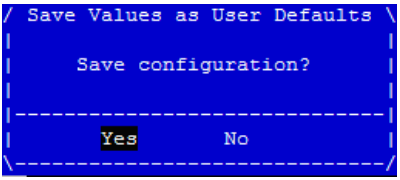
Restore Defaults

Restore/Load Defaults values for all the setup options.



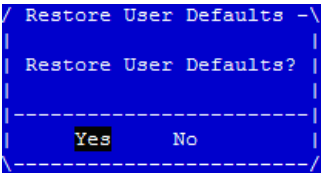
Save as User Defaults

Save the changes done so far as user defaults..



Restore User Defaults

Save changes done so far to any of the setup options.



9 Checkpoints & Beep Codes

The eight GP LEDs on the front panel display port 80h POST codes in hexadecimal during boot up. Users can use the POST codes to identify issues during the BIOS POST process (see See “General Purpose LEDs” on page 23.).

Below are the BIOS checkpoints and beep codes for the cPCI-6530BL. For assistance interpreting these codes, please login to **http://askanexpert.adlinktech.com**.

9.1 Checkpoint Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

9.2 Standard Checkpoints

SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).

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Status Code	Description
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization
SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

SEC Beep Codes

None

PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started

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Status Code	Description
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started

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Status Code	Description
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes

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Status Code	Description
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

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PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

DXE Phase

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)

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Status Code	Description
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes

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Status Code	Description
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error

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Status Code	Description
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

DXE Beep Codes

# of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

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ACPI/ASL Checkpoints

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

9.3 OEM-Reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

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10 IPMI User Guide

10.1 Introduction

This chapter is written for those who already have a basic understanding of the newest implementation of the baseboard management controller (BMC) of the Intelligent Platform Management Interface (IPMI) specification rev. 2.0. It also describes the OEM extension IPMI command usages which are not listed in the IPMI specification.

10.2 Summary of Commands Supported by BMR-AVR-cPCI

The table below lists all the commands supported by the IPMC. The right most column indicates if a particular command is mandatory or optional for PICMG 3.0/2.9.

Command	IPMI Spec	NetFn	CMD	Description (Required by PICMG 3.0/2.9)
IPM Device "Global" Commands				
Get Device ID	20.1	App	01h	This command is used to retrieve the Intelligent Device's Hardware Revision, Firmware/Software Revision, and Sensor and Event Interface Command specification revision information.
Cold Reset	20.2	App	02h	This command directs the Responder to perform a 'Cold Reset' of itself. (Optional/Optional)
Warm Reset	20.3	App	03h	This command directs the Responder to perform a 'Warm Reset' of itself.
Get Self Test Results	20.4	App	04h	This command directs the device to return its Self Test results, if any. (Mandatory/Mandatory)

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Command	IPMI Spec	NetFn	CMD	Description (Required by PICMG 3.0/2.9)
Get Device GUID	20.8	App	08h	This command returns a GUID (Globally Unique ID), also referred to as a UUID (Universally Unique IDentifier), for the management controller. (Optional/Optional)
Broadcast "Get Device ID"	20.9	App	01h	This is a broadcast version of the 'Get Device ID' command that is provided for the 'discovery' of Intelligent Devices on the IPMB. (Mandatory/Mandatory)
IPMI Messaging Support Commands				
Send Message	22.7	App	34h	The *Send Message* command is used for bridging IPMI messages between channels, and between the system management software (SMS) and a given channel. (Optional/Optional)
BMC Watchdog Timer				
Reset Watchdog Timer	27.5	App	22h	The *Reset Watchdog Timer* command is used for starting and restarting the Watchdog Timer from the initial countdown value that was specified in the *Set Watchdog Timer* command. (Mandatory/Optional)
Set Watchdog Timer	27.6	App	24h	The *Set Watchdog Timer* command is used for initializing and configuring the watchdog timer. The command is also used for stopping the timer. (Mandatory/Optional)
Get Watchdog Timer	27.7	App	25h	This command retrieves the current settings and present countdown of the watchdog timer. (Mandatory/Optional)
Event Commands				
Set Event Receiver	29.1	S/E	00h	This global command tells a controller where to send Event Messages. (Mandatory/Optional)

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Command	IPMI Spec	NetFn	CMD	Description (Required by PICMG 3.0/2.9)
Get Event Receiver	29.2	S/E	01h	This global command is used to retrieve the present setting for the Event Receiver Slave Address and LUN. This command is only applicable to management controllers that act as IPMB Event Generators. (Mandatory/Optional)
Platform Event Message	29.3	S/E	02h	This command may be thought of as a request for the BMC to process the event data that the command contains. Typically, the data will be logged to the System Event Log (SEL). (Mandatory/Optional)
Sensor Device Commands				
Get Device SDR Info	35.2	S/E	20h	This command returns general information about the collection of sensors in a Dynamic Sensor Device. (Mandatory/Optional)
Get Device SDR	35.3	S/E	21h	The 'Get Device SDR' command allows SDR information for sensors for a Sensor Device (typically implemented in a satellite management controller) to be returned. (Mandatory/Optional)
Reserve Device SDR Repository	35.4	S/E	22h	This command is used to obtain a *Reservation ID*. (Mandatory/Optional)
Set Sensor Hysteresis	35.6	S/E	24h	This command provides a mechanism for setting the hysteresis values associated with the thresholds of a sensor that has threshold based event generation. (Optional/Optional)
Get Sensor Hysteresis	35.7	S/E	25h	This command retrieves the present hysteresis values for the specified sensor. (Optional/Optional)
Set Sensor Threshold	35.8	S/E	26h	This command is used to set the specified threshold for the given sensor. (Optional/Optional)
Get Sensor Threshold	35.9	S/E	27h	This command retrieves the threshold for the given sensor. (Optional/Optional)

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Command	IPMI Spec	NetFn	CMD	Description (Required by PICMG 3.0/2.9)
Set Sensor Event Enable	35.10	S/E	28h	This command provides the ability to disable or enable Event Message Generation for individual sensor events. The command is also used to enable or disable sensors in their entirety using the *disable scanning* bit. (Optional/Optional)
Get Sensor Event Enable	35.11	S/E	29h	This command returns the enabled/ disabled state for Event Message Generation from the selected sensor. The command also returns the enabled/ disabled state for scanning on the sensor. (Optional/Optional)
Get Sensor Event Status	35.13	S/E	2Bh	The Get Sensor Event Status command is provided to support systems where sensor polling is used in addition to, or instead of, Event Messages for event detection. (Optional/Optional)
Get Sensor Reading	35.14	S/E	2Dh	This command returns the present reading for sensor. The sensor device may return a stored version of a periodically updated reading, or the sensor device may scan to obtain the reading after receiving the request. (Mandatory/Optional)
Get Sensor Type	35.16	S/E	2Fh	This command is used to assign the Sensor Type and Event/Reading Type to a specified sensor. (Optional/Optional)
FRU Device Commands				
Get FRU Inventory Area Info	34.1	Storage	10h	Returns overall the size of the FRU Inventory Area in this device, in bytes. (Mandatory/Optional)
Read FRU Data	34.2	Storage	11h	The command returns the specified data from the FRU Inventory Info area. (Mandatory/Optional)
Write FRU Data	34.3	Storage	12h	The command writes the specified byte or word to the FRU Inventory Info area. (Mandatory/Optional)

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10.3 CompactPCI Address Map

Since more than one system may be installed in a single chassis, we allocate each IPMB address based on GA input as peripheral cards. The CompactPCI Peripheral Address Mapping Table is given below.

CompactPCI Peripheral Address Mapping			
Geo. Addr.	**IPMB Addr.**	**Geo. Addr.**	**IPMB Addr.**
0	**Disabled**	16	D0h
1	B0h	17	D2h
2	B2h	18	D4h
3	B4h	19	D6h
4	B6h	20	D8h
5	B8h	21	DAh
6	Bah	22	DCh
7	BCh	23	DEh
8	BEh	24	E0h
9	Coh	25	E2h
10	C4h	26	E4h
11	C6h	27	E6h
12	C8h	28	E8h
13	CAh	29	EAh
14	CCh	30	ECh
15	CEh	**31**	**Disabled**

10.4 Communications with IPMC

Operating systems need to use a serial port to communicate with the IPMC. The resource setting of the serial port must be IO: 0x2F0 and IRQ: 7. The communication setting of the serial port must be BaudRate: 9600, DataBit: 8, ParityCheck: None, StopBit: 1, and FlowControl: None. In Windows XP, use "COM6" to communicate with the IPMC.

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10.5 IPMI Sensors List

Sensor Number	Sensor name	Normal Reading	Sensor Reading Value of IPMI Get Sensor Reading Command
01h	BMC Watchdog		Timeout action: 000b = no action 001b = Hard Reset 000b = Power Down 011b = Power Cycle 100b - 111b = reserved
02h	3.3V	3.3 V	Raw data of 3.3V sensor
03h	5V	5 V	Raw data of 5.0V sensor
04h	12V	12 V	Raw data of 12.0V sensor
05h	CPU Temp	40ºC	Raw data of CPU Temp sensor
06h	SYSTEM Temp	25ºC	Raw data of SYSTEM Temp sensor

10.6 Relevant Documents

Document Title	Revision	Source
Intelligent Platform Management Interface Specification v2.0	Document Revision 1.0 February 12, 2004	Intel Corp. http://www.intel.com/design/servers/ipmi/spec.htm
PICMG 2.9 D1.0 CompactPCI System Management Specification	January 21, 2000	
Intelligent Platform Management Bus Communications Protocol Specification v0.9	Document Revision 0.15 June 24, 1997	Intel Corp. http://www.intel.com/design/servers/ipmi/license_ipmi.htm

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Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

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- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

A Lithium-type battery may be provided for uninterrupted, backup or emergency power.



Risk of explosion if battery is replaced with one of an incorrect type. Dispose of used batteries appropriately.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

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Getting Service

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