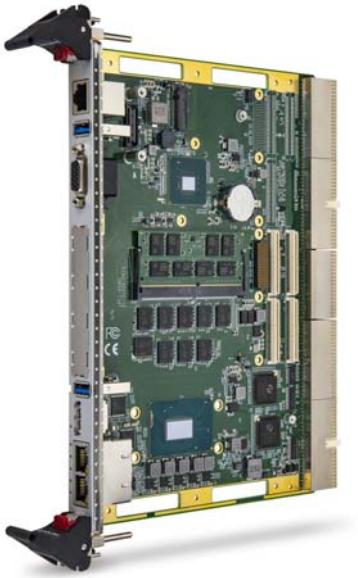
cPCI-6540 Series

Performance 6U CompactPCI®
Intel® Xeon®, Core™ i7/i3 Processor Blade

User's Manual



Manual Rev.: 1.4

Revision Date: July 14, 2023

Part Number: 50M-31426-1040

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Revision History

Revision	Release Date	Description of Change(s)
1.0	2022-04-20	Initial release
1.1	2022-04-21	Update M.2 module specification
1.2	2022-07-11	Correct COM specification and WDT info; update OS and EMI specifications
1.3	2022-09-13	Correct JN1 -12V power specification
1.4	2023-07-24	Update ECC info; add power consumption data Previous revision: P/N 50M-00038-1030

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Preface

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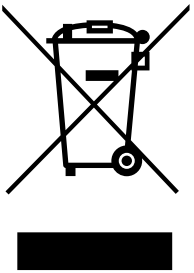
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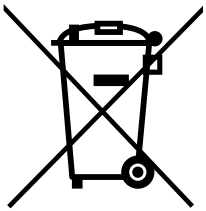
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Battery Labels (for products with battery)









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California Proposition 65 Warning

WARNING: This product can expose you to chemicals including acrylamide, arsenic, benzene, cadmium, Tris(1,3-dichloro-2-propyl)phosphate (TDCPP), 1,4-Dioxane, formaldehyde, lead, DEHP, styrene, DINP, BBP, PVC, and vinyl materials, which are known to the State of California to cause cancer, and acrylamide, benzene, cadmium, lead, mercury, phthalates, toluene, DEHP, DIDP, DnHP, DBP, BBP, PVC, and vinyl materials, which are known to the State of California to cause birth defects or other reproductive harm. For more information go to www.P65Warnings.ca.gov**.**

Trademarks

Product names mentioned herein are used for identification purposes only and may be trademarks and/or registered trademarks of their respective companies.

Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

NOTE: Additional information, aids, and tips that help users perform tasks.

CAUTION: Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

WARNING: Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

1.1 Overview

The ADLINK cPCI-6540 Series is a 6U CompactPCI® processor blade with soldered DDR4-2666 memory up to 32GB and DDR4-2666 socket type memory up to 32GB. The ADLINK cPCI-6540 features an Intel® Xeon® E and 9th Gen Intel® Core™ (formerly Coffee Lake-H) with Mobile Intel® CM246 Chipset.

The cPCI-6540 Series is a 6U CompactPCI blade in single-slot (4HP) width form factor. Front panel I/O for the cPCI-6540 includes 1x DP, 2x GbE, 2x USB 3.1 ports, 1x RJ-45 COM port, 1x VGA and 1x PCM/XMC slot. The cPCI-6540V front panel includes 1x DP, 2x GbE, 1x USB 3.1 port and 2x PMC/XMC slots.

Graphics support is integrated on the CPU and supports 3 independent displays when mated with selected rear transition modules (cPCI-R6700 and cPCI-R6500). Storage for both cPCI-6540V and cPCI-6540 versions includes an M.2 socket (M key) and a SATA connector with adapter board (DB-LSATA).

For expansion, both cPCI-6540 and cPCI-6540V are equipped with one 64-bit/33, 66,133MHz PMC site or one PCIe x8 Gen 2 XMC site with rear I/O. The cPCI-6540V is equipped with one additional PMC/XMC slot supporting PCI 64-bit/33,66,133MHz PMC site or one PCIe x8 Gen 2 XMC site.

Rear I/O signals to RTM include 2x GbE by Intel® Ethernet Controller I210, 1x DVI-I, 1x eDP, 1x PCIe x4 (configurable to 4x PCIe x1), 3x SATA 3.0, 6x USB 2.0, 1x USB 3.1, 16x GPIO, high definition audio, KB/MS, and 2x serial ports (one supports Tx/Rx only).

The cPCI-6540 Series offers outstanding performance provided by Intel® Xeon® E, 9th Gen Intel® Core™ processor family, and is an ideal solution for military, aerospace, transportation and other industrial applications that require best value per watt computing power. The ADLINK cPCI-6540 Series provides higher flexibility, supporting operation in peripheral slots with CompactPCI bus communication (Universal mode) and as a standalone computer if there is no CPU blade in the host slot. Internet remote manageability includes IPMI for system health monitoring over Internet and a GbE port on the faceplate supports Intel® AMT 9.0 for remote monitoring.

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1.2 Features

- 6U CompactPCI blade in 4HP width form factor
- Intel® Xeon® E, 9th Gen Intel® Core™and Mobile Intel® CM246 Chipset
- Graphics and memory controllers integrated in processor
- One channel DDR4-2666 soldered onboard memory up to 32GB and one channel DDR4-2666 socket memory up to 32GB (total 64GB). ECC support dependent on CPU.
- 64bit/66MHz CompactPCI Interface based on PCI specifications, universal V(I/O)
- Supports Universal mode operation as a slave in peripheral slots and operation as a standalone computer if no CPU blade in host slot
- One 64-bit/33,66,133MHz PMC or PCIe x8 Gen2 XMC site on cPCI-6540 with rear I/O; one additional PMC/XMC site on cPCI-6540V
- Supports IPMI over LAN for system health monitoring
- DisplayPort and VGA port port on front panel, additional DVI-I and eDP routed to rear
- Two PCIe Gigabit Ethernet egress ports supported by Intel LAN controller on front panel, one supports Intel® AMT 9.0 by Intel® Ethernet Controller I210 (PHY)
- Two additional PCIe Gigabit Ethernet by Intel® Ethernet Controller I210 routed to J2 (PICMG 2.16 compliant)
- Additional two Gigabit Ethernet ports with selected rear transition module (cPCI-R6100 Series)
- High definition audio routed to RTM
- 2.5" SATA SSD supported on cPCI-6540 only
- M.2 SATA SSD supported on both cPCI-6540 and cPCI-6540V
- Optional Infineon SLB9665XT2.0 TPM support

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1.3 Package Contents

The cPCI-6540 is packaged with the following components. If any of the following items are missing or damaged, retain the shipping carton and packing material and contact the dealer for inspection. Please obtain authorization before returning any product to ADLINK. The packing contents of cPCI-6540 Series non-standard configurations will vary depending on customer requests.

CPU module

- The cPCI-6540 Series Processor Blade
  - CPU and memory specifications will differ depending on options selected
  - Thermal module is assembled on the board
- RJ-45 to DB-9 COM adapter cable (cPCI-6540)
- 2.5” SATA drive accessory pack

Rear Transition Module

- Dependent on the module selected


NOTE:

The contents of non-standard cPCI-6540 configurations may vary depending on the customer’s requirements.


CAUTION:

This product must be protected from static discharge and physical shock. Never remove any of the components except at a static-free workstation. Use the anti-static bag shipped with the product when putting the board on a surface. Wear an anti-static wrist strap properly grounded on one of the system's ESD ground jacks when installing or servicing system components.

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2 Specifications

2.1 cPCI-6540 Processor Blade Specifications

CompactPCI® Standards	• PICMG® 2.0 CompactPCI® Rev. 3.0 • PICMG® 2.1 Hot Swap Specification Rev. 2.0 • PICMG® 2.9 System Management (IPMI Rev. 1.5) • PICMG® 2.16 Packet Switching Backplane Rev. 1.0
Mechanical	• Standard 6U CompactPCI® • Board size: 233mm x 160mm • Single slot (4HP, 20.32mm) • CompactPCI® connectors: J1, J2, J3, J4, J5
Processor	• Intel® Xeon® E-2276ME processor, 6 cores/12 threads, 12MB cache, 45/35W by cTDP, Intel® UHD Graphic P630 • Intel® Core™ i7-9850HE processor, 6 cores/12 threads, 9MB cache, 2.7/4.4GHz, 45/35W by cTDP, Intel® UHD Graphics 630 • Intel® Core™ i7-9850HL Processor, 6 cores/12 threads, 9MB cache, 1.9/4.1GHz, 25W, Intel® UHD Graphics 630 • Intel® Core™ i3-9100HL processor, 4 cores/4 threads, 6MB cache, 1.6/2.9GHz, 25W, Intel® UHD Graphics 630 • Intel® Celeron® G4930E processor, 2 cores/2 threads, 2MB cache, 2.4GHz, 35W, Intel® UHD Graphics 610
Chipset	• Mobile Intel® CM246 Chipset
Memory	• Dual channel up to DDR4-2666 memory • One channel DDR4 soldered up to 32GB • One channel SODIMM socket memory up to 32GB • DRAM configuration 64GB/32GB/16GB/8GB • ECC supported by Intel® Xeon® E-2276ME, Intel® Core™ i3-9100HL and Intel® Celeron® G4930E
CompactPCI Bus	• PCI 64-bit/66MHz; 3.3V, 5V universal V I/O • Supports operation in system slot as master or in peripheral slot with connectivity to CompactPCI bus (Universal mode) • Supports operation in peripheral slot as standalone CPU board when no host blade in host slot
Gigabit Ethernet	• Four PCIe x1 Intel® I210 Gigabit Ethernet controllers • Two egress 10/100/1000BASE-T ports on front panel, one supporting NCSI • Two egress 10/100/1000BASE-T ports routed to rear transition module supporting PICMG 2.16

Table 2-1: cPCI-6540 Processor Blade Specifications

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Graphics	• Intel® Xeon® E-2276ME: Intel® UHD Graphics P630 • Intel® Core™ i7-9850HE: Intel® UHD Graphics 630 • Intel® Core™ i7-9850HL: Intel® UHD Graphics 630 • Intel® Core™ i3-9100HL: Intel® UHD Graphics 630 • Intel® Celeron® G4930E: Intel® UHD Graphics 610 • One VGA port and one DP port on front panel • One VGA port routed to rear J3, and one TMDS port routed to rear J5
Serial Ports	• Up to three serial ports • One RS-232/422/485 serial port on front panel (cPCI-6540) • Up to two RS-232 COM port routed to RTM (one port supports RS-232 Tx/Rx only)
USB	• One USB 3.0 to rear J5 • Up to six USB 2.0 ports routed to rear transition module • Two USB 3.1 Gen2 on front panel
PMC/XMC	• One 64-bit/33,66,133 MHz PMC site or PCIe x8 Gen 2 XMC site for cPCI-6540V version with rear I/O • Two 64-bit/33,66,133 MHz PMC sites or PCIe x8 Gen 2 XMC sites on cPCI-6540 version
Audio	• High definition audio routed to rear J3
TPM	TPM 2.0 • SLB9665XT2.0 FW 5.51
Storage Interfaces[1]	• One onboard 2.5” SATA connector supporting SATA 6Gb/s drive on cPCI-6540 • One PCIe x4 M.2 • Three SATA 6Gb/s channels routed to RTM
Faceplate I/O	cPCI-6540 (4HP) • 2x 10/100/1000BASE-T Ethernet ports • 1x DP port • 1x VGA port • 2x USB 3.1 ports • 1x RJ-45 serial port • 1x PMC/XMC slot cPCI-6540V (4HP) • 2x 10/100/1000BASE-T Ethernet ports • 1x DP port • 1x USB 3.1 port • 2x PMC/XMC slots
OS Compatibility	• Ubuntu desktop 20.04 LTS (Focal Fossa) 64-bit • Windows 10 Enterprise 2004 64-bit Please contact ADLINK for other OS support

Table 2-1: cPCI-6540 Processor Blade Specifications

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Environmental	• Operating Temperature (with forced air flow)[2]: Standard: -20°C to +70°C Extreme temperature: -40°C to +85°C • Storage Temperature: -50°C to 100°C • Humidity: 95% @60°C non-condensing • Shock: 20G peak-to-peak, 11ms duration, non-operating • Vibration[1]: 2Grms, 5-500Hz, each axis, operating (w/o hard drive)
EMI	• EMC: EN 55032/35 • EMI: CISPR 32, FCC Part 15B Class A • EMS: IEC 61000-4-11 IEC 61000-4-2 ESD: Contact: 4 kV; Air: 8 kV IEC 61000-4-3 RS: 80 MHz to 1 GHz: 10 V/m IEC 61000-4-4 EFT: Power: 2 kV; Signal: 1 kV IEC 61000-4-5 Surge: Power: 2 kV; Signal: 1 kV IEC 61000-4-6 CS: 1 V IEC 61000-4-8 PFM

Table 2-1: cPCI-6540 Processor Blade Specifications

1. The storage device limits the operational vibration tolerance. When the application requires higher specification for anti-vibration, it is recommended to use a flash storage device.
2. ADLINK-certified thermal design. The thermal performance is dependent on the chassis cooling design. Sufficient forced air-flow is required. Temperature limits of optional mass storage devices may also affect the thermal specification.

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2.2 Block Diagrams

cPCI-6540 Processor Blade

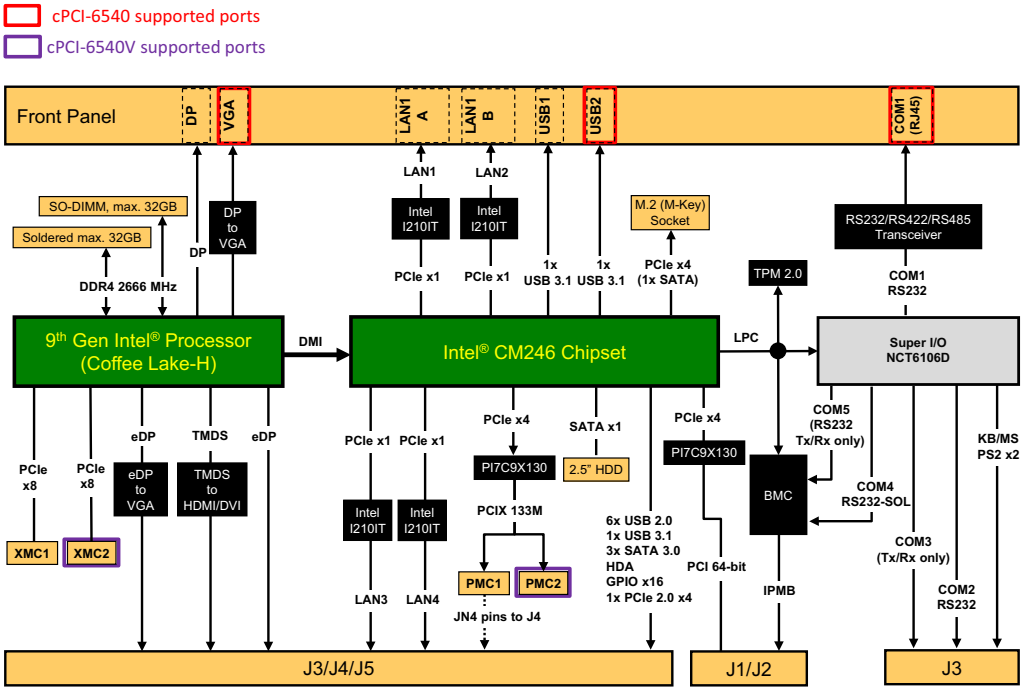


Figure 2-1: cPCI-6540 Processor Blade Functional Block Diagram

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2.3 I/O Connectivity Table

Function	cPCI-6540 (4HP)		cPCI-6540V (4HP)	
	Faceplate	Onboard	Faceplate	Onboard
Gigabit Ethernet	Y x2	–	Y x2	–
COM	Y (RJ-45)	–	–	–
USB 3.1	Y x2	–	Y x1	–
DP	Y x1	–	Y x1	–
VGA	Y x1	–	–	–
Serial ATA	–	Y x1	–	-
M.2	–	Y x1	–	Y x1
PMC/XMC	–	Y x1	–	Y x2
LED	Y x5	–	Y x5	–
Reset Button	Y	–	Y	–

Table 2-2: cPCI-6540 I/O Connectivity

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2.4 Power Requirements

In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. **An industrial power supply unit should be able to provide at least twice as much power as the entire system requires of each voltage**. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires of each voltage.

The tolerance of the voltage lines described in the CompactPCI specification (PICMG 2.0 R3.0) is +5%/-3% for 5, 3.3 V and ±5% for ±12V. This specification is for power delivered to each slot and it includes both the power supply and the backplane tolerance.

Voltage	Nominal Value	Tolerance	Max. Ripple (P - P)
5V	+5.0 VDC	+5% / -3%	50 mV
3.3V	+3.3 VDC	+5% / -3%	50 mV
+12V	+12 VDC	+5% / -5%	240 mV
-12V	-12 VDC	+5% / -5%	240 mV
V I/O (PCI I/O Buffer Voltage)	+3.3 VDC or +5 VDC	+5% / -3%	50 mV
GND			

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Power Consumption

This section provides information on the power consumption of cPCI-6530BL Series when using Intel® Core™ i7-9850HL and Intel® Xeon® E-2276ML processors. Storage device is used with ADLINK ASD26-MT1064-CT 64GB SATA SSD, Windows 10 Enterprise 2004. Power consumption at 100% CPU stress was measured using the Intel Thermal Analysis Tool 6.0.1027 (TAT).

Intel® Core™i7-9850HL (32GB DDR4 soldered, cTDP nominal)					
OS/Mode	**EIST**	**3.3V (A)**	**5V (A)**	**12V (A)**	**Total Power (W)**
Windows Idle mode	enabled	2.07	0.84	0.01	11.15
	disabled	2.07	0.89	0.01	11.40
Windows Typical mode	enabled	2.96	6.56	0.01	42.69
	disabled	2.90	6.40	0.01	41.69
Windows Max mode	enabled	3.18	6.6	0.01	43.61
	disabled	3.07	6.47	0.01	42.60

Intel® Xeon® E-2276ML (16GB DDR4 soldered, cTDP nominal)					
OS/Mode	**EIST**	**3.3V (A)**	**5V (A)**	**12V (A)**	**Total Power (W)**
Windows Idle mode	enabled	2.07	0.82	0.01	11.05
	disabled	2.06	0.82	0.01	11.02
Windows Typical mode	enabled	3.03	6.33	0.11	42.97
	disabled	2.99	6.25	0.01	41.24
Windows Max mode	enabled	3.20	6.51	0.01	43.23
	disabled	3.10	6.43	0.01	42.50

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3 Functional Description

The following sections describe the cPCI-6540 Series features and functions.

3.1 Processors

The Mobile 9th Generation Intel® Core™ Processor FamilyIntel® Xeon® E Processor, and Celeron® Processor G Series are 64-bit, multi-core mobile processor built on14-nanometer process technology. The processor is designed for a two-chip platform consisting of a processor and chipset. The platform enables higher performance, lower cost, easier validation, and improved x-y footprint. The processor includes an Integrated Display Engine, Processor Graphics and Integrated Memory Controller.

The cPCI-6540 Series supports Intel® Core™ i7/i5/i3 processors, Intel® Xeon® E Processor, and Intel® Celeron® Processor G Series. The table below lists the general specifications and power ratings of the CPUs supported by the cPCI-6540 Series.

Features	Xeon® E-2276G	Core™ i7-9850HE	Core™ i3-9100HL	Celeron® G4930E
Clock	3.8 Hz	2.7GHz	1.6GHz	2.4GHz
Max. Single Core Turbo Freq.	4.9GHz	4.4GHz	2.9GHz	2.4GHz
Last Level Cache	12MB	9MB	6MB	2MB
No. of Core(s)	6/12	6/12	4/4	2/2
Max. Power (TDP[1])	80W	45W	25W	35W
DMI	8 GT/s	8 GT/s	8 GT/s	8 GT/s
$T_{junction, MAX}$[2]	100°C	100°C	100°C	100°C

1. The highest expected sustainable power while running known power intensive applications. TDP is not the maximum power that the processor can dissipate.
2. The maximum temperature allowed at the processor die.

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Supported Technologies

Features	Xeon® E-2276G	Core™ i7-9850HE	Core™ i3-9100HL	Celeron® G4930E
Intel® Virtualization Technology for Directed I/O (Intel® VT-d)	Yes	Yes	Yes	Yes
Intel® Virtualization Technology (Intel® VT-x)	Yes	Yes	Yes	Yes
Intel® VT-x with Extended Page Tables (EPT)	Yes	Yes	Yes	Yes
Intel® Hyper-Threading Technology	Yes	Yes	No	No
Intel® 64 Architecture	Yes	Yes	Yes	Yes
Execute Disable Bit	Yes	Yes	Yes	Yes
Intel® Turbo Boost Technology	2.0	2.0	2.0	No
Intel® vPro Technology	Yes	Yes	No	No
Enhanced Intel SpeedStep® Technology	Yes	Yes	Yes	Yes
Thermal Monitoring Technologies	Yes	Yes	Yes	Yes
Intel® Identity Protection Technology	Yes	Yes	Yes	Yes

Interfaces

- Two channels of DDR4-2666 memory (Celeron® G4930 supports DDR-2400 memory)
- Theoretical maximum memory bandwidth of
  - 37.5 GB/s in dual-channel mode assuming 2400 MT/s
  - 41.6 GB/s in dual-channel mode assuming 2666 MT/s
- 64-bit wide channels
- DDR4 I/O voltage of 1.2V
- Standard 4-Gb, 8-Gb technologies and addressing are supported for x8 and x16 devices, 16-Gb technologies and addressing supported for x8 device.
- PCI Express ports are fully-compliant with the PCI Express Base Specification, Revision 3.0.
- 8 GT/s point-to-point DMI interface to chipset is supported

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3.2 Chipset

The Mobile Intel® C240 Series Chipset provides extensive I/O support. Functions and capabilities include:

- PCI Express Base Specification, Revision 3.0
- ACPI Power Management Logic Support, Revision 4.0a
- Interrupt controller and timer functions
- Integrated Serial ATA host controller 3.2, supports data transfer rates up to 6Gb/s on all ports
- XHCI USB 3.1 Controller
- Integrated 10/100/1000 Gigabit Ethernet MAC with System Defense
- System Management Bus (SMBus) Specification, Version 2.0 with additional support for I2C devices
- Supports Intel® High Definition Audio
- Supports Intel® Rapid Storage Technology
- Supports Intel® Virtualization Technology for Directed I/O
- Integrated Clock Controller
- Analog and Digital Display ports
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support
- Serial Peripheral Interface (SPI) support

3.3 PMC/XMC

The cPCI-6540(V) models support up to two PMC or XMC sites for front panel I/O expansion. The PMC site provides a maximum 64-bit/33,66,133 MHz PCI bus link using a Pericom PI7C9X130 PCI-Express-to-PCI bridge and PCI-Express x4 link. The PMC sites support +3.3V signaling only. The XMC sites provide PCI-Express x8 lanes which are supported by a PCIe x8 switch.

3.4 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology is a feature that allows the processor to opportunistically and automatically run faster than its rated operating core and/or render clock frequency when there is sufficient power headroom, and the product is within specified temper-

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ature and current limits. The Intel Turbo Boost Technology feature is designed to increase performance of both multi-threaded and single-threaded workloads. The processor supports a Turbo mode where the processor can use the thermal capacity associated with package and **run at power levels higher than TDP power for short durations**. This improves the system responsiveness for short, bursty usage conditions.

Turbo Mode availability is independent of the number of active cores; however, the Turbo Mode frequency is dynamic and dependent on the instantaneous application power load, the number of active cores, user configurable settings, operating environment, and system design. If the power, current, or thermal limit is reached, the processor will automatically reduce the frequency to stay with its TDP limit.

3.5 Intel® Hyper-Threading Technology

Intel® Hyper-Threading Technology allows an execution core to function as two logical processors. While some execution resources (such as caches, execution units, and buses) are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled using the BIOS and requires operating system support. Intel recommends enabling Hyper-Threading Technology with Microsoft Windows 7 and newer, and disabling Hyper-Threading Technology using the BIOS for all previous versions of Windows operating systems.

3.6 Trusted Platform Module

The cPCI-6540 integrates an Infineon SLB 9665TT2.0 Trusted Platform Module (TPM). The TPM is a secure controller with added cryptographic functionality to provide users a secure environment in e-commerce transactions and Internet communications.

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The key features the Trusted Platform Module (TPM) offers are:

- Compliant to TPM 2.0 Rev. 01.16
- Pin compatible to SLB9660
- Low Pin Count (LPC) to allow easy system integration
- TCG and Common Criteria certified with EAL4+
- FIPS 140-2 certified FW available via FW update
- Full personalization with Endorsement Key (EK) and EK certificate
- 1280 byte I/O buffer.

3.7 Battery

The cPCI-6540(V) is equipped with a 3.0V "coin cell" lithium battery for the Real Time Clock (RTC). The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. A Rayovac BR2032 is equipped on board by default.

3.8 Watchdog Timer

The Watchdog Timer is implemented using the IPMC. The WDT can be configured with IPMI commands (see Section 8.2 Summary of Commands Supported by BMR-AVR-cPCI). For detailed information, please refer to the Intelligent Platform Management Interface Specification v2.0, sections 27.5, 27.6, 27.7 (see Section 8.6 Relevant Documents).

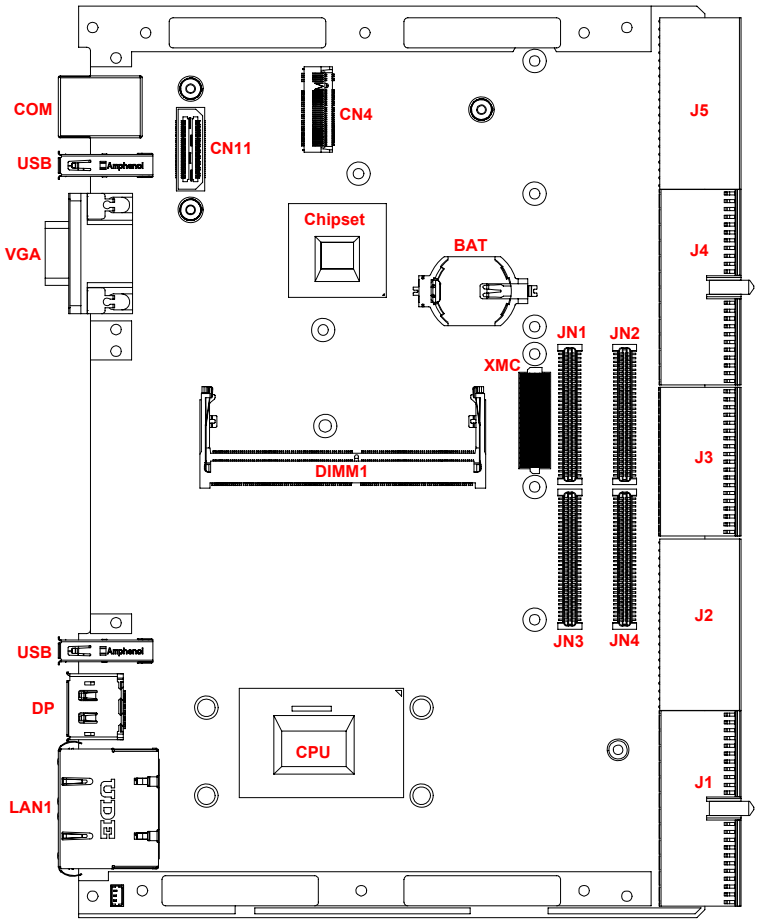
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4 Board Interfaces

4.1 cPCI-6540 Board Layout

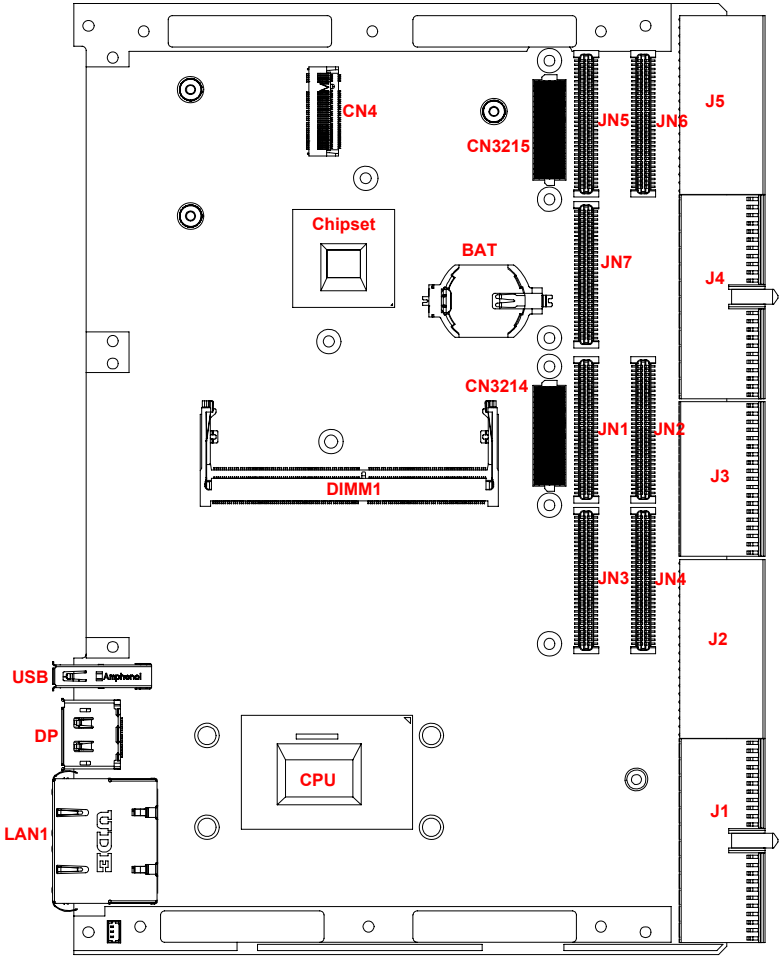


CPU	Intel® Core™ Processor	**J1-J5**	CompactPCI connectors
Chipset	Intel® CM246 PCH	**LAN1**	Dual Ethernet connectors
DIMM1	Memory socket	**CN4**	M.2 connector
DP	Display Port connector	**CN11**	SATA board-to-board conn.
COM	COM port in RJ-45 conn.	**USB**	USB 3.1 connectors
BAT1	Battery socket	**XMC**	XMC Connector
VGA	VGA Connector	**JN1/2/3/4**	PMC connectors

Figure 4-1: cPCI-6540 Series Board Layout

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4.2 cPCI-6540V Board Layout



CPU	Intel® Core™ Processor	**J1-J5**	CompactPCI connectors
Chipset	Intel® CM246 PCH	**LAN1**	Dual Ethernet connectors
DIMM1	Memory socket	**CN4**	M.2 connector
DP	Display Port connector	**CN3214/ CN3215**	XMC Connectors
USB	USB 3.1 connector	**JN1~7**	PMC Connectors
BAT1	Battery socket		

Figure 4-2: cPCI-6540V Series Board Layout

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4.3 cPCI-6540 Series Front Panel

Front Panel Layout

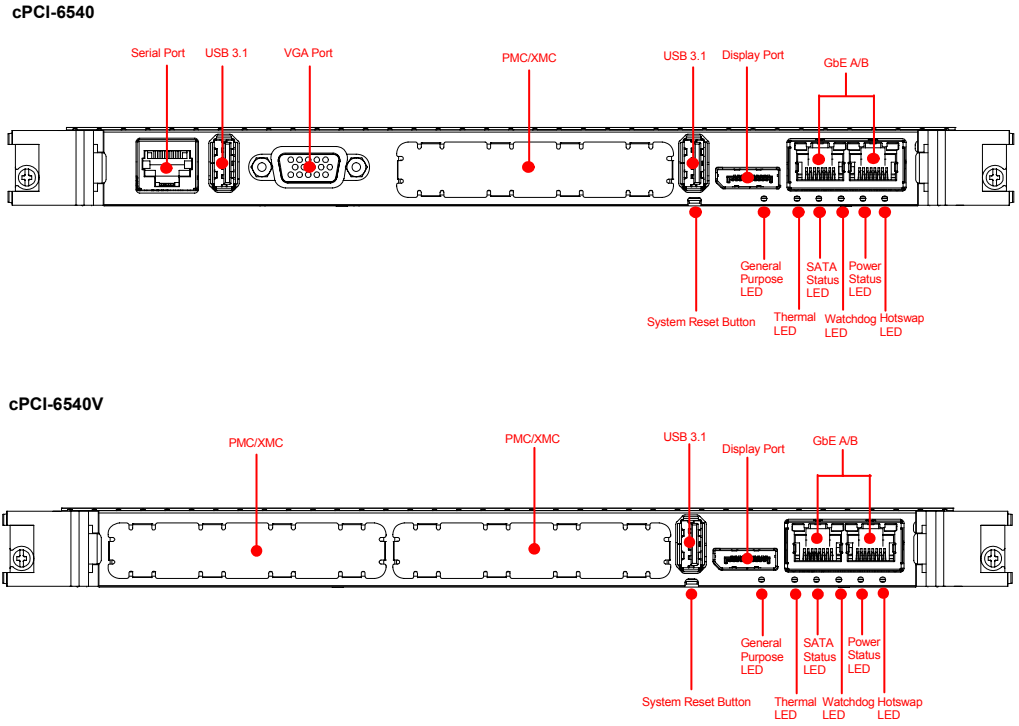


Figure 4-3: cPCI-6540 Series Front Panel Layout

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System LEDs

LED	Color	Condition	Indication
Power Status	Green/ Red	OFF	System is off
		Red	System Power ready (PWGD)
		Green	Post OK
Watchdog	Amber	OFF	No Watchdog event
		Blinking	Watchdog event alert
SATA Status	Blue	OFF	No SATA HDD activity
		Blinking	Data read/write in process for SATA HDD
Hot Swap	Blue	OFF	Handles closed, system is on
		ON	Handles open and blade ready to be removed
Thermal Status	Red	OFF	Normal CPU operating temperature
		Blinking	CPU temperature over 95°C
General Purpose	Yellow	User Defined	Controlled by IPMC

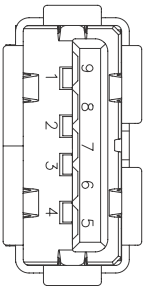
Table 4-1: cPCI-6540 Front Panel System LED Descriptions

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4.4 Connector Pin Assignments

USB 3.1 Connectors

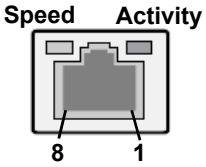
Pin #	Signal Name
1	USB3.0_P5VA
2	USB2_CMAN
3	USB2_CMAP
4	GND
5	USB3A_CMRXN
6	USB3A_CMRXP
7	GND
8	USB3A_CMTXN
9	USB3A_CMTXP



RJ-45 Gigabit Ethernet Connectors

Pin #	10BASE-T/ 100BASE-TX	1000BASE-T
1	TX+	LAN_TX0+
2	TX-	LAN_TX0-
3	RX+	LAN_TX1+
4	—	LAN_TX2+
5	—	LAN_TX2-
6	RX-	LAN_TX1-
7	—	LAN_TX3+
8	—	LAN_TX3-

Table 4-2: RJ-45 GbE Pin Definitions



Status		Speed LED (Green/Orange)	Activity LED (Yellow)
Network link is not established or system powered off		OFF	OFF
10 Mbps	Link	OFF	ON
	Active	OFF	Blinking
100 Mbps	Link	Green	ON
	Active	Green	Blinking
1000 Mbps	Link	Orange	ON
	Active	Orange	Blinking

Table 4-3: LAN LED Status Definitions

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COM (RJ-45)

Pin #	RS-232	RS-422	RS-485
1	DCD#	TX-	Data-
2	RTS#	—	—
3	DSR#	—	—
4	TXD	RX+	—
5	RXD	TX+	Data+
6	GND	—	—
7	CTS#	—	—
8	DTR#L	RX-	—

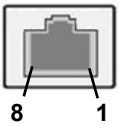


Table 4-4: Front Panel COM Pin Definitions

COM RJ-45 to DB-9 Cable

Pin #	RS-232	RS-422	RS-485
1	DCD#	TX-	Data-
2	RXD	TX+	Data+
3	TXD	RX+	—
4	DTR#L	RX-	—
5	GND	—	—
6	DSR#	—	—
7	RTS#	—	—
8	CTS#	—	—
9	—	—	—

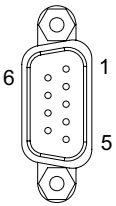


Table 4-5: COM RJ-45 to DB-9 Cable Pin Definitions

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SATA Board-to-Board Connector (CN11)

Signal Name	Pin #	Pin #	Signal Name
GND	1	2	GND
GND	3	4	GND
GND	5	6	GND
GND	7	8	GND
GND	9	10	GND
GND	11	12	GND
GND	13	14	GND
GND	15	16	GND
GND	17	18	GND
GND	19	20	GND
GND	21	22	GND
GND	23	24	GND
GND	25	26	GND
GND	27	28	GND
GND	29	30	GND
NC	31	32	+5V
NC	33	34	+5V
NC	35	36	+5V
NC	37	38	+5V
NC	39	40	+12V
NC	41	42	+12V
NC	43	44	+12V
GND	45	46	GND
GND	47	48	SATA_TXN0
GND	49	50	SATA_TXP0
SATA_RXN0	51	52	GND
SATA_RXP0	53	54	GND
GND	55	56	PLTRST_SATA_L
GND	57	58	GND
GND	59	60	GND

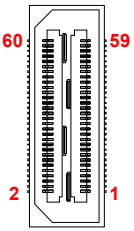


Table 4-6: SATA Board-to-Board Connector Pin Definition

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Serial ATA Connector with Power (from adapter board)

Pin #	Signal
S1	GND
S2	TX+
S3	TX-
S4	GND
S5	RX-
S6	RX+
S7	GND
P1	NC
P2	NC
P3	NC
P4	GND
P5	GND
P6	GND
P7	5V
P8	5V
P9	5V
P10	GND
P11	NC
P12	GND
P13~P15	NC

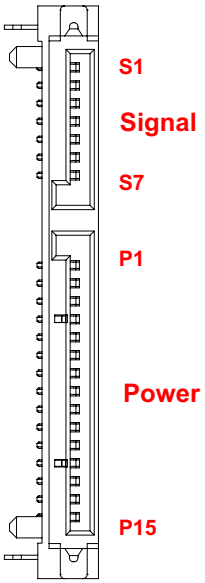
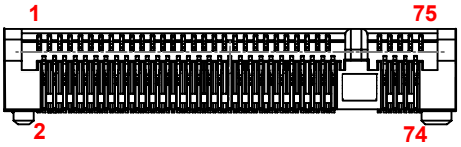


Table 4-7: Serial ATA Connector with Power Pin Definition

M.2 Socket, M-Key (CN4)



Signal Name	Pin #	Pin #	Signal Name
GND	75	74	P3V3
GND	73	72	P3V3
GND	71	70	P3V3
CONFIG	69	68	NC
NC	67		
M-key			
GND	57	58	NC
CLK_M2_100MR_P	55	56	NC
CLK_M2_100MR_N	53	54	NC
GND	51	52	NC
PCIE_M2-0_TXC_P	49	50	PCH_PLTRST-L_M2
PCIE_M2-0_TXC_N	47	48	NC
GND	45	46	NC
PCIE_M2-0_RXR_N	43	44	NC
PCIE_M2-0_RXR_P	41	42	NC
GND	39	40	NC
PCIE_M2-1_TXC_P	37	38	NC
PCIE_M2-1_TXC_N	35	36	NC
GND	33	34	NC
PCIE_M2-1_RXR_P	31	32	NC
PCIE_M2-1_RXR_N	29	30	NC
GND	27	28	NC
PCIE_M2-2_TXC_P	25	26	NC
PCIE_M2-2_TXC_N	23	24	NC
GND	21	22	NC
PCIE_M2-2_RXR_P	19	20	NC
PCIE_M2-2_RXR_N	17	18	P3V3_M2
GND	15	16	P3V3_M2

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Signal Name	Pin #	Pin #	Signal Name
PCIE_M2-3_TXC_P	13	14	P3V3_M2
PCIE_M2-3_TXC_N	11	12	P3V3_M2
GND	9	10	NC
PCIE_M2-3_RXR_P	7	8	NC
PCIE_M2-3_RXR_N	5	6	NC
GND	3	4	P3V3_M2
GND	1	2	P3v3_M2

Table 4-8: M.2 Socket Pin Definition

DisplayPort Connector (CN3212)

Pin #	Signal	Pin #	Signal
1	CN_DP0_P	2	Ground
3	CN_DP0_N	4	CN_DP1_P
5	Ground	6	CN_DP1_N
7	CN_DP2_P	8	Ground
9	CN_DP2_N	10	CN_DP3_P
11	Ground	12	CN_DP3_N
13	CN_CAD-L	14	CN_CEC
15	CN_AUX_P	16	Ground
17	CN_AUX_N	18	DDP_HPD
19	Ground	20	P3V3

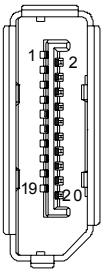
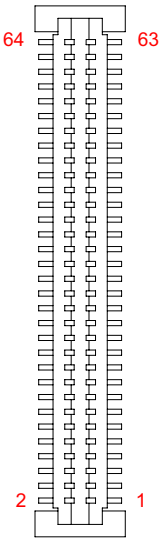


Table 4-9: DisplayPort Connector Definition

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PMC Connector (JN1/5, JN2/6, JN3/7, JN4)

Pin#	JN1/5 Signal	JN2/6 Signal	JN3/7 Signal	JN4 Signal
1	PMC_TCK	+12V	NC	PIO1
2	-12V	PMC_TRST-L	GND	PIO2
3	GND	PMC_TMS	GND	PIO3
4	PCIX_INTA-L	NC (PMC_TDO)	PCIX_CBE-L7	PIO4
5	PCIX_INTB-L	PMC_TDI	PCIX_CBE-L6	PIO5
6	PCIX_INTC-L	GND	PCIX_CBE-L5	PIO6
7	PMC_MOD-L1	GND	PCIX_CBE-L4	PIO7
8	+5V	NC	GND	PIO8
9	PCIX_INTD-L	NC	PMC_VIO	PIO9
10	NC	NC	PCIX_PAR64	PIO10
11	GND	PMC_MOD-L2	PCIX_AD63	PIO11
12	+3.3V AUX	+3.3V	PCIX_AD62	PIO12
13	CLK66_PCIX_PMC	PMC_RST-L	PCIX_AD61	PIO13
14	GND	PMC_MOD-L3	GND	PIO14
15	GND	+3.3V	GND	PIO15
16	PCIX_GNT-L0	PMC_MOD-L4	PCIX_AD60	PIO16
17	PCIX_REQ-L0	PMC_PME-L	PCIX_AD59	PIO17
18	+5V	GND	PCIX_AD58	PIO18
19	PMC_VIO	PCIX_AD30	PCIX_AD57	PIO19
20	PCIX_AD31	PCIX_AD29	GND	PIO20
21	PCIX_AD28	GND	GND	PIO21
22	PCIX_AD27	PCIX_AD26	PCIX_AD56	PIO22
23	PCIX_AD25	PCIX_AD24	PCIX_AD55	PIO23
24	GND	PCIX_AD23	PCIX_AD54	PIO24
25	GND	PMC_IDSEL	PCIX_AD53	PIO25
26	PCIX_CBE-L3	PCIX_AD23	GND	PIO26
27	PCIX_AD22	+3.3V	GND	PIO27
28	PCIX_AD21	PCIX_AD20	PCIX_AD52	PIO28
29	PCIX_AD19	PCIX_AD18	PCIX_AD51	PIO29
30	+5V	GND	PCIX_AD50	PIO30
31	PCIX_FRAME-L	PCIX_AD16	PCIX_AD49	PIO31



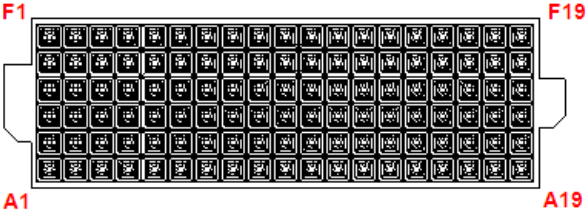
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Pin#	JN1/5 Signal	JN2/6 Signal	JN3/7 Signal	JN4 Signal
32	PCIX_AD17	PCIX_CBE-L2	GND	PIO32
33	PCIX_FRAME-L	GND	GND	PIO33
34	GND	NC	PCIX_AD48	PIO34
35	GND	PCIX_TRDY-L	PCIX_AD47	PIO35
36	PCIX_IRDY-L	+3.3V	PCIX_AD46	PIO36
37	PCIX_DEVSEL-L	GND	PCIX_AD45	PIO37
38	+5V	PCIX_STOP-L	GND	PIO38
39	PCIX_PCIXCAP	PCIX_PERR-L	GND	PIO39
40	PCIX_LOCK-L	GND	PCIX_AD44	PIO40
41	NC	+3.3V	PCIX_AD43	PIO41
42	NC	PCIX_SERR-L	PCIX_AD42	PIO42
43	PCIX_PAR	PCIX_CBE-L1	PCIX_AD41	PIO43
44	GND	GND	GND	PIO44
45	PMC_VIO	PCIX_AD14	GND	PIO45
46	PCIX_AD15	PCIX_AD13	PCIX_AD40	PIO46
47	PCIX_AD12	PCIX_M66EN	PCIX_AD39	PIO47
48	PCIX_AD11	PCIX_AD10	PCIX_AD38	PIO48
49	PCIX_AD9	PCIX_AD8	PCIX_AD37	PIO49
50	+5V	+3.3V	GND	PIO50
51	GND	PCIX_AD7	GND	PIO51
52	PCIX_CBE-L0	NC	PCIX_AD36	PIO52
53	PCIX_AD6	+3.3V	PCIX_AD35	PIO53
54	PCIX_AD5	NC	PCIX_AD34	PIO54
55	PCIX_AD4	NC	PCIX_AD33	PIO55
56	GND	GND	GND	PIO56
57	PMC_VIO	NC	GND	PIO57
58	PCIX_AD3	NC	PCIX_AD32	PIO58
59	PCIX_AD2	GND	NC	PIO59
60	PCIX_AD1	NC	NC	PIO60
61	PCIX_AD0	PCIX_ACK64-L	NC	PIO61
62	+5V	+3.3V	GND	PIO62
63	GND	GND	GND	PIO63
64	PCIX_REQ64-L	NC	NC	PIO64

Table 4-10: PMC Connector Pin Definitions

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XMC1 Connector (CN3214)

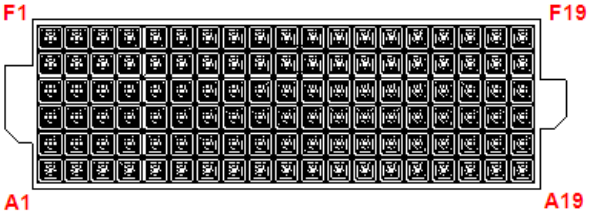


Pin#	A	B	C	D	E	F
1	PCIE_XMC1_RXP0	PCIE_XMC1_RXN0	P3V3_PSU	PCIE_XMC1_RXP1	PCIE_XMC1_RXN1	XMC1_VPWR
2	GND	GND	XMC_TRST-L	GND	GND	PLTRST_XMC1-L
3	PCIE_XMC1_RXP2	PCIE_XMC1_RXN2	P3V3_PSU	PCIE_XMC1_RXP3	PCIE_XMC1_RXN3	XMC1_VPWR
4	GND	GND	XMC1_TCK	GND	GND	XMC1_RST-L
5	PCIE_XMC1_RXP4	PCIE_XMC1_RXN4	P3V3_PSU	PCIE_XMC1_RXP5	PCIE_XMC1_RXN5	XMC1_VPWR
6	GND	GND	XMC1_TMS	GND	GND	P12V
7	PCIE_XMC1_RXP6	PCIE_XMC1_RXN6	PSVS_PSU	PCIE_XMC1_RXP7	PCIE_XMC1_RXN7	XMC1_VPWR
8	GND	GND	XMC1_TD1	GND	GND	NC
9	NC	NC	NC	NC	NC	XMC1_VPWR
10	GND	GND	NC	GND	GND	XMC1_GA0
11	PCIE_XMC1_TXP0	PCIE1_XMC1_TXN0	NC	PCIE1_XMC1_TXP1	PCIE1_XMC1_TXN1	XMC1_VPWR
12	GND	GND	XMC1_GA1	GND	GND	GND
13	PCIE_XMC1_TXP2	PCIE_XMC1_TXN2	PSVS_PSU	PCIE_XMC1_TXP3	PCIE_XMC1_TXN3	XMC1_VPWR
14	GND	GND	XMC1_GA2	GND	GND	XMC1_DAT
15	PCIE_XMC1_TXP4	PCIE_XMC1_TXN4	NC	PCIE_XMC1_TXP5	PCIE_XMC1_TXN5	XMC1_VPWR
16	GND	GND	NC	GND	GND	XMC1_CLK
17	PCIE_XMC1_TXP6	PCIE_XMC1_TXN6	NC	PCIE_XMC1_TXP7	PCIE_XMC1_TXN7	NC
18	GND	GND	NC	GND	GND	NC
19	CLK_XMC1-P	CLK_XMC1-N	NC	PCIE_WAKE-L	P3V3_PSU	NC

Table 4-11: XMC1 Connector Pin Definition

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XMC2 Connector (CN3215)



Pin#	A	B	C	D	E	F
1	PCIE_XMC2_RXP0	PCIE_XMC2_RXN0	P3V3_PSU	PCIE_XMC2_RXP1	PCIE_XMC2_RXN1	XMC2_VPWR
2	GND	GND	XMC_TRST-L	GND	GND	PLTRST_XMC2-L
3	PCIE_XMC2_RXP2	PCIE_XMC2_RXN2	P3V3_PSU	PCIE_XMC2_RXP3	PCIE_XMC2_RXN3	XMC2_VPWR
4	GND	GND	XMC2_TCK	GND	GND	XMC2_RST-L
5	PCIE_XMC2_RXP4	PCIE_XMC2_RXN4	P3V3_PSU	PCIE_XMC2_RXP5	PCIE_XMC2_RXN5	XMC2_VPWR
6	GND	GND	XMC2_TMS	GND	GND	P12V
7	PCIE_XMC2_RXP6	PCIE_XMC2_RXN6	PSVS_PSU	PCIE_XMC2_RXP7	PCIE_XMC2_RXN7	XMC2_VPWR
8	GND	GND	XMC2_TD1	GND	GND	NC
9	NC	NC	NC	NC	NC	XMC2_VPWR
10	GND	GND	NC	GND	GND	XMC2_GA0
11	PCIE_XMC2_TXP0	PCIE_XMC2_TXN0	NC	PCIE_XMC2_TXP1	PCIE_XMC2_TXN1	XMC2_VPWR
12	GND	GND	XMC2_GA1	GND	GND	GND
13	PCIE_XMC2_TXP2	PCIE_XMC1_TXN2	PSVS_PSU	PCIE_XMC1_TXP3	PCIE_XMC1_TXN3	XMC2_VPWR
14	GND	GND	XMC2_GA2	GND	GND	XMC2_DAT
15	PCIE_XM2_TXP4	PCIE_XMC2_TXN4	NC	PCIE_XMC2_TXP5	PCIE_XMC2_TXN5	XMC2_VPWR
16	GND	GND	NC	GND	GND	XMC2_CLK
17	PCIE_XMC2_TXP6	PCIE_XMC2_TXN6	NC	PCIE_XMC2_TXP7	PCIE_XMC2_TXN7	NC
18	GND	GND	NC	GND	GND	NC
19	CLK_XMC2-P	CLK_XMC2-N	NC	PCIE_WAKE-L	P3V3_PSU	NC

Table 4-12: XMC2 Connector Pin Definition

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CompactPCI J1 Connector

Pin	Z	A	B	C	D	E	F
25	GND	+5V	CPCI_REQ64-L	CPCI_ENUM-L	+3.3V	+5V	GND
24	GND	CPCI_AD1	+5V	CPCI_VIO	CPCI_AD0	CPCI_ACK64-L	GND
23	GND	+3.3V	CPCI_AD4	CPCI_AD3	+5V	CPCI_AD2	GND
22	GND	CPCI_AD7	GND	+3.3V	CPCI_AD6	CPCI_AD5	GND
21	GND	+3.3V	CPCI_AD9	CPCI_AD8	CPCI_M66EN	CPCI_CBE-L0	GND
20	GND	CPCI_AD12	GND	CPCI_VIO	CPCI_AD11	CPCI_AD10	GND
19	GND	+3.3V	CPCI_AD15	CPCI_AD14	GND	CPCI_AD13	GND
18	GND	CPCI_SERR-L	GND	+3.3V	CPCI_PAR	CPCI_CBE-L1	GND
17	GND	+3.3V	IPMCB_CLK	IPMB_DAT	GND	CPCI_PERR-L	GND
16	GND	CPCI_DEVSEL-L	GND	CPCI_VIO	CPCI_STOP-L	CPCI_LOCK-L	GND
15	GND	+3.3V	CPCI_FRAME-L	CPCI_IRDY-L	CPCI_BDSEL-L	CPCI_TRDY-L	GND
12-14	Key						
11	GND	CPCI_AD18	CPCI_AD17	CPCI_AD16	GND	CPCI_CBE-L2	GND
10	GND	CPCI_AD21	GND	+3.3V	CPCI_AD20	CPCI_AD19	GND
9	GND	CPCI_CBE-L3	CPCI_IDSEL	CPCI_AD23	GND	CPCI_AD22	GND
8	GND	CPCI_AD26	GND	CPCI_VIO	CPCI_AD25	CPCI_AD24	GND
7	GND	CPCI_AD30	CPCI_AD29	CPCI_AD28	GND	CPCI_AD27	GND
6	GND	CPCI_VIO	CPCI_PRESENT-L	+3.3V	CPCI_CLK0	CPCI_AD31	GND
5	GND	NC	NC	CPCI_RST-L	GND	CPCI_VIO	GND
4	GND	+5V_IPMB	IPMC_HEALTHY-L	CPCI_VIO	NC	NC	GND
3	GND	CPCI_INTA-L	CPCI_INTB-L	CPCI_INTC-L	+5V	CPCI_INTD-L	GND
2	GND	NC	+5V	NC	NC	NC	GND
1	GND	+5V	-12V	NC	+12V	+5V	GND

Table 4-13: CompactPCI J1 Connector Pin Definition

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CompactPCI J2 Connector

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CPCI_CLK6	GND	NC	NC	NC	GND
20	GND	CPCI_CLK5	GND	NC	GND	NC	GND
19	GND	GND	GND	IPMB_DAT	IPMB_CLK	P3V3_AUX	GND
18	GND	NC	NC	NC	GND	NC	GND
17	GND	NC	GND	J2_RST-L	CPCI_REQ-L6	CPCI_GNT-L6	GND
16	GND	NC	NC	CPCI_DEG-L	GND	NC	GND
15	GND	NC	GND	CPCI_FAL-L	CPCI_REQ-L5	CPCI_GNT-L5	GND
14	GND	CPCI_AD35	CPCI_AD34	CPCI_AD33	GND	CPCI_AD32	GND
13	GND	CPCI_AD38	GND	CPCI_VIO	CPCI_AD37	CPCI_AD36	GND
12	GND	CPCI_AD42	CPCI_AD41	CPCI_AD40	GND	CPCI_AD39	GND
11	GND	CPCI_AD45	GND	CPCI_VIO	CPCI_AD44	CPCI_AD43	GND
10	GND	CPCI_AD49	CPCI_AD48	CPCI_AD47	GND	CPCI_AD46	GND
9	GND	CPCI_AD52	GND	CPCI_VIO	CPCI_AD51	CPCI_AD50	GND
8	GND	CPCI_AD56	CPCI_AD55	CPCI_AD54	GND	CPCI_AD53	GND
7	GND	CPCI_AD59	GND	CPCI_VIO	CPCI_AD58	CPCI_AD57	GND
6	GND	CPCI_AD63	CPCI_AD62	CPCI_AD61	GND	CPCI_AD60	GND
5	GND	CPCI_CBE-L5	CPCI_DEV64-L	CPCI_VIO	CPCI_CBE-L4	CPCI_PAR64	GND
4	GND	CPCI_VIO	NC	CPCI_CBE-L7	GND	CPCI_CBE-L6	GND
3	GND	CPCI_CLK4	GND	CPCI_GNT-L3	CPCI_REQ-L4	CPCI_GNT-L4	GND
2	GND	CPCI_CLK2	CPCI_CLK3	SYSEN-L	CPCI_GNT-L2	CPCI_REQ-L3	GND
1	GND	CPCI_CLK1	GND	CPCI_REQ-L1	CPCI_GNT-L1	CPCI_REQ-L2	GND

Table 4-14: CompactPCI J2 Connector Pin Definition

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CompactPCI J3 Connector

Pin	Z	A	B	C	D	E	F
19	GND	+5V	+5V	+12V	+5V	+5V	GND
18	GND	LAN3_TXDP0	LAN3_TXDN0	GND	LAN3_TXDP2	LAN3_TXDN2	GND
17	GND	LAN3_TXDP1	LAN3_TXDN1	GND	LAN3_TXDP3	LAN3_TXDN3	GND
16	GND	LAN4_TXDP0	LAN4_TXDN0	GND	LAN4_TXDP2	LAN4_TXDN2	GND
15	GND	LAN4_TXDP1	LAN4_TXDN1	GND	LAN4_TXDP3	LAN4_TXDN3	GND
14	GND	USB_OC5#	USB_OC6#	USB_OC7#	USB_OC8#	USB_OC9#	GND
13	GND	USB8-P	USB8-N	GND	USB9-P	USB9-N	GND
12	GND	USB6-P	USB6-N	GND	USB7-P	USB7-N	GND
11	GND	USB4-P	USB4-N	GND	USB5-P	USB5-N	GND
10	GND	USB_OC4#	CRT_DDC_CLK	CRT_DDC_DATA	CRT_HSYNC	CRT_VSYNC	GND
9	GND	COM2_CTS-L	COM2_RI-L	CRT_BLUE	CRT_RED	CRT_GREEN	GND
8	GND	COM2_RX	COM2_TX	COM2_DTR-L	COM2_DSR-L	COM2_RTS-L	GND
7	GND	COM3_TX	COM3_RX	COM2_DCD-L	IPMB_CLK	IPMB_DAT	GND
6	GND	SATA_RXP4	SATA_RXN4	GND	SATA_RXP3	SATA_RXN3	GND
5	GND	GND	GND	NC	GND	GND	GND
4	GND	SATA_TXP4	SATA_TXN4	GND	SATA_TXP3	SATA_TXN3	GND
3	GND	KBDATA	KBCLK	NC	MSDATA	MSCLK	GND
2	GND	AUD_SDIN1	NC	NC	NC	NC	GND
1	GND	AUD_RST-L	AUD_SYNC	AUD_BIT_CLK	AUD_SDOUT	AUD_SDIN0	GND

Table 4-15: CompactPCI J3 Connector Pin Definition

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CompactPCI J4 Connector

Pin	Z	A	B	C	D	E	F
25	GND	PMC IO:P1	PMC IO:N1	NC	PMC IO:P2	PMC IO:N2	GND
24	GND	PMC IO:P3	PMC IO:N3	NC	PMC IO:P4	PMC IO:N4	GND
23	GND	NC	NC	NC	NC	NC	GND
22	GND	PMC IO:P5	PMC IO:N5	NC	PMC IO:P6	PMC IO:N6	GND
21	GND	PMC IO:P7	PMC IO:N7	NC	PMC IO:P8	PMC IO:N8	GND
20	GND	NC	NC	NC	NC	NC	GND
19	GND	PMC IO:17	PMC IO:19	NC	PMC IO:18	PMC IO:20	GND
18	GND	PMC IO:21	PMC IO:23	NC	PMC IO:22	PMC IO:24	GND
17	GND	NC	NC	NC	NC	NC	GND
16	GND	PMC IO:25	PMC IO:27	NC	PMC IO:26	PMC IO:28	GND
15	GND	PMC IO:29	PMC IO:31	NC	PMC IO:30	PMC IO:32	GND
12-14	GND	Key Area					Key
11	GND	PMC IO:33	PMC IO:35	NC	PMC IO:34	PMC IO:36	GND
10	GND	PMC IO:37	PMC IO:39	NC	PMC IO:38	PMC IO:40	GND
9	GND	NC	NC	NC	NC	NC	GND
8	GND	PMC IO:41	PMC IO:43	NC	PMC IO:42	PMC IO:44	GND
7	GND	PMC IO:45	PMC IO:47	NC	PMC IO:46	PMC IO:48	GND
6	GND	NC	NC	NC	NC	NC	GND
5	GND	PMC IO:49	PMC IO:51	NC	PMC IO:50	PMC IO:52	GND
4	GND	PMC IO:53	PMC IO:55	NC	PMC IO:54	PMC IO:56	GND
3	GND	NC	NC	NC	NC	NC	GND
2	GND	PMC IO:57	PMC IO:59	NC	PMC IO:58	PMC IO:60	GND
1	GND	PMC IO:61	PMC IO:63	NC	PMC IO:62	PMC IO:64	GND

Table 4-16: CompactPCI J4 Connector Pin Definition

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CompactPCI J5 Connector

Pin	Z	A	B	C	D	E	F
22	GND	PWRLED-L	LAN4_LED_ACT-L	NC	LAN3_LED_ACT-L	NC	GND
21	GND	EDP_TX_P1	EDP_TX_N1	GND	NC	NC	GND
20	GND	EDP_TX_P0	EDP_TX_N0	GND	NC	NC	GND
19	GND	GND	GND	GND	EDP_AUX_P	EDP_AUX_N	GND
18	GND	GPIO6	GPIO7	GPIO8	GPIO9	GPIO10	GND
17	GND	GPIO11	GPIO12	GPIO13	GPIO14	GPIO15	GND
16	GND	GND	GND	EDP_HPD	GND	GPIO16	GND
15	GND	NC	NC	GND	SATA_RXP5	SATA_RXN5	GND
14	GND	NC	NC	GND	SATA-TXP5	SATA-TXN5	GND
13	GND	LAN4_LED_100-L	LAN3_LED_100-L	NC	LAN3_LED_1000-L	LAN4_LED_1000-L	GND
12	GND	DVI_SDA	DVI_SCL	DVI_HPD	NC	NC	GND
11	GND	TMDSC_DATA2_P	TMDSC_DATA2_N	GND	TMDSC_CLK_P	TMDSC_CLK_N	GND
10	GND	TMDSC_DATA0_P	TMDSC_DATA0_N	GND	TMDSC_DATA1_P	TMDSC_DATA1_N	GND
9	GND	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GND
8	GND	USB3_TX_3P	USB3_TX_3N	GND	USB3_RX_3P	USB3_RX_3N	GND
7	GND	GND	GND	BAT_RTM	GND	GND	GND
6	GND	PCIE_CLK-P	PCIE_CLK-N	GND	PLTRST-L	SATA_LED-L	GND
5	GND	GND	GND	GND	GND	GND	GND
4	GND	PCIE_TX3-P	PCIE_TX3-N	GND	PCIE_RX3-P	PCIE_RX3-N	GND
3	GND	PCIE_TX2-P	PCIE_TX2-N	GND	PCIE_RX2-P	PCIE_RX2-N	GND
2	GND	PCIE_TX1-P	PCIE_TX1-N	GND	PCIE_RX1-P	PCIE_RX1-N	GND
1	GND	PCIE_TX0-P	PCIE_TX0-N	GND	PCIE_RX0-P	PCIE_RX0-N	GND

Table 4-17: CompactPCI J5 Connector Pin Definition

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4.5 Switches and Buttons

Solder Side

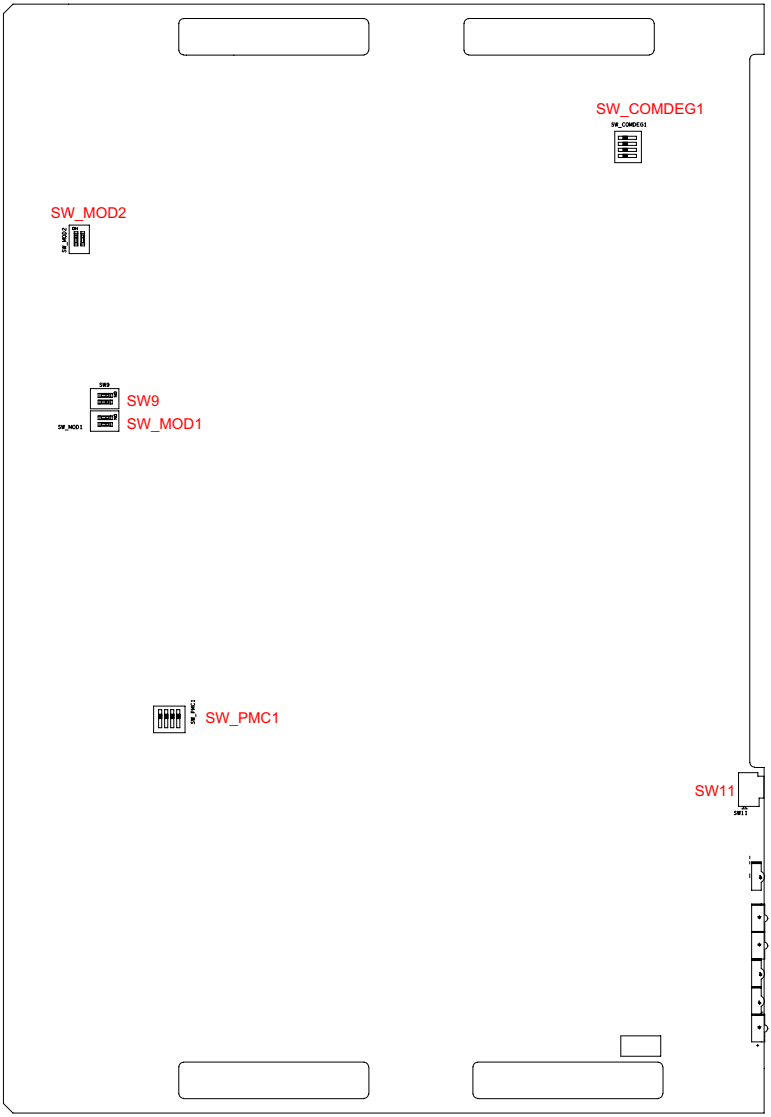


Figure 4-4: Solder-side switch and button locations

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Component Side

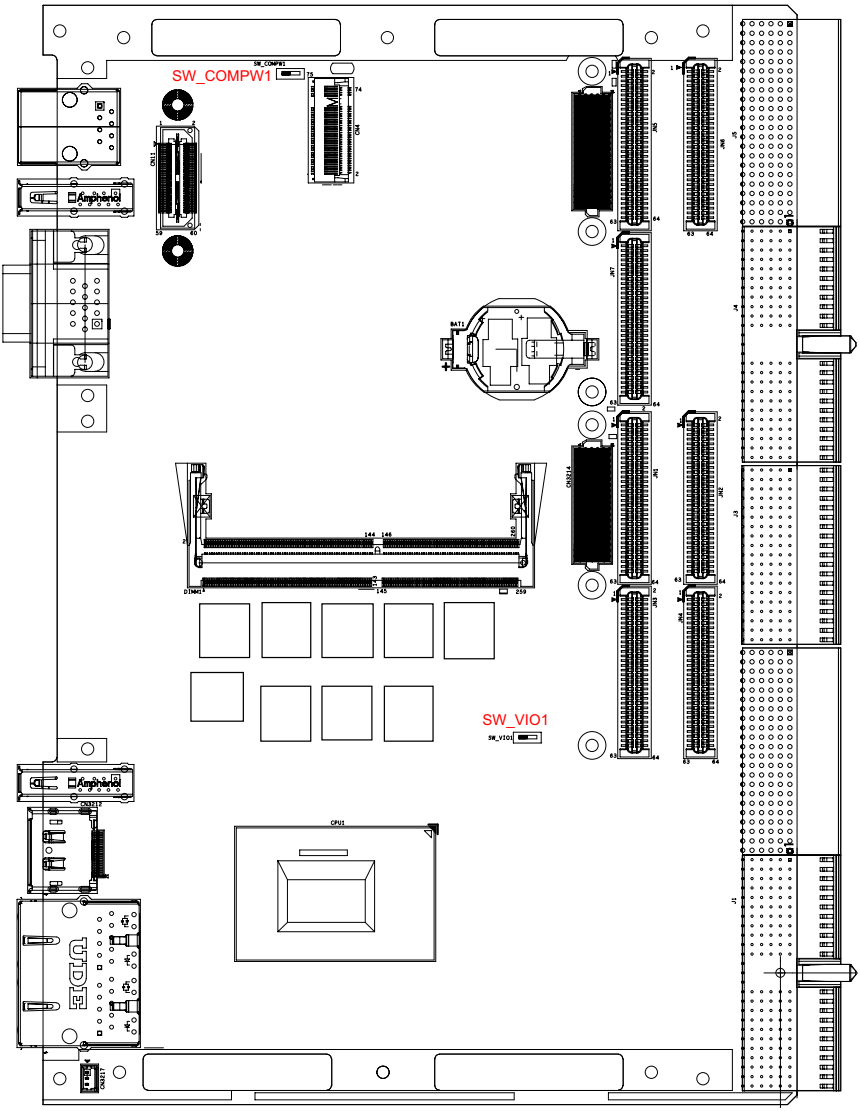
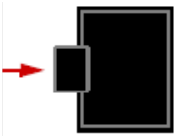


Figure 4-5: Component-side switch locations

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System Reset Button (SW11)

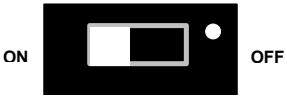
The cPCI-653040(V) has a system reset button on the front panel. See “cPCI-6540 Series Front Panel” on page 19 for the button location.



The following switches are located on the solder side. See “Solder-side switch and button locations” on page 37 for their locations.

PMC VIO Function (SW_VIO1)

Pin	Function
OFF	5V
ON	3.3V (Default)

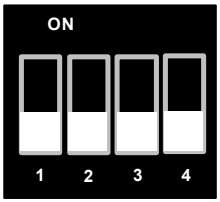


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PMC Clock Settings (SW_PMC1)

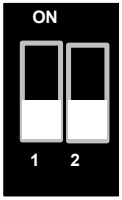
Switch SW_PMC1 allows the user to force the PCI bus to lower bandwidth and clock settings. All are set to OFF by default to support PCI-X mode up to 64-bit/133MHz maximum with the bandwidth and clock determined by the PCI device attached. For SKUs with two PMC slots, both slots will have the same clock settings.

Pin	On	Off
1	Force the PCI bandwidth to 32-bit	Auto Negotiation
2	Force the PCI clock to PCI 66MHz	
3	Force the PCI bus to PCI mode (no PCI-X mode support)	
4	Force the PCI clock to PCI-X 100MHz	



Debug Switches (SW9, SW_MOD1/SW_MOD2)

Switches SW9, SW_MOD1 and SW_MOD2 are for debugging purposes and should be left in the default settings (all OFF).



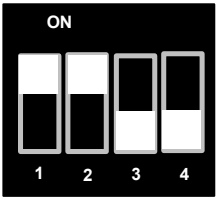
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The following switches are located on the component side. See “Component-side switch locations” on page 38 for their locations.

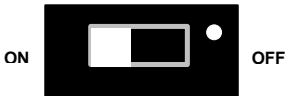
COM Debug Switches (SW_COMDEG1, SW_COMPW1)

Switch **SW_COMDEG1** is set 1, 2 ON and 3, 4 OFF by default to set the front panel RJ-45 COM (CN7) serial port as a standard RS-232 serial port. The setting can be changed to use CN7 as an IPMI debugging port. Leave on default settings unless instructed by ADLINK.

SW_COMDEG1	Function
1, 2 ON, 3, 4 OFF	Normal COM (Default)
1, 2 OFF, 3, 4 ON	IPMI Debug



Switch **SW_COMPW1** is set ON by default. Leave on default settings unless instructed by ADLINK.



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5 Getting Started

This chapter describes the following installation procedures for the cPCI-6540 and rear transition module:

- CPU and Heatsink
- M.2 SATA module
- 2.5” SATA drive
- PMC/XMC module installation

5.1 CPU and Heatsink

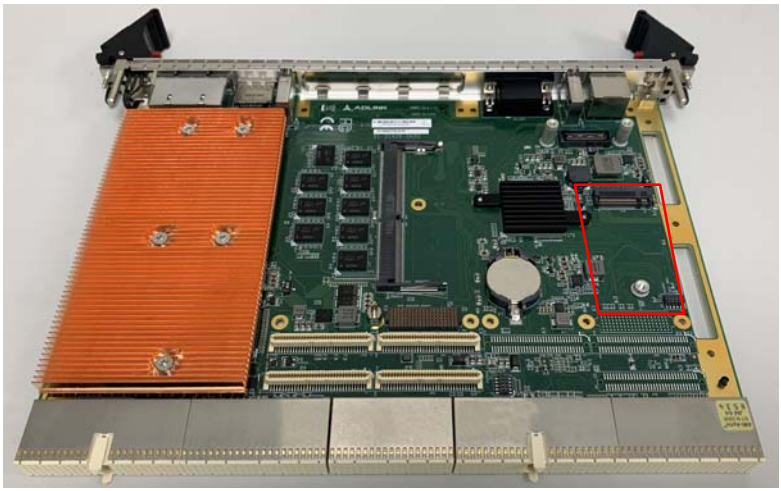
The cPCI-6540 Series come with CPU and heatsink pre-installed. Removal of heatsink/CPU by users is not recommended. Please contact your ADLINK service representative for assistance.

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5.2 M.2 SATA Module Installation

The cPCI-6540 provides space to install a M.2 SATA module. Follow the instructions below to install a M.2 SATA module to the cPCI-6540.

1. An M.2 SATA module can be installed in the location marked as below.



2. Insert the M.2 SATA module into the M.2 SATA slot and secure it with two screws as shown below.



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5.3 2.5" SATA Drive Installation

The cPCI-6540V provides space to install a 2.5” SATA drive.

1. Locate the screws and 2.5” SATA drive bracket in the accessory pack.



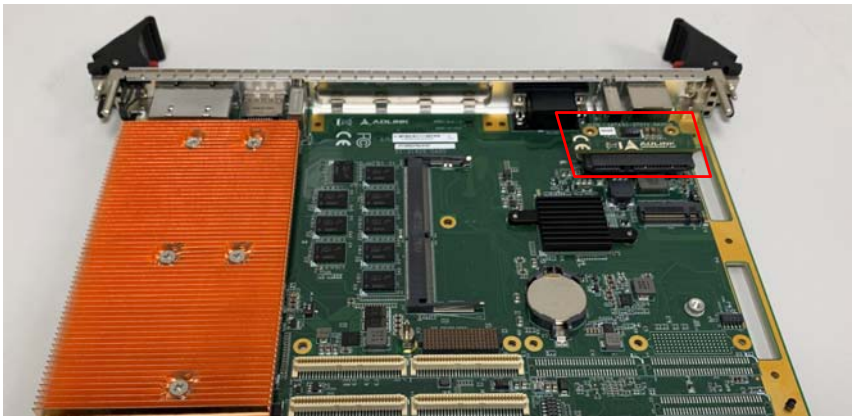
2. Secure the drive to the bracket by fastening the four screws provided as shown below.



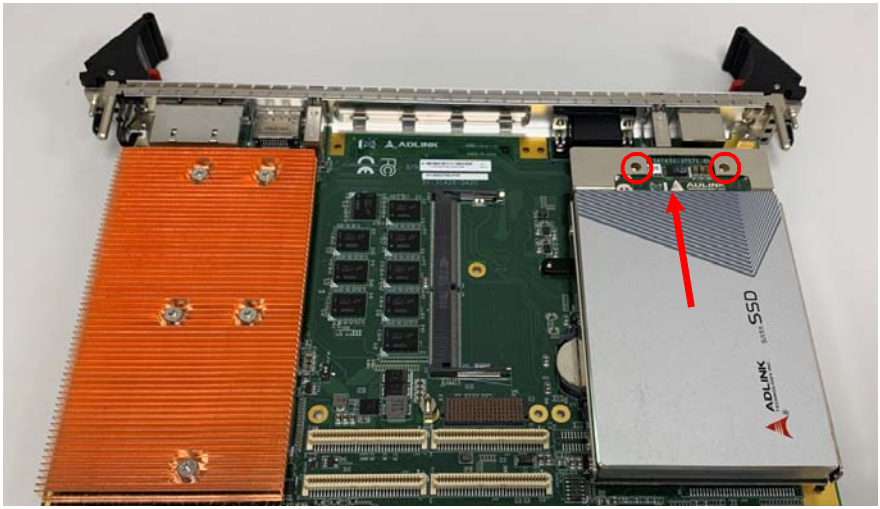
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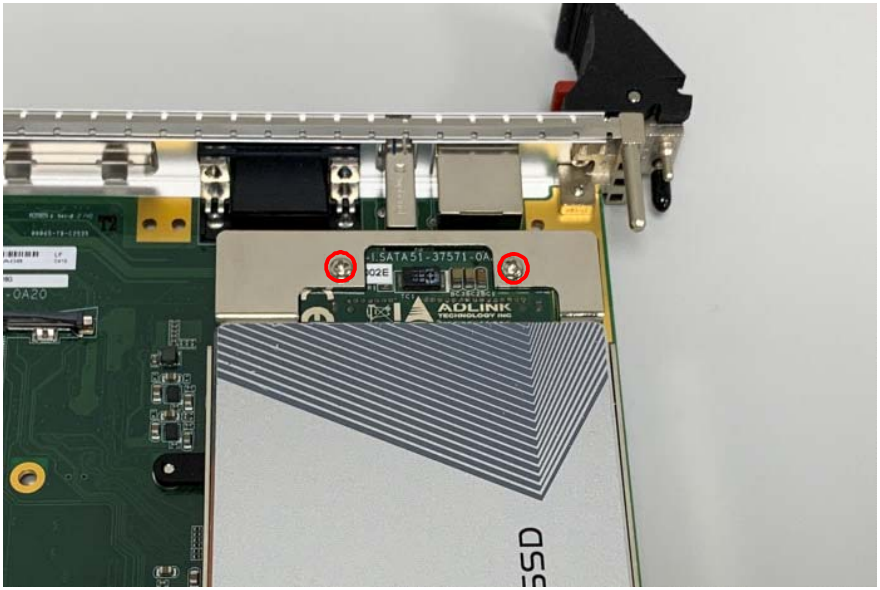
3. Find the SATA adapter board (DB-LSATA) in the accessory pack. Align the adapter board with the onboard SATA connector (CN11).





4. Align the drive assembly as shown below and insert it into the SATA connector on the adapter board until it is properly seated. Secure the drive assembly to the blade with two screws circled below.





5. Turn the blade over and secure with two screws as marked below to complete the SATA drive installation.

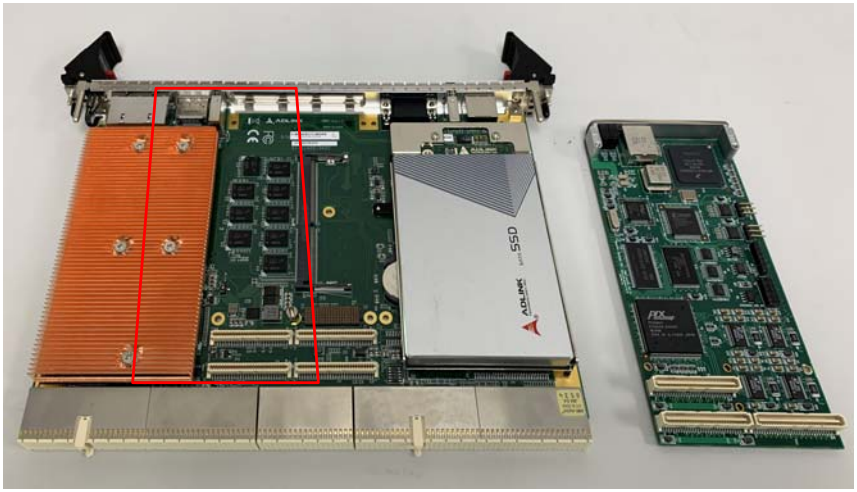


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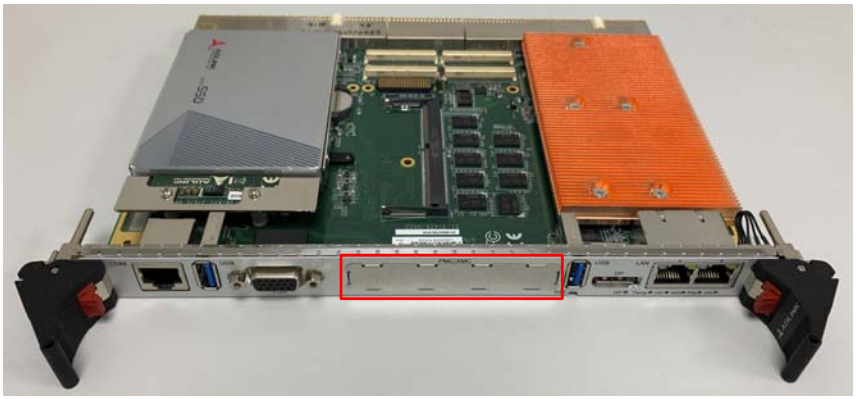
5.4 PMC/XMC Installation

The cPCI-6540 series provides space to install PMC or XMC module(s). The cPCI-6540 provides 1 PMC/XMC site and the cPCI-6540V has 2 PMC/XMC sites. The instructions below show the cPCI-6540. The same procedure is used to install a second module in the cPCI-6540V's second PMC/XMC site.

1. The cPCI-6540's single PMC/XMC slot is shown below.



2. Remove the PMC filler plate on the front panel.

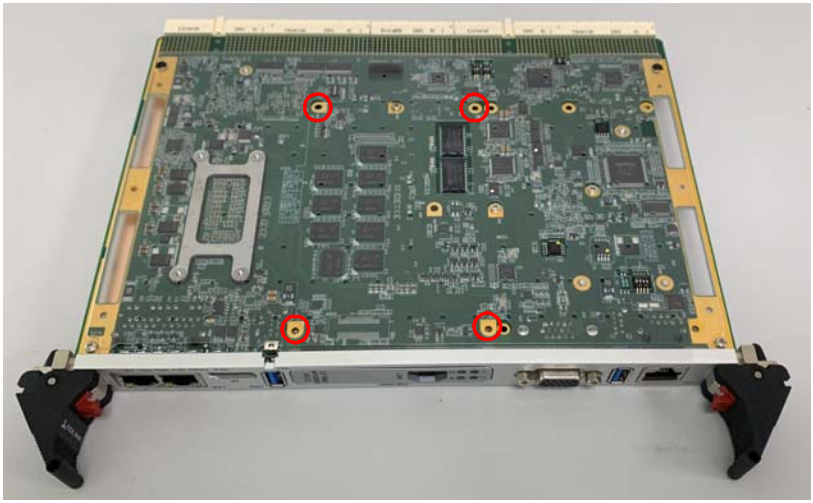


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3. Align the connectors on the PMC/XMC module to the PMC/XMC connectors on cPCI-6540(V) blade. Press down to secure the PMC/XMC module to the cPCI-6540(V).



4. Secure four screws provided by the PMC/XMC module supplier to the solder side of the cPCI-6540(V) blade to complete the installation of the PMC/XMC module.



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5.5 Installing the cPCI-6540 to the Chassis

The cPCI-6540 may be installed in a system or peripheral slot of a 6U CompactPCI chassis. These instructions are for reference only. Refer to the user guide that comes with the chassis for more information.

1. Be sure to select the correct slot depending on the operational purpose of the module. The system power may now be powered on or off.
2. Remove the blank face cover from the selected slot, if necessary.
3. Press down on the release catches of the cPCI-6540 ejector handles.
4. **Remove the black plastic caps securing the mounting screws to the front panel.**
5. Align the module's top and bottom edges to the chassis card guides, and then carefully slide the module into the chassis. A slight resistance may be felt when inserting the module. If the resistance it too strong, check if there are bent pins on the backplane or if the board's connector pins are not properly aligned with connectors on the backplane. Then push the board until it is completely flush with the chassis.
6. Push the ejector handles outwards to secure the module in place, and then fasten the screws on the module front panel.
7. Connect the cables and peripherals to the board, and then turn the chassis on if necessary.

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6 Driver Installation

The cPCI-6540 drivers are available the ADLINK website (https://www.adlinktech.com/Products/CompactPCI/6UCompactPCI2.0Blades/cPCI-6540_Series). ADLINK provides validated drivers for Windows 10 64-bit. We recommend using these drivers to ensure compatibility.

6.1 cPCI-6540 Drivers

The following describes the cPCI-6540 driver installation procedures for Windows 10 64-bit.

1. Install the Windows operating system before installing any driver. Most standard I/O device drivers are installed during Windows installation.
2. Install the **chipset driver** by extracting and running the program in **...\Chipset\Intel_Chipset_10.1.17541.8066.zip**.
3. Install the **graphics driver** and utilities by extracting and running the program in **...\Graphics\Intel_Graphics_Driver.zip**.
4. Install the **LAN drivers** by extracting and running the program in **…\LAN\Intel_Gigabit_Network_connection_Win10_x64_25.0.zip**.
5. Install the **Intel Rapid Storage Technology Utility** by extracting and running the program in **…\RST\Intel_Rapid_Storage_Technology_16.0.2.1086.zip**.
6. Install the **audio driver** and utilities by extracting and running the program in **…\Audio\Realtek_High_Definition_Audio_Driver_R2.82.zip**.
7. Install the **Intel® Management Engine Interface driver** for Intel® AMT support by extracting and running the program in
   - ▷ CM Series Chipset supporting Xeon Processors: **...\Chipset\Intel_Management_Engine_Corporate_12.0.3.1091.zip** or
   - ▷ QM Series Chipset supporting i7/i5/i3/Celeron Processors **...\Chipset\Intel_Management_Engine_Corporate_12.0.3.1091.zip**
8. Install the Intel Serial Rapid IO driver by extracting and running the program in ...**\SIO\Intel_Serial_IO_30.100.1727.1.zip**.

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7 BIOS Setup Utility

The following chapter describes basic navigation for the AMI EFI BIOS setup utility.

7.1 Starting the BIOS

To enter the setup screen, follow these steps:

1. Power on the motherboard
2. Press the < Delete > key on your keyboard when you see the following text prompt:
   < Press DEL to run Setup >
3. After you press the < Delete > key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu.



In most cases, the < Delete > key is used to invoke the setup screen. There are several cases that use other keys, such as < F1 >, < F2 >, and so on.

Setup Menu

The main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in this user's guide.

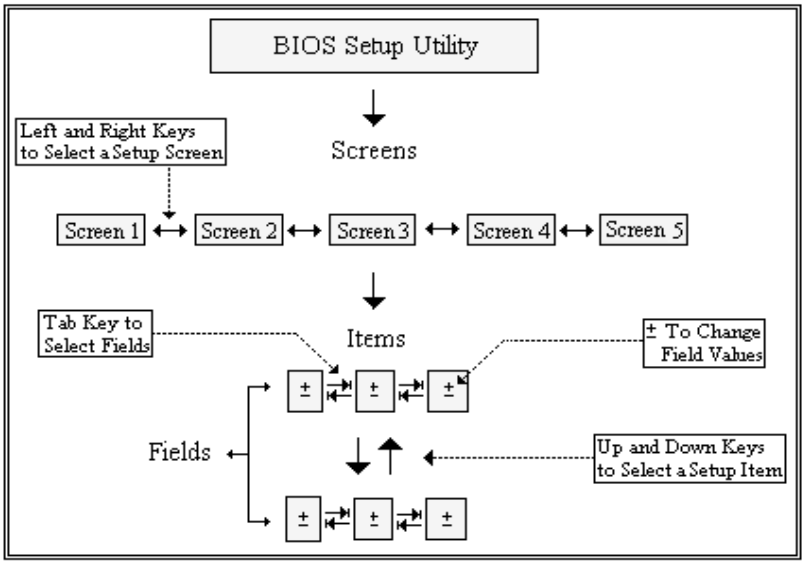
The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed" options cannot be configured, "Blue" options can be.

The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

Navigation

The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process.

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NOTE: There is a hot key legend located in the right frame on most setup screens.

→←	Left/Right. The Left and Right < Arrow > keys allow you to select a setup screen. For example: Main screen, Advanced screen, Chipset screen, and so on.
↑↓	Up/Down The Up and Down < Arrow > keys allow you to select a setup item or sub-screen.
+-	Plus/Minus The Plus and Minus < Arrow > keys allow you to change the field value of a particular setup item. For example: Date and Time.
Tab	The < Tab > key allows you to select setup fields.
ESC	The < Esc > key allows you to discard any changes you have made and exit the Setup. Press the < Esc > key to exit the setup without saving your changes. Press the < Enter > key to discard changes and exit. You can also use the < Arrow > key to select Cancel and then press the < Enter > key to abort this function and return to the previous screen.

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7.2 Main Setup

When you first enter the Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. The Main BIOS Setup menu is shown below.

Main	Advanced	Chipset	Security	Boot	Save & Exit	Server Mgmt
-BIOS Information -System Information -System Date -System Time	-CPU ► Configuration -USB ► Configuration -CSM ► Configuration -Super IO ► Configuration -Serial Console Redirection ► -Hardware ► Monitor Timer -Network ► Stack Configuration	-System ► Agent (SA) Configuration -PCH-IO ► Configuration	-Password Description -Secure Boot Menu ►	-Boot Configuration	-Save Options -Boot Override	-BMC Self Test Status -BMC Device ID -BMC Device Revision -BMC Firmware Revision -IPMI Version -BMC Intreface(s)


NOTE:

► indicates a submenu
Gray text indicates info only

7.2.1 BIOS Information

Feature	Options	Description
BIOS Vendor	Info only	American Megatrends
BIOS Version	Info only	Display Core Version
Build Date	Info only	Date the BIOS was built
MRC Version	Info only	Platform MRC Version
GOP Version	Info only	Platform GOP Version
ME FW Version	Info only	Intel Management Engine Version

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7.2.2 System Information

Feature	Options	Description
Project Name	Info only	Display Project Name
CPU Board Version	Info only	Display CPU Board Version
CPU Brand String	Info only	Display Intel CPU Brand Information
CPU Frequency	Info only	Display CPU Frequency
Total Memory	Info only	Display Current System installed Memory Size
Memory Frequency	Info only	Display Memory Frequency Information
PCH SKU	Info only	Display PCH Version
Stepping	Info only	Display PCH Stepping

7.2.3 System Date and Time

Feature	Options	Description
System Date	MM/DD/YYYY	Requires the alpha-numeric entry of the day of the week, day of the month, calendar month, and all 4 digits of the year, indicating the century and year (Fri XX/XX/20XX).
System Time	HH/MM/SS	Presented as a 24-hour clock setting in hours, minutes, and seconds.

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7.3 Advanced

This menu contains the settings for most of the user interfaces in the system.

7.3.1 CPU Configuration

Feature	Options	Description
Type	Info only	Manufacturer, model
ID	Info only	Display CPU Information
Microcode Revision	Info only	Display Microcode Revision
Speed	Info only	Display CPU Speed.
L1 Data Cache	Info only	Display L1 Data Cache size
L1 Instruction Cache	Info only	Display L1 Instruction Cache size
L2 Cache	Info only	Display L2 Data Cache size
L3 Cache	Info only	Display L3 Data Cache size
L4 Cache	Info ony	Display L4 Data Cache size
Boot performance mode	Max Battery **Max Non-Turbo Performance** Turbo Perfromance	Select the performance state that the BIOS will set starting from reset vector.
Hyper-Threading	Disabled **Enabled**	Enabled or Disabled Hyper-Threading Technology
Active Processor Cores	**All** 1 2 3 4 5 6 7	Number of cores to enable in each processor package
Intel® SpeedStep™	Disabled **Enabled**	Allows more than two frequency ranges to be supported
Intel® Speed Shift Technology	Disabled **Enabled**	Enable/Disable Intel® Speed Shift Technology support.
Turbo Mode	Disabled **Enabled**	Enable/Disable processor Turbo Mode
Configurable TDP Boot Mode	**Nominal** Deactivate	Configurable TDP Mode as Nominal/Deactivate TDP selection. Deactivate option will set MSR to Nominal and MMIO to Zero
Platform PL1 Enable	Disabled **Enabled**	When a processor thermal sensor trips (either core), the PROCHOT# will be driven. If bi-direction is enabled, external agents can drive PROCHOT# to throttle the processor

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Feature	Options	Description
Platform PL1 Power	0	Platform Power Limit 1 Power in Milli Watts. BIOS will round to the nearest 1/8W when programming. Any value can be programmed between Max and Min Power Limits (specified by PACKAGE_POWER_SKU_MSR). For 12.50W, enter 12500. This setting will act as the new PL1 value for the Package RAPL algorithm.
Platform PL1 Time Window	0	Platform Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0 = default values. Indicates the time window over which Platform TDP value should be maintained.
C state	Disabled **Enabled**	Enable/Disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized.
Package C State Limit	C0/C1 C2 C3 C6 C7 C7S C8 C9 C10 CPU Default **Auto**	Maximum Package C State Limit Setting. CPU Default: Leaves to Factory default value. Auto: Initializes to deepest available Package C State Limit
Active Processor Cores	**All** 1 2 3 4 5	Number of cores to enable in each processor package.
VT-d	Disabled **Enabled**	Enable/Disable VT-d capability
DTS SMM	Disabled **Enabled** Critical Temp Reporting (Out of spec)	Disabled: ACPI thermal management uses EC reported temperature values. Enabled: ACPI thermal management uses DTS SMM mechanism to obtain CPU temperature values. Out of Spec: ACPI Thermal Management uses EC reported temperature values and DTS SMM is used to handle Out of Spec.
Intel Trusted Execution Technology	**Disabled** Enabled	Enable/Disable utilization of additional hardware capabilities provided by Intel® Trusted Execution Technology. Changes require a full power cycle to take effect.

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7.3.2 USB Configuration

Feature	Options	Description
USB Module version	Info only	
USB Controllers:	Info only	
USB Devices:	Info only	.
USB Mass Storage Driver Support	Disabled **Enabled**	Enable/Disable USB Mass Storage Driver Support
XHCI Compliance Mode	Enabled **Disabled**	Option to enable Compliance Mode. Default is to disable Compliance Mode. Change to enabled for Complaince Mode testing.
xDCI Support	Enabled **Disabled**	Enable/Disable xDCI (USB OTG device)
USB Port Disable Override	**Disable Link** Select Per-Pin	Select to Enable/Disable the corresponding USB port from reporting a Device Connection to the Controller.

7.3.3 CMS Configuration

Feature	Options	Description
CSM Support	**Disabled** Enabled	Enable/Disable CSM Support.
CSM16 Module Version	Info only	
GateA20 Active	**Upon Request** Always	UPON REQUEST - GA20 can be disabled using BIOS services. ALWAYS - do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.
Boot Option filter	**UEFI and Legacy** Legacy only UEFI only	This option controls Legacy/UEFI ROMs priority.
Option ROM execution	Info only	
Network	**Do not launch** Legacy UEFI	Controls the execution of UEFI and Legacy Network OpROM.
Storage	Do not launch **UEFI** Legacy	Controls the execution of UEFI and Legacy Storage OpROM
Video	Do not launch **UEFI** Legacy	Controls the execution of UEFI and Legacy Video OpROM.
Other PCI devices	Do not launch **UEFI** Legacy	Determines OpROM execution policy for devices other than Network, Storage, or Video.

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7.3.4 Super IO Management

Feature	Options	Description
NCT6106D Super IO Configuration	Info only	
Serial Port 1 Configuration	Submenu	
Serial Port 2 Configuration	Submenu	
Serial Port 3 Configuration	Submenu	
Serial Port 4 Configuration	Submenu	
Serial Port 5 Configuration	Submenu	

Super IO Management > Serial Port 1 Configuration

Feature	Options	Description
Serial Port 1 Configuration	Info only	
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	IO=3F8h; IRQ=4	Fixed configuration of serial port.
Device Mode	**RS232 Mode** RS485 Mode RS422 Mode	Change the Serial Port mode.

Super IO Management > Serial Port 2 Configuration

Feature	Options	Description
Serial Port 2 Configuration	Info only	
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	IO=2F8h; IRQ=3	Fixed configuration of serial port.

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Super IO Management > Serial Port 3 Configuration

Feature	Options	Description
Serial Port 3 Configuration	Info only	
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	IO=3E8h; IRQ=5	Fixed configuration of serial port.

Super IO Management > Serial Port 4 Configuration

Feature	Options	Description
Serial Port 4 Configuration	Info only	
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	IO=2E8h; IRQ=7	Fixed configuration of serial port.

Super IO Management > Serial Port 5 Configuration

Feature	Options	Description
Serial Port 5 Configuration	Info only	
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	IO=2F0h; IRQ=6	Fixed configuration of serial port.

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7.3.5 Serial Console Redirection

Feature	Options	Description
Serial Console Redirection	Info only	
COM1~5		
Console Redirection	Enabled **Disabled**	Console Redirection enable or disable
Console Redirection Settings	Submenu	

Console Redirection Settings

Feature	Options	Description
Console Redirection Settings	Info only	
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7 **8**	Data Bits.
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection..
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.

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Feature	Options	Description
VT-UTF8 Combo Key Support	Disabled **Enable**	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.
Recorder Mode	**Disabled** Enable	With this mode enabled only text will be sent. This is to capture Terminal data.
Resolution 100x31	**Disabled** Enable	Enables or disables extended terminal resolution
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.

7.3.6 Miscellaneous

Feature	Options	Description
Trusted Computing	Submenu	Trusted Computing Settings
NVMe Configuration	Submenu	NVMe Device Options Settings
Power Supply Unit	Emulate AT Mode **ATX Mode**	ATX: OS will turn off system power when shutdown. AT mode will not support S3 & S4 & S5, so it will change Power Loss State to Power On.
Network	**Do not launch** UEFI Legacy	Controls the execution of UEFI Network OpROM

Trusted Computing

Feature	Options	Description
Security Device Support	**Disabled** Enabled	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.

NVMe Configuration

Feature	Options	Description
NVMe Configuration	Info only	

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7.3.7 Hardware Monitor

Feature	Options	Description
PC Health Status	Info only	
CPU temperature	Read only	
System temperature	Read only	
3.3V	Read only	
5V	Read only	
12V	Read only	

7.3.8 Network Stack Configuration

Feature	Options	Description
Network Stack	**Disabled** Enabled	Enable/Disable UEFI network stack.
IPv4 PXE Support	**Disabled** Enabled	Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.
IPv4 HTTP Support	**Disabled** Enabled	Enable/Disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.
IPv6 PXE Support	**Disabled** Enabled	Enable/Disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.
IPv6 HTTP Support	**Disabled** Enabled	Enable/Disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.
IPSEC Certificate	**Enabled**	Support to Enable/Disable IPSEC certificate for Ikev.
PXE boot wait time	**0**	Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.
Media detect count	**1**	Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

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7.4 Chipset

Feature	Options	Description
System Agent (SA) Configuration	Submenu	System Agent (SA) Parameters
PCH-IO Configuration	Submenu	PCH parameters

7.4.1 System Agent (SA) Configuration

Feature	Options	Description
SA PCIe Code Version	Info only	Displaye SA PCIe code revision
VT-d	Info only	Display VT-d supported or not
Memory Configuration	Submenu	Memory parameters
Graphics Configuration	Submenu	Graphics parameters
PEG Port Configuration	Submenu	PEG port parameters
Above 4GB MMIO BIOS assignment	Enabled **Disabled**	Enable/Disable above 4GB memory mapped BIOS assignment.

Memory Configuration

Feature	Options	Description
Memory RC Version	Info only	Display RC version
Memory Frequency	Info only	Display memory frequency
Memory Voltage	Info only	Display memory voltage
Memory Timings (tCL-tRCD-tRP-tRAS)	Info only	Display memory timing parameters
Channel 0 Slot 0	Info only	Display memory Size
Channel 1 Slot 0	Info only	Display memory Size
Maximum Memory Frequency	**Auto** 1067, 1200…, 5867	Maximum memory frequency selections in MHz. Valid values should match the refclk, i.e. divided by 133 or 100
Max TOLUD	**Dynamic** 1 GB, 1.25GB…3.5GB	Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.

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Graphics Configuration

Feature	Options	Description
Skip Scaning of External Gfx Card	**Disabled** Enabled	If Enabled, it will not scan for External Gfx card on PEG and PCH PCIE ports
Primary Display	**Auto** IGFX PEG PCIe	Select which IGFX/PEG/PCI Graphics device should be Primary Display.
Select PCIe Card	**Auto** Elk Creek 4 PEG Eval	Select the card used on the platform Auto: Skip GPIO based power enable to dGPU Elk Creek 4: dGPU Power Enable = ActiveLow PEG Eval: dGPU Power Enable = ActiveHigh
Internal Graphics	**Auto** Disabled Enabled	Keep IGFX enabled based on the setup options
GTT Size	2MB 4MB **8MB**	Select the GTT Size
Aperture Size	128MB **256MB** 512MB 1024MB 2048MB	Select the Aperture Size Note: Above 4GB MMIO BIOS assignment is automatically enabled when selecting 2048MB aperture. To use this feature, please disable CSM support.
DVMT Pre-Allocated	0M **32M** 64M 4M 8M 12M 16M 20M 24M 28M 32M/F7 36M 40M 44M 48M 52M 56M 60M	Select DVMT 5.0 pre-allocated (fixed) graphics memory size used by the internal graphics device.
DVMT Total Gfx Mem	128M **256M** Max	Select DVMT5.0 total graphics memory used by the internal graphics device.

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PEG Port Configuration

Feature	Options	Description
PEG 0:1:0 / 0:1:1 / 0:1:2 / 0:6:0		
Enable Root Port	Disabled Enabled **Auto**	Enable or disable this root port
Max Link Speed	**Auto** Gen1 Gen2 Gen3	Configure PEG 0:1:0 max speed
PEG0 Slot Power Limit Value	75	Sets the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying this value by the Slot Power Limit Scale. Values 0-255
PEG0 Slot Power Limit Scale	**1.0x** 0.1x 0.01x 0.001x	Select the scale used for the Slot Power Limit Value.
PEG0 Physical Slot Number	1	Set the physical slot number attached to this Port. The number has to be globally unique within the chassis. Values 0-8191
Gen3 RxCTLE Control	Submenu	Gen3 RxCTLE Control per Bundle
PCIe Rx CEM Test Mode	**Disabled** Enabled	Enable/Disable PEG Rx CEM Loopback Mode
PCIe Spread Spectrum Clocking	**Enabled** Disabled	Allows disabling Spread Spectrum Clocking for compliance testing

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Gen3 RxCTLE Control

Feature	Options	Description
Bundle0	**0**	Gen3 RxCTLE setting for Bundle0 (Lane0, Lane1)
Bundle1	**0**	Gen3 RxCTLE setting for Bundle1 (Lane2, Lane3)
Bundle2	**0**	Gen3 RxCTLE setting for Bundle2 (Lane4, Lane5)
Bundle3	**0**	Gen3 RxCTLE setting for Bundle3 (Lane6, Lane7)
Bundle4	**0**	Gen3 RxCTLE setting for Bundle4 (Lane8, Lane9)
Bundle5	**0**	Gen3 RxCTLE setting for Bundle5 (Lane10, Lane11)
Bundle6	**0**	Gen3 RxCTLE setting for Bundle6 (Lane12, Lane13)
Bundle7	**0**	Gen3 RxCTLE setting for Bundle7 (Lane14, Lane15)
PEG10 RxCTLE Override	**Disabled** Enabled	When Enabled, it overrides PEG0 RxCTLE adaptive behaviour
PEG11 RxCTLE Override	**Disabled** Enabled	When Enabled, it overrides PEG1 RxCTLE adaptive behavior
PEG12 RxCTLE Override	**Disabled** Enabled	When Enabled, it overrides PEG2 RxCTLE adaptive behavior
DMI RxCTLE Override	**Disabled** Enabled	When Enabled, it overrides DMI RxCTLE adaptive behavior

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7.4.2 PCH-IO Configuration

Feature	Options	Description
PCI Express Configuraiton	Submenu	Configure Serial IRQ Mode.
SATA And RST Configuration	Submenu	Enable/Disable SMBus Support.
HD Audio Configuration	Submenu	Select the target OS.
PCH LAN Controller	**Enabled** Disabled	Enable/Disable onboard NIC
Serial IRQ Mode	Quiet **Continuous**	Configure Serial IRQ Mode
High Precision Timer	**Enabled** Disabled	Enable or Disable the High Precision Event Timer
PCIE PLL SSC	**Auto** 0.1%~2.0%	PCIe PLL SSC percentage. Auto – Keep HW default, no BIOS override. Range is 0.0%-2.0%
SPD Write Disable	**True** False	Enable/Disable setting SPD write disable.

PCIe Express Configuration

Feature	Options	Description
PCIe Configuration	Info only	
PCI Express Clock Gating	Disabled **Enabled**	PCI Express Clock Gating Enable/Disable for each root port
DMI Link ASPM Control	**Disabled** Enabled	The control of Active State Power Management of the DMI Link
PCIE Port assigned to LAN	Read only	
Compliance Test Mode	**Disabled** Enabled	Enable when using Compliance Load Board
PCIe-USB Glitch W/A	**Disabled** Enabled	PCIe-USB Glitch W/A for bad USB device(s) connected behind PCIE/PEG port.
PCIe function swap	Disabled **Enabled**	When Disabled, prevents PCIE root port function swap. If any function other than 0^{th} is enabled, 0^{th} will become visible.
PCIe Express Root Port1/5/6/7/8/9/17/21	Submenu	Control the PCI Express Root Port. Auto: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIE root port Disable: Disable PCIE root port.

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PCIe Express Configuration > PCI Express Root PortX

Feature	Options	Description
PCIe Express Root PortX	Disabled **Enabled**	Control the PCI Express Root Port.
Connection Type	Built-in **Slot**	Built-In: a built-in device is connected to this rootport. SlotImplemented bit will be clear. Slot: this rootport connects to user-accessible slot. SlotImplemented bit will be set.
ASPM	**Disable** L0s L1 L0sL1 Auto	Set the ASPM Level: Force L0s – Force all inks to L0s State Auto – BIOS auto configure Disable – Disables ASPM
L1 Substates	Disabled L1.1 **L1.1 & L1.2**	PCI Express L1 substates settings.
Gen3 Eq Phase3 Method	**Hardware** Static Coeff.	PCIe Gens3 Equalization Phase 3 Method
Hot Plug	**Disabled** Enabled	PCI Express Hot Plug Enable/Disable.
UPTP	Info only	Upstream Port Transmitter Preset
DPTP	Info only	Downstream Port Transmitter Preset
ACS	**Enabled** Disabled	Enable/Disable Access Control Services Extended Capability
PTM	**Enabled** Disabled	Enable/Disable Precision Time Measurement
DPC	**Enabled** Disabled	Enable/Disable Downstream Port Containment
EDPC	**Enabled** Disabled	Enable/Disable Rootport extensions for Downstream Port Containment
URR	Enabled **Disabled**	PCI Express Unsupported Request Reporting Enable/Disable
FER	Enabled **Disabled**	PCI Express Device Fatal Error Reporting Enable/Disable
NFER	Enabled **Disabled**	PCI Express Device Non-Fatal Error Reporting Enable/Disable
CER	Enabled **Disabled**	PCI Express Device Correctable Error Reporting Enable/Disable
CTO	Enabled **Disabled**	PCI Express Completion Timer TO Enable/Disable.
SEFE	Enabled **Disabled**	Root PCI Express System Error on Fatal Error Enable/Disable
SENFE	Enabled **Disabled**	Root PCI Express System Error on Non-Fatal Error Enable/Disable.

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Feature	Options	Description
SECE	Enabled **Disabled**	Root PCI Express System Error on Correctable Error Enable/Disable
PME SCI	**Enabled** Disabled	PCI Express PME SCI Enable/Disable
Hot Plug	Enabled **Disabled**	PCI Express Hot Plug Enable/Disable
Advanced Error Reporting	**Enabled** Disabled	Advanced Error Reporting Enable/Disable
PCIe Speed	**Auto** Gen1 Gen2 Gen3	Configure PCIe Speed
Transmitter Half Swing	**Disabled** Enabled	Transmitter Half Swing Enable/Disable
Detect Timeout	Info only	The number of milliseconds reference code will wait for link to exit Detect State for enabled ports before assuming there is no device and potentially disabling the port.
Extra Bus Reserved	Info only	Extra Bus Reserved (0-7) for bridges behind this Root Bridge
Reserved Memory	Info only	Resreved Memory for this Root Bridge (1-20) MB
Reserved I/O	Info only	Reserved I/O (4K/8K/12K/16K/20K) range for this root bridge
PCH PCIe LTR Configuration		
LTR	**Enabled** Disabled	PCH PCIE Latency Reporting Enable/Disable
Snoop Latency Override	Disabled Manual **Auto**	Snoop Latency Override for PCH PCIE. Disabled: Disable override Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Non Snoop Latency Override	Disabled Manual **Auto**	Non Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Force LTR Override	**Disabled** Enabled	Force LTR Override for PCH PCIE. Disabled: LTR override values will not be forced. Enabled: LTR override values will be forced and LTR messages from the device will be ignored.
LRT Lock	**Disabled** Enabled	PCIE LTR configuration lock

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SATA And RST Configuration

Feature	Options	Description
SATA And RST Configuration	Info only	
SATA Controller(s)	Disabled **Enabled**	
SATA Mode Selection	**AHCI** Intel RST Premium With Intel Optane System Acceleration	Determines how SATA controller(s) operate.
SATA Test Mode	Enabled **Disabled**	Test Mode Enable/Disable (Loop Back)
Software Feature Mask Configuration	Submenu	RST Legacy OROM/RST UEFI driver will refer to the SWFM configuration to enable/disable the storage features.
Aggressive LPM Support	Disabled **Enabled**	Enable PCH to aggressively enter link power state.
SATA Controller Speed	Default Gen1 **Gen2** Gen3	Indicates the maximum speed the SATA controller can support
Serial ATA Port X, X = 0-7	Info only	
Software Preserve	Info only	
Port X	Disabled **Enabled**	Enable or Disable SATA Port.
Hot Plug Capability	**Disabled** Enabled	Designates this port as Hot Pluggable
Configured as eSATA	Info only	
External	**Disabled** Enabled	Marks this port as external
Spin Up Device	**Disabled** Enabled	If enabled for any of ports Staggerred Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
SATA Device Type	**Hard Disk Drive** Solid State Drive	Identify the SATA port is connected to solid state drive or hard disk drive
SATA Port X DevSlp	**Disabled** Enabled	Enable/Disable SATA Port X DevSlp. For DevSlp to work, both hard drive and SATA port need to support DevSlp function, otherwise an unexpected behavior might happen. Please check board design before enabling it.
DTTO Configuration	**Disabled** Enabled	Enable/Disable DITO configuration
DITO Value	Info only	Display DITO value
DM Value	Info only	Display DM value

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HD Audio Configuration

Feature	Options	Description
HD-Audio Support	Disabled **Enabled**	Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled Enabled = HAD will be unconditionally enabled.

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7.5 Security

7.5.1 Password Description

Feature	Options	Description
Administrator Password	Enter password	Set Administrator Password
User Password	Enter password	Set user Password
Secure Boot Menu	Submenu	Customizable Secure Boot settings

Secure Boot Menu

Feature	Options	Description
System Mode	Info only	Show system mode.
Secure Boot	Info only	Show Secure Boot status.
Secure Boot Control	**Disabled** Enabled	Secure Boot activated when platform Key (PK) is enrolled, system mode is User/Deployed, and CSM function is disabled.
Secure Boot Mode	**Standard** Custom	Secure Boot mode options: If Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication.

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7.6 Boot

Feature	Options	Description
Setup Prompt Timeout	1	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
Bootup NumLock State	On **Off**	Select the keyboard NumLock state after system boot.
Quiet Boot	Disabled **Enabled**	Enables or disables Quiet Boot option.
Fast Boot	Disabled **Enabled**	Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.
SATA Support	**Last Boot SATA Devices Only** All SATA Devices	If Last Boot SATA Devices Only, Only last boot SATA device will be available in Post. If All SATA Devices, all SATA devices will be available in OS and Post.
VGA Support	Auto **EFI Driver**	If Auto, only install Legacy OpRom with Legacy OS and logo will NOT be shown during post. EFI driver will still be installed with EFI OS.
USB Support	Disabled **Full Initial** Partial Initial	If Disabled, all USB devices will NOT be available util after OS boot. If Partial Initial, USB Mass Storage and specific USB port/device will NOT be available before OS boot. If Enabled, all USB devices will be available in OS and Post.
PS2 Deivces Support	Disabled **Enabled**	If Disabled, PS2 devices will be skipped.
Network Stack Driver Support	**Disabled** Enabled	If Disabled, Network Stack Driver will be skipped.
Redirection Support	**Disabled** Enabled	If disable, Redirection function will be disabled.
Boot mode select	Legacy **UEFI**	Select boot mode LEGACY/UEFI.
Boot Configuration	Info only	

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7.7 Save & Exit

Feature	Options	Description
Save Changes and Reset	Save changes and reset the system.	Exit system setup after saving the changes.
Discard Changes and Reset	Reset the system without saving any changes.	Exit system setup without saving the changes.
Save Changes and Reset	Reset the system with saving any changes.	Reset the system after saving the changes.
Discard Changes and Reset	Reset the system and discard any changes.	Reset the system after without the changes.
Save Changes		Save Changes done so far to any of the setup options.
Discard Changes		Discard Changes done so far to any of the setup options.
Restore Default		Restore/Load the Default values for all the setup options.
Save as User Default		Save the changes done so far as User Defaults.
Restore User Default		Restore the User Defaults to all the setup options.
UEFI: Built-in EFI Shell		
Launch EFI Shell from filesystem device		

7.8 Server Mgmt

Feature	Options	Description
BMC Self Test Status	Info only	
BMC Device ID	Info only	
BMC Device Revision	Info only	
BMC Firmware Revision	Info only	
IPMI Version	Info only	
BMC Interface(s)	Info only	

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8 IPMI User Guide

8.1 Introduction

This chapter is written for those who already have a basic understanding of the newest implementation of the baseboard management controller (BMC) of the Intelligent Platform Management Interface (IPMI) specification rev. 2.0. It also describes the OEM extension IPMI command usages which are not listed in the IPMI specification.

8.2 Summary of Commands Supported by BMR-AVR-cPCI

The table below lists all the commands supported by the IPMC. The right most column indicates if a particular command is mandatory or optional for PICMG 3.0/2.9.

Command	IPMI Spec	NetFn	CMD	Description (Required by PICMG 3.0/2.9)
IPM Device "Global" Commands				
Get Device ID	20.1	App	01h	This command is used to retrieve the Intelligent Device's Hardware Revision, Firmware/Software Revision, and Sensor and Event Interface Command specification revision information.
Cold Reset	20.2	App	02h	This command directs the Responder to perform a 'Cold Reset' of itself. (Optional/Optional)
Warm Reset	20.3	App	03h	This command directs the Responder to perform a 'Warm Reset' of itself.
Get Self Test Results	20.4	App	04h	This command directs the device to return its Self Test results, if any. (Mandatory/Mandatory)

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Command	IPMI Spec	NetFn	CMD	Description (Required by PICMG 3.0/2.9)
Get Device GUID	20.8	App	08h	This command returns a GUID (Globally Unique ID), also referred to as a UUID (Universally Unique IDentifier), for the management controller. (Optional/Optional)
Broadcast "Get Device ID"	20.9	App	01h	This is a broadcast version of the 'Get Device ID' command that is provided for the 'discovery' of Intelligent Devices on the IPMB. (Mandatory/Mandatory)
IPMI Messaging Support Commands				
Send Message	22.7	App	34h	The *Send Message* command is used for bridging IPMI messages between channels, and between the system management software (SMS) and a given channel. (Optional/Optional)
BMC Watchdog Timer				
Reset Watchdog Timer	27.5	App	22h	The *Reset Watchdog Timer* command is used for starting and restarting the Watchdog Timer from the initial countdown value that was specified in the *Set Watchdog Timer* command. (Mandatory/Optional)
Set Watchdog Timer	27.6	App	24h	The *Set Watchdog Timer* command is used for initializing and configuring the watchdog timer. The command is also used for stopping the timer. (Mandatory/Optional)
Get Watchdog Timer	27.7	App	25h	This command retrieves the current settings and present countdown of the watchdog timer. (Mandatory/Optional)
Event Commands				
Set Event Receiver	29.1	S/E	00h	This global command tells a controller where to send Event Messages. (Mandatory/Optional)

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Command	IPMI Spec	NetFn	CMD	Description (Required by PICMG 3.0/2.9)
Get Event Receiver	29.2	S/E	01h	This global command is used to retrieve the present setting for the Event Receiver Slave Address and LUN. This command is only applicable to management controllers that act as IPMB Event Generators. (Mandatory/Optional)
Platform Event Message	29.3	S/E	02h	This command may be thought of as a request for the BMC to process the event data that the command contains. Typically, the data will be logged to the System Event Log (SEL). (Mandatory/Optional)
Sensor Device Commands				
Get Device SDR Info	35.2	S/E	20h	This command returns general information about the collection of sensors in a Dynamic Sensor Device. (Mandatory/Optional)
Get Device SDR	35.3	S/E	21h	The 'Get Device SDR' command allows SDR information for sensors for a Sensor Device (typically implemented in a satellite management controller) to be returned. (Mandatory/Optional)
Reserve Device SDR Repository	35.4	S/E	22h	This command is used to obtain a *Reservation ID*. (Mandatory/Optional)
Set Sensor Hysteresis	35.6	S/E	24h	This command provides a mechanism for setting the hysteresis values associated with the thresholds of a sensor that has threshold based event generation. (Optional/Optional)
Get Sensor Hysteresis	35.7	S/E	25h	This command retrieves the present hysteresis values for the specified sensor. (Optional/Optional)
Set Sensor Threshold	35.8	S/E	26h	This command is used to set the specified threshold for the given sensor. (Optional/Optional)
Get Sensor Threshold	35.9	S/E	27h	This command retrieves the threshold for the given sensor. (Optional/Optional)

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Command	IPMI Spec	NetFn	CMD	Description (Required by PICMG 3.0/2.9)
Set Sensor Event Enable	35.10	S/E	28h	This command provides the ability to disable or enable Event Message Generation for individual sensor events. The command is also used to enable or disable sensors in their entirety using the *disable scanning* bit. (Optional/Optional)
Get Sensor Event Enable	35.11	S/E	29h	This command returns the enabled/ disabled state for Event Message Generation from the selected sensor. The command also returns the enabled/ disabled state for scanning on the sensor. (Optional/Optional)
Get Sensor Event Status	35.13	S/E	2Bh	The Get Sensor Event Status command is provided to support systems where sensor polling is used in addition to, or instead of, Event Messages for event detection. (Optional/Optional)
Get Sensor Reading	35.14	S/E	2Dh	This command returns the present reading for sensor. The sensor device may return a stored version of a periodically updated reading, or the sensor device may scan to obtain the reading after receiving the request. (Mandatory/Optional)
Get Sensor Type	35.16	S/E	2Fh	This command is used to assign the Sensor Type and Event/Reading Type to a specified sensor. (Optional/Optional)
FRU Device Commands				
Get FRU Inventory Area Info	34.1	Storage	10h	Returns overall the size of the FRU Inventory Area in this device, in bytes. (Mandatory/Optional)
Read FRU Data	34.2	Storage	11h	The command returns the specified data from the FRU Inventory Info area. (Mandatory/Optional)
Write FRU Data	34.3	Storage	12h	The command writes the specified byte or word to the FRU Inventory Info area. (Mandatory/Optional)

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8.3 CompactPCI Address Map

Since more than one system may be installed in a single chassis, we allocate each IPMB address based on GA input as peripheral cards. The CompactPCI Peripheral Address Mapping Table is given below.

CompactPCI Peripheral Address Mapping			
Geo. Addr.	**IPMB Addr.**	**Geo. Addr.**	**IPMB Addr.**
0	**Disabled**	16	D0h
1	B0h	17	D2h
2	B2h	18	D4h
3	B4h	19	D6h
4	B6h	20	D8h
5	B8h	21	DAh
6	Bah	22	DCh
7	BCh	23	DEh
8	BEh	24	E0h
9	Coh	25	E2h
10	C4h	26	E4h
11	C6h	27	E6h
12	C8h	28	E8h
13	CAh	29	EAh
14	CCh	30	ECh
15	CEh	**31**	**Disabled**

8.4 Communications with IPMC

Operating systems need to use a serial port to communicate with the IPMC. The resource setting of the serial port must be IO: 0x2F0 and IRQ: 7. The communication setting of the serial port must be BaudRate: 9600, DataBit: 8, ParityCheck: None, StopBit: 1, and FlowControl: None. In Windows XP, use "COM6" to communicate with the IPMC.

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8.5 IPMI Sensors List

Sensor Number	Sensor name	Sensor Reading Value of IPMI Get Sensor Reading Command
01h	BMC Watchdog	Timeout action: 000b = no action 001b = Hard Reset 000b = Power Down 011b = Power Cycle 100b - 111b = reserved
11h	3.3V	Raw data of 3.3V sensor
14h	5V	Raw data of 5.0V sensor
05h	12V	Raw data of 12.0V sensor
18h	CPU Temp	Raw data of CPU Temp sensor
19h	SYSTEM Temp	Raw data of SYSTEM Temp sensor

8.6 Relevant Documents

Document Title	Revision	Source
Intelligent Platform Management Interface Specification v2.0	Document Revision 1.1 October 1, 2013	Intel Corp. http://www.intel.com/design/servers/ipmi/spec.htm
PICMG 2.9 D1.0 CompactPCI System Management Specification	January 21, 2000	

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Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

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- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

A Lithium-type battery may be provided for uninterrupted, backup or emergency power.



Risk of explosion if battery is replaced with one of an incorrect type. Dispose of used batteries appropriately.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

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