cPCI-6811AA

RCC/ServerWorks Champion LE-Based 6U *CompactPCI* Motherboard

User's Guide



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Product Model			
Environment to Use	OS: Computer Brand: M/B: CPU: Chipset: BIOS: Video Card: Network Interface Card: Other:		
Detail Description			
Suggestions to ADLINK			

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1

Introduction

The ADLINK cPCI-6811AA Single Board Computer (SBC) is a powerful and flexible CompactPCI universal system/peripheral slot processor board based on the Intel® Pentium® III processor-Low Power. This board is specially designed to add system functional density to 6U CompactPCI platform for communication, high-density servers and Telecom applications. It is also suitable for high-density, high-reliability, and high-availability embedded applications where performance and a rich feature set are mandatory.

The cPCI-6811AA also features an Intel® 82546EB dual port gigabit Ethernet (GbE) controller on the 66MHz 64bit PCI bus. The dual GbE connections can be routed to the rear I/O connector or to a PICMG 2.16 compliant backplane.

1.1 Enhanced Features

The cPCI-6811AA 6U Compact PCI CPU Card adds full control functions over the cPCI-6810. The newly added “full control” allows software controllable hot-swapping.

cPCI-6811AA IPMI Hardware modification

GPIO	Zircon Pin	Signal	In/Out	Description
18	#117	IPMI_RESET#_OUT	Out	Resets the board
5	#27	cPCI_PRESENT#	In	Reflects cPCI_PRESENT#
6	#28	SYSEN#	In	Reflects SYSEN#
2	#24	GA0	In	Geographic address
1	#23	GA1	In	Geographic address
0	#22	GA2	In	Geographic address
28	#124	GA3	In	Geographic address
29	#125	GA4	In	Geographic address
6	#28	HS_LED	Out	Turns on the Hot

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		(Or'd with L_STAT of HB6)		Swap LED
7	#29	IPMI_PWRON# (Or'd with cPCI_BDSEL)	Out	Powers down board. Add one pull-high on GPIO7 (If the PM doesn't boot, the board won't power on)
9	#36	HEALTHY#_OUT (Or'd with on-board healthy#_out)	Out	Healthy signal output that leads to the cPCI bus
13	#31	PWR_GOOD	In	Reflects the system power good signal
32	#67	BDSEL#	In	Reflects the state of Board Select (goes to hot swap controller pin-ON#)
12	#30	L_HEALTHY#	In	Local healthy repeats HEALTHY#_OUT (GPIO9)
27	#123	EJECT	In	Reflects the state of the eject latch
34	#69	L_RESET#	In	Local on-board reset signal
35	#70	BRG_RST#	In	Reflects the state of cPCI reset
33	#68	64EN#	In	Reflects the state of cPCI 64EN#
26	#122	ENUM#	In	Reflects the state of ENUM#

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1.2 Checklist

The cPCI-6811AA series products support both front and rear panel I/O.

1.1.1 cPCI-6811AA Front Board

The cPCI-6811AA CPU module may be equipped with different capacities of RAM, HDD, and PCM depending on requirements. Please check your configurations with your dealer and check that your package is complete and contains the items below. If you discover damaged or missing items, please contact your dealer.

- This User's Manual
- The cPCI-6811AA SBC
- ADLINK CD

Note: The delivered package of the cPCI-6811AA OEM version (non-standard configuration, functionality, customized logo, modified faceplate or package) may vary depending on customized requests.

1.1.2 cPCI-R6820 RTM

The cPCI-R6820 is designed to provide additional I/O functionality through rear I/O connectivity for the cPCI-6811AA. The cPCI-R6820 can be shipped with or without a storage device (IDE HDD or CF card) depending on the options ordered. Please check possible configurations with your dealer. As shipped, the product package should contain the following items:

- The cPCI-R6820 RTM
- The Y-shape Keyboard/Mouse Combo cable

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1.2 Features

1.2.1 cPCI-6811AA Features

- PICMG 2.16 CompactPCI Packet Switching Backplane (cPSB) Compliant
- PICMG 2.9 System Management Bus Compliant
- Standard 6U form factor, 1-slot (4HP) wide
- Design for Intel® Pentium® III processor-Low Power running at FSB 133MHz
- Up to two registered 144-pin SO-DIMM (up to 1GB PC-133 SDRAM)
- 64-bit/66MHz CompactPCI
- Universal operation for both system and peripheral slots
- Full hot-swap support
- On-board up to two 64-bit PMC module slot

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1.3 Functional Block

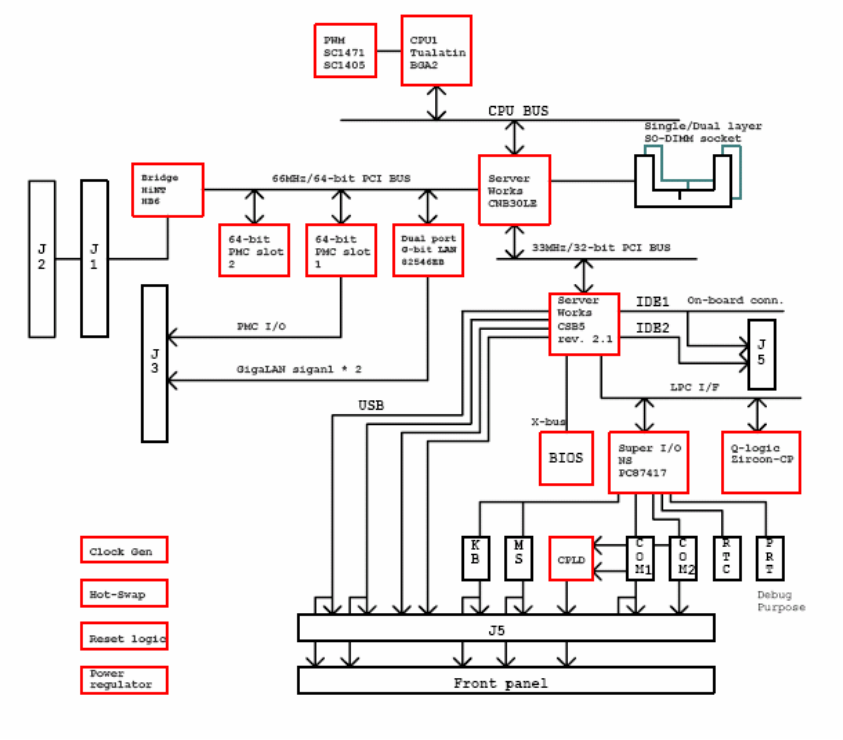


Figure 1. **cPCI-6811AA Block Diagram**

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1.3.1 CompactPCI Bus Interface

The cPCI-6811AA operates in a 6U CompactPCI system. The CompactPCI standard is electrically identical to the PCI local bus standard but has been enhanced to work in harsh environments and support more peripheral slots. Additionally, when used in a Hot Swap compliant backplane and in accordance with the *CompactPCI Hot Swap Specification, PICMG 2.1, Version 1.0,* the cPCI-6811AA supports hosting hot swappable peripherals in a powered system. The cPCI-6811AA can also function in a standard (non-Hot Swap) CompactPCI system without live insertion and extraction capability.

1.3.2 PCI-to-PCI Bridge

The HiNT HB6 is a dual-mode universal PCI-to-PCI Bridge and is used to implement the system/peripheral slot on the cPCI-6811AA. The HB6 non-transparent mode permits independent memory mapping of both primary and secondary buses with powerful configuration options to support intelligent subsystems. The Universal mode permits jumper-less configuration between application to CompactPCI interface at Peripheral Slot and System Slot. With the Universal option, the HB6 Bridge can be configured as a transparent bridge in a System Slot supporting a host, or as a Non Transparent bridge in a Peripheral Slot as an intelligent subsystem. These options allow the cPCI-6811AA board to be inserted into both the Peripheral Slot and the System Slot.

In addition to the 66MHz/64bit capability, allowing the host bus and subsystem bus to operate at different speeds. Together with 64-bit to 32-bit access conversion, system architects can utilize the bridge and connect slower or higher speed controllers on primary or secondary bus, hence supporting independent speed and data bus frequency on either side of the PCI bus.

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Key features

- Large 1kByte total buffering supporting concurrent Primary and Secondary operation as well as traffic isolation.
- Multiple output clock pins and 9 pairs of REQ/GNT signals support up to 9 bus masters directly on secondary bus without external clock buffer and bus arbiter.
- 5V tolerant I/O buffer, EEPROM support for extra register control, Vital Product Data (VPD), 16 general purpose IO interface, and proven PME
- D3 wakeup power management is part of the large array of functionalities available in a single HB6 bridge.

1.3.3 BIOS

The cPCI-6811AA adopts the Award BIOS with a 4-Mbit flash ROM implemented to load the BIOS. A boot block device is used to allow recovery of the BIOS in the event of a catastrophic failure (power fail during BIOS update). The BIOS supports the following features:

- CPU/memory speed auto-detection
- DMI BIOS Support: Desktop Management Interface (DMI) allows users to download system hardware-level information such as CPU type, CPU internal/external frequencies, and memory size
- Green Function: APM/ACPI compliant Power management via BIOS, activated through mouse/keyboard movement or other wake-up events
- PCI Plug-and-Play support
- Intel pre-boot execution environment (PXE) support
- PICMG2.1 CompactPCI hot-swap specification Rev. 1.0 support on CompactPCI I/O bus

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1.3.4 Processor

The cPCI-6811AA motherboard is based on the RCC/ServerWorks Champion LE chipset and supports a single Intel® Pentium® III processor-Low Power. The supported CPU package is a micro-FCBGA.

The Intel® Pentium® III processor-Low Power is a 0.18-micron product, which is a highly integrated assembly with all its immediate system-level support. This low power version of the Intel® Pentium® III processor runs at a lower voltage than the desktop version.

The 256kB on-die transfer L2 cache is integrated with the CPU, eliminating the need for separate components and improving performance. The Mobile Intel Pentium III Processor also operates with a 100/133MHz Front Side Bus for faster access to memory and data. The FSB speed depends on the CPU type with its core speed automatically detected by the BIOS.

1.3.5 Supported Memory

The cPCI-6811AA supports PC100/PC133 registered SO-DIMMs only. The SDRAM speed, type and size can be determined by the BIOS reading the DIMM presence detect bits on the SMBus. The DRAM timing register, which provides the DRAM speed control for the entire array, must be programmed to use the parameters of the slowest installed SDRAM. The DRAM interface supports 64Mbit, 128Mbit, and 256Mbit technology, allowing up to 512Mbytes per double-sided SO-DIMM. The cPCI-6811AA can support up to 1GB of SDRAM memory with two 144-pin SO-DIMMs. .

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1.3.6 Interrupts

Two enhanced interrupt controllers provide the cPCI-6811AA with a total of 15 interrupt inputs. Interrupt controller features include support for:

- Level-triggered and edge-triggered inputs
- Individual input masking
- Fixed and rotating priorities

Interrupt sources include:

- Counter/Timers
- Serial I/O
- Keyboard
- Printer port
- Floppy disk
- IDE interface
- Real-Time clock
- On-board PCI devices

Enhanced capabilities include the ability to configure each interrupt level for active high going edge or active low-level inputs. The cPCI-6811AA interrupt controllers reside in the CNB30LE.

1.3.7 DMA

Two enhanced DMA controllers are provided on the cPCI-6811AA or use by the onboard peripherals. The cPCI-6811AA DMA controllers reside in the CNB30LE device.

1.3.8 Real-Time Clock

The super I/O PC87417 provides DS1287 compatible Real-Time Clock. It provides a Y2K compliant century calendar as well as a time of day function. In addition, 242 bytes of battery-backed-up CMOS RAM accessed through 70-71h and 72-73h are available for use by the BIOS. A separate 3V coin cell battery (PANSONIC CR2032 or compatible) provides battery-back-up

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1.3.9 Baseboard Management

The Zircon CP baseboard management controller is used to manage all aspects of the system board. The features are summarized as follows.

- ARM7/TDMI controller with internal 14kB SRAM
- IPMB interface
- External 16-bit flash ROM interface with ROM size 1MB
- Six channels A-to-D converter for voltage monitoring, 10-bit resolution
- Provide a heartbeat timer
- Support CPU internal instruction error input (IERR#)
- Support CPU floating point error input (FERR#)

QLogic provides a firmware suite supporting the Intelligent Platform Management Interface (IPMI) specification, including the Intelligent Platform Management Bus (IPMB). See appendix A for an in-depth programmers guide.

1.3.10 Power Ramp Circuitry

The cPCI-6811AA features a power controller with power ramp circuitry to allow the board's voltages to be ramped in a controlled fashion. The power ramp circuitry eliminates any large voltage or current spikes caused by hot swapping boards. This controlled ramping is a requirement of the *CompactPCI Hot Swap specification, PICMG 2.1, Version 1.0*. The cPCI-6811AA power controller unconditionally resets the board when it detects that the 3.3V, 5V, and 12V supplies are below an acceptable operating limit. These limits are defined as 4.75V (5V supply), 3.0V (3.3V supply), and 10.0V (+12V supply).

1.3.11 Watchdog Timer

The cPCI-6811AA implements a watchdog timer embedded in the NS PC87417. The watchdog timer is an 8-bit down counter with 1-minute resolution. Programmable I/O ports 10h -12h of bank 3 are used to configure the watchdog timer. The 8-bit timer is programmable from 1-255 minutes. Once a value is set, the timer begins to count down. Any movement of keyboard, mouse, or software will reset the value and reload the timer again. The Watchdog output is connected to “reset”. When the system hangs without software re-trigger, the system will be reset. The watchdog register is cleared on power-up, enabling system software to take appropriate action.

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1.3.12 Ethernet Interfaces

The onboard Intel 82546EB dual-port gigabit Ethernet controller provides two Ethernet interfaces. The 82546EB is implemented on 64-bit/66-MHz PCI bus. The 82546EB supports IEEE 802.3x compliant flow control and IEEE 802.3ab compliant 10/100/1000 Mbps auto-negotiation. The Ethernet interfaces are connected to J3, which is compliant to PICMG 2.16 specification.

Each Ethernet interface is assigned a unique Ethernet Address of the form 003064XXXXXh where XXXXX is the unique number assigned to a particular interface and 003064 is the ADLINK Company ID. Each of the board's Ethernet Addresses is displayed on a label attached to the board. LED drive signals for Ethernet link status, activity, and speed are routed to the front panel.

1.3.13 IDE Interface

The fast IDE interface on cPCI-6811AA supports up to four IDE devices including hard disk drives and CD ROMs. Each IDE device can have independent timing. The IDE interface supports PIO IDE transfers of up to 14MB/s and the Bus Master IDE up to 100MB/s. The CSB5's IDE system contains two independent IDE signal channels. They be electrically isolated and are configured to the standard primary and secondary channels.

1.3.14 Universal Serial Bus (USB)

The root hub integrated in the CSB5 supports 4 USB serial ports. Two ports are available on the front panel, with the other 2 ports routed to the rear I/O board through J5. Additional ports can be added through the use of an external USB hub. USB allows for the easy addition of peripherals such as mouse, keyboard, speakers, etc. Transfer up to 24Mb/s is supported. The cPCI-6811AA provides the standard 0.5A at 5V to the peripherals. The power to each port is protected by a single poly-switch (this current rating allows for inrush currents).

1.3.15 Serial I/O

Two serial ports are supported on the cPCI-6811AA. The EIA232 drivers and receivers reside on board. COM1 is implemented as an RJ45 connector on the front panel. Both COM1 and COM2 are available on rear I/O board. The BIOS will initialize the serial ports as COM1 and COM2 with default ISA I/O base addresses 3F8h and 2F8h respectively. This default configuration also assigns COM1 to IRQ4 and COM2 to IRQ3. The supported baud rate are 1200, 2400, 4800, 9600, 19200, 38400, 57600, and 115200 bps.

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1.3.16 Keyboard/Mouse Controller

Two 6-pin circular DIN connectors are located on the front panel of single-processor version of cPCI-6811AA, for example cPCI-6811AA, for keyboard and mouse connections. The power provided to the keyboard and mouse is protected by a poly-switch rated at 1.1A. The keyboard and mouse interface are also available on the rear I/O board

1.4 Specifications

1.4.1 cPCI-6811AA Specifications

CompactPCI Compliancy

- PICMG 2.0 CompactPCI core specification R3.0
- PICMG 2.1 CompactPCI hot swap R1.0
- PICMG 2.16 CompactPCI packet switching backplane (cPSB) R1.0
- PICMG 2.9 System Management Bus R1.0
- PCI Rev 2.1 complaint

Form Factor

- Standard 6U CompactPCI (board size: 233.35mm x160mm)
- Single-slot (4 TE/HP, 20.32mm) width, incl. housing for 2.5" HDD

CPU / Cache

- Intel® Pentium® III processor – Low Power (uFCBGA) up to 1033MHz with 512k on-die L2 cache

Chipset

- ServerWorks LE-III

Host Memory

- Up to four 144-pin SO-DIMM sockets
- Capacity up to 1 Gigabytes of PC-133 Registered ECC SDRAM

BIOS: ADLINK Enhanced Award / Phoenix BIOS

- Support Intel® Pre-boot Execution Environment (PXE) version 2.x, WFM 2.0. Include BIOS setup options and boot from LAN
- Support DMI / SMBIOS 2.3

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- CPU, memory operating frequency auto-detection
- Bootable from USB storage devices including USB-Floppy, USB-ZIP USB-CD-ROM, and USB-HDD.
- Option OEM BIOS features
  - ✓ Customized OEM splash image / power on screen
  - ✓ Serial remote-console redirected to serial COM1 port

Note: Due to BIOS segment limitations, enabling the remote console function may occupy the same memory space as other ROM mapping add-on or boot-up devices such like Pre-boot Agent of Ethernet Boot ROM, SCSI Boot ROM, or add-on EIDE Boot ROM. It is recommended only one ROM-mapping add-on or boot-up device be enable when enabling the remote console function.

Gigabit Ethernet

- Two Gigabit Ethernet (GbE) ports with Intel® 82546EB Ethernet controller, based on local 66MHz/64-bit PCI bus
- Support 1000Base-T, 100Base-TX and 10Base-T (IEEE 802.3, 802.3u, and 802.3ab)
- IEEE802.3x compliant flow control, support auto-negotiation, and link setup
- GbE connection on PICMG 2.16 PSB or on RTM rear access
- Speed and connection status LED on the front panel

USB Interface

- Supports up to four USB version 1.1 ports with integrated USB host controller. Two USB ports (USB-0 and USB-1) are BIOS configurable for front or rear access. Two USB ports (USB-2 and USB-3) are rear access only.
- USB ports provide 0.5A @ 5V power for peripheral devices with over current protection

IDE Ports

- Bus master IDE controller supports two ultra ATA-100 interfaces.
- Primary IDE is on board with 44-pin IDE connector
- Both Primary and Secondary IDE ports are on J5 for RTM extension.

Super I/O, WDT and Hardware Monitoring

- Chipset: NS PC87417 low pin-count (LPC) Server I/O controller
- Two 16C550 UART compatible RS-232 COM ports. COM1 on the front with RJ-45 type connector. COM2 is on the J3 and can be accessed on the RTM.

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- PS2 keyboard and mouse connector:
- W82782D built-in monitoring CPU temperatures, FAN speed, system temperature, V core, and DC voltages.
- Watchdog timer: Programmable I/O port 10h - 12h of bank 3 to configure watchdog timer, programmable 8-bit timer 1-255 minutes.
- Real -Time Clock and Nonvolatile Memory: DS1287 compatible Real-Time Clock. 242 bytes CMOS RAM backup by a separate 3V cell battery (PANSONIC CR2032 or compatible)

IPMI Interface

- Supports PICMG 2.9 secondary system managing bus. Implements IPMI functions as defined in the IPMI specification v 1.0
- Qlogic Zircon CP Baseboard Management Controller (BMC) with 14k bytes internal SRAM, 1MB external flash ROM

Front Panel LED Indicators and Reset

- 4 LED on the front panel including storage access LED (RED), Power LED (GREEN), Hot-Swap status (Blue), and Watchdog timer LED (Yellow).
- 4 LED to indicate GbE ports status including speed (yellow) and link/activity (green)
- Flush tact switch for system reset

PCI Bus and CompactPCI connectors

- HiNT HB6 Universal PCI to PCI bridge
- 64-bit/66MHz, support 4 bus-mastering devices
- 32-bit/33MHz, support 7 bus-mastering devices

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1.4.2 cPCI-R6820 RTM Specifications

Form Factor

- Standard 6U CompactPCI rear I/O (board size: 233.35mmx80mm)
- 1-slot (4TE/HP, 20.32mm) wide, include space of 2.5 inches HDD

Connection Interface

- RTM signals are from CompactPCI rJ3 and rJ5 connectors, without rJ1, rJ2 and rJ4. Use AB type connector on rJ5

Faceplate I/O Connectors

- Two USB ports: USB2, USB3 (type A connector)
- VGA port on DB-15 connector (only available for the series with VGA chipset on front board)
- Keyboard/mouse combo PS2 mini-DIN 6-pin connector
- Two GbE ports on RJ-45 connectors
- Serial COM2 ports on RJ-45 connectors

IDE Connectors

- Primary IDE supported on one 40-pin connector
- Secondary IDE supported on one 40-pin IDE connector, one 44-pin connector for 2.5 inches HDD or flash drive; and one CompactFlash type-II socket.

1.4.3 Common Spec. for cPCI-6811AA and RTM

Flash Storage Support Options:

- DiskOnModule via the 40-pin IDE on RTM, 16-256MB
- CompactFlash card via the CF socket on RTM, 8-512MB
- 2.5 inches Flash disk drive on front board or RTM, 32MB-2GB

OS Compatibility

- Microsoft® Windows NT, Windows 2000, Windows XP, Red Hat Linux 7.2
- Other OS support upon request

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Environment

- Operating temperature: 0 - 50 °C (Note 1)
- Storage temperature: -20 - 80 °C
- Humidity: 5% - 95% non-condensed
- Shock: 15G peak-to-peak, 11ms duration, 3 axes, 3 times/axis non-operation
- Vibration: (Note 3)
  - ✓ None-operation: 1.88Grms, 5-500Hz, 3 axes, with package
  - ✓ Operation: 0.5Grms, 5-500Hz, each axis with flash disk drive

Safety Certificate and Test

- CE, FCC Class B
- HALT (temperature and vibration stress) verified
- All plastic material, PCB and Battery used are all UL-94V0 certified
- Designed for NEBS 3.0 requirement
- MTBF: >100,000 hours

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Power Requirement (Typical)

Typical Current and Maximum Current	+5V (+/-5%)	+3.3V (+/-5%)	+12V (+/-5%)	-12V (+/-5%)
cPCI-6811AA/P10/M1G	2.50A 3.88A	4.10A 14.636A	3mA 8mA	0mA 0mA
cPCI-6811AA/P10/M1G (Without PMC, VGA cards & RTM)	1.44A 3.73A	3.64A 14.636A	3mA 8mA	0mA 0mA
cPCI-6811AA/P10/M1G with HDD	3.16A 3.88A+HDD	4.76A 14.636A	3mA 8mA	0mA 0mA

Test conditions

- Single LV P-III 1GHz
- Memory: 1GB (512MB x 2)
- HDD: FUJITSU MHR2040AT 40GB installed on RTM (Max. current requirement is 0.55A @ +5V
- CompactFlash: PQI 64MB Flash Card
- PMC card: ADLINK PMC-8615 Gigabit Ethernet Card
- PMC VGA card: ADLINK PMC-8217V (only available with CRUX-SP)

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I/O Connectivity

I/O	cPCI-6811AA		RTM (cPCI-R6820)		
	Faceplate	Board	J3/J5	Faceplate	Board
Serial Port (COM1)	--	--	J5	RJ-45	--
Serial Port (COM2)	--	--	J5	--	10-pin Header
PS2 Keyboard	--	--	J5	PS2	--
PS2 Mouse	--	--	J5	PS2	--
VGA	--	--	J5	DB-15	--
USB (port 0, port 1)	USB x 2	--	J5	--	--
USB (port 2, port 3)	--	--	J5	USB x 2	--
Gigabit Ethernet Port 1	--	2.16	J3	RJ-45	--
Gigabit Ethernet Port 2	--	2.16	J3	RJ-45	--
ATA-100 Primary IDE	--	44-pin	J5	--	40-pin
ATA-100 Secondary IDE	--	--	J5	--	40-pin 44-pin CF-type 2
PC Beeper	--	--	J5	--	4-pin Header
General Purpose LED	Y	--	--	--	--
Reset button	Y	--	--	--	--
PMC #1	--	Y	--	--	--
PMC #2	--	Y	J3	--	--

Table 1: I/O Connectivity

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1.5 Model Variations

The cPCI-6811AA series products include the following 4 base configurations. All models have the CPU pre-mounted. The number of SO-DIMM sockets and PMC slots are varied depending on the model. If a HDD is installed on board, it may occupy and sacrifice one PMC socket space. Note that the RTM is sold separately and are not listed in the following table.

	I	II
	cPCI-6811AA/P10/M512	cPCI-6811AAB/P10/M1G
Slot Width	1-slot	1-slot
CPU	Single P III-1GHz	Single P III-1GHz
Memory sockets	Single x 2	Single x 2
Max. SO-DIMM#	2	2
Memory Configuration	512MB	1 GB
2.5 inches HDD installation	Possible	Possible
PMC slot # (without HDD)	2	2
PMC slot # (with HDD)	1	1
Onboard VGA	N/A	N/A
PS/2 Keyboard	On RTM	On RTM
PS/2 mouse	On RTM	On RTM

Table 2: CPCI-6811AA Model Table

The following table lists the recommended PMC modules made by ADLINK, which are compatible with 6820 series SBC.

Model number	Description/Configuration
PMC-8217	SMI SM-721 VGA PMC card
PMC-8615	Single Port 64-bit/66MHz Gigabit Ethernet PMC card
PMC-8611	Single Port 32-bit/33MHz Fast Ethernet PMC card
PMC-8670	Port80 Display PMC card

Table 3: Recommended PMC Modules

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The following table lists the recommended chassis available from ADLINK, which are compatible with the cPCI-6811AA series SBC.

Chassis	Description/Configuration
cPCIS-6130R	19” 1U high standard depth chassis with RIO
cPCIS-6400X	19” 4U high chassis, 4-slot I/O, 64-bit BP, ATX Power
cPCIS-6400U	19” 4U high chassis, 4-slot I/O, 64-bit BP, Redundant cPCI Power
cPCIS-3140	19” 8U high chassis, 7-slot I/O, 64-bit BP, Redundant AC Input Power with Door, all sub-models
cPCIS-3330/64	19” 9U high chassis, 7-slot I/O, 64-bit BP, Redundant cPCI Power, all sub-models
cPCIS-3100BLS	19” 8U high chassis, 9-slot compute blades, Redundant AC Input Power with Door, all models
cPCIS-3300BLS	19” 9U high PICMG 2.16 chassis, 12 node slots with 2 fabric slots and three 6U cPCI redundant power slots

Table 4: Recommended Chasses

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Jumpers and Connectors

This chapter will familiarize the user with the cPCI-6811AA before getting started; it will provide information about the board layout, connector definitions, and jumper setup. This includes the following information:

- cPCI-6811AA board outline and illustration
- cPCI-R6820 board outline and illustration
- Connector pin assignments

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2.1 cPCI-6811AA Board Outline and Illustratoin

2.1.1 cPCI-6811AA Top and Front View

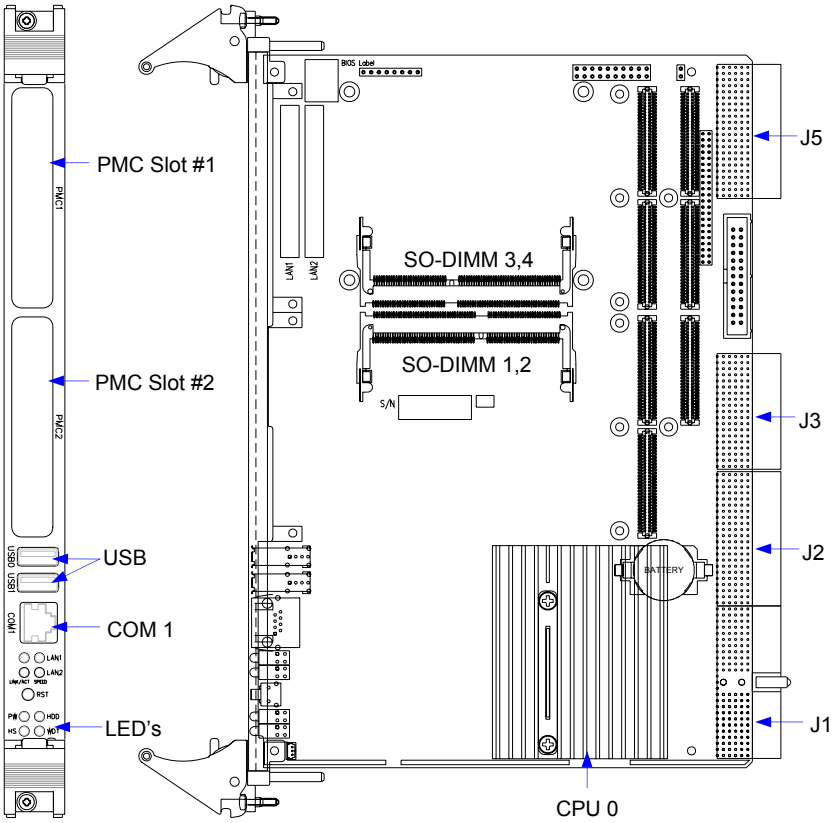


Figure 2. Top and Front View of cPCI-6811AA

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cPCI-6811AA Table

	cPCI-6811AA/P10
No. of Memory sockets	2
SO-DIMM 1, 2	Single SODIMM
SO-DIMM 3, 4	Single SODIMM
Max. Memory	1.0 GB
HDD Installation	Possible
PMC slot # (without HDD)	2
PMC slot # (with HDD)	1 *(1)*

Table 5: cPCI-6811AA Table

Note:

1. If a HDD is installed, then PMC slot #1 becomes unavailable.

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2.2 cPCI-R6820 Board Outline and Illustratoin

2.2.1 cPCI-R6820 Top and Front View

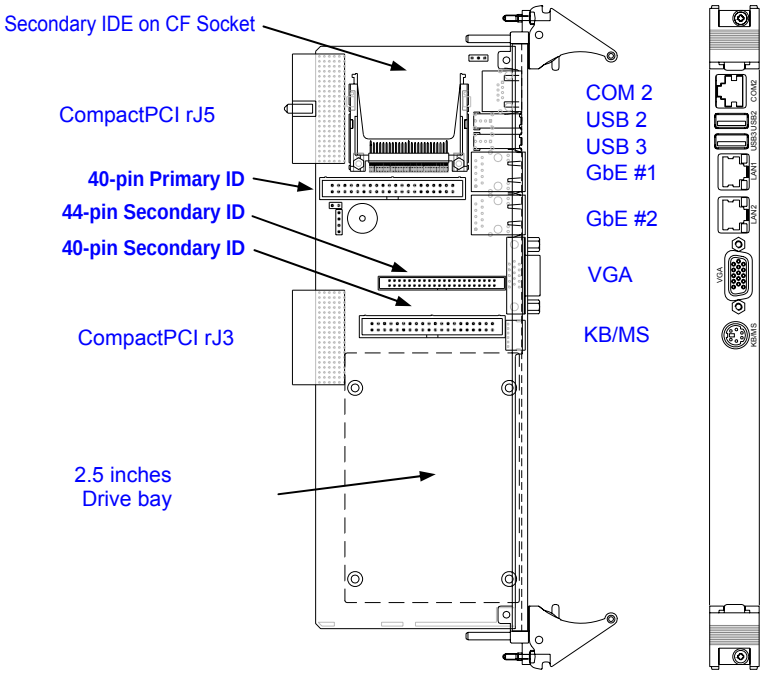
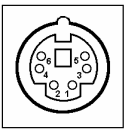


Figure 3. Top and front View of cPCI-R6820

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2.3 Connectors Pin Assignment

2.3.1 Keyboard and Mouse Combo Connector



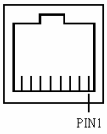
Pin #	Signal	Function
1	KBDATA	Keyboard Data
2	MSDATA	Mouse Data
3	GND	Ground
4	+5V	Power
5	KBCLK	Keyboard Clock
6	MSCLK	Mouse Clock

Table 6: Keyboard and Mouse Combo Connector

Note: Keyboard and Mouse Combo Connector is available on the cPCI-R6820 RTM only. A Y-cable is shipped with the RTM and can be use to connect a PS/2 keyboard and mouse at the same time. Direct connection of a PS/2 keyboard is also supported for applications that do not require a mouse.

2.3.2 Serial Port Connectors

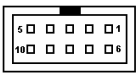
Serial Port on RJ-45 Connector



Pin #	Signal Name
1	DCD, Data carrier detect
2	RTS, Request to send
3	DSR, Data set ready
4	**TXD, Transmit data**
5	RXD, Receive data
6	GND, ground
7	CTS, Clear to send
8	DTR, Data terminal ready

Table 7: COM1 on front board or COM2 on the RTM

Serial Port on 10-pin Header Connector



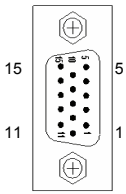
Pin #	Signal Name
1	DCD: Data Carrier Detect
2	RXD: Receive Data
3	TXD: Transmit Data
4	DTR: Data Terminal Ready
5	Ground
6	DSR: Data Set Ready
7	RTS: Request to Send
8	CTS: Clear to Send

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9	RI: Ring Indicate
10	No Connect

Table 8: COM1 on the RTM

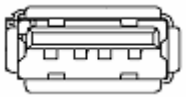
2.3.3 VGA Connector



Signal Name	Pin #	Pin #	Signal Name
Red	1	2	Green
Blue	3	4	N.C.
GND	5	6	GND
GND	7	8	GND
+5V.	9	10	GND
N.C.	11	12	N.C.
HSYNC	13	14	VSYNC
NC	15		

Table 9: VGA Connector on RTM (only available for the series with VGA chip on front board)

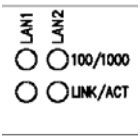
2.3.4 USB Connector



Pin #	Signal Name
1	VCC
2	USB-
3	USB+
4	Ground

Table 10: USB Connector

2.3.5 LED for Gigabit Ethernet Ports

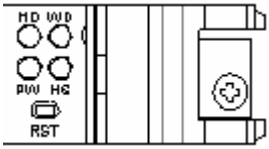


LED	Color	Status	Description
Link Speed LED	Green	OFF	10 or 100 Mbps
		ON	1000 Mbps
Link / Activity LED	Amber	OFF	No Link
		ON	Linked
		Blinking	Port Accessing

Table 11: LED indicators on the GbE ports

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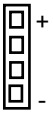
2.3.6 General Purpose LED definitions



LED	Color	Status	Description
IDE Media Access	Red	OFF	IDE idle
		ON	IDE access
Power OK	Green	OFF	System is not power-on or power failed
		ON	Power ON
Hot swappable status	Blue	OFF	Board inserted and power on OK.
		ON	Board inserted but not power on yet.

Table 12: General Purpose LED definitions

2.3.7 Speaker connector on RTM

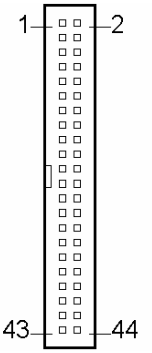


Pin #	Signal Name
1	SPK-
2	GND
3	GND
4	SPK+

Table 13: Speaker Connector on RTM

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2.3.8 44-pin IDE Port



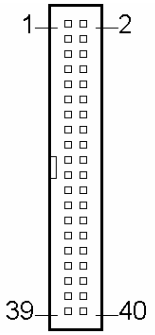
Signal	Pin #	Pin #	Signal
RESET-	1	2	Ground
DD7	3	4	DD8
DD6	5	6	DD9
DD5	7	8	DD10
DD4	9	10	DD11
DD3	11	12	DD12
DD2	13	14	DD13
DD1	15	16	DD14
DD0	17	18	DD15
Ground	19	20	N.C (key pin)
DMARQ	21	22	Ground
DIOW-	23	24	Ground
DIOR-	25	26	Ground
IORDY	27	28	CSEL
DMACK-	29	30	Ground
INTRQ	31	32	reserved
DA1	33	34	PDIAG-
DA0	35	36	DA2
CS0-	37	38	CS1-
DASP-	39	40	Ground
+5V	41	42	+5V
Ground	43	44	TYPE-

Table 14: 44-pin IDE connector

Note: Primary IDE is on the front board (CN8) and the Secondary IDE is on the RTM.

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2.3.9 40-pin IDE Port



Signal	Pin #	Pin #	Signal
RESET-	1	2	Ground
DD7	3	4	DD8
DD6	5	6	DD9
DD5	7	8	DD10
DD4	9	10	DD11
DD3	11	12	DD12
DD2	13	14	DD13
DD1	15	16	DD14
DD0	17	18	DD15
Ground	19	20	+5V (for DOM)
DMARQ	21	22	Ground
DIOW-	23	24	Ground
DIOR-	25	26	Ground
IORDY	27	28	CSEL
DMACK-	29	30	Ground
INTRQ	31	32	reserved
DA1	33	34	PDIAG-
DA0	35	36	DA2
CS0-	37	38	CS1-
DASP-	39	40	Ground

Table 15: 40-pin Primary and Secondary IDE channels on the RTM

2.3.10 IPMB Interface on RTM

Pin #	Signal Name
1	IPMB_CLK
2	GND
3	IPMB_DATA
4	IPMB_PWR
5	N.C

Table 16: IPMI Interface on RTM

The IPMB interface is connected to the rJ5 of the RTM. The IPMB_PWR is connected to pin-C1 of the rJ5.

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2.3.11 CompactPCI J1 Pin Assignments

Pin	Z	A	B	C	D	E	F
25	GND	+5V	REQ64#	ENUM# (4)	+3.3V	+5V	GND
24	GND	AD [1]	+5V	V (I/O) (1)	AD [0]	ACK64#	GND
23	GND	+3.3V	AD [4]	AD [3]	+5V	AD [2]	GND
22	GND	AD [7]	GND	+3.3V	AD [6]	AD [5]	GND
21	GND	+3.3V	AD [9]	AD [8]	M66EN	C/BE [0]#	GND
20	GND	AD [12]	GND	V (I/O) (1)	AD [11]	AD [10]	GND
19	GND	+3.3V	AD [15]	AD [14]	GND	AD [13]	GND
18	GND	SERR#	GND	+3.3V	PAR	C/BE [1]#	GND
17	GND	+3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	GND	V (I/O) (1)	STOP#	LOCK#	GND
15	GND	+3.3V	FRAME#	IRDY#	BDSEL	TRDY#	GND
12-14	Key						
11	GND	AD [18]	AD [17]	AD [16]	GND	C/BE [2]#	GND
10	GND	AD [21]	GND	+3.3V	AD [20]	AD [19]	GND
9	GND	C/BE[3]#	IDSE	AD [23]	GND	AD [22]	GND
8	GND	AD [26]	GND	V (I/O) (1)	AD[25]	AD [24]	GND
7	GND	AD [30]	AD [29]	AD [28]	GND	AD [27]	GND
6	GND	REQ#	GND	+3.3V	CLK	AD [31]	GND
5	GND	Reserved (1)	Reserved (1)	PCIRST#	GND	GNT#	GND
4	GND	IPMB_PWR	HEALTHY#	V (I/O) (1)	INTP (1)	INTS	GND
3	GND	INTA#	INTB#	INTC#	+5V	INTD#	GND
2	GND	TCK (3)	+5V	TMS (2)	TDO (1)	TDI (2)	GND
1	GND	+5V	-12V	TRST# (3)	+12V	+5V	GND
Pin	Z	A	B	C	D	E	F

Table 17: CompactPCI J1 pin assignments

Note:

1. These signals are not connected.
2. These signals are pulled high on the board.
3. These signals are pulled low on the board.
4. ENUM# can be routed to IRQ 3 or IRQ 9 based on the hardware configuration. There is a BIOS setting to Enable/Disable the ENUM# function. It is disabled by the BIOS by default and the factory default hardware configuration is IRQ 9. To support PICMG 2.1 Hot Swap for peripheral boards, the backplane should bus all peripheral slots ENUM# together to the system slot and the ENUM# function enabled in the BIOS.

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2.3.12 CompactPCI J2 Pin Assignments

Pin	Z	A	B	C	D	E	F
22	GND	GA4 (2)	GA3 (2)	GA2 (2)	GA1 (2)	GA0 (2)	GND
21	GND	CLK6	GND	BRSV (1)	BRSV (1)	BRSV (1)	GND
20	GND	CLK5	GND	BRSV (1)	GND	BRSV (1)	GND
19	GND	GND	GND	IPMBSDA (1)	IPMBSCL (1)	IPMBALR (1)	GND
18	GND	BRSV (1)	BRSV (1)	BRSV (1)	GND	BRSV (1)	GND
17	GND	BRSV (1)	GND	PRST#	REQ6#	GNT6#	GND
16	GND	BRSV (1)	BRSV (1)	DEG#	GND	BRSV (1)	GND
15	GND	BRSV (1)	GND	FAL#	REQ5#	GNT5#	GND
14	GND	AD [35]	AD [34]	AD [33]	GND	AD [32]	GND
13	GND	AD [38]	GND	V (I/O) (1)	AD [37]	AD [36]	GND
12	GND	AD [42]	AD [41]	AD [40]	GND	AD [39]	GND
11	GND	AD [45]	GND	V (I/O) (1)	AD [44]	AD [43]	GND
10	GND	AD [49]	AD [48]	AD [47]	GND	AD [46]	GND
9	GND	AD [52]	GND	V (I/O) (1)	AD [51]	AD [50]	GND
8	GND	AD [56]	AD [55]	AD [54]	GND	AD [53]	GND
7	GND	AD [59]	GND	V (I/O) (1)	AD [58]	AD [57]	GND
6	GND	AD [63]	AD [62]	AD [61]	GND	AD [60]	GND
5	GND	C/BE [5]#	GND	V (I/O) (1)	C/BE [4]#	PAR 64	GND
4	GND	V (I/O) (1)	BRSV (1)	C/BE [7]#	GND	C/BE [6]#	GND
3	GND	CLK4	GND	GNT3#	REQ#4	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND
Pin	Z	A	B	C	D	E	F

Table 18: CompactPCI J2 pin assignments

Note:

1. These signals are not connected.
2. These signals are pulled high on the board.
3. These signals are pulled low on the board.

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2.3.13 CompactPCI J3 and rJ3 Pin Assignments

Pin	Z	A	B	C	D	E	F
19	GND	**GND**	**+12V** (1)	**GND**	**-12V** (1)	**GND**	GND
18	GND	LPa_DA0+	LPa_DA0-	**GND**	LPa_DC0+	LPa_DC0-	GND
17	GND	LPa_DB0+	LPa_DB0-	**GND**	LPa_DD0+	LPa_DD0-	GND
16	GND	LPb_DA1+	LPb_DA1-	**GND**	LPb_DC1+	LPb_DC1-	GND
15	GND	LPb_DB1+	LPb_DB1-	**GND**	LPb_DD1+	LPb_DD1-	GND
14	GND	**+3.3V** (1)	**+3.3V** (1)	**+3.3V** (1)	**+5V** (1)	**+5V** (1)	GND
13	GND	PMCIO5	PMCIO4	PMCIO3	PMCIO2	PMCIO1	GND
12	GND	PMCIO10	PMCIO9	PMCIO8	PMCIO7	PMCIO6	GND
11	GND	PMCIO15	PMCIO14	PMCIO13	PMCIO12	PMCIO11	GND
10	GND	PMCIO20	PMCIO19	PMCIO18	PMCIO17	PMCIO16	GND
9	GND	PMCIO25	PMCIO24	PMCIO23	PMCIO22	PMCIO21	GND
8	GND	PMCIO30	PMCIO29	PMCIO28	PMCIO27	PMCIO26	GND
7	GND	PMCIO35	PMCIO34	PMCIO33	PMCIO32	PMCIO31	GND
6	GND	PMCIO40	PMCIO39	PMCIO38	PMCIO37	PMCIO36	GND
5	GND	PMCIO45	PMCIO44	PMCIO43	PMCIO42	PMCIO41	GND
4	GND	PMCIO50	PMCIO49	PMCIO48	PMCIO47	PMCIO46	GND
3	GND	PMCIO55	PMCIO54	PMCIO53	PMCIO52	PMCIO51	GND
2	GND	PMCIO60	PMCIO59	PMCIO58	PMCIO57	PMCIO56	GND
1	GND	VIO (2)	PMCIO64	PMCIO63	PMCIO62	PMCIO61	GND
Pin	Z	A	B	C	D	E	F

Table 19: CompactPCI J3 and rJ3 pin assignments

Note:

1. The +3.3V, +5V and +/-12V power lines are supplied from the main board to the RTM.
2. The VIO is connected to the VIO plane (default is +5V) of the PMC slot #2.

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2.3.14 CompactPCI J5 and rJ5 Pin Assignments

Pin	Z	A	B	C	D	E	F
22	GND	DA2	C-	CS3-	DA1	DASP-	GND
21	GND	DIOW-	DMACK-	DIOR-	PDIAG-	DA0	GND
20	GND	DD0	DD15	INTRQ	DMARQ	IORDY	GND
19	GND	DD12	DD2	DD13	DD1	DD14	GND
18	GND	DD5	DD10	DD4	DD11	DD3	GND
17	GND	DRESET-	DD7	DD8	DD6	DD9	GND
16	GND	USB-0+ (5)	USB-0- (5)	**GND**	USB-1+ (5)	USB-1- (5)	GND
15	GND	SMUX (4)	**GND**	SMUX (4)	**GND**	SMUX (4)	GND
14	GND	SMUX (4)	SMUX (4)	SMUX (4)	SMUX (4)	SMUX (4)	GND
13	GND	**+5V** (2)	**+5V** (2)	**+5V** (2)	**+3.3V** (2)	**+3.3V** (2)	GND
12	GND	DDCCLK	DDCDAT	**GND**	**GND**	**GND**	GND
11	GND	VSYNC	HSYNC	BLUE	GREEN	RED	GND
10	GND	USB-2+	USB-2-	**GND**	USB-3+	USB-3-	GND
9	GND	RSVD (1)	RSVD (1)	**GND**	RSVD (1)	RSVD (1)	GND
8	GND	SDA2	SDC-	SDCS3-	SDA1	SDASP-	GND
7	GND	SDIOW-	SDDACK-	SDIOR-	SPDIAG-	SDA0	GND
6	GND	SDD0	SDD15	SINTRQ	SDDREQ	SDIORDY	GND
5	GND	SDD12	SDD2	SDD13	SDD1	SDD14	GND
4	GND	SDD5	SDD10	SDD4	SDD11	SDD3	GND
3	GND	SDRESET-	SDD7	SDD8	SDD6	SDD9	GND
2	GND	MSDATA	MSCLK	KBDATA	KBCLK	PCBEEP	GND
1	GND	IPMB_CLK	IPMB_DAT	IPMB_PWR	RSVD (1)	USB_OC(3)	GND
Pin	Z	A	B	C	D	E	F

Table 20: CompactPCI J5 and rJ5 pin assignments

Note:

1. The pins are reserved with no connection.
2. The 3.3V and 5V power lines are supplied from the main board to the RTM.
3. USB_OC is the USB over-current feedback from the RTM to main board.
4. The SMUX signals are used for serial COM port extension.
5. USB Port 1 and 2 are not used on the cPCI-R6820 RTM.

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2.3.15 PMC Connector Pin Assignments

PMC J11/J21 and J12/J22 Connector Pin Assignments

Signal Name	J11 J21 Pin #	J11 J21 Pin #	Signal Name	Signal Name	J11 J21 Pin #	J11 J21 Pin #	Signal Name
TCK (3)	1	2	-12V	+12V	1	2	TRST# (3)
GND	3	4	INTA#	TMS (2)	3	4	TDO (1)
INTB#	5	6	INTC#	TDI (2)	5	6	GND
BM1 (1)	7	8	+5V	GND	7	8	N/C
INTD#	9	10	N/C	N/C	9	10	N/C
GND	11	12	+3.3V	BM2 (2)	11	12	+3.3V
CLKP1	13	14	GND	RST#	13	14	BM3 (3)
GND	15	16	GNT0#	+3.3V	15	16	BM4 (3)
REQ0#	17	18	+5V	PME#	17	18	GND
VIO (4)	19	20	AD31	AD30	19	20	AD29
AD28	21	22	AD27	GND	21	22	AD26
AD25	23	24	GND	AD24	23	24	+3.3V
GND	25	26	CBE3#	IDSEL	25	26	AD23
AD22	27	28	AD21	+3.3V	27	28	AD20
AD19	29	30	+5V	AD18	29	30	GND
VIO (4)	31	32	AD17	AD16	31	32	CBE2#
P1FRAME#	33	34	GND	GND	33	34	IDSL_B(1)
GND	35	36	IRDY#	TRDY#	35	36	+3.3V
DEVSL	37	38	+5V	GND	37	38	STOP#
GND	39	40	LOCK#	PERR#	39	40	GND
N/C	41	42	N/C	+3.3V	41	42	SERR#
PAR	43	44	GND	CBE1#	43	44	GND
VIO (4)	45	46	AD15	AD14	45	46	AD13
AD12	47	48	AD11	M66EN	47	48	AD10
AD9	49	50	+5V	AD8	49	50	+3.3V
GND	51	52	CBE0#	AD7	51	52	REQ_B#(1)
AD6	53	54	AD5	+3.3V	53	54	GNT_B# (1)
AD4	55	56	GND	N/C	55	56	GND
VIO (4)	57	58	AD3	N/C	57	58	EREADY(1)
AD2	59	60	AD1	GND	59	60	RSTOUT#(1)
AD0	61	62	+5V	ACK64#	61	62	+3.3V
GND	63	64	REQ64#	GND	63	64	Monarch#(1)

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PMC J13/J23 and J24 Connector Pin Assignments

Signal Name	J13 J23 Pin #	J13 J23 Pin #	Signal Name
N/C	1	2	GND
GND	3	4	CBE [7]
CBE [6]	5	6	CBE [6]
CBE [5]	7	8	GND
VIO (4)	9	10	PAR64
AD63	11	12	AD62
AD61	13	14	GND
GND	15	16	AD60
AD59	17	18	AD58
AD57	19	20	GND
VIO (4)	21	22	AD56
AD55	23	24	AD54
AD53	25	26	GND
GND	27	28	AD52
AD51	29	30	AD50
AD49	31	32	GND
GND	33	34	AD48
AD47	35	36	AD46
AD45	37	38	GND
VIO (4)	39	40	AD44
AD43	41	42	AD42
AD41	43	44	GND
GND	45	46	AD40
AD39	47	48	AD38
AD37	49	50	GND
GND	51	52	AD36
AD35	53	54	AD34
AD33	55	56	GND
VIO (4)	57	58	AD32
N/C	59	60	N/C
N/C	61	62	GND
GND	63	64	N/C

Signal Name	J24 Pin #	J24 Pin #	Signal Name
PMCIO1	1	2	PMCIO2
PMCIO3	3	4	PMCIO4
PMCIO5	5	6	PMCIO6
PMCIO7	7	8	PMCIO8
PMCIO9	9	10	PMCIO10
PMCIO11	11	12	PMCIO12
PMCIO13	13	14	PMCIO14
PMCIO15	15	16	PMCIO16
PMCIO17	17	18	PMCIO18
PMCIO19	19	20	PMCIO20
PMCIO21	21	22	PMCIO22
PMCIO23	23	24	PMCIO24
PMCIO25	25	26	PMCIO26
PMCIO27	27	28	PMCIO28
PMCIO29	29	30	PMCIO30
PMCIO31	31	32	PMCIO32
PMCIO33	33	34	PMCIO34
PMCIO35	35	36	PMCIO36
PMCIO37	37	38	PMCIO38
PMCIO39	39	40	PMCIO40
PMCIO41	41	42	PMCIO42
PMCIO43	43	44	PMCIO44
PMCIO45	45	46	PMCIO46
PMCIO47	47	48	PMCIO48
PMCIO49	49	50	PMCIO50
PMCIO51	51	52	PMCIO52
PMCIO53	53	54	PMCIO54
PMCIO55	55	56	PMCIO56
PMCIO57	57	58	PMCIO58
PMCIO59	59	60	PMCIO60
PMCIO61	61	62	PMCIO62
PMCIO63	63	64	PMCIO64

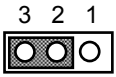
Note:

1. These signals are not connected on the board.
2. These signals are pulled high on the board.
3. These signals are pulled low on the board.
4. The VIO signals by default set to +5V via zero ohm resistors. Therefore, DO NOT apply any “3.3V only” PMC module to the PMC sockets.
5. J24 signals are connected to the CompactPCI J3 connector. To use these signals, the RTM need to be custom designed for special purposes or have a PIM connector available on board. Please contact ADLINK for details of custom RTM applications.

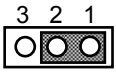
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2.3.16 IDE Setting Jumper on the RTM

A CompactFlash (CF) socket is available on the RTM as a Secondary IDE port. A 3-pin jumper (CN12) is used to set the CF card as either master or slave device of the IDE channel.



CF card is a Master IDE device

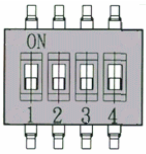


CF card is a Slave IDE device
(default factory setting)

2.3.17 GbE Connection Selection

The cPCI-6810AA supports dual Ethernet connection for PICMG2.16 compliant backplanes and the RTM. While using the PICMG 2.16 compliant backplane, it is recommended that none of the GbE ports on the rear panel be used. There are four mini switches that control the GbE routing located on the bottom side (solder side) of the RTM. Refer to the following information to choose either PICMG 2.16 or rear panel Ethernet connections.

S3, S4: LAN1 Connecting Selection

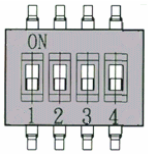


LAN 1 Connecting	Switch S3		Switch S4	
	Pin#	State	Pin#	State
Connect to PICMG 2.16 Backplane only	S3-1	OFF	S4-1	OFF
	S3-2	OFF	S4-2	OFF
	S3-3	OFF	S4-3	OFF
	S3-4	OFF	S4-4	OFF
Connect to Rear Panel (Default)	S3-1	ON	**S4-1**	**ON**
	S3-2	ON	**S4-2**	**ON**
	S3-3	ON	**S4-3**	**ON**
	S3-4	ON	**S4-4**	**ON**

Table 21: LAN1 Connection Selection

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S1, S2: LAN2 Connecting Selection



LAN 2 Connecting	Switch S1		Switch S2	
	Pin#	State	Pin#	State
Connect to PICMG 2.16 Backplane	S1-1	OFF	S2-1	OFF
	S1-2	OFF	S2-2	OFF
	S1-3	OFF	S2-3	OFF
	S1-4	OFF	S2-4	OFF
Connect to Rear Panel (Default)	S1-1	ON	**S2-1**	**ON**
	S1-2	ON	**S2-2**	**ON**
	S1-3	ON	**S2-3**	**ON**
	S1-4	ON	**S2-4**	**ON**

Table 22: LAN2 Connecting Selection

2.3.18 Setting Jumper on cPCI-6811AA

A 3-pin jumper (JP1) is used to set the SBC as either “in normal operation” or “forcing the SBC to SYSTEM mode”.

Note: When cPCI-6811AA is in the Packet Switching Backplane has no PCI bus, please set JP1 as “1-2”.



Normal operation (Default setting)

Pin #	Signal Name
1	GND
2	SYSEN#
3	NC



Force cPCI-6810/6820 to SYSTEM mode

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3

Getting Started

This chapter provides information on how to install necessary components on the cPCI-6811AA and cPCI-R6820 RTM, including:

- CPU and heat sink
- Memory module installation
- HDD installation on main board
- HDD installation on RTM
- CF installation on RTM
- PMC installation
- RTM installation
- Main board installation

3.1 CPU and Heatsink

The cPCI-6811AA SBC supports the Intel® Pentium® processor – Low Voltage, which is pre-mounted to the PCB (printed circuit board). The heatsink is also pre-mounted in the factory. There are no jumper settings necessary to set the CPU operating frequency or CPU type.

DO NOT try to replace the CPU in the field or remove the heatsink. It will cause board defects and void the warranty.

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3.2 Memory Module Installation

The cPCI-6811AA SBC supports up to two sockets of 144-pin PC-133 registered ECC SO-DIMM's. The maximum memory capacity is 1GB. If memory modules are pre-installed when you receive the your package, this section can be skipped.

The chipset supports 64Mb, 128Mb, 256Mb, and 512Mb memory technologies. The supported DRAM types are listed in the following table.

DRAM Depth	DRAM Type (Row/Column)
16M 2-bank SDRAM	11/9
	11/10
64M 2-bank SDRAM	13/10
64M 4-bank SDRAM	12/8
	12/9
	12/10
	13/10
	12/9
128M 4-bank SDRAM	12/10
	13/10
256M 4-bank SDRAM	13/8
	13/9
	13/10
	13/11

Table 23: Supported SDRAM Chip

While installing the SO-DIMM, ensure that the SO-DIMM modules are firmly seated in it sockets and do not hinder with any components.

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3.3 HDD Installation on Main Board

A slim-type 2.5-inch HDD can be mounted to the cPCI-6811AA main board. If a HDD is pre-installed when you receive the cPCI-R6820 product package, this section maybe skipped.

Step 1: Remove the PMC Key-bolt of the PMC slot #1.

Step 2: Screw the bolts on to the HDD and attach a 44-pin IDE cable.

Step 3: Install the assembly on to the board; tighten the 4 screws from the bottom side of the main board to secure the HDD in to place.

Step 4: Attach the other end of the 44-pin IDE cable to CN4 on board.

3.4 HDD Installation on RTM

A 2.5-inch HDD or Flash Disk can be installed on the RTM directly. If a HDD is pre-installed when you receive the cPCI-R6820, please skip this section.

Step 1: Attach the IDE cable to the HDD or Flash Disk

Step 2: Put the HDD on component side of the RTM, align the HDD mounting holes with the holes on the PCB.

Step 3: tighten the 4 screws from the bottom side of the RTM to secure the HDD in to place

Step 4: Connect the IDE cable to the 44-pin connector CN4.

3.5 CF Installation on RTM

The CompactFlash Card (or CF storage card) is widely applied in digital consumer devices such as PDAs, digital cameras and MP3 players. Because of the CF anti-shock, anti-vibration, better environment tolerance, low power consumption, small form factor, and high reliability, it has been widely accepted in mission critical embedded applications.

For the cPCI-6811AA, the CF card socket is available on the rear transition module (cPCI-R6820).

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3.6 PCI Mezzanine Card (PMC) Installation

The PMC slots are designed as 5V and/or as a universal PCI interfaces. The PMC sites are keyed to prevent users from installing a 3.3V only PMC module.

The rear I/O signals on the J14 of the upper PMC slot are routed to J3 of the 6811AA main-board. Refer to section 2.3.15 for detailed PMC I/O signal routing. If a HDD is mounted to the main board, the HDD will occupy the upper PMC slot #1.

For install the PMC modules:

Step 1: Prepare an ESD protected area including an anti-ESD table and ESD strap. Attach the ESD strap to your wrist and connect the end of the ESD strap to ground of the anti-ESD table.

Step 2: Remove the PMC panel from the front panel.

Step 3: Install the PMC module on to the PMC sockets.

Step 4: Screw the PMC mounting bolts to the main board from the bottom side up to fix the PMC module in place.

3.7 RTM Installation

This section describes important information regarding the use of the rear I/O connections. Refer to section 2.4 for peripheral connectivity of all I/O ports on the RTM. When installing the cPCI-6811AA and its RTM, make sure the RTM is the correct model that matches its front board.

Use the correct RTM to enable functions (I/O interfaces) on rear side. The RTM or system board can be damaged if the incorrect RTM is used.

Some I/O ports are supported on both the front board and the RTM, including Keyboard, Mouse, VGA and USB. These I/O ports can be connected either via the front or rear modules but DO NOT access these ports on both front and rear simultaneously.

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3.8 Main Board Installation

Use the following procedure to install the cPCI-6811AA main board to its ***CompatPCI*** chassis.

Step 1: Refer to the relevant chassis user manual for pre-preparation of the chassis before installing the main board. Users need to assign a slot to the board. Be sure to select the correct slot (system or peripheral) depending the operation purpose of the board. The system power may now be powered on.

Step 2: Remove the blank face panel from the slot.

Step 3: Align the top and bottom edges of the board with the card guides on the chassis then slide the board into the chassis until resistance is felt. If the system power is on, the blue LED (hot-swap status) should light.

Step 4: Move the upper and lower ejectors in an inward direction simultaneously. Note a small amount of resistive force will be felt while inserting the board. If this resistive force is higher than in normal conditions, check to ensure that there are no pins bend on the backplane and that the board's connector pins are aligned properly with the connectors on the backplane.

Step 5: Verify that the board is seated properly. With the board in place and the blue LED on, wait for the blue LED to go out before proceeding to the next step.

Step 6: Secure the two screws hidden behind the upper and lower ejector; connect the proper cables to the board.

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4

Device Driver Installation

To install the drivers for the cPCI-8611, refer to the installation information in this chapter. Basic information is presented in this section, however, for more detailed installation information for non-Windows Operating Systems, refer to the extensive explanation inside the ADLINK CD. The drivers are located in the following directories of the CD-ROM:

LAN driver	\CHIPDRV\LAN\82546EB\win2kxp

As the Bus-mastering IDE drivers are automatically installed by most Windows based operating systems, it will not be described.

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4.1 LAN Drivers Installation

This chapter describes the LAN driver installation for the onboard Ethernet controller ***Intel 82546EB***. All associated drivers are located under the following ADLINK CD directory: ***X:\CHIPDRV\LAN\82546EB***, where X: is the location of the CD-ROM drive.

4.1.1 Software and Drivers Support

The 82546EB driver supports the following OS or platforms:

- Windows 2000, Windows XP

All the above drivers are included in the ADLINK CD. In the following section, we will describe the driver installation for Windows 2000, and Windows XP.

4.1.2 Driver Installation on Windows 2000

Windows 2000 will attempt to install a standard LAN driver automatically. To guarantee compatibility, manually install the most updated LAN driver, which is stored in the ADLINK CD. After installing Windows 2000, update to the most updated driver using the following procedures.

1. Run " pro2kxpm.exe" in x:\chipdrv\LAN\82546EB\win2kxp to extract the files needed for the installation. Files will be extracted to c:\IntelPRO
2. Click "Install Now" to install driver.
3. Click "Finish".

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A

IPMI Functions List

The following table lists the IPMI V1.0 functions that are supported by the cPCI-6811AA.

IPMI V1.0 Function List	CPCI-6811AA
IPM Device "Global" Commands	
Get Device ID	√
Cold Reset	√
Warm Reset	√
Get Self Test Results	√
Set ACPI Power State	√
Get ACPI Power State	√
Get Device GUID	√
BMC Watchdog Timer Commands	
Reset Watchdog Timer	√
Set Watchdog Timer	√
Get Watchdog Timer	√
BMC Device and Messaging Commands	
Set BMC Global Enables	√
Get BMC Global Enables	√
Clear Message Flags	√
Get Message Flags	√
Enable Message Channel Receive	√
Get Message	√
Send Message	√
Read Event Message Buffer	√
Get BT Interface Capabilities	√
Get System GUID	√
Chassis Device Commands	
Get Chassis Status	√
Chassis Control	√
Get POH Counter	√

Event Commands	
Set Event Receiver	√
Get Event Receiver	√

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Platform Event (a.k.a. “Event Message”)	√
PEF and Alerting Commands	
Sensor Device Commands	
Get Device SDR Info	√
Get Device SDR	√
Reserve Device SDR Repository	√
Get Sensor Reading Factors	√
Set Sensor Hysteresis	(2)
Get Sensor Hysteresis	√
Set Sensor Threshold	(2)
Get Sensor Threshold	√
Set Sensor Event Enable	(2)
Get Sensor Event Enable	√
Re-arm Sensor Events	(2)
Get Sensor Reading	√
Set Sensor Type	(2)
Get Sensor Type	√
FRU Device Commands	
Get FRU Inventory Area Info	√(1)
Read FRU Data	√(1)
Write FRU Data	√(1)
SDR Device Commands	
Get SDR Repository Info	√
Get SDR Repository Allocation Info	√
Reserve SDR Repository	√
Get SDR	√
Add SDR	√
Partial Add SDR	√
Delete SDR	√
Clear SDR Repository	√
Get SDR Repository Time	√
Set SDR Repository Time	√
Enter SDR Repository Update Mode	√
Exit SDR Repository Update Mode	√
Run Initialization Agent	√

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SEL Device Commands	
Get SEL Info	√(1)
Get SEL Allocation Info	√(1)
Reserve SEL	√(1)
Get SEL Entry	√(1)
Add SEL Entry	√(1)
Partial Add SEL Entry	√(1)
Delete SEL Entry	(3)
Clear SEL	√(1)
Get SEL Time	√(1)
Set SEL Time	√(1)

(1)Supported on PCB rev.A3 or higher.

(2)The SDR information are read only.

(3) The SEL storage is not supported random access

A.1 IPMI Address Map

The IPMI address of the SBC is defined by GA pins which is relative with the physical slot the SBC is installed. The following table shows the relationship between the IPMI address and the Slot number SBC installed.

Address (Hex)	CompactPCI Slot
B0	Peripheral Slot1
B2	Peripheral Slot2
B4	Peripheral Slot3
B6	Peripheral Slot4
B8	Peripheral Slot5
BA	Peripheral Slot6
BC	Peripheral Slot7

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B

WatchDog Timer Programming Guide

The Watchdog Timer (WDT) can monitor the system's status. Once a value is given to the WDT, the timer will begin to count down. If the system idles or hangs, the system will reboot itself when the timer times out.

The Watch Dog timer includes an 8-bit timer clocked by a 1-minute internal clock that is derived from the battery-backed 32.768KHz crystal clock generator. The timer is loaded with the WATCHDOG Time-Out data value written in the WDTO register and counts down to zero. This 8-bit data enables time-out values between 1 to 255 minutes to be programmed (00h is an invalid data value)

Following events can trigger the WATCHDOG by reloading the timer:

- Keyboard interrupt
- Mouse interrupt
- Serial Port 1 interrupt.
- Serial Port 2 interrupt.
- Software writing to control register

All control registers are accessed through the following I/O ports.

I/O mapped Port	
Index port	Data Port
2EH	2FH

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B.1 WDT Setup Procedures

Followings are the Watch Dog Timer setup procedures:

1. Set pin 55 of PC87417 as Watch Dog Timer output pin

   →Set Bit 7 of SIOCF2 Register (Index: 22H) to 1, for example:

   - o 2E 22
   - o 2F 80

2. Set Logic Device to System Wake-Up Control (SWC)

   →Set Logic Device Number Register (Index: 07H) to 04H, for example:

   - o 2E 07
   - o 2F 04

3. Enable Logic Device Control

   →Set Logic Device Control Register (Index: 30H) to 01H, for example:

   - o 2E 30
   - o 2F 01

4. Get I/O Base Address (MSB) of SWC

   →Get SWC base address MSB from 60H, for example:

   - o 2E 60
   - i 2F
   - 08 →BIOS default value

5. Get I/O Base Address (LSB) of SWC

   →Get SWC base address MSB from 61H, for example:

   - o 2E 61
   - i 2F
   - 40 →BIOS default value

(The I/O Base Address of SWC BIOS set is 840H)

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6. Select Bank 3 for Watch Dog Timer from SWC base address.

   →Set Bit 1-0 of BANKSEL Register (I/O Base: 840H, Offset: 0FH) to 11, for example:

   - o 84F 03

7. Set the count down value for Watch Dog timer.

   →Set count down value to WDTO Register (I/O Base: 840H, Offset: 11H)

   00000000: Reserved

   00000001: 1 minute

   00000010: 2 minutes

   :

   :

   11111111: 255 minutes

   For example:

   - o 851 03→3 minutes

8. Enable trigger event to re-start new counter value

   →Set WDCFG Register (I/O Base: 840H, Offset: 12H) to 82H, for example:

   - o 852 82

9. Enable Watch Dog Timer function

   →Set Bit 0 of WDCTL Register (I/O Base: 840H, Offset: 10H) to 1, for example:

   - o 850 01

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C

SMBus Address Map

The SMBus address Map on cPCI-6820 products are as following.

Address (Hex)	Function	Device
0x A0	SO-DIMM ID(1)	SO-DIMM
0x 5C	Hardware Monitor	ADM1026
0x AC	SEL data storage (IPMI)	24C64
0x AE	FRU data storage (IPMI)	24C64
0x AA	BIOS CMOS storage	24C02

Note: ID of SO-DIMM 1-4 are selected by two GPIO pins from CSB5 SO-DIMM selection table:

GPIO13	GPIO12	DIMM
0	0	1
0	1	2
1	0	3
1	1	4

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Warranty Policy

Thank you for choosing ADLINK. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. Before using ADLINK's products please read the user manual and follow the instructions exactly. When sending in damaged products for repair, please attach an RMA application form which can be downloaded from: http://rma.adlinktech.com/policy/.
2. All ADLINK products come with a limited two-year warranty, one year for products bought in China.
    - The warranty period starts on the day the product is shipped from ADLINK's factory.
    - Peripherals and third-party products not manufactured by ADLINK will be covered by the original manufacturers' warranty.
    - For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ADLINK is not responsible for any loss of data.
    - Please ensure the use of properly licensed software with our systems. ADLINK does not condone the use of pirated software and will not service systems using such software. ADLINK will not be held legally responsible for products shipped with unlicensed software installed by the user.
    - For general repairs, please do not include peripheral accessories. If peripherals need to be included, be certain to specify which items you sent on the RMA Request & Confirmation Form. ADLINK is not responsible for items not listed on the RMA Request & Confirmation Form.
3. Our repair service is not covered by ADLINK's guarantee in the following situations:
    - Damage caused by not following instructions in the User's Manual.
    - Damage caused by carelessness on the user's part during product transportation.
    - Damage caused by fire, earthquakes, floods, lightening, pollution, other acts of God, and/or incorrect usage of voltage transformers.

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- Damage caused by inappropriate storage environments such as with high temperatures, high humidity, or volatile chemicals.
- Damage caused by leakage of battery fluid during or after change of batteries by customer/user.
- Damage from improper repair by unauthorized ADLINK technicians.
- Products with altered and/or damaged serial numbers are not entitled to our service.
- This warranty is not transferable or extendible.
- Other categories not protected under our warranty.

4. Customers are responsible for all fees necessary to transport damaged products to ADLINK.

For further questions, please e-mail our FAE staff: service@adlinktech.com

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