cPCI-6810/6820 Series

6U CompactPCI

Dual/Single Pentium TM III SBC
and Rear I/O Transition Modules

User's Manual

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1 Introduction

The ADLINK's cPCI-6810/6820 series Single Board Computer (SBC) and its corresponding rear I/O transition module is a powerful and flexible CompactPCI universal system/peripheral slot processor board. It is based on the Intel® mobile Pentium-III/ Tualatin CPU. This board is specially designed to add system functional density to the 6U CompactPCI platform for communication, high-density servers, and Telecom applications. It is also suitable for high-density, high-reliability, and high-availability embedded applications where having a diverse range of features and performance are paramount.

The cPCI-6820 series product complies with PICMG 2.0 Rev. 3.0 CompactPCI specifications for 6U, single-slot (4 TE/HP) form factor boards. The cPCI-6820 board features dual Intel® Pentium® III Processor - Low Power (933 MHz) with 512KB L2 cache, while the cPCI-6810 is based on the same architecture as the cPCI-6820 but features only a single Intel® Pentium® III Processor - Low Power (933 MHz).

The cPCI-6820 series SBC uses the ServerWorks chipset, which supports a 133MHz processor front side bus (FSB) and up to four 144-pin SO-DIMM sockets of PC-133 Registered SDRAM.

The cPCI-6810/6820 also features an Intel® 82546EB dual port gigabit Ethernet (GbE) controller on the 66MHz 64bit PCI bus. The dual GbE connections can be routed to the cPCI-R6820 RTM or to the PICMG 2.16 compliant backplane.

In addition to its high computing performance and communication capability, the cPCI-6820 also supports Intelligent Platform Management IPMI v1.0 based on PICMG 2.9 specifications for applications that require high reliability and serviceability.

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Topics covered in this chapter include:

- Model Variations
- Checklist
- Features
- Specifications
- Block diagram

1.1 Checklist

The cPCI-6820 series products support both front and rear panel I/O. The front board (the SBC) and the cPCI-R6820 RTM are sold separately. The CPU configurations can be single or dual CPU.

cPCI-6810 or cPCI-6820 Front Board

The cPCI-6810/6820 CPU module may be equipped with different capacities of RAM, HDD, and PCM depending on requirements. Please check the configurations with your dealer and check that the package is complete and contain the items below. If you discover any damaged or missing items, please contact your dealer.

- This User's Manual
- The cPCI-6810 or cPCI-6820 SBC
- ADLINK CD

Note:	The delivered package of the cPCI-6810/6820 OEM version (non-standard configuration, functionality, customized logo, modified faceplate, or package) may vary depending on customized requests.

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cPCI-R6820 RTM

The cPCI-R6820 is designed to provide additional I/O functionality through rear I/O connectivity for the cPCI-6820 or cPCI-6810. The cPCI-R6810 can be shipped with or without a storage device (IDE HDD or CF card) depending on the options ordered. Please check possible configurations with your dealer. As shipped, the product package should contain the following items:

- cPCI-R6820 RTM
- Y-shape Keyboard/Mouse Combo cable

1.2 Features

cPCI-6810/6820 Features

- PICMG 2.16 CompactPCI Packet Switching Backplane (cPSB) Compliant
- PICMG 2.9 System Management Bus Compliant
- Standard 6U form factor, 1-slot (4HP) wide
- Design for mobile Pentium-III/Tualatin CPU running at FSB 133MHz, single processor (cPCI-6810) or dual processors (cPCI-6820)
- Up to four 144-pin SO-DIMM sockets supporting up to 2GB PC-133 SDRAM
- 64-bit/66MHz CompactPCI
- Universal operation for both system and peripheral slots
- Full hot-swap support
- Onboard up to two 64-bit PMC module slot

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cPCI-R6820 Features

- PICMG 2.0 CompactPCI Specification R3.0 Compliant
- 6U form factor, 1-slot (4TE/HP) in width, 80mm in board depth
- Designed for cPCI-6810 and 6820 series front board
- Supports dual RJ-45 GbE connectors, onboard dual EIDE interfaces with CF socket and housing for onboard 2.5” ATA HDD
- Supports two USB ports (type A connector), COM port over RJ-45 connector, one VGA port, keyboard and mouse combo connector, and an optional COM2 connector.

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1.3 Functional Block

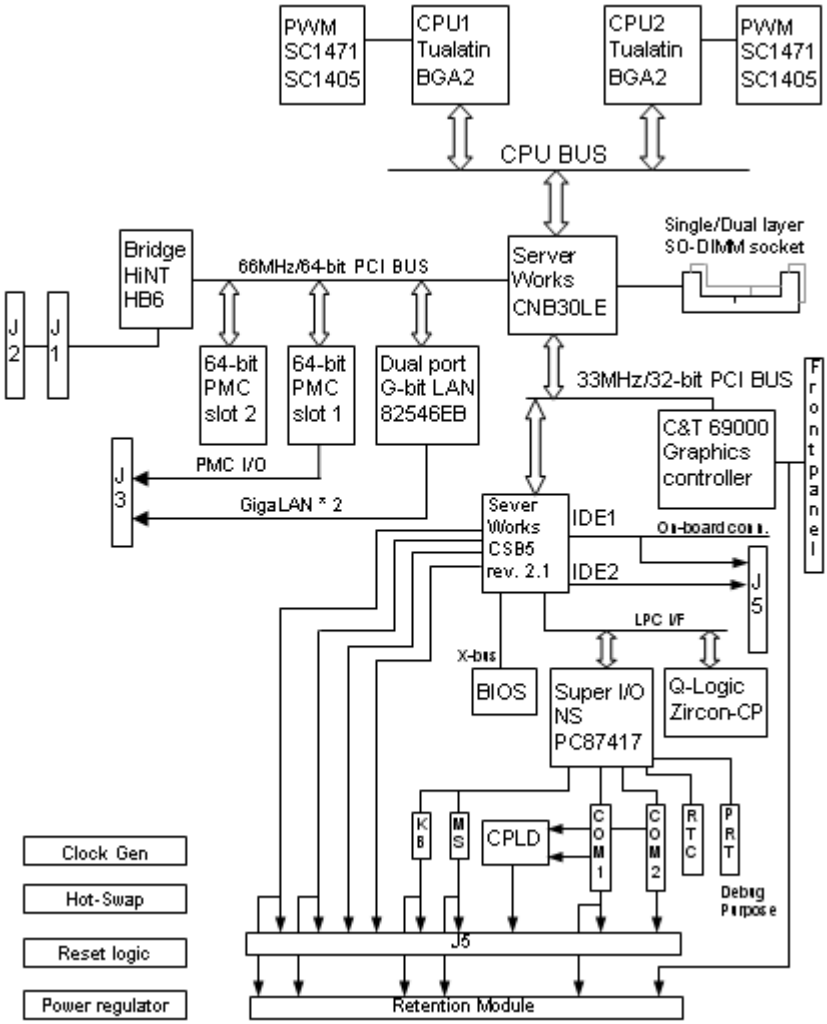


Figure 1-1: cPCI-6810/6820 Block Diagram

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CompactPCI Bus Interface

The cPCI-6810/6820 operates in a 6U CompactPCI system. The CompactPCI standard is electrically identical to the PCI local bus standard but has been enhanced to work in harsh environments and support more peripheral slots. Additionally, when used in a hot-swap compliant backplane and in accordance with the CompactPCI Hot Swap Specification, PICMG 2.1, Version 1.0, the cPCI-6810/6820 supports hosting hot-swappable peripherals in a powered system. The cPCI-6810/6820 can also function in a standard (non-hot-swap) CompactPCI system without live insertion and extraction capability.

PCI-to-PCI Bridge

The HiNT HB6 is a tri-mode universal PCI-to-PCI Bridge and is used to implement the system/peripheral slot on the cPCI-6810/6820. The three-mode bridge is capable of operating in Transparent, Non-Transparent, or Universal mode. The HB6 Non-Transparent mode permits independent memory mapping of both primary and secondary buses with powerful configuration options to support intelligent subsystems. The Universal mode permits jumper-less configuration between application to CompactPCI interface at Peripheral Slot and System Slot. With the Universal option, the HB6 Bridge can be configured as a transparent bridge in a System Slot supporting a host, or as a Non-Transparent bridge in a Peripheral Slot as an intelligent subsystem. These options allow the cPCI-6810/6820 board to be inserted into both the Peripheral Slot and the System Slot.

In addition to the 66MHz/64bit capability, the host bus and subsystem bus can operate at different speeds. Together with 64-bit to 32-bit access conversion, system architects can utilize the bridge and connect slower or higher speed controllers on primary or secondary bus, thereby supporting independent speed and data bus frequency on either side of the PCI bus.

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Key features

- Large 1kB total buffering supporting concurrent Primary and Secondary operation as well as traffic isolation.
- Multiple output clock pins and nine pairs of REQ/GNT signals support up to nine bus masters directly on secondary bus without external clock buffer and bus arbiter.
- 5V tolerant I/O buffer, EEPROM support for extra register control, Vital Product Data (VPD), 16 general purpose I/O interface, and proven PME
- D3 wakeup power management – one of the many functions available in a single HB6 bridge.

BIOS

The cPCI-6810/6820 adopts the Award BIOS with a 4Mb flash ROM implemented to load the BIOS. A boot block device is used to allow recovery of the BIOS in the event of a catastrophic failure (power failure during BIOS update). The BIOS supports the following features:

- CPU/memory speed auto-detection
- DMI BIOS Support: Desktop Management Interface (DMI) allows users to download system hardware-level information such as CPU type, CPU internal/external frequencies, and memory size.
- Green Function: APM/ACPI compliant Power management via BIOS, activated through mouse/keyboard movement or other wake-up events.
- PCI Plug and Play support.
- Intel pre-boot execution environment (PXE) support
- PICMG2.1 CompactPCI hot-swap specification Rev. 1.0 support on CompactPCI I/O bus.

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Processor

The cPCI-6810/6820 motherboard is based on the RCC/ ServerWorks Champion LE chipset and supports a single or dual Intel Mobile Pentium III processor – M. The supported CPU package is a micro-FCBGA.

The Intel® Pentium® III processor - Low Power is a 0.18-micron product, which is a highly integrated assembly with all its immediate system-level support. This mobile version of the Pentium III processor runs at a lower voltage than the desktop version.

The 256 KB on-die transfer L2 cache is integrated with the CPU, eliminating the need for separate components and improving performance. The Intel® Pentium® III processor - Low Power also operates on a 100/133 MHz Front Side Bus for faster access to memory and data. The FSB speed depends on the CPU type with its core speed is automatically detected by the BIOS.

Supported Memory

The cPCI-6810/6820 supports PC100/PC133 registered SO-DIMMs only. The SDRAM speed, type, and size can be determined by the BIOS reading the DIMM presence detect bits on the SMBus. The DRAM timing register, which provides the DRAM speed control for the entire array, must be programmed to use the parameters of the slowest installed SDRAM. The DRAM interface supports 64Mbit, 128Mbit, and 256Mbit technology allowing up to 512MB per double-sided SO-DIMM. The cPCI-6810/6820 can support up to 2GB of SDRAM memory with four 144-pin SO-DIMMs. Refer to the table below for memory size configurations according to model type.

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	cPCI-6810		cPCI-6820		
	AA	AB	AC	AD	AE
Memory sockets	Single x2	Single x2	Single + Dual	Single + Dual	Dual x2
Max. SO-DIMM#	2	2	3	3	4
Max. Memory	1GB	1GB	1.5GB	1.5GB	2GB

Table 1-1: cPCI-6810/6820 Memory Configurations

Interrupts

Two enhanced interrupt controllers provide the cPCI-6810/6820 with a total of 15 interrupt inputs. Interrupt controller features include support for:

- Level-triggered and edge-triggered inputs
- Individual input masking
- Fixed and rotating priorities

Interrupt sources include:

- Counter/Timers
- Serial I/O
- Keyboard
- Printer Port
- Floppy disk
- IDE interface
- Real-Time Clock
- Onboard PCI devices

Enhanced capabilities include the ability to configure each interrupt level for active high going edge or active low-level inputs. The cPCI-6810/6820's interrupt controllers reside in the CNB30LE.

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DMA

Two enhanced DMA controllers are provided on the cPCI-6810/6810 for use by onboard peripherals. The cPCI-6810/6820's DMA controllers reside in the CNB30LE device.

Real-Time Clock

The super I/O PC87417 provides DS1287 compatible Real-Time Clock. It provides a Y2K compliant century calendar as well as a time of day function. In addition, 242 bytes of battery-backed-up CMOS RAM accessed through 70 - 71h and 72 - 73h are available for use by the BIOS. A separate 3V coin cell battery (PANSONIC CR2032 or compatible) provides battery-back-up.

Baseboard Management

The Zircon CP baseboard management controller is used to manage all aspects of the system board. The features are summarized as follows.

- ARM7/TDMI controller with internal 14KB SRAM
- IPMB interface
- External 16-bit flash ROM interface with 2Mb - 8Mb ROM size
- Six channels A-to-D converter for voltage monitoring, 10-bit resolution
- Heartbeat timer
- Supports CPU internal instruction error input (IERR#)
- Supports CPU floating point error input (FERR#)

QLogic provides a firmware suite supporting the Intelligent Platform Management Interface (IPMI) specification, including the Intelligent Platform Management Bus (IPMB). See Appendix A for an in-depth programmers' guide.

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Power Ramp Circuitry

The cPCI-6810/6820 features a power controller with power ramp circuitry to allow the board's voltages to be ramped in a controlled fashion. The power ramp circuitry eliminates any large voltage or current spikes caused by hot-swap boards. This controlled ramping is a requirement of the CompactPCI hot-swap specification, PICMG 2.1, Version 1.0. The cPCI-6810/6810's power controller unconditionally resets the board when it detects that the 3.3V, 5V, and 12V supplies are below an acceptable operating limit. These limits are defined as 4.75V (5V supply), 3.0V (3.3V supply), and 10.0V (+12V supply).

PCI Mezzanine Card (PMC) Interface

The cPCI-6810/6820 supports up to two PMC expansion slots (only one slot on cPCI-6820). The PMC supports 3.3V PCI environment and operates at up to 64bit/66MHz. The PMC expansion card is on the secondary PCI bus of CNB30LE, i.e., it is on PCI bus 1. Table 1-2 illustrates PMC availability depending on the cPCI-6810/6820 model.

	cPCI-6810		cPCI-6820		
	AA	AB	AC	AD	AE
PMC 1 (with rear I/O)	Yes	No	Yes	No	No
PMC 2	Yes	Yes	No	No	No
2.5” HDD	No	Yes	No	Yes	No

Table 1-2: PMC Options

Watchdog Timer

The cPCI-6810/6820 implements a watchdog timer embedded in the NS PC87417. The watchdog timer is an 8-bit down counter with 1-minute resolution. Programmable I/O ports 10h - 12h of bank 3 are used to configure the watchdog timer. The 8-bit timer is programmable from 1 - 255 minutes. Once a value is set to the WDT, the timer begins to count down. Any movement of keyboard, mouse or software will reset the value and reload the timer again.

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The watchdog output is connected to “reset”. When the system hangs without software re-trigger, the system will be reset. The watchdog register is cleared on power-up, enabling system software to take appropriate action.

Ethernet Interfaces

The onboard Intel® 82546EB dual-port gigabit Ethernet controller provides two Ethernet interfaces on cPCI-6810/6820. The 82546EB is implemented on 64-bit/66-MHz PCI bus. The 82546EB supports IEEE 802.3x compliant flow control and IEEE 802.3ab compliant 10/100/1000 Mbps auto-negotiation. The Ethernet interfaces are connected to J3, which is compliant with the PICMG 2.16 specification.

Each Ethernet interface is assigned with a unique Ethernet Address of the form 003064XXXXXh where XXXXX is the unique number assigned to a particular interface and 003064 is the ADLINK Company ID. Each of the board’s Ethernet Address is displayed on a label attached to the board. LED drive signals for Ethernet link status, activity, and speed are routed to the front panel.

Video (Only available on cPCI-6820)

The display interface features the 69000 PCI graphics accelerator, an Asiliant Technologies (formerly Chips and Technologies) product. The 2MB SDRAM is integrated in the 69000 as a display memory and internally operates at 83MHz. The 69000 integrates 8-bit 135MHz RAMDAC and can support up to 640x480x24bpp, 800x600x24bpp, 1024x768x16bpp, and 1280x1024x8bpp display modes. The CRT interconnections are available on both the front panel of cPCI-6820 and rear I/O board.

IDE Interface

The fast IDE interface on cPCI-6810/6820 supports up to four IDE devices including hard disk drives and CD ROMS. Each IDE device can have independent timing. The IDE interface supports PIO IDE transfers of up to 14MB/sec. and the Bus Master IDE up to 100MB/sec. The CSB5’s IDE system contains two independent

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IDE signal channels. They can be electrically isolated and configured to the standard primary and secondary channels.

Universal Serial Bus (USB)

The root hub integrated in the CSB5 supports four USB serial ports. Two ports are available on the front panel, with the other two ports routed to the rear I/O board through J5. Additional ports can be added through the use of an external USB hub. USB's allow the flexibility for the addition of peripherals such as mouse, keyboard, speakers, etc. Transfer speeds of up to 24Mb/s are supported. The cPCI-6810/6820 provides the standard 0.5A at 5V to the peripherals. The power to each port is protected by a single polyswitch (this current rating allows for inrush currents).

Serial I/O

Two serial ports are supported on the cPCI-6810/6820. The EIA232 drivers and receivers reside onboard. COM1 is implemented as an RJ45 connector on the front panel. Both COM1 and COM2 are available on rear I/O board. The BIOS will initialize the serial ports as COM1 and COM2 with default ISA I/O base addresses 3F8h and 2F8h respectively. This default configuration also assigns COM1 to IRQ4 and COM2 to IRQ3. The supported baud rates are 1200, 2400, 4800, 9600, 19200, 38400, 57600, and 115200 bps.

Keyboard/Mouse Controller

Two 6-pin circular DIN connectors are located on the front panel of single-processor version of cPCI-6810/6820, for example cPCI-6810, for keyboard and mouse connections. The power provided to the keyboard and mouse is protected by a polyswitch at 1.1A. The keyboard and mouse interface are also available on the rear I/O board.

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1.4 Specifications

Specifications of cPCI-6820 front board

CompactPCI Compliancy

- PICMG 2.0 CompactPCI core specification R3.0
- PICMG 2.1 CompactPCI hot-swap R1.0
- PICMG 2.16 CompactPCI packet switching backplane (cPSB) R1.0
- PICMG 2.9 System Management Bus R1.0
- PCI Rev 2.1 compliant

Form Factor

- Standard 6U CompactPCI (board size: 233.35 x160mm2)
- Single-slot (4 TE/HP, 20.32mm) width, incl. housing for 2.5” HDD

CPU / Cache

- Intel® Pentium® III Processor - Low Power up to 1033 MHz with 512K on-die L2 cache

Chipset

- ServerWorks LE-III

Host Memory

- Up to four 144-pin SO-DIMM sockets
- Capacity of up to two Gigabytes of PC-133 Registered ECC SDRAM (note: It is dependent on the model variation, please refer to table 1).

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BIOS: ADLINK Enhanced Award / Phoenix BIOS

- Support Intel® Pre-boot Execution Environment (PXE) version 2.x, WFM 2.0. Include BIOS setup options and boot from LAN
- Support DMI / SMBIOS 2.3
- CPU, memory operating frequency auto-detection
- Bootable from USB storage devices including USB-Floppy, USB-ZIP USB-CD-ROM and USB-HDD.
- Optional OEM BIOS features
  - Customized OEM splash image / power on screen
  - Serial remote-console redirected to serial COM1 port

Note:	Due to BIOS segment limitations; enabling the remote console function may occupy the same memory space as other ROM mapping add-on or boot-up devices such like Pre-boot Agent of Ethernet Boot ROM, SCSI Boot ROM or add-on EIDE Boot ROM. It is recommended that only one ROM-mapping add-on or boot-up device be enable when enabling the remote console function.

Gigabit Ethernet

- Two Gigabit Ethernet (GbE) ports with Intel® 82546EB Ethernet controller, based on local 66MHz/64-bit PCI bus.
- Support 1000Base-T, 100Base-TX, and 10Base-T (IEEE 802.3, 802.3u, and 802.3ab).
- IEEE802.3x compliant flow control, support auto-negotiation and link setup.
- GbE connection on PICMG 2.16 PSB or on RTM rear access.
- Speed and connection status LED on the front panel.

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Graphic Display (available on cPCI-6820)

- C&T 69000 VGA controller with integrated 2MB of memory.
- VGA DB-15 connectors on front panel.

USB Interface

- Supports up to four USB version 1.1 ports with integrated USB host controller. Two USB ports (USB-0 and USB-1) are BIOS configurable for front or rear access. Two USB ports (USB-2 and USB-3) are rear access only.
- USB ports provide 0.5A @ 5V power for peripheral devices with over current protection.

IDE Ports

- Bus master IDE controller supports two ultra ATA-100 interfaces.
- Primary IDE is onboard with 44-pin IDE connector.
- Both Primary and Secondary IDE ports are on J5 for RTM extension.

Super I/O, WDT and Hardware Monitoring

- Chipset: NS PC87417 low pin-count (LPC) Server I/O controller.
- Two 16C550 UART compatible RS-232 COM ports. COM1 on the front with RJ-45 type connector. COM2 is on the J3 and can be accessed on the RTM.
- PS2 keyboard and mouse connector:
  - cPCI-6820: With 6-pin circular DIN connectors on both the front board and RTM.
  - cPCI-6810: Connectors on RTM only.
- Built-in W82782D monitoring CPU temperatures, FAN speed, system temperature, V core, and DC voltages.
- Watchdog timer: Programmable I/O port 10h-12h of bank 3 to configure watchdog timer, programmable 8-bit timer 1 - 255 minutes.
- Real-Time Clock and Nonvolatile Memory: DS1287 compatible Real-Time Clock. 242 bytes CMOS RAM

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backup by a separate 3V coin cell battery (PANSONIC CR2032 or compatible).

IPMI Interface

- Supports PICMG 2.9 secondary system managing bus. Implements IPMI functions as defined in the IPMI specification v1.0.
- Qlogic Zircon CP Baseboard Management Controller (BMC) with 14KB internal SRAM, 1MB external flash ROM.

Front Panel LED Indicators and Reset

- Four LEDs on the front panel including storage access LED (RED), Power LED (GREEN), hot-swap status (Blue), and watchdog timer LED (Yellow).
- Four LEDs to indicate GbE ports status including speed (yellow) and link/activity (green).
- Flush tact switch for system reset.

PCI Bus and CompactPCI connectors

- HiNT HB6 Universal PCI to PCI bridge.
- 64-bit/66MHz, supporting four bus-mastering devices.
- 32-bit/33MHz, supporting seven bus-mastering devices.

Specifications of cPCI-R6820 RTM

Form Factor

- Standard 6U CompactPCI rear I/O (board size: 233.35x80mm^2).
- 1-slot (4TE/HP, 20.32mm) wide, include space of 2.5” HDD.

Connection Interface

- RTM signals are from CompactPCI rJ3 and rJ5 connectors, without rJ1, rJ2, and rJ4. Use AB type connector on rJ5.

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Faceplate I/O Connectors

- Two USB ports: USB2, USB3 (type A connector).
- VGA port on DB-15 connector.
- Keyboard/mouse combo PS2 mini-DIN 6-pin connector.
- Two GbE ports on RJ-45 connectors.
- Serial COM2 ports on RJ-45 connectors.

IDE Connectors

- Primary IDE supported on one 40-pin connector and one 44-pin connector for 2.5” HDD.
- Secondary IDE supported on one 40-pin IDE connector and one CompactFlash type-II socket.

Common Spec. for cPCI-6810/6820 and RTM

Flash Storage Support Options

- DiskOnModule via the 40-pin IDE on RTM, 16 - 256MB.
- CompactFlash card via the CF socket on RTM, 8 - 12MB.
- 2.5” Flash disk drive on front board or RTM, 32MB - 2GB.

OS Compatibility

- Microsoft® Windows NT, Windows 2000, Windows XP, Red Hat Linux 7.2.
- Other OS support upon request.

Environment

- Operating temperature: 0 to 50°C (Note 1)
- Storage temperature: -20 to 80°C
- Humidity: 5% to 95% non-condensed
- Shock: 15G peak-to-peak, 11ms duration, 3 axes, 3 times/ axis non-operation.
- Vibration: (Note 3)
  - Non-operation: 1.88G rms, 5 - 500Hz, 3 axes, with package
  - Operation: 0.5G rms, 5 - 500Hz, each axis with flash disk drive.

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Note:

1. Certified with ADLINK thermal design. The thermal performance is dependent on the cooling design.
2. Temperature limit of optional mass storage devices may have an impact on the thermal specification of the board.
3. Operational vibration is limited by the 2.5 inch HDD. When the application requires higher definition for anti-vibration, we recommend using Flash2000 Flash Disk (FFD series) or CompactFlash to avoid using the hard disk drive.

Safety Certificate and Test

- CE; FCC Class B
- HALT (temperature and vibration stress) verified
- All plastic material, PCB and Battery used are all UL-94V0 certified
- Designed for NEBS 3.0 requirement
- MTBF: >100,000 hours

Power Requirement (Typical)

Typical Current and Maximum Current	+5V (+/-5%)	+3.3V (+/-5%)	+12V (+/-5%)	-12V (+/-5%)
cPCI-6810A/P9	2.28A 3.73A	4.10A 14.636A	3mA 8mA	0mA 0mA
cPCI-6810A/P9 with HDD	2.94A 3.73A+HDD	4.82A 14.636A	3mA 8mA	0mA 0mA
cPCI-6810A/1G	2.50A 3.88A	4.10A 14.636A	3mA 8mA	0mA 0mA

Table 1-3: Power Requirement (Typical)

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Typical Current and Maximum Current	+5V (+/-5%)	+3.3V (+/-5%)	+12V (+/-5%)	-12V (+/-5%)
cPCI-6810A/1G (Without PMC, VGA cards & RTM)	1.44A 3.73A	3.64A 14.636A	3mA 8mA	0mA 0mA
cPCI-6810/1G with HDD	3.16A 3.88A+HDD	4.76A 14.636A	3mA 8mA	0mA 0mA
cPCI-6820A/P9	2.66A 3.73A	4.36A 16.526A	3mA 8mA	0mA 0mA
cPCI-6820A/P9 with HDD	3.56A 3.73A+HDD	5.36A 16.526A	3mA 8mA	0mA 0mA
cPCI-6820B/1G	3.38A 3.88A	4.98A 16.526A	3mA 8mA	0mA 0mA
cPCI-6820B/1G with HDD	4.34A 3.88A+HDD	5.92A 16.526A	3mA 8mA	0mA 0mA
cPCI-6820B/1G (Without PMC card)	3.79A 3.88A+HDD	5.26A 16.526A	3mA 8mA	0mA 0mA
cPCI-6820A /1G	TBD 3.88A	TBD 18.416A	3mA 8mA	0mA 0mA

Table 1-3: Power Requirement (Typical)

Test conditions

- Single or Dual LV P-III 933M or 1GHz.
- Memory: 1GB (512MB x 2) or 1.5GB (512MBx3).
- HDD: FUJITSU MHR2040AT 40GB installed on RTM (Max. current requirement is 0.55A @ +5V.
- CompactFlash: PQI 64MB Flash Card.
- PMC card: ADLINK PMC-8615 Gigabit Ethernet Card.
- PMC VGA card: ADLINK PMC-8217V (only available with CRUX-SP).

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I/O Connectivity

I/O	cPCI-6820		cPCI-6810		RTM (cPCI-R6820)		
	Faceplate	Board	Faceplate	Board	J3/J5	Faceplate	Board
Serial Port (COM1)	RJ-45	--	--	--	J5	RJ-45	--
Serial Port (COM2)	--	--	--	--	J5	--	10-pin Header
PS2 Keyboard	PS2	--	--	--	J3	PS2	--
PS2 Mouse	PS2	--	--	--	J3	PS2	--
VGA	DB-15	--	--	--	J5	DB-15	--
USB (port 0, port 1)	USB x 2	--	USB x 2	--	J5	--	--
USB (port 2, port 3)	--	--	--	--	J5	USB x 2	--
Gigabit Ethernet Port 1	--	2.16	--	2.16	J3	RJ-45	--
Gigabit Ethernet Port 2	--	2.16	--	2.16	J3	RJ-45	--
ATA-100 Primary IDE	--	44-pin	--	44-pin	J5	--	40-pin 44-pin
ATA-100 Secondary IDE	--	--	--	--	J5	--	40-pin CF-type 2
PC Beeper	--	--	--	--	J5	--	4-pinHeader
General Purpose LED	Y	--	Y	--	--	--	--
Reset button	Y	--	Y	--	--	--	--
PMC #1	--	Y	--	Y	--	--	--
PMC #2	--	--	--	Y	J3	--	--

Table 1-4: I/O Connectivity

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1.5 Model Variations

The cPCI-6810/6820 series products include the following four base configurations. All models have the CPU pre-mounted. The number of SO-DIMM sockets and PMC slots are varied depending on the model. If a HDD is installed onboard, it may occupy and sacrifice one PMC socket space. Note that the RTM is sold separately and are not listed in the following table.

	I	II	III	IV
	cPCI-6810A/P9	**cPCI-6810B/P9**	**cPCI-6820A/P9**	**cPCI-6820B/P9**
Slot Width	1-slot	1-slot	1-slot	1-slot
CPU	Single P III-933	Single P III-933	Dual P III-933	Dual P III-933
Memory sockets	Single x 2	Single x1+ Dual x1	Single x1+ Dual x1	Dual x 2
Max. SO-DIMM#	2	3	3	4
Max. Memory	1GB	1.5GB	1.5GB	2.0GB
2.5 inches HDD installation	Possible	Possible	Possible	Not Feasible
PMC slot # (without HDD)	2	1	1	0
PMC slot # (with HDD)	1	0	0	0
Onboard VGA	N/A	N/A	CT69000	CT69000
PS/2 Keyboard	On RTM	On RTM	Y (rear, front)	Y (rear, front)
PS/2 mouse	On RTM	On RTM	Y (rear, front)	Y (rear, front)
	V	**VI**	**VII**	**VIII**
	cPCI-6810A/1G	**cPCI-6810B/1G**	**cPCI-6820A/1G**	**cPCI-6820B/1G**
CPU	Single P III-1033	Single P III-1033	Dual P III-1033	Dual P III-1033

Table 1-5: CPCI-6810/6820 Model Variations Table

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The following table lists the recommended PMC modules made by ADLINK, which are compatible with 6820 series SBC.

Model number	Description/Configuration
PMC-8217	SMI SM-721 VGA PMC card
PMC-8615	Single Port 64-bit/66MHz Gigabit Ethernet PMC card
PMC-8611	Single Port 32-bit/33MHz Fast Ethernet PMC card
PMC-8670	Port80 Display PMC card

Table 1-6: Recommended PMC Modules

The following table lists the recommended chassis available from ADLINK, which are compatible with the cPCI-6810/6820 series SBC.

Chassis	Description / Configuration
cPCIS-6130R	19” 1U high standard depth chassis with RIO
cPCIS-6400X	19” 4U high chassis, 4-slot I/O, 64-bit BP, ATX Power
cPCIS-6400U	19” 4U high chassis, 4-slot I/O, 64-bit BP, Redundant cPCI Power
cPCIS-3140	19” 8U high chassis, 7-slot I/O, 64-bit BP, Redundant AC Input Power with Door, all sub-models
cPCIS-3330/64	19” 9U high chassis, 7-slot I/O, 64-bit BP, Redundant cPCI Power, all sub-models
cPCIS-3100BLS	19” 8U high chassis, 9-slot compute blades, Redundant AC Input Power with Door, all models
cPCIS-3300BLS	19” 9U high PICMG 2.16 chassis, 12 node slots with two fabric slots and three 6U cPCI redundant power slots

Table 1-7: Recommended Chassis

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2 Jumpers and Connectors

This chapter will familiarize the user with the cPCI-6810/6820 before getting started; information on the board layout, connector definitions, and jumper setup is provided. It also includes the following information:

- cPCI-6810/6820 board outline and illustration
- cPCI-R6820 board outline and illustration
- Connectors pin assignments

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2.1 cPCI-6820 / 6810 Board Outline and Illustration

cPCI-6820 Top and Front View

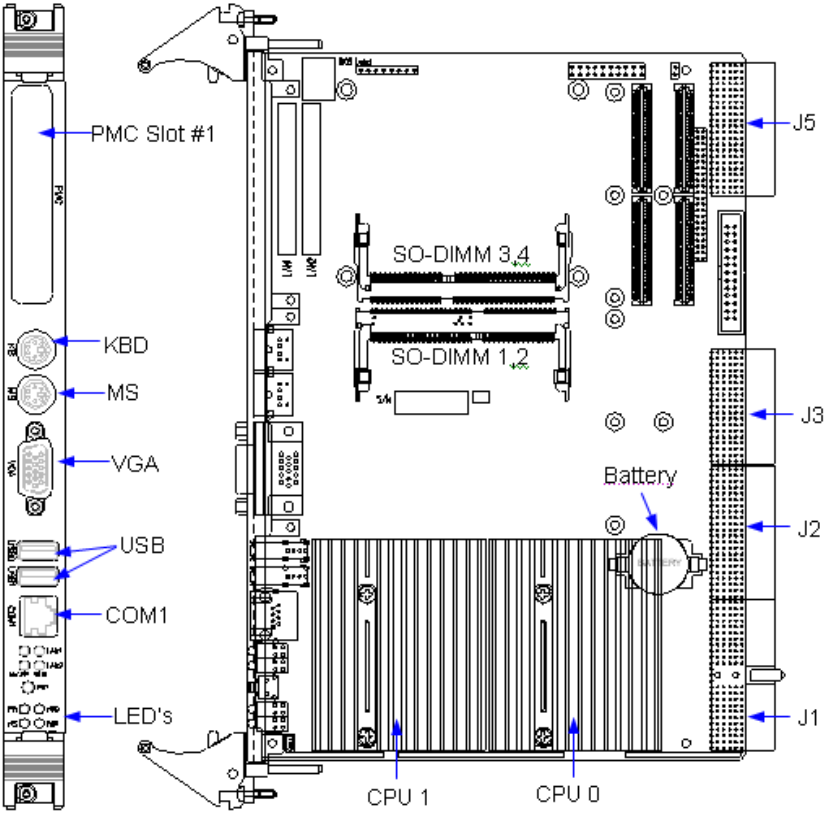


Figure 2-1: Top and Front View of cPCI-6820

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cPCI-6820 Model comparison table

	cPCI-6820A/P9	cPCI-6820B/P9
No. of Memory sockets	3	4
SO-DIMM 1,2	Dual SODIMM	Dual SODIMM
SO-DIMM 3,4	Single SODIMM	Dual SODIMM (1)
Max. Memory	1.5GB	2.0GB
HDD Installation	Possible	Not Feasible (1)
PMC slot# (without HDD)	1	0
PMC slot# (with HDD)	0 (2)	0

Table 2-1: Comparison of cPCI-6820A and cPCI-6820B

Note:

1. Because of dual stack SO-DIMM 3, four sockets are installed, there is no space for a HDD.
2. If the cPCI-6820A is installed with a HDD, the PMC socket is unavailable.

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cPCI-6810 Top and Front View

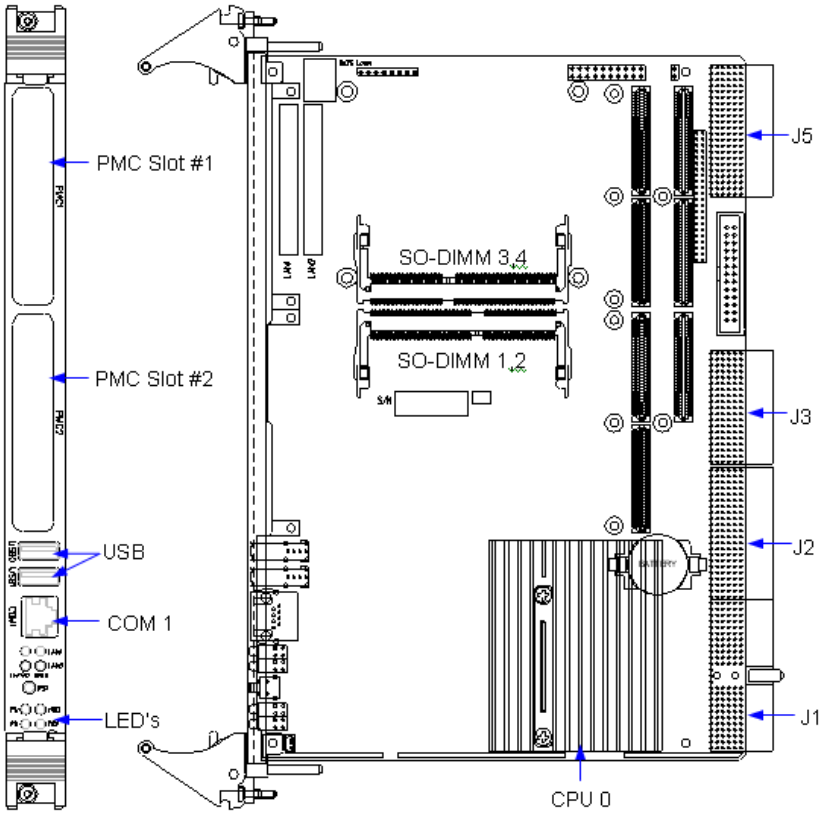


Figure 2-2: Top and Front View of cPCI-6810

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cPCI-6810 Model comparison table

	cPCI-6810A/P9	cPCI-6810B/P9
No. of Memory sockets	2	3
SO-DIMM 1, 2	Single SODIMM	Dual SODIMM (1)
SO-DIMM 3, 4	Single SODIMM	Single SODIMM
Max. Memory	1.0GB	1.5GB
HDD Installation	Possible	Possible
PMC slot# (without HDD)	2	1 (1)
PMC slot# (with HDD)	1 (2)	0 (2)

Table 2-2: Comparison of cPCI-6810A and cPCI-6810B

Note:

1. Dual stack SO-DIMM 1, two sockets will occupy the PMC slot space, so only one PMC slot is available on the cPCI-6810B.
2. If a HDD is installed, then PMC slot #1 becomes unavailable.

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2.2 cPCI-R6820 Board Outline and Illustration

cPCI-R6820 Top and Front View

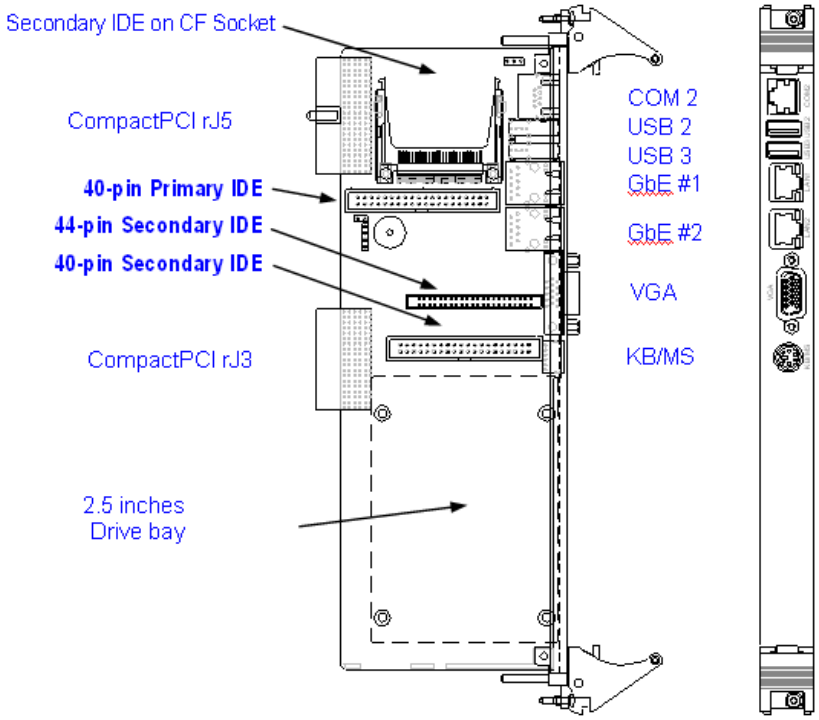
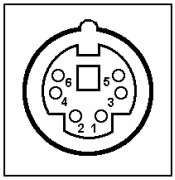


Figure 2-3: Top and front View of cPCI-R6820

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2.3 Connectors Pin Assignment

Keyboard Connector

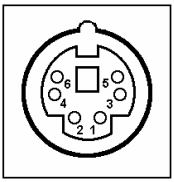


Pin	Signal	Function
1	KBDATA	Keyboard Data
2	NC	No Connect
3	GND	Ground
4	+5V	Power
5	KBCLK	Keyboard Clock
6	NC	No connect

Table 2-3: Keyboard Connector

Note: Circular DIN keyboard connector is available on the cPCI-6820 only. The cPCI-6810 does not support a keyboard connector.

Mouse Connector



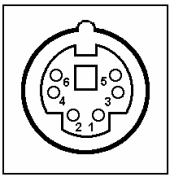
Pin	Signal	Function
1	MSDATA	Mouse Data
2	NC	No Connect
3	GND	Ground
4	+5V	Power
5	MSCLK	Mouse Clock
6	NC	No Connect

Table 2-4: Mouse Connector

Note: Circular DIN mouse connector is available on the cPCI-6820 only. The cPCI-6810 does not support a mouse connector.

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Keyboard and Mouse Combo Connector



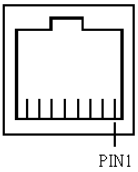
Pin	Signal	Function
1	KBDATA	Keyboard Data
2	MSDATA	Mouse Data
3	GND	Ground
4	+5V	Power
5	KBCLK	Keyboard Clock
6	MSCLK	Mouse Clock

Table 2-5: Keyboard and Mouse Combo Connector

Note: Keyboard and Mouse Combo Connector is available on the cPCI-R6820 RTM only. A Y-cable is shipped with the RTM and can be used to connect a PS/2 keyboard and mouse simultaneously. Direct connection of a PS/2 keyboard is also supported for applications that do not require a mouse.

Serial Port Connectors

Serial Port on RJ-45 Connector

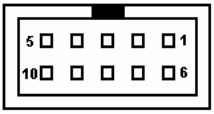


Pin	Signal Name
1	DCD, Data carrier detect
2	RTS, Request to send
3	DSR, Data set ready
4	TXD, Transmit data
5	RXD, Receive data
6	GND, ground
7	CTS, Clear to send
8	DTR, Data terminal ready

Table 2-6: COM1 on front board or COM2 on the RTM

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Serial Port on 10-pin Header Connector

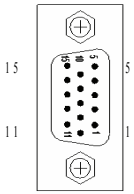


Pin	Signal Name
1	DCD: Data Carrier Detect
2	RXD: Receive Data
3	TXD: Transmit Data
4	DTR: Data Terminal Ready
5	Ground
6	DSR: Data Set Ready
7	RTS: Request to Send
8	CTS: Clear to Send
9	RI: Ring Indicate
10	No Connect

Table 2-7: COM1 on RTM

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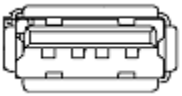
VGA Connector



Signal Name	Pin	Pin	Signal Name
Red	1	2	Green
Blue	3	4	N.C.
GND	5	6	GND
GND	7	8	GND
+5V.	9	10	GND
N.C.	11	12	N.C.
HSYNC	13	14	VSYNC
NC	15		

Table 2-8: TVGA Connector on cPCI-6820 and RTM

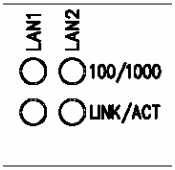
USB Connector



Pin	Signal Name
1	VCC
2	USB-
3	USB+
4	Ground

Table 2-9: USB Connector

LED for Gigabit Ethernet Ports

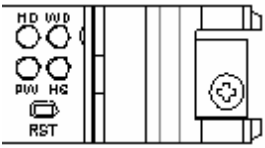


LED	Color	Status	Description
Link Speed LED	Green	OFF	10 or 100 Mbps
		ON	1000 Mbps
Link / Activity LED	Amber	OFF	No Link
		ON	Linked
		Blinking	Port Accessing

Table 2-10: LED indicators on the GbE ports

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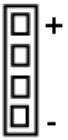
General Purpose LED definitions



LED	Color	Status	Description
IDE Media Access	Red	OFF	IDE idle
		ON	IDE access
Power OK	Green	OFF	System is not power-on or power failed
		ON	Power ON
Hot swap-pable status	Blue	OFF	Board inserted and power on
		ON	Board inserted but not power on yet

Table 2-11: General Purpose LED definitions

Speaker connector on RTM

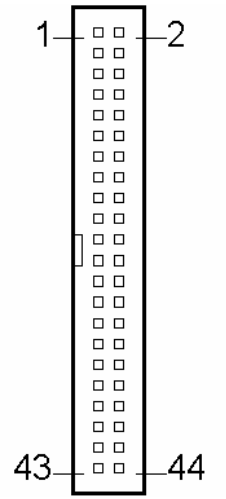


Pin	Signal Name
1	SPK-
2	GND
3	GND
4	SPK+

Table 2-12: Speaker Connector on RTM

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44-pin IDE Port



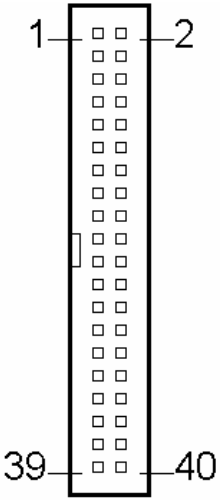
Signal	Pin	Pin	Signal
RESET-	1	2	Ground
DD7	3	4	DD8
DD6	5	6	DD9
DD5	7	8	DD10
DD4	9	10	DD11
DD3	11	12	DD12
DD2	13	14	DD13
DD1	15	16	DD14
DD0	17	18	DD15
Ground	19	20	N.C (key pin)
DMARQ	21	22	Ground
DIOW-	23	24	Ground
DIOR-	25	26	Ground
IORDY	27	28	CSEL
DMACK-	29	30	Ground
INTRQ	31	32	reserved
DA1	33	34	PDIAG-
DA0	35	36	DA2
CS0-	37	38	CS1-
DASP-	39	40	Ground
+5V	41	42	+5V
Ground	43	44	TYPE-

Table 2-13: 44-pin IDE connector

Note: Primary IDE is on the front board (CN8) on the RTM.

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40-pin IDE Port



Signal	Pin	Pin	Signal
RESET-	1	2	Ground
DD7	3	4	DD8
DD6	5	6	DD9
DD5	7	8	DD10
DD4	9	10	DD11
DD3	11	12	DD12
DD2	13	14	DD13
DD1	15	16	DD14
DD0	17	18	DD15
Ground	19	20	+5V (for DOM)
DMARQ	21	22	Ground
DIOW-	23	24	Ground
DIOR-	25	26	Ground
IORDY	27	28	CSEL
DMACK-	29	30	Ground
INTRQ	31	32	reserved
DA1	33	34	PDIAG-
DA0	35	36	DA2
CS0-	37	38	CS1-
DASP-	39	40	Ground

Table 2-14: 40-pin Primary and Secondary IDE channels on the RTM

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IPMB Interface on RTM

Pin	Signal Name
1	IPMB_CLK
2	GND
3	IPMB_DATA
4	IPMB_PWR
5	N.C

Table 2-15: IPMI Interface on RTM

The IPMB interface is connected to the rJ5 of the RTM. The IPMB_PWR is connected to pin-C1 of the rJ5.

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CompactPCI J1 Pin Assignments

Pin	Z	A	B	C	D	E	F
25	GND	+5V	REQ64#	ENUM# (4)	+3.3V	+5V	GND
24	GND	AD [1]	+5V	V (I/O)	AD [0]	ACK64#	GND
23	GND	+3.3V	AD [4]	AD [3]	+5V	AD [2]	GND
22	GND	AD [7]	GND	+3.3V	AD [6]	AD [5]	GND
21	GND	+3.3V	AD [9]	AD [8]	M66EN	C/BE [0]#	GND
20	GND	AD [12]	GND	V (I/O)	AD [11]	AD [10]	GND
19	GND	+3.3V	AD [15]	AD [14]	GND	AD [13]	GND
18	GND	SERR#	GND	+3.3V	PAR	C/BE [1]#	GND
17	GND	+3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	GND	V (I/O)	STOP#	LOCK#	GND
15	GND	+3.3V	FRAME#	IRDY#	BDSEL	TRDY#	GND
12-14	Key						
11	GND	AD [18]	AD [17]	AD [16]	GND	C/BE [2]#	GND
10	GND	AD [21]	GND	+3.3V	AD [20]	AD [19]	GND
9	GND	C/BE[3]#	IDSE	AD [23]	GND	AD [22]	GND
8	GND	AD [26]	GND	V (I/O)	AD[25]	AD [24]	GND
7	GND	AD [30]	AD [29]	AD [28]	GND	AD [27]	GND
6	GND	REQ#	GND	+3.3V	CLK	AD [31]	GND
5	GND	Reserved (1)	Reserved (1)	PCIRST#	GND	GNT#	GND
4	GND	IPMB_PWR	HEALTHY#	V (I/O)	INTP (1)	INTS	GND
3	GND	INTA#	INTB#	INTC#	+5V	INTD#	GND
2	GND	TCK (3)	+5V	TMS (2)	TDO (1)	TDI (2)	GND
1	GND	+5V	-12V	TRST# (3)	+12V	+5V	GND
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**

Table 2-16: CompactPCI J1 pin assignments

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Note:	(1) These signals are not connected. (2) These signals are pulled high on the board. (3) These signals are pulled low on the board. (4) As a peripheral CPU, ENUM# is automatically driven during insertion or extraction to support PICMG 2.1 hot-swap. As a system host CPU (slot-1), ENUM# can be disabled (factory default) or routed to IRQ 7, 10, or 11 using BIOS settings under "Advanced Chipset Features." If an IRQ is assigned, it should be reserved under "PnP/PCI Configurations".

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CompactPCI J2 Pin Assignments

Pin	Z	A	B	C	D	E	F
22	GND	GA4 (2)	GA3 (2)	GA2 (2)	GA1 (2)	GA0 (2)	GND
21	GND	CLK6	GND	BRSV (1)	BRSV (1)	BRSV (1)	GND
20	GND	CLK5	GND	BRSV (1)	GND	BRSV (1)	GND
19	GND	GND	GND	IPMBSDA (1)	IPMBSCL (1)	IPMBALR (1)	GND
18	GND	BRSV (1)	BRSV (1)	BRSV (1)	GND	BRSV (1)	GND
17	GND	BRSV (1)	GND	PRST#	REQ6#	GNT6#	GND
16	GND	BRSV (1)	BRSV (1)	DEG#	GND	BRSV (1)	GND
15	GND	BRSV (1)	GND	FAL#	REQ5#	GNT5#	GND
14	GND	AD [35]	AD [34]	AD [33]	GND	AD [32]	GND
13	GND	AD [38]	GND	V (I/O)	AD [37]	AD [36]	GND
12	GND	AD [42]	AD [41]	AD [40]	GND	AD [39]	GND
11	GND	AD [45]	GND	V (I/O)	AD [44]	AD [43]	GND
10	GND	AD [49]	AD [48]	AD [47]	GND	AD [46]	GND
9	GND	AD [52]	GND	V (I/O)	AD [51]	AD [50]	GND
8	GND	AD [56]	AD [55]	AD [54]	GND	AD [53]	GND
7	GND	AD [59]	GND	V (I/O)	AD [58]	AD [57]	GND
6	GND	AD [63]	AD [62]	AD [61]	GND	AD [60]	GND
5	GND	C/BE [5]#	GND	V (I/O)	C/BE [4]#	PAR 64	GND
4	GND	V (I/O)	BRSV (1)	C/BE [7]#	GND	C/BE [6]#	GND
3	GND	CLK4	GND	GNT3#	REQ#4	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND
Pin	Z	A	B	C	D	E	F

Table 2-17: CompactPCI J2 pin assignments

Note:
(1) These signals are not connected.
(2) These signals are pulled high on the board.
(3) These signals are pulled low on the board.

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CompactPCI J3 and rJ3 Pin Assignments

Pin	Z	A	B	C	D	E	F
19	GND	GND	+12V (1)	GND	-12V (1)	GND	GND
18	GND	LPa_DA0+	LPa_DA0-	GND	LPa_DC0+	LPa_DC0-	GND
17	GND	LPa_DB0+	LPa_DB0-	GND	LPa_DD0+	LPa_DD0-	GND
16	GND	LPb_DA1+	LPb_DA1-	GND	LPb_DC1+	LPb_DC1-	GND
15	GND	LPb_DB1+	LPb_DB1-	GND	LPb_DD1+	LPb_DD1-	GND
14	GND	+3.3V (1)	+3.3V (1)	+3.3V (1)	+5V (1)	+5V (1)	GND
13	GND	PMCIO5	PMCIO4	PMCIO3	PMCIO2	PMCIO1	GND
12	GND	PMCIO10	PMCIO9	PMCIO8	PMCIO7	PMCIO6	GND
11	GND	PMCIO15	PMCIO14	PMCIO13	PMCIO12	PMCIO11	GND
10	GND	PMCIO20	PMCIO19	PMCIO18	PMCIO17	PMCIO16	GND
9	GND	PMCIO25	PMCIO24	PMCIO23	PMCIO22	PMCIO21	GND
8	GND	PMCIO30	PMCIO29	PMCIO28	PMCIO27	PMCIO26	GND
7	GND	PMCIO35	PMCIO34	PMCIO33	PMCIO32	PMCIO31	GND
6	GND	PMCIO40	PMCIO39	PMCIO38	PMCIO37	PMCIO36	GND
5	GND	PMCIO45	PMCIO44	PMCIO43	PMCIO42	PMCIO41	GND
4	GND	PMCIO50	PMCIO49	PMCIO48	PMCIO47	PMCIO46	GND
3	GND	PMCIO55	PMCIO54	PMCIO53	PMCIO52	PMCIO51	GND
2	GND	PMCIO60	PMCIO59	PMCIO58	PMCIO57	PMCIO56	GND
1	GND	VIO (2)	PMCIO64	PMCIO63	PMCIO62	PMCIO61	GND
Pin	Z	A	B	C	D	E	F

Table 2-18: CompactPCI J3 and rJ3 pin assignments

Note:
(1) The +3.3V, +5V, and +/-12V power lines are supplied from the main board to the RTM.
(2) The VIO is connected to the VIO plane (default is +5V) of PMC slot #2.

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CompactPCI J5 and rJ5 Pin Assignments

Pin	Z	A	B	C	D	E	F
22	GND	DA2	C-	CS3-	DA1	DASP-	GND
21	GND	DIOW-	DMACK-	DIOR-	PDIAG-	DA0	GND
20	GND	DD0	DD15	INTRQ	DMARQ	IORDY	GND
19	GND	DD12	DD2	DD13	DD1	DD14	GND
18	GND	DD5	DD10	DD4	DD11	DD3	GND
17	GND	DRESET-	DD7	DD8	DD6	DD9	GND
16	GND	USB-0+ (5)	USB-0- (5)	GND	USB-1+ (5)	USB-1- (5)	GND
15	GND	SMUX (4)	GND	SMUX (4)	GND	SMUX (4)	GND
14	GND	SMUX (4)	SMUX (4)	SMUX (4)	SMUX (4)	SMUX (4)	GND
13	GND	+5V (2)	+5V (2)	+5V (2)	+3.3V (2)	+3.3V (2)	GND
12	GND	DDCCLK	DDCDAT	GND	GND	GND	GND
11	GND	VSYNC	HSYNC	BLUE	GREEN	RED	GND
10	GND	USB-2+	USB-2-	GND	USB-3+	USB-3-	GND
9	GND	RSVD (1)	RSVD (1)	GND	RSVD (1)	RSVD (1)	GND
8	GND	SDA2	SDC-	SDCS3-	SDA1	SDASP-	GND
7	GND	SDIOW-	SDDACK-	SDIOR-	SPDIAG-	SDA0	GND
6	GND	SDD0	SDD15	SINTRQ	SDDREQ	SDIORDY	GND
5	GND	SDD12	SDD2	SDD13	SDD1	SDD14	GND
4	GND	SDD5	SDD10	SDD4	SDD11	SDD3	GND
3	GND	SDRESET-	SDD7	SDD8	SDD6	SDD9	GND
2	GND	MSDATA	MSCLK	KBDATA	KBCLK	PCBEEP	GND
1	GND	IPMB_CLK	IPMB_DAT	IPMB_PWR	RSVD (1)	USB_OC (3)	GND
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**

Table 2-19: CompactPCI J5 and rJ5 pin assignments

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Note:	(1) The pins are reserved with no connection. (2) The 3.3V and 5V power lines are supplied from the main board to the RTM. (3) USB_OC is the USB over-current feedback from the RTM to main board. (4) The SMUX signals are used for serial COM port extension. (5) USB Ports 1 and 2 are not used on the cPCI-R6820 RTM.

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PMC Connector Pin Assignments

PMC J11/J21 and J12/J22 Connector Pin Assignments

Signal Name	J11/J21 Pin	J11/J21 Pin	Signal Name		Signal Name	J12/J22 Pin	J12/J22 Pin	Signal Name
TCK (3)	1	2	-12V		+12V	1	2	TRST# (3)
GND	3	4	INTA#		TMS (2)	3	4	TDO (1)
INTB#	5	6	INTC#		TDI (2)	5	6	GND
BM1 (1)	7	8	+5V		GND	7	8	N/C
INTD#	9	10	N/C		N/C	9	10	N/C
GND	11	12	+3.3V		BM2 (2)	11	12	+3.3V
CLKP1	13	14	GND		RST#	13	14	BM3 (3)
GND	15	16	GNT0#		+3.3V	15	16	BM4 (3)
REQ0#	17	18	+5V		PME#	17	18	GND
VIO (4)	19	20	AD31		AD30	19	20	AD29
AD28	21	22	AD27		GND	21	22	AD26
AD25	23	24	GND		AD24	23	24	+3.3V
GND	25	26	CBE3#		IDSEL	25	26	AD23
AD22	27	28	AD21		+3.3V	27	28	AD20
AD19	29	30	+5V		AD18	29	30	GND
VIO (4)	31	32	AD17		AD16	31	32	CBE2#
P1FRAME#	33	34	GND		GND	33	34	IDSL_B (1)
GND	35	36	IRDY#		TRDY#	35	36	+3.3V
DEVSL	37	38	+5V		GND	37	38	STOP#
GND	39	40	LOCK#		PERR#	39	40	GND
N/C	41	42	N/C		+3.3V	41	42	SERR#
PAR	43	44	GND		CBE1#	43	44	GND
VIO (4)	45	46	AD15		AD14	45	46	AD13
AD12	47	48	AD11		M66EN	47	48	AD10
AD9	49	50	+5V		AD8	49	50	+3.3V
GND	51	52	CBE0#		AD7	51	52	REQ_B# (1)
AD6	53	54	AD5		+3.3V	53	54	GNT_B# (1)
AD4	55	56	GND		N/C	55	56	GND
VIO (4)	57	58	AD3		N/C	57	58	EREADY (1)
AD2	59	60	AD1		GND	59	60	RSTOUT# (1)
AD0	61	62	+5V		ACK64#	61	62	+3.3V
GND	63	64	REQ64#		GND	63	64	Monarch# (1)

Table 2-20: PMC J11/J21 and J12/J22 Connector Pin Assignments

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PMC J13/J23 and J24 Connector Pin Assignments

Signal Name	J13/ J23 Pin	J13/ J23 Pin	Signal Name
N/C	1	2	GND
GND	3	4	CBE [7]
CBE [6]	5	6	CBE [6]
CBE [5]	7	8	GND
VIO (4)	9	10	PAR64
AD63	11	12	AD62
AD61	13	14	GND
GND	15	16	AD60
AD59	17	18	AD58
AD57	19	20	GND
VIO (4)	21	22	AD56
AD55	23	24	AD54
AD53	25	26	GND
GND	27	28	AD52
AD51	29	30	AD50
AD49	31	32	GND
GND	33	34	AD48
AD47	35	36	AD46
AD45	37	38	GND
VIO (4)	39	40	AD44
AD43	41	42	AD42
AD41	43	44	GND
GND	45	46	AD40
AD39	47	48	AD38
AD37	49	50	GND
GND	51	52	AD36
AD35	53	54	AD34
AD33	55	56	GND
VIO (4)	57	58	AD32
N/C	59	60	N/C
N/C	61	62	GND
GND	63	64	N/C

Signal Name	J24 Pin	J24 Pin	Signal Name
PMCIO1	1	2	PMCIO2
PMCIO3	3	4	PMCIO4
PMCIO5	5	6	PMCIO6
PMCIO7	7	8	PMCIO8
PMCIO9	9	10	PMCIO10
PMCIO11	11	12	PMCIO12
PMCIO13	13	14	PMCIO14
PMCIO15	15	16	PMCIO16
PMCIO17	17	18	PMCIO18
PMCIO19	19	20	PMCIO20
PMCIO21	21	22	PMCIO22
PMCIO23	23	24	PMCIO24
PMCIO25	25	26	PMCIO26
PMCIO27	27	28	PMCIO28
PMCIO29	29	30	PMCIO30
PMCIO31	31	32	PMCIO32
PMCIO33	33	34	PMCIO34
PMCIO35	35	36	PMCIO36
PMCIO37	37	38	PMCIO38
PMCIO39	39	40	PMCIO40
PMCIO41	41	42	PMCIO42
PMCIO43	43	44	PMCIO44
PMCIO45	45	46	PMCIO46
PMCIO47	47	48	PMCIO48
PMCIO49	49	50	PMCIO50
PMCIO51	51	52	PMCIO52
PMCIO53	53	54	PMCIO54
PMCIO55	55	56	PMCIO56
PMCIO57	57	58	PMCIO58
PMCIO59	59	60	PMCIO60
PMCIO61	61	62	PMCIO62
PMCIO63	63	64	PMCIO64

Table 2-21: PMC J13/J23 and J24 Connector Pin Assignments

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Note:

(1) These signals are not connected on the board.

(2) These signals are pulled high on the board.

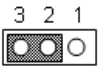
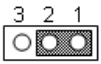
(3) These signals are pulled low on the board.

(4) By default, the VIO signals are set to +5V via zero ohm resistors. Therefore, DO NOT apply any “3.3V only” PMC module to the PMC sockets.

(5) J24 signals are connected to the CompactPCI J3 connector. To use these signals, the RTM needs to be custom designed for special purposes or have a PIM connector available onboard. Please contact ADLINK for details on customized RTM applications.

IDE Setting Jumper on the RTM

A CompactFlash (CF) socket is available on the RTM as a Secondary IDE port. A 3-pin jumper (CN12) is used to set the CF card as either master or slave device of the IDE channel.

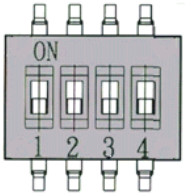
	CF card is a Master IDE device
	CF card is a Slave IDE device (default factory setting)

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GbE Connection Selection

The cPCI-6820 supports dual Ethernet connection for PICMG2.16 compliant backplanes and the RTM. While using the PICMG 2.16 compliant backplane, it is recommended that none of the GbE ports on the rear panel be used. There are four mini switches that control the GbE routing located on the bottom side (solder side) of the RTM. Refer to the following information to choose either PICMG 2.16 or rear panel Ethernet connections.

S3, S4: LAN1 Connecting Selection

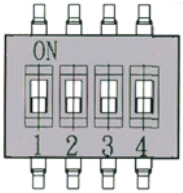


LAN 1 Connecting	Switch S3		Switch S4	
	Pin	State	Pin	State
Connect to PICMG 2.16 Backplane	S3-1	OFF	S4-1	OFF
	S3-2	OFF	S4-2	OFF
	S3-3	OFF	S4-3	OFF
	S3-4	OFF	S4-4	OFF
Connect to Rear Panel (Default)	S3-1	ON	S4-1	ON
	S3-2	ON	S4-2	ON
	S3-3	ON	S4-3	ON
	S3-4	ON	S4-4	ON

Table 2-22: LAN1 Connection Selection

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S1, S2: LAN2 Connecting Selection



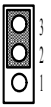
LAN 2 Connecting	Switch S1		Switch S2	
	Pin	State	Pin	State
Connect to PICMG 2.16 Backplane only	S1-1	OFF	S2-1	OFF
	S1-2	OFF	S2-2	OFF
	S1-3	OFF	S2-3	OFF
	S1-4	OFF	S2-4	OFF
Connect to Rear Panel (Default)	S1-1	ON	S2-1	ON
	S1-2	ON	S2-2	ON
	S1-3	ON	S2-3	ON
	S1-4	ON	S2-4	ON

Table 2-23: LAN2 Connecting Selection

Setting Jumper on cPCI-6810/6820

A 3-pin jumper (JP1) is used to set the SBC as either “in normal operation” or “forcing the SBC to SYSTEM mode”.

Note: When cPCI-6810/6820 in the Packet Switching Backplane has no PCI bus, set JP1 as “1-2”.

	Normal operation (Default setting)
	Force cPCI-6810/6820 to SYSTEM mode

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Pin	Signal Name
1	GND
2	SYSEN#
3	NC

Table 2-24: Setting Jumper on cPCI-6810/6820

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3 Getting Started

This chapter provides information on how to install the necessary components on the cPCI-6810/6820 and cPCI-R6820 RTM. The topics covered are:

- CPU and heat sink
- Memory module installation
- HDD installation on main board
- HDD installation on RTM
- CF installation on RTM
- PMC installation
- RTM installation
- Main board installation

3.1 CPU and Heatsink

The cPCI-6810/6820 SBC supports the Intel® Pentium® III Processor - Low Power up to 1033MHz, which is pre-mounted to the PCB (printed circuit board). The heatsink has also been pre-mounted in the factory. There is no jumper setting necessary to set the CPU operating frequency or CPU type.

WARNING: DO NOT try to replace the CPU in the field or remove the heatsink. It will cause board defects and void all warranty for the board.



3.2 Memory Module Installation

The cPCI-6810/6820 SBC supports up to four sockets of 144-pin PC-133 registered ECC SO-DIMMs. The maximum memory capacity is therefore 2GB. If memory modules are pre-installed when the package is received, this section can be skipped.

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The chipset supports 64Mb, 128Mb, 256Mb, and 512Mb memory technologies. The supported DRAM types are listed in the following table.

DRAM Depth	DRAM Type (Row/Column)
16M 2-bank SDRAM	11/9
	11/10
64M 2-bank SDRAM	13/10
64M 4-bank SDRAM	12/8
	12/9
	12/10
	13/10
	12/9
128M 4-bank SDRAM	12/10
	13/10
256M 4-bank SDRAM	13/8
	13/9
	13/10
	13/11

Table 3-1: Supported SDRAM Chip

While installing the SO-DIMM, ensure that the SO-DIMM modules are firmly seated in its sockets and do not interfere with any components.

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3.3 HDD Installation on Main Board

A slim-type 2.5-inch HDD can be mounted to the cPCI-6810/6820 main board. If a HDD comes pre-installed in the cPCI-R6820 product package, this section may be skipped.

1. Remove the PMC Key-bolt of the PMC slot #1.
2. Screw the bolts on to the HDD; attach a 44-pin IDE cable.
3. Install the assembly on to the board; tighten the four screws from the bottom side of the main board to secure the HDD in place.
4. Attach the other end of the 44-pin IDE cable to CN4 on the board.

3.4 HDD Installation on RTM

A 2.5 inches HDD or Flash Disk can be installed on the RTM directly. If a HDD comes pre-installed, please skip this section.

1. Attach the IDE cable to the HDD or Flash Disk
2. Put the HDD on component side of the RTM, align the HDD's mounting holes with the holes on the PCB.
3. Tighten the four screws from the bottom side of the RTM to secure the HDD in place.
4. Connect the IDE cable to the 44-pin connector CN4.

3.5 CF Installation on RTM

The CompactFlash Card (or called CF storage card) is widely applied in digital consumer devices such as PDA's, Digital Cameras, and MP3 players. Because of the CF anti-shock, anti-vibration, better environment tolerance, low power consumption, small form factor, and high reliability, it has been widely accepted in mission critical embedded applications.

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With the cPCI-6810/6820, the CF card is very easy to use; the CF card socket is available on the cPCI-R6820, which is a rear transition module.

3.6 PCI Mezzanine Card (PMC) Installation

The PMC slots are designed as 5V and / or as a universal PCI interface. The PMC sites are keyed to prevent users from installing a 3.3V only PMC module.

The rear I/O signals on the J14 of the upper PMC slot are routed to J3 of the 6810/6820 mainboard. Refer to section 2.3 and 2.3 for detailed PMC I/O signal routing. If a HDD is mounted to the mainboard, the HDD will occupy the upper PMC slot #1.

Installation of the PMC modules:

1. Prepare an ESD protected area including an anti-ESD table and ESD strap. Attach the ESD strap to your wrist and connect the end to the ground of the anti-ESD table.
2. Remove the PMC panel from the front panel.
3. Install the PMC module onto the PMC sockets.
4. Screw the PMC mounting bolts to the main board from the bottom side up to fix the PMC module in place.

3.7 RTM Installation

This section describes important information regarding the use of the rear I/O connections. Refer to section 2.4 for peripheral connectivity of all I/O ports on the RTM. When installing the cPCI-6820 and its RTM, make sure the RTM is the correct model that matches its front board.

WARNING: Use the correct RTM to enable functions (I/O interfaces) on rear side. The RTM or system board may be damaged if the incorrect RTM is used.

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Some I/O ports are supported on both the front board and the RTM, including Keyboard, Mouse, VGA, and USB. These I/O ports can be connected either via the front or rear modules but DO NOT access these ports on both front and rear simultaneously.

3.8 Main Board Installation

Follow the instructions below to install the cPCI-6810/6820 main board to its CompactPCI chassis.

1. Refer to the relevant chassis user manual for pre-preparation of the chassis before installing the mainboard. Users need to assign a slot to the board. Be sure to select the correct slot (system or peripheral) depending on the operation purpose of the board. The system power may now be powered on.
2. Remove the blank face panel from the slot.
3. Align the top and bottom edges of the board with the card guides on the chassis then slide the board into the chassis until resistance is felt. If the system power is on, the blue LED (hot-swap status) should light.
4. Move the upper and lower ejectors in an inward direction simultaneously. Note that some resistance will be felt while inserting the board. If this resistance is unusually high, check that no pins are bent on the backplane and that the board's connector pins are properly aligned with the connectors on the backplane.
5. Verify that the board is seated properly. With the board in place and the blue LED on, wait for the blue LED to go out before proceeding to the next step.
6. Secure the two screws hidden behind the upper and lower ejector; connect the proper cables to the board.

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4 Device Driver Installation

To install the drivers for the cPCI-8610/8620, refer to the installation information in this chapter. Basic information is presented in this section, however, for more detailed installation information for non-Windows Operating Systems, refer to the extensive explanation inside the ADLINK CD. The drivers are located in the following directories of the CD-ROM:

VGA/AGP driver	\CHIPDRV\VGA\69000
LAN driver	\CHIPDRV\LAN\82546EB

As the Bus-mastering IDE drivers are automatically installed by most Windows based operating systems, it will not be described.

Since Windows NT is a non-Plug and Play OS, here are some useful tips for installing Windows NT drivers:

1. Install the LAN driver before installing any service pack.
2. Install the VGA/AGP driver after installing the service pack. Make sure your service pack supports AGP. Service pack 6 or higher is recommended.

If Windows NT boots with a warning message, check the Event Viewer to view the source generating the message. If an unusual event has occurred and it cannot be solved, re-install Windows NT service pack, then install the drivers in a different sequence.

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4.1 VGA Drivers Installation

This section describes the VGA driver installation for the onboard VGA controller **M69000**. The relative drivers are located in **X:\CHIPDRV\VGA\69000** directory of the ADLINK CD: where **X:** is the location of the CD-ROM drive. The VGA drivers for Windows 98/95, Windows NT, and Windows 2000 are included.

Driver Installation on Windows NT

Windows NT may install the standard VGA driver. It is recommend that the most recently updated driver be installed manually, which is shipped with the ADLINK CD to ensure compatibility. After installing Windows NT, follow the instructions below to update to the newer driver.

1. From the **Control Panel**, double-click the **Display** icon.
2. Click the **Settings** tab, then **Display Type…**, and click **Change…**
3. Insert the ADLINK CD and click **Have Disk**.
4. Browse for the **M69000 driver** in the following path: **X:\CHIPDRV\VGA\ 69000\NT40**, highlight **oemsetup.inf**, click **OPEN**, then **OK**.
5. A window will appear and display chips Video Accelerator (65545/48/50/54/55 68554 69000), click **OK**, then **Yes** to continue.
6. An Installation Driver window will appear indicating a successful installation, Click **OK** to continue.
7. Click **Close**
8. Click **Close**, then restart the computer to activate the new driver.

Note: If the driver does not work after installing the VGA/ AGP drivers, this may be caused by failing to install the NT service pack in advance. To fix this problem, install NT service pack 4 or higher to enable AGP capability.

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Driver Installation on Red Hat Linux 7.3

The standard Linux installation procedure will install the graphic driver for the VGA chip. However, under Red Hat Linux 7.3 or higher, the standard VGA driver is not fully compatible with the C&T69000 VGA chip. The installation of Red Hat Linux 7.3 may hang after entering X-Windows.

To fix this compatibility issue, two configuration files must be modified under text mode. Both files are locate in the **/etc/X11** directory.

XF86Config

```
. . . . . .
Identifier"Chips & Technologies CT69000"
VendorName"CHIPS 69000 Super VGA"
# Option "noaccel"     <- unmark this item, remove '#'
# Option "no_bitblt"   <- unmark this item, remove '#'
# Option …….
# Option …….
```

XF86Config-4

```
. . . . . .
Section"Device"
Identifier"Chips & Technologies CT69000"
Driver"chips"
VendorName"Chips & Technologies CT69000"
BoardName"Chips & Technologies CT69000"
Option "noaccel"      <- add this item
Option "no_bitblt"    <- add this item
```

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4.2 LAN Drivers Installation

This chapter describes the LAN driver installation for the onboard Ethernet controller **Intel 82546EB**. All associated drivers are located under the following ADLINK CD directory: **X:\CHIPDRV\LAN\82546EB**, where **X:** is the location of the CD-ROM drive.

Software and Drivers Support

The 82546EB drivers support the following OS or platforms:

- Windows 2000, Windows XP

All of the above drivers are included on the ADLINK CD. In the following section, we will describe the driver installation for Windows 2000 and Windows XP.

Driver Installation on Windows 2000/XP

Windows 2000 will attempt to install a standard LAN driver automatically. To guarantee compatibility, manually install the most updated LAN driver, which is stored on the ADLINK CD. After installing Windows 2000, follow the instructions below to update to the most recently updated driver.

1. Run **pro2kxpm.exe** in **x:\chipdrv\LAN\82546EB\win2kxp** to extract the files needed for the installation. Files will be extracted to **c:\IntelPRO**.
2. Click **Install Now** to install driver.
3. Click **Finish**.

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Appendix

Appendix A - IPMI Functions List

The following table lists the IPMI V1.0 functions that are supported by the cPCI-6810 and cPCI-6820.

IPMI V1.0 Function List	CPCI-6820 CPCI-6810
IPM Device "Global" Commands	
Get Device ID	√
Cold Reset	√
Warm Reset	√
Get Self Test Results	√
Set ACPI Power State	√
Get ACPI Power State	√
Get Device GUID	√
BMC Watchdog Timer Commands	
Reset Watchdog Timer	√
Set Watchdog Timer	√
Get Watchdog Timer	√
BMC Device and Messaging Commands	
Set BMC Global Enables	√
Get BMC Global Enables	√
Clear Message Flags	√
Get Message Flags	√
Enable Message Channel Receive	√
Get Message	√
Send Message	√
Read Event Message Buffer	√

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IPMI V1.0 Function List	CPCI-6820 CPCI-6810
Get BT Interface Capabilities	√
Get System GUID	√
Chassis Device Commands	
Get Chassis Status	√
Chassis Control	√
Get POH Counter	√
Event Commands	
Set Event Receiver	√
Get Event Receiver	√
Platform Event (a.k.a. “Event Message”)	v
PEF and Alerting Commands	
Sensor Device Commands	
Get Device SDR Info	√
Get Device SDR	√
Reserve Device SDR Repository	√
Get Sensor Reading Factors	√
Set Sensor Hysteresis	(2)
Get Sensor Hysteresis	√
Set Sensor Threshold	(2)
Get Sensor Threshold	√
Set Sensor Event Enable	(2)
Get Sensor Event Enable	√
Re-arm Sensor Events	(2)
Get Sensor Reading	√
Set Sensor Type	(2)
Get Sensor Type	√
FRU Device Commands	
Get FRU Inventory Area Info	√(1)

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IPMI V1.0 Function List	CPCI-6820 CPCI-6810
Read FRU Data	√(1)
Write FRU Data	√(1)
SDR Device Commands	
Get SDR Repository Info	√
Get SDR Repository Allocation Info	√
Reserve SDR Repository	√
Get SDR	√
Add SDR	√
Partial Add SDR	√
Delete SDR	√
Clear SDR Repository	√
Get SDR Repository Time	√
Set SDR Repository Time	√
Enter SDR Repository Update Mode	√
Exit SDR Repository Update Mode	√
Run Initialization Agent	√
SEL Device Commands	
Get SEL Info	√(1)
Get SEL Allocation Info	√(1)
Reserve SEL	√(1)
Get SEL Entry	√(1)
Add SEL Entry	√(1)
Partial Add SEL Entry	√(1)
Delete SEL Entry	(3)
Clear SEL	√(1)
Get SEL Time	√(1)
Set SEL Time	√(1)

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Note: (1) Supported on PCB rev.A3 or higher.
(2) The SDR information are read-only.
(3) The SEL storage is not supported random access.

Not available means that an additional onboard EEPROM is required to store information. This requires a modification of the A3 version board - the A2 version board does not have the EEPROM.

IPMI Address Map

The IPMI address of the SBC is defined by GA pins which is relative to the physical slot the SBC is installed on. The following table shows the relationship between the IPMI address and the Slot number SBC installed.

Address (Hex)	CompactPCI Slot
B0	Peripheral Slot1
B2	Peripheral Slot2
B4	Peripheral Slot3
B6	Peripheral Slot4
B8	Peripheral Slot5
BA	Peripheral Slot6
BC	Peripheral Slot7

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Appendix B - WatchDog Timer Programming Guide

The Watchdog Timer (WDT) can monitor the system's status. Once a value is given to the WDT, the timer will begin to count down. If the system becomes idle or hangs, the system will reboot itself when the timer times out.

The Watch Dog timer includes an 8-bit timer clocked by a 1-minute internal clock that is derived from the battery-backed 32.768KHz crystal clock generator. The timer is loaded with the WATCHDOG Time-Out data value written in the WDTO register and counts down to zero. This 8-bit data enables time-out values between 1 and 255 minutes to be programmed (00h is an invalid data value).

The following events can trigger the WATCHDOG by reloading the timer:

- Keyboard interrupt
- Mouse interrupt
- Serial Port 1 interrupt
- Serial Port 2 interrupt
- Software writing to control register

All control registers are accessed through the following I/O ports.

I/O mapped Port	
Index port	Data Port
2EH	2FH

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WDT Setup Instructions

1. Set pin 55 of PC87417 as Watch Dog Timer output pin

- Set Bit 7 of SIOCF2 Register (Index: 22H) to 1, for example:
  - o 2E 22
  - o 2F 80

2. Set Logic Device to System Wake-Up Control (SWC)

- Set Logic Device Number Register (Index: 07H) to 04H, for example:
  - o 2E 07
  - o 2F 04

3. Enable Logic Device Control

- Set Logic Device Control Register (Index: 30H) to 01H, for example:
  - o 2E 30
  - o 2F 01

4. Get I/O Base Address (MSB) of SWC

- Get SWC base address MSB from 60H, for example:
  - o 2E 60
  - i 2F
  - 08 -> BIOS default value

5. Get I/O Base Address (LSB) of SWC

- Get SWC base address MSB from 61H, for example:
  - o 2E 61
  - i 2F
  - 40 -> BIOS default value

(The I/O Base Address of SWC BIOS set is 840H)

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6. Select Bank 3 for Watch Dog Timer from SWC base address.

- Set Bit 1-0 of BANKSEL Register (I/O Base: 840H, Offset: 0FH) to 11, for example:
  - o 84F 03

7. Set the count down value for Watch Dog timer.

-> Set count down value to WDTO Register (I/O Base: 840H, Offset: 11H)

00000000: Reserved

00000001: 1 minute

00000010: 2 minutes

:

:

11111111: 255 minutes

For example:

- o 851 03?3 minutes

8. Enable trigger event to re-start new counter value

- Set WDCFG Register (I/O Base: 840H, Offset: 12H) to 82H, for example:
  - o 852 82

9. Enable Watch Dog Timer function

- Set Bit 0 of WDCTL Register (I/O Base: 840H, Offset: 10H) to 1, for example:
  - o 850 01

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Appendix C - Power Consumption

Hardware Environment:

- Single or Dual LV P-III 933M or 1GHz
- Memory: 1GB (512MB x 2) or 1.5GB (512MBx3)
- HDD: FUJITSU MHR2040AT 40GB installed on RTM (Max. current requirement is 0.55A @ +5V
- CompactFlash: PQI 64MB Flash Card
- PMC card: ADLINK PMC-8615 Gigabit Ethernet Card
- PMC VGA card: ADLINK PMC-8217V (only available with CRUX-SP)

Software Environment:

- OS: Windows 2000 Professional
- KPOWER.EXE
- HCT 9.5
- Burn-In Test

Test Setup:

- SBC power consumption data is measured with the RTM installed, if not specified.
- Single-CPU SBC is tested with PMC-8217V and PMC-8615 installed, dual-CPU SBC is tested with PMC-8615 installed.
- The value with HDD is tested with KPOWER, HCT and BrunIn in Win2000. The typical and maximum values are shown.
- The value without HDD is tested under DOS without running anything. The typical and maximum values are shown.

The power requirements of cPCI-6820 series products are shown in the following table:

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Typical Current and Maximum Current	+5V (+/-5%)	+3.3V (+/-5%)	+12V (+/-5%)	-12V (+/-5%)
cPCI-6810A/P9	2.28A 3.73A	4.10A 14.636A	3mA 8mA	0mA 0mA
cPCI-6810A/P9 with HDD	2.94A 3.73A+HDD	4.82A 14.636A	3mA 8mA	0mA 0mA
cPCI-6810A/1G	2.50A 3.88A	4.10A 14.636A	3mA 8mA	0mA 0mA
cPCI-6810A/1G (Without PMC, VGA cards, and RTM)	1.44A 3.73A	3.64A 14.636A	3mA 8mA	0mA 0mA
cPCI-6810/1G with HDD	3.16A 3.88A+HDD	4.76A 14.636A	3mA 8mA	0mA 0mA
cPCI-6820A/P9	2.66A 3.73A	4.36A 16.526A	3mA 8mA	0mA 0mA
cPCI-6820A/P9 with HDD	3.56A 3.73A+HDD	5.36A 16.526A	3mA 8mA	0mA 0mA
cPCI-6820B/1G	3.38A 3.88A	4.98A 16.526A	3mA 8mA	0mA 0mA
cPCI-6820B/1G with HDD	4.34A 3.88A+HDD	5.92A 16.526A	3mA 8mA	0mA 0mA
cPCI-6820B/1G (Without PMC card)	3.79A 3.88A+HDD	5.26A 16.526A	3mA 8mA	0mA 0mA
cPCI-6820A /1G	TBD 3.88A	TBD 18.416A	TBD 8mA	0mA 0mA

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Appendix D - SMBus Address Map

The SMBus address Map on the cPCI-6820 products are as follows:

Address (Hex)	Function	Device
0x A0	SO-DIMM ID(1)	SO-DIMM
0x 5C	Hardware Monitor	ADM1026
0x AC	SEL data storage (IPMI)	24C64
0x AE	FRU data storage (IPMI)	24C64
0x AA	BIOS CMOS storage	24C02

ID of SO-DIMM 1-4 are selected by two GPIO pins from CSB5 SO-DIMM selection table:

GPIO13	GPIO12	DIMM
0	0	1
0	1	2
1	0	3
1	1	4

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Warranty Policy

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1. Before using ADLINK's products please read the user manual and follow the instructions exactly. When sending in damaged products for repair, please attach an RMA application form which can be downloaded from: http://rma.adlinktech.com/policy/.
2. All ADLINK products come with a two-year guarantee:
   - The warranty period starts from the product's shipment date from ADLINK's factory.
   - Peripherals and third-party products not manufactured by ADLINK will be covered by the original manufacturers' warranty.
   - For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ADLINK is not responsible for loss of data.
   - Please ensure the use of properly licensed software with our systems. ADLINK does not condone the use of pirated software and will not service systems using such software. ADLINK will not be held legally responsible for products shipped with unlicensed software installed by the user.
   - For general repairs, please do not include peripheral accessories. If peripherals need to be included, be certain to specify which items you sent on the RMA Request & Confirmation Form. ADLINK is not responsible for items not listed on the RMA Request & Confirmation Form.

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3. Our repair service is not covered by ADLINK's two-year guarantee in the following situations:
   - Damage caused by not following instructions in the user's manual.
   - Damage caused by carelessness on the user's part during product transportation.
   - Damage caused by fire, earthquakes, floods, lightening, pollution, other acts of God, and/or incorrect usage of voltage transformers.
   - Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).
   - Damage caused by leakage of battery fluid during or after change of batteries by customer/user.
   - Damage from improper repair by unauthorized technicians.
   - Products with altered and/or damaged serial numbers are not entitled to our service.
   - Other categories not protected under our warranty.
4. Customers are responsible for shipping costs to transport damaged products to our company or sales office.
5. To ensure the speed and quality of product repair, please download an RMA application form from our company website: http://rma.adlinktech.com/policy. Damaged products with attached RMA forms receive priority.

If you have any further questions, please email our FAE staff: service@adlinktech.com.

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