cPCI-6910 Series

6U CompactPCI® Single Board Computer with
Dual-Core Intel® Xeon® Processor LV/ULV

User's Manual

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Part No: 50-15056-1030



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Revision History

Version	Release Date	Revision(s)
2.00	2006/12/29	First release.
2.01	2007/04/04	Added power consumption data.
		Updated J1 to J5 pin assignment.
		Added RJ-45 COM pin-out.
		Updated SW1 function description.
		Modified various installations in Chapter 5: Getting Started.
		Added CF adapter information (supports CF by adapter design on front board).
2.02	2007/07/19	Modified cPCI-6910 with cPCI-R6910 Block Diagram.
		Updated SWZ2 function description.
		Updated Onboard Devices descriptions.
		Updated IPMI Sensor Lists.
		Updated Firmware Revision History.
		Added Switch information for RTM configuration.
2.03	2007/08/08	Added new cPCI-6910 Configuration options.
		Added CPU specifications.
		Added power consumption specifications under idle DOS, idle Linux®, full-load WIndows® XP and idle Windows® XP environments.
		Revised Firmware revision history information.
		Added Voltage, Amperage and wattage units on power consumption tables.
		Updated switch function information

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Version	Release Date	Revision(s)
2.04	2008/02/25	Revised CompactPCI® J3 Pin Assignments
		Revised Oem Command Summary Table
		Revised BMR-AVR-cPCI Supported Command List
		Revised Onboard Device BIOS descriptions
		Revised USB 2.0 Controller descriptions
		Updated Block Diagram
		Revised CompactPCI J2 Pin Assignments
		Revised RJ-45 Connector Pin Assignments
		Revised OemShowRevision Table
2.05	2008/06/06	Correct LAN status table
		Correct address

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Preface

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Using this Manual

Audience and Scope

The cPCI-6910 Series User's Manual is intended for hardware technicians and systems operators with knowledge of installing, configuring and operating industrial grade single board computers.

Manual Organization

This manual is organized as follows:

Preface: Presents important copyright notifications, disclaimers, trademarks, and associated information on the proper understanding and usage of this document and its associated product(s).

Chapter 1, Introduction: Introduces the cPCI-6910 Series, its features, block diagrams, and package contents.

Chapter 2, Specifications: Presents information on cPCI-6910 Series blades, Rear Transition Modules, I/O connectivity and power consumption.

Chapter 3, Functional Description: Provides detailed information on supported processors, chipsets, memory, high speed I/O, blade features and various functions.

Chapter 4, Jumpers and Connectors: Provides detailed information on board layout, connector pin assignments, switches, jumpers, etc.

Chapter 5, Getting Started: Describes installation of the blade and rear transition module.

Chapter 6, Driver Installation: Explains how to install drivers and the operating system environment for the cPCI-6910 Series.

Chapter 7, Watchdog Timer: This section explains the operation of the cPCI-6910 Series watchdog timer (WDT).

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Chapter 8, BIOS Setup: Describes the setup utility program for specifying cPCI-6910 Series system configurations and settings.

Chapter 9, IPMI Interface: Describes OEM extension IPMI commands' usages which are not listed in the associated IPMI specification documentation.

Appendix, Serial Console: Provides a detailed explanation of how to setup and use a serial console for remote access to POST messages and system commands.

Important Safety Instructions: Presents saftety instructions all users must follow for the proper setup, installation and usage of equipment and/or software.

Warranty Information: Presents important warranty information for users/manufacturers rights and responsibilities regarding ADLINK products and services.

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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly..



Additional information, aids, and tips that help users perform tasks.



Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.



Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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Related Documentation

The following list of documents may be used as reference materials to support the installation, configuraiton and/or operation of the ADLINK cPCI-6910 Series.

Document Title	Publication Number and Date	Source
Intelligent Platform Management Interface Specification v1.5	Document Revision 1.1 February 20, 2002	Intel® Corp. http://www.intel.com/design/servers/ipmi/license_ipmi.htm
PICMG® 2.9 D1.0 CompactPCI® System Management Specification	January 21, 2000	
Intelligent Platform Management Bus Communications Protocol Specification v0.9	Document Revision 0.15 June 24, 1997	Intel® Corp. http://www.intel.com/design/servers/ipmi/license_ipmi.htm

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1 Introduction

The cPCI-6910 Series is a state-of-the-art single board computer in a 6U single slot (4HP) CompactPCI form factor featuring the fastest and energy-efficient Dual-Core Intel® Xeon® Processor LV 2.0 GHz or ULV 1.66 GHz with 2 MB L2 cache. Packed with a powerful 667 MHz FSB, the cPCI-6910 combined the server-grade Intel® E7520 and Intel® 6300ESB chipset with I/O versatility and cutting-edge storage solutions. The cPCI-6910 is intended for demanding and multitasking military, telecom, data, or Internet applications.

Manufactured using the 65 nm process technology, the Dual-Core Intel® Xeon® Processor LV/ULV integrates two cores in one physical package providing twice the performance of previous single-core Intel® Xeon® processors. These processors are developed with an intelligent power management that significantly reduces power consumption for maximum energy efficiency.

The cPCI-6910 Series supports up to 2 GB of system memory using DDR2 400 MHz registered SDRAM with ECC. Promoting seamless network connectivity, the SBC comes with two Intel® 82571EB controllers that support four gigabit Ethernet ports that utilize the rapid PCI Express® bus. For peripheral connections, the cPCI-6910 features four USB 2.0, one PMC slot sitting on a 64-bit/66 MHz bus, two serial ports, dual-channel UltraATA 100, two removable Serial ATA connectors, one VGA port, and a PS2 keyboard/mouse combo port.

Extending the cPCI-6910 I/O capability are two optional rear transition modules (RTM): cPCI-R6910 and cPCI-R6911. The cPCI-R6910 supports a Serial Attached SCSI (SAS) connector for advanced storage. The cPCI-R6911 RTM comes with a 68-pin SCSI connector for additional storage with RAID 1 capability for superior data protection.

For UltraATA 100 storage, the cPCI-6910 implements the primary IDE channel onboard. The rear transition module provides the secondary IDE channel via the CF slot (cPCI-R6910) and/or a 40-pin IDE connector (cPCI-R6911).

The CompactPCI bus is based on the PLX PCI-6540 universal PCI-X-to-PCI-X bridge chip that provides either a transparent or

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non-transparent PCI interface. cPCI-6910 can be used as a system slot or peripheral slot and may also be a server blade for stand-alone operation on any non-system slot with no PCI bus. The cPCI-6910, when deployed on peripheral or non-PCI bus slot, supports hot-swap functionality for superior performance and shorter MTTR.

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1.1 Features

- Supports one Dual-Core Intel® Xeon® Processor LV/ULV with up to 2.0 GHz core speeds, 2 MB L2 cache
- Up to 667 MHz Front Side Bus
- Server-grade Intel® E7520 and Intel® 6300ESB chipset
- Up to 2 GB system memory using registered DDR2 400 MHz SDRAM with ECC (soldered)
- 64-bit/66MHz CompactPCI interface based on PCI specifications and supports universal application as stand-alone server blade, system slot SBC, or peripheral SBC
- Four gigabit Ethernet ports on PCI Express® bus
- PMC slot with 64-bit/66 MHz bus
- Up to four USB 2.0 ports (two in front and two on rear panel)
- Multiple storage interfaces, including:
  - Serial ATA
  - UltraATA 100 (40-pin or 44-pin IDE)
  - CompactFlash
  - Serial Attached SCSI (SAS) on cPCI-R6910 RTM
  - Ultra-320 SCSI with RAID 1 support on cPCI-R6911 RTM
- PICMG 2.0, 2.1, 2.9, 2.16 compliant, IPMI v.1.5

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1.2 Block Diagrams

cPCI-6910 with cPCI-R6910 Block Diagram

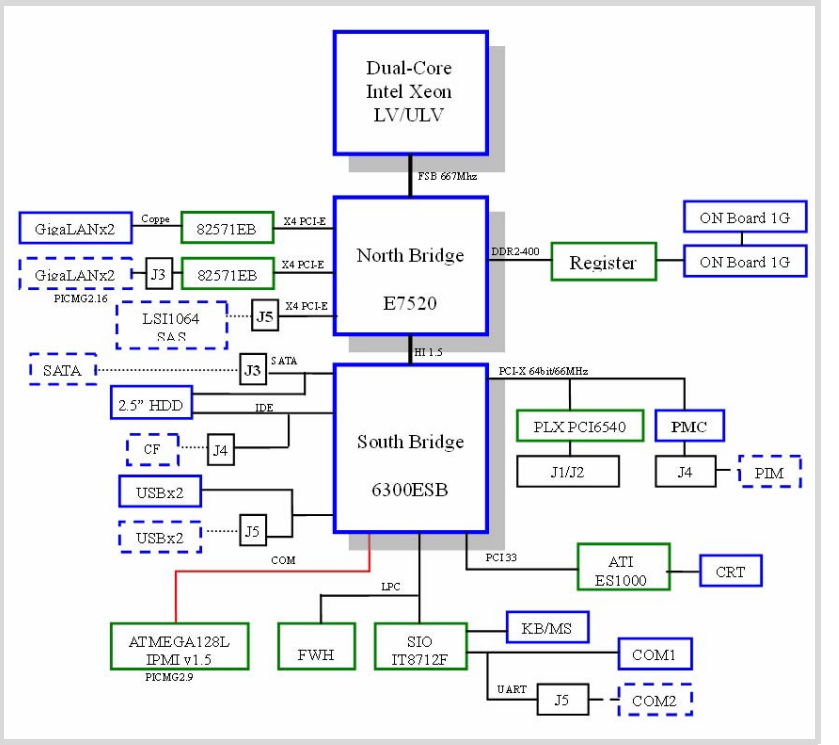


Figure 1-1: cPCI-6910 with cPCI-R6910 Block Diagram

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cPCI-R6911 Block Diagram

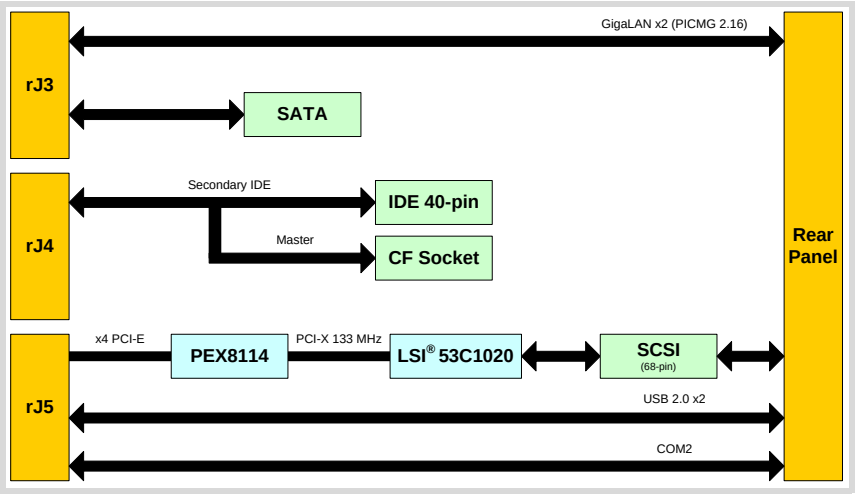


Figure 1-2: cPCI-R6911 Block Diagram

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1.3 Product List

The cPCI-6910 Series SBS and supported rear transition modules come in the following configurations.

cPCI-6910 Configurations

- cPCI-6910/DCX20/M1G

Dual-Core Intel® Xeon® Processor LV 2.0 GHz with 1 GB soldered memory. Ports: COM1, PS/2, VGA, 2 x USB, 2 x GbE, PMC. Storage: IDE/SATA/CF (optional)

- cPCI-6910/DCX20/M2G

Dual-Core Intel® Xeon® Processor LV 2.0 GHz with 2 GB soldered memory. Ports: COM1, PS/2, VGA, 2 x USB, 2 x GbE, PMC. Storage: IDE/SATA/CF (optional)

- cPCI-6910/DCX16/M1G

Dual-Core Intel® Xeon® Processor ULV 1.66 GHz with 1 GB soldered memory. Ports: COM1, PS/2, VGA, 2 x USB, 2 x GbE, PMC. Storage: IDE/SATA/CF (optional)

- cPCI-6910/DCX16/M2G

Dual-Core Intel® Xeon® Processor ULV 1.66 GHz with 2 GB soldered memory. Ports: COM1, PS/2, VGA, 2 x USB, 2 x GbE, PMC. Storage: IDE/SATA/CF (optional)

- cPCI-6910/DXL16/M1G

Dual-Core Intel® Xeon® Processor LV 1.66 GHz with 1 GB soldered memory. Ports: COM1, PS/2, VGA, 2 x USB, 2 x GbE, PMC. Storage: IDE/SATA/CF (optional)

- cPCI-6910/DXL16/M2G

Dual-Core Intel® Xeon® Processor LV 1.66 GHz with 2 GB soldered memory. Ports: COM1, PS/2, VGA, 2 x USB, 2 x GbE, PMC. Storage: IDE/SATA/CF (optional)

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Rear Transition Modules

- cPCI-R6910

  2 x GbE, 2 x USB, COM2, CF card slot, and SAS/SATA connector

- cPCI-R6911

  2 x GbE, 2 x USB, COM2, SATA, IDE, CF card slot, and SCSI connector

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1.4 Package Contents

Before unpacking, check the shipping carton for any damage. If the shipping carton and/or contents are damaged, inform your dealer immediately. Retain the shipping carton and packing materials for inspection. Obtain authorization from your dealer before returning any product to ADLINK.

Check if the following items are included in the package.

CPU Module

- cPCI-6910 single board computer
- 2.5" SATA HDD accessory pack (including one DB-6910SAT removable SATA socket adapter and screws)
- 2.5" IDE HDD accessory pack (including one DB-6910IDE removable IDE socket adapter and screws)
- Heatsink kit
- RJ-45-DB9 cable
- Y-cable for PS/2 combo port
- ADLINK All-in-One driver CD
- User's manual

Rear Transition Module (RTM)

- cPCI-R6910/cPCI-R6911 RTM
- 2.5” SATA HDD accessory pack including one DB-R6910SAT and screws (cPCI-R6910 only)
- 2.5” SAS HDD accessory pack including one DB-R6910SAS and screws (cPCI-R6910 only)
- SATA HDD signal and power cables (cPCI-R6911 only)
- Ultra-320 SCSI cable (cPCI-R6911 only)

Optional Components

- CompactFlash® adapter accessory pack, including DB-6910CF removable CF socket adapter and screws

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NOTES: CPU, memory, and HDD specifications may vary depending on the selected SBC configuration.

The HDD accessory pack is not available when the 2.5" HDD is pre-installed.

The heatsink kit is not included when the CPU is pre-installed.

The contents of non-standard cPCI-6910 configurations may vary depending on customer requirements.

CAUTION: This product must be protected from static discharge and physical shock. Never remove any of the components except at a static-free workstation. Use the anti-static bag shipped with the product when putting the board on a surface. Wear an anti-static wrist strap properly grounded on one of the system's ESD ground jacks when installing or servicing system components.

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2 Specifications

This section tells you the specifications of the SBC and supported rear transition modules.

2.1 cPCI-6910 SBC Specifications

CompactPCI® Standards	• PICMG® 2.0 CompactPCI® Rev. 3.0 • PICMG® 2.1 CompactPCI® hot-swap specification Rev. 2.0 • PICMG® 2.9 System Management Bus Rev. 1.0 (IPMI v1.5) • PICMG® 2.16 Packet Switching Backplane Rev.1.0
Form Factor	• Standard 6U CompactPCI® Board size: 233.35 mm x 160 mm • One slot width (4HP, 20.32 mm)
CPU	• Single processor on 478-pin micro FCPGA socket • Dual-Core Intel® Xeon® Processor LV, 2.0 GHz, Dual-Core Intel® Xeon® Processor LV, 1.66 GHz or Dual-Core Intel® Xeon® Processor ULV, 1.66 GHz set in 65 nm process technology • 2 MB on die L2 cache, 677 MHz FSB
Chipset	• Intel® E7520 Memory Controller Hub (GMCH) • Intel® 6300ESB I/O Hub
Host Memory	• 2 GB or 1 GB soldered system memory • DDR2 400 MHz registered SDRAM with ECC
CompactPCI® Bus	• 64-bit/66 MHz CompactPCI® Bus • PLX PCI-6540 64-bit/66 MHz PCI-X to PCI-X Bridge
Graphics	• ATI ES1000 controller on PCI 32-bit/33 MHz bus • Up to 250 MHz graphics memory • 2D graphics accelerator
Gigabit Ethernet	• Up to four gigabit Ethernet ports, two in front and 2 on rear panel • Two Intel® 82546EB Ethernet controller, based on PCI Express® x4 bus connected to J3 for Packet Switched Backplane (PSB)

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IDE	• Dual-channel IDE • 44-pin primary IDE connector for onboard HDD and secondary connector on rear via J4 connector • Bus Master IDE controller supports two UltraATA 100/66/33 devices
BIOS[1]	• Award-Phoenix with 4 MB Flash ROM • BIOS write protection feature • Boot from USB storage devices including USB-Floppy, USB-ZIP, USB-CD-ROM, and USB-HDD • Supports Desktop Management Interface (DMI) • Supports Enhanced Intel SpeedStep® technology • Supports optional OEM BIOS features
IPMI Interface	• Supports PICMG® 2.9 secondary system managing bus • Implements IPMI functions defined by IPMI Specification v1.5 • ATmega128L-8AU Baseboard Management Controller (BMC) with 128 KB programmable In-System Flash, 4 KB EEPROM, and 4 KB internal SDRAM
Faceplate I/O Ports	• COM1 (RS-232) • PS/2 keyboard and mouse combo port • VGA (DB-9) • 2 x USB 2.0 • 2 x gigabit Ethernet ports (RJ-45)
Onboard Peripherals[2]	• 44-pin IDE connector • Serial ATA connector • CompactFlash® connector
OS Compatibility	• Windows® 2000 • Windows® XP • Windows® Server 2003 • Red Hat Fedora Core 6 • Other OS supported upon request

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Environment	• Operating temperature[3]**:** Intel® Xeon® LV CPU: -10 °C to 50 °C Intel® Xeon® ULV CPU: -10 °C to 70 °C • Storage temperature: -40 °C to 85 °C • Humidity: 5% to 95% non-condensing • Shock: 15G peak-to-peak, 11ms duration, non-operation • Vibration[4]: Non-operation: 1.88 Grms, 5 Hz to 500 Hz, each axis Operation: 0.5 Grms, 5 Hz to 500 Hz, each axis
Safety Certificates and Tests	CE/FCC Class A

1. Due to BIOS segment limitations, enabling the remote console function may occupy the same memory space as other ROM mapping add-on or boot-up devices including Pre-boot Agent of Ethernet Boot ROM, SCSI Boot ROM, or add-on EIDE Boot ROM. It is recommended that you enable only one ROM-mapping add-on or boot-up device when enabling the remote console function.

2. The IDE HDD/Serial ATA HDD/CompactFlash card connector comes in an adapter design. These are removable and should not be used/connected simultaneously. The 2.5” HDD space is reserved.

3. ADLINK-certified thermal design. The thermal performance is dependent on the chassis cooling design. Forced airflow with 30 CFM is required. Temperature limit of optional mass storage devices may affect the thermal specification.

4. The HDD limits the operational vibration. When application requires higher definition for anti-vibration, it is recommended that you use a flash disk.

Specifications are subject to change without prior notice.

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2.2 cPCI-R6910/cPCI-R6911 RTM Specifications

Form Factor	• Standard 6U CompactPCI® rear I/O • Board size: 233.35 mm x 80 mm • One slot width (4HP, 20.32 mm) • CompactPCI® connectors: with rJ3, rJ4 and rJ5 connectors
Faceplate I/O Connectors	• COM2 (RS-232) • 2 x gigabit Ethernet ports • 2 x USB 2.0 ports • 68-pin SCSI socket *(cPCI-R6911 only)*
Onboard Peripherals	• CompactFlash® Type II card slot • Serial Attached SCSI connector[1] *(cPCI-R6910 only)* • Serial ATA connector *(cPCI-R6910 only)* • 40-pin IDE connector[2] *(cPCI-R6911 only)* • 68-pin SCSI connector *(cPCI-R6911 only)*
SCSI *(cPCI-R6911 only)*	• LSI® Logic LSI53C1020 PCI-X Ultra320 SCSI Controller Integrated RAID™ on PCI-X 64-bit/133 MHz bus • 320 MB per second data transfer rate • Supports RAID™ 0 (striping) and RAID™ 1/1E (mirroring)

1. The Serial Attached SCSI and Serial ATA HDD connectors come in a removable adapter design. These should not be used/connected simultaneously. The 2.5” HDD space is reserved.

2. When using the CompactFlash card slot, the 40-pin IDE connector supports only one IDE device.

Specifications are subject to change without prior notice.

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2.3 I/O Connectivity Table

I/O	cPCI-6910		cPCI-R6910 RTM		cPCI-R6911 RTM	
	Faceplate	Onboard	Faceplate	Onboard	Faceplate	Onboard
Serial Port	Y	--	Y(J5)	--	Y(J5)	--
USB	Yx2	--	Y(J5) x2	--	Y(J5) x2	--
Gigabit Ethernet	Yx2	--	Y(J3) x2	--	Y(J3) x2	--
SCSI				--	Y(J3)	Y(J3)
PS2 Keyboard/Mouse	Y	--	--	--	--	--
VGA	Y	--	--	--	--	--
IDE	--	Y (44-pin)*	--	--	--	Y(J4, 40-pin)
CompactFlash®	--	Y*	--	Y	--	Y
SATA	--	Y*	--	Y(J5)*	--	Y(J5)
SAS	--	--	Y(J5)*	--	--	--
PMC	Y	--	--	--	--	--
General Purpose LED	Y	--	--	--	--	--
Reset button	Y	--	--	--	--	--

** Removable adapter design*

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2.4 Power Consumption

This section provides information on the power consumption of cPCI-6910 when using Dual-Core Intel® Xeon® ULV Processor at 1.66 GHz and a Dual-Core Intel® Xeon® LV Processor at 2.0 GHz. The cPCI-6910 was tested under the following environment:

Operating system	DOS, Linux®, Windows® XP
System memory	2 GB DDR2-400 registered SDRAM with ECC
Storage	Seagate Momentus 5400 X2 SATA 1.5 Gb/s 80 GB HDD
Program	Intel® Sossaman Maximum Power Program Rev. 2.0
Backplane	ADLINK cBP-6105R Rev.A2
Power Supply	Seventeam ST-350HLP 350W

The following tables show the cPCI power consumption during idle mode (no application is running) and full loading (100% CPU usage).

Idle mode under DOS

Voltage (V)	CPU					
	ULV 1.66 GHz		LV 2.0 GHz		LV 1.66 GHz	
	Current (A)	Power (watts)	Current (A)	Power (watts)	Current (A)	Power (watts)
5	4.5	22.5	5.7	28.5	5.1	25.5
3.3	1.5	5.0	1.5	5.0	1.49	4.92
Total		27.5		33.5		30.4

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Idle mode under Linux®

Voltage (V)	CPU					
	ULV 1.66 GHz		LV 2.0 GHz		LV 1.66 GHz	
	Current (A)	Power (watts)	Current (A)	Power (watts)	Current (A)	Power (watts)
5	3.9	19.5	4.4	22.0	4.2	2.1
3.3	1.6	5.3	1.7	5.6	1.6	5.3
Total		24.8		27.6		26.3

Full-load CPU mode under Windows® XP

Voltage (V)	CPU					
	ULV 1.66 GHz		LV 2.0 GHz		LV 1.66 GHz	
	Current (A)	Power (watts)	Current (A)	Power (watts)	Current (A)	Power (watts)
5	6.9	34.5	8.7	43.5	7.6	38
3.3	1.5	5.0	1.55	5.0	1.55	5.1
Total		39.5		48.5		43.1

Idle mode under Windows® XP

Voltage (V)	CPU					
	ULV 1.66 GHz		LV 2.0 GHz		LV 1.66 GHz	
	Current (A)	Power (watts)	Current (A)	Power (watts)	Current (A)	Power (watts)
5	3.9	19.5	4.1	20.5	4.2	21.0
3.3	1.5	5.0	1.6	5.3	1.5	5.0
Total		24.5		25.8		26.0

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3 Functional Description

The following sections describe the cPCI-6910 features and functions.

3.1 Processor

The cPCI-6910 supports a Dual-Core Intel® Xeon® processor LV/ULV (2.0 GHz/1.66 GHz) with 2 MB L2 cache in a micro-FCPGA package. The Dual-Core Intel® Xeon® processor LV/ULV is a high-performance, low-power consuming processor with several micro-architectural enhancements over existing Intel processors, including:

- Chip Multi-Processing (CMP)-based architecture (dual-cores on chip)
- Optimized for best MPS/Watt with CMP-enabled software
- Advanced pre-fetching mechanisms
- Advanced power management and throttling mechanisms

3.2 Chipset

The cPCI-6910 incorporates the Intel® E7520 chipset consisting of three PCI Express® x8 channels, Memory Controller Hub, and I/O Controller Hub (Intel® 6300ESB).

The Intel® E7520 comes with a memory controller hub component for embedded platforms. It also provides the processor, DDR2 system memory, hub, and PCI Express® interfaces.

3.3 Memory

The cPCI-6910 comes with a dual-channel DDR2 system memory architecture that supports x72, buffered, registered DDR2 400 MHz SDRAM with ECC. The Intel® E7520 supports 1 GB/512 MB memory with error checking and correcting (ECC) mechanism provided by Chipkill technology on x8 DIMMS to ensure data and memory integrity. The Intel® E7520 memory interface supports the following:

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- Direct connection of two memory channel interfaces with DDR2 400 DIMMs
- Full operational support in single-channel mode on either channel interface. Lock-step support only for dual-channel operation (logically shared address, independent data)
- Stacked or unstacked DIMM support for registered DDR2-400 DIMMs
- 144-bit wide with ECC slot supports x72, registered DDR2 400 DIMMs in 256 MB/512 MB/1 GB package
- Maximum 16 GB support with DDR2 400 up to two stacked DIMMs (1 GB x 4 DRAMs)
- Base DDR2 clock rates of up to 200 MHz
- Data interface double-pumped to 400 MHz
- Up to 3.2 GB/s (DDR2 400) data bandwidth per channel
- S4EC/D4ED (144, 128) x 4, Intel® x4 Signal Device Data Correction (x4 SDDC) ECC in dual-channel mode
- SEC/DED (72, 64) ECC on each channel when Intel® Signal Device Data Correction (SDDC) is disable
- 14-bit address bus
- RASUM fail-over to an on-line spare DIMM device
- Hardware refresh support for 100 MHz operation to facilitate debug frequencies
- Memory mirroring
- ODT (on-die termination) for DDR2 400
- Four-channel DMA controller for embedded applications.

NOTE Refer to the Intel® E7520 Memory Controller Hub (MCH) DMA Application Note. For additional details, contact your local Intel field representative.

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3.4 PCI Express® (High-speed Serial I/O)

- Three x8 port configuration interfaces, with each interface supporting connection to PCI, Ethernet, iSCSI devices (6700PXH, 82571EB Gigabit Ethernet Controller, or I/O processor), or other PCI Express® peripherals
- Each x8 interface is capable of logically dividing into separate x4 interfaces, with half the bandwidth of x8 interface and fully compliant with x4 specifications
- Simultaneous 2.5 Gb/s (each direction, 5 Gb/s per port) maximum theoretical peak bandwidth for every x8 PCI Express interface
- Simultaneous 1.25 Gb/s (each direction, 2.5 Gb/s per port) maximum theoretical peak bandwidth for every x4 PCI Express® interface
- Automatic wake-up and training of PCI Express® ports out of reset
- 32-bit CRC on all transaction layer packets with link-level retry on error (recovery from transient errors without software visible system failure)
- 16-bit CRC on all link message information
- Hardware detection hot-plug support at the PCI Express® link level above and beyond the PCI hot-plug support provided by the 6700PXH or any equivalent bridge

3.5 Hub Interface 1.5

- 266 MB/s Point-to-Point Connection for Intel® 6300ESB with parity protection
- 8-bit wide, 66 MHz base clock, 4X data transfer
- Parallel termination mode for longer trace length
- Upstream hub interface for Intel® E7520 access

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3.6 Intel® 6300ESB I/O Controller Hub (ICH)

The cPCI-6910 features a highly-integrated, multi-functional I/O Controller Hub (ICH) that supports the interface to the PCI bus, and various I/O functions for current and legacy devices. The chipset communicates via a dedicated hub interface (HI-1.5). The Intel® 6300ESB functions and features include:

- Upstream hub interface for Intel® E7520 access
- 2-port Serial ATA controller
- 2-channel Ultra ATA/100 Bus Master IDE controller
- EHCI USB 2.0 host controller and two UHCI USB 1.1 host controller (supporting up to 4 USB ports)
- I/O APIC
- SMBus 2.0 controller
- FWH interface
- LPC interface
- AC'97 2.2 interface
- PCI-X 1.0 interface
- PCI 2.2 interface
- Two serial I/O ports
- 2-stage watchdog timer

The Intel® 6300ESB also comes with the necessary arbitration and buffering to ensure efficient utilization of supported interfaces.

NOTE For Intel® 6300ESB design and layout information, refer to the Intel® 6300ESB I/O Controller Hub Design Guide.

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3.7 Ultra ATA100/66/33 IDE

The cPCI-6910 supports dual-channel Ultra ATA100 IDE. The primary IDE channel comes onboard the cPCI-6910, while the secondary IDE is routed to the rear transition module (cPCI-R6910) via the J4 connectors. 2.5” hard disk drive slots may be used for the primary IDE interfaces. The Intel® 6300ESB IDE controller supports both legacy and native IDE interface modes. In native mode, the IDE controller functions as a PCI-compliant software interface and does not use any legacy I/O or interrupt resources. For Ultra ATA100/66 modes, proper IDE cables must be used.

3.8 USB 2.0

The cPCI-6910 comes with two EHCI USB 2.0 Host Controllers (shared with UHCI ports) for up to two USB ports on the front panel. The Intel® 6300ESB host controllers support the standard Universal Host Controller Interface (UHCI) Design Guide and over-current detection on all USB ports. Legacy USB devices, such as keyboard, mouse, and floppy disk drives are supported and may be enabled or disabled in the BIOS. Booting the system from a USB floppy disk drive is implemented on all USB ports.

3.9 LPC/Firmware Hub

The 4 Mb system BIOS flash—SST 49LF004A—is compatible with Intel 82802 Firmware Hub (FWH) device specifications. The BIOS is shielded by a write-protect function that can be enabled or disabled in the BIOS option menu.

3.10 System Management Bus

The Intel® 6300ESB comes with a System Management Bus (SMBus) that is compliant with SMBus Specification Version 2.0. The host controller provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves) as well as I2C-compatible devices. The Slave Interface allows an external master to read from or write to the Intel® 6300ESB.

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3.11 UART

The serial port has a UART that supports all functions of a standard 16550 UART including hardware flow control interface. The UART performs serial-to-parallel conversion of data characters received from a peripheral device or a modem and parallel-to-serial conversion of data characters received from the processor.

3.12 Watchdog Timer

The cPCI-6910 implements a 2-stage watchdog timer (WDT). The WDT is embedded in the Intel® 6300ESB and may be enabled or disabled through the BIOS. The WDT supports selectable presclear that is approximately 1 MHz (1 us to 1 s) and approximately 1 KHz (1 ms to 10 min). When the programmed time is up, the WDT generates an IRQ, SMI, or SCI interrupt, then drives the ICH_WDT-L low, and resets the cPCI-6910.

3.13 Real Time Clock

The Real Time Clock (RTC) module provides a battery backed-up date and time keeping device with two banks of 128-byte static RAM. The design is functionally compatible with the Motorola MS146818. The time keeping comes from a 32.768 KHz oscillating source, that is divided to achieve an update every second.

3.14 PCI 32-bit and PCI-X Interface

The Intel® 6300ESB supports one 32-bit/33 MHz PCI interface compliant with PCI Local Bus Specification Revision 2.2. With a 120 MB/s throughput, this bus supports 44-bit addressing using DAC protocol. The cPCI-6910 uses this bus to implement the VGA interface (ATI RS 1000 chip), one PMC port, and one PCI to PCI bridge in PCI-X bus.

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3.15 ATI ES1000 VGA chip

- Maximum 2D performance with the fastest available 2D graphics for multimedia applications in true 24-bit color
- Comprehensive support for Windows® Server OS, including GDI extension acceleration like Alpha BLTs and Gradient Fills, as well as exclusive alpha cursor support

3.16 Hardware Monitor

The IT8712F monitors critical hardware parameters including system and CPU voltages and temperatures. All hardware health status may be accessed in the BIOS and run-time utilities. In addition, once the preset thresholds of hardware conditions are reached, the W83627HF chip alerts or resets the system.

3.17 PCI Resource Allocation

The cPCI-6910 comes with a 133 MHz PCI bus. The IDSEL, INT#, and REQ#/GNT# routines of the cPCI bus slots on the backplane follow standard definitions with the Intel® 6300ESB as the interrupt controller. The table below shows the cPCI-6910 PCI resource allocation.

Function	REQ	GNT	IDSEL	INTA	INTB	INTC	INTD
PXL PCI-6540	PCIX_REQ-L0	PCIX_GNT-L0	PCIX_AD20	PCIX_IRQ-L0			
PMC	PCIX_REQ-L1	PCIX_GNT-L1	PCIX_AD22		PCIX_IRQB-L1		
J1				PCIX_IRQ-L0	PCIX_IRQ-L1	PCIX_IRQ-L2	PCIX_IRQ-L3
ATI ES1000	PCI_REQ-L0	PCI_GNT-L0	PCI_AD18	PCI_IRQ-L0			

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3.18 PCI-X to PCI-X Bridge

The PLX FastLane™ PCI-6540 is a dual-mode universal PCI-X-to-PCI-X bridge and implements the system/peripheral slot on the cPCI-6910. The dual-mode device is capable of operating in transparent, non-transparent, or universal mode. When in non-transparent mode, the cPCI-6910 permits independent memory mapping of both primary and secondary bus with powerful configuration options to support intelligent subsystems. The universal mode permits jumper-less configuration between applications to CompactPCI® interface at peripheral and/or system slot. The universal mode option enables configuration of the PCI-6540 bridge as a transparent bridge in a system slot supporting a host, or as a non-transparent bridge in a peripheral slot as an intelligent subsystem. These options allow installation of the cPCI-6910 in both peripheral and/or system slots.

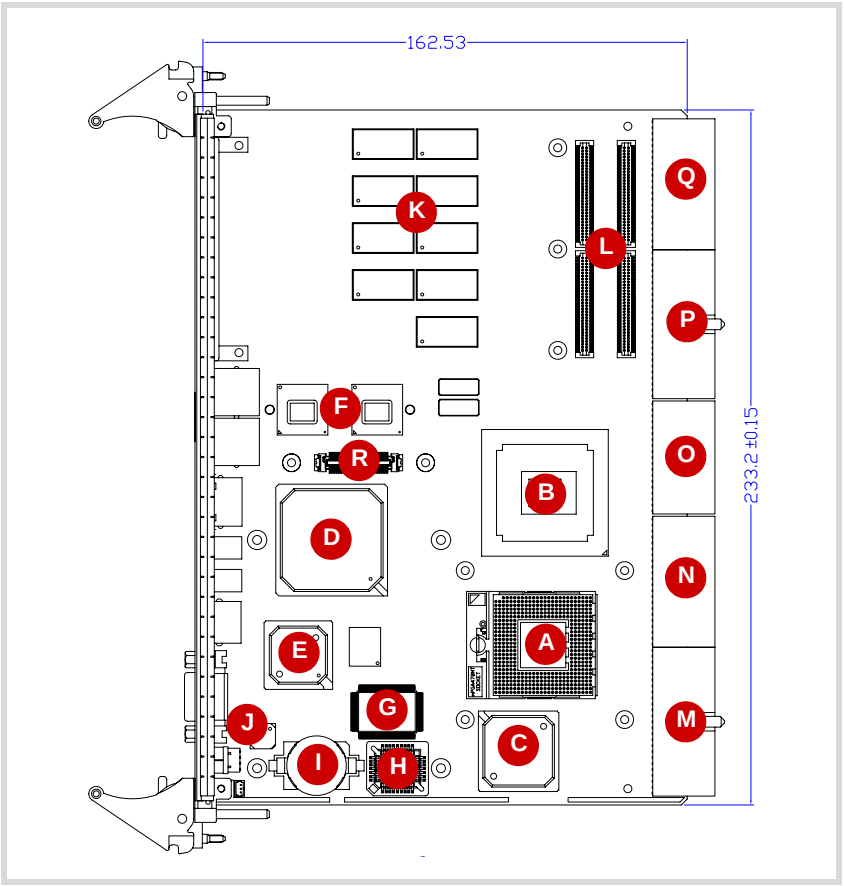
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4 Jumpers and Connectors

This chapter illustrates the board layout, connector pin assignments, and jumper settings to familiarize the users on the cPCI-6910.

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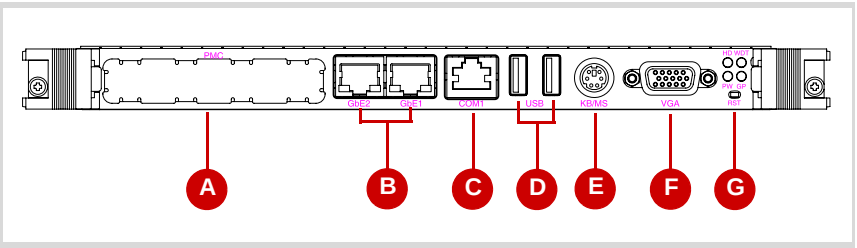
4.1 cPCI-6910 Board Layout



A	CPU Socket	**J**	Buzzer
B	Intel® E7520	**K**	Soldered memory chips
C	PLX PCI-6540	**L**	PMC socket
D	Intel® 6300ESB	**M**	cPCI-J1
E	ATI ES1000	**N**	cPCI-J2
F	Intel® 82571EB	**O**	cPCI-J3
G	SIO (IT8217F)	**P**	cPCI-J4
H	BIOS	**Q**	cPCI-J5
I	RTC Battery	**R**	Board-to-board connector

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4.2 cPCI-6910 Front Panel



A	PMC slot
B	Gigabit Ethernet Port 1/2
C	COM1 port
D	USB 2.0 ports
E	KB/MS port
F	VGA port
G	System LEDs and reset button

System LED indication

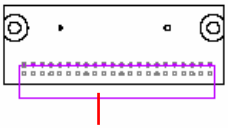


LED	Color	Condition	Indication
HDD	Red	OFF	No HDD
		ON	HDD is installed
		Blinking	Data read/write in process
Power	Yellow	OFF	System is off
		ON	System in on
Watchdog	Amber	OFF	Watchdog event de-alert
		ON	Watchdog event alert
Hotswap	Blue	OFF	Handler is close/System is on
		ON	Handler is open

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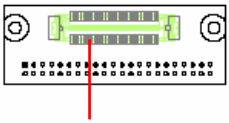
4.3 cPCI-6910 Daughterboard Layout

DB-6910IDE



44-pin IDE connector

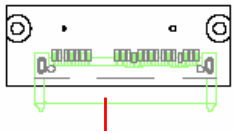
Front view



Board to board connector

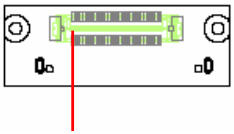
Rear View

DB-6910SAT



SATA connector

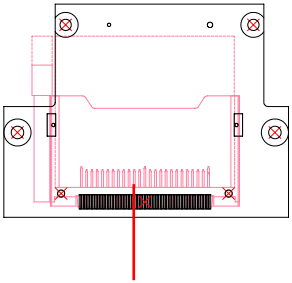
Front view



Board to board connector

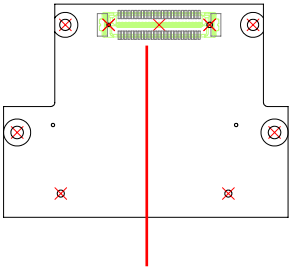
Rear View

DB-6910CF



CompactFlash socket

Front view

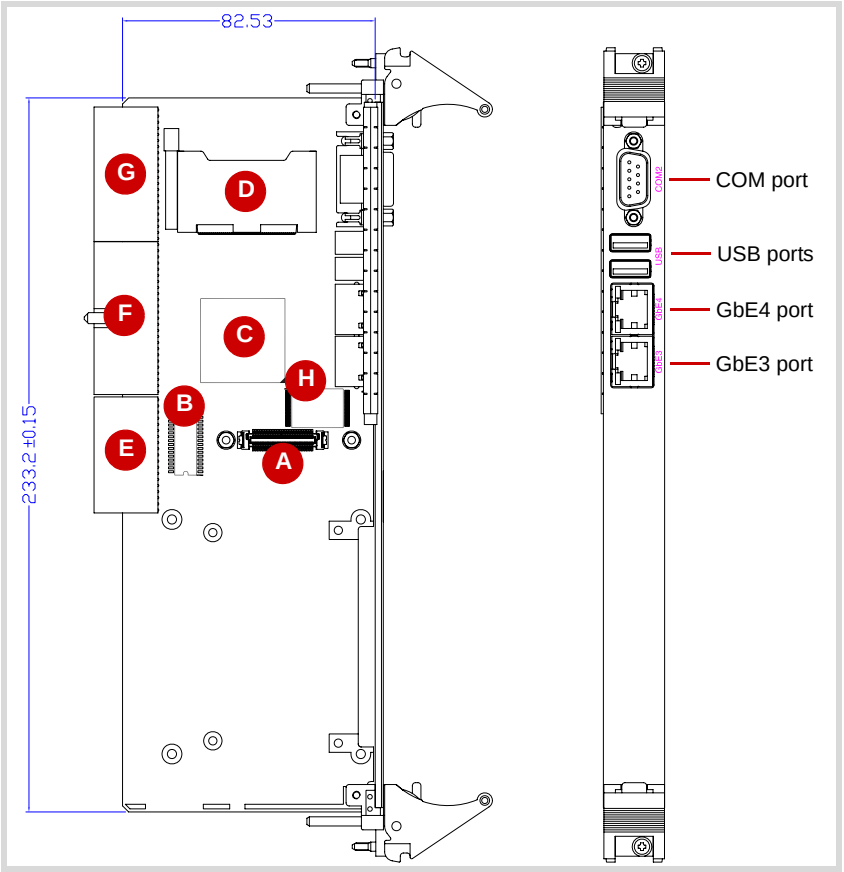


Board to board connector

Rear View

4.4 Rear Transition Modules

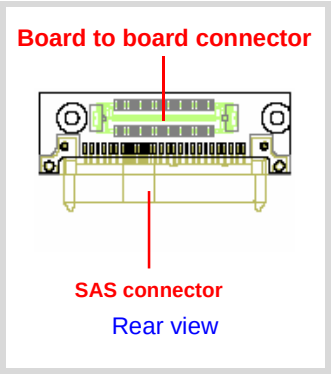
cPCI-R6910 Board and Daughterboard Layouts



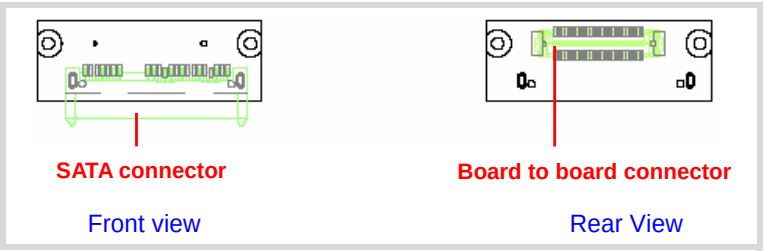
A	Board to board connector	**E**	cPCI rJ3 connector
B	SAS nVRAM	**F**	cPCI rJ4 connector
C	LSI1064E controller	**G**	cPCI rJ5 connector
D	CompactFlash® socket	**H**	SAS Flash ROM

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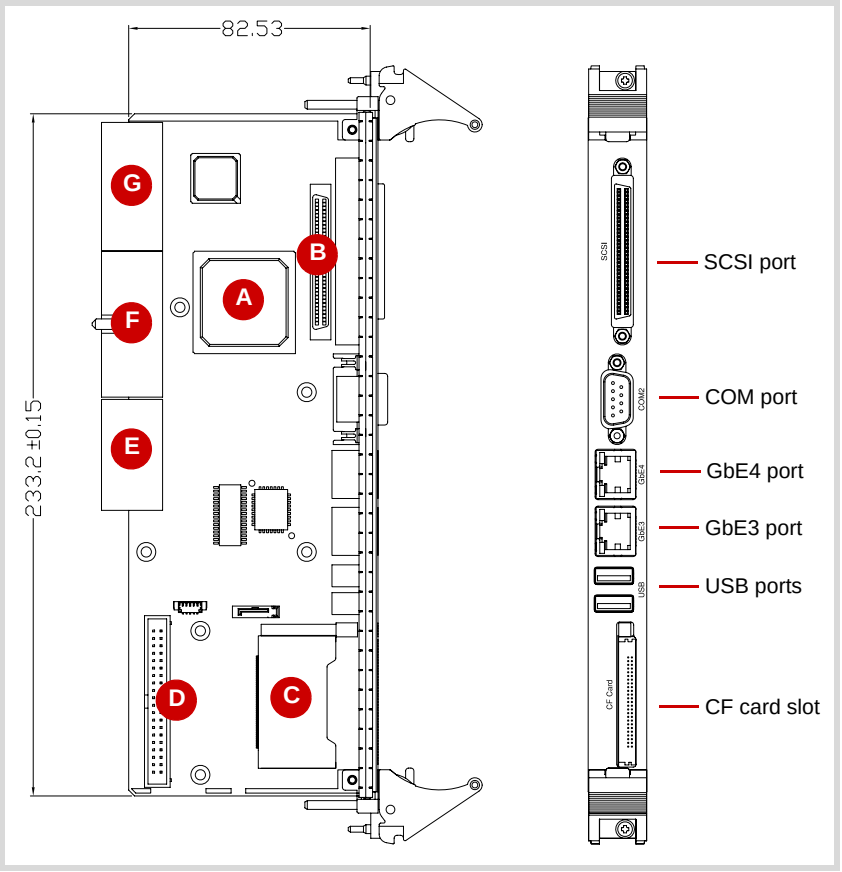
DB-R6910SAS



DB-R6910SAT



cPCI-R6911 Board Layout

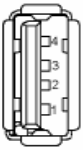


A	LSI1020 controller	**E**	cPCI rJ3 connector
B	68-pin SCSI connector	**F**	cPCI rJ4 connector
C	CompactFlash® socket	**G**	cPCI rJ5 connector
D	40-pin IDE connector		

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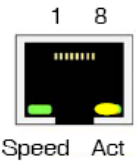
4.5 Connector Pin Assignments

USB Connectors



Pin #	Signal Name
1	Vcc
2	USB-
3	USB+
4	GND

Ethernet (RJ-45) Connector

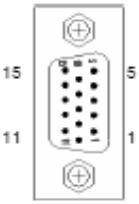


Pin #	Signal Name	Function
1	GBE0_MDI0+	Media Dependent Interface 0+
2	GBE0_MDI0-	Media Dependent Interface 0-
3	GBE0_MDI1+	Media Dependent Interface 1+
4	GBE0_MDI2+	Media Dependent Interface 2+
5	GBE0_MDI2-	Media Dependent Interface 2-
6	GBE0_MDI1-	Media Dependent Interface 1-
7	GBE0_MDI3+	Media Dependent Interface 3+
8	GBE0_MDI3-	Media Dependent Interface 3-

Status		Speed LED (Green)	Act LED (Amber)
Network link is not established		OFF	OFF
10/100 Mbps	Link	OFF	ON
	Active	OFF	Blink
1000 Mbps	Link	ON	ON
	Active	ON	Blink

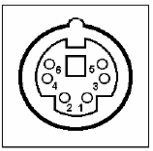
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VGA Connector



Signal Name	Pin #	Pin #	Signal Name
Red	1	2	Green
Blue	3	4	N.C.
GND	5	6	GND
GND	7	8	GND
+5V.	9	10	GND
N.C.	11	12	CRTDATA
HSYNC	13	14	VSYNC
CRTCLK	15		

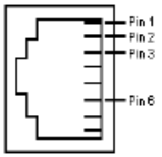
PS2 Connector



Pin #	Signal	Function
1	KBDATA	Keyboard Data
2	MSDATA	Mouse Data
3	GND	Ground
4	+5V	Power
5	KBCLK	Keyboard Clock
6	MSCLK	Mouse Clock

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Serial Port (COM1)



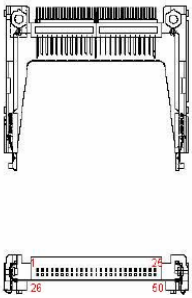
Pin #	Signal Name	Function
1	DCD#	Data Carrier Detect
2	RTS#	Request to Send
3	DSR#	Data Set Ready
4	TXD	Transmit Data
5	RXD	Receive Data
6	GND	Ground
7	CTS#	Clear to Send
8	DTR#	Data Terminal Ready

COM Port Signal Definitions

- CTS: Indicates that the data set is ready to exchange data.
- DCD: Indicates that the data set has detected the data carrier.
- DSR: Indicates that the data set is ready to establish a communications link.
- DTR: Indicates that the data terminal is ready to establish a communications link.
- RI: Indicates that the modem has received a telephone-ringing signal.
- RTS: Communicates to the data set that UART is ready to exchange data.
- RX: Receives serial data input from communications link.
- TX: Sends a serial output to communications link.

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CompactFlash® Connector



Signal Name	Pin #	Pin #	Signal Name
GND	1	26	GND
DD3	2	27	DD11
DD4	3	28	DD12
DD5	4	29	DD13
DD6	5	30	DD14
DD7	6	31	DD15
CS1#	7	32	CS3#
GND	8	33	GND
GND	9	34	DIOR#
GND	10	35	DIOW#
GND	11	36	5V
GND	12	37	IRQ15
5V	13	38	NC
GND	14	39	PCSEL
GND	15	40	5V
GND	16	41	PCIRST4#
GND	17	42	DIORDY
DA2	18	43	DREQ
DA1	19	44	DACK#
DA0	20	45	DACT#
DD0	21	46	66DECT
DD1	22	47	DD8
DD2	23	48	DD9
NC	24	49	DD10
GND	25	50	GND

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4.6 Hard Disk Drive Board to Board Connector

On CPU Blade - SATA/IDE Connector

Signal Name	Pin #	Pin #	Signal Name
GND	1	27	PIDE_DIOR-L
GND	2	28	PIDE_66DECT
PCIRST4#	3	29	PIDE_IORDY
PIDE_D8	4	30	GND
PIDE_D7	5	31	PIDE_DACK-L
PIDE_D9	6	32	+5V
PIDE_D6	7	33	IDE_IRQ14
PIDE_D10	8	34	+5V
PIDE_D5	9	35	PIDE_DA1
PIDE_D11	10	36	+5V
PIDE_D4	11	37	PIDE_DA0
PIDE_D12	12	38	+12V
PIDE_D3	13	39	PIDE+CS1-L
PIDE_D13	14	40	+12V
PIDE_D2	15	41	PIDE_DACT-L
PIDE_D14	16	42	+12V
PIDE_D1	17	43	GND
PIDE_D15	18	44	GND
PIDE_D0	19	45	GND
GND	20	46	SATA0_TX-N
GND	21	47	SATA0_RX-N
PIDE_LOW	22	48	SATA0_TX-P
PIDE_DREQ	23	49	SATA0_RX-P
PIDE_DA2	24	50	GND
PIDE_DIOW#	25	51	GND
PIDE_CS3#	26	52	GND

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On Rear I/O - SATA/SAS Connector

Signal Name	Pin #	Pin #	Signal Name
GND	1	27	GND
SAS0_RX-N	2	28	GND
SAS0_TX-N	3	29	GND
SAS0_RX-P	4	30	GND
SAS0_TX-P	5	31	+12V
GND	6	32	+5V
GND	7	33	+12V
SAS1_RX-N	8	34	+5V
SAS1_TX-N	9	35	+12V
SAS1_RX-P	10	36	+5V
SAS1_TX-P	11	37	+12V
GND	12	38	+5V
GND	13	39	GND
SAS2_RX-N	14	40	GND
SAS2_TX-N	15	41	SATA_LED#
SAS2_RX-P	16	42	GND
SAS2_TX-P	17	43	GND
GND	18	44	GND
GND	19	45	SATA1_RX-N
SAS3_RX-N	20	46	SATA1_TX-N
SAS3_TX-N	21	47	SATA1_RX-P
SAS3_RX-P	22	48	SATA1_TX-P
SAS3_TX-P	23	49	GND
GND	24	50	GND
GND	25	51	GND
GND	26	52	GND

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CompactPCI® J1 Pin Assignment

	A	B	C	D	E	F
1	+5V	-12V	TRST#	+12V	+5V	GND
2	TCK	+5V	TMS	NC	TDI	GND
3	INTA#	INTB#	INTC#	+5V	INTD#	GND
4	+5V_IPMB	HEALTHY#	VIO	NC	NC	GND
5	NC	NC	RST#	GND	GNT0#	GND
6	REQ#	PRESENT	3.3V	BP_CLK0	AD[31]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
8	AD[26]	GND	VIO	AD25	AD[24]	GND
9	CBE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
10	AD[21]	GND	+3.3V	AD[20]	AD[19]	GND
11	AD[18]	AD[17]	AD[16]	GND	CBE2#	GND
12-14	Key					GND
15	+3.3V	FRAME#	IRDY#	BDSEL#	TRDY#	GND
16	DEVSEL#	PCIXCAP	VIO	STOP#	LOCK#	GND
17	+3.3V	IPMB_CLK	IPMB_DAT	GND	PERR#	GND
18	SERR#	GND	+3.3V	PAR	CBE1#	GND
19	+3.3V	AD[15]	AD[14]	GND	AD[13]	GND
20	AD[12]	GND	VIO	AD[11]	AD[10]	GND
21	+3.3V	AD[9]	AD[8]	M66EN	CBE0#	GND
22	AD[7]	GND	+3.3V	AD[6]	AD[5]	GND
23	+3.3V	AD[4]	AD[3]	+5V	AD[2]	GND
24	AD[1]	+5V	VIO	AD[0]	ACK64#	GND
25	+5V	REQ64#	ENUM#	+3.3V	+5V	GND
	A	B	C	D	E	F

NOTE To support PICMG® 2.1 hot-swap function for peripheral boards, the backplane must bus together all ENUM# peripheral slots to the system slot. The ENUM# signal can be polled by software or generated by an interrupt.

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CompactPCI® J2 Pin Assignment

	A	B	C	D	E	F
1	CLK1	GND	REQ1#	GNT1#	REQ2#	GND
2	CLK2	CLK3	SYSTEM#	GNT2#	REQ3#	GND
3	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
4	VIO	NC	C/BE[7]#	GND	C/BE[6]#	GND
5	C/BE[5]#	64EN#	VIO	C/BE[4]#	PAR64	GND
6	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
7	AD[59]	GND	VIO	AD[58]	AD[57]	GND
8	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
9	AD[52]	GND	VIO	AD[51]	AD[50]	GND
10	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
11	AD[45]	GND	VIO	AD[44]	AD[43]	GND
12	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
13	AD[38]	GND	VIO	AD[37]	AD[36]	GND
14	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
15	NC	GND	FAL#	REQ5#	GNT5#	GND
16	NC	NC	DEG#	GND	NC	GND
17	NC	GND	RST#	REQ6#	GNT6#	GND
18	NC	NC	NC	GND	NC	GND
19	GND	GND	NC	NC	NC	GND
20	CLK5	GND	NC	GND	NC	GND
21	CLK6	GND	NC	NC	NC	GND
22	GA4	GA3	GA2	GA1	GA0	GND
	A	B	C	D	E	F

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CompactPCI® J3 Pin Assignment

	A	B	C	D	E	F
1	+5V	+5V	+5V	+5V	+5V	GND
2	+5V	+5V	+5V	+5V	+5V	GND
3	+3.3V	+3.3V	+3.3V	+3.3V	+3.3V	GND
4	+3.3V	+3.3V	+3.3V	+3.3V	+3.3V	GND
5	+12V	+12V	+12V	+12V	+12V	GND
6	-12V	-12V	GND	SATA_LED#	GND	GND
7	GND	GND	GND	GND	GND	GND
8	GND	SATA1_TX-N	GND	SATA_RX-N	GND	GND
9	GND	SATA1_TX-P	GND	SATA1_RX-P	GND	GND
10	GND	GND	GND	GND	GND	GND
11	+5V	+5V	+5V	IPM_CLK	IPM_DAT	GND
12	LANBB_LINK#	LANBB_100#	LANBB_ACT#	+5V	+5V	GND
13	LANBA_1G#	LANBA_100#	LANBA_ACT#	LANBA_LINK#	LANBB_1G#	GND
14	GND	GND	P1V8_LANB	GND	GND	GND
15	LANBA_TXDP1	LANBA_TXDN1	GND	LANBA_TXDP3	LANBA_TXDN3	GND
16	LANBA_TXDP0	LANBA_TXDN0	GND	LANBA_TXDP2	LANBA_TXDN2	GND
17	LANBB_TXDP1	LANBB_TXDN1	GND	LANBB_TXDP3	LANBB_TXDN3	GND
18	LANBB_TXDP0	LANBB_TXDN0	GND	LANBB_TXDP2	LANBB_TXDN2	GND
19	GND	GND	GND	GND	GND	GND
	A	B	C	D	E	F

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CompactPCI® J4 Pin Assignment

	A	B	C	D	E	F
1	PMC_IO9	PMC_IO7	PMC_IO5	PMC_IO3	PMC_IO1	GND
2	PMC_IO10	PMC_IO8	PMC_IO6	PMC_IO4	PMC_IO2	GND
3	PMC_IO19	PMC_IO17	PMC_IO15	PMC_IO13	PMC_IO11	GND
4	PMC_IO20	PMC_IO18	PMC_IO16	PMC_IO14	PMC_IO12	GND
5	PMC_IO29	PMC_IO27	PMC_IO25	PMC_IO23	PMC_IO21	GND
6	PMC_IO30	PMC_IO28	PMC_IO26	PMC_IO24	PMC_IO22	GND
7	PMC_IO39	PMC_IO37	PMC_IO35	PMC_IO33	PMC_IO31	GND
8	PMC_IO40	PMC_IO38	PMC_IO36	PMC_IO34	PMC_IO32	GND
9	PMC_IO49	PMC_IO47	PMC_IO45	PMC_IO43	PMC_IO41	GND
10	PMC_IO50	PMC_IO48	PMC_IO46	PMC_IO44	PMC_IO42	GND
11	PMC_IO59	PMC_IO57	PMC_IO55	PMC_IO53	PMC_IO51	GND
12-14	Key Area					
15	PMC_IO60	PMC_IO58	GND	NC	GND	GND
16	PMC_IO56	PMC_IO54	PMC_IO52	PMC_IO63	PMC_IO61	GND
17	PMC_IO64	PMC_IO62	NC	NC	NC	GND
18	SIDE_D4	SIDE_D3	SIDE_D2	SIDE_D1	SIDE_D0	GND
19	SIDE_D9	SIDE_D8	SIDE_D7	SIDE_D6	SIDE_D5	GND
20	SIDE_D14	SIDE_D13	SIDE_D12	SIDE_D11	SIDE_D10	GND
21	SIDE_D15	SIDE_DACK#	SIDE_DREQ	SIDE_DIOR#	SIDE_DIOW#	GND
22	SIDE_IORDY	SIDE_DA2	SIDE_DA1	SIDE_DA0	SIDE_CS1#	GND
23	SIDE_CS3#	IDE_IRQ15	SIDE_DACT#	SIDE_66DECT	NC	GND
24	NC	NC	NC	NC	NC	GND
25	NC	NC	NC	NC	NC	GND
	A	B	C	D	E	F

NOTES

The cPCI-6910 does not function on a peripheral slot with CT bus backplane (H.110).

Depending on ODM project requirements, the J4 connector may be removed to support an H.110 backplane.

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CompactPCI® J5 Pin Assignment

	A	B	C	D	E	F
1	GND	COM2_DCD#	COM2_RI#	COM2_CTS#	COM2_DTR#	GND
2	GND	COM2_RTS#	COM2_DSR#	COM2_TXD	COM2_RXD	GND
3	GND	GND	GND	RTM_IN#	PCIRST4#	GND
4	GND	GND	USB2-N	USB2-P	GND	GND
5	GND	GND	GND	GND	GND	GND
6	GND	GND	USB3-N	USB3-P	GND	GND
7	USB_OC3#	USB_OC2#	GND	GND	GND	GND
8	GND	GND	GND	CLK100_SAS-P	CLK100_SAS-N	GND
9	GND	GND	GND	GND	GND	GND
10	GND	PCIEC_TP0	GND	PCIEC_RP0	GND	GND
11	GND	PCIEC_TN0	GND	PCIEC_RN0	GND	GND
12	GND	GND	GND	GND	GND	GND
13	GND	PCIEC_TP1	GND	PCIEC_RP1	GND	GND
14	GND	PCIEC_TN1	GND	PCIEC_RN1	GND	GND
15	GND	GND	GND	GND	GND	GND
16	GND	GND	GND	GND	GND	GND
17	GND	PCIEC_TP2	GND	PCIEC_RP2	GND	GND
18	GND	PCIEC_TN2	GND	PCIEC_RN2	GND	GND
19	GND	GND	GND	GND	GND	GND
20	GND	PCIEC_TP3	GND	PCIEC_RP3	GND	GND
21	GND	PCIEC_TN3	GND	PCIEC_RN3	GND	GND
22	GND	GND	GND	GND	GND	GND
	A	B	C	D	E	F

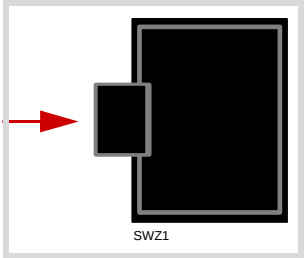
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4.7 Switches

Clear CMOS Switch (SWZ1)

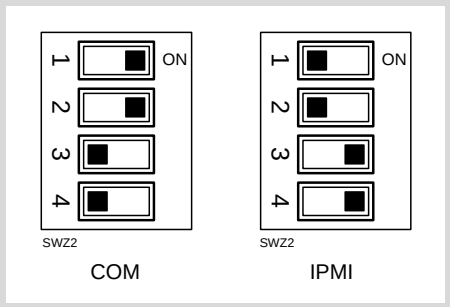
To reset the CMOS values to default, the cPCI-6910 comes with a clear CMOS switch. Press the switch to clear the CMOS

.



COM and IPMI Switch (SWZ2)

This switch allows you to set the serial port to COM or IPMI mode. Refer to the table for the switch settings.



Mode	1	2	3	4
COM	ON	ON	OFF	OFF
IPMI	OFF	OFF	ON	ON

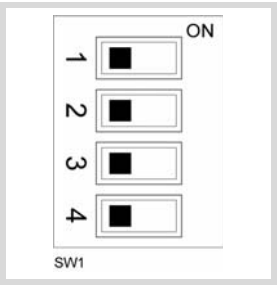
NOTE: This switch is set to COM by default.

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PCB Switch (SW1)

The SW1 switch is OFF by default. Refer to the tables below for switch settings:

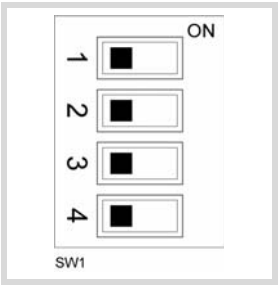
SW1 settings for PCB version B2 and previous versions.



Switch	Status	Description
1	ON	Reserved for debugging purposes
2	ON	Reserved for debugging purposes
3	ON	Precharge disabled. The board boots up in peripheral slot even without a system board.
4	ON	SYSTEM# ENABLE. Reserved for debugging purposes.

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SW1 settings for PCB version B3 and future versions.



Switch	Status	Description
1	ON	Disables CMM control
2	ON	Reserved for debugging purposes
3	ON	Precharge disabled. The board boots up in peripheral slot even without a system board.
4	ON	SYSTEM# ENABLE. The board behaves as the system board in a peripheral slot.

Miniature Switch on the Lower Ejector (Front Panel)

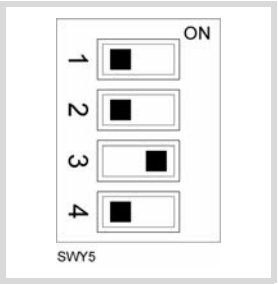
This switch is designed for power and hot-swap control. When the cPCI-6910 is installed to the system slot, it does not power up until the lower ejector is closed. The lower ejector also issues a power button signal when you open it.

When the cPCI-6910 is installed to a peripheral slot, it does not power up until the lower ejector is closed. After the lower ejector is closed, the cPCI-6910 sends out an ENUM# signal to the system to indicate that it has been installed to the CompactPCI backplane. When the lower ejector is opened, the cPCI-6910 sends out an ENUM# to the system, then waits for the command from system.

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cPCI-R6911 RTM Switches (SWY1, 2, 3 & 4)

SWY 5 Settings



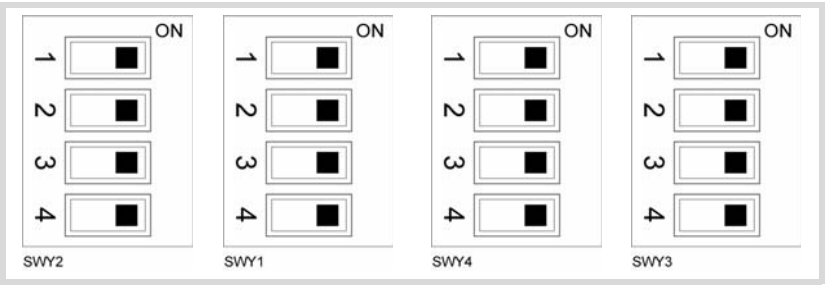
Switch	Status	Description
1	OFF	Reserved
2	OFF	Reserved
3	ON	CF Slave (default)
4	ON	CF Master

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SWY2, SWY1, SWY4, and SWY3 Settings

All SWY switches are set to ON by default

.



The cPCI-R6911 supports GbE3 and GbE4 on both the 2.16 backplane and rear I/O. The PICMG® 2.16 backplane and rear I/O cannot be accessed simultaneously. SWY1 to SWY4 must be set to either the 2.16 backplane or the RTM. The following table shows how to set the DIP switches to enable either the 2.16 backplane or RTM for GbE3 and GbE4.

Connected to:	GbE3 (SWY1 and SWY2)	GbE4 (SWY3 and SWY4)
PICMG® 2.16 Backplane	ALL OFF	ALL OFF
Rear faceplate RJ-45 connectors	ALL ON (default)	ALL ON (default)

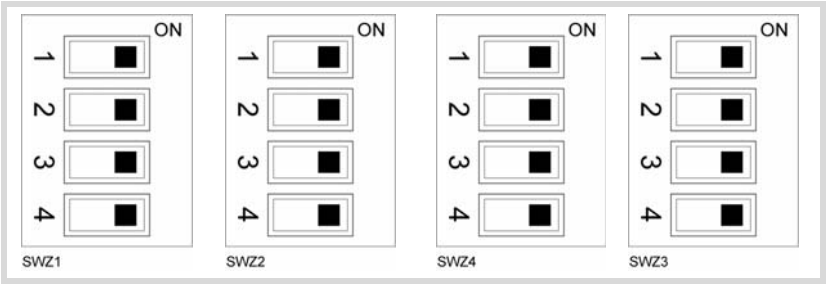
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cPCI-R6910 RTM Switches (SWZ1, 2, 3 & 4)

SWZ1, SWZ2, SWZ4, and SWZ3 Settings

All SWZ switches are set to ON by default

.



The cPCI-R6910 supports GbE3 and GbE4 on both the 2.16 backplane and rear I/O. The PICMG® 2.16 backplane and rear I/O cannot be accessed simultaneously. SWZ1 to SWZ4 must be set to either the 2.16 backplane or the RTM. The following table shows how to set the DIP switches to enable either the 2.16 backplane or RTM for GbE3 and GbE4.

Connected to:	GbE3 (SWZ1 and SWZ2)	GbE4 (SWZ3 and SWZ4)
PICMG® 2.16 Backplane	ALL OFF	ALL OFF
Rear faceplate RJ-45 connectors	ALL ON (default)	ALL ON (default)

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5 Getting Started

This chapter describes the installation of the following components to the cPCI-6910 and cPCI-R6910 rear transition module:

- CPU
- Heat sink
- 2.5" hard disk drive (IDE/Serial ATA/SAS)
- CompactFlash card

5.1 Tools

Keep the following tools on hand when installing components to the cPCI-6910:

- Phillips (cross) screwdriver
- Flathead screwdriver
- Hexagon hole sleeve (for HDD standoffs installation)

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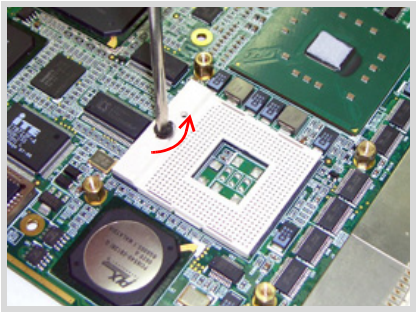
5.2 Installing the CPU

The cPCI-6910 supports one Dual-Core Intel® Xeon® processor LV/ULV. A proprietary heatsink is included in the package for thermal management. Follow these procedures to install the CPU and heatsink.

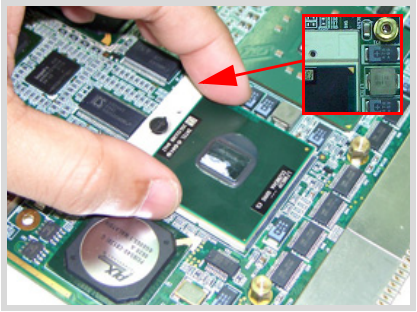
NOTE Skip this section if the CPU and heatsink comes pre-installed on the cPCI-6910.

To install the CPU:

1. Locate the CPU socket on the cPCI-6910.
2. Use a flathead screwdriver to turn the CPU lock screw counterclockwise and unlock the socket.

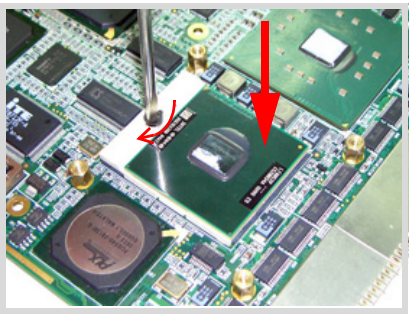


3. Carefully place the CPU into the socket. Make sure that the gold triangle at one corner of the CPU matches the triangular mark at one corner of the socket.



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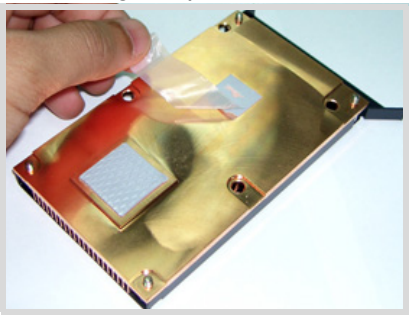
4. Gently press the CPU until it is properly seated on the socket, then turn the CPU lock screw clockwise to lock the socket.



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5.3 Installing the Heatsink

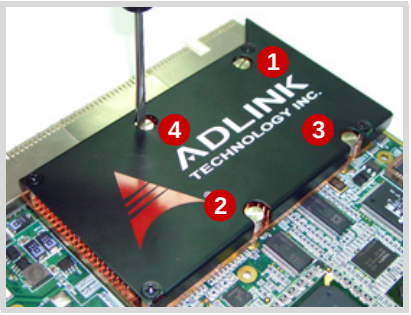
1. Peel the plastic film that covers the thermal strip for the CPU and Northbridge chip.



2. Position the heatsink on top of the CPU and the Northbridge chip until the heatsink screw holes align with the board standoffs. Make sure that the CPU/Northbridge and the heatsink thermal pads have proper contact.



3. Secure the heatsink with four screws in a diagonal sequence to prevent tilt. Refer to the illustration below.



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5.4 Installing the Hard Disk Drive

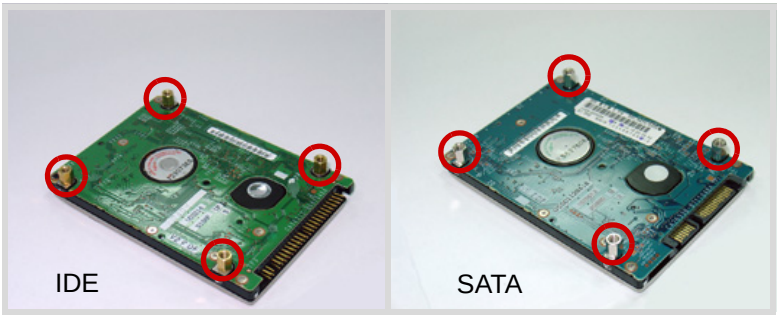
On the cPCI-6910

The cPCI-6910 supports a 2.5" IDE or Serial ATA HDD. All accessories are packed in the HDD accessory pack (DB-6910IDE/DB-6910SAT HDD kit).

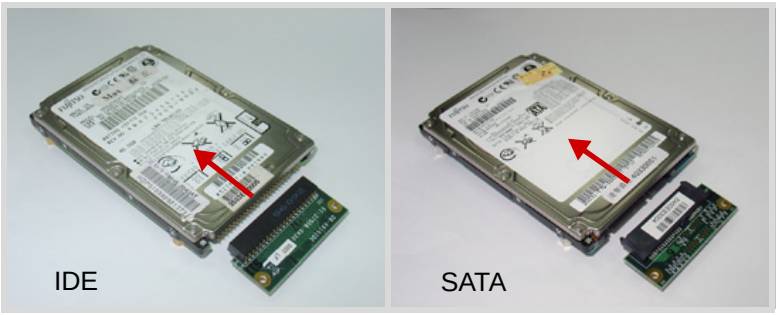
NOTE If the cPCI-6910 comes with a pre-installed HDD, proceed to the next section.

To install an IDE/SATA hard disk drive:

1. Use a hexagon hole sleeve to attach four stand-offs on the IDE/SATA hard disk drive.

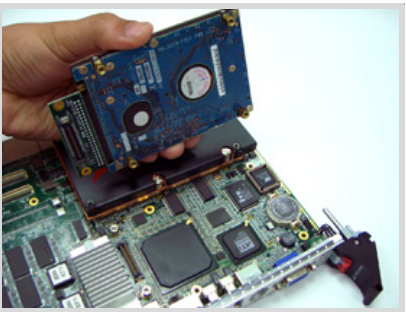


2. Attach the DB-6910IDE/DB-6910SAT adapter board to the HDD connectors.



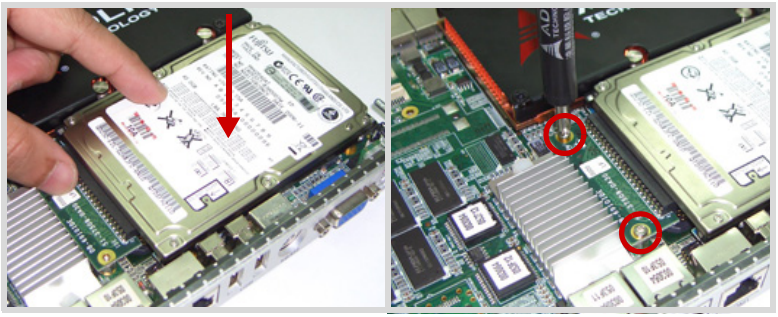
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3. Position the HDD assembly on top of the cPCI-6910. Make sure you align the HDD standoffs with the board screw holes and the adapter board with the board-to-board connector.



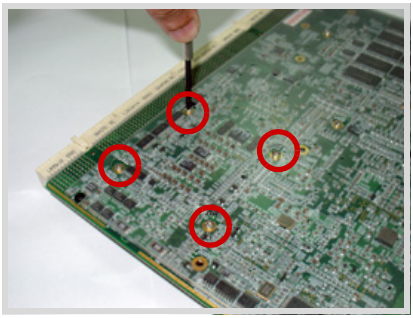
NOTE When removing the HDD, always lift it with the adapter board in a vertical motion (up/down) to avoid damaging the board and other components.

4. Press the DB-6910IDE/DB-6910SAT adapter to the board-to-board connector until it is properly seated. Secure the adapter with two screws.



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5. Secure the HDD with four screws from the board's solder side.



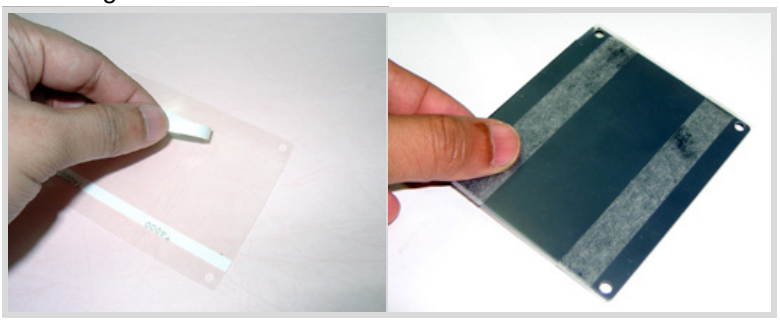
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On the cPCI-R6910 rear transition module

The cPCI-6910 supports a 2.5" Serial ATA or Serial Attached SCSI (SAS) HDD. All accessories are packed in the HDD accessory pack (DB-R6910SAT/DB-R6910SAS HDD kit).

To install a SATA/SAS hard disk drive to the RTM:

1. **SAS HDD only**: Locate the bundled plastic film, remove the adhesive strips, then stick the film into the drive tray bottom. Make sure that the film and the tray screw holes align.



2. **SAS HDD only**: Place the SAS HDD on the drive tray, then secure it with one screw.



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3. Attach the DB-R6910SAT/DB-R6910SAS adapter board to the HDD connectors.



4. Position the HDD assembly on top of the RTM. Make sure that the bottom HDD and the board screw holes align and the adapter board matches with the board-to-board connector.



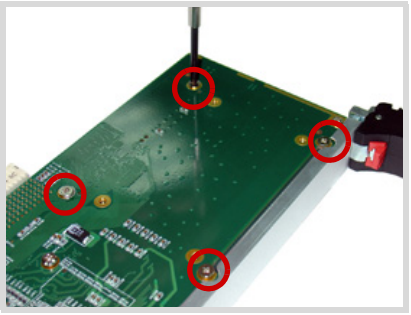
NOTE	When removing the HDD, always lift it with the adapter board in a vertical motion (up/down) to avoid damaging the board and other components.

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5. Press the DB-R6910SAT/DB-R6910SAS adapter to the board-to-board connector until it is properly seated. Secure the adapter with two screws.



6. Secure the HDD with four screws on the solder side of the board.



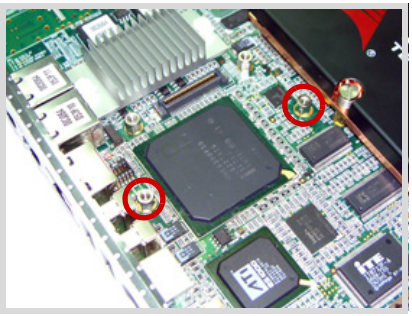
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5.5 Installing the CompactFlash® Card Slot

Depending on your selected configuration, the cPCI-6910 comes with an optional DB-6910CF accessory kit that allows installation of an internal CF card slot instead of a hard disk drive. CompactFlash® storage is required by some industrial applications because of its resistance to vibration and convenient installation/ replacement.

To install the CF card slot:

1. Install two DB-6910CF standoffs.

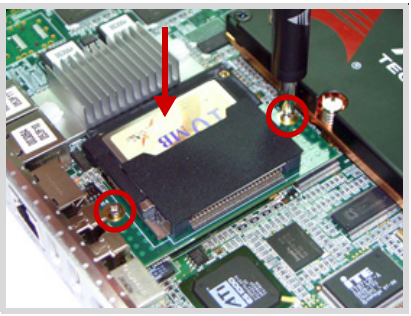


2. Insert the CF card to the DB-6910CF slot.

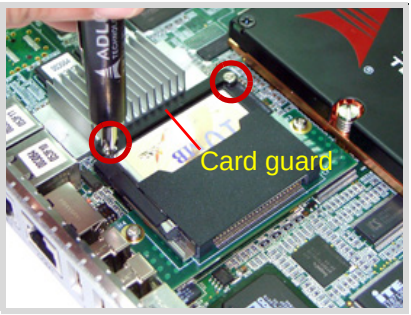


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3. Press the DB-6910CF adapter to the board-to-board connector until it is properly seated. Secure the adapter with two screws.



4. Install the CF card guard, then secure the DB-6910CF adapter to the board-to-board connector using two screws.



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5.6 Installing the cPCI-6910 to the Chassis

The cPCI-6910 may be installed in a system or peripheral slot of a 6U cPCI chassis. These instructions are for reference only. Refer to the documentation that came with the chassis for more information.

To install the cPCI-6910 to the chassis:

1. Locate and remove the system controller slot cover.
2. Press down the cPCI-6910 ejector/injector handle(s) to loosen.
3. Align the controller's top and bottom edges to the chassis card guides, then carefully slide the controller into the chassis.
4. Push the ejector/injector handle(s) up to secure the controller in place, then fasten the screws on the module front panel.
5. Connect all devices to the system controller.

5.7 Installing the cPCI-R6910 to the Chassis

The cPCI-R6910 may be installed in a 6U cPCI chassis with rear transition module slots. These instructions are for reference only. Refer to the documentation that came with the chassis for more information.

To install the cPCI-R6910 to the chassis:

1. Turn the chassis to access the RTM slots.
2. Press down the cPCI-R6910 ejector/injector handle(s) to loosen.
3. Align the modules's top and bottom edges to the chassis card guides, then carefully slide the module into the chassis.
4. Push the ejector/injector handle(s) up to secure the module in place, then fasten the screws on the module front panel.
5. Connect all cables and devices to the module.

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6 Driver Installation

The cPCI-6910 drivers are available from the ADLINK All-In-One CD or from the ADLINK website (http://www.adlinktech.com). The following describes the driver installation procedures for Windows® 2000, Windows® XP:

1. Install the Windows® operating system before installing any driver. Most standard I/O device drivers are installed during Windows installation.
2. Install the chipset driver.
3. Install the VGA driver and utilities. Refer to section 6.1 for details on how to install the VGA driver in Windows® 2000/XP operating systems.
4. Install the LAN drivers.
5. Install the SAS driver (cPCI-R6910 only)
6. Install the SCSI driver (cPCI-R6911 only)

We recommend using the chipset, VGA, and LAN drivers provided on the ADLINK All-in-One CD or downloaded from the ADLINK website to ensure compatibility. Contact ADLINK to get support for Linux® and VxWorks® BSP drivers.

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6.1 Installing the VGA driver

Windows® 2000

1. Click **Start**, right-click on **My Computer**, then select **Properties** from the drop-down menu.
2. Click on the **Hardware** tab, then click **Device Manager**.
3. Right-click on the Video Controller (VGA Compatible) item, then click **Properties** from the drop-down menu.
4. From the **General** tab, click **Reinstall Driver**.
5. Click **Next** when the **Upgrade Device Driver Wizard** window appears.
6. Select **Search for a suitable driver for my device (recommended)**, then click **Next**.
7. Check the **Specify a location** option, then click **Next**.
8. When prompted to locate the file, click **Browse**, then select **C2_29263.inf** from this support CD directory:

   `X:\ES1000\2KXP_INF\`
9. When the file is found, click **OK**, then click **Next**.
10. Follow screen procedures to install the drivers, then restart the system to complete installation.

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Windows® XP Professional

1. Follow steps 1 to 4 of the previous section.
2. When the Hardware Update Wizard window appears, select the **Yes, this time only** option, then click **Next**.
3. Select the **Install from a list or specific location (Advanced)** option, then click **Next**.
4. Select the **Search for a best driver in these locations** option, uncheck the **Search removable media (floppy, CD-ROM...)**, then check **Include this location in the search:** option.
5. When prompted to locate the file, click **Browse**, then open this support CD directory:

   `X:\ES1000\2KXP_INF\`
6. Click **Continue Anyway** from the **Hardware Installation** window.
7. After installation is complete, click **Finish**, then restart the system.

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7 Watchdog Timer

This section explains the operation of the cPCI-6910's watchdog timer (WDT). It provides an overview of watchdog operation and features, as well as a sample code to help you learn how the watchdog timer works.

7.1 WDT Overview

The primary function of the watchdog timer is to monitor the cPCI-6910's operation and to generate IRQ or reset the system if the software fails to function as programmed. The watchdog timer may be:

- Enabled and disabled through software control
- Armed and strobed through software control

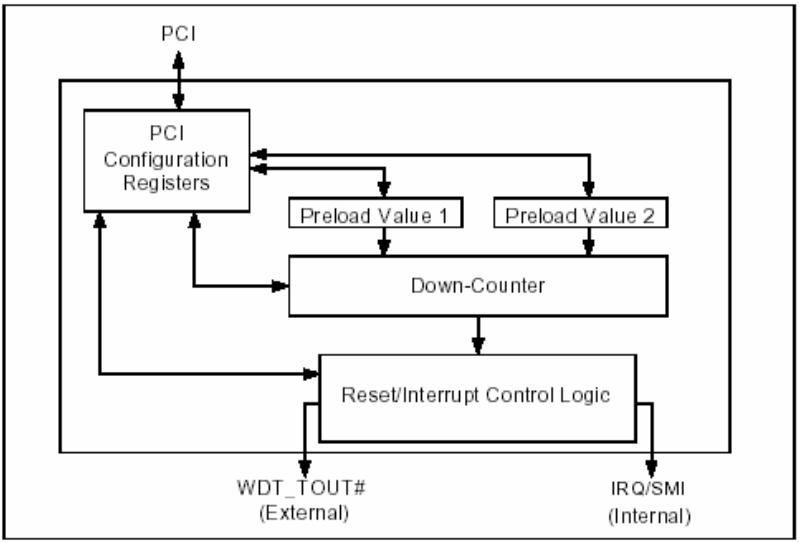


Figure 7-1: WDT Block Diagram

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The cPCI-6910's custom watchdog timer circuit is integrated in the Intel® 6300ESB Southbridge.

The Intel® 6300ESB ICH includes a two-stage Watchdog Timer (WDT) that provides a resolution ranging from one microsecond to ten minutes. The timer uses a 35-bit Down-Counter that is loaded with the value from the first Preload register. The timer is then enabled and starts to count down. The time at which the WDT first starts counting down is called the first stage. If the host fails to reload the WDT before the 35-bit down counter reaches zero, the WDT generates an internal interrupt. After the interrupt is generated, the WDT loads the value from the second Preload register into the WDT's 35-bit Down-Counter and starts counting down. The WDT is now in the second stage. If the host still fails to reload the WDT before the second timeout, the WDT drives the WDT_TOUT# pin low. The WDT_TOUT# pin is held low until the system resets.

The WDT also supports free-running mode. Free-running mode is a one stage timer that toggles the WDT_TOUT# after a programmable time.

Configuration Registers

The Intel® 6300ESB ICH WDT appears as PCI Bus 0, Device 29, Function 4 in the BIOS and has the standard set of PCI configuration register. The configuration registers include:

Offset 10H: Base Address Register (BAR)

Determines the memory base for WDT down-counter setting. This is used to set Preload value 1 register, Preload value 2 register, General Interrupt Status register, and Reload register.

Preload Value 1 & 2 registers

Holds the preload value for the WDT timer. This value is automatically transferred to the down-counter every time the WDT enters the first and second stages. Preload Value 1 register locates at Base + 00H and Preload Value 2 register locates at Base + 04H. Only bit [19:0] may be set. The register unlocking sequence is necessary when writing to the Preload registers.

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Follow these to write a value to preload value 1 and 2 register:

1. Write 80H to offset BAR + 0CH.
2. Write 86H to offset BAR + 0CH.
3. Write desired value to preload register. (BAR + 00H or BAR + 04H)

General Interrupt Status Register

This register is at Base + 08H. Bit 0 is set when the first stage of down-counter reaches zero.

- Bit 0 = 0 – No Interrupt
- Bit 1 = 1 – Interrupt Active

NOTE This bit is not set in free running mode.

Reload Register

This register is at Base + 0CH. Write 1 to bit 8 will reload the down-counter's value. To prevent a timeout:

1. Write 80H to offset BAR + 0CH
2. Write 86H to offset BAR + 0CH
3. Write a '1' to RELOAD[8] of the reload register

Offset 60 – 61H: WDT Configuration Register

- Bit 5 indicates whether or not the WDT will toggle the WDT_TOUT# pin when WDT times out. (0 = Enabled, 1 = Disabled)
- Bit 2 provides two options for pre-scaling the main down-counter. (0 = 1ms – 10min, 1 = 1us – 1sec)
- Bit [1:0] allows you to choose the type of interrupt desired when the WDT reached the end of the first stage without being reset. (00 = IRQ, 01 = reserved, 10 = SMI, 11 = Disabled)

NOTE The WDT does not support SMI. IRQ uses APIC 1, INT 10 and is active low, level triggered.

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Offset 68H: WDT Lock Register

- Bit 2 chooses the functionality of the timer. (0 = Watchdog Timer mode, 1 = Free running mode) The free running mode ignores the first stage and uses only Preload Value 2. It is not necessary to reload the timer in free running mode as it is done automatically every time the down counter reaches zero.
- Bit 1 enables or disables the WDT. (0 = Disabled, 1 = Enabled)
- Bit 0 locks the values of this register until a hard reset occurs or power is cycled (0 = unlocked, 1 = locked). The default is 0.

GPIO Control Registers

Three GPIOs on the cPCI-6910 relate to the watchdog timer. The GPIO control base port is 480H.

WDT_TOUT# pin selection

The WDT_TOUT# signal is multiplexed with GPIO32. When using WDT, this signal must be switched to WDT_TOUT# function. It uses bit 0 of GPIOBASE + 30H to set WDT_TOUT function. (0 = WDT_TOUT#, 1 = GPIO32)

RESET hardware circuit selection

The GPO57 of the Intel® 6300ESB is designed to control reset circuit. When GPO57 is low, system resets according to the level of WDT_TOUT# signal. When GPO57 is high, system does not reset by WDT_TOUT#. Bit 57 of GPIOBASE + 38H determines the level of GPO57 (0 = Low, 1 = High). There already exists a setting in BIOS setup menu (Integrated Peripherals). User can set this item before programming WDT.

WDT LED Control

The GPO25 of Intel® 6300ESB is designed to control WDT LED. The cPCI-6910 features two WDT LED. WDT LED lights up or blinks.

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WDT LED light

Sets bit 25 of GPIOBASE + 04H to 0. Bit 25 of GPIOBASE + 0CH determines the state of WDT LED (0 = on, 1 = off).

WDT LED blink

Sets bit 25 of GPIOBASE + 04H to 0. Bit 25 of GPIOBASE + 18H enables the WDT LED to blink (0 = function normally, 1 = enable blinking). The high and low times have approximately 0.5 seconds each.

WDT Programming Procedure

1. Enable the Watchdog Timer option in the BIOS (Integrated Peripherals > Onboard Device).
2. Make sure that the WDT_TOUT# signal is functional (not GPIO32 function).
3. Enable the WDT output, pre-scaler, and interrupt type in the WDT configuration register.
4. Obtain control base from Base Address register.
5. Program Preload register's value according to the unlocking sequence.
6. Set the WDT timer mode in the WDT Lock Register.
7. Enable WDT from the WDT Lock register and program the WDT LED functionality.

To prevent the timer from causing an interrupt or driving WDT_TOUT#, the timer must be reloaded periodically. The frequency of reloads required is dependent on the value of the preload values. To reload the down-counter, the register unlocking sequence must be performed.

If the user wishes to disable WDT, set bit 1 of WDT Lock Register to 0.

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Utilities

ADLINK provides a demo DOS utility: `HRWDT.EXE`. It is included in the support CD. For a detailed description, run **`hrwdt /?`** under this directory:

```
X:\CHIPDRV\WDT\HRWDT
```

You can also download the Intel WDT demo windows application from Intel driver download center.

7.2 Intel® Preboot Execution Environment (PXE)

The cPCI-6910 series supports the Intel® Preboot Execution Environment (PXE) that is capable of booting up or executing an OS installation through the Ethernet ports. To use PXE, there must be a DHCP server in the network with one or more servers running PXE and MTFTP services. It could be a Windows® NT or Windows® 2000 server running DHCP, PXE, and MTFTP service or a dedicated DHCP server with one or more additional server running PXE and MTFTP service.

To build a network environment with PXE support:

1. Setup a DHCP server with PXE tag configuration.
2. Install the PXE and MTFTP services
3. Make a boot image file on the PXE server (that is the boot server).
4. Enable the PXE boot function on the client computer.

For further details, refer to **pdkrel30.pdf** file in the support CD. You may find this file in:

```
X:\Utility\PXE_PDK
```

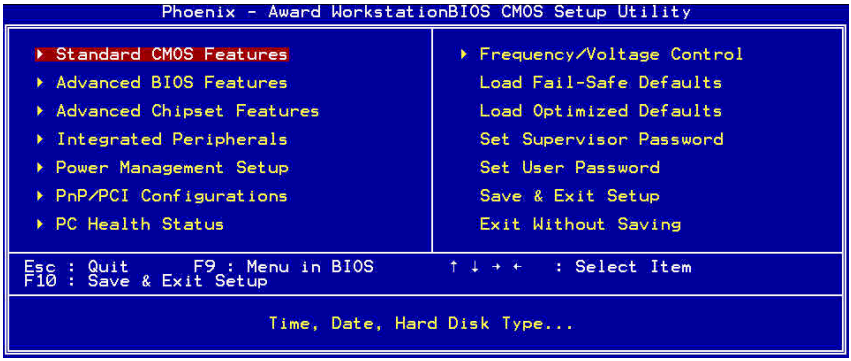
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8 BIOS Setup

The Phoenix-Award BIOS provides a setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the setup utility. When you turn on the computer, the BIOS is immediately activated. Pressing the <Del> or <Tab> key immediately allows you to enter the setup utility. If you are a little bit late pressing the <Del> or <Tab> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the setup. If you still want to enter the setup utility, restart the system by pressing the RESET button or press <Ctrl>+<Alt>+<Delete>. You may also turn the system OFF and ON again. Press <Del> when this message appears on the screen:

Press DEL to Enter Setup

The BIOS Setup main menu appears.



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8.1 Navigating Through the BIOS Menus

You can navigate the BIOS menus using the arrow keys to highlight the items, then by pressing <Enter> to select. Use the <PgUp> and <PgDn> keys to select from the options, <F1> for help, and <Esc> to exit. When you enter the setup utility, the main menu screen appears. The main menu allows you to select from various setup functions and exit choices.

The section below the setup items displays the control keys for the particular menu. Another section at the bottom of the main menu just below the control keys section displays information on the currently highlighted item in the list.

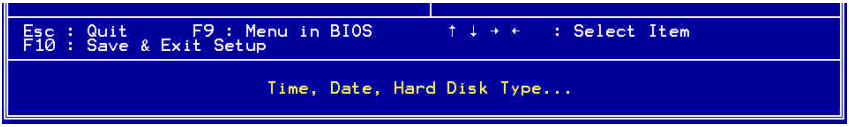


Figure 8-1: Control keys & Information Bar in Main Menu



Figure 8-2: Control keys in Sub-menu

The BIOS setup stores the CMOS settings into the non-volatile ROM by pressing <F6>/<F7> key.

NOTE

1. When the system fails to boot after adjusting and saving changes to the BIOS setup, enter the BIOS setup, load the fail-safe default, then restart the system.

2. It is strongly recommend that you avoid making any changes to chipset defaults. These default values have been configured for optimum performance and reliability.

For sub-menus, an **Item Help** section appears at the right side of the screen to describe the selected BIOS parameter and/or define the parameter's options.

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8.2 Standard CMOS Features

This menu sets the system date/time, shows basic hardware configurations present in your system, and error handling mode. Use this menu when you need to change the system hardware configurations, when the onboard battery fails, or when the configuration stored in the CMOS memory fails or gets corrupted.



Date / Time

Sets up the system date and time. To set the date/time, highlight the Date/Time fields using the arrow keys, then press the <PgUp>/<PgDn> or +/- keys to adjust the date/time.

The date format is:

Day	*Sun to Sat (read only)*
Month	*Jan to Dec*
Date	*1 to 31*
Year	*1994 to 2079*

The time format is:

Hour	*00 to 23*
Minute	*00 to 59*
Second	*00 to 59*

IDE Channel 0 Master/0 Slave/1 Master/1 Slave

Refer to section 8.2.1 for details.

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Video

Selects the type of video display card installed in your system. You may choose from the following video display cards:

EGA/VGA	*For EGA, VGA, SEGA, SVGA or PGA monitor adapters*
CGA 40	*Power up in 40 columns mode*
CGA 80	*Power up in 80 columns mode*
MONO	*For Hercules or MDA adapters*

Halt On

Determines whether or not the system halts if an error is detected during power up.

No Errors	*The system boot does not halt for any error detected.*
All Errors	*Whenever the BIOS detects a non-fatal error, the system stops and the user is prompted.*
All, But Keyboard	*The system boot does not halt during a keyboard error, but halts for all other errors.*

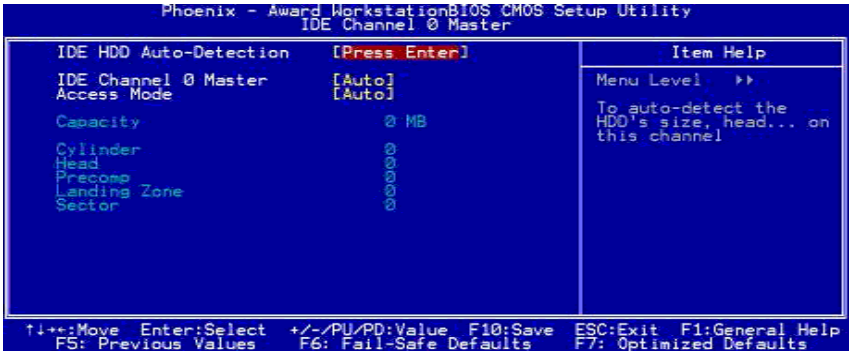
Base / Extended / Total Memory

Displays the base, extended and total system memory auto-detected by the BIOS.

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8.2.1 IDE Devices

The IDE devices sub-menu allows you to auto-detect installed storage drives or to set the HDD parameters manually.



IDE HDD Auto-Detection

Highlight this item, then press <Enter> to allow the BIOS to auto-detect installed HDDs. When auto-detection is successful, the BIOS fills-in the other parameters such as cylinder, head, pre-comp, landing zone, and sector.

IDE Channel 0 Master / 0 Slave / 1 Master / 1 Slave

Auto	*BIOS auto-detects the hard disk drive type.*
Manual	*You assign the type of hard disk drive when access mode is normal.*
None	*Select this option when no hard disk is installed.*

Access Mode

Auto	*Auto-detects the HDD mode*
Normal	*Select this for HDDs with less than 528 MB*
Large	*For MS-DOS only*
LBA	*Select this for HDDs with more than 528 MB and supports Logical Block Addressing*

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If your hard disk drive type is undetected, you can use normal access mode to manually define the drive type. The **Capacity** item is adjusted automatically according to the configuration. If you select normal access mode, related information are requested for the following parameters.

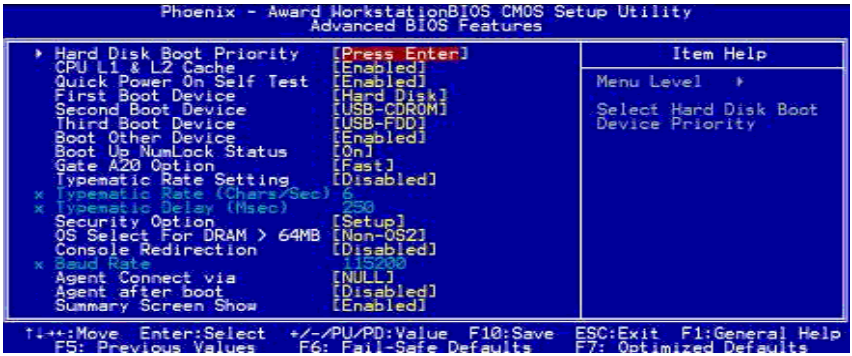
Cylinder	*Number of cylinders*
Head	*Number of read/write heads*
Precomp	*Write precompensation*
Landing Zone	*Landing zone*
Sector	*Number of sectors*

NOTE The specifications of the HDD must match with the drive table. The HDD fails if you enter incorrect information in these fields.

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8.3 Advanced BIOS Features

This menu enables you to configure advanced system configurations and enable/disable various system features.



Hard Disk Boot Priority

Allows you to select the HDD where you want to boot the system. Select this item, then press <Enter> to enter a sub-menu. The sub-menu allows you to select the HDD where you want the system to boot.

CPU L1 & L2 Cache

Enables the CPU's L1/L2 cache. Cache memory is an additional memory that is faster than conventional DRAM (system memory). x486 and latest processors has an internal and external (available on some CPUs only) cache. When the CPU requests data, the system transfers the requested data from the main memory to the cache memory for faster CPU access. Options include:

Enabled	*Open CPU L1 & L2 Cache*
Disabled	*Close CPU L1 & L2 Cache*

Quick Power On Self Test

When enabled, this field speeds up the Power On Self Test (POST). When enabled, the BIOS skips some memory and disk checking during POST.

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First/Second/Third Boot Device
Boot Other Device

Sets the device where the system boots. The BIOS loads the operating system from the devices sequentially listed in these parameters. The **First Boot Device** default is **Hard Disk**, followed by CDROM and USB-CDROM. Options include:

LS120 / Hard Disk / CDROM / ZIP100 / USB-FDD / USB-ZIP / USB-CDROM / Legacy LAN / Disabled

Boot Up NumLock Status

Sets the status of the NumLock key during bootup.

On	*Numeric keypad is used for numbers*
Off	*Numeric keypad is used for arrows*

Gate A20 Option

Selects how Gate A20 is accessed. Gate A20 is a device used to address memory above 1 MB. Options include:

Fast	*The A20 signal is controlled by chipset specific method*
Normal	*The A20 signal is controlled by keyboard controller or chipset hardware*

Typematic Rate Setting

Sets the typematic rate. When enabled, you may adjust the typematic rate (chars/sec) and typematic delay (msec). Options include:

Enabled	*Enable typematic rate and typematic delay programming*
Disabled	*Disable typematic rate and typematic delay programming. The system BIOS will use default value of these 2 items and the default controlled by keyboard*

Typematic Rate (Chars/Sec)

Sets the keystroke speeds. You can set this parameter from 6 to 30 characters per second.

Typematic Delay (Msec)

Sets the time interval between the first and second characters.

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Security Option

Limits the access to the system and/or the BIOS setup.

Setup	*The system prompts you to enter the supervisor password every time you try to access the BIOS setup*
System	*The system prompts you to enter the user password every time the system boots up*

NOTE To disable security, select PASSWORD SETTING from the main menu. When prompted for the password, leave the password field empty, then press <Enter>. When security is disabled, you can boot the system and access the BIOS setup.

OS Select for DRAM > 64 MB

This option allows the system to access greater than 64 MB of DRAM memory when used with OS/2, depending on certain BIOS calls to access memory.

Console Redirection

Allows system access without video display or keyboard. Using display/keyboard redirection, remote console allows another computer to display the system's POST messages and commands via the serial (COM) port. Default value is Enabled. For more information on serial communications, refer to the section Appendix: Using Serial Console.

NOTE Remote console is a character-based terminal application that supports either VT100 or ANSI terminals. It does not support graphics or graphical user interfaces.

Baud Rate

When **Console Redirection** is enabled, set the serial port's operating baud rate. Options include: 9600, 19200, 38400, 57600, and 115200 Kbps.

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NOTE The Baud rate setting of the cPCI-6910 and the monitoring computer must be the same. When there is difference in Baud rate, an “Award Preboot Agent Installation Failed” message appears when BIOS builds the connection between the two computers.

Agent Connect via

Selects the connection mode. The cPCI-6910 supports null mode. Null mode connects two computers using a null modem cable.

Agent after boot

Monitors text-based applications (such as DOS) after POST. Disable this option to terminate remote console after POST. This item is disabled by default.

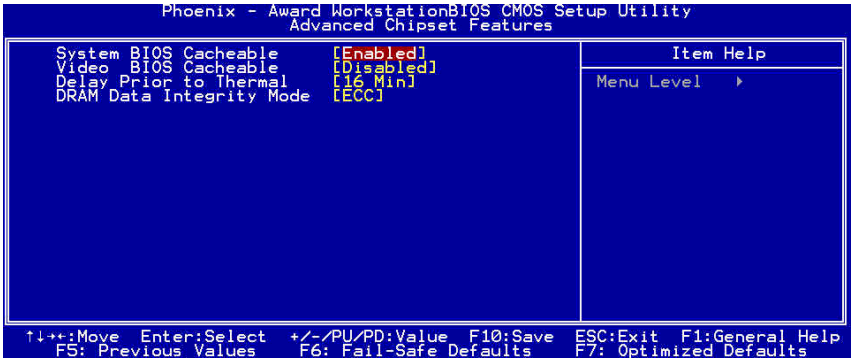
Summary Screen Show

Shows or hides the table showing system information such as CPU frequency, memory size, onboard device, and PCI devices during POST.

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8.4 Advanced Chipset Features

This setup menu controls the configuration of the chipset.



System BIOS Cacheable

When enabled, the BIOS ROM addresses at F0000H-FFFFFH is duplicated in the SRAM and works with the enabled cache controller. Options include:

Enabled	*BIOS access cached*
Disabled	*BIOS access not cached*

Video BIOS Cacheable

When enabled, the video BIOS cache causes the video BIOS addressed at C0000H to C7FFFH to be cached with the cache controller enabled. Options include:

Enabled	*Video BIOS access cached*
Disabled	*Video BIOS access not cached*

Delay Prior to Thermal

Sets a delay before enabling automatic thermal mode that activates the thermal control circuit (TCC). Thermal monitor is a feature of the Intel® Xeon® processor that allows system designers to lower the cost of thermal solutions without compromising system integrity or reliability. By using a factory-tuned, precision on-die temperature sensor, and a fast acting TCC, the processor, without the aid of any additional software or hardware, can control the pro-

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cessor's die temperature within factory specifications under typical real-world operating conditions.

Once automatic mode is activated, the TCC activates only when the internal die temperature is very near the temperature thresholds of the processor. When TCC is enabled, and the CPU is in high temperature, the clocks are modulated by maintaining a duty cycle within a range of 30% to 50%.

DRAM Data Integrity Mode

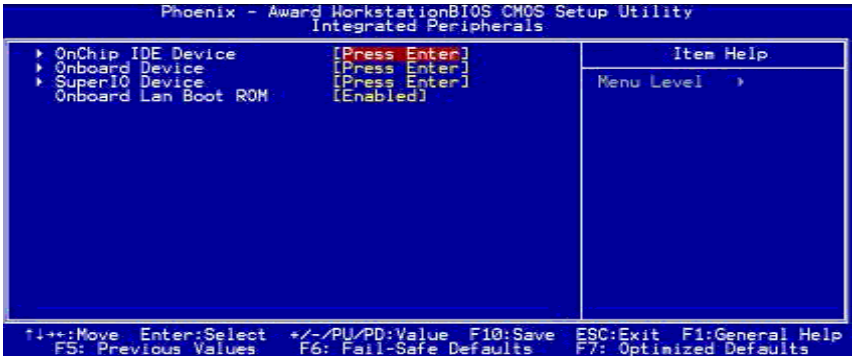
Shows the DRAM data integrity mode. This item is non-configurable.

ECC	*A 72-bit wide DRAM is installed.*
Non-ECC	*A 64-bit wide DRAM is installed.*

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8.5 Integrated Peripherals

This menu allows you to configure integrated system devices. Select an item, then press <Enter> to display the sub-menu.



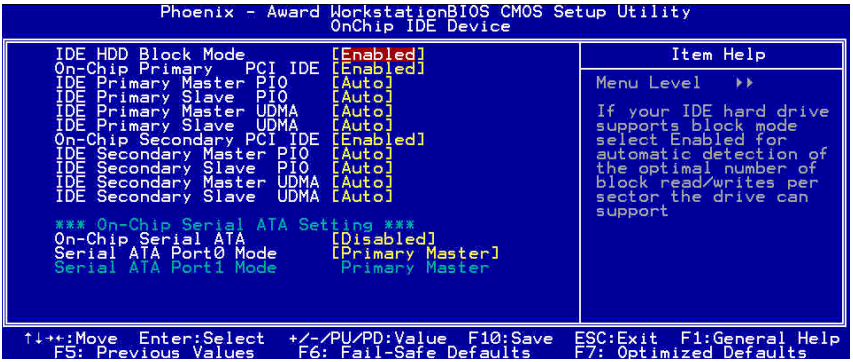
Onboard Lan Boot ROM

Allows you to enable or disable PXE support. The PXE function allows system boot from a network environment. This option is enabled by default. For additional information on the PXE function, refer to section 7.2.

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8.5.1 OnChip IDE Device

This sub-menu lets you configure advanced IDE controller configurations.



IDE HDD Block Mode

Allows the hard disk drive controller to use the fast block mode when transferring data. Options include:

Enabled	*IDE controller uses block mode*
Disabled	*IDE controller uses standard mode*

On-Chip Primary PCI IDE
On-Chip Secondary PCI IDE

The integrated peripheral controller comes with an IDE interface that supports two IDE channels. Enable these options to activate each channel separately.

IDE Primary Master PIO
IDE Primary Slave PIO
IDE Secondary Master PIO
IDE Secondary Slave PIO

Allows your system hard disk controller to perform faster. Rather than have the BIOS issue a series of commands that transfer to or from the disk drive, PIO (Programmed Input/Output) allows the BIOS to communicate with the controller and CPU directly.

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The system supports five modes, numbered 0 to 4, that differ in timing. Setting this item to **Auto** allows the BIOS to select the best available mode.

Auto	*Auto select which mode that BIOS communicates with the controller and CPU*
Mode0~Mode4	*User-defined the PIO mode*

IDE Primary Master UDMA
IDE Primary Slave UDMA
IDE Secondary Master UDMA
IDE Secondary Slave UDMA

Allows your system to improve disk I/O throughput up to 100MB/sec with the Ultra DMA/100 feature. Options include **Auto** and **Disabled**.

On-Chip Serial ATA

Sets the Serial ATA HDD mode. Options include:

Disabled	*Disables the SATA controller*
Auto	*BIOS auto-configures the SATA controller*
Combined Mode	*Combined PATA and SATA. Maximum 2 IDE drives per channel.*
Enhanced Mode	*Enables both SATA and PATA. Maximum 6 IDE drives.*
SATA Only	*SATA is operating in legacy mode.*

Serial ATA Port Mode 0
Serial ATA Port Mode 1

Sets the Serial ATA hard disk drive as Primary Master or Secondary Master device.

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8.5.2 Onboard Devices

This menu allows configuration of the USB controller.



USB2.0 Controller

Select Enabled if your system contains a Universal Serial Bus(USB) controller and you have USB peripherals. The default is Enabled.

USB Keyboard Support

Select Enabled to support USB Keyboard functionality under legacy OS such as MS-DOS. The default is Disabled.

BIOS Write Protect

To protect the BIOS from corruption or loss, this item allows BIOS data protection to avoid BIOS errors.

Disabled (Default) - User can flash BIOS anywhere.

Enabled - User can not flash the newest BIOS data.

Watch Dog Timer

cPCI-6910 has a function that enables/disables Southbridge (6300ESB) Watch Dog Function Output. The default is Disabled.

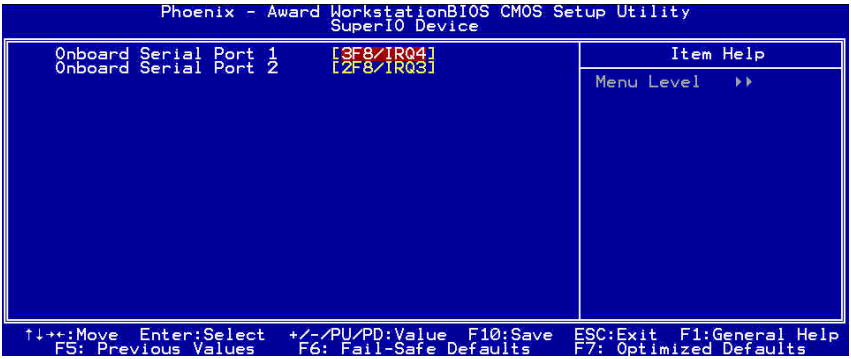
HB8 Reset

cPCI-6910 has a function that enables/disables the PCI-X to PCI-X bridge (HB8) Reset Function Output. The default is Disabled.

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8.5.3 Super IO Function Setup

The SuperIO menu lets you set the IRQ addresses of the serial ports.



Onboard Serial Port 1
Onboard Serial Port 2

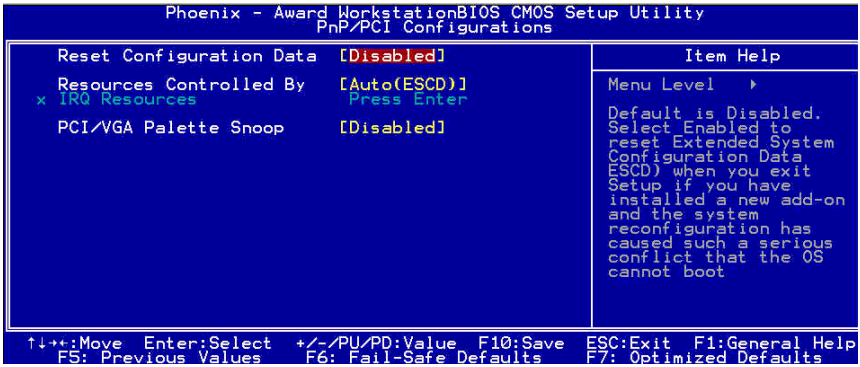
Sets the addressed of the onboard serial ports. The default values for these ports are:

Serial Port 1	*3F8 / IRQ4*
Serial Port 2	*2F8 / IRQ3*

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8.6 PnP/PCI Configuration

This menu allows to configure the PCI bus system.



Reset Configuration Data

Disabled by default. Enable this item to reset the Extended System Configuration Data (ESCD). You need to reset the ESCD when you installed a new add-on card and the system reconfiguration has caused a serious conflict that the operating system does not boot.

Resources Controlled by

The PnP BIOS automatically configures all IRQ resources for boot and compatible devices. However, this feature is available only for PnP-supported operating systems such as Windows® 98, 2000, or XP. When you set this field to **Manual**, set the IRQ resources by going into each of the submenu items that appears after this option.

Auto (ESCD))	*PnP BIOS configure all compatible devices automatically*
Manual	*User can assign IRQ & DMA to the devices*

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IRQ Resources

Sets the IRQ resource when the **Resources Controlled by** is set to **Manual**. Assign each system interrupt a type depending on the type of device using the interrupt.

PCI/VGA Palette Snoop

Some non-standard VGA display cards may not show colors properly. This field allows you to specify whether MPEG ISA/VESA VGA cards can work with PCI/VGA or not.

Enabled	*PCI/VGA can work with MPEG ISA/VESA VGA card*
Disabled	*PCI/VGA can not work with MPEG ISA/VESA VGA card*

8.7 Frequency/Voltage Control



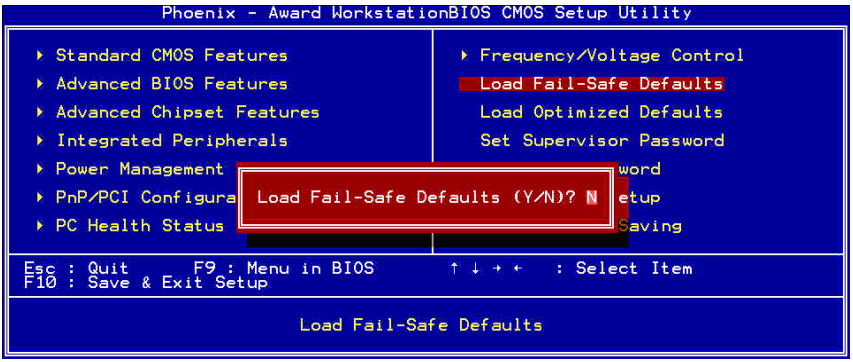
Spread Spectrum

This item allows you to enable or disable the spread spectrum.

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8.8 Load Fail-Safe Defaults

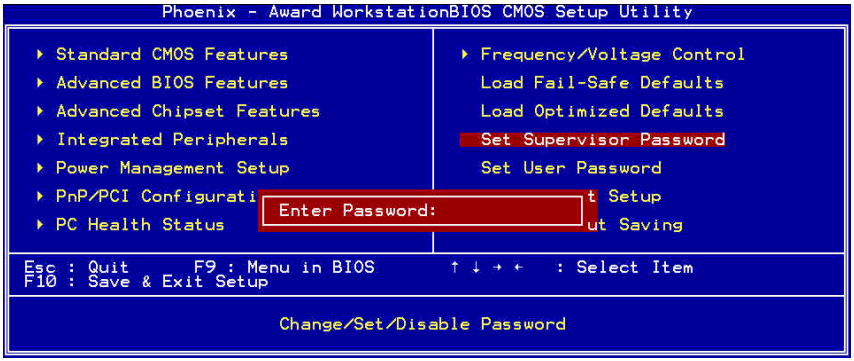
This option allows you to load the default values permanently stored in the BIOS ROM. These values are not optimized and disables all high-performance features.



To load the fail-safe default values, select **Load Fail-Safe Defaults**, press <Enter>, press <Y>, then press <Enter>.

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8.9 Setting the Supervisor and User Passwords



You may set the supervisor and user passwords using these options. The **Supervisor Password** protects the system from unauthorized access. When set, the system prompts every user to enter the correct password every time the system boots up. The User Password prevents unauthorized access to the BIOS setup.

To set the supervisor/user password:

1. Select **Set Supervisor Password/Set User Password**, then press <Enter>. The **Enter Password** window appears.
2. Key-in the password (up to eight characters), then press <Enter>.
3. When prompted, key-in the password again, then press <Enter> to confirm. The screen returns to the main menu.

To disable the supervisor/user password:

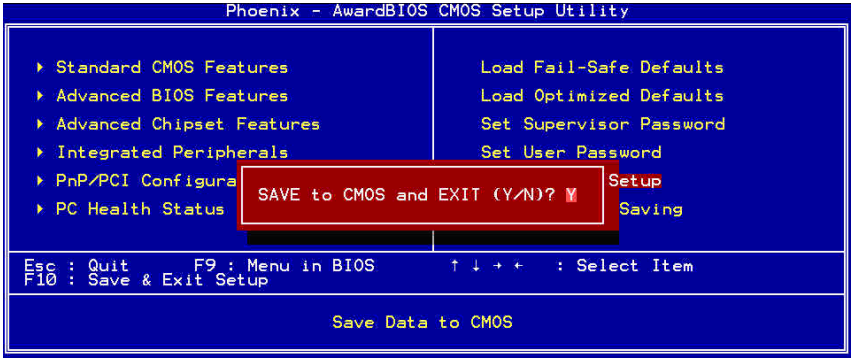
1. Select **Set Supervisor Password/Set User Password**, then press <Enter>. The **Enter Password** window appears.
2. Press <Enter>. A confirmation message appears telling you that the password has been disabled. The screen returns to the main menu.

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8.10 Saving and Exiting the BIOS Setup

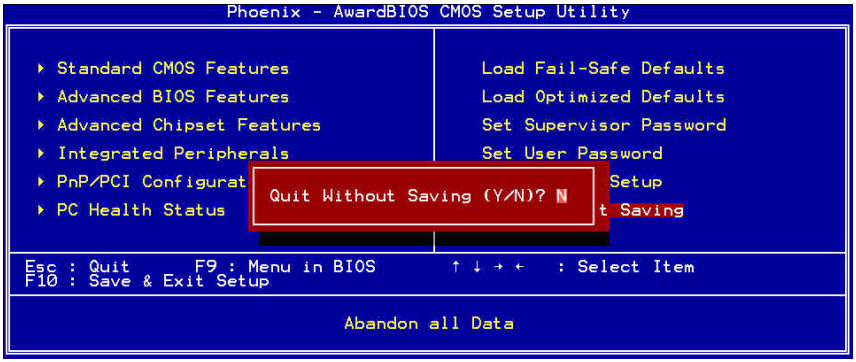
Save & Exit Setup

Select this option when you want to save the changes to the CMOS before exiting. When prompted, type <Y> to accept the changes and exit the setup. Type <N> to ignore the changes and return to the main menu.



Exit Without Saving

Allows you to ignore the changes made to the BIOS setup. Select this option, then press <Y> to exit the setup without saving the changes. Type <N> to return to the main menu.



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9 IPMI Interface

9.1 Audience

This section is intended for users with a basic understanding of the the newest BMC implementation in the IPMI specification rev. 1.0 and describes some OEM extension IPMI commands' usages which are not listed in the IPMI specification. This section also has a short revision history of the firmware.

9.2 BMR-AVR-cPCI Command Summary

The following table lists all the commands supported by the BMR-AVR-cPCI. The right most column indicates if a particular command is required by PICMG® 3.0 and 2.9 or if it is optional.

Command	IPMI Spec	NetFn	CMD	IPM Controller Req (PICMG 3.0/PICMG 2.9)
IPM Device "Global" Commands				
Get Device ID	17.1	App	01h	Mandatory/Mandatory
Cold Reset	17.2	App	02h	Optional/Optional
Warm Reset	17.3	App	03h	Optional/Optional
Get Self Test Results	17.4	App	04h	Mandatory/Mandatory
Get Device GUID	17.8	App	08h	Optional/Optional
Broadcast "Get Device ID"	17.9	App	01h	Mandatory/Mandatory
IPMI Messaging Support Commands				
Send Message	18.7	App	34h	Optional
BMC Watchdog Timer				
Reset Watchdog Timer	21.5	App	22h	Mandatory/Optional
Set Watchdog Timer	21.6	App	24h	Mandatory/Optional
Get Watchdog Timer	21.7	App	25h	Mandatory/Optional
Event Commands				
Set Event Receiver	23.1	S/E	00h	Mandatory/Optional
Get Event Receiver	23.2	S/E	01h	Mandatory/Optional
Platform Event (a.k.a. "Event Message")	23.3	S/E	02h	Mandatory/Optional
Sensor Device Commands				

Table 9-1: Commands Supported by BMR-AVR-cPCI

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Command	IPMI Spec	NetFn	CMD	IPM Controller Req (PICMG 3.0/PICMG 2.9)
Get Device SDR Info	29.2	S/E	20h	Mandatory/Optional
Get Device SDR	29.3	S/E	21h	Mandatory/Optional
Reserve Device SDR Repository	29.4	S/E	22h	Mandatory/Optional
Set Sensor Hysteresis	29.6	S/E	24h	Optional/Optional
Get Sensor Hysteresis	29.7	S/E	25h	Optional/Optional
Set Sensor Threshold	29.8	S/E	26h	Optional/Optional
Get Sensor Threshold	29.9	S/E	27h	Optional/Optional
Set Sensor Event Enable	29.10	S/E	28h	Optional/Optional
Get Sensor Event Enable	29.11	S/E	29h	Optional/Optional
Get Sensor Event Status	29.13	S/E	2Bh	Optional/Optional
Get Sensor Reading	29.14	S/E	2Dh	Mandatory/Optional
Get Sensor Type	29.16	S/E	2Fh	Optional/Optional
FRU Device Commands				
Get FRU Inventory Area Info	28.1	Storage	10h	Mandatory/Optional
Read FRU Data	28.2	Storage	11h	Mandatory/Optional
Write FRU Data	28.3	Storage	12h	Mandatory/Optional

Table 9-1: Commands Supported by BMR-AVR-cPCI

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9.3 OEM Commands Summary Table

Command	NetFn Code	Cmd Code
OemShowRevision	OEM (30h)	12h
OemRescanGaInput	OEM (30h)	22h
OemTestFunction	OEM (30h)	30h
OemReportGeoAddress	OEM (30h)	F0h
OemEnableSmbus	OEM (30h)	F2h
OemDisableSmbus	OEM (30h)	F3h
OemDispDebugVariable	OEM (30h)	F4h
OemResetHost	OEM (30h)	F5h
OemPowerOff	OEM (30h)	F6h
OemPowerOn	OEM (30h)	F7h

Table 9-2: OEM Commands Summary Table

OemShowRevision

Shows the current information of the firmware including the firmware revision, product ID, and additional features.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	12h	OEM defined command
Response	0	Complete Code	00h means OK
	1	A5h	Internal check byte. Always A5h
	2	*Firmware Rev	‘V’ in ASCII code for verification
	3	*Firmware Rev	Revision info high byte
	4	*Firmware Rev	Revision info low byte
	5	*Product ID	‘P’ in ASCII code for verification
	6	*Product ID	Product info high byte
	7	*Product ID	Product info low byte
	8	*Special Info	‘S’ in ASCII code for verification
	9	*Special Info	Additional info byte
	10	5AH	Internal check bye. Always 5AH

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OemRescanGaInput

Re-scans the geo-address input pins and reset the IPMB address according the input value.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	22h	OEM defined command
Response	0	Complete Code	00h means OK
	1	New IPMB address	New IPMB address value

OemTestFunction

Internal test purposes only.

OemReportGeoAddress

This command can report the IPMB address, the GA pin input status, and the event forwarding control value.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F0h	OEM defined command
Response	0	Complete Code	00h means OK
	1	IPMB address	IPMB address value
	2	GA value	GA pin input status
	3	Control value	Current control value of event forwarding

OemEnableSmbus

Turns the I2C bus on when it is off during boot-up. BIOS usually performs this command after booting on boards with ServerWorks chipset.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F2h	OEM defined command

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Action	Byte	Value	Description
Response	0	Complete Code	00h means OK

OemDisableSmbus

This command is used to shut down the I2C bus accessing.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F3h	OEM defined command
Response	0	Complete Code	00h means OK

OemDispDebugVariable

This command can report up to 5 interval value for the debug purpose one time. For developer only.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F4h	OEM defined command
Response	0	Complete Code	00h means OK
	1	*Debug variable 1	
	2	*Debug variable 2	
	3	*Debug variable 3	
	4	*Debug variable 4	
	5	*Debug variable 5	

OemResetHost

This command is implement to control the system's status if rebooting is required. Operators can control the system from remote.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F5h	OEM defined command
Response	0	Complete Code	00h means OK

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OemPowerOff

This command is implement to control the system's status if power off is required. Operators can control the system from remote.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F6h	OEM defined command
Response	0	Complete Code	00h means OK

OemPowerOn

This command is implement to control the system's status if power on is required. Operators can control the system from remote.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F7h	OEM defined command
Response	0	Complete Code	00h means OK

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9.4 CompactPCI® Address Map

Since you may insert more than one system in a single chassis, we allocate their IPMB addresses based on GA input as peripheral cards. The CompactPCI® Peripheral Address Mapping Table is provided below.

Geo Address	IPMB Address	Geo Address	IPMB Address
0	Disabled	16	D0h
1	B0h	17	D2h
2	B2h	18	D4h
3	B4h	19	D6h
4	B6h	20	D8h
5	B8h	21	DAh
6	BAh	22	DCh
7	BCh	23	DEh
8	BEh	24	E0h
9	C0h	25	E2h
10	C4h	26	E4h
11	C6h	27	E6h
12	C8h	28	E8h
13	CAh	29	EAh
14	CCh	30	ECh
15	CEh	31	Disabled

Table 9-3: CompactPCI Address Map

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9.5 IPMI Sensors List

cPCI-6910 B2 and earlier versions

Sensor Number	Sensor name	Normal Reading
01h	BMC Watchdog	
02h	3.3 V	3.3 V
03h	5 V	5 V
04h	CPU Temp.	40 °C
05h	System Temp.	25 °C

cPCI-6910 B3 and future versions

Sensor Number	Sensor name	Normal Reading
01h	BMC Watchdog	3.3 V
02h	3.3 V	3.3 V
03h	5 V	5 V
04h	12 V	12 V
05h	CPU Temp.	40 °C
06h	System Temp.	25 °C
07h	Power Failure	High
08h	Power Good	Low

9.6 Firmware Revision History

Revision	Description
Revision 1.3.5	Initial Release
Revision 1.3.6	Added Boot loader support to upgrade firmware
	Modified CPU and Sys temp thresholds in sensor data
	Modified GA first and last pin
	Removed Hot Swap and IPMB logic sensor

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Revision	Description
Revision 1.3.7	Disabled sensor function at OS shutdown and Fixed BMC watchdog hardware reset command
	Added support for CMM power on/off/reset command for Intel CMM ZT7102
	Fixed the IPMB address error for Intel® Chassis MPCHC5091AC
	Fixed the ipmb_status error on the Get_Self_Test_Results command
	Removed first BD_SEL check for Intel® chassis
	Fixed soft-I2C access EEPROM address error
	Modified watchdog function to support system shut-down
Revision 2.3.5	Added 12 V sensor
	Added 12 V voltage when backplane does not have 12 V
	Added CMM_Select Function
	Detected Hot Swap LSTAT pin
	Detected power failure function (GATE_FAULT and GATE_PWRGD pin)

NOTE: Revisions 1.X are for B2 and earlier versions. Revisions 2.3.X are for B3 and future versions.

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9.7 Known Issues

Timestamp resets after the system is powered up

No real time clock (RTC) is built in the BMC of the IPMI solution. This is the reason why the internal clock resets after the system is powered on.

SDR records read-only

The hardware design stores all SDR in the Flash ROM. Flash ROM may not be accessed randomly.

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Appendix: Using Serial Console

10.1 Introduction

Most industrial implementations use wired network or direct cable as an interface between the user and the computer. This product comes with a serial console redirection function that allows a remote computer to display the Power-On Self Test (POST) messages from the system and to execute commands via the serial port. This feature is integrated in the BIOS.

NOTE Serial Console is a character-based terminal application. It supports either VT100 or ANSI terminals. It does not support graphics or graphical user interfaces. Serial Console is referred to as Award Preboot Agent by Phoenix Technologies Ltd.

10.2 Before Using Serial Console

Before using serial console, check if you have the following items/ setup:

- Server computer with an Award Preboot Agent BIOS.
- Client computer with a VT100 or ANSI terminal utility or application.
- Direct connection cable.

Client computers obtain POST information from the server computer via a direct connection cable. The system must have the Award Preboot Agent BIOS to support Serial Console. Setup is required as explained below.

To use serial console, a VT100 or ANSI-compatible terminal or application is required. This must be executed at the client computer to receive the data from server computer. In this section, Windows HyperTerminal application is used as the terminal console.

A null-modem cable is used to connect the client with the server computer. It connects two serial ports from the client computer to the server computer. The null-modem pin routing illustration is provided.

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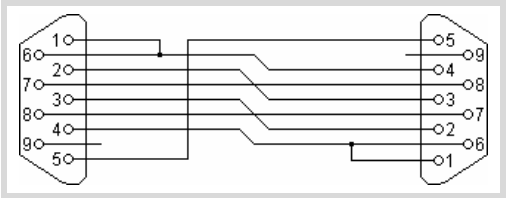


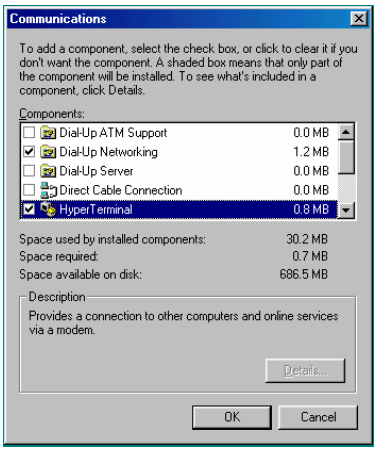
Figure 10-1: Null Modem Connection

Setting up the Server Computer

The server computer used in the following guide is a CPU board with an Award Preboot Agent integrated in the BIOS. To support serial console, the BIOS parameters must be adjusted accordingly. When you turn on the computer, enter the BIOS setup, then go to the **Advanced BIOS Features** menu. Refer to section 8.3 for details.

Using Serial Console with HyperTerminal

HyperTerminal is a console utility included in Windows operating systems such as Windows® 98/NT/2000. Other console utilities may also be used for remote controlling. If HyperTerminal is not installed in your system, use the **Add/Remove Program Properties** in the **Control Panel** to install. Check the **HyperTerminal** item, then click on **OK** to install.

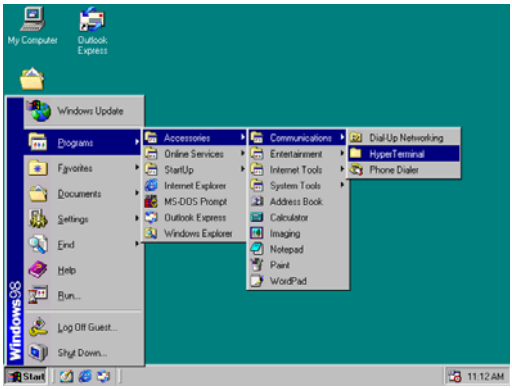


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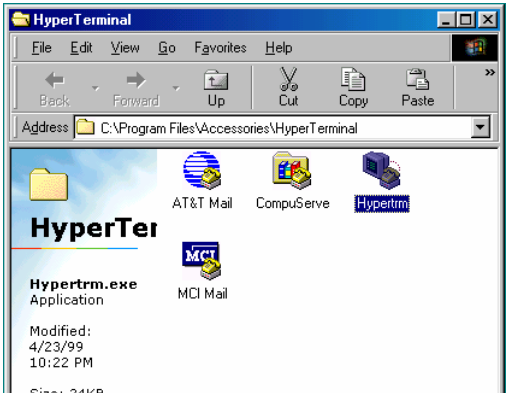
To use HyperTerminal:

NOTE The following illustrations use HyperTerminal under Windows® 98 SE operating system.

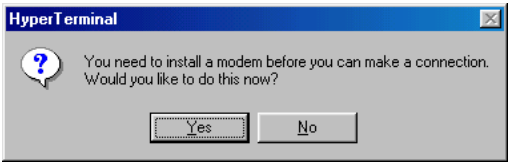
1. Click **Start** > **Accessories** > **Communications** > **HyperTerminal**.



2. Double-click on the HyperTerminal icon.

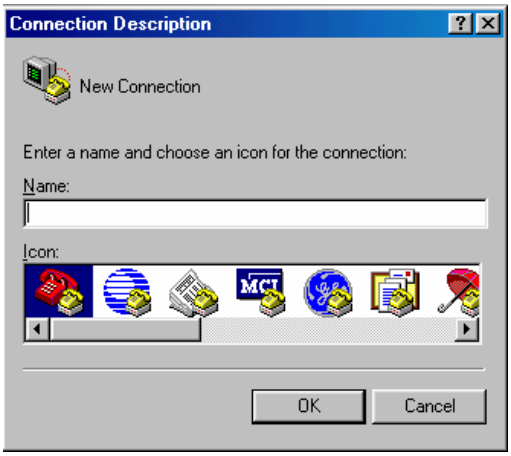


3. When prompted to install a modem before running HyperTerminal, click **No**.



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4. When the **Connection Description** window appears, key-in a name for the serial connection, click on , then click **OK**.

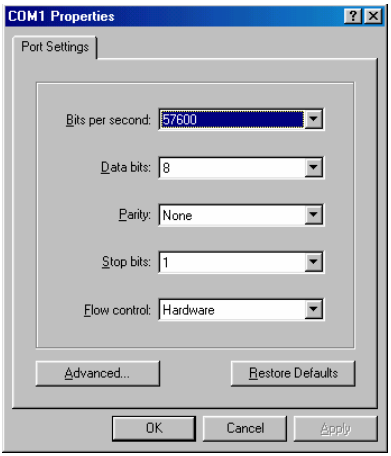


5. After building the connection node, select the serial port that will connect to the server computer from the **Connect using:** field, then click **OK**.

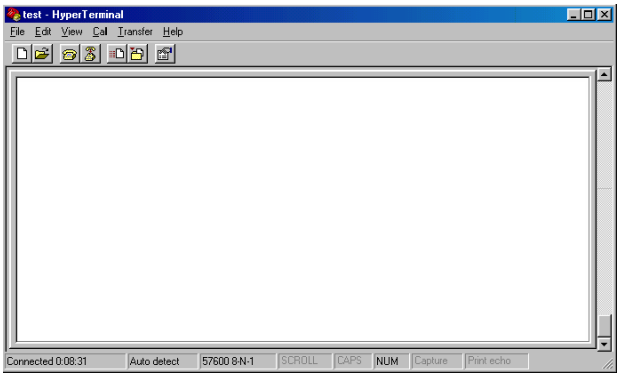


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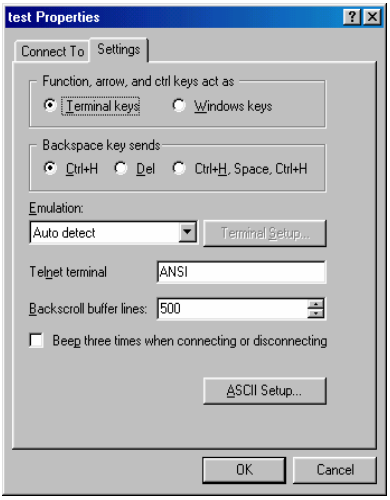
6. When the serial port's properties window appears, set the **Bits per second** (Baud rate) the same as with the server computer's Baud rate, click on **Apply**, then click **OK**.



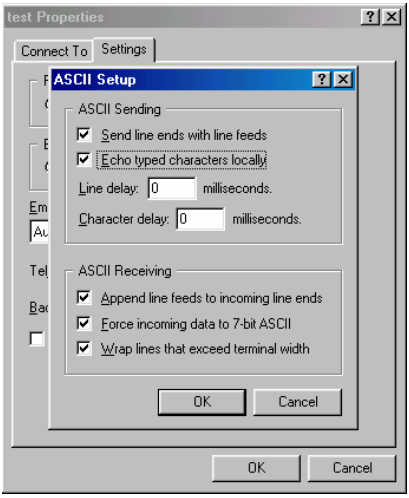
7. The HyperTerminal main window appears. Click **File** > **Properties** to adjust the connection properties.



8. From the connection Properties window, click the **Settings** tab, then check if the Telnet terminal mode is set to ANSI. When finished, click the **ASCII Setup** button.



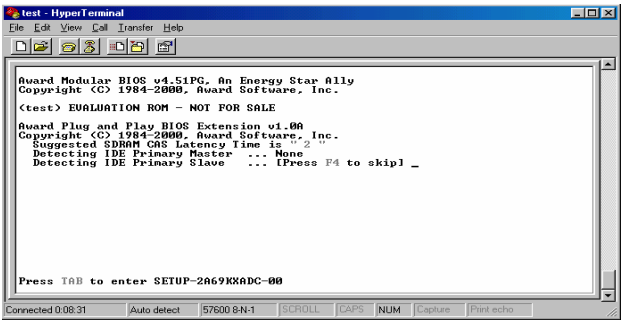
9. To echo the data that the client computer sends, check all options in the ASCII Setup window, then click **OK**.

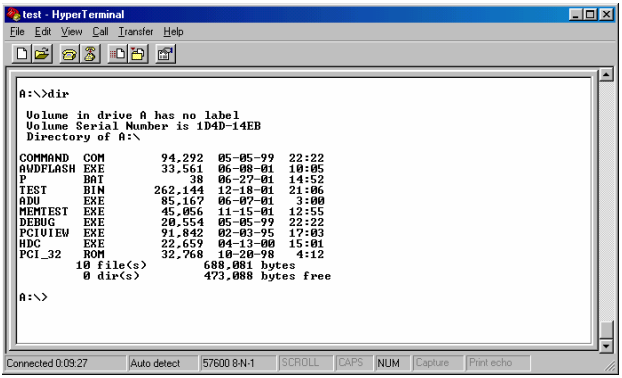


10. When HyperTerminal is properly set up and the serial cable is properly connected, power on the server com-

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puter. The POST messages of the server computer is displayed in the HyperTerminal console.





11. After the server computer enters the OS, execute commands through the HyperTerminal console.

10.3 Performing Operations in the HyperTerminal Console

The <DEL>, <ESC>, <Page Up>, <Page Down>, <Up Arrow>, <Down Arrow>, <Left Arrow>, and <Right Arrow> keys may not be recognized by the server computer's BIOS through the HyperTerminal console. Use the following key sequences to perform these operations.

Function Key/Operation	Key Sequence
HOME	ESC [1 ~

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Function Key/Operation	Key Sequence
INS	ESC [2 ~
DEL	ESC [3 ~
END	ESC [4 ~
ESC	ESC ESC
PG UP	ESC [5 ~
PG DOWN	ESC [6 ~
UP ARROW	ESC [A
DOWN ARROW	ESC [B
RIGHT ARROW	ESC [C
LEFT ARROW	ESC [D
Reboot system	ESC C

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Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.
- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

A Lithium-type battery may be provided for uninterrupted, backup or emergency power.



Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

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- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

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Warranty Policy

Thank you for choosing ADLINK. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. Before using ADLINK's products please read the user manual and follow the instructions exactly. When sending in damaged products for repair, please attach an RMA application form which can be downloaded from: http://rma.adlinktech.com/policy/

2. All ADLINK products come with a limited two-year warranty, one year for products bought in China:
   - The warranty period starts on the day the product is shipped from ADLINK's factory.
   - Peripherals and third-party products not manufactured by ADLINK will be covered by the original manufacturers' warranty.
   - For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ADLINK is not responsible for any loss of data.
   - Please ensure the use of properly licensed software with our systems. ADLINK does not condone the use of pirated software and will not service systems using such software. ADLINK will not be held legally responsible for products shipped with unlicensed software installed by the user.
   - For general repairs, please do not include peripheral accessories. If peripherals need to be included, be certain to specify which items you sent on the RMA Request & Confirmation Form. ADLINK is not responsible for items not listed on the RMA Request & Confirmation Form.

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3. Repair service is not covered by ADLINK's two-year guarantee in the following situations:
   - ▶ Damage caused by not following instructions in the User's Manual.
   - ▶ Damage caused by carelessness on the user's part during product transportation.
   - ▶ Damage caused by fire, earthquakes, floods, lightening, pollution, other acts of God, and/or incorrect usage of voltage transformers.
   - ▶ Damage caused by inappropriate storage environments such as high temperatures, high humidity, or volatile chemicals.
   - ▶ Damage caused by leakage of battery fluid during or after change of batteries by customer/user.
   - ▶ Damage from improper repair by unauthorized technicians.
   - ▶ Products with altered and/or damaged serial numbers are not entitled to our service.
   - ▶ This warranty is not transferable or extendable.
   - ▶ Other categories not protected under our warranty.

4. Customers are responsible for all fees necessary to transport damaged products to ADLINK.

5. To ensure the speed and quality of product repair, please download an RMA application form from our company website: http://rma.adlinktech.com/policy/ Products with attached RMA forms receive priority.

For further questions, please e-mail our FAE staff: service@adlinktech.com.

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