ETX 802
Computer On Module
Reference Manual

P/N 5001789A Revision A

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Notice Page

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Audience Assumptions

This reference manual is for the person who designs computer related equipment, including but not limited to hardware and software design and implementation of the same. Ampro Computers, Inc. assumes you are qualified in designing and implementing your hardware and its related software into your prototype computer equipment.

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Chapter 1 About This Manual

Purpose of this Manual

This manual is for designers of systems based on the ETX 802 computer on module. This manual contains information that permits designers to create an embedded system based on specific design requirements.

Information provided in this reference manual includes:

- ETX 802 Specifications
- Environmental requirements
- Major integrated circuits (chips) and features implemented
- ETX 802 connector/pin numbers and definition
- BIOS Setup Utility information

Information not provided in this reference manual includes:

- Detailed chip specifications
- Internal component operation
- Internal registers or signal operations
- Bus or signal timing for industry standard busses and signals

Reference Material

The following list of reference materials may be helpful for you to complete your design successfully. Most of this reference material is also available on the Ampro web site in the Embedded Design Resource Center. The Embedded Design Resource Center was created for embedded system developers to share Ampro's knowledge, insight, and expertise gained from years of experience.

Specifications

- ETX Component SBC™ Specification Revision 2.6, 2001
- ETX Component SBC™ Design Guide, Revision 1.5, 2001

  For latest revision of the ETX specifications, contact the Working Group, at:

  Web site: http://www.etx-ig.org

- PCI 2.2 Compliant Specifications

  For latest revision of the PCI specifications, contact the PCI Special Interest Group Office at:

  Web site: http://www.pcisig.com

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Major Integrated Circuit (Chip) Specifications used on the ETX 802 board:

- Intel® Corporation and the Pentium® M or Celeron® M processors used for the embedded CPU

  Web site: http://www.intel.com/design/mobile/datashts/252612.htm = Pentium M

  Web site: http://www.intel.com/design/intarch/datashts/301753.htm = Celeron M

- Intel Corporation and the 82855GME and 82801DBM chips used for the Memory Hub/Video controller and I/O Hub respectively.

  Web site: http://www.intel.com/design/chipsets/mobile/855gme.htm = Memory Hub

  Web site: http://www.intel.com/design/mobile/datashts/252337.htm = I/O Hub

- Standard Microsystems Corp's chip, LPC47B272, used for the Super I/O controller.

  Web site: http://www.smsc.com/main/datasheets/47b27x.pdf

- Realtek Semiconductor, Corp's chip ALC202A, used for the AC'97 Audio CODEC.

  Web site: http://www.realtek.com.tw/products/products.aspx

- Intel Corporation and the chip, 82551QM, used for the Ethernet controller.

  Web site: http://developer.intel.com/design/network/datashts/82551QM_DS.htm

- ITE Tech Inc. and the chip, ITE8888G, PCI to ISA Bridge.

  Web site: http://www.ite.com.tw/product_info/PC/Brief-IT8888_2.asp

NOTE	If you are unable to locate the datasheets using the links provided, go to the manufacturer's web site where you should be able to perform a search using the chip datasheet number or name listed, including the extension, htm, pdf, etc.

Related Ampro Products

The following items are directly related to successfully using the Ampro product you have just purchased or plan to purchase. Ampro highly recommends that you purchase and utilize an ETX 802 QuickStart Kit for ease of operation and development.

ETX 802 Support Products

- ETX 802 QuickStart Kit (QSK)

  The QuickStart Kit includes the ETX 802 module, SODIMM, an ETX baseboard, and the ETX 802 Documentation and Support Software (Doc & SW) CD-ROM.

- ETX 802 Documentation and Support Software CD-ROM

  The ETX 802 Documentation and Support Software (ETX 802 Doc & SW) CD-ROM is provided with the ETX 802 QuickStart Kit. The CD-ROM includes all of the ETX 802 documentation, including this reference manual and the ETX 802 QuickStart Guide in PDF format, software utilities, board support packages, and drivers for the unique devices used with Ampro supported operating systems.

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Other Ampro ETX Products

- ETX 700 – This high-performance, compact, rugged Computer-on-Module (COM) solution uses Intel 650 MHz Low Voltage Celeron or 400 MHz Ultra Low Voltage Celeron CPUs with up to 512 kB Level 2 Cache on board. This ETX module comes with the standard peripherals, including dual Ultra/DMA 33/66/100 IDE, floppy drive interface, PCI bus, ISA bus, serial, parallel, PS/2 keyboard and mouse interfaces, 10/100BaseT Ethernet, USB ports, AGP 4X video interface with up to 32 MB UMA Frame Buffer that supports built-in LVDS at 1600x1200 resolution, and AC'97 sound. It also supports up to 512 MB of SODIMM DRAM on a 50% thicker PCB to meet your custom baseboard needs.

Other Ampro Products

- CoreModule™ Family – These complete embedded-PC subsystems on single PC/104 or PC/104-Plus form-factor (3.6"x3.8") modules feature 486, Celeron, or Celeron M CPUs. Each CoreModule includes a full complement of PC core logic functions, plus disk controllers, and serial and parallel ports. Most modules also include CRT and flat panel graphics controllers and/or an Ethernet interface. The CoreModules also come with built-in extras to meet the critical reliability requirements of embedded applications. These include onboard solid state disk compatibility, watchdog timer, and smart power monitor.

- LittleBoard™ Family – These high-performance, highly integrated single-board computers use the EBX form factor (5.75"x8.00"), and are available with the Intel Pentium M, Celeron M, Pentium III, or Celeron processors. The EBX-compliant LittleBoard single-board computers offer functions equivalent to a complete laptop or desktop PC system, plus several expansion cards. Built-in extras to meet the critical requirements of embedded applications include onboard solid state disk capability, watchdog timer, and smart power monitor.

- MightyBoard™ Family – These low-cost, high-performance single-board computers (SBC) use the Mini-ITX form factor (6.75"x 6.75") and are available with Intel Celeron M or Pentium M processors. MightyBoard products offer the equivalent functions of a complete laptop or desktop PC system, including DDR memory, high performance graphics, USB 2.0, Gigabit Ethernet, plus standard PCI expansion capability in one card slot.

- MiniModule™ Family – This line of peripheral interface modules, compliant with PC/104, PC/104-Plus, and/or PCI-104 form factor (3.6"x3.8") standards can be used with Ampro's CoreModule, LittleBoard, and ReadyBoard single board computers (SBCs) to expand the I/O configuration of embedded systems. Ampro's highly reliable MiniModule products add value to existing designs by adding I/O ports, such as IEEE 1394 (FireWire), or by adding support for legacy boards, such as a PCI to ISA bridge adapter board.

- ReadyBoard™ Family – These low-cost, high-performance single-board computers (SBC) use the EPIC form factor (4.5"x6.5") and are available with the Intel Pentium III, Celeron, Pentium M and Celeron M processors. ReadyBoard products offer functions equivalent to a complete laptop or desktop PC system with standard PC-style connections, and features such as DDR or DDR2 memory, high performance graphics, USB 2.0, Ethernet and Gigabit Ethernet ports, AC'97 Audio, plus several expansion cards. Ampro also includes such features as watchdog timer, battery-free boot, a customizable splash screen, Oops! jumper (BIOS recovery), and serial console.

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Chapter 2 Product Overview

This introduction presents general information about the ETX Architecture and the ETX 802 Computer On Module (COM). After reading this chapter you should understand:

- ETX Computer On Module concept
- ETX 802 architecture
- ETX 802 features
- Major components
- Connectors
- Specifications

ETX Computer On Module Concept

Embedded system designers face increasing pressure to bring products to market quickly. Many products that once incorporated a custom CPU design can no longer afford the time to develop and debug a custom CPU let alone port operating system software to it. Furthermore, CPU subsystem design usually plays a small part in providing any uniqueness to an embedded product. The remainder of the embedded product design adds key logic elements that provide a unique product and differentiate it from other products serving the same market. The challenge is to speed these designs to market by eliminating the need for a custom CPU design while providing the flexibility to include all critical elements, which make the embedded product unique.

The Embedded Technology eXtended (ETX) module provides an off-the-shelf CPU subsystem that can be included in virtually any embedded system. ETX modules work like a high-integration chip, plugging into your custom circuit board design to provide specific control for your logic application. See Figure 2-1.

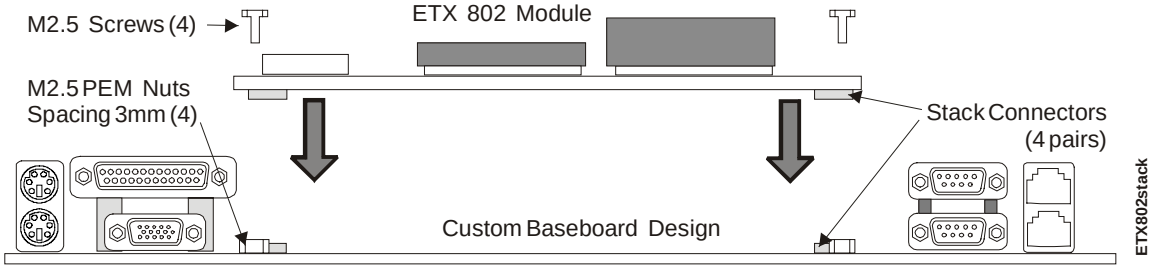


Figure 2-1. ETX 802 Stacked on Custom Baseboard

ETX provides a simple, standard interface that is independent of CPU type. The ETX interface includes the industry-standard PCI bus, ISA bus, I/O signals from the peripheral components on the ETX module, power, and ground. The ETX modules support Intel architecture (x86) processors. Go to the Ampro web site (www.ampro.com) for the latest ETX processor support information.

The standard ETX interface lets you try different processors and different processor types in your actual product environment with the ability to defer a processor choice until late in the project if you so choose. The interface also lets you easily offer different versions of your product with different capabilities by either selecting different ETX modules with the same baseboard, or by designing different baseboards for the same CPU. This simple ability to upgrade by either selecting a more powerful CPU (without baseboard redesign) or enhancing the baseboard without touching the CPU subsystem or the bulk of the applications software.

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The ETX flexibility enables designers to take an accelerated, low risk path with proven ETX module designs. Your design flow might look similar to the one shown in Figure 2-2. This diagram gives a Typical Design Flow of hardware and software functions.

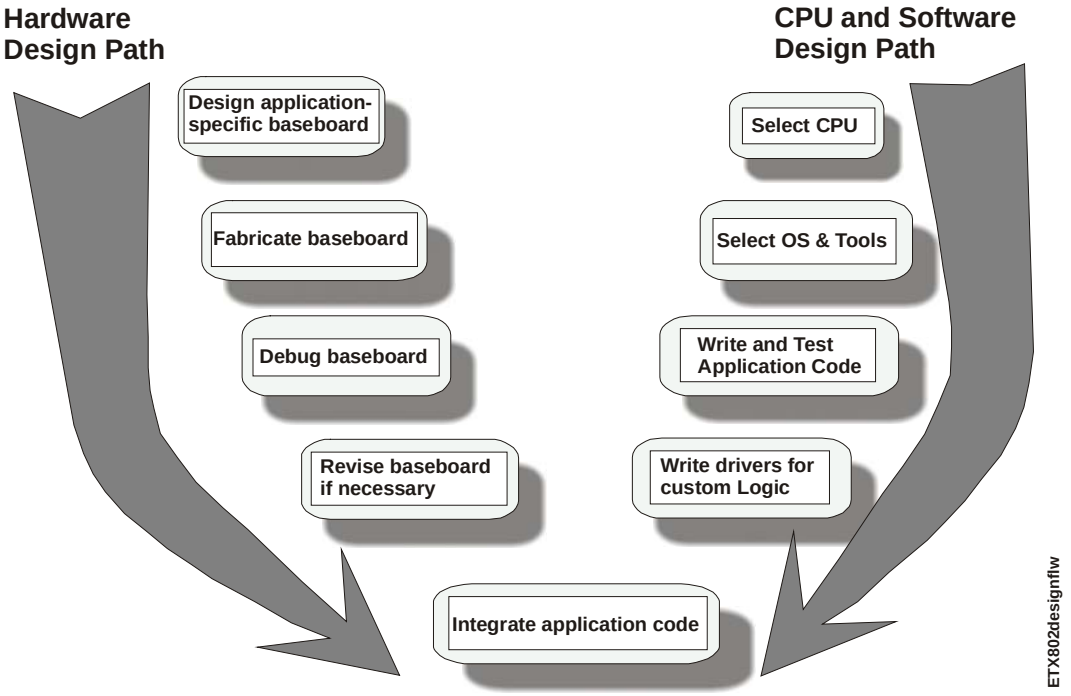


Figure 2-2. Typical Design Flow

Product Description

The ETX 802 is an exceptionally high integration, high performance, rugged, and high quality Computer-on-Module (COM), which contains all the component subsystems of an ATX motherboard plus the equivalent of up to 2 expansion boards. The ETX 802 is based on one of the ultra high performance, high-integration Intel Pentium M or Celeron M processors, and gives designers the choice of a complete, high performance, rugged, embedded processor based on the ETX form factor that conforms to the ETX V2.7 specification. The module plugs into a custom baseboard, which has connectors and additional circuitry to meet your application requirements.

Each ETX 802 incorporates an Intel® 855GME chipset (82855GME + 82801DBM) for the Memory and Graphics Hub (Northbridge) and I/O Hub (Southbridge) controllers. This includes the Intel 82855GME Memory and Graphics Hub (Northbridge), which controls graphics and memory interface and the Intel 82801DBM I/O Hub (Southbridge) Controller for some I/O functions. A Super I/O chip by Standard Microsystems Corp. provides most of the I/O functions including a PCI to ISA Bridge chip for ISA functions. Together these chips provide two Ultra/DMA 33/66/100 IDE controllers supporting two IDE drives each, floppy, four USB 2.0 ports, two serial ports, an EPP/ECP parallel port, PS/2 keyboard and mouse interfaces, and an audio AC'97 controller on the module. The ETX 802 also supports an Ethernet controller (10/100BaseT), up to 1 GB of DDR RAM in a single 200-pin DDR SODIMM socket, and a 128-bit graphics controller, which provides CRT (VGA) and flat panel video interfaces.

The ETX 802 is particularly well suited to either embedded or portable applications and meets the size, power consumption, temperature range, quality, and reliability demands of embedded system applications. The ETX 802 requires a single +5V power supply.

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Board Features

- CPU features
  - 1.4 GHz Low Voltage (LV) Intel Pentium® M 738 (with 2 MB L2 cache), 1.0 GHz Ultra Low Voltage (ULV) Celeron® M 373 (with 512 kB L2 cache), or 800 MHz ULV Celeron M (with 0 kB L2 cache) processors
  - All processors support a Front Side Bus (FSB) of 400 MHz
- Memory
  - Provides a single 200-pin DDR SODIMM socket
  - Supports a single +2.5V DDR RAM SODIMM up to 1 GB
  - Supports PC2700 DDR 333 (166 MHz)
- PCI Bus/ISA Bus
  - PCI 2.2 compliant, 32-bits wide
  - Supports PCI Bus speed at 33 MHz
  - Supports ISA bus speed at 8 MHz
- IDE Interfaces
  - Supports two enhanced IDE controllers (4 devices)
  - Supports dual bus master mode
  - Supports Ultra DMA 33/66/100 modes
  - Supports ATAPI and DVD peripherals
  - Supports IDE native and ATA compatibility modes
- Floppy Disk Interface
  - Supports shared output connector with Parallel port
  - Supports two floppy drives
  - Supports all standard PC/AT formats: 360 kB, 1.2 MB, 720 kB, 1.44 MB, and 2.88 MB
- Serial Ports
  - Provides two buffered TTL serial ports with full handshaking (transceivers on baseboard)
  - Provides two 16550-equivalent controllers, each with a built-in 16-byte FIFO buffer
  - Provides programmable word length, stop bits, and parity
  - Provides 16-bit programmable baud-rate generator
  - Provides full modem capability
- Infrared Interface
  - Provides a single IrDA 1.1 port
  - Supports HPSIR and ASKIR infrared modes
- Parallel Port
  - Supports shared output connector with Floppy controller
  - Supports standard 25-pin printer (LPT1) port
  - Supports IEEE standard 1284 protocols of EPP and ECP outputs
  - Bi-directional data lines

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- Supports 16 byte FIFO for ECP mode.

- USB Ports
  - Supports two root USB hubs
  - Supports four USB ports
  - Supports USB v2.0 and legacy v1.1
  - Supports over-current fuses on baseboard
  - Supports USB Boot and the respective USB Boot devices
- Keyboard/Mouse Interface
  - Supports PS/2 keyboard
  - Supports PS/2 mouse
- Audio Interface
  - Supports AC'97 standard
  - Provides AC'97 CODEC onboard
  - Supports an audio amplifier on baseboard
- Ethernet Interface
  - Provides an Intel 82551QM Controller and one Ethernet port
  - Supports LAN Boot (See Appendix B)
  - Supports magnetics and RJ45 connector on baseboard
  - Supports IEEE 802.3 10BaseT/100BaseTX compatible physical layer
  - Supports Auto-negotiation for speed and duplex mode
  - Supports full duplex or half-duplex mode
    - Full-duplex mode supports transmit and receive frames simultaneously
    - Supports IEEE 802.3x Flow control in full duplex mode
    - Half-duplex mode supports enhance proprietary collision reduction mode
- Video Interfaces (CRT/LVDS)
  - Supports CRT (1600 x 1200) with 64 MB UMA (Unified Memory Architecture)
  - Provides integrated 128-bit graphics controller
  - Provides LVDS outputs (1 or 2 channel)
- Miscellaneous
  - Provides a Real-Time Clock (RTC)
  - Supports battery-free boot
  - Supports an external battery for Real-Time Clock operation
  - Supports a Oops! Jumper (BIOS recovery)
  - Supports Remote Access function (Serial Console or Console Redirection)
  - Provides Watchdog Timer feature
  - Supports a customizable Splash Screen (OEM boot logo)
  - Supports Power Management (ACPI 2.0, including S3 suspend-to-RAM)

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Block Diagram

Figure 2-3 shows the functional components of the board.

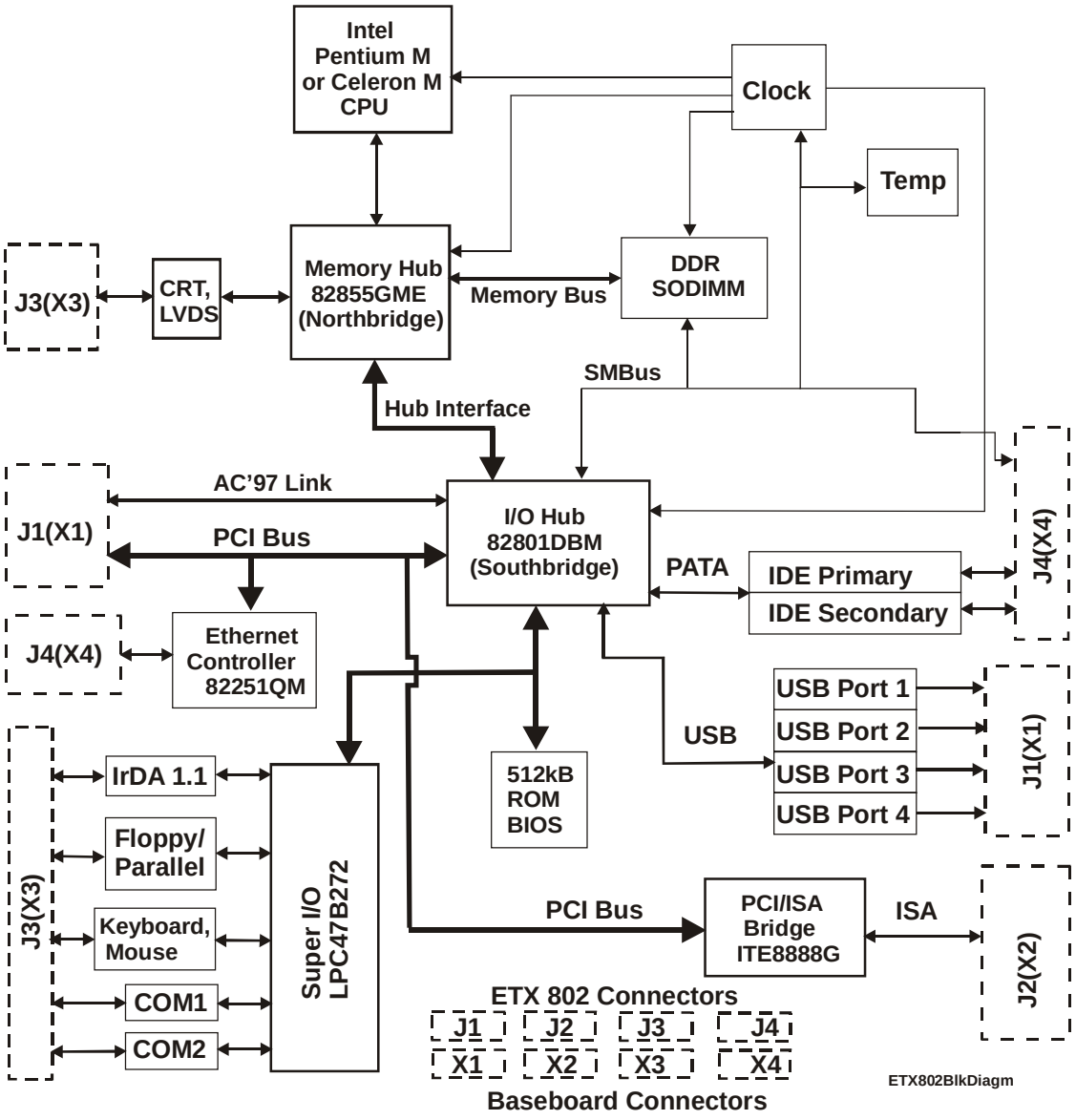


Figure 2-3. Simplified Functional Block Diagram

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Major Integrated Circuits (ICs)

Table 2-1 lists the major integrated circuits (chips), including a brief description, on the ETX 802 module and Figures 2-4 and 2-5 show the location of the major chips.

Table 2-1. Major Integrated Circuit Description and Function

Chip Type	Mfg.	Model	Description	Function
CPU (U1)	Intel	Pentium M Celeron M	LV 1.4 GHz, ULV 1.0 GHz, or ULV 800 MHz CPU's	Embedded CPU
Memory Hub (U2)	Intel	82855GME	Provides Memory control and Video functions	Memory and Video
I/O Hub (U8)	Intel	82801DBM	Provides some of standard I/O functions	Some I/O Functions
Super I/O (U13)	Standard Microsystems Corp.	LPC47B272	Provides the remaining I/O functions	Most I/O Functions
Audio CODEC (U9)	RealTek	ALC202A	Provides audio component functions	Audio Functions
Ethernet Controller (U10)	Intel	82551QM	Provides 10/100BaseT Ethernet controller	Ethernet Functions
PCI/ISA Bridge (U33)	ITE Tech Inc.	ITE8888G	Provides bridging of PCI and ISA busses	PCI/ISA Bridge

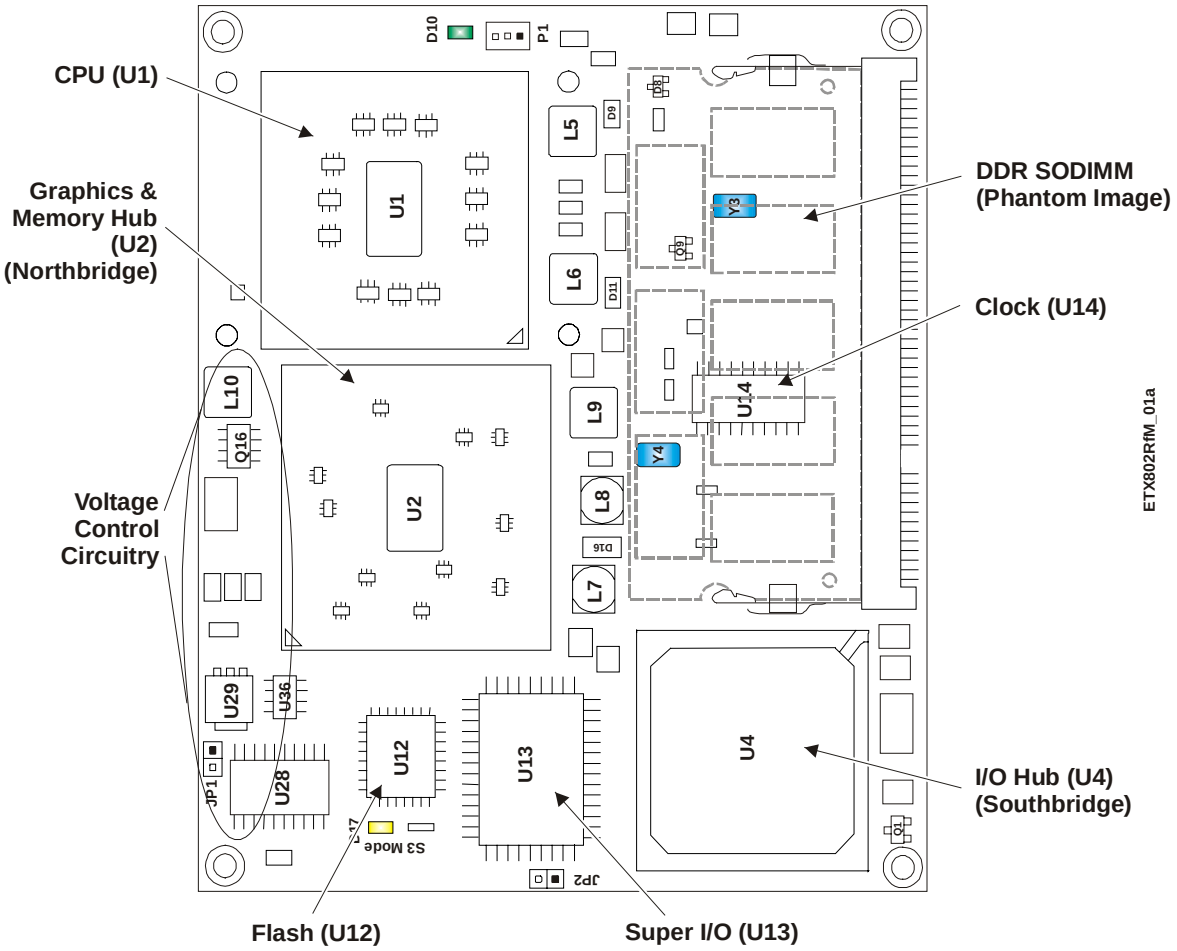


Figure 2-4. Component Locations (Top view)

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Connector Definitions

Table 2-2 describes the connectors shown in Figures 2-4 and 2-5.

Table 2-2. Connector Descriptions

No.	Signals	Description
P1	CPU Fan connector	3-pin header provides +5V, Fan Tachometer, and ground to fan
J1	PCI, USB, Audio	100-pin connector for 32-bit PCI, USB (4 ports), and Audio
J2	ISA Bus	100-pin connector for ISA bus
J3	Video, I/O	100-pin connector for Video (VGA, LVDS) and I/O (Floppy/Parallel, Serial Ports 1 & 2, and Infrared) signals
J4	IDE, Ethernet	100-pin connector for IDE (Primary & Secondary IDE), I^2C bus, Power Management, and the Ethernet port
J5	DDR Memory	200-pin socket for a RAM SODIMM

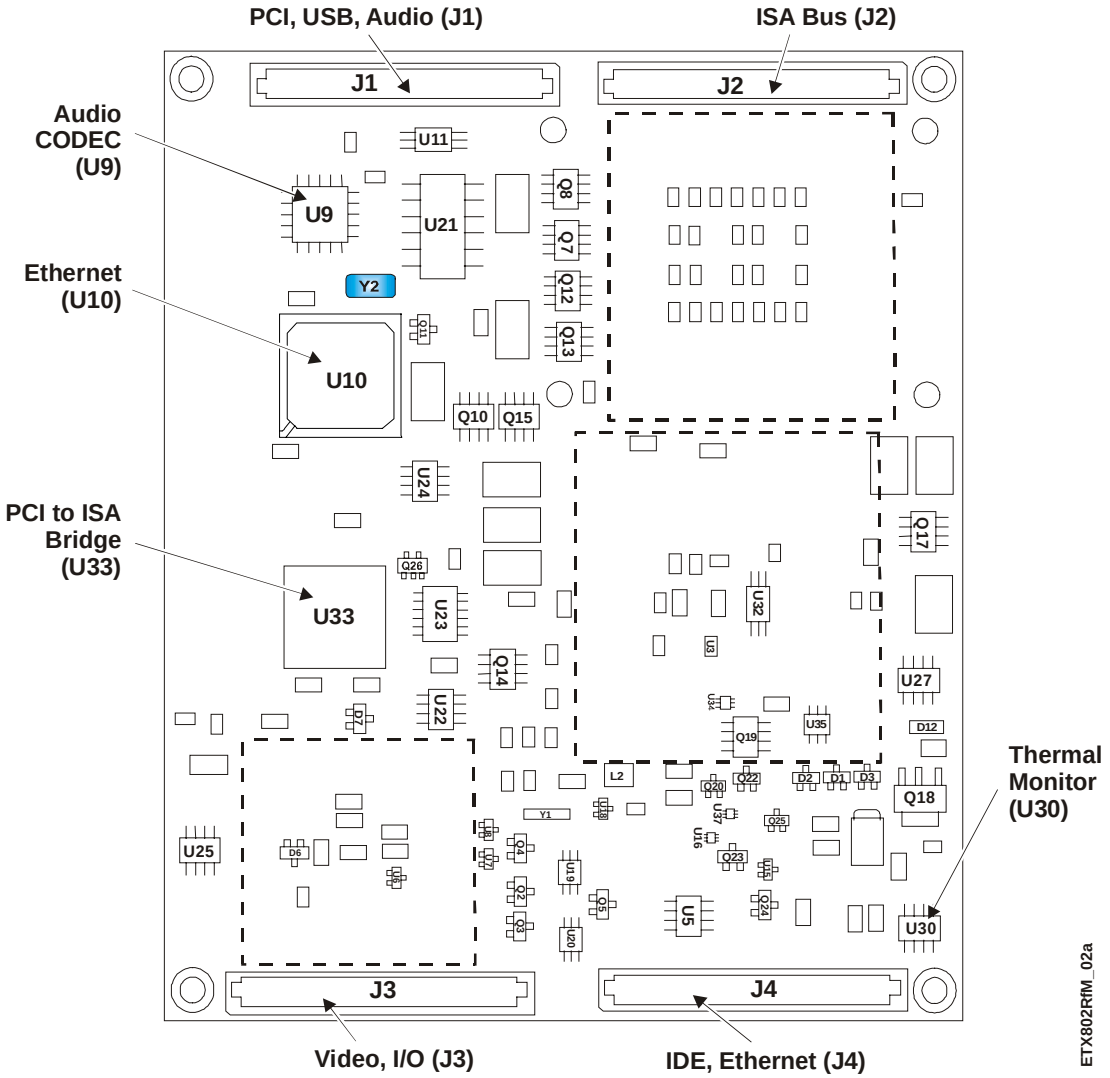


Figure 2-5. Connector and Component Locations (Bottom view)

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Jumper Definition

Table 2-3 describes the jumpers shown in Figure 2-6.

Table 2-3. Jumper Settings

Jumper #	Installed	Removed/Enabled
JP1 – AT/ATX Power Select	AT, or +5 Volt only (pins 1-2)	ATX Operation (Removed) **Default**
JP2 – CMOS Normal/Clear	Clear (pins 1-2)	Normal (Removed) **Default**

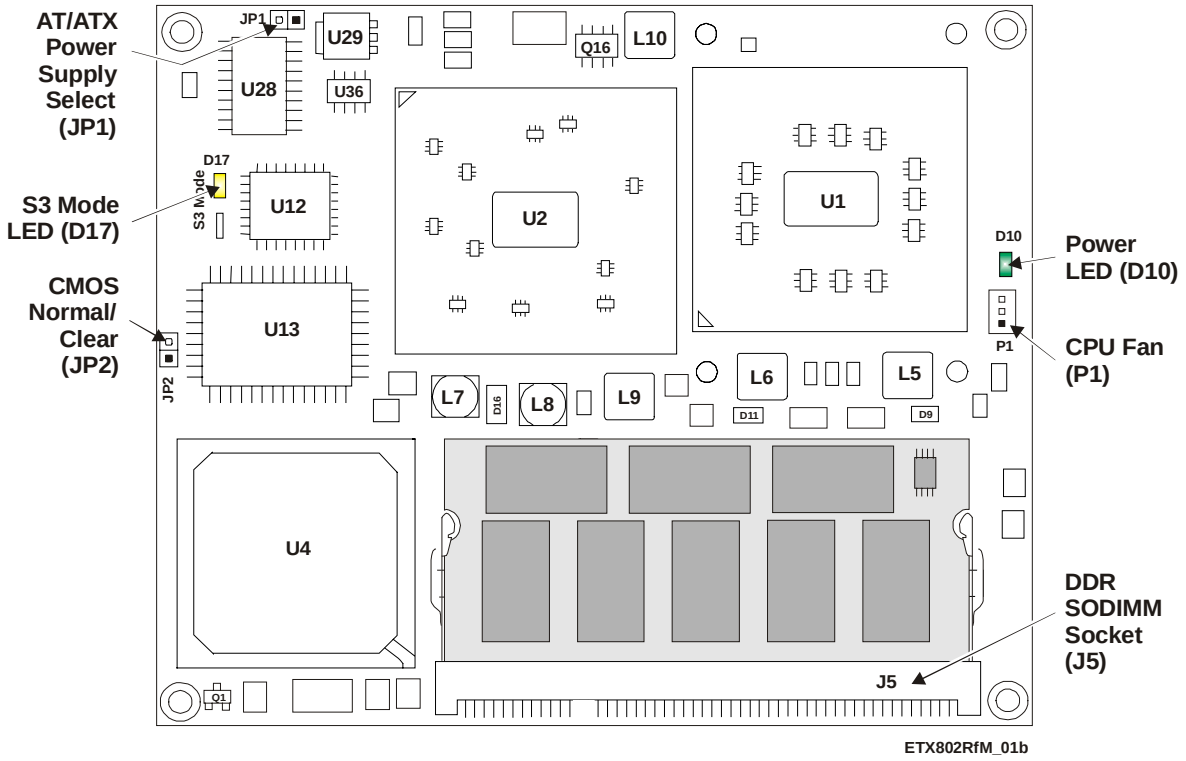


Figure 2-6. Jumper Locations (Top view)

LED Definitions

Table 2-4 provides the definition of the LED located on the ETX 802 board. Refer to Figure 2-6.

Table 2-4. LED Indicators

Indicator	On State	Off State
Power Indicator (D10)	Steady Green = Power On	Steady Off = Power Off
S3 Mode (D17)	Steady Yellow = In S3 (suspend to RAM) mode	Steady Off = Not in S3 state

Note: The ETX 802's power LED also indicates there is power to the baseboard, when the green LED (D10) is brightly lit.

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Specifications

Physical Specifications

Table 2-5 gives the physical dimensions of the board and Figure 2-7 gives the mounting dimensions.

Table 2-5. Weight and Footprint Dimensions

Item	Dimension
Weight	0.11 kg. (0.243lbs.) w SODIMM, w/o heatsinks
Height (overall)	5.29 mm (0.208")
Width	95 mm (3.74")
Length	114 mm (4.48")
Thickness	2.36 mm (0.093")

NOTE Overall height is measured from the upper board surface to the highest permanent component (SODIMM socket, J5) on the upper board surface. This measurement does not include the heatsinks available for this board or the various sizes of SODIMM inserted into the socket. The heatsinks will increase this dimension.

Mechanical Specifications

Figure 2-7 provides a through the board view of the ETX 802 with the mechanical mounting dimensions.

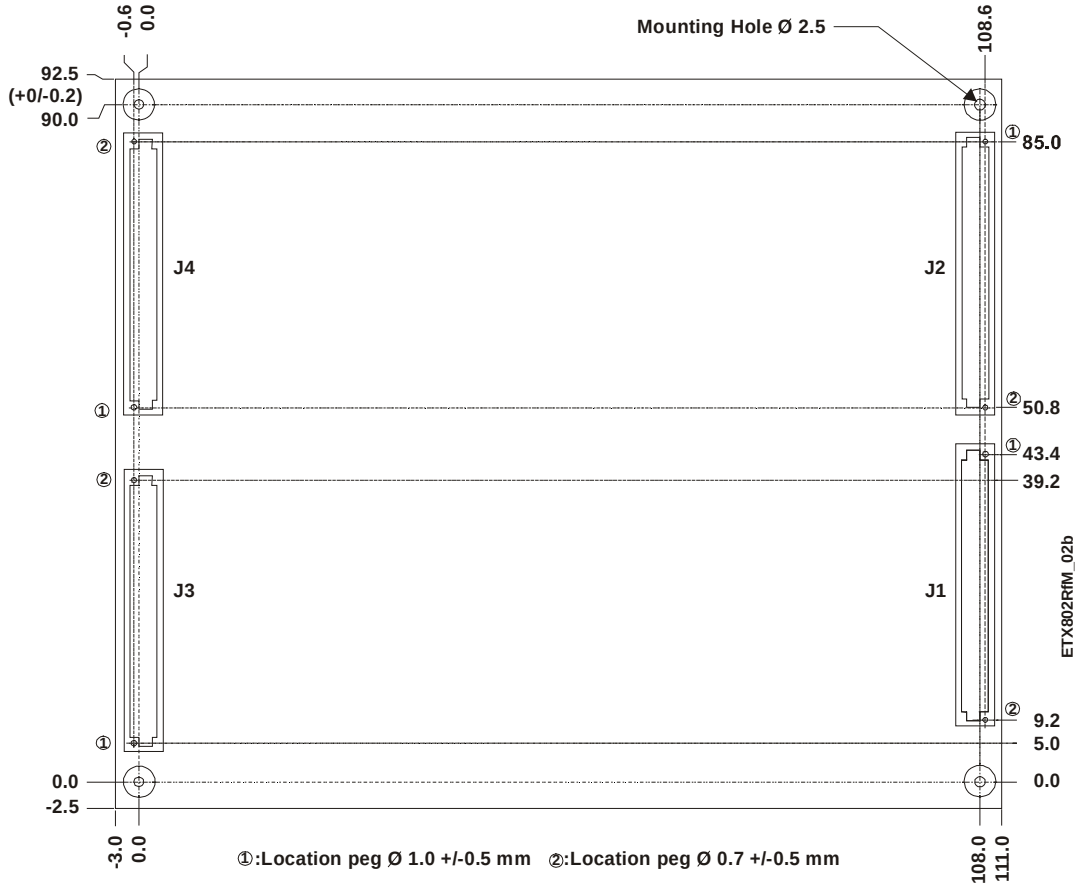


Figure 2-7. Dimensions (Top, Through Board View)

NOTE All dimensions are given in millimeters and all dimensions without tolerance are +/-0.2 mm.

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Power Specifications

Table 2-6 shows the power requirements from the baseboard and the board power output.

Table 2-6. Power Supply Requirements

Parameter	800 MHz ULV Celeron M Characteristics	1.0 GHz ULV Celeron M Characteristics	1.4 GHz LV Pentium M Characteristics
Input Type	Regulated DC voltages	Regulated DC voltages	Regulated DC voltages
In-rush Current*	14.24 Amps	14.24 Amps	14.24 Amps
Typical BIT** Current (W)	2.68 Amps (13.41W)	2.75 Amps (13.73W)	3.34 Amps (16.68W)

**Notes: ***The In-rush current represents video, 128 MB RAM, and power only connected through the Ampro baseboard. Typically, in-rush current reflects the short duration current spike associated with charging large on-board bulk capacitance during power supply start up. However, the listed in-rush current value is the result of placing a switch on the DC output of a fully 'ramped' power supply to give a worst-case current value, which is much higher than the standard method. This in-rush value should be regarded as a maximum design guideline, not a requisite value.

**The Burn-In-Test (BIT) current setup has CRT video, 128 MB RAM, floppy drive (1), IDE hard disk drive (1), USB hard disk drive (1), USB CD-ROM (1), serial ports (2) with loopbacks, keyboard, mouse, compact flash card (64 MB) installed on baseboard (1), USB compact flash card reader with compact flash card (64 MB) installed (1), USB Jump-drive (1), and the Ethernet port (1) operating under Microsoft® Windows® XP (SP2). Since the ETX 802 can not operate without a baseboard, all current measurements include the Ampro baseboard in the QuickStart Kit.

Environmental Specifications

Table 2-7 provides the most efficient operating and storage condition ranges required for this board.

Table 2-7. Environmental Requirements

Parameter	800 MHz ULV Celeron M Conditions	1.0 GHz ULV Celeron M Conditions	1.4 GHz LV Pentium M Conditions
Temperature			
Operating	–20° to +70°C (-4° to +158°F)	–20° to +70°C (-4° to +158°F)	–20° to + 70°C (-4° to +158°F)
Extended (Optional)	–40° to +85°C (-40° to +185°F)	–40° to +85°C (-40° to +185°F)	–40° to +85°C (-40° to +185°F)
Storage	–55° to +85°C (–67° to +185°F)	–55° to +85°C (–67° to +185°F)	–55° to +85°C (–67° to +185°F)
Humidity			
Operating	5% to 95% relative humidity, non-condensing	5% to 95% relative humidity, non-condensing	5% to 95% relative humidity, non-condensing
Non-operating	5% to 95% relative humidity, non-condensing	5% to 95% relative humidity, non-condensing	5% to 95% relative humidity, non-condensing

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Thermal/Cooling Requirements

The CPU, Memory Hub, I/O Hub, and voltage regulators are the main sources of heat on the board. The ETX 802 is designed to operate at its maximum CPU speed of 800 MHz, 1.0 GHz, or 1.4 GHz. The CPUs and Memory & Graphics Hub (Northbridge) require a heatsink, but no fan below + 70°C. However, the 1.4 GHz Pentium M requires a fan above + 70°C. Thermal sensors are provided on the ETX 802 and an optional heatspreader plate is also available.

NOTE	If you use Ampro's optional heatspreader plate, you must provide an additional form of cooling, such as a fan. A heatspreader plate should not be considered a complete thermal solution for any of the processors listed above, especially the 1.4 GHz Pentium M CPU.

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Chapter 3 Hardware

Overview

This chapter discusses the chips and features of the connectors in the following order:

- CPU (U1)
- Memory (J5)
- PCI Bus Interface (J1)
  - USB
  - Audio Interface
- ISA Bus Interface (J2)
- Primary I/O Interface (J3)
  - Floppy/Parallel Interface
  - Serial Port Interfaces
  - Keyboard
  - Mouse
  - Infrared (IrDA)
  - Video Interfaces (CRT & LVDS)
- IDE and Auxiliary Interface (J4)
  - Primary IDE Interface
  - Secondary IDE Interface
  - Ethernet Interface
  - Time of Day (RTC)/Battery
  - Speaker
  - Power Control and Management
  - SMBus
- Miscellaneous
  - Oops! Jumper (BIOS recovery)
  - Remote Access (Serial Console)
  - Temperature Monitoring
  - Watchdog timer (WDT)
  - Power Interface (including ACPI)

NOTE	Ampro Computers, Inc. only supports the features/options tested and listed in this manual. The main integrated circuits (chips) used in the ETX 802 may provide more features or options than are listed for the ETX 802, but some of these chip features/options are not supported on the board and will not function as specified in the chip documentation.

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CPU (U1)

The ETX 802 supports three Intel processor choices; high performance Low Voltage (LV) 1.4 GHz Pentium® M 738, Ultra Low Voltage (ULV) 1.0 GHz Celeron® M 373, or a ULV 800 MHz Celeron M processor.

Celeron M Processors

The 800 MHz Celeron M processor (Dothan core) has 0 kB L2 Cache on board, with a 400 MHz FSB (front side bus). This Celeron M processor uses 90 nm architecture and requires a heatsink, but no fan.

The 1.0 GHz Celeron M 373 processor (Dothan core) has 512 kB L2 Cache on board with a 400 MHz FSB. This Celeron M 373 processor uses 90 nm architecture and requires a heatsink, but no fan.

Pentium M Processor

The 1.4 GHz Pentium M 738 processor (Dothan core) has 2 MB L2 Cache on board with a 400 MHz FSB. This Pentium M 738 processor uses 90 nm architecture and requires a heatsink, but no fan below + 70°C. For the extended temperature range (+70°C to +85°C) a fan is required.

CAUTION	To prevent processor overheating, you must provide a heatsink on the CPU. If you use an optional heatspreader, you must provide an additional form of cooling, such as a fan. The heatspreader is not a complete thermal solution for any of the processors listed.

Memory

The ETX 802 memory consists of the following elements:

- DDR RAM SODIMM
- Flash memory

DDR Memory SODIMM Socket (J5)

The ETX 802 supports a single 200-pin DDR SODIMM socket.

- DDR SODIMM socket can support up to 1 GB of memory
- Supports +2.5V, PC2700 DDR 333 (333 Mbps, 166 MHz (6 ns))

NOTE	Ampro recommends using PC2700 DDR 333 (333 Mbps, 166 MHz, 6 ns), +2.5V, 200-pin, DDR RAM SODIMM for maximum performance. The ETX 802 will operate acceptably with a PC2100 DDR 266 (266 Mbps, 133 MHz, 7.5 ns) SODIMM.

Flash Memory (U12)

There is an 8-bit wide, 512 kB flash device used for system BIOS and is connected to the I/O Hub (82801DBM), through an LPC bus transceiver. The flash memory is used to store system parameters and can be used for battery-free boot capability when there is no battery present. The BIOS is re-programmable and the features supported are detailed in Chapter 4, *BIOS Setup Utility*.

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Interrupt Channel Assignments (IRQs)

The channel interrupt assignments are listed in Table 3-1.

Table 3-1. Interrupt Channel (IRQs) Assignments (Typical)

Device vs IRQ No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timer	X															
Keyboard		X														
Secondary Cascade			X													
COM1				O	D											
COM2				D	O											
Floppy							X									
Parallel						O		D								
RTC									X							
IDE Primary															D	O
IDE Secondary															O	D
Math Coprocessor														X		
PS/2 Mouse													X			
AC'97 CODEC						D		O		O	O					
PCI INTA	Automatically Assigned or User selectable															
PCI INTB	Automatically Assigned or User selectable															
PCI INTC	Automatically Assigned or User selectable															
PCI INTD	Automatically Assigned or User selectable															
USB	Automatically Assigned															
VGA	Automatically Assigned															
Ethernet	Automatically Assigned															

Legend: D = Default, O = Optional, X = Fixed Refer also to the IRQs listed in Chapter 4, BIOS Setup.

NOTE	The IRQs for the Ethernet, Video, and Internal LPC bus are automatically assigned by the BIOS Plug and Play logic.

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Memory Map

This table provides the common PC/AT memory allocations. BIOS uses memory below 000500h.

Table 3-2. Memory Map

Base Address	Function
00000000h - 0009FFFFh	Conventional Memory
000A0000h - 000AFFFFh	Graphics Memory
000B0000h - 000B7FFFh	Mono Text Memory
000B8020h - 000BFFFFh	Color Text Memory
000C0000h - 000CFFFFh	Standard Video BIOS
000E0000h - 000FFFFFh	System BIOS Area (Storage and RAM Shadowing)
00100000h - 04000000h	Extended Memory (If onboard VGA is enabled, then the amount of memory assigned is subtracted from extended memory)
FFF80200h - FFFFFFFFh	System Flash

I/O Address Map

Table 3-3 list the I/O address map.

Table 3-3. I/O Address Map

Address (hex)	Subsystem
000-00F	Primary DMA Controller
020-021	Master Interrupt Controller
040-043	Programmable Interrupt Timer (Clock/Timer)
060-06F	Keyboard Controller
070-07F	CMOS RAM, NMI Mask Reg, RT Clock
080-09F	DMA Page Registers
092	Fast A20 gate and CPU reset
094	Motherboard enable
102	Video subsystem register
0A0-0BF	Slave Interrupt Controller
0C0-0DF	Slave DMA Controller #2
0F0-0FF	Math Coprocessor
170-177	Secondary IDE Hard Disk Controller
1F0-1F8	Primary IDE Hard Disk Controller
201	Watchdog Timer (WDT)
278-27F	Parallel Printer
2F8-2FF	Serial Port 2 (COM2)
378-37F	Parallel Port (Standard and EPP)
3C0-3DF	VGA
3F0-3F7	Floppy Disk Controller
3F8-3FF	Serial Port 1 (COM1)
778-77A	Parallel Port (ECP Extensions) (Port 378+400)
CF8-CFF	PCI bus Configuration Address and Data

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PCI Bus Interface Connector (J1)

The J1 connector has 100 pins and is used for the PCI bus, USB ports, and Audio (AC'97) interface connections.

Tables 3-4 to 3-7 provide the PCI, USB, and Audio signals and descriptions in a simplified table and Table 3-8 provides the complete pin-outs for the J1 (X1) connector.

NOTE	Table 3-4 relates the pin-outs of the standard PCI bus connector, 32-bit, 124 pins (62-pins for each side, A & B), to the respective pins in the J1 (100-pin) connector.

PCI Bus

The Memory Hub (82855GME) integrates a PCI arbiter that supports up to four external PCI masters.

- This interface carries all of the appropriate PCI signals
- Bus operates at clock speeds up to 33 MHz.
- PCI 2.2 Compliant, 32-bit +3.3V PCI interface with +5V tolerant inputs

Table 3-4. Simplified PCI Pin/Signal Descriptions (J1)

J1 Pin #	Signal	PCI Pin #	Description
	NC	1 (A1)	Not connected (Test Reset)
	+12V	2 (A2)	+12 volt power
	NC	3 (A3)	Not connected (Test Mode Select)
	NC	4 (A4)	Not connected (Test Data Input)
	+5V	5 (A5)	+5 volt power
97	INTA*	6 (A6)	Interrupt A – This signal is used to request an interrupt.
95	INTC*	7 (A7)	Interrupt C – This signal is used to request an interrupt and only has meaning on a multi-function device.
	+5V	8 (A8)	+5 volt power
	NC	9 (A9)	Not connected (Reserved)
	+5VI/O	10 (A10)	+5.0 volt I/O
	NC	11 (A11)	Not connected (Reserved)
	GND	12 (A12)	Ground
	GND	13 (A13)	Ground
	3.3Vaux	14 (A14)	3.3 Volt Auxiliary – This voltage is an optional power source that delivers power to the PCI add-in card for generation of power management events when the main power to the card has been turned off by software. A system or add-in card that does not support PCI bus power management must treat the 3.3Vaux pin as reserved.
93	RST*	15 (A15)	PCI Bus Reset – This signal is used to bring PCI-specific registers, sequencers, and signals to a consistent state. Anytime Reset is asserted, all PCI output signals must be driven to the benign state.
	+5VI/O	16 (A16)	+5 volt I/O
	GNT#*	17 (A17)	Grant # – This is a point-to-point signal and indicates to the agent that access to the bus has been granted. Every master has its own Grant signal, which must be ignored while RST is asserted.

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J1 Pin #	Signal	PCI Pin #	Description
	GND	18 (A18)	Ground
57	PME*	19 (A19)	Power Management Event – This signal is an optional signal that can be used by a device to request a change in the device or system power state.
91	AD[30]	20 (A20)	Address/Data bus 30 – These signals (AD31 – AD0) are multiplexed on the same PCI connector pins. During the address phase of a PCI cycle, AD31 – AD0 contain a 32-bit address or other destination information. During the data phase, AD31 – AD0 contain data.
	+3.3V	21 (A21)	+3.3 volt power
87	AD[28]	22 (A22)	Address/Data bus 28 – Refer to J1, pin-91 for more information
86	AD[26]	23 (A23)	Address/Data bus 26 – Refer to J1, pin-91 for more information
	GND	24 (A24)	Ground
81	AD[24]	25 (A25)	Address/Data bus 24 – Refer to J1, pin-91 for more information)
60	IDSEL	26 (A26)	Initialization Device Select – This signal is used as a chip select during configuration read and write transactions.
	+3.3V	27 (A27)	+3.3 volt power
77	AD[22]	28 (A28)	Address/Data bus 22 – Refer to J1, pin-91 for more information
75	AD[20]	29 (A29)	Address/Data bus 20 – Refer to J1, pin-91 for more information
	GND	30 (A30)	Ground
74	AD[18]	31 (A31)	Address/Data bus 18 – Refer to J1, pin-91 for more information
69	AD[16]	32 (A32)	Address/Data bus 16 – Refer to J1, pin-91 for more information
	+3.3V	33 (A33)	+3.3 volt power
65	FRAME*	34 (A34)	PCI bus Frame access – This signal is driven by the current master to indicate the start of a transaction and will remain active until the final data cycle.
	GND	35 (A35)	Ground
61	TRDY*	36 (A36)	Target Ready – This signal indicates the selected device's ability to complete the current cycle of transaction. Both IRDY* and TRDY* must be asserted to terminate a data cycle.
	GND	37 (A37)	Ground
64	STOP*	38 (A38)	Stop – This signal is driven by the current PCI target to request the master to stop the current transaction.
	+3.3V	39 (A39)	+3.3 volt power
	NC	40 (A40)	Not connected (Reserved)
	NC	41 (A41)	Not connected (Reserved)
	GND	42 (A42)	Ground
53	PAR	43 (A43)	PCI bus Parity bit – This signal is the even parity bit on AD[31:0] and CBE[3:0]*.
47	AD[15]	44 (A44)	Address/Data bus 15 – Refer to J1, pin-91 for more information
	+3.3V	45 (A45)	+3.3 volt power
43	AD[13]	46 (A46)	Address/Data bus 13 – Refer to J1, pin-91 for more information
39	AD[11]	47 (A47)	Address/Data bus 11 – Refer to J1, pin-91 for more information

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J1 Pin #	Signal	PCI Pin #	Description
	GND	48 (A48)	Ground
34	AD[09]	49 (A49)	Address/Data bus 9 – Refer to J1, pin-91 for more information
	Key	50 (A50)	Key
	Key	51 (A51)	Key
31	CBE[0]*	52 (A52)	PCI Bus Command/Byte Enable 0 – This signal line is one of four signal lines multiplexed on the same pins, so that during the address cycle, the command is defined and during the data cycle, the byte enable is defined.
	+3.3V	53 (A53)	+3.3 volt power
29	AD[06]	54 (A54)	Address/Data bus 06 – Refer to J1, pin-91 for more information
27	AD[04]	55 (A55)	Address/Data bus 04 – Refer to J1, pin-91 for more information
	GND	56 (A56)	Ground
26	AD[02]	57 (A57)	Address/Data bus 02 – Refer to J1, pin-91 for more information
23	AD[00]	58 (A58)	Address/Data bus 00 – Refer to J1, pin-91 for more information
	+3.3VI/O	59 (A59)	+3.3 volt I/O
	NU	60 (A60)	Not used in 32-bit system (Request 64-bit Transfer) tied to +5v through 4.7k ohm resistor.
	+5V	61 (A61)	+5 volt power
	+5V	62 (A62)	+5 volt power
	-12V	63 (B1)	-12 volt power
	NC	64 (B2)	Not connected (Test Clock)
	GND	65 (B3)	Ground
	NC	66 (B4)	Not connected (Test Output)
	+5V	67 (B5)	+5 volt power
	+5V	68 (B6)	+5 volt power
98	INTB*	69 (B7)	Interrupt B – This signal is used to request an interrupt and only has meaning on a multi-function device.
96	INTD*	70 (B8)	Interrupt D – This signal is used to request an interrupt and only has meaning on a multi-function device.
	NU	71 (B9)	Not used (Present 1)
	NC	72 (B10)	Not connected (Reserved)
	NU	73 (B11)	Not used (Present 2)
	GND	74 (B12)	Ground
	GND	75 (B13)	Ground
	NC	76 (B14)	Not connected (Reserved)
	GND	77 (B15)	Ground
	CLK	78 (B16)	Clock – This signal provides timing for all transactions on the PCI bus and is an input to every PCI device.
	GND	79 (B17)	Ground

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J1 Pin #	Signal	PCI Pin #	Description
	REQ#*	80 (B18)	Request # – This is a point-to-point signal and indicates to the arbiter that this agent desires use of the bus. Every master has its own Request, which must be tri-stated while Reset is asserted.
	+5VI/O	81 (B19)	+5 volt I/O
94	AD[31]	82 (B20)	Address/Data bus 31 – Refer to J1, pin-91 for more information
90	AD[29]	83 (B21)	Address/Data bus 29 – Refer to J1, pin-91 for more information
	GND	84 (B22)	Ground
89	AD[27]	85 (B23)	Address/Data bus 27 – Refer to J1, pin-91 for more information
85	AD[25]	86 (B24)	Address/Data bus 25 – Refer to J1, pin-91 for more information
	+3.3V	87 (B25)	+3.3 volt power
82	CBE[3]*	88 (B26)	Bus Command and Byte Enable 3 – Refer to J1, pin-31 for more information.
79	AD[23]	89 (B27)	Address/Data bus 23 – Refer to J1, pin-91 for more information
	GND	90 (B28)	Ground
78	AD[21]	91 (B29)	Address/Data bus 21 – Refer to J1, pin-91 for more information
73	AD[19]	92 (B30)	Address/Data bus 19 – Refer to J1, pin-91 for more information
	+3.3V	93 (B31)	+3.3 volt power
71	AD[17]	94 (B32)	Address/Data bus 17 – Refer to J1, pin-91 for more information
70	CBE[2]*	95 (B33)	Bus Command and Byte Enable 2 – Refer to J1, pin-31 for more information.
	GND	96 (B34)	Ground
63	IRDY*	97 (B35)	Initiator Ready – This signal indicates the master's ability to complete the current data cycle of the transaction.
	+3.3V	98 (B36)	+3.3 volt power
60	DEVSEL*	99 (B37)	Device Select – This signal is driven by the target device when its address is decoded.
	GND	100 (B38)	Ground
59	LOCK*	101 (B39)	Lock – This signal indicates an operation that may require multiple transactions to complete.
55	PERR*	102 (B40)	Parity Error – This signal is driven by the PCI target during a write to indicate a data parity error has been detected.
	+3.3V	103 (B41)	+3.3 volt power
54	SERR*	104 (B42)	System Error – This signal is for reporting address parity errors.
	+3.3V	105 (B43)	+3.3 volt power
49	CBE[1]*	106 (B44)	Bus Command and Byte Enable 1 – Refer to J1, pin-31 for more information.
45	AD[14]	107 (B45)	Address/Data bus 14 – Refer to J1, pin-91 for more information
	GND	108 (B46)	Ground
41	AD[12]	109 (B47)	Address/Data bus 12 – Refer to J1, pin-91 for more information
37	AD[10]	110 (B48)	Address/Data bus 10 – Refer to J1, pin-91 for more information
	GND	111 (B49)	Ground
	Key	112 (B50)	Key

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J1 Pin #	Signal	PCI Pin #	Description
	Key	113 (B51)	Key
33	AD[08]	114 (B52)	Address/Data bus 08 – Refer to J1, pin-91 for more information
32	AD[07]	115 (B53)	Address/Data bus 07 – Refer to J1, pin-91 for more information
	+3.3V	116 (B54)	+3.3 volt power
30	AD[05]	117 (B55)	Address/Data bus 05 – Refer to J1, pin-91 for more information
28	AD[03]	118 (B56)	Address/Data bus 03 – Refer to J1, pin-91 for more information
	GND	119 (B57)	Ground
25	AD[01]	120 (B58)	Address/Data bus 01 – Refer to J1, pin-91 for more information
	+5V I/O	121 (B59)	+5 volt I/O
	NU	122 (B60)	Not used in 32-bit system (Acknowledge 64-bit Transfer) tied to +5v through 4.7k ohm resistor.
	+5V	123 (B61)	+5 volt power
	+5V	124 (B62)	+5 volt power

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Universal Serial Bus (USB)

The ETX 802 module supports up to four USB ports on the baseboard and the supported features are listed below.

- USB v2.0 and backwards compatible to Universal OHCI v1.1
- Two root USB hubs and 4 USB ports
- Supports USB boot of floppy disk drives, hard disk drives, CD-ROMs, or other USB boot devices.
- Integrated physical layer transceivers
- Over-current detection status on USB ports 1 and 2

Table 3-5. Simplified USB Interface Pin/Signal Descriptions (J1)

J1 Pin #	Signal	Description
	USBP	USB Power – +5 volts
76	USB0-	Universal Serial Bus Port 0 Data Negative Polarity
88	USB0+	Universal Serial Bus Port 0 Data Positive Polarity
80	USB1-	Universal Serial Bus Port 1 Data Negative Polarity
92	USB1+	Universal Serial Bus Port 1 Data Positive Polarity
58	USB2-	Universal Serial Bus Port 2 Data Negative Polarity
66	USB2+	Universal Serial Bus Port 2 Data Positive Polarity
62	USB3-	Universal Serial Bus Port 3 Data Negative Polarity
72	USB3+	Universal Serial Bus Port 3 Data Positive Polarity
	GND	Ground

Notes: The shaded area denotes power or ground.

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Serial Interrupt Request

This SERIRQ signal is connected to serial request input on the I/O Hub (82801DBM) for the alternative ISA/PCI interrupts. If this feature is utilized, then DMA2 (DAck2 and DRQ2) will be supported by ETX 802 module. The ETX 802 SERIRQ pin (pin-21) must be connected to the baseboard to use the ISA bus on the baseboard.

Table 3-6. Simplified Serial Interrupt Request (J1)

J1 Pin #	Signal	Description
21	SERIRQ	Serial Interrupt Request – This pin is used to support the serial interrupt protocol.

Audio Interface

The RealTek Audio CODEC (ALC202A) on the ETX 802 supports the AC'97 audio standard and the supported features listed below.

- I/O Hub (82801DBM) supports the onboard CODEC (ALC202A)
- AC'97 Rev 2.1 compliant
- Supports audio amplifier on baseboard
- PC-Beep passthrough to Line Out while reset is held active low
- True Line Level Output with volume control independent of Line Out
- Digital 3V and 5V compliant

Table 3-7. Simplified Audio Interface Pin/Signal Descriptions (J1)

J1 Pin #	Signal	Description
38	AUX_AL	Auxiliary A Input Left – This signal is normally used for an external CD-ROM analog output or similar live-level audio source. Minimum input impedance is 5k Ohms and nominal input level is 1 volt RMS.
40	MIC	Microphone reference signal – This microphone input signal has a minimum input impedance of 5k Ohms, and the maximum input voltage is 0.15 V p-p.
42	AUX_AR	Auxiliary A Input Right – This signal is normally used for an external CD-ROM analog output or similar live-level audio source. Minimum input impedance is 5k Ohms and nominal input level is 1 volt RMS.
44	ASVCC	Analog Supply Voltage – This test voltage is used for the sound controller, but is not available for customer use.
46	SNDL	Stereo Line Output Left channel – This output signal has a nominal level of 1 volt RMS into 10k impedance load. This output signal can not drive low-impedance speakers directly.
48	ASGND	Analog Ground – This ground is used for the sound controller and an external amplifier to achieve the lowest audio noise levels.
50	SNDR	Stereo Line Output Right channel – This output signal has a nominal level of 1 volt RMS into 10k impedance load. This output signal can not drive low-impedance speakers directly

Notes: The shaded area denotes power or ground.

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Table 3-8. Complete J1 Interface Pin/Signal Descriptions (J1)

J1 Pin #	Signal	Description
1, 2	GND	Ground
3	PCICLK3	PCI clock 3 – This signal line is one of four signal lines. These clock signals provide the timing outputs for four external PCI devices and the timing for all transactions on the PCI bus.
4	PCICLK4	PCI clock 4 – Refer to J1, pin-3 for more information.
5, 6	GND	Ground
7	PCICLK1	PCI clock 1 – Refer to J1, pin-3 for more information.
8	PCICLK2	PCI clock 2 – Refer to J1, pin-3 for more information.
9	REQ3*	Bus Request 3 – This signal line is one of four signal lines. These signals indicate to the arbitrator that the device desires use of the bus.
10	GNT3*	Grant 3 – This signal line is one of four signal lines. These signal lines indicate access has been granted to the requesting device (PCI Masters).
11	GNT2*	Grant 3 – Refer to J1, pin-10 for more information.
12	+3.3V	+3.3 volts +/- 5%
13	REQ2*	Bus Request 0 – This signal line is one of three signal lines. These signals indicate the device desires use of the bus to the arbitrator.
14	GNT1*	Grant 1 – Refer to J1, pin-10 for more information.
15	REQ1*	Bus Request 1 – Refer to J1, pin-13 for more information.
16	+3.3V	+3.3 volts +/- 5%
17	GNT0*	Grant 0 – Refer to J1, pin-10 for more information.
18	NC	Not Connected (Reserved)
19, 20	VCC	DC Power – +5 volts +/- 5%
21	SERIRQ	Serial Interrupt Request – This signal supports the serial interrupt protocol.
22	REQ0*	Bus Request 0 – Refer to J1, pin-13 for more information.
23	AD0	Address/Data bus 0 – These signals <AD31 – AD0> are multiplexed on the same PCI connector pins. During the address phase of a PCI cycle, AD31–AD0 contain a 32-bit address or other destination information. During the data phase, AD31 – AD0 contain data.
24	+3.3V	+3.3 volts +/- 5%
25	AD1	Address/Data bus 1 – Refer to J1, pin-23 for more information.
26	AD2	Address/Data bus 2 – Refer to J1, pin-23 for more information.
27	AD4	Address/Data bus 4 – Refer to J1, pin-23 for more information.
28	AD3	Address/Data bus 3 – Refer to J1, pin-23 for more information.
29	AD6	Address/Data bus 6 – Refer to J1, pin-23 for more information.
30	AD5	Address/Data bus 5 – Refer to J1, pin-23 for more information.
31	CBE0*	PCI Bus Command/Byte Enable 0 – This signal line is one of four signal lines multiplexed on the same pins, so that during the address cycle, the command is defined and during the data cycle, the byte enable is defined.
32	AD7	Address/Data bus 7 – Refer to J1, pin-23 for more information.
33	AD8	Address/Data bus 8 – Refer to J1, pin-23 for more information.

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J1 Pin #	Signal	Description
34	AD9	Address/Data bus 9 – Refer to J1, pin-23 for more information.
35, 36	GND	Ground
37	AD10	Address/Data bus 10 – Refer to J1, pin-23 for more information.
38	AUXAL	Auxiliary A Input Left – This signal is normally used for an external CD-ROM analog output or similar live-level audio source. Minimum input impedance is 5k Ohms and nominal input level is 1 volt RMS.
39	AD11	Address/Data bus 11 – Refer to J1, pin-23 for more information.
40	MIC	Microphone reference signal – This microphone input signal has a minimum input impedance of 5k Ohms, and the maximum input voltage is 0.15 V p-p.
41	AD12	Address/Data bus 12 – Refer to J1, pin-23 for more information.
42	AUXAR	Auxiliary A Input Right – This signal is normally used for an external CD-ROM analog output or similar live-level audio source. Minimum input impedance is 5k Ohms and nominal input level is 1 volt RMS.
43	AD13	Address/Data bus 13 – Refer to J1, pin-23 for more information.
44	ASVCC	Analog Supply Voltage – This test voltage is used for the sound controller, but is not available for customer use.
45	AD14	Address/Data bus 14 – Refer to J1, pin-23 for more information.
46	SNDL	Stereo Line Output Left channel – Output signal has a nominal 1 volt RMS level into 10k impedance load. This output signal can not drive low-impedance speakers directly.
47	AD15	Address/Data bus 15 – Refer to J1, pin-23 for more information.
48	ASGND	Analog Ground – This ground is used for the sound controller and an external amplifier to achieved the lowest audio noise levels.
49	CBE1*	Bus Command and Byte Enable 1 – Refer to J1, pin-31 for more information.
50	SNDR	Stereo Line Output Right channel – This output signal has a nominal level of 1 volt RMS into 10k impedance load. This output signal can not drive low-impedance speakers directly
51, 52	VCC	DC Power – +5 volts +/- 5%
53	PAR	PCI bus Parity bit – This signal is even parity bit on AD[31:0] and CBE[3:0]*.
54	SERR*	System Error – This signal is for reporting address parity errors.
55	PERR*	Parity Error – This signal is driven by the PCI target during a write to indicate a data parity error has been detected.
56	NC	Not connected (Reserved)
57	PME*	Power Management Event – This signal is an optional signal that can be used by a device to request a change in the device or system power state.
58	USB2-	Universal Serial Bus Port 2 Data Negative Polarity
59	LOCK*	Lock – This signal indicates an operation that may require multiple transactions to complete.
60	DEVSEL*	Device Select – Driven by the target device when its address is decoded.
61	TRDY*	Target Ready – This signal indicates the selected device's ability to complete the current cycle of transaction. Both IRDY and TRDY must be asserted to terminate a data cycle.
62	USB3-	Universal Serial Bus Port 3 Data Negative Polarity

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J1 Pin #	Signal	Description
63	IRDY*	Initiator Ready – Indicates the master's ability to complete the current data cycle.
64	STOP*	Stop – Driven by the current PCI target when requesting the master stop the current transaction.
65	FRAME*	PCI bus Frame access – Driven by the current master to indicate the start of a transaction and will remain active until the final data cycle.
66	USB2+	Universal Serial Bus Port 2 Data Positive Polarity
67, 68	GND	Ground
69	AD16	Address/Data bus 16 – Refer to J1, pin-23 for more information.
70	CBE2*	Bus Command and Byte Enable 2 – Refer to J1, pin-31 for more information.
71	AD17	Address/Data bus 17 – Refer to J1, pin-23 for more information.
72	USB3+	Universal Serial Bus Port 3 Data Positive Polarity
73	AD19	Address/Data bus 19 – Refer to J1, pin-23 for more information.
74	AD18	Address/Data bus 18 – Refer to J1, pin-23 for more information.
75	AD20	Address/Data bus 20 – Refer to J1, pin-23 for more information.
76	USB0-	Universal Serial Bus Port 0 Data Negative Polarity
77	AD22	Address/Data bus 22 – Refer to J1, pin-23 for more information.
78	AD21	Address/Data bus 21 – Refer to J1, pin-23 for more information.
79	AD23	Address/Data bus 23 – Refer to J1, pin-23 for more information.
80	USB1-	Universal Serial Bus Port 0 Data Negative Polarity
81	AD24	Address/Data bus 24 – Refer to J1, pin-23 for more information.
82	CBE3*	Bus Command and Byte Enable 3 – Refer to J1, pin-31 for more information.
83, 84	VCC	DC Power – +5 volts +/- 5%
85	AD25	Address/Data bus 25 – Refer to J1, pin-23 for more information.
86	AD26	Address/Data bus 26 – Refer to J1, pin-23 for more information.
87	AD28	Address/Data bus 28 – Refer to J1, pin-23 for more information.
88	USB0+	Universal Serial Bus Port 0 Data Positive Polarity
89	AD27	Address/Data bus 27 – Refer to J1, pin-23 for more information.
90	AD29	Address/Data bus 29 – Refer to J1, pin-23 for more information.
91	AD30	Address/Data bus 30 – Refer to J1, pin-23 for more information.
92	USB1+	Universal Serial Bus Port 1 Data Positive Polarity
93	PCIRST*	PCI Bus Reset – Signal resets entire PCI Bus. Asserted during a system reset.
94	AD31	Address/Data bus 31 – Refer to J1, pin-23 for more information.
95	INTC*	Interrupt C – This signal is used to request an interrupt and only has meaning on a multi-function device.
96	INTD*	Interrupt D – This signal is used to request an interrupt and only has meaning on a multi-function device.
97	INTA*	Interrupt A – This signal is used to request an interrupt.
98	INTB*	Interrupt B – This signal is used to request an interrupt and only has meaning on a multi-function device.
99, 100	GND	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

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ISA Bus Interface (J2)

The J2 connector has 100 pins and is only used for the ISA Bus interface.

Table 3-9. Complete J2 ISA Bus Interface Pin/Signal Descriptions (J2)

J2 Pin #	Signal	Description
1, 2	GND	Ground
3	SD14	System Data 14 – These signals (0 to 19) provide system data bits.
4	SD15	System Data 15 – Refer to SD14 pin-3, for more information.
5	SD13	System Data 13 – Refer to SD14, pin-3, for more information.
6	BUSM*	Bus Master – This signal is used by an ISA board along with a DRQ line to gain ownership of the ISA bus. Upon receiving a -DACK a device can pull -MASTER low which will allow it to control the system address, data, and control lines. After -MASTER is low, the device should wait one CLK period before driving the address and data lines, and two clock periods before issuing a read or write command.
7	SD12	System Data 12 – Refer to SD14, pin-3, for more information.
8	DREQ7	DMA Request 7 – Used by I/O resources to request DMA service. Must be held high until associated DACK7 line is active.
9	SD11	System Data 11 – Refer to SD14, pin-3, for more information.
10	DACK7*	DMA Acknowledge 7 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
11	SD10	System Data 10 – Refer to SD14, pin-3, for more information.
12	DREQ6	DMA Request 6 – Used by I/O resources to request DMA service. Must be held high until associated DACK6 line is active.
13	SD9	System Data 9 – Refer to SD14, pin-3, for more information.
14	DACK6*	DMA Acknowledge 6 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
15	SD8	System Data 8 – Refer to SD14, pin-3, for more information.
16	DREQ5	DMA Request 5 – Used by I/O resources to request DMA service. Must be held high until associated DACK5 line is active.
17	MEMW*	Memory Write – This signal instructs a selected memory device to store data currently on the data bus. It is active on all memory write cycles.
18	DACK5*	DMA Acknowledge 5 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
19	MEMR*	Memory Read – This signal instructs a selected memory device to drive data onto the data bus. It is active on all memory read cycles.
20	DREQ0	DMA Request 0 – Used by I/O resources to request DMA service. Must be held high until associated DACK0 line is active.

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J2 Pin #	Signal	Description
21	LA17	Latchable Address 17 – These signals (0-23) must be latched by the resource if the line is required for the entire data cycle.
22	DACK0*	DMA Acknowledge 0 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
23	LA18	Latchable Address 18 – Refer to LA17 pin-21, for more information.
24	IRQ14	Interrupt Request 14 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
25	LA19	Latchable Address 19 – Refer to LA17 pin-21, for more information.
26	IRQ15	Interrupt Request 15 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
27	LA20	Latchable Address 20 – Refer to LA17 pin-21, for more information.
28	IRQ12	Interrupt Request 12 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
29	LA21	Latchable Address 21– Refer to LA17 pin-21, for more information.
30	IRQ11	Interrupt Request 11 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
31	LA22	Latchable Address 22 – Refer to LA17 pin-21, for more information.
32	IRQ10	Interrupt Request 10 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
33	LA23	Latchable Address 23 – Refer to LA17 pin-21, for more information.
34	IO16*	I/O Chip Select 16 – This signal is driven low by an I/O slave device to indicate it is capable of performing a 16-bit I/O data transfer. This signal is driven from a decode of the SA15 to SA0 address lines.
35, 36	GND	Ground
37	SBHE*	System Byte High Enable – This signal is driven low to indicate a transfer of data on the high half of the data bus (D15 to D8).
38	M16*	Memory Chip Select 16 – This is signal is driven low by a memory slave device to indicates it is cable of performing a 16-bit memory data transfer. This signal is driven from a decode of the LA23 to LA17 address lines.
39	SA0	System Address 0 – These signals (0 to 19) provide system address bits.
40	OSC	Oscillator – This clock signal operates at 14.3 MHz. This signal is not synchronous with the system clock (SYSCLK).
41	SA1	System Address 1– Refer to SA0 pin-39, for more information.
42	BALE	Buffered Address Latch Enable – This signal is used to latch the LA23 to LA17 signals or decodes of these signals. Addresses are latched on the falling edge of BALE. It is forced high during DMA cycles. When used with AENx, it indicates a valid processor or DMA address.
43	SA2	System Address 2 – Refer to SA0 pin-39, for more information.
44	TC	Terminal Count – This signal is a pulse to indicate a terminal count has been reached on a DMA channel operation.

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J2 Pin #	Signal	Description
45	SA3	System Address 3 – Refer to SA0 pin-39, for more information.
46	DACK2*	DMA Acknowledge 2 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
47	SA4	System Address 4 – Refer to SA0 pin-39, for more information.
48	IRQ3	Interrupt Request 3 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
49	SA5	System Address 5 – Refer to SA0 pin-39, for more information.
50	IRQ4	Interrupt Request 4 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
51, 52	VCC	DC Power – +5 volts +/- 5%
53	SA6	System Address 6 – Refer to SA0 pin-39, for more information.
54	IRQ5	Interrupt Request 5 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
55	SA7	System Address 7 – Refer to SA0 pin-39, for more information.
56	IRQ6	Interrupt Request 6 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
57	SA8	System Address 8 – Refer to SA0 pin-39, for more information.
58	IRQ7	Interrupt Request 7 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
59	SA9	System Address 9 – Refer to SA0 pin-39, for more information.
60	SYSCLK	System Clock – This is a free running clock typically in the 8 MHz to 10 MHz range, although its exact frequency is not guaranteed.
61	SA10	System Address 10 – Refer to SA0 pin-39, for more information.
62	REFSH*	Memory Refresh – This signal is driven low to indicate a memory refresh cycle is in progress. Memory is refreshed every 15.6 usec.
63	SA11	System Address 11 – Refer to SA0 pin-39, for more information.
64	DREQ1	DMA Request 1– Used by I/O resources to request DMA service. Must be held high until associated DACK1 line is active.
65	SA12	System Address 12 – Refer to SA0 pin-39, for more information.
66	DACK1*	DMA Acknowledge 1 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
67, 68	GND	Ground
69	SA13	System Address 13 – Refer to SA0 pin-39, for more information.
70	DREQ3	DMA Request 3 – Used by I/O resources to request DMA service. Must be held high until associated DACK3 line is active.
71	SA14	System Address 14 – Refer to SA0 pin-39, for more information.
72	DACK3*	DMA Acknowledge 3 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.

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J2 Pin #	Signal	Description
73	SA15	System Address 15 – Refer to SA0 pin-39, for more information.
74	IOR*	I/O Read – This strobe signal is driven by the owner of the bus (ISA bus master or DMA controller) and instructs the selected I/O device to drive read data onto the data bus.
75	SA16	System Address 16 – Refer to SA0 pin-39, for more information.
76	IOW*	I/O Write – This strobe signal is driven by the owner of the bus (ISA bus master or DMA controller) and instructs the selected I/O device to capture the write data on the data bus.
77	SA18	System Address 18 – Refer to SA0 pin-39, for more information.
78	SA17	System Address 17 – Refer to SA0 pin-39, for more information.
79	SA19	System Address 19 – Refer to SA0 pin-39, for more information.
80	SMEMR*	System Memory Read – This signal is used by bus owner to request a memory device to drive data onto the data bus and only active for lower 1 MB. Used for legacy compatibility with 8-bit cards.
81	IOCHRDY	I/O Channel Ready – This signal allows slower ISA boards to lengthen I/O or memory cycles by inserting wait states. This signal's normal state is active high (ready). ISA boards drive the signal inactive low (not ready) to insert wait states. Devices using this signal to insert wait states should drive it low immediately after detecting a valid address decode and an active read, or write command. The signal is released high when the device is ready to complete the cycle.
82	AEN	Address Enable – This signal is used to degate the system processor and other devices from the bus during DMA transfers. When this signal is active, the system DMA controller has control of the address, data, and read/write signals. This signal should be included as part of ISA board select decodes to prevent incorrect board selects during DMA cycles.
83, 84	VCC	DC Power – +5 volts +/- 5%
85	SD0	System Data 0 – Refer to SD14 pin-3, for more information.
86	SMEMW*	System Memory Write – This signal is used by bus owner to request a memory device to store data currently on the data bus and only active for the lower 1 MB. Used for legacy compatibility with 8-bit cards.
87	SD2	System Data 2 – Refer to SD14 pin-3, for more information.
88	SD1	System Data 1 – Refer to SD14 pin-3, for more information.
89	SD3	System Data 3 – Refer to SD14 pin-3, for more information.
90	NOWS*	No Wait State – This signal is driven low by a bus slave device to indicate it is capable of performing a bus cycle without inserting any additional wait states. To perform a 16-bit memory cycle without wait states, this signal is derived from an address decode.
91	DREQ2	DMA Request 2 – Used by I/O resources to request DMA service. Must be held high until associated DACK2 line is active.
92	SD4	System Data 4 – Refer to SD14 pin-3, for more information.
93	SD5	System Data 5 – Refer to SD14 pin-3, for more information.
94	IRQ9	Interrupt Request 9 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
95	SD6	System Data 6 – Refer to SD14 pin-3, for more information.

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J2 Pin #	Signal	Description
96	SD7	System Data 7 – Refer to SD14 pin-3, for more information.
97	IOCHK*	I/O Channel Check – This signal may be activated by ISA boards to request that a non-maskable interrupt (NMI) be generated to the system processor. It is driven active to indicate an uncorrectable error has been detected.
98	RSTDRV	Reset Drive – This signal is used to reset or initialize system logic on power up or subsequent system reset.
99	GND	Ground
100	GND	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

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Primary I/O Interface (J3)

The J3 connector has 100 pins and is used for Floppy or Printer (LPT1) interface, Serial interfaces (COM1 and COM2), Mouse and Keyboard interfaces, Infrared (IrDA) interface, and the video interfaces for standard CRT video and LVDS interfaces.

Floppy Interface

The Floppy interface shares signal lines with the Parallel interface and is provided by the Super I/O chip (LPC47B272). The BIOS settings determine which one is operational. A Standard 34-pin floppy drive connector is listed in Table 3-10 for reference along with the J3 connector pins. This type of connector can be located on the custom baseboard if desired.

- Supports two floppy drives
- 16 bytes of FIFO with data rates up to 1 Mbps

Table 3-10. Simplified Floppy Drive Interface Pin/Signal Descriptions (J3)

J3 Pin #	Signal	34 Pin Cable	Description
51	LPT/FLPY*	NC	Parallel/Floppy Select – This signal selects the parallel or floppy port signals. If this signal is Low at boot time, the floppy drive is selected. If signal is High at boot time, the parallel port is selected. This state can not be changed until the next boot cycle.
56	DENSEL*	2	Drive Density Select – This signal indicates if a low (250/300 kbps) or high (500 kbps/1 Mbps) data rate is selected.
NC	NC	4	NC
NC	KEY	6	Key – Not connected
80	INDEX*	8	Index – This signal indicates when head is positioned over the beginning of a track or index hole.
62	MTR0*	10	Motor Control 0 – Select motor on drive 0.
55	DS0*	12	Drive Select 0 – Selects drive 0.
84	DS1*	14	Drive Select 1 – Selects drive 1.
86	MTR1*	16	Motor Control 1 – Select motor on drive 1.
64	DIR*	18	Direction – Direction of head movement (0 = inward motion, 1 = outward motion).
70	STEP*	20	Step – Low pulse for each track-to-track movement of the head.
88	WDATA*	22	Write Data – Sends encoded data to drive for write operations.
90	WGATE*	24	Write Enable – Signal enables current flow in write head of drive.
78	TRK0	26	Track 0 – Sensor detects head is positioned over track 0.
76	WPT	28	Write Protect – Senses the diskette is write protected.
74	RDATA*	30	Read Data – Raw serial bit stream from the drive for read operations.
60	HDSEL*	32	Head Select – Selects the side for Read/Write operations (0 = side 1, 1 = side 0)
72	DSKCHG*	34	Disk Change – Senses the drive door is open or the diskette has been changed since the last drive selection.
66	GND	all odd	Ground (1-33)

Notes: The shaded area denotes power or ground. The signals marked with * indicate active low.

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Parallel Interface

Parallel interface supports standard parallel, Bi-directional, ECP and EPP protocols. The Super I/O chip (LPC47B272) provides the parallel interface signals, which are shared with the floppy drive interface.

- The Parallel interface shares signal lines with the Floppy interface and the BIOS settings determine which one is operational.
- Supports Standard Printer Port (SPP), Enhanced Parallel Port (EPP) and Enhanced Capabilities Port (ECP)

A standard parallel interface cable pin-out is listed in Table 3-11 for reference along with the J3 connector pins. A DB25 connector can be located on the custom baseboard if desired.

Table 3-11. Simplified Parallel Interface (SPP) Pin/Signal Descriptions (J3)

J3 Pin #	Signal	DB25 Pin #	Description
51	LPT/ FLPY*	NC	Parallel/Floppy Select – This signal selects the parallel or floppy port signals. If this signal is Low at boot time, the floppy drive is selected. If signal is High at boot time, the parallel port is selected. This state can not be changed until the next boot cycle.
55	Strobe*	1	Strobe – Output signal strobes data into the printer. I/O pin in ECP/EPP mode.
80	PD0	2	Parallel Port Data 0 – These signals <0 to 7> provide parallel port data signals and this signal is the LSB of the printer data.
78	PD1	3	Parallel Port Data 1 – Refer to J3, pins-80 & -58 for more information.
76	PD2	4	Parallel Port Data 2 – Refer to J3, pins-80 & -58 for more information
74	PD3	5	Parallel Port Data 3 – Refer to J3, pins-80 & -58 for more information
72	PD4	6	Parallel Port Data 4 – Refer to J3, pins-80 & -58 for more information
68	PD5	7	Parallel Port Data 5 – Refer to J3, pins-80 & -58 for more information
62	PD6	8	Parallel Port Data 6 – Refer to J3, pins-80 & -58 for more information
58	PD7	9	Parallel Port Data 7 – This signal provides a parallel port data signal and is the MSB of the printer data.
84	ACK*	10	Acknowledge – A status input signal from the printer. A Low State indicates it has received the data and is ready to accept new data.
86	BUSY*	11	Busy – A status input signal from the printer. A high state indicates the printer is not ready to accept data.
88	PE	12	Paper End – A status input signal from the printer. A high state indicates it is out of paper.
90	SLCT*	13	Select – A status output signal from the printer. A high state indicates it is selected and powered on.
56	AFD*	14	Auto Feed – A output signal from the printer to automatically feed one line after each line is printed.
60	ERR*	15	Error – A status output signal from the printer. A low state indicates an error condition on the printer.
64	INIT*	16	Initialize – This signal initializes the printer. Output in standard mode, I/O in ECP/EPP mode.
70	SLCTIN*	17	Select In – Output signal selects the printer. I/O pin in ECP/EPP mode.
66	GND	18-25	Ground

Notes: The shaded area denotes power or ground. The signals marked with * indicate active low.

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Serial Ports 1 and 2

The Super I/O chip (LPC47B272) provides the circuitry for two serial port UARTs with TTL compatible signals. The signals for serial ports 1 and 2 are provided to the baseboard through connector J3. However, the baseboard must provide the serial transceivers to make use of this feature. The serial port features are:

- Two individual 16550-compatible UARTs
- Programmable word length, stop bits and parity
- 16-bit programmable baud rate generator and Interrupt generator
- Loop-back mode
- Two individual 16-bit FIFOs

The standard serial DB9 cable pin-outs are listed in Table 3-12 for reference along with the J3 connector pins. DB9 connectors can be designed onto the custom baseboard, as the application requires.

Table 3-12. Simplified Serial Interface Pin/Signal Descriptions (J3)

J3 Pin #	Pin # DB9	Signal	Description
89	1 (COM1)	DCD1*	Data Carrier Detect 1 – Indicates external serial device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input is driven by DTR1 as part of the DTR1/DSR1 handshake.
91	6	DSR1*	Data Set Ready 1 – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR1 for overall readiness.
83	2	RXD1	Receive Data 1 – Serial port 1 receive data in.
85	7	RTS1*	Request To Send 1 – Indicates Serial port 1 is ready to transmit data. Used as hardware handshake with CTS1 for low level flow control.
95	3	TXD1	Transmit Data 1 – Serial port 1 transmit data out.
93	8	CTS1*	Clear To Send 1 – Indicates external serial device is ready to receive data. Used as hardware handshake with RTS1 for low level flow control.
87	4	DTR1*	Data Terminal Ready 1 – Indicates Serial port 1 is powered, initialized, and ready. Used as hardware handshake with DSR1 for overall readiness.
97	9	RI1*	Ring Indicator 1 – Indicates external serial device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
	5	GND	Ground
71	1 (COM2)	DCD2*	Data Carrier Detect 2 – Indicates external serial device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input is driven by DTR2 as part of the DTR2/DSR2 handshake.
73	6	DSR2*	Data Set Ready 2 – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR2 for overall readiness.
63	2	RXD2	Receive Data 2 – Serial port 2 receive data in
67	7	RTS2*	Request To Send 2 – Indicates Serial port 2 is ready to transmit data. Used as hardware handshake with CTS2 for low level flow control.
77	3	TXD2	Transmit Data 2 – Serial port 2 transmit data out.

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J3 Pin #	Pin # DB9	Signal	Description
75	8	CTS2*	Clear To Send 2 – Indicates external serial device is ready to receive data. Used as hardware handshake with RTS2 for low level flow control.
69	4	DTR2*	Data Terminal Ready 2 – Indicates Serial port 2 is powered, initialized, and ready. Used as hardware handshake with DSR2 for overall readiness.
79	9	RI2*	Ring Indicator 2 – Indicates external serial device is detecting a ring condition. Used by software to initiate operations to answer and then open the communications channel.
	5	GND	Ground

Notes: The shaded area denotes power or ground.

Infrared (IrDA) Port

The Infrared Data Association (IrDA) port provides two-way wireless communications port signals using infrared as a transmission medium at the basic level. However, the custom baseboard must provide the infrared (IrDA) transceiver to implement this feature. There are two basic infrared implementations provided; the Hewlett-Packard Serial Infrared (HPSIR) and the Amplitude Shift Keyed Infrared (ASKIR) methods. HPSIR is a serial implementation of infrared developed by Hewlett-Packard. The IrDA (HPSIR and ASKIR) signals share Serial Port 2 with the modem and RS232 functions on the port. This port can be enabled/disabled and configured for HPSIR or ASKIR signals in the BIOS Setup Utility. Refer to *Advanced Settings* in Chapter 4, *BIOS Setup Utility* for more information.

The HPSIR method allows serial communication at baud rates up to 115 k baud. Each word is sent serially beginning with a zero value start bit. A zero is sent when a single infrared pulse is sent at the beginning of the serial bit time. A one is sent when no infrared pulse is sent during the bit time.

The Amplitude Shift Keyed infrared (ASKIR) allows serial communication at baud rates up to 19.2 k baud. Each word is sent serially beginning with a zero value start bit. A zero is sent when a 500 kHz waveform is sent for the duration of the serial bit time. A one is sent when no transmission is sent during the serial bit time.

Both of these methods require an understanding of the timing diagrams provided in the Super I/O controller (LPC47B272) specifications available from the manufacture's web site and referenced earlier in this manual. For more information, refer to the Standard Microsystems LPC47B272 databook and the Infrared Data Association web site at http://www.irda.org.

NOTE	For infrared applications not covered in this brief description, refer to the LPC47B272 chip specifications by Standard Microsystems, Inc.

PS/2 Keyboard

The signal lines for a PS/2 keyboard are provided through the J3 connector from the Super I/O chip (LPC47B272).

PS/2 Mouse

The signal lines for a PS/2 mouse are provided through the J3 connector from Super I/O chip (LPC47B272).

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Table 3-13. Simplified Keyboard, Mouse, and Infrared (IrDA) Port Pin/Signal Descriptions (J3)

J3 Pin #	Signal	Description
	VCC	DC Power – +5 volt Keyboard/Mouse power
98	KBDAT	Keyboard Data signal – This signal provides the keyboard data.
96	KBCLK	Keyboard Clock signal – This signal provides the clocks to the keyboard.
94	MSDAT	Mouse Data signal – This signal provides the mouse data.
92	MSCLK	Mouse Clock signal – This signal clocks the data from the mouse.
	GND	Signal Ground
61	IRTx	IR Transmit Data (HPSIR or ASKIR)
59	IRRx	IR Receive Data (HPSIR or ASKIR)

Notes: The shaded area denotes power or ground.

CRT Interface

- Graphic controller is integrated in the Memory Hub (82855GME) chip.
- Maximum resolution for CRT output is 1600x1200 x 32 with full use of 64 MB Unified Memory Architecture (UMA).

Table 3-14. Simplified CRT Interface Pin/Signal Descriptions (J3)

J3 Pin #	Signal	VGA 15-Pin #	Description
3	RED	1	Red – This is the Red analog output signal to the CRT.
6	GREEN	2	Green – This is the Green analog output signal to the CRT.
4	BLUE	3	Blue – This is the Blue analog output signal to the CRT.
	NC	4, 11	Not Connected
	GND	5, 10	Ground
	GND	6, 7, 8	Ground Return – Red return, Green return, and Blue return
	VCC	9	DC Power – +5 volts +/- 5%
10	DDDA	12	Display Data Channel Data – This signal line provides information to the Memory Hub about the monitor type, brand, model. This is part of the Plug n' Play standard developed by the VESA trade association.
5	HSYNC	13	Horizontal Sync – Used as digital horizontal sync output to the CRT.
7	VSYNC	14	Vertical Sync – Used as digital vertical sync output to the CRT.
8	DDCLK	15	Display Data Channel Clock – This signal line provides the data clock signal to the Memory Hub from the monitor. This is part of the Plug and Play standard developed by the VESA trade association.

Notes: The shaded area denotes power or ground.

LVDS Interface

The Memory Hub provides direct LVDS outputs. This output is independent of other panel interfaces. The LVDS interface will support 1 or 2 channels. A single channel interface uses the Y[2:0]+, Y[2:0]-, and YCLK+ and YCLK- outputs. The second LVDS interface is assigned the Z[2:0]+, Z[2:0]-, and ZCLK+ and ZCLK- outputs.

Table 3-15. Simplified LVDS Interface Pin/Signal Descriptions (J3)

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J3 Pin #	Signal	Description	Line	Channel
	GND	Ground	NA	NA
37	LVDS_Y0M	Data Negative Output	0	Channel 1
35	LVDS_Y0P	Data Positive Output		
38	LVDS_Y1M	Data Negative Output	1	
36	LVDS_Y1P	Data Positive Output		
29	LVDS_Y2M	Data Negative Output	2	
31	LVDS_Y2P	Data Positive Output		
32	LVDS_CLKYM	Clock Negative Output	Clock	
30	LVDS_CLKYP	Clock Positive Output		
23	LVDS_Y3M	Data Negative Output	3	
25	LVDS_Y3P	Data Positive Output		
26	LVDS_Z0P	Data Negative Output	0	Channel 2
24	LVDS_Z0P	Data Positive Output		
19	LVDS_Z1M	Data Negative Output	1	
17	LVDS_Z1P	Data Positive Output		
20	LVDS_Z2M	Data Negative Output	2	
18	LVDS_Z2P	Data Positive Output		
11	LVDS_CLKZM	Clock Negative Output	Clock	
13	LVDS_CLKZP	Clock Positive Output		
12	LVDS_Z3P	Data Negative Output	3	
14	LVDS_Z3P	Data Positive Output		
41	FP_I^2C_DAT	Flat Panel I^2C Data – I^2C data interface to flat panel parameter EEPROM.		
43	FP_I^2C_CLK	Flat Panel I^2C Clock – I^2C clock interface to flat panel parameter EEPROM.		
44	BLON*	Backlight On – Control signal for external flat panel backlight power.		
45	BIASON	BIAS ON – Flat panel contrast voltage control.		
46	DIGON	Digital Power-On – Digital flat panel power on control.		

Notes: The shaded area denotes power or ground.

NOTE The necessary voltages to drive a flat panel are not supplied through the J3 connector on the ETX 802 module. The required drive voltages for the flat panel must be designed into the customer's baseboard and supplied from the ATX or AT power supply to provide drive voltages for the LVDS connector to the flat panel.

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Table 3-16. Complete J3 Interface Pin/Signal Descriptions (J3)

J3 Pin #	Signal	Description
1, 2	GND	Ground
3	Red	Red – This is the Red analog output signal to the CRT.
4	Blue	Blue – This is the Blue analog output signal to the CRT.
5	HSYNC	Horizontal Sync – This signal is used for the digital horizontal sync output to the CRT.
6	Green	Green – This is the Green analog output signal to the CRT.
7	VSYNC	Vertical Sync – This signal is used for the digital vertical sync output to the CRT.
8	DDCK	Display Data Channel Clock – This signal line provides the data clock signal to the Memory Hub from the monitor. This is part of the Plug and Play standard developed by the VESA trade association.
9	NC	Not Connected (DETECT*)
10	DDDA	Display Data Channel Data – This signal line provides information to the Memory Hub about the monitor type, brand, model. This is part of the Plug and Play standard developed by the VESA trade association.
11	LVDS_ZClk-	Clock Negative Output, Clock, Channel 2
12	LVDS_Z3-	Data Negative Output, Line 3, Channel 2
13	LVDS_ZClk+	Clock Positive Output, Clock, Channel 2
14	LVDS_Z3+	Data Positive Output, Line 3, Channel 2
15, 16	GND	Ground
17	LVDS_Z1+	Data Positive Output, Line 1, Channel 2
18	LVDS_Z2+	Data Positive Output, Line 2, Channel 2
19	LVDS_Z1-	Data Negative Output, Line 1, Channel 2
20	LVDS_Z2-	Data Negative Output, Line 2, Channel 2
21, 22	GND	Ground
23	LVDS_Y3-	Data Negative Output, Line 3, Channel 1
24	LVDS_Z0+	Data Positive Output, Line 0, Channel 2
25	LVDS_Y3+	Data Positive Output, Line 3, Channel 1
26	LVDS_Z0-	Data Negative Output, Line 0, Channel 2
27, 28	GND	Ground
29	LVDS_Y2-	Data Negative Output, Line 2, Channel 1
30	LVDS_YClk+	Clock Positive Output, Clock, Channel 1
31	LVDS_Y2+	Data Positive Output, Line 2, Channel 1
32	LVDS_YClk-	Clock Negative Output, Clock, Channel 1
33, 34	GND	Ground
35	LVDS_Y0+	Data Positive Output, Line 0, Channel 1
36	LVDS_Y1+	Data Positive Output, Line 1, Channel 1
37	LVDS_Y0-	Data Negative Output, Line 0, Channel 1
38	LVDS_Y1-	Data Negative Output, Line 1, Channel 1

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J3 Pin #	Signal	Description
39, 40	VCC	DC Power – +5V +/- 5%
41	FP_I^{2}C_DAT	Flat Panel I^{2}C Data – This is the I^{2}C data interface to the parameter EEPROM used with the flat panel
42	NC	Not Connected (LTGIO0)
43	FP_I^{2}C_CLK	Flat Panel I^{2}C Clock – This is the I^{2}C clock interface to the parameter EEPROM used with the flat panel.
44	BLON*	Backlight On – This signal controls the external backlight power for the flat panel.
45	BIASON	BIAS ON – This signal controls the flat panel contrast voltage.
46	DIGON	Digital Power On – This signal controls the digital flat panel power up.
47	NC	Not Connected (Composite Analog Output)
48	NC	Not Connected (S-Video Y Analog Output)
49	NC	Not Connected (Sync Output)
50	NC	Not Connected (S-Video C Analog Output)
51	LPT/FLPY*	Parallel/Floppy Select – This signal selects the parallel or floppy port signals. If this signal is Low at boot time, the floppy drive is selected. If this signal is High at boot time, the parallel port is selected. This state can not be changed until the next boot cycle.
52	NC	Not Connected (Reserved)
53	VCC	DC Power – +5 volts +/- 5%
54	GND	Ground
55	Strobe*	Parallel Strobe – This output signal is used to strobe data into the printer. I/O pin in ECP/EPP mode.
	DS0*	Floppy Drive Select 0 – Selects drive 0.
56	AFD*	Parallel Auto Feed – This is a output signal from the printer to automatically feed one line after each line is printed.
	DENSEL	Floppy Drive Density Select – This signal indicates if a low (250/300 kbps) or high (500/1 kbps) data rate is selected.
57	NC	Not Connected (Reserved)
58	PD7	Parallel Port Data 7 – This signal (0 to 7) provides a parallel port data signal and is the printer data MSB.
59	IRRX	IR Receive Data (HPSIR or ASKIR)
60	ERR*	Parallel Error – This is a status output signal from the printer. A low state indicates an error condition on the printer.
	HDSEL*	Floppy Head Select – Selects floppy diskette side for Read/Write operations (0 = side 1, 1 = side 0).
61	IRTX	IR Transmit Data (HPSIR or ASKIR)
62	PD6	Parallel Port Data 5 – Refer to pin-58 and 80 for more information.
	MTR0*	Floppy Motor Control 0 – Select motor on drive 0.
63	RXD2	Receive Data 2 – Serial port 2 receive data in.

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J3 Pin #	Signal	Description
64	INIT*	Parallel Initialize – This signal initializes the printer. Output in standard mode, I/O in ECP/EPP mode.
	DIR*	Floppy Direction – Direction of head movement (0 = inward motion, 1 = outward motion).
65, 66	GND	Ground
67	RTS2*	Request To Send 2 – Indicates Serial port 2 is ready to transmit data. Used as hardware handshake with CTS2 for low level flow control.
68	PD5	Parallel Port Data 5 – Refer to pin-58 and 80 for more information.
69	DTR2*	Data Terminal Ready 2 – Indicates Serial port 2 is powered, initialized, and ready. Used as hardware handshake with DSR2 for overall readiness.
70	SLCTIN	Parallel Select In – This output signal is used to select the printer. I/O pin in ECP/EPP mode.
	STEP*	Floppy Step – Low pulse for each track-to-track movement of the head.
71	DCD2*	Data Carrier Detect 2 – Indicates external serial device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input is driven by DTR2 as part of the DTR2/DSR2 handshake.
72	PD4	Parallel Port Data 4 – Refer to pin-58 and 80 for more information.
	DSKCHG*	Floppy Disk Change – Senses the drive door is open or the diskette has been changed since the last drive selection.
73	DSR2*	Data Set Ready 2 – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR2 for overall readiness.
74	PD3	Parallel Port Data 3 – Refer to pin-58 and 80 for more information.
	RDATA*	Floppy Read Data – Raw serial bit stream from drive for read operations.
75	CTS2*	Clear To Send 2 – Indicates external serial device is ready to receive data. Used as hardware handshake with RTS2 for low level flow control.
76	PD2	Parallel Port Data 2 – Refer to pin-58 and 80 for more information.
	WPT*	Floppy Write Protect – Senses the diskette is write protected.
77	TXD2	Transmit Data 2 – Serial port 2 transmit data out.
78	PD1	Parallel Port Data 1 – Refer to pin-58 and 80 for more information.
	TRK0*	Floppy Track 0 – Sensor detects when head is positioned over track 0.
79	RI2*	Ring Indicator 2 – Indicates external serial device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
80	PD0	Parallel Port Data 0 – This pin (0 to 7) provides a parallel port data signal and is the printer data LSB.
	INDEX*	Floppy Index – Sense to detect that the head is positioned over the beginning of a track.
81, 82	VCC	+5 volts +/- 5%
83	RXD1	Receive Data 1 – Serial port 1 receive data in.
84	ACK*	Parallel Acknowledge – This is a status input signal from the printer. A Low State indicates it has received the data and is ready to accept new data.
	DR1	Floppy Drive Select 1 – This signal selects drive 1.

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J3 Pin #	Signal	Description
85	RTS1*	Request To Send 1 – Indicates Serial port 1 is ready to transmit data. Used as hardware handshake with CTS1 for low level flow control.
86	BUSY	Parallel Busy – This is a status input signal from the printer. A high state indicates the printer is not ready to accept data.
	MTR1	Floppy Motor Control 1 – This signal selects motor on drive 1.
87	DTR1*	Data Terminal Ready 1 – Indicates Serial port 1 is powered, initialized, and ready. Used as hardware handshake with DSR1 for overall readiness.
88	PE	Parallel Paper End – This is a status input signal from the printer. A high state indicates it is out of paper.
	WDATA*	Floppy Write Data – Sends encoded data to drive for write operations.
89	DCD1*	Data Carrier Detect 1 – Indicates external serial device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input is driven by DTR1 as part of the DTR1/DSR1 handshake.
90	SLCT	Parallel Select – This is a status output signal from the printer. A high state indicates it is selected and powered on.
	WGATE*	Floppy Write Enable – Signal enables current flow in drive write head.
91	DSR1*	Data Set Ready 1 – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR1 for overall readiness.
92	MSCLK	Mouse Clock signal – This signal clocks the data from the mouse.
93	CTS1*	Clear To Send 1 – Indicates external serial device is ready to receive data. Used as hardware handshake with RTS1 for low level flow control.
94	MSDAT	Mouse Data signal – This signal provides the mouse data.
95	TXD1	Transmit Data 1 – Serial port 1 transmit data out.
96	KBCLK	Keyboard Clock signal – This signal clocks the data from the keyboard.
97	RI1*	Ring Indicator 1 – Indicates external serial device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
98	KBDAT	Keyboard Data signal – This signal provides the keyboard data.
99	GND	Ground
100	GND	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

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IDE and Auxiliary Interface (J4)

The J4 connector has 100 pins and is used for Primary IDE, Secondary IDE, Ethernet port, RTC/Battery, speaker, power management, SMBus, and miscellaneous power interface signals.

IDE Ports

- Supports 2 EIDE channels (Primary and Secondary)
- Supports EIDE Ultra DMA 33/66/100 in Master Mode
- Supports ATAPI compliant devices including DVD devices
- Supports PIO IDE transfers up to 14 Mbytes/sec
- Supports IDE Bus Master transfers up to 100 Mbytes/sec

The standard 40-pin cable pin-outs are listed in Tables 3-17 and 3-18 for reference along with the J4 connector pins. One or both channels can be routed to the IDE connector or a compact flash socket on a custom baseboard per the application requirements.

Table 3-17. Simplified Primary IDE Interface Pin/Signal Descriptions (J4)

J4 Pin #	Signal	40-Pin #	Description
98	HDRST*	1	Hard Reset – Low active hardware reset (RSTDRV inverted)
	GND	2	Ground
96	PIDE_D7	3	Disk Data 7– These signals (0 to 15) provide the disk data signals
92	PIDE_D8	4	Disk Data 8 – Refer to D7, pin-3, for more information.
88	PIDE_D6	5	Disk Data 6 – Refer to D7, pin-3, for more information.
86	PIDE_D9	6	Disk Data 9 – Refer to D7, pin-3, for more information.
84	PIDE_D5	7	Disk Data 5 – Refer to D7, pin-3, for more information.
80	PIDE_D10	8	Disk Data 10 – Refer to D7, pin-3, for more information.
78	PIDE_D4	9	Disk Data 4 – Refer to D7, pin-3, for more information.
76	PIDE_D11	10	Disk Data 11 – Refer to D7, pin-3, for more information.
74	PIDE_D3	11	Disk Data 3 – Refer to D7, pin-3, for more information.
72	PIDE_D12	12	Disk Data 12 – Refer to D7, pin-3, for more information.
70	PIDE_D2	13	Disk Data 2 – Refer to D7, pin-3, for more information.
68	PIDE_D13	14	Disk Data 13 – Refer to D7, pin-3, for more information.
64	PIDE_D1	15	Disk Data 1 – Refer to D7, pin-3, for more information.
62	PIDE_D14	16	Disk Data 14 – Refer to D7, pin-3, for more information.
60	PIDE_D0	17	Disk Data 0 – Refer to D7, pin-3, for more information.
58	PIDE_D15	18	Disk Data 15 – Refer to D7, pin-3, for more information.
	GND	19	Ground
	Key	20	Key pin plug
56	PIDE_DRQ	21	DMA Request – Used for DMA transfers between host and drive (direction of transfer controlled by IOR and IOW). Also used in an asynchronous mode with ACK. Drive asserts an IRQ when ready to transfer or receive data.
	GND	22	Ground

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J4 Pin #	Signal	40-Pin #	Description
54	PIDE_IOW*	23	Drive I/O Write – Strobe signal for write functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
	GND	24	Ground
52	PIDE_IOR*	25	Drive I/O Read – Strobe signal for read functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
	GND	26	Ground
48	PIDE_RDY	27	I/O Channel Ready – When negated extends the host transfer cycle of any host register access when the drive is not ready to respond to a data transfer request. High impedance if asserted.
90	CBLID_P*	28	Cable ID Select – Detects the presence of an 80 conductor IDE cable on the primary IDE channel. This allows BIOS or system software to determine if is necessary to enable high-speed transfer modes (DMA66 or DMA100).
46	PIDE_AK*	29	DMA Channel Acknowledge – Used by the host to acknowledge data has been accepted or data is available. Used in response to DMARQ asserted.
	GND	30	Ground
44	PIDE_INTRQ	31	Drive Interrupt Request (IRQ 14) – Asserted by drive when a pending interrupt exist (PIO transfer of data to or from the drive to the host).
	NC	32	Not Connected (IOCS16*)
40	PIDE_A1	33	Drive Address Bus 1 – Used <0 to 2> to indicate which byte in the ATA command block or control block (register) is being accessed.
	NC	34	Not Connected (Passed Diagnostics)
38	PIDE_A0	35	Drive Address Bus 0 – Refer to J4, pin-40, for more information.
36	PIDE_A2	36	Drive Address Bus 2 – Refer to J4, pin-40, for more information.
32	PIDE_CS1*	37	Chip Select 0 – Selects host-accessible Command Block Register.
30	PIDE_CS3*	38	Chip Select 1 – Selects host-accessible Command Block Register.
	NC	39	Not Connected (Drive Active/Drive Present)
	GND	40	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

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Table 3-18. Simplified Secondary IDE Interface Pin/Signal Descriptions (J4)

J4 Pin #	Signal	40-Pin #	Description
	NC	1	Not Connected (Hard Reset)
	GND	2	Ground
94	SIDE_D7	3	Disk Data – These signals <0 to 15> provide the disk data signals.
87	SIDE_D8	4	Disk Data 8 – Refer to D7, pin-3, for more information.
85	SIDE_D6	5	Disk Data 6 – Refer to D7, pin-3, for more information.
83	SIDE_D9	6	Disk Data 9 – Refer to D7, pin-3, for more information.
79	SIDE_D5	7	Disk Data 5 – Refer to D7, pin-3, for more information.
77	SIDE_D10	8	Disk Data 10 – Refer to D7, pin-3, for more information.
75	SIDE_D4	9	Disk Data 4 – Refer to D7, pin-3, for more information.
73	SIDE_D11	10	Disk Data 11 – Refer to D7, pin-3, for more information.
71	SIDE_D3	11	Disk Data 3 – Refer to D7, pin-3, for more information.
69	SIDE_D12	12	Disk Data 12 – Refer to D7, pin-3, for more information.
67	SIDE_D2	13	Disk Data 2 – Refer to D7, pin-3, for more information.
63	SIDE_D13	14	Disk Data 13 – Refer to D7, pin-3, for more information.
61	SIDE_D1	15	Disk Data 1 – Refer to D7, pin-3, for more information.
59	SIDE_D14	16	Disk Data 14 – Refer to D7, pin-3, for more information.
57	SIDE_D0	17	Disk Data 0 – Refer to D7, pin-3, for more information.
55	SIDE_D15	18	Disk Data 15 – Refer to D7, pin-3, for more information.
	GND	19	Ground
	Key	20	Key pin plug
53	SIDE_DRQ	21	DMA Request – Used for DMA transfers between host and drive (direction of transfer controlled by IOR and IOW). Also used in an asynchronous mode with ACK. Drive asserts an IRQ when ready to transfer or receive data.
	GND	22	Ground
51	SIDE_IOW*	23	Drive I/O Write – Strobe signal for write functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
	GND	24	Ground
47	SIDE_IOR*	25	Drive I/O Read – Strobe signal for read functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
	GND	26	Ground
45	SIDE_RDY	27	I/O Channel Ready – When negated extends the host transfer cycle of any host register access when the drive is not ready to respond to a data transfer request. High impedance if asserted.
	NC	28	Not Connected (Cable ID)
43	SIDE_AK*	29	DMA Channel Acknowledge – Used by the host to acknowledge data has been accepted or data is available. Used in response to DMARQ asserted.
	GND	30	Ground

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J4 Pin #	Signal	40-Pin #	Description
39	SIDE_INTRQ	31	Drive Interrupt Request (IRQ 15) – Asserted by drive when a pending interrupt exist (PIO transfer of data to or from the drive to the host).
	NC	32	Not Connected (IOCS16*)
37	SIDE_A1	33	Drive Address Bus 1 – Used <0 to 2> to indicate which byte in the ATA command block or control block (register) is being accessed.
35	SPDIAG*	34	Passed Diagnostics – Used for Master/Slave negotiation on the Secondary IDE channel. If it is asserted by the Slave, indicates to master, slave has passed its internal Diagnostics command. If a compact flash is connected to the baseboard, this signal must be routed to the SDASP pin of any other device connected to the Secondary IDE channel. This pin may also be used to detect the presence of an 80 conductor IDE cable, which is required for support of the DMA66 or DMA100 high-speed transfers.
31	SIDE_A0	35	Drive Address Bus 0 – Refer to J4, pin-37, for more information.
29	SIDE_A2	36	Drive Address Bus 2 – Refer to J4, pin-37, for more information.
27	SIDE_CS1*	37	Chip Select 0 – Selects host-accessible Command Block Register.
25	SIDE_CS3*	38	Chip Select 1 – Selects host-accessible Command Block Register.
28	SDASP*	39	Drive Active/Drive Present – This signal is time-multiplexed and indicates the secondary drive is present and active. If a compact flash is connected to the baseboard, this signal must be routed to the SDASP pin of any other device connected to the Secondary IDE channel. Can also used for Master/Slave negotiation on the Secondary IDE channel.
	GND	40	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

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Ethernet Port Interface

The Ethernet solution is provided by an Intel 82551QM Fast Ethernet PCI controller chip, which consists of both the Media Access Controller (MAC) and the physical layer (PHY) combined into a single component solution. The 82551QM is a 32-bit PCI controller that features enhanced scatter-gather bus mastering capabilities, which enables the 82551QM to perform high-speed data transfers over the PCI bus. The 82551QM bus master capabilities enable the component to process high-level commands and perform multiple operations, thereby off-loading communication tasks from the system CPU.

- Routed to J4 connector
- Low power 3.3 V device
- Backward software compatible to the 82559, 82558, and 82557
- Chained memory structure
- Supports full duplex or half-duplex operation
- Supports full duplex operation at 10 Mbps and 100 Mbps
- Supports half-duplex mode with enhanced performance by a proprietary collision reduction mechanism
- Provides IEEE 802.3 10BaseT/100BaseT compatible physical layer
- Supports data transmission with minimum interframe spacing (IFS).
- Supports IEEE 802.3u Auto-Negotiation
- Provides 3 KB transmit and 3 KB receive FIFOs (helps prevent data underflow and overflow)
- Provides IEEE 802.3x 100BASE-TX flow control
- Improved dynamic transmit chaining with multiple priorities transmit queues
- Supports an Ethernet port RJ-45 connector and the magnetics on the baseboard only

Table 3-19. Simplified Ethernet Port Pin/Signal Descriptions (J4)

J4 Pin #	Signal	Description
97	TX+	Analog Twisted Pair Ethernet Transmit Differential Pair – These pins transmit the serial bit stream on the Unshielded Twisted Pair Cable (UTP).
95	TX-	
93	RX+	Analog Twisted Pair Ethernet Receive Differential Pair – These pins receive the serial bit stream on the Unshielded Twisted Pair Cable (UTP).
91	RX-	
	GND	Ground
10	LILED	Link Integrity LED – The Link LED pin indicates link integrity. If the link is valid in either 10 or 100 Mbps, the LED is on; if the link is invalid, the LED is off.
12	ACTLED	Activity LED – The Activity LED pin indicates either transmit or receive activity. When activity is present, the activity LED is on; when no activity is present, the activity LED is off.
14	SPDLED	Speed LED – The Speed LED pin indicates the speed. The speed LED will be on at 100 Mbps and off at 10 Mbps.

Notes: The shaded area denotes power or ground.

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Power Control Signals

The ETX 802 supports various power control signals provided through the baseboard to control the ETX 802 and the power supply. These signals are listed here and in Tables 3-20 and 3-22.

- The Power Good input signal (PWGIN) is provided from an external input typically from the external power supply (ATX) to the baseboard. This signal is typically an active-high input to the ETX baseboard and indicates to the ETX module it can begin the boot process. This Power Good signal can also be used as an active-low reset input to the ETX module.
- The Power Suspend signal (5V_SB) must be provided through the power supply interface for standby operation, typically an ATX power supply. The power supply must provide a 5 volt 100 mA stand-by power source for this function to be available.
- The Power On signal (PS_ON) is provided by the ETX module to the PS_ON input of an ATX power supply allowing it to switch to main output power from a standby state. This signal is used in conjunction with the 5V_SB supplied to the ETX module from the ATX power supply.
- The Power Button Input signal (PWRBTN*) provides a ground temporally through a momentary-contact switch or through an open collector driver to the ATX power supply. This signal is used in conjunction with the PS_ON and the 5V_SB signals from the ATX power supply to activate the power control function of the power supply.
- A voltage monitor on the ETX 802 tracks the VCC voltage (+5 volts) state by monitoring the +3.3V generated on the ETX module. When the +3.3V drops below 3.0V or the Reset Button signal goes low, the voltage monitor sends a reset pulse to the Memory Hub (82855GME), the I/O Hub (82801DBM), and the CPU.

Power Management Signals

The ETX 802 supports various power management signals listed below and in Tables 3-20 and 3-22.

- The External System Management Interrupt (EXTSMI) signal is routed to the baseboard through J4 to allow external circuitry to initiate an SMI for the EXT module.
- The Resume Reset input (RSMRST*) signal to the EXT module may be driven low by external control circuitry to reset the power management logic on the ETX module.
- The System Management Bus Alert input (SMBALRT*) signal is used by SMBus devices to indicate an event on the SMBus to the EXT module.
- The Battery Low input (BATLOW*) signal is used by external voltage monitoring circuitry to indicate the system battery is low to the ETX module.

Speaker

The signal lines for a speaker port with 0.1-watt drive are provided through J4 connector to the baseboard where the speaker must be located.

- The I/O Hub (82801DBM, Southbridge) provides the speaker output signal, but the output drive circuit must be implemented on the baseboard.

Real Time Clock (RTC)/Battery

The ETX 802 supports a Real Time Clock (RTC) and CMOS RAM for the BIOS Setup Utility. The RTC and 256 byte of CMOS RAM are included inside the I/O Hub (82801DBM). The RTC and CMOS are backed up through the BAT pin on J4 with a Lithium Battery located on the baseboard. If the battery is not present, the BIOS has a battery-free boot option to complete the boot process.

Table 3-20. Simplified Power Control and Miscellaneous Pin/Signal Descriptions (J4)

J4 Pin #	Signal	Description

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J4 Pin #	Signal	Description
3	5V_SB	5 volt Suspend – This control signal is sent to the ATX power supply for a suspended or standby state.
4	PWGIN	Power Good In – This active high input signal indicates to the ETX 802, the ATX power is good and it can begin the boot process.
5	PS_ON	Power Supply On – This active-low output signal from the ETX 802 is sent to the ATX power supply to turn the ATX power supply on.
7	PWRBTN*	Power Button – This pin provides a ground temporally through an open collector driver to the ATX power supply to change states (turn it on).
6	SPEAKER	Speaker – This PC speaker output signal must be connected to a speaker (piezoelectric or dynamic) on the baseboard to hear the output (beeps).
11	RSMRST	Resume Reset – This signal is driven low by external circuitry to reset the power management logic on the ETX 802.
19	OVCR	Over Current Detect – This signal indicates a USB over-current condition.
8	BAT	Battery Voltage – This is the + battery connection to baseboard for +3 volt lithium backup battery used for RTC operation and CMOS non-volatile memory.
41	BATLOW*	Battery Low – This external signal to the ETX 802 indicates when the external battery voltage is low.
21	EXTSMI	External System Management Interrupt – This signal is provided by external circuitry to initiate an SMI event with the ETX 802.
23	SMBCLK	System Management Bus Clock – This signal is used to support internal and external SMBus devices, such as temperature and battery monitoring.
24	SMBDATA	System Management Bus Data – This signal is used to support internal and external SMBus devices, such as temperature and battery monitoring.
26	SMBALRT*	System Management Bus Alert – This signal is used by SMBus devices to signal an event on the SM Bus.

SMBus (I^2C Bus)

The I/O Hub (82801DBM) contains an integrated SMBus controller with both a host and slave SMBus port; but the host cannot access the slave internally. The slave port allows an external master access to the I/O Hub through the J4 connector. The master contained in the I/O Hub is used to communicate with the SEEP, SDRAM EPROM, ADM1023 (thermal monitor), and the clock generator. Table 3-21 list the addresses for these devices with the components and corresponding binary addresses of the SMBus.

- The I^2C slave address must not be the same as the I^2C device on the baseboard.

Table 3-21. SMBus Reserved Addresses

Matrix Component	Address Binary
Configuration SEEP	$1010,010x_b$
SDRAM EPROM	$1010,000x_b$
Clock Generator (ICS950811)	$1101,001x_b$
I/O Hub (82801DBM)	$0000,000x_b$ (default) Programmable
Thermal monitor (ADM1023)	$0011,000\ x_b$

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Table 3-22. Complete J4 Interface Pin/Signal Descriptions (J4)

J4 Pin #	Signal	Description
1, 2	GND	Ground
3	5V_SB	5 volt Suspend – This control signal is sent to the ATX power supply for a suspended or standby state.
4	PWGIN	Power Good In – This active high input signal indicates to the ETX 802, the power is good and it can begin the boot process.
5	PS_ON	Power Supply On – This active-low output signal from the ETX 802 is sent to the ATX power supply from the to turn it on.
6	SPEAKER	Speaker – This PC speaker output signal must be connected to a speaker (piezoelectric or dynamic) on the baseboard to hear the output (beeps).
7	PWRBTN*	Power Button – This signal provides a ground temporally through an open collector driver to the ATX power supply to change states (turn it on).
8	BATT	Battery Voltage – This is the + battery connection to baseboard for +3 volt lithium backup battery used for RTC operation and CMOS non-volatile memory.
9	NC	Not Connected (KBINH)
10	LILED	Link Integrity LED – The LINK LED pin indicates link integrity. If the link is valid in either 10 or 100Mbps, the LED is on; if the link is invalid, the LED is off.
11	RSMRST*	Resume Reset – This signal is driven low by external circuitry to reset the power management logic on the ETX 802.
12	ACTLED	Activity LED – The Activity LED pin indicates either transmit or receive activity. When activity is present, the activity LED is on; when no activity is present, the activity LED is off.
13	NC	Not Connected (ROMKBCS*)
14	SPDLED	Speed LED – The speed LED pin indicates the speed. The speed LED will be on at 100 Mbps and off at 10 Mbps.
15	NC	Not Connected (EXT_PRG)
16	NC	Not Connected (I^2CLK)
17, 18	VCC	DC Power – +5 volts +/-5%
19	OVCR*	Over Current Detect – This signal indicates a USB over-current condition.
20	NC	Not Connected (GPCS*)
21	EXTSMI*	Extern System Management Interrupt – This signal is provided by external circuitry to initiate an SMI event with the ETX 802.
22	NC	Not Connected (I^2DAT)
23	SMBCLK	System Management Bus Clock – This signal is used to support internal and external SMBus devices, such as temperature and battery monitoring.
24	SMBDATA	System Management Bus Data – This signal is used to support internal and external SMBus devices, such as temperature and battery monitoring.
25	SIDE_CS3*	Secondary Chip Select 1 – Selects host-accessible Command Block Register.
26	SMBALRT*	System Management Bus Alert – This signal is used by SMBus devices to signal an event on the SMBus.
27	SIDE_CS1*	Secondary Chip Select 0 – Selects host-accessible Command Block Register.

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J4 Pin #	Signal	Description
28	SDASP	Drive Active/Drive Present – This signal is time-multiplexed and indicates the secondary drive is present and active. If a compact flash is connected to the baseboard, this signal must be routed to the SDASP pin of any another device connected to the Secondary IDE channel. May also be used for Master/Slave negotiation on the Secondary IDE channel.
29	SIDE_A2	Secondary Drive Address Bus 2 – Used <0 to 2> to indicate which byte in the ATA command block or control block (register) is being accessed.
30	PIDE_CS3*	Primary Chip Select 1 – Selects host-accessible Command Block Register.
31	SIDE_A0	Secondary Drive Address Bus 0 – Refer to J4, pin-29, for more information.
32	PIDE_CS1*	Primary Chip Select 0 – Selects host-accessible Command Block Register.
33, 34	GND	Ground
35	SPDIAG	Passed Diagnostics – This signal is used for Master/Slave negotiation on the Secondary IDE channel. It is asserted by the Slave to indicate to master that the slave has passed its internal Diagnostics command. If a compact flash is connected to the baseboard, this signal must be routed to the SDASP pin of any another device connected to the Secondary IDE channel. May also be used to detect the presence of an 80-conductor IDE cable, which is required for support of the DMA66 or DMA100 high-speed transfers.
36	PIDE_A2	Primary Drive Address Bus 2 – Used <0 to 2> to indicate which byte in the ATA command block or control block (register) is being accessed.
37	SIDE_A1	Secondary Drive Address Bus 1 – Refer to J4, pin-29, for more information.
38	PIDE_A0	Primary Drive Address Bus 0 – Refer to J4, pin-36, for more information.
39	SIDE_INTRQ	Secondary Drive Interrupt Request (IRQ 15) – Asserted by drive when it has pending interrupt (PIO transfer of data to or from the drive to the host).
40	PIDE_A1	Primary Drive Address Bus 1 – Refer to J4, pin-36, for more information.
41	BATLOW*	Battery Low – This external signal to the ETX 802 indicates when the external battery is low.
42	NC	Not Connected (GPE1*)
43	SIDE_AK*	Secondary DMA Channel Acknowledge – Used by the host to acknowledge data has been accepted or data is available. Used in response to SIDE_DMARQ when asserted.
44	PIDE_INTRQ	Primary Drive Interrupt Request (IRQ 14) – Asserted by drive when it has pending interrupt (PIO transfer of data to or from the drive to the host).
45	SIDE_RDY	Secondary I/O Channel Ready – When negated extends the host transfer cycle of any host register access when the drive is not ready to respond to a data transfer request. High impedance if asserted.
46	PIDE_AK*	Primary DMA Channel Acknowledge – Used by the host to acknowledge data has been accepted or data is available. Used in response to PIDE_DMARQ when asserted.
47	SIDE_IOR*	Secondary Drive I/O Read – Secondary strobe signal for read functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
48	PIDE_RDY	Primary I/O Channel Ready – When negated extends the host transfer cycle of any host register access when the drive is not ready to respond to a data transfer request. High impedance if asserted.
49, 50	VCC	DC Power – +5 volts +/-5%

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J4 Pin #	Signal	Description
51	SIDE_IOW*	Secondary Drive I/O Write – Secondary strobe signal for write functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
52	PIDE_IOR*	Primary Drive I/O Read – Primary strobe signal for read functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
53	SIDE_DRQ	Secondary DMA Request – Used for DMA transfers between host and drive (direction of transfer controlled by IOR* and IOW*). Also used in an asynchronous mode with ACK*. Drive asserts an IRQ when ready to transfer or receive data.
54	PIDE_IOW*	Primary Drive I/O Write – Primary strobe signal for write functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
55	SIDE_D15	Secondary Disk Data 15 – These signals <0 to 15> provide the Secondary IDE disk data signals.
56	PIDE_DRQ	Primary DMA Request – Used for DMA transfers between host and drive (direction of transfer controlled by IOR* and IOW*). Also used in an asynchronous mode with ACK*. Drive asserts an IRQ when ready to transfer or receive data.
57	SIDE_D0	Secondary Disk Data 15 – Refer to J4, pin-55 for more information.
58	PIDE_D15	Primary Disk Data 15 – These signals (0 to 15) provide the Primary IDE disk data signals.
59	SIDE_D14	Secondary Disk Data 15 – Refer to J4, pin-55 for more information.
60	PIDE_D0	Primary Disk Data 0 – Refer to J4, pin-58 for more information.
61	SIDE_D1	Secondary Disk Data 15 – Refer to J4, pin-55 for more information.
62	PIDE_D14	Primary Disk Data 14 – Refer to J4, pin-58 for more information.
63	SIDE_D13	Secondary Disk Data 15 – Refer to J4, pin-55 for more information.
64	PIDE_D1	Primary Disk Data 1 – Refer to J4, pin-58 for more information.
65, 66	GND	Ground
67	SIDE_D2	Secondary Disk Data 15 – Refer to J4, pin-55 for more information.
68	PIDE_D13	Primary Disk Data 13 – Refer to J4, pin-58 for more information.
69	SIDE_D12	Secondary Disk Data 15 – Refer to J4, pin-55 for more information.
70	PIDE_D2	Primary Disk Data 2 – Refer to J4, pin-58 for more information.
71	SIDE_D3	Secondary Disk Data 15 – Refer to J4, pin-55 for more information.
72	PIDE_D12	Primary Disk Data 12 – Refer to J4, pin-58 for more information.
73	SIDE_D11	Secondary Disk Data 15 – Refer to J4, pin-55 for more information.
74	PIDE_D3	Primary Disk Data 3 – Refer to J4, pin-58 for more information.
75	SIDE_D4	Secondary Disk Data 15 – Refer to J4, pin-55 for more information.
76	PIDE_D11	Primary Disk Data 11 – Refer to J4, pin-58 for more information.
77	SIDE_D10	Secondary Disk Data 15 – Refer to J4, pin-55 for more information.
78	PIDE_D4	Primary Disk Data 4 – Refer to J4, pin-58 for more information.
79	SIDE_D5	Secondary Disk Data 15 – Refer to J4, pin-55 for more information.
80	PIDE_D10	Primary Disk Data 10 – Refer to J4, pin-58 for more information.

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J4 Pin #	Signal	Description
81, 82	VCC	DC Power – +5 volts +/-5%
83	SIDE_D9	Secondary Disk Data 15 – Refer to J4, pin-55 for more information.
84	PIDE_D5	Primary Disk Data 5 – Refer to J4, pin-58 for more information.
85	SIDE_D6	Secondary Disk Data 15 – Refer to J4, pin-55 for more information.
86	PIDE_D9	Primary Disk Data 9 – Refer to J4, pin-58 for more information.
87	SIDE_D8	Secondary Disk Data 15 – Refer to pin-55 for more information.
88	PIDE_D6	Primary Disk Data 6 – Refer to J4, pin-58 for more information.
89	NC	Not Connected (GPE2*)
90	PCBLID*	Primary Cable ID Select – Used to detects the presence of an 80 conductor IDE cable on the primary IDE channel. This allows BIOS or system software to determine if is necessary to enable the high-speed transfer modes (DMA66 or DMA100).
91	RXD-	Half of Ethernet Analog Twisted Pair Receive Differential Pair – This pin and pin-93 make up the Receive twisted pair and receive the serial bit stream on the Unshielded Twisted Pair Cable (UTP).
92	PIDE_D8	Primary Disk Data 8 – Refer to J4, pin-58 for more information.
93	RXD+	Part of Ethernet Analog Twisted Pair Receive Differential Pair – Refer to pin-91 for more information.
94	SIDE_D7	Secondary Disk Data 15 – Refer to J4, pin-55 for more information.
95	TXD-	Half of Ethernet Analog Twisted Pair Transmit Differential Pair – This pin and pin-97 make up the Transmit twisted pair and transmit the serial bit stream on the Unshielded Twisted Pair Cable (UTP).
96	PIDE_D7	Primary Disk Data 7 – Refer to J4, pin-58 for more information.
97	TXD+	Part of Ethernet Analog Twisted Pair Transmit Differential Pair – Refer to pin-95 for more information.
98	HDRST*	Hard Reset – Low active hardware reset (RSTDRV inverted)
99	GND	Ground
100	GND	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

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Miscellaneous

Oops! Jumper (BIOS Recovery)

The Oops! jumper is provided in the event the BIOS settings you've selected prevent you from booting the system. By using the Oops! jumper you can prevent the current BIOS settings in the Flash memory from being loaded, forcing the use of the default settings. Connect the DTR pin to the RI pin on serial port 1 (COM 1) on the baseboard prior to boot up to prevent the present BIOS settings from loading. After booting with the Oops! jumper in place, remove the Oops! jumper from the baseboard connector and go into the BIOS Setup Utility. Change the desired BIOS settings, or select the default settings, and save changes before rebooting the system.

To convert a standard DB9 connector to a Oops! jumper for use on the custom baseboard, short together the DTR (4) and RI (9) pins on the rear of the connector as shown in Figure 3-1 on the Serial Port 1 DB9 connector.

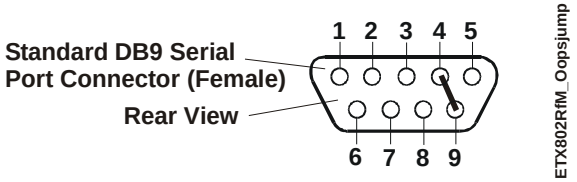


Figure 3-1. Oops! Jumper Connection

Serial Console (Remote Access)

The BIOS Setup Utility supports the serial console (or console redirection) feature, but refers to it as Remote Access. This I/O function can be accessed by an ANSI-compatible serial terminal, or the equivalent terminal emulation software running on another system. This can be very useful when setting up the BIOS on a production line for systems that are not connected to a keyboard and display (sometimes referred to as a headless system).

Serial Console Setup

The serial console feature is implemented by connecting a standard null modem cable or a modified serial cable (or "Hot Cable") between one of the serial ports, such as Serial 1 or Serial 2, and the serial terminal or a PC with communications software. The BIOS Setup Utility controls the serial console settings for the ETX 802. Refer to *Accessing BIOS Setup Utility (Remote Access/Serial Console)* and *Advanced* settings, in Chapter 4, *BIOS Setup Utility* for the Remote Access option to set the serial terminal, or PC with communications software.

Hot (Serial) Cable

To convert a standard serial cable to a Hot Cable for use on the custom baseboard, two pins must be shorted together at the Serial port DB9 connector. Short together the RTS (7) and RI (9) pins on Serial port DB9 connector as shown in Figure 3-2.

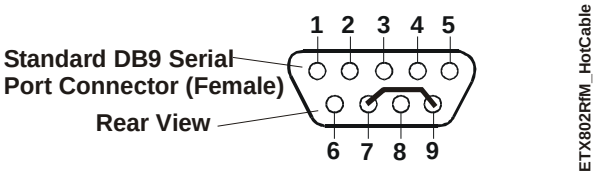


Figure 3-2. Hot Cable Jumper

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Temperature Monitoring

The temperature monitoring function is preformed by Analog Devices, ADM1023 chip and it takes an input connection from the thermal diode in the Intel Celeron M or Pentium M CPU. The ADM1023 chip uses the two-wire SMBus interface to communicate with the other devices on the SMBus, including the I/O Hub (82801DBM).

NOTE	The ETX 802 requires a heatsink for all Intel CPUs and the Memory Hub (Northbridge), but no fan, below +70° C. The 1.4 GHz Pentium M requires a fan for extended temperatures (+70° to +85° C).

Watchdog Timer (WDT)

The watchdog timer (WDT) restarts the system if an error or mishap occurs, allowing the system to recover from the mishap, even though the error condition may still exist. Possible problems include failure to boot properly, loss of control by the application software, failure of an interface device, unexpected conditions on the bus, or other hardware or software malfunctions.

The WDT (watchdog timer) can be used both during the boot process and during normal system operation.

- During the Boot process – If the operating system fails to boot in the time interval set in the BIOS, the system will reset.

  The watchdog timer (WDT) is enabled and configured in the *Boot* settings screen of the BIOS Setup Utility. Set the WDT for a time-out interval in seconds, between 1 and 255, in one second increments. Ensure you allow enough time for the operating system to boot. The OS or application must tickle (reset) the WDT before the timer expires. This can be done by accessing the hardware directly or through a BIOS call.

- During System Operation – An application can set up the WDT hardware through a BIOS call, or by accessing the hardware directly. Some Ampro Board Support Packages provide an API interface to the WDT. The application must tickle (reset) the WDT before the timer expires or the system will be reset. The BIOS implements interrupt 15 function 0C3h to manipulate the WDT.

- Watchdog Code examples – Ampro will provide code examples on the ETX 802 Doc & SW CD-ROM illustrating how to control the WDT in the final release.

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Power Interface

The ETX 802 draws its input voltage (+5V) through the four connectors (X1, X2, X3, X4) on the custom baseboard, which requires an external power supply, typically an ATX power supply or other power source as the application requires. The ETX 802 generates its own internal voltages onboard, including the CPU core voltages and requires the externally supplied +5 volts DC +/- 5%.

The –5V, –12V, +12V and +3.3V voltages used for the PCI and ISA buses and the LVDS video connector are supplied to the baseboard and ETX 802 module from the externally connected power supply, typically an ATX power supply.

Optional CPU Fan (P1)

Table 3-23 lists the pins and signals of the optional CPU Fan and it has 3 pins, single row, with 0.100" pin spacing.

Table 3-23. CPU Fan (P1)

Pin #	Signal	Description
1	GND	Ground
2	+5	+5.0 volts DC +/- 5%
3	Fan_Tach	Fan Speed Tachometer

Note: The shaded area denotes power or ground.

Power and Sleep States

The following information only applies if an ATX power supply is connected to the ETX baseboard where the ETX 802 is installed. If a non-ATX power supply is used, then the ETX 802 is only controlled by the Power-On/Off switch on the power supply and the various sleep states are not available. The ACPI sleep states are OS dependent and not available if your OS does not support power management based on the ACPI standard. The signals used for control of the ATX power supply and sleep states in general is located in Table 3-20 and described in more detail under *topics Power Control Signals* and *Power Management Signals* earlier in this chapter.

Power-On Switch

The Power-On switch, on or connected to the ETX Baseboard, turns the ETX 802 and its attached power supply to a fully On condition, if you are using an ATX power supply and an OS that supports sleep states. If the operating system (OS) supports sleep states, the OS will turn off the ETX 802 and its power supply during the OS shut down process. Typically, the Power-On switch will also transition the ETX 802, the ETX baseboard, and its power supply between a fully powered on state and the various sleep states, including a fully powered off state. If the OS does not support sleep states, then the Power-On switch only turns power, On or Off, to the ETX 802 and its baseboard.

Typically, an OS that supports ACPI, also allows the Power-On switch to be configured through a user interface. The Power-On switch for the ETX 802 must be provided on, or connected to the baseboard.

Sleep States (ACPI)

The ETX 802 supports the ACPI (Advanced Configuration and Power Interface) standard, which is a key component of certain Operating Systems' (OS's) power management. The supported features (sleep states) listed here are only available when an ACPI-compliant OS is used for the ETX 802, such as Windows 2000/XP. The term "sleep" state refers to a low wake latency (reduced power consumption) state, which can be re-started (awakened) restoring full operation to the ETX 802.

In these various sleep states, the computer appears to be off, indicated by such things as no display on the attached monitor and no activity for the connected CD-ROM or hard drives. Normally, when a

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computer detects certain activity (i.e. power switch, mouse, keyboard, serial port, or certain types of LAN activity), it returns to a fully operational state.

NOTE	Currently, the Power-On switch, Wake-on-Ring, Wake-on-LAN, Wake on RTX alarm, Wake on PME, and Keyboard/Mouse activity are the only activities that will wake the ETX 802 from a powered down state, such as Standby (S1), Suspend-to-RAM (S3), Hibernate (S4) and Power Off (S5). However, not all of the listed activities will wake each sleep state. Refer to the ETX 802 Software and Hardware Release Notes for more information.

The ETX 802 supports at least five ACPI power states, depending on the operating system used and its ability to manage sleep states. Typically, the Power-On switch is used to wake up from a sleep state, or transition from one state to another, but this is dependent on the operating system.

- 1st state is normal Power On (S0).
  - To go to a fully powered on state, the ETX 802 must either be powered Off (S5), or in a sleep state (S1 or S4), and then the Power-On switch is pressed for less than 4 seconds (default).
  - The ETX 802 can transition from this state (S0) to the various states described below, depending on the power management capability of the OS and how it is programmed.
- 2nd state is a standby state (S1).

  In this state there are internal operations taking place, including the internal RTC (real time clock), contents of RAM, activity for the CPU, but the external peripherals, such as hard disk drives, CD-ROMs, and monitor are off. The ETX 802 appears to be on due to the Power-On LED.
  - Normally, to enter this sleep state, the ETX 802 must be fully powered on (S0) and the OS transitions the ETX 802 into this standby state (S1) under user control.
  - To exit this sleep state a wake up event, such as the Power-On switch, is used to wake up the ETX 802 and restore full operation, including the Power-On LED. Typically, pressing the Power-On switch for less than 4 seconds (default) will restore full operation.
- 3rd state is a suspend-to-RAM state (S3).

  This sleep state stores your open files and programs in RAM before powering down. In this state there are no internal operations taking place, except for the internal RTC (real time clock) and low power level keeping the contents of RAM alive. This includes no activity for the CPU and external peripherals, such as hard disk drives or CD-ROMs. The ETX 802's Power-On LED is off, but the S3 Mode LED is turned on only when in S3 Mode. This state is only safe as long as you have power to your system. If power is lost to the ATX power supply or the battery fails, then the contents of RAM is lost, including any open applications and data files. This state is quicker than S4, but much more volatile.
  - Normally, to enter this sleep state, the ETX 802 must be fully powered on (S0) and the OS transitions the ETX 802 into this suspend-to-RAM (S3) state under user control.
  - To exit this sleep state a wake up event, such as the Power-On switch, is used to wake up the ETX 802 and restore full operation, including the Power-On LED, but the S3 Mode LED turns off. Typically, pressing the Power-On switch for less than 4 seconds (default) will restore full operation.

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- 4th state is a hibernate or suspend-to-disk state (S4).

  This condition stores the state of your system (open files and programs) on the hard disk drive before powering down. In this state there are no internal operations taking place, except for the internal RTC. This includes no activity for the RAM, CPU, and external peripherals, such as hard disk drives or CD-ROMs. The ETX 802 appears to be off, including the Power-On LED and the S3 Mode LED. Your system will take longer to wake-up in this sleep state than S3, but since your data is saved to the disk, it is more secure and should not be lost in the event of a power failure.

  - To enter a hibernate or suspend-to-disk state, the ETX 802 must be fully powered on and the OS transitions the ETX 802 into this sleep state (S4) under user control.
  - To exit this sleep state a wake up even, such as the Power-On switch, is used to wake up the ETX 802 and restore full operation, including the Power-On LED. Typically, pressing the Power-On switch for less than 4 seconds (default) will restore full operation.

- 5th state is the normal power Off or shutdown (S5).

  All activity stops except the internal clock, unless the power cord is removed from the power source.

  - To go to a fully powered down state, the ETX 802 must either be powered On, or in a sleep state, and then the Power-On switch is pressed for more than 4-to-6 seconds.
  - To go to a fully powered up state, press the Power-On switch for less than 4 seconds (default) and full operation is restored.

The OS may provide additional programming features to change the activation time for each state, and to shutdown or transition the ETX 802 at certain times, depending on the way the OS interface is programmed. Refer to the OS vender's documentation for power management conditions under the ACPI standard.

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Chapter 4 BIOS Setup Utility

Introduction

This chapter describes the BIOS Setup Utility menus and the various screens used for configuring the ETX 802. Some features in the Operating System or application software may require configuration in the BIOS Setup Utility screens.

This section assumes the user is familiar with general BIOS Setup and does not attempt to describe the BIOS functions. Refer to the appropriate PC reference manuals for information about the onboard ROM-BIOS software interface. If Ampro has added to or modified the standard functions, these functions will be described.

The options provided for the ETX 802 are controlled by BIOS Setup. BIOS Setup is used to configure the board, modify the fields in the Setup screens, and save the results in the onboard configuration memory. Configuration memory consists of portions of the CMOS RAM in the battery-backed real-time clock chip and the flash memory.

The Setup information is retrieved from configuration memory when the board is powered up or when it is rebooted. Changes made to the Setup parameters, with the exception of the time and date settings, do not take effect until the board is rebooted.

Setup is located in the ROM BIOS and can be accessed while the board is in the Power-On Self Test (POST) state, just before starting the boot process. Typically, the screen displays a message indicating when you can press <Del> to enter the BIOS Setup Utility.

The ETX 802 BIOS Setup Utility is used to configure items in the BIOS using the following menus:

- Main
- Advanced
- PCIPnP
- Boot
- Security
- Chipset
- Power
- Exit

Table 4-1 summarizes the list of BIOS menus and some of the features available for ETX 802. The BIOS Setup menu offers the menu choices listed above and the related topics and screens are described on the following pages.

Accessing BIOS Setup Utility (VGA Display)

To access the BIOS Setup Utility using a VGA display for the ETX 802:

1. Turn on the VGA monitor and the power supply to the ETX 802.
2. Start Setup by pressing the [Del] key, when the following message appears on the boot screen.

```
Hit <Del> if you want to run SETUP
```

NOTE	If the setting for *Quick Boot* is set to [Enabled], you may not see this prompt appear on screen if the monitor is too slow to display it on start up. If this happens, press the <Del> key early in the boot sequence to enter the BIOS Setup Utility.

3. Use the <Enter> key to select the screen menus listed in the Opening BIOS screen. See Figure 4-1.
4. Follow the instructions at the bottom of each screen to navigate through the selections and modify any settings.

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Accessing BIOS Setup Utility (Remote Access)

Once you set up the BIOS Utility for Remote Access (serial console or console redirection) in VGA mode, entering the BIOS in the remote access mode, is very similar to the method used when entering the BIOS with a VGA display.

1. Turn on the power supply to the ETX 802 and baseboard to access the BIOS Setup Utility in VGA mode.
2. Set the BIOS feature *Remote Access* to [Enabled] under the **Advanced** menu.
3. Accept the default options or make your own selections for the balance of the Remote Access fields and record your settings.
4. Ensure you select the type of remote serial terminal you will be using and record your selection.
5. Select *Save Changes and Exit* and then shut down the ETX 802 and baseboard.
6. Connect the remote serial terminal (or the PC with communications software) to the COM port you selected on the ETX 802 using a Hot Cable or a standard null-modem serial cable.
7. Turn on the remote serial terminal (or the PC with communications software) and set it to the settings you selected and recorded earlier in the BIOS Setup Utility.

   COM1, 115200, 8 bits, 1 stop bit, no parity, no flow control, and [Always] for *Redirection After BIOS POST* are the default settings for the ETX 802.
8. Restore power to the ETX 802 and look for the screen prompt shown below.

```
Hit ^C if you want to run SETUP
```

9. Press the CTRL–C keys to enter Setup early in the boot sequence, especially if *Quick Boot* is set to [Enabled].

   If *Quick Boot* is set to [Enabled], you may never see the screen prompt.
10. Use the <Enter> key to select the screen menus listed in the Opening BIOS screen. See Figure 4-1.

NOTE	The serial console port is not hardware protected, and is not listed in the COM table within BIOS Setup Utility. Diagnostic software that probes hardware addresses may cause a loss or failure of the serial console functions.

Table 4-1. BIOS Setup Utility Menus

BIOS Setup Utility Menu	Item/Topic
Main Settings	Date and Time
Advanced Settings	CPU Configuration, IDE Configuration, Floppy Configuration, Super I/O Configuration, ACPI Configuration, MPS Configuration, Smbios Configuration, Remote Access (Serial Console) Configuration, and USB Configuration
PCIPnP (PCI, Plug n' Play)	PCI settings, Plug & Play settings, Interrupt settings and DMA channel settings, Reserved memory
Boot	Boot up Settings Configuration, Boot Device Priority, Removable Drives
Security	Setting or changing Supervisor/User Passwords, Boot Sector Virus Protection
Chipset	Northbridge Configuration, Southbridge Configuration
Power	Power Management/APM and Resume Power conditions
Exit	Exiting with or without changing settings, Loading Optimal or Fail-safe conditions

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BIOS Setup Utility Menus

Main Menu Screen

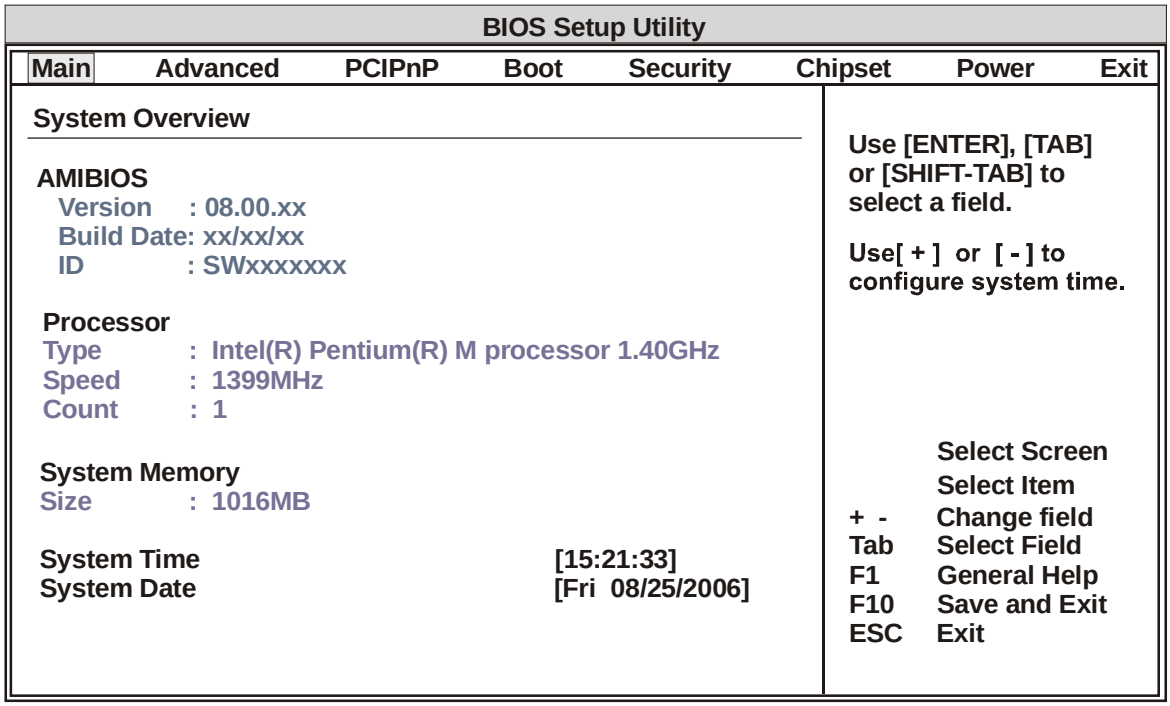


Figure 4-1. Main Menu Screen

System Overview

- **Date & Time**
  - System Time (hh:mm:ss) – This is a 24-hour clock setting in hours, minutes, and seconds
  - System Date (day of week, mm:dd:yyyy) – This field requires the alpha-numeric entry of the day of week, calendar month, day of the month, and all 4 digits of the year, indicating the century plus year (*Fri 02/14/2006*).

NOTE	The Optimal Default values are shown highlighted as **bold text** and the Fail-safe Defaults are shown highlighted as *italic text* in the list of options. In many cases the Optimal values are the same as the Fail-safe values, so you will see text options as ***italic*** and ***bold*** text at the same time. Refer to the right of the BIOS screens for navigation and selection instructions not listed in the following table.

Table 4-2. Exiting and Loading Default Keys

Key	Description
F7	Discard Changes without leaving BIOS Setup
F8	Load failsafe default settings.
F9	Load optimal default settings.
F10	Save Changes and Exit BIOS Setup

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Advanced Menu Screen

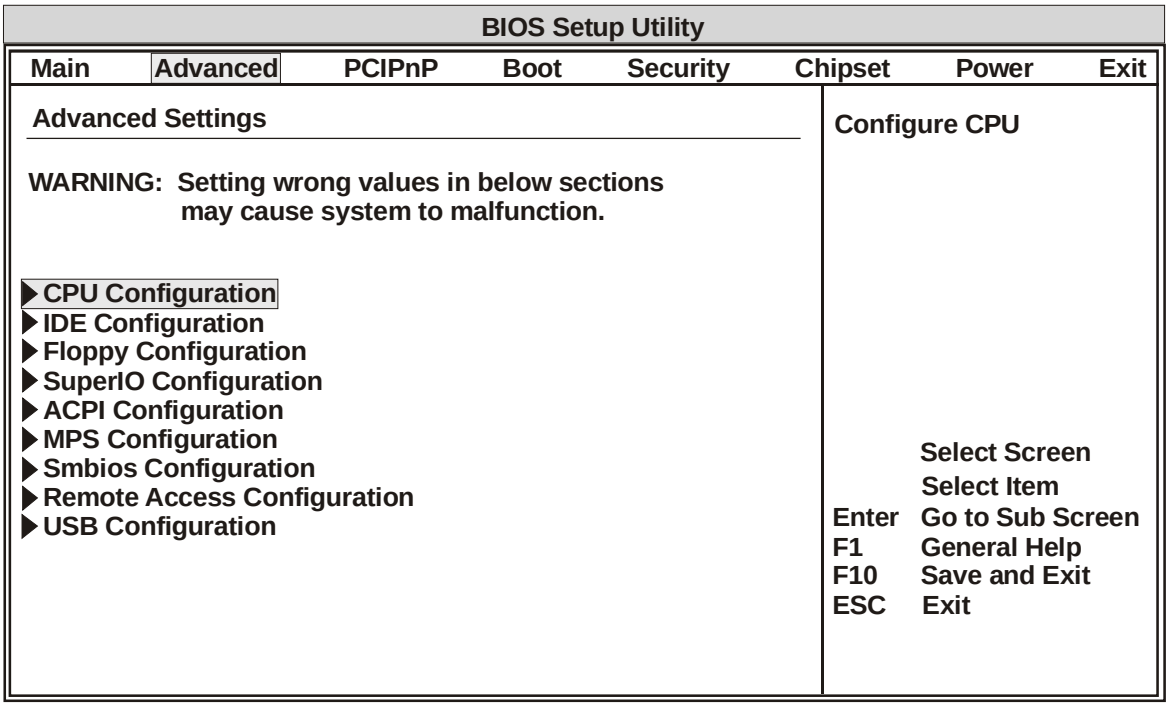


Figure 4-2. Advanced Menu Screen

Advanced Settings

>CPU Configuration

Configure advanced CPU settings
Module version - 11.05

Manufacture	: Intel
Brand String	: Intel® Pentium® M processor 1.40GHz
Frequency	: 1.39GHz
FSB Speed	: 400MHz
Cache L1	: 32kB
Cached L2	: 2048kB

- Intel® SpeedStep(™) Technology – [**Maximum Speed**], [Minimum Speed], [Automatic], or [Disabled]

  This feature is only available for the Pentium CPU.

  Intel® Mobile Pentium® Processors with Intel® SpeedStep™ technology lets you customize high performance computing on your mobile PC. When the ETX 802 is connected to the power, the ETX 802 COM will run applications with speed virtually identical to a desktop system. When powered by a battery, the processor drops to a lower frequency (by changing the bus ratios) and voltage, conserving battery life while maintaining a high level of performance. Manual override lets you boost the frequency back to the high frequency when on battery, allowing you to customize performance.

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>IDE Configuration

- OnBoard PCI IDE Controller – [Disabled], [Primary], [Secondary], or [***Both***]

  This item specifies the IDE channels used by the onboard PCI IDE controller.

  - If [Disabled] is selected, the ETX 802 is prevented from using either of the onboard IDE controllers.
  - If [Primary] is selected, the BIOS only detects the Primary IDE channel, including both Primary Master and Primary Slave.
  - If [Secondary] is selected, the BIOS only detects the Secondary IDE channel, including both Secondary Master and Secondary Slave.
  - If [Both] is selected, both Primary and Secondary IDE channels will be detected, including Master and Slave for each channel.

- OnBoard PCI IDE Operate Mode – [***Legacy Mode***] or [Native Mode]

  Native mode is only used with Windows XP.

> Primary IDE Master – [Not Detected] or [**Device Type**]

* If the BIOS does not detect a device on the Primary IDE Master channel, [Not Detected] will be displayed. You can still go to the submenu to set options for an IDE device.
* If the BIOS auto detects a IDE device, the device type will be displayed; for example, [Hard Disk], with the parameters automatically selected, due to the default setting of **Auto** for Type.

  - Type – [Not Installed], [***Auto***], [CD/DVD], or [ARMD]

    This field sets the boot device type used by the BIOS after the Power On Self Test (POST) has completed.

    * If [Not Installed] is selected, the BIOS is prevented from searching for an IDE disk drive on the specified channel.
    * If [Auto] is selected, the BIOS auto any detects IDE disk drives on the specified channel. This is the default setting and should be used if an IDE hard disk drive is attached to the specified IDE channel.
    * If [CD/DVD] is selected, the BIOS only searches for an IDE CD-ROM or IDE DVD device on the Primary IDE channel. The BIOS will not attempt to search for other types of IDE disk devices on the specified channel.
    * If [ARMD] is selected, the BIOS detects an ATAPI Removable Media Device on the specified IDE channel. This includes, but is not limited to ZIP drives and LS-120 drives.

  - LBA/Large Mode – [Disabled] or [***Auto***]

    This field sets the LBA (Logical Block Addressing) on the IDE disk drive. In LBA mode with a setting of [***Auto***], the maximum drive capacity is greater than 137 GB.

  - Block (Multi-Sector Transfer) – [Disabled] or [***Auto***]

    This field sets the block mode multi-sector transfers option and allows the BIOS to auto detect device support for Multi-Sector Transfers on the specified channel. Block mode boosts IDE drive performance by increasing the amount of data transferred. Only 512 bytes of data can be transferred per interrupt if block mode is not used. Block mode allows transfers of up to 64 kB per interrupt.

    * If [Auto] is selected, the BIOS will auto detect the number of sectors per block for transfer from the hard disk drive to the memory. The data transfer to and from the device will occur multiple sectors at a time.

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- PIO Mode – [***Auto***], [0], [1], [2], [3], or [4]

  This field sets the IDE PIO (Programmable I/O) mode and programs the timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases.

  * If [Auto] is selected, the BIOS auto detects the PIO mode.
  * If [0] is selected, the BIOS uses PIO mode 0, with a data transfer rate of 3.3 MBs.
  * If [1] is selected, the BIOS uses PIO mode 1, with a data transfer rate of 5.2 MBs.
  * If [2] is selected, the BIOS uses PIO mode 2, with a data transfer rate of 8.3 MBs.
  * If [3] is selected, the BIOS uses PIO mode 3, with a data transfer rate of 11.1 MBs.
  * If [4] is selected, the BIOS uses PIO mode 4, with a data transfer rate of 16.6 MBs.

- DMA Mode – [***Auto***], [SWDMA0], [SWDMA01], [SWDMA2], [MWDMA0], [MWDMA1], [MWDMA2], [UDMA0], [UDMA1], [UDMA2], [UDMA3], [UDMA4], [UDMA5], or [UDMA6]

  This field allows you to select DMA modes and adjust the respective transfer rate. The list of available DMA modes is dependent on the IDE device and its supported modes, including the transfer speed and cable type (40-pin or 80-pin).

  SWDMAn = Single Word DMA mode n

  MWDMAn = Muliti Word DMA mode n

  UDMAn = Ultra DMA mode n

  * If [Auto] is selected, the BIOS auto detects the DMA Mode. Use this value if the IDE disk drive support cannot be determined.
  * If [SWDMA0] is selected, the BIOS uses Single Word DMA mode 0, with a data transfer rate of 2.1 MBs.
  * If [SWDMA1] is selected, the BIOS uses Single Word DMA mode 1, with a data transfer rate of 4.2 MBs.
  * If [SWDMA2] is selected, the BIOS uses Single Word DMA mode 2, with a data transfer rate of 8.3 MBs.
  * If [MWDMA0] is selected, the BIOS uses Double Word DMA mode 0, with a data transfer rate of 4.2 MBs.
  * If [MWDMA1] is selected, the BIOS uses Double Word DMA mode 1, with a data transfer rate of 13.3 MBs.
  * If [MWDMA2] is selected, the BIOS uses Double Word DMA mode 2, with a data transfer rate of 16.6 MBs.
  * If [UDMA0] is selected, the BIOS uses Ultra DMA mode 0, with a data transfer rate of 16.6 MBs.
  * If [UDMA1] is selected, the BIOS uses Ultra DMA mode 1, with a data transfer rate of 25 MBs.
  * If [UDMA2] is selected, the BIOS uses Ultra DMA mode 2, with a data transfer rate of 33.3 MBs.

NOTE	The following DMA modes, UDMA3, UDMA4, UDMA5, or UDMA6, require an 80-conductor ATA cable and may not appear without it.

  * If [UDMA3] is selected, the BIOS uses Ultra DMA mode 3, with a data transfer rate of 44.4 MBs. To use this mode, an 80-conductor ATA cable is required.

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* If [UDMA4] is selected, the BIOS uses Ultra DMA mode 4, with a data transfer rate of 66.6 MBs. To use this mode, an 80-conductor ATA cable is required.
* If [UDMA5] is selected, the BIOS uses Ultra DMA mode 5, with a data transfer rate of 99.9 MBs. To use this mode, an 80-conductor ATA cable is required.
* If [UDMA6] is selected, the BIOS uses Ultra DMA mode 6, with a data transfer rate of 133.2 MBs. To use this mode, an 80-conductor ATA cable is required.

- S.M.A.R.T.– [***Auto***], [Disabled], or [Enabled]

  The Self-Monitoring Analysis and Reporting Technology (SMART) feature can help predict impending drive failures.

  * If [Auto] is selected, the BIOS auto detects hard disk drive support. Use this setting if the IDE disk drive support cannot be determined.
  * If [Disabled] is selected, the BIOS is prevented from using SMART feature.
  * If [Enabled] is selected, the BIOS uses the SMART feature on the hard disk drives.

- 32Bit Data Transfer – [*Disabled*] or [**Enabled**]

  This field sets the 32-bit data transfer rate.

  If [Enabled] is selected, the BIOS uses 32-bit data transfers on the supported hard disk drive.

> Primary IDE Slave – [**Not Detected**] or [Device Type]

The descriptions used for the Primary IDE Master are the same for the Primary IDE Slave except where noted.

- Type – [Not Installed], [***Auto***], [CD/DVD], or [ARMD]
  * If [Not Installed] appears due to Not Detected, the balance of the options for Primary IDE Slave do not appear on screen.
- LBA/Large Mode – [Disabled] or [***Auto***]
- Block (Multi-Sector Transfer) – [Disabled] or [***Auto***]
- PIO Mode – [***Auto***], [0], [1], [2], [3], or [4]
- DMA Mode – [***Auto***], [SWDMA0], [SWDMA01], [SWDMA2], [MWDMA0], [MWDMA1], [MWDMA2], [UDMA0], [UDMA1], [UDMA2], [UDMA3], [UDMA4], [UDMA5], or [UDMA6]
- S.M.A.R.T.– [***Auto***], [Disabled], or [Enabled]
- 32Bit Data Transfer – [*Disabled*] or [**Enabled**]

> Secondary IDE Master – [**Not Detected**] or [Device Type]

The descriptions used for the Primary IDE Master are the same for the Secondary IDE Master except where noted.

- Type – [Not Installed], [***Auto***], [CD/DVD], or [ARMD]
  * If [Not Installed] appears due to Not Detected, the balance of the options for Secondary IDE Master do not appear on screen.
- LBA/Large Mode – [Disabled] or [***Auto***]
- Block (Multi-Sector Transfer) – [Disabled] or [***Auto***]
- PIO Mode – [***Auto***], [0], [1], [2], [3], or [4]
- DMA Mode – [***Auto***], [SWDMA0], [SWDMA01], [SWDMA2], [MWDMA0], [MWDMA1], [MWDMA2], [UDMA0], [UDMA1], [UDMA2], [UDMA3], [UDMA4], [UDMA5], or [UDMA6]
- S.M.A.R.T.– [***Auto***], [Disabled], or [Enabled]

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- 32Bit Data Transfer – [*Disabled*] or [**Enabled**]

> Secondary IDE Slave – [**Not Detected**] or [Device Type]

The descriptions used for the Primary IDE Master are the same for the Secondary IDE Slave except where noted.

- Type – [Not Installed], [***Auto***], [CD/DVD], or [ARMD]
  - ∗ If [Not Installed] appears due to Not Detected, the balance of the options for Secondary IDE Slave do not appear on screen.
- LBA/Large Mode – [Disabled] or [***Auto***]
- Block (Multi-Sector Transfer) – [Disabled] or [***Auto***]
- PIO Mode – [***Auto***], [0], [1], [2], [3], or [4]
- DMA Mode – [***Auto***], [SWDMA0], [SWDMA01], [SWDMA2], [MWDMA0], [MWDMA1], [MWDMA2], [UDMA0], [UDMA1], [UDMA2], [UDMA3], [UDMA4], [UDMA5], or [UDMA6]
- S.M.A.R.T. for hard disk drives – [***Auto***], [Disabled], or [Enabled]
- 32Bit Data Transfer – [*Disabled*] or [**Enabled**]

- Hard disk drive Write Protect – [***Disabled***] or [Enabled]

  This field protects the hard disk drive from being overwritten.

  - ∗ If [Disabled] is selected, the HDD operates normally, allowing Read, Write, and Erase functions to be performed on the IDE hard disk drive.
  - ∗ If [Enabled] is selected, the BIOS is prevents the IDE HDD from being erased.

- IDE Detect Time Out (Seconds) – [0], [5], [10], [15], [20], [25], [30], or [***35***]

  The field determines how long the BIOS searches for the available IDE devices on the specified channels. Some IDE HDDs take the BIOS longer to locate than others, but this field allows you fine-tune the settings to allow for faster boot times.

  - ∗ If [0] is selected, the BIOS does not search for an IDE device. This is the best setting to use if the onboard IDE controllers are set to a specific IDE HDD in the BIOS.
  - ∗ If [5] is selected, the BIOS stops searching for an IDE device after 5 seconds. A large majority of ultra ATA HDDs can be detected with within 5 seconds.
  - ∗ If [10] is selected, the BIOS stops searching for an IDE device after 10 seconds.
  - ∗ If [15] is selected, the BIOS stops searching for an IDE device after 15 seconds.
  - ∗ If [20] is selected, the BIOS stops searching for an IDE device after 20 seconds.
  - ∗ If [25] is selected, the BIOS stops searching for an IDE device after 25 seconds.
  - ∗ If [30] is selected, the BIOS stops searching for an IDE device after 30 seconds.
  - ∗ If [35] is selected, the BIOS stops searching for an IDE device after 35 seconds. This is the default setting and is the recommended setting when all IDE connectors are set to Auto.

- ATA (PI) 80 pin Cable Detection – [***Host & Device***], [Host], or [Device]

  This field selects the method used to detect the ATA (PI) 80-pin cable. The default setting for EXT 802 BIOS is 40-pins.

  - ∗ If [Host & Device] is selected, the BIOS uses both the onboard IDE controller and the IDE hard disk drive (HDD) to detect the type of IDE cable used.
  - ∗ If [Host] is selected, the BIOS uses only the onboard IDE controller to detect the type of IDE cable used.

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* If [Device] is selected, the BIOS uses only the IDE hard disk drive (HDD) to detect the type of IDE cable used.

NOTE	An 80-conductor ATA cable is required when operating with Ultra ATA/66, Ultra ATA/100 and Ultra ATA/133 IDE hard disk drives. The standard 40-conductor ATA cable cannot handle the higher speeds. Due to the plug compatibility of the 80-conductor ATA cable to the standard 40-conductor ATA cable, the BIOS must have a feature to set this or determine if the 80-conductor ATA cable is present. The BIOS detects a break in one of the lines on the 80-conductor ATA cable that is normally an unbroken connection in the standard 40-conductor ATA cable. If a faster speed is set in the BIOS than the connected cable can support, the BIOS instructs the IDE HDD to run at the correct speed for the cable type detected.

>Floppy Configuration

- Drive A – [Disabled], [360 kB, 5 1/4 "], [1.2 MB, 1/4"], [720 kB, 3 1/2"], [***1.44 MB, 3 1/2"],*** or [2.88 MB, 3.5"]
- Drive B – [***Disabled***], [360 kB, 5 1/4"], [1.2 MB, 1/4"], [720 kB, 3 1/2"], [1.44 MB, 3 1/2"], or [2.88 MB, 3.5"]

>Super I/O Configuration

- Onboard Floppy Controller – [Disabled] or [***Enabled***]
  * If this feature is [Enabled], the onboard floppy controller is selected over the Parallel Port and the entry, 1st Floppy Drive, appears in the boot order under Boot Device Priority. You must select a Floppy A, typically [1.44 MB, 3 1/2"] to use this feature. The Parallel Port can not be enabled since these two devices share the same pins on the baseboard interface connector.
  * If this feature is [Disabled], the Parallel Port can be Enabled by selecting one of the Parallel port address.
- Serial Port 1 Address – [Disabled], [***3F8/IRQ4***], [2F8/IRQ3], [3E8/IRQ4], or [2E8/IRQ3]
- Serial Port 2 Address – [Disabled], [3F8/IRQ4], [***2F8/IRQ3***], [3E8/IRQ4], or [2E8/IRQ3]
  - Serial Port 2 Mode – [***Normal***], [IrDA], or [ASK IR]
    * If [IrDA] or [ASK IR] are selected, the following items appear on screen.
      ◊ IR Duplex mode – [***Half Duplex***] or [Full Duplex]
      ◊ IR I/O Pin select – [***SINB/SOUTB***] or [IRRX/IRTX]
      ◊ COMB Receiver Polarity – [***High***] or [Low]
      ◊ COMB Xmitter Polarity – [***High***] or [Low]
- Parallel Port Address – [***Disabled***], [378], [278], or [3BC]

  If [378], [278], or [3BC] are selected, the following items appear on screen.
  - Parallel Port Mode– [***Normal***], [Bi-Directional], [EPP], or [ECP]
    * If [Normal] is selected, the standard parallel port mode is used. This is the default setting.
    * If [Bi-Directional] is selected, the data is sent to and received from the parallel port.
    * If [EPP] is selected, the following options are listed. The parallel port can be used with devices adhering to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bi-directional data transfer driven by the host device.

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◊ EPP version [1.9] or [1.7]

* If [ECP] is selected, the following options are listed. The parallel port can be used with devices adhering to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Megabits per second. ECP also provides symmetric bi-directional communication.

◊ ECP Mode DMA Channel [DMA3], [DMA0], or [DMA1]

♦ Parallel Port IRQ – [IRQ5] or [***IRQ 7***]

>ACPI Configuration

- General ACPI Configuration
  - ♦ Suspend Mode – [Auto], [S1 (POS)], or [***S3 (STR)***]

    This field determines which sleep state (S1 or S3) is used for suspended mode.

    * If [Auto] or [S3 (STR)] is selected, the following item appears on screen. Enabling S3 will also enable the S3 Mode LED on the ETX 802.

    - Repost Video on S3 Resume – [***No***] or [Yes]

      * If [Yes] is selected, the video BIOS is initialized coming out of the S3 state. Some video controllers require this option to be enabled.

      * If [No] is selected, the video BIOS will not be initialized coming out of the S3 state.

- Advanced ACPI Configuration
  - ♦ ACPI 2.0 Features – [No] or [***Yes***]

    If [Yes] is selected, the BIOS will support the ACPI 2.0 specifications.

  - ♦ Headless Mode – [***Disabled***] or [Enabled]

    If [Enabled] is selected, the ACPI FACP (Fixed System Description Table) table is updated to indicate headless operation mode through ACPI. Today, headless operation implies no keyboard or mouse.

- Chipset ACPI Configuration
  - ♦ APIC ACPI SCI IRQ – [***Disabled***] or [Enabled]
  - ♦ USB Device Wakeup from S3 – [***Disabled***] or [Enabled]

>MPS Configuration

- MPS Configuration Version – [1.1] or [***1.4***]

>Smbios Configuration

- Smbios Smi Support – [Disabled] or [***Enabled***]

>Remote Access Configuration

- Remote Access – [***Hotcable***] or [Enabled]

  This field enables the remote access (Serial Console or Console Redirection) features.

  - ♦ Serial Port Number – [COM1] or [***COM2***]

    Base Address, IRQ [2F8h, 3]

  - ♦ Serial Port Mode – [***115200, 8, n, 1***], [57600, 8, n, 1], [38400, 8, n, 1], [19200, 8, n, 1], or [09600, 8, n, 1]

    If [57600, 8, n, 1] is selected, the remote Serial Terminal should be set for 57.6 kHz baud rate with 8 start bits, no parity, and 1 stop bit.

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- Flow Control – [***None***], [Hardware], or [Software]
  - If [Hardware] is selected, flow control is handled by hardware.
  - If [Software] is selected, flow control is handled by software.
- Redirection After BIOS Post – [Disabled], [Boot Loader], or [***Always***]
- Terminal Type – [***ANSI***], [VT100], or [VT-UTF8]
  - If [VT-UTF8] is selected, the following item disappear from the screen.
    - VT-UTF8 Combo Key Support – [Disabled] or [***Enabled***]
- Sredir Memory Display Delay – [***No Delay***], [Delay 1 sec], [Delay 2 sec] or [Delay 4 sec]

>USB Configuration

Depending on the USB devices detected, examples similar to those listed below may be displayed.

Module Version - x.xx.xx-xx.x **Or** **Module Version - x.xx.xx-xx.x**

USB Devices Enabled:
2 drives

USB Devices Enabled:
None:

- USB Function – [Disabled], [2 USB ports], or [***4 USB ports***]
  - If [Disabled] is selected, remaining options for USB, except USB 2.0 Controller, will disappear from the screen.
- Legacy USB Support – [Disabled], [***Enabled***], or [Auto]

  This field supports the USB mouse and USB keyboard when no USB drivers are loaded for the operating system (OS).
  - If [Disabled] is selected, remaining options for USB, except USB 2.0 Controller, will disappear from the screen.
  - If [Enabled] is not enabled, the attached USB mouse and USB keyboard will not be available until a USB compatible OS is fully booted with all the USB drivers loaded.
  - If [Auto] is selected, Legacy USB Support is disabled if no USB devices are connected.

NOTE	If this field is not enabled with [Enabled] or [Auto] the USB mouse and USB keyboard will not be recognized by the BIOS until the OS is fully booted and the USB drivers are loaded.

  - If [Enabled] is selected, USB devices may be used during boot time and while using DOS.
  - If [Auto] is selected, USB devices like, a USB keyboard or USB mouse will be automatically detected and if found, will be initialized and utilized during Boot time.
- USB 2.0 Controller – [*Disabled*] or [**Enabled**]
  - If [Disabled] is selected, the following item disappears from the screen.
    - USB 2.0 Controller Mode – [*Full Speed*] or [**Hi Speed**]

      This field configures the USB 2.0 controller for [Full Speed = 12 Mbps] or [Hi Speed = 480 Mbps]
- BIOS EHCI Hand-Off – [Disabled] or [***Enabled***]

  This field is used as work around for operating systems (OSs) that do not have EHCI hand-off support. The EHCI ownership change should be claimed by the EHCI driver.

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>**USB MASS Storage Device Configuration**

- USB Mass Storage Reset Delay – [10 sec], [**20 sec**], [30 sec], or [40 sec]

  This field determines the number of seconds POST waits for the storage device after the start unit command is sent.

  - Device #1 – [Mfg + model or device type]
  - Emulation Type – [**Auto**], [Floppy], [Forced FDD], [Hard Disk], or [CDROM]

    This field emulates USB device types.

    * If this field is set to [Auto] it will emulate USB devices less than 530 MB as Floppy and devices larger than 530 MB as Hard Drives.
    * If the [Forced FDD] options is selected, a HDD formatted drive can be forced to boot as FDD (except ZIP drives).

  The remaining fields only appear if the BIOS detects additional USB mass storage devices up to three more USB devices.

  - Device #2 – [Mfg + model or USB device type]
  - Emulation Type – [**Auto**], [Floppy], [Forced FDD], [Hard Disk], or [CDROM]
  - Device #3 – [Mfg + model or USB device type]
  - Emulation Type – [**Auto**], [Floppy], [Forced FDD], [Hard Disk], or [CDROM]
  - Device #4 – [Mfg + model or USB device type]
  - Emulation Type – [**Auto**], [Floppy], [Forced FDD], [Hard Disk], or [CDROM]

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PCIPnP (Plug & Play) Menu Screen

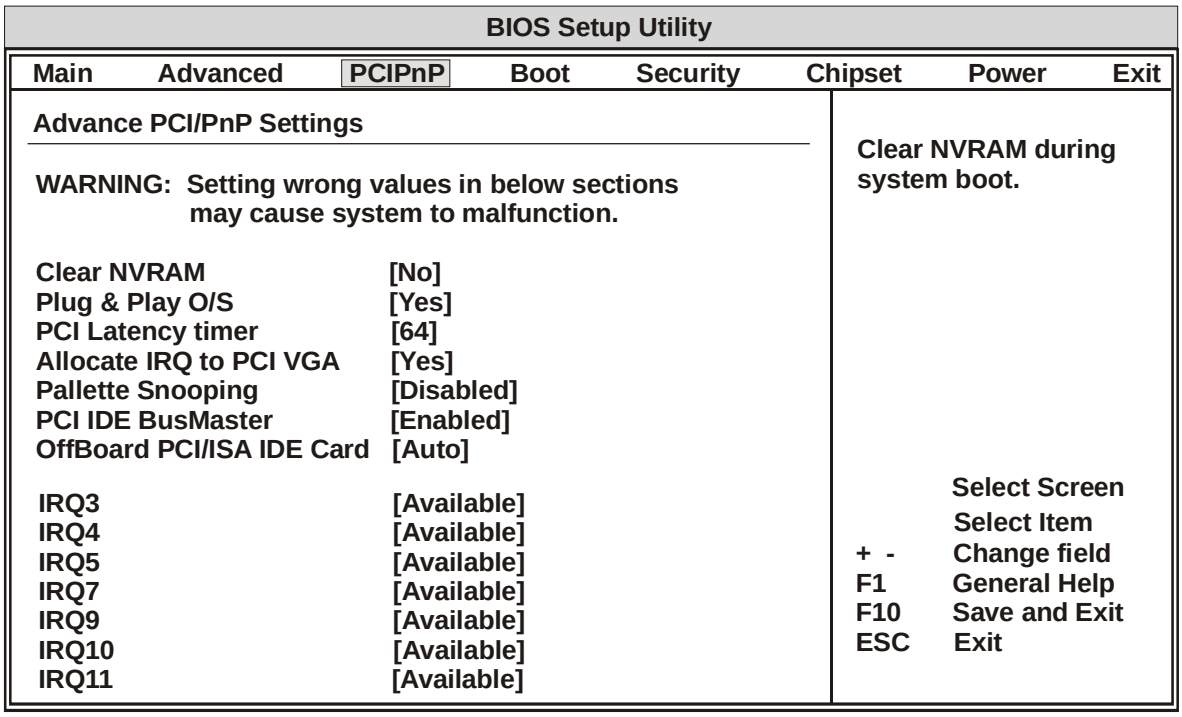


Figure 4-3. PCIPnP Menu Screen

Advance PCI/PnP Settings

- Clear NVRAM – [***No***] or [Yes]

  This field is used to clear NVRAM during system boot.

- Plug & Play O/S – [No] or [***Yes***]

  * If [No] is selected, the BIOS is allowed to configure all the devices in the system.

  * If [Yes] is selected, the Operating System (OS) is allowed to configure Plug and Play (PnP) devices not required for boot if your ETX 802 is using a Plug and Play OS. The OS is allowed to change the interrupt, I/O, and DMA settings for the devices in the system.

- PCI Latency timer – [32], [***64***], [96], [128], [160], [192], [224], or [248]

  This feature sets the latency of all PCI devices on the PCI bus. The various settings allow the PCI Latency timer to be adjusted to the number of clock cycles specified. The default setting [64] adjust the PCI Latency timer to 64 PCI clock cycles.

- Allocate IRQ to PCI VGA – [***Yes***] or [No]

  This field allows or restricts the system from giving the VGA adapter card an interrupt address.

  * If [Yes] is selected, the BIOS is allowed to allocate an IRQ to any VGA adapter card that uses the PCI local bus.

- Palette Snooping – [***Disabled***] or [Enabled]

  * If [Disabled] is selected, the BIOS prevents an installed VGA card from using Palette Snooping, even if the VGA card request IRQs. This should not be changed unless the VGA card manufacturer requires this feature to be Enabled.

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- If [Enabled] is selected, PCI devices are informed an ISA graphics card is installed in the system so the card will function correctly.

- PCI IDE BusMaster – [Disabled] or [***Enabled***]
  - If [Enabled] is selected, the BIOS allows the IDE controller on the PCI local bus to have bus mastering capabilities, including reading/writing to IDE drives.
- OffBoard PCI/ISA IDE card – [***Auto***], [PCI Slot 1], [PCI Slot 2], [PCI Slot 3], or [PCI Slot 4]
  - If [Auto] is selected, which works with most PCI IDE cards, it allows BIOS to automatically select the location of an OffBoard PCI IDE adapter card. Don't select the other PCI slot positions, unless the IDE adapter card is installed in the respective card slot position.
  - If [PCI Slot 1] to [PCI Slot 4] are selected the following options appear:
    - OffBoard PCI IDE Primary IRQ – [Disabled], [INTA], [INTB], [INTC], [INTD], or [Hardwired]
      - If [Disabled] is selected, the PCI Slot # does not use or need an IRQ.
      - If [INT#] is selected, the PCI Slot # needs an IRQ assigned to the device installed in the PCI slot.
    - OffBoard PCI IDE Secondary IRQ – [Disabled], [INTA], [INTB], [INTC], [INTD], or [Hardwired]
      - If [Disabled] is selected, the PCI Slot # does not use or need an IRQ.
      - If [INT#] is selected, the PCI Slot # needs an IRQ assigned to the device installed in the PCI slot.
- IRQ3 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this IRQ to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this IRQ for a legacy ISA device.
- IRQ4 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this IRQ to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this IRQ for a legacy ISA device.
- IRQ5 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this IRQ to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this IRQ for a legacy ISA device.
- IRQ7 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this IRQ to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this IRQ for a legacy ISA device.
- IRQ9 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this IRQ to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this IRQ for a legacy ISA device.
- IRQ10 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this IRQ to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this IRQ for a legacy ISA device.
- IRQ11 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this IRQ to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this IRQ for a legacy ISA device.

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- IRQ14 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this IRQ to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this IRQ for a legacy ISA device.
- IRQ15 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this IRQ to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this IRQ for a legacy ISA device.
- DMA Channel 0 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this DMA Channel to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this DMA Channel for a legacy ISA device.
- DMA Channel 1 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this DMA Channel to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this DMA Channel for a legacy ISA device.
- DMA Channel 3 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this DMA Channel to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this DMA Channel for a legacy ISA device.
- DMA Channel 5 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this DMA Channel to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this DMA Channel for a legacy ISA device.
- DMA Channel 6 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this DMA Channel to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this DMA Channel for a legacy ISA device.
- DMA Channel 7 – [***Available***] or [Reserved]
  - If [Available] is selected, the BIOS can assign this DMA Channel to a PCI/PnP device.
  - If [Reserved] is selected, the BIOS holds this DMA Channel for a legacy ISA device.
- Reserved Memory – [***Disabled***], [16k], [32k], or [64k]

  This field reserves the memory block size for Legacy ISA devices.
  - If [Disabled] is selected, the BIOS is prevented from reserving memory for ISA devices.
  - If [64k] is selected, the BIOS reserves 64k of system memory for ISA devices at the Reserved Memory Address of [C8000].
- PCI Slot 1 – IRQ Preference– [***Auto***]. [3], [4], [5], [7], [9], [10], [11], [12], [14], or [15]

  These fields select the PCI slot IRQ preference. Manually selecting IRQs does not guarantee the PCI slot devices will be configured with the IRQ choices, because PnP ISA cards (if present) are assigned the available resources before PCI devices.
- PCI Slot 2 – IRQ Preference– [***Auto***]. [3], [4], [5], [7], [9], [10], [11], [12], [14], or [15]
- PCI Slot 3 – IRQ Preference– [***Auto***]. [3], [4], [5], [7], [9], [10], [11], [12], [14], or [15]
- PCI Slot 4 – IRQ Preference– [***Auto***]. [3], [4], [5], [7], [9], [10], [11], [12], [14], or [15]

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Boot Menu Screen

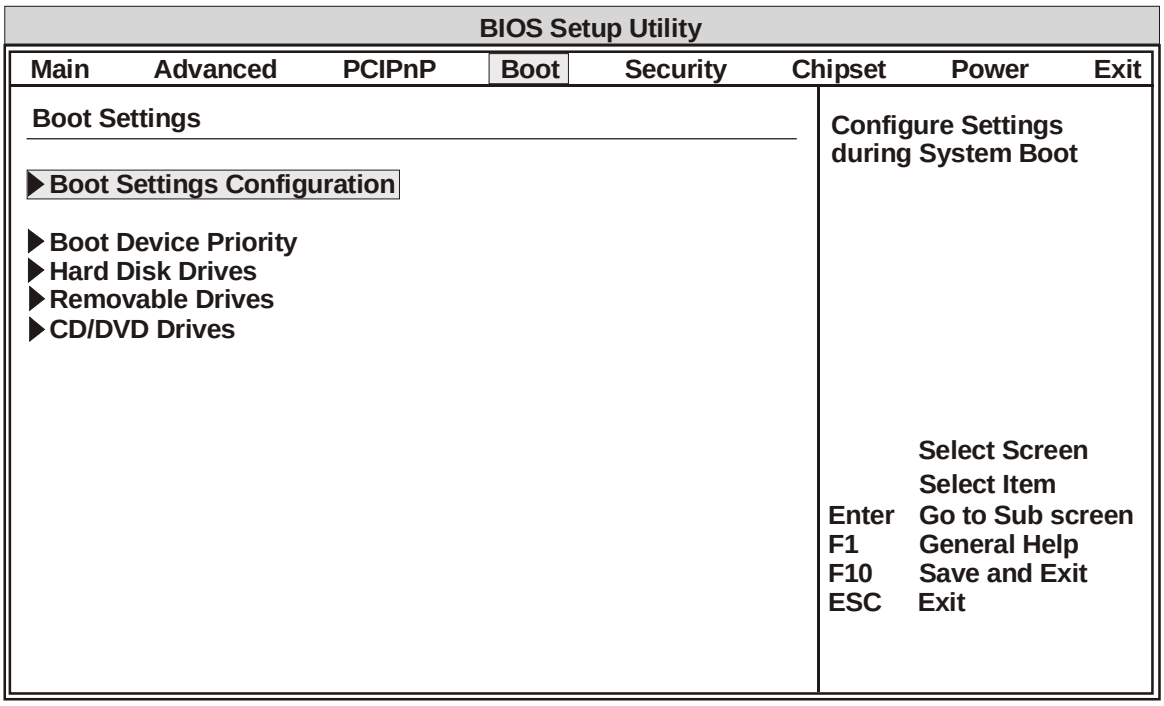


Figure 4-4. Boot Menu Screen

Boot Settings

>Boot Settings Configuration

- Quick Boot – [Disabled] or [***Enabled***]
  - If [Disabled] is selected, the BIOS is allowed to perform all POST test, but this slows the boot process.
  - If [Enabled] is selected, the BIOS is allowed to skip certain POST tests to boot faster.
- Quiet Boot – [***Disabled***] or [Enabled]
  - If [Disabled] is selected, the BIOS is allowed to display the POST messages on screen.
  - If [Enabled] is selected, the BIOS displays the customized splash screen (OEM boot logo). The splash screen image (or boot logo) will appear on the display instead of the POST messages.

    For more information about how to customized a splash screen image(OEM boot logo), refer to the Splash Screen files in the *CD-ROM/Software/Misc/Splash* directory on the ETX 802 Doc & SW CD-ROM for instructions when creating your own logo to display.
- AddOn ROM Display Mode – [***Force BIOS***] or [Keep Current]
  - If [Force BIOS] is selected, any third party BIOS or add-on ROM messages will be displayed on screen during the boot process.
  - If [Keep Current] is selected, no third party BIOS messages will be displayed on screen during the boot process.

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- Bootup Num-Lock – [***Off***] or [On]

  This field enables or disables the Num-Lock (Number Lock) keypad, including the 10-key numeric keys, to be turned on or off automatically when the system boots up. The field selection will remain unchanged until the Num-Lock key on the keyboard is pressed to change the Num-Lock state.

- PS/2 Mouse Support – [Disabled], [Enabled], or [***Auto***]

  * If [Disabled] is selected, the PS/2 Mouse will not have access to system resources and will not be active after boot up.
  * If [Enabled] is selected, the PS/2 Mouse can be used and will have access to system resources after boot up.
  * If [Auto] is selected, the BIOS will detect the PS/2 Mouse automatically, if present, during the boot process. The PS/2 Mouse will have access to system resources and be active after boot up.

- Wait for 'F1' If Error – [***Disabled***] or [Enabled]

  * If [Disabled] is selected, this does not allow for user intervention if an error occurs. Use this setting only when a known BIOS error will appear.
  * If [Enabled] is selected, allows the BIOS to display an Error message indicating when an error has occurred during POST (power on self test) and wait for you to respond by hitting the <F1> key. Pressing <F1> will enter Setup and the BIOS setting can be adjusted to fix the problem.

- Hit 'Del' Message Display – [Disabled] or [***Enabled***]

  * If [Disabled] is selected, the BIOS will not place the “Hit Del to enter Setup" message on screen during the boot process. If Quiet Boot is enabled, the Hit 'Del" message will not display.
  * If [Enabled] is selected, the BIOS will place the “Hit Del to enter Setup" message on screen during the boot process, to indicate when you may press “Del” to enter the BIOS Setup menus.

- Interrupt 19 Capture – [***Disabled***] or [Enabled]

  * If [Disabled] is selected, the BIOS prevents option ROMs from trapping interrupt 19.
  * If [Enabled] is selected, the BIOS allows option ROMs to trap interrupt 19.

- Watchdog Timeout in Seconds – [***Disabled***] or [1-255]

  * If this field [1-255] is enabled by selecting a time interval (select a whole number between 255 seconds and 1 second), it will direct the watchdog timer to reset the system if it fails to boot the OS properly. Refer to the watchdog timer section in Chapter 3 for more information.

>Boot Device Priority

Use these fields to set the boot device priority (boot order), which determines the boot sequence used by the BIOS to check for a boot device. You set the boot order by selecting from the list of the available boot devices, as well as, changing the order of the device types. Refer to the following examples, including the device types.

- 1st Boot Device – [Disabled], [***1st Floppy Drive***], [Hard Drive], [CD/DVD], or [Network: IBA FE Slot 01xx]
  * Example, [1st Floppy Drive]
- 2nd Boot Device – [Disabled], [1st Floppy Drive], [Hard Drive], [***CD/DVD***], or [Network: IBA FE Slot 01xx]
  * Example, [CD/DVD: Mfg, model]
- 3rd Boot Device – [Disabled], [1st Floppy Drive], [***Hard Drive***], [CD/DVD], or [Network: IBA FE Slot 01xx]
  * Example, [HDD: Mfg, model]

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- 4th Boot Device – [Disabled], [1st Floppy Drive], [Hard Drive], [CD/DVD], or [***Network:IBA FE Slot 01xx***]

  * Example, [Network: IBA FE Slo]

  Changing Boot Order Example:

  1. Scroll to the 1st Boot Device [1st Floppy Drive] and press the <**Enter**> key.

     The Options list appears with all of the 1st Drive selections from the device types shown in the popup menu.

     If you want to change from a standard floppy drive to a USB floppy drive, go to the Removable Drives list, where you can select the device that appears in the list instead of the 1st Floppy Drive.

  2. Scroll down the popup menu list and select another device, such as the CD-ROM in the 3rd Boot Device position and press the <**Enter**> key.

     The CD-ROM changes place with the 1st Floppy Drive, while at the same time putting the 1st Floppy Drive in the 3rd Boot Device position (former location of the CD-ROM).

  3. If you select [Disabled], the 1st Floppy Drive moves to the 4th position (last), and changes to *Disabled*, while all other devices move up in the Boot order.

The following device type fields are dependent on the type and number of devices connected to the system. For example, you may not see the CD/DVD type field if there is no CD-ROM or DVD connected to the system.

>**Hard Disk Drives**

This option specifies the boot sequence from the available Hard Disk Drives (HDD). This option and the number of HDDs only appears on screen if the BIOS detects Hard Disk Drives (HDD) attached to the system.

- 1st Drive – [HDD: Mfg + Model], [HDD: Mfg + Model], or [Disabled]

  The 1st Drive in this list is the only device to appear in the Boot Device Priority list. The remaining fields are dependent on the number of HDD devices detected by the BIOS, including the compact flash card. Use the example method described earlier when changing the order of these devices.

- 2nd Drive – [HDD: Mfg + Model], [HDD: Mfg + Model], [HDD: Mfg + Model], or [Disabled]

- 3rd Drive – [HDD: Mfg + Model], [HDD: Mfg + Model], [HDD: Mfg + Model], or [Disabled]

>**Removable Drives**

This option specifies the boot sequence from the available Removable Drives. The number of devices only appear on screen if the BIOS detects more than one Removable Drive attached to the system.

- 1st Drive – [1st Floppy Drive], [USB: Mfg + model or device type], [USB: Mfg + model or device type], or [Disabled]

  The 1st Drive in this list is the only device to appear in the Boot Device Priority list. The remaining fields and options are dependent on the number of removable devices detected by the BIOS. Use the example method described earlier when changing the order of these devices.

- 2nd Drive – [1st Floppy Drive], [USB: Mfg + model or device type], [USB: Mfg + model or device type], [USB: Mfg + model or device type], or [Disabled]

- 3rd Drive – [1st Floppy Drive], [USB: Mfg + model or device type], [USB: Mfg + model or device type], [USB: Mfg + model or device type], or [Disabled]

- 4th Drive – [1st Floppy Drive], [USB: Mfg + model or device type], [USB: Mfg + model or device type], [USB: Mfg + model or device type], or [Disabled]

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>**CD/DVD Drives**

This option specifies the boot sequence from the available CD/DVDs. This option only appears on screen if the BIOS detects any CD/DVDs attached to the system. Use the example method described earlier when changing the order of these devices.

- 1st Drive – [CD/DVD: Mfg + Model] or [Disabled]

  The 1st Drive in this list is the only device to appear in the Boot Device Priority list. The remaining fields and options are dependent on the number of CD/DVD devices detected by the BIOS.

- 2nd Drive – [CD/DVD: Mfg + Model], [CD/DVD: Mfg + Model], or [Disabled]

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Security Menu Screen

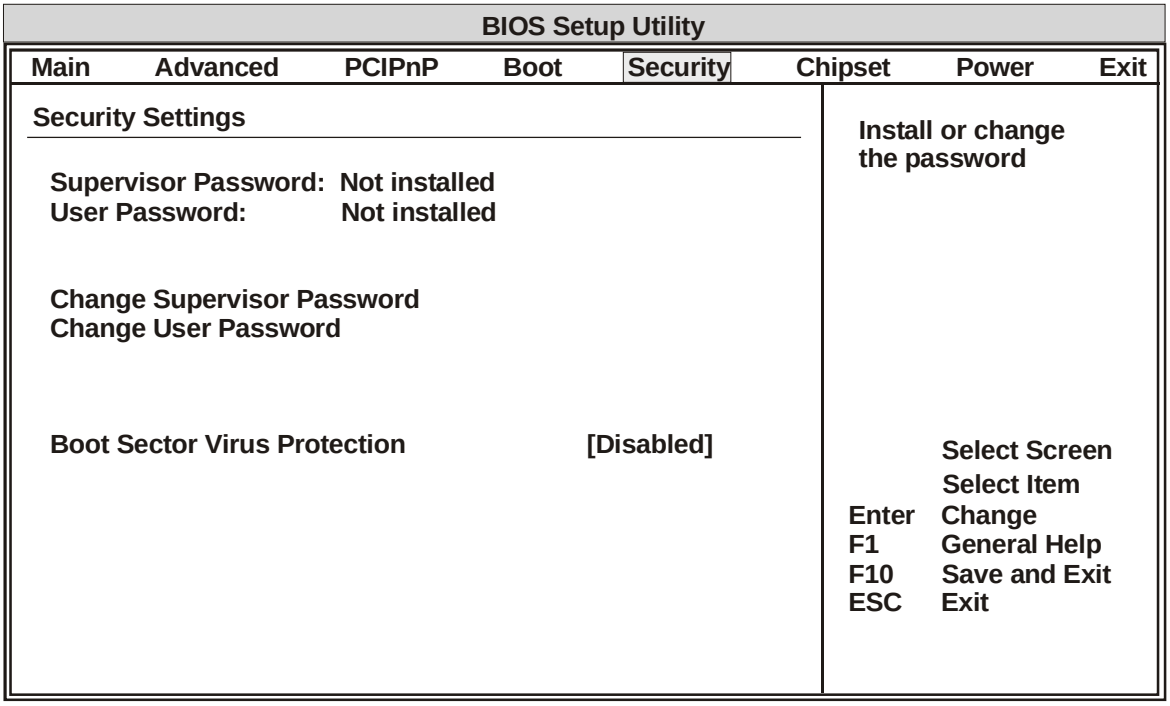


Figure 4-5. Security Menu Screen

Security Settings

- Supervisor Password – [***Not Installed***] or [Installed]

  Indicates if a supervisor password has been set.

  * If the password has been installed, Installed appears on screen.
  * If no the password has be selected, then Not Installed appears on screen.

- User Password – [***Not Installed***] or [Installed]

  Indicates if a user password has been set. If the password has been installed, Installed displays. If not, Not Installed displays.

- Change Supervisor Password

  a. Select **Change Supervisor Password** from the Security Setup menu.

  b. Press <*Enter*> to access the pop-up menu, *Enter New Password:*

  c. Type the password and press <*Enter*> again.

  The screen will not display the password as you type.

  d. Retype the password when prompted by the pop-up menu and press <*Enter*> again.

  If the password is not confirmed when you retype it, an error message will appear. The password is stored in NVRAM and you have successfully entered the password.

To clear Supervisor password: .

a. Press <*Enter*> to access the pop-up menu, *Enter New Password:*

b. Do not enter a password and press the <*Enter*> key, following the prompts.

c. Repeat this process until the old password is gone, which is indicated by *Not Installed*.

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If the Supervisor Password field is “Installed”, the following item appears on the screen.

- User Access Level – [No Access] or [View Only], [Limited], or [Full Access]

- Change User Password

  a. Select **Change User Password** from the Security Setup menu.

  b. Press <*Enter*> to access the pop-up menu, *Enter New Password:*

  c. Type the password and press <*Enter*> again.

     The screen will not display the password as you type.

  d. Retype the password when prompted by the pop-up menu and press <*Enter*> again.

  If the password is not confirmed when you retype it, an error message will appear. The password is stored in NVRAM and you have successfully entered the password.

  If the Change User Password field is “Installed”, a Pop-Up screen, titled “Clear User Password?” appears with these selections.

  - Clear User Password – [OK] or [Cancel]
  - Password Check – [Setup] or [Always]

- Boot Sector Virus Protection – [***Disabled***] or [Enabled]

  This field displays a warning when any program (or virus) issues a Disk Format command or attempts to write to the boot sector of the hard disk drive.

  * If [Disabled] is selected, there is no Boot Sector Virus Protection warning displayed for the hard disk drive.
  * If [Enabled] is selected, a warning is displayed when any program (or virus) issues a Disk Format command or attempts to write to the boot sector of the hard disk drive. A warning display also appears if there is any attempt to format any cylinder, head, or sector of any hard disk drive.

    The following display appears when a write is attempted to the boot sector.

    ```
    Boot Sector Write!
    Possible VIRUS: Continue (Y/N)?
    ```

    You may have to type N several times to prevent the boot sector write.

    The following appears after any attempt to format any cylinder, head, or sector of any hard disk drive via the BIOS INT 13 Hard disk drive.

    ```
    Service:
    Format!!!
    Possible VIRUS: Continue (Y/N)?
    ```


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Chipset Menu Screen

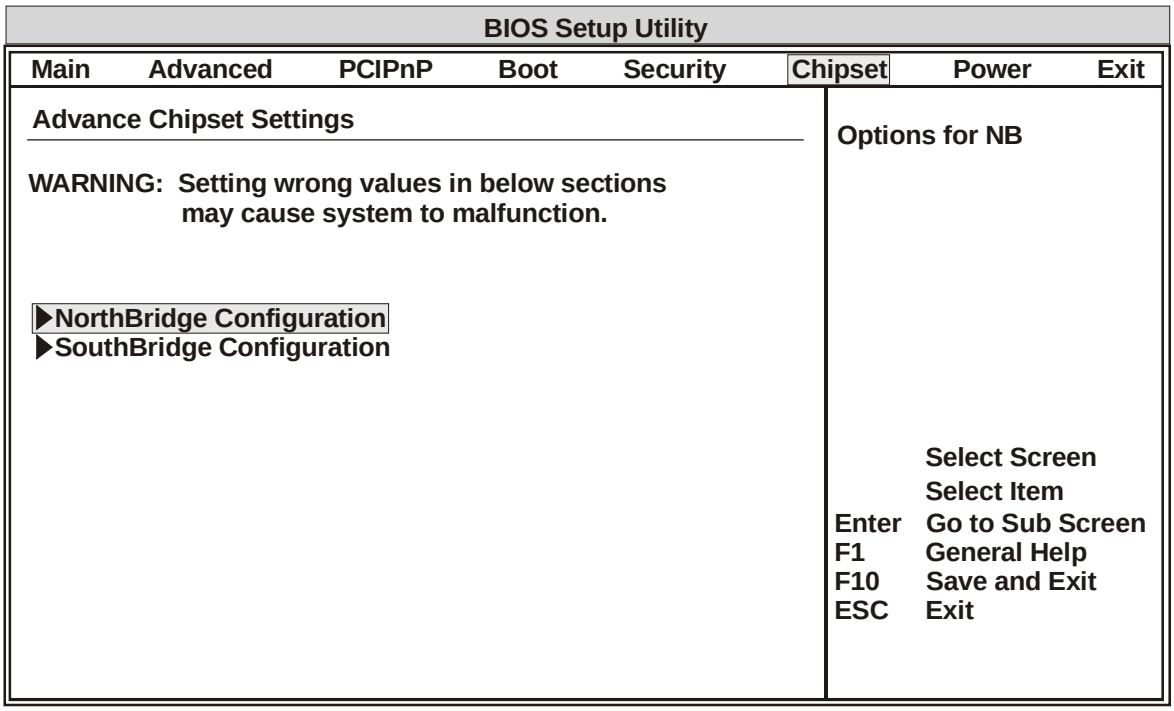


Figure 4-6. Chipset Menu Screen

Advance Chipset Settings

>Northbridge Chipset Configuration

- DRAM Frequency – [*200 MHz*], [266 *MHz*], [333 *MHz*], or [**Auto**]
- Configure DRAM Timing by SPD – [Disabled] or [***Enabled***]

  If [Enabled] is selected, the following items disappear from the screen.

  - DRAM CAS# Latency – *[**2.5***] or [2]
  - DRAM RAS# Precharge – [2 Clocks] or [***3 Clocks***]
  - DRAM RAS# to CAS# Delay – [2 Clocks] or [***3 Clocks***]
  - DRAM Precharge Delay – [5 Clocks], [6 Clocks], or [***7 Clocks***]
- DRAM Burst Length – [*4*] or [**8**]
- Memory Hole – [***Disabled***] or [15MB-16MB]
- Init. Graphics Adapter Priority – [Internal VGA] or [***PCI/Int-VGA***]
- Internal Graphics Mode Select – [Disabled], [Enabled, 1 MB], [Enabled, 4 MB], [***Enabled, 8 MB***], [Enabled, 16 MB], or [Enabled, 32 MB]
- Graphics Aperture Size – [***64 MB***], [128 MB], or [256 MB]

  Video Function Configuration

  - DVMT Mode Select – [Fixed Mode], [DVMT Mode], or [***Combo Mode***]
  - Boot Display Device – [***Auto***], [CRT], [LFP], or [CRT + LFP]

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- Flat Panel Type [***None***]

  Refer to Table 4-3 for the list of supported resolutions and flat panel types. Some LCD panels may require video BIOS modifications. It you think this is the case, or would like help in setting up your LCD panel, contact Ampro for assistance with the LCD panel adaptation.

- Local Flat Panel Scaling – [***Auto***], [Forced Scaling], or [Disabled]

Table 4-3. LCD Panel Type List

#	LCD Resolution	BITs
0	***None***	
1	640 x 480 LVDS	
2	800 x 600 LVDS	
3	1024 x 768 LVDS	24 bits
4	1280 x 1024 LVDS	
5	1400 x 1050 LVDS	
6	1024 x 768 LVDS	18 bits
7	1600 x 1200	48 bits
8	1280 x 1024	48 bits

#	LCD Resolution	BITs
9	800 x 600	24 bits
10	800 x 600	18 bits
11	1024 x 768	36 bits
12		
13		
14		
15		
16		
17		

>Southbridge Configuration

- Onboard AC'97 Audio – [***Auto***] or [Disabled]
- Restore on AC Power Loss – [Power Off], [***Power On***], or [Last State]

  Use this field to determine how the system responds after an AC power loss, but this feature only operates with an ATX type power supply.

  * If [Power Off] is selected, the power is held off until the power button is pressed.
  * If [Power On] is selected, the power is restored to the computer, as soon as, AC power is available.
  * If [Last State] is selected, power is restored to the previous power state before the power loss actually occurred.

NOTE

This feature only operates with an ATX type power supply. The term *AC power loss* used in this context refers to the loss of the standby voltage on the 5V_SB pins and is continuously monitored after the system is turned off. If the standby voltage is not detected after 30 seconds, then it is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.

If you use an inexpensive ATX power supply, you may experience a short AC power sag, where the system turns off but does not switch back on. This can occur even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.

The ETX 802 does not require a CMOS battery to support the *Power Loss Control* feature.

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Power Menu Screen

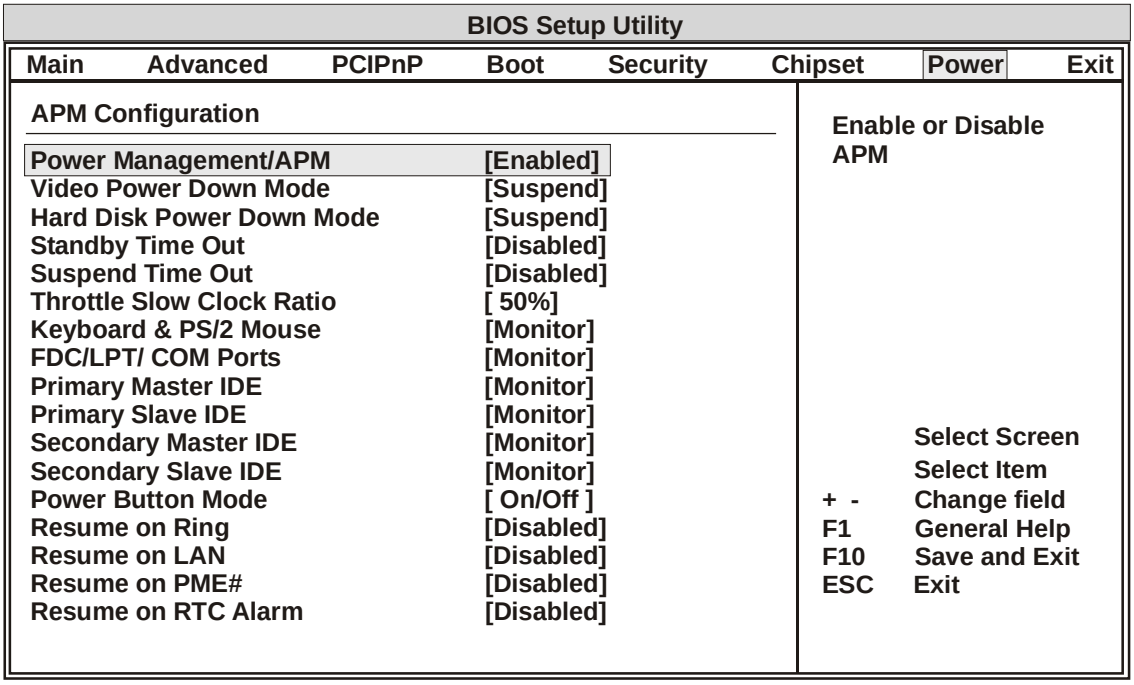


Figure 4-7. Power Menu Screen

APM Configuration

This power management feature is an older standard and may not be as widely supported today as it once was. The current preference for power management control is ACPI.

- Power Management/APM – [Disabled] or [***Enabled***]

  If [Enabled] is selected, the following items appear on the screen.

  - Video Power Down Mode – [*Disabled*], [Standby] or [**Suspend**]
    - If [Disabled] is selected, the BIOS is prevented from initiating any power saving modes related to the video display or the monitor.
    - If [Standby] is selected, the monitor is placed into standby mode after the specified period of display inactivity has expired. The monitor screen appears blacked out, but the monitor remains powered in a low state.
    - If [Suspend] is selected, the monitor is placed into a suspended mode after the specified period of display inactivity has expired. The monitor screen appears blacked out, but the monitor remains powered in a low state.
  - Hard Disk Drive (HDD) Power Down Mode – [*Disabled*], [Standby] or [**Suspend**]
    - If [Disabled] is selected, the hard disk drive (HDD) is prevented from going into a power down mode. .
    - If [Standby] is selected, the hard disk drive (HDD) is stopped from spinning during this standby mode.
    - If [Suspend] is selected, the power to the hard disk drive (HDD) is removed during this system suspend state.

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- Standby Time Out – [***Disabled***], [1 Min], [2 Min], [4 Min], [8 Min], [10 Min], [20 Min], [30 Min], [40 Min], [50 Min], or [60 Min]
  - If [Disabled] is selected, the system is prevented from entering the standby mode.
  - If [1 to 60] is selected, the system enters standby mode after being inactive for the specified number of minutes, such as, 1 minute, 2 minutes, 4 minutes, etc.
- Suspend Time Out – [***Disabled***], [1 Min], [2 Min], [4 Min], [8 Min], [10 Min], [20 Min], [30 Min], [40 Min], [50 Min], or [60 Min]
  - If [Disabled] is selected, the system is prevented from entering the suspend mode.
  - If [1 to 60] is selected, the system enters suspend mode after being inactive for the specified number of minutes, such as, 1 minute, 2 minutes, 4 minutes, etc.
- Throttle Slow Clock Ratio – [87.5%], [75.0%], [62.5%], [***50%***], [37.5%], [25%], or [12.5%]

  This field allows the BIOS to throttle the CPU clock to reduce power consumption by the percentage selected. .

  Selecting [87.5% to 12.5%] allows the BIOS to throttle back the CPU clock and operate a the percentage specified. For example, a throttle ratio of 50% means the clock is turned off during half of it its normal operational time. Selecting 87.5%, means the CPU clock is operating 87.5% of the time.
- Keyboard & PS/2 Mouse – [***Monitor***] or [Ignore]
  - If [Monitor] is selected, the activity of the Keyboard & PS/2 Mouse can wake up the system from a power management state.
  - If [Ignore] is selected, the Keyboard & PS/2 Mouse will not wake up the system from a power management state.
- FDC/LPT/COM Ports – [***Monitor***] or [Ignore]
  - If [Monitor] is selected, the activity on the FDC/LPT/COM Ports can wake up the system from a power management state.
  - If [Ignore] is selected, the FDC/LPT/COM Ports will not wake up the system from a power management state.
- Primary master IDE – [***Monitor***] or [Ignore]
  - If [Monitor] is selected, activity on the Primary Master IDE channel can wake up the system from a power management state.
  - If [Ignore] is selected, activity on the Primary Master IDE channel will not wake up the system from a power management state.
- Primary slave IDE – [***Monitor***] or [Ignore]
  - If [Monitor] is selected, activity on the Primary Slave IDE channel can wake up the system from a power management state.
  - If [Ignore] is selected, activity on the Primary Slave IDE channel will not wake up the system from a power management state.
- Secondary master IDE – [***Monitor***] or [Ignore]
  - If [Monitor] is selected, activity on the Secondary Master IDE channel can wake up the system from a power management state.
  - If [Ignore] is selected, activity on the Secondary Master IDE channel will not wake up the system from a power management state.

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- Secondary slave IDE – [***Monitor***] or [Ignore]
  - If [Monitor] is selected, activity on the Secondary Slave IDE channel can wake up the system from a power management state.
  - If [Ignore] is selected, activity on the Secondary Slave IDE channel will not wake up the system from a power management state.

- Power Button Mode – [***On/Off***] or [Suspend]

  This field allows you to activate the Power Button for use with sleep states and it will transition the system between power on and sleep states. This feature is also OS dependent as well.
- Resume On Ring – [***Disabled***] or [Enabled]
- Resume On LAN – [***Disabled***] or [Enabled]
- Resume On PME# – [***Disabled***] or [Enabled]
- Resume on RTC Alarm – [***Disabled***] or [Enabled]
  - If Resume on RTC Alarm is [Enabled] the following fields appear on screen.
  - RTC Alarm Date (Days) – [***Every Day***], [01], [02], [03], [04], [05], [06], [07], [08], [09], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], or [31]
  - System Time – [**12:30:30**]

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Exit and Defaults Menu Screen

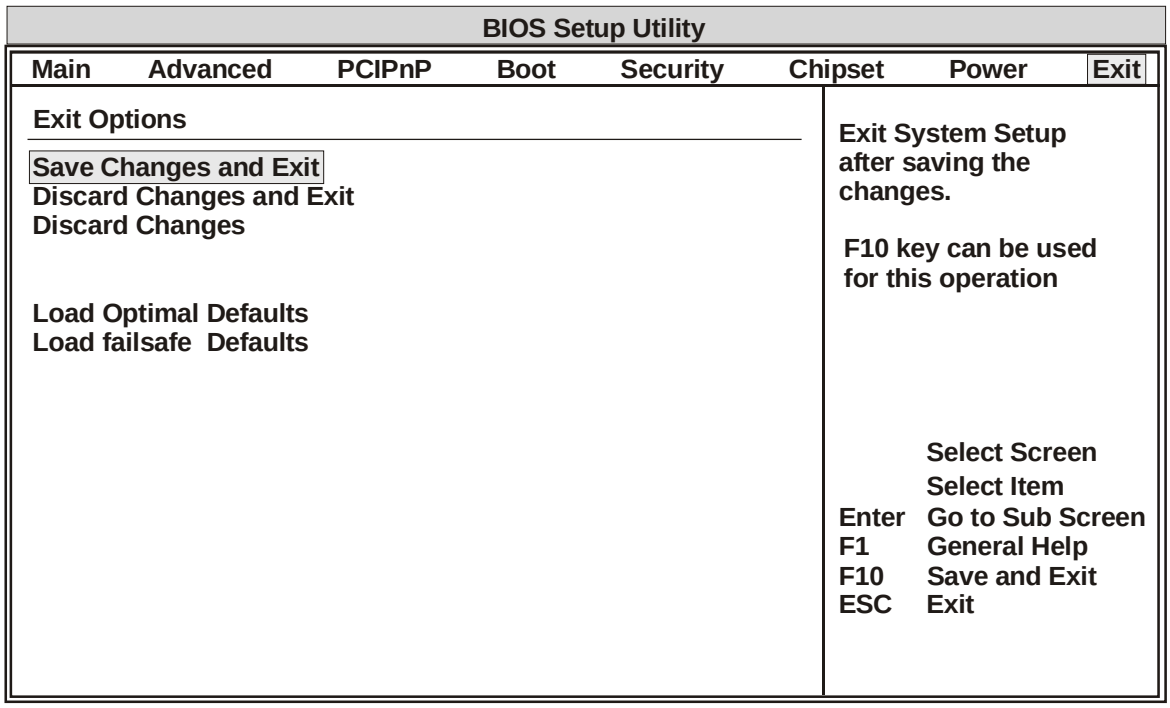


Figure 4-8. Exit and Defaults Menu Screen

Exit Options

- Save Changes and Exit

  This selection allows you to leave Setup, saving your changes, and rebooting the system so the new BIOS Setup configuration parameters can take effect.

  - Select **Save Changes and Exit** from the Exit Options menu and press <*Enter*>.

    The following text appears on screen:

    ```
    Save configuration changes and exit setup?

    [Ok][Cancel]
    ```

  - Select **Ok** to save changes and exit.

  The < F10 > key can also be used for this operation.

- Discard Changes and Exit

  This selection allows you to quit Setup without making any permanent changes to the BIOS Setup system configuration.

  - Select **Discard Changes and Exit** from the Exit Options menu and press <*Enter*>.

    The following text appears on screen:

    ```
    Discard changes and exit setup?

    [Ok][Cancel]
    ```


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- Select **Ok** to discard changes and exit.

The < ESC > key can also be used for this operation.

- Discard Changes

  This selection allows you to discard any changes made to BIOS Setup without leaving BIOS Setup.

  - Select **Discard Changes** from the Exit menu and press <*Enter*>.

    The following text appears on screen:

    ```
    Discard Changes?

    [Ok][Cancel]
    ```

  - Select **Ok** to discard changes.

  The < F7 > key can also be used for this operation.

Loading Defaults

- Load Optimal Defaults

  This selection automatically sets all BIOS Setup options to a complete set of default Optimal settings. The Optimal settings are designed for maximum system performance, but may not work best for all system applications. In particular, do not use the Optimal setup options if your system is experiencing system configuration problems.

  - Select **Load Optimal Defaults** from the Exit menu and press <*Enter*>.

    The following text appears on screen:

    ```
    Load Optimal Defaults?

    [Ok][Cancel]
    ```

  - Select **Ok** to load Optimal defaults.

  The < F9 > key can also be used for this operation.

- Load Failsafe Defaults

  This selection automatically sets all BIOS Setup options to a complete set of default Fail-Safe settings. The Fail-Safe settings are designed for maximum system stability, but not maximum performance. Select the Fail-Safe Setup options if your system is experiencing system configuration problems.

  - Select **Load Fail-Safe Defaults** from the Exit menu and press <*Enter*>.

    The following text appears on screen:

    ```
    Load Failsafe Defaults?

    [Ok][Cancel]
    ```

  - Select **Ok** to load Failsafe defaults.

  The < F8 > key can also be used for this operation.

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Appendix A Technical Support

Ampro Computers, Inc. provides a number of methods for contacting Technical Support listed in the Table A-1 below. Requests for support through the Virtual Technician are given the highest priority, and usually will be addressed within one working day.

- Ampro Virtual Technician – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the Ampro web site at http://ampro.custhelp.com. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online before you can log in to access this service.
- Personal Assistance – You may also request personal assistance by going to the "Ask a Question" area in the Virtual Technician. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request, you must log in to go to the "My Stuff" area where you can check status, update your request, and access other features.
- Embedded Design Resource Center – This service is also free and available 24 hours a day at the Ampro web site at http://www.ampro.com. However, you must be register online before you can log in to access this service.

  The Embedded Design Resource Center was created as a resource for embedded system developers to share Ampro's knowledge, insight, and expertise gained from years of experience. This page contains links to White Papers, Specifications, and additional technical information.

Table A-1. Technical Support Contact Information

Method	Contact Information
Virtual Technician	http://ampro.custhelp.com
Web Site	http://www.ampro.com
Standard Mail	Ampro Computers, Incorporated 5215 Hellyer Avenue San Jose, CA 95138-1007, USA

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Appendix B LAN Boot Feature

This Appendix describes the LAN Boot feature provided with ETX 802 COM (Computer-on-Module). The balance of this appendix briefly describes how to set up LAN Boot feature using the PXE boot agent BIOS settings. The LAN Boot feature is not enabled or disabled in the ETX 802 BIOS Setup Utility, but its boot order can be changed.

Introduction

LAN Boot is supported by the single Ethernet port on the ETX 802 assembly (baseboard), and is based on the Preboot eXecution Environment (PXE), an open industry standard. PXE (pronounced “pixie”) was designed by Intel, along with other hardware and software vendors, as part of the Wired for Management (WfM) specification to improve management of desktop systems. This technology can also be applied to the embedded system market place. PXE turns the ETX 802 Ethernet port into boot device when connected over a network (LAN).

PXE boots the ETX 802 from the network (LAN) by transferring a "boot image file" from a server. This image file is typically the operating system for the ETX 802, or a pre-OS agent that can perform management tasks prior to loading the image file (OS). A management task could include scanning the hard drive for viruses before loading the image file.

PXE is not operating system-specific, so the image file can load any OS. The most common application of PXE (LAN Boot) is installing an OS on a brand new device (hard disk drive) that has no operating system, (or reinstalling it when the operating system has failed or critical files have been corrupted).

Using PXE prevents the user from having to manually install all of the required software on the storage media device, (typically a hard disk drive) including the OS, which might include a stack of installation CD-ROMs. Installing from the network is as simple as connecting the ETX 802 and its baseboard to the network and powering it on. The server can be set up to detect new devices and install software automatically, thereby greatly simplifying the management of small to large numbers of systems attached to a network.

If the hard disk drive should crash, the network can be set up to do a hardware diagnostic check, and once a software-related problem is detected, the server can re-install the defective software, or all the ETX 802 software from the server. Booting from the network also guarantees a "clean" boot, with no boot-time viruses or user-modified files. The boot files are stored on the PXE server, where the files can be protected from infection and user-modification.

To effectively make use of the Ampro supplied feature (LAN Boot), a PXE boot agent (included with ETX 802 BIOS) and a PXE server are required. The PXE server is designed to work in conjunction with a Dynamic Host Configuration Protocol (DHCP) server and also requires a TFTP (Trivial File Transfer Protocol) server. The PXE server can be shared with DHCP server or installed on a different server and may require additional PXE server components. This makes it possible to add PXE to an existing network without affecting the existing DHCP server or configuration. Refer to the LAN Boot directory on the ETX 802 Doc & SW CD-ROM and the web sites listed here for more information on PXE boot agents, PXE servers, and PXE server components. For a more detailed technical description of how PXE works go to, http://www.pxe.ca. For more detailed information concerning pre-OS agents, go to: http://www.pre-OS.com.

Ampro provides an Intel® PXE boot agent integrated into the ETX 802 BIOS, but does not provide the PXE server or its components. You will need to provide your own PXE server and any of its components, before making full use of the LAN Boot feature. When you change the BIOS settings to move LAN Boot to the top of the boot order, you will need to exit BIOS Setup, saving your settings, and reboot the system to enter and set the PXE boot agent settings. Refer to the next topic *Accessing PXE Boot Agent BIOS Setup* for more setup and configuration information.

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Accessing PXE Boot Agent BIOS Setup

This section describes how to setup the LAN boot feature and access Intel's PXE Boot agent BIOS settings, which is integrated into the ETX 802 BIOS Setup Utility. The PXE Boot Agent's BIOS setup menu and screens are used when configuring the LAN Boot feature in the ETX 802 BIOS.

The Intel PXE Boot agent provided by Ampro only supports two boot protocols over the network. It supports RPL (Remote Program Load) and the Wired for Management (WfM) 2.0 specification for Preboot eXecution Environment (PXE).

To access PXE Boot Agent BIOS Setup when you want to use the LAN Boot feature in the ETX 802 BIOS Setup, refer to this procedure:

1. Connect an Ethernet cable to the ETX 802 baseboard and reboot the system.
2. Access the ETX 802 BIOS Setup utility and scroll to the Boot menu.
3. Move the [Network: IBA FE Slot 0100 v4.xxx] device to the top of the boot order (1st Boot Device) in Boot Device Priority, before selecting *Save Changes and Exit*.

   This should reboot the system, but if you miss it, reboot the system so you can enter the LAN Boot Setup.
4. Access the PXE Boot Agent (LAN Boot) Setup by pressing the Ctrl + S keys, when the following message appears on the boot screen.

   ```
   Initializing Intel (R) Boot Agent FE v4.x.xx
   PXE v2.0 Build 084 (WfM 2.0), RPL v2.78
   Press Ctrl + S to enter the setup Menu..
   ```

   If you miss this message, reboot the system and press Ctrl + S early in the boot process.
5. Select from the menu options when the PXE Boot Agent screen appears similar to the one shown in Figure B-1.
6. Follow the instructions at the bottom of the screen to navigate through the selections and modify any settings.
7. Save your changes (F4) and reboot the system.

   When you reboot the system the PXE Boot Agent will make two attempts to find and load the boot image using a PXE server (DHCPServer).

   Messages similar to the ones listed here may appear, however briefly, on screen.

```
Intel (R) Boot Agent FE v4.x.xx
Copyright © 1997-2005, Intel Corporation

Intel (R) Boot Agent PXE Base Code (PXE-2.1 build 084)
Copyright © 1997-2005, Intel Corporation

Initializing and Establishing Link…… (BIOS detecting Ethernet link)

CLIENT MAC ADDR:  xx xx xx xx xx xx GUID: xxxxxxxx xxxx xxxxx……
DHCP ……/  (looking for PXE server and boot filename)


(If errors occur, you might see one of the following messages)
PXE-E53:  No boot filename received (no boot filename found)
Or
PXE-E61:  Media test failure, check cable (no cable connection)

PXE-M0F:  Exiting Intel Boot Agent
```


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PXE Boot Agent Setup Screen

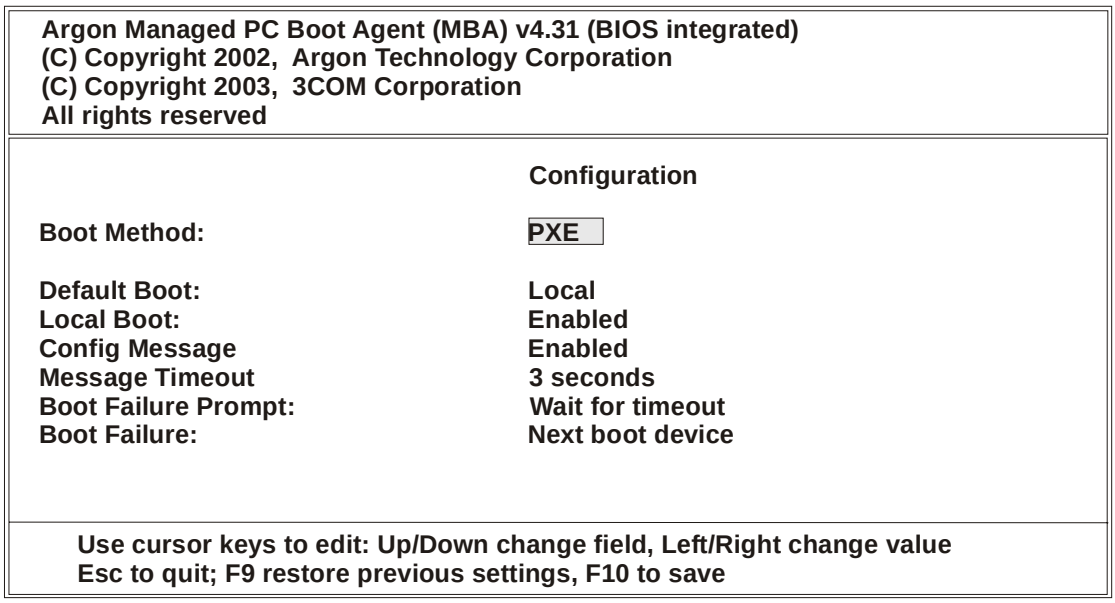


Figure B-1. PXE Agent Boot Setup Screen

- **PXE Configuration**
  - Network Boot Protocol – [**PXE**], or [RPL]

    Selects PXE (Preboot eXecution Environment) or RPL (Remote Program Load) protocol
  - Boot Order – [**Use BIOS setup Boot order**]

    This field selects boot order method for boot device queries.
  - Show Setup Prompt – [Disabled] or [**Enabled**]

    This field selects when the Ctrl + S message appears during initialization.
  - Setup Menu Wait Time – [0 seconds], [**2 seconds**], [3 seconds], or [5 seconds]

    This field select number of seconds to wait for Ctrl + S message during initialization.
  - Legacy OS Wakeup Support – [Disabled] or [**Enabled**]

    This field allows non-windows OS to use adapter remote wakeup capability.
- **RPL Configuration**
  - Network Boot Protocol – [PXE], or [**RPL**]
  - Boot Order – [**Use BIOS setup Boot order**]
  - Show Setup Prompt – [Disabled] or [**Enabled**]
  - Setup Menu Wait Time – [0 seconds], [**2 seconds**], [3 seconds], or [5 seconds]
  - Legacy OS Wakeup Support – [Disabled] or [**Enabled**]

NOTE	The default values are shown highlighted (**bold text**) in the list of options on the following pages. Refer to the bottom of the Setup screen for navigation instructions and when making selections.

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