ETX

ETX-EV133

User's Manual
ver. 1.2



ADLINK TECHNOLOGY INC.

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Revision History

Release	Date	Initials	Change
1.0	9/6/2004	JC	Initial release
1.1	10/12/2004	JC	- changed all reference to Audio Codec AL201A to VT1616 - added shared FDD support - updated SMB/I²C parapgraph - added Appendix A : Heatspreader
1.2	11/1/2005	HB	- changed I2C addresses for onboard devices

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1 Introduction

1.1 Description

ETX-EV133 is an ETX compatible module specially designed to facilitate speedy development of semi custom designs. ETX is an open standard that targets the market for embedded OEM projects. An ETX core combined with a custom made carrier board represents a value solution that allows OEM customers to get to the market fast. ETX Core modules are also know as COM (Computer on module) or as SOM (System on Module).

ETX-EV133 is based on the VIA's Eden ESP processor combined with VIA Apollo PLE133T and VT82C686B chipsets. The onboard SODIMM socket supports 144-pin SODIMM type memory modules that can accommodates up to 512MB non-ECC SDRAM modules. VIA Eden Processor is available in the range of 400 Mhz up to 1 Ghz.

The VIA VT82C686B Southbridge incorporates a PCI/ISA bridge, a VGA AGP controller, an EIDE controller supporting both PIO and UDMA modes, USB ports v1.1, two serial ports, one parallel port (SPP/ECP/EPP), one PS2 keyboard/mouse interface, AC97 audio interface and power management functionallity.

Additonally onboard are an 10/100Base-T Ethernet port, watchdog timer, an AC97 Audio Codec and support for LVDS based Flat Panel displays.

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2 Specifications

1.1 General

- **CPU** : VIA Eden ESP processor (eBGA package)
  Standard : VIA Eden ESP 4000, 6000, 8000 or 10K Low Voltage CPU's
  with 133 MHz FSB and 64 KB L2 cache
- **System Memory** : 144-pin SODIMM socket for up 512 MB PC100/133 non-ECC SDRAM
- **L2 Cache** : integrated in CPU (see above)
- **Chipset** : VIA Apollo PLE133T with VT8601T Northbridge and VT82C686B Southbridge
- **Enhanced IDE** : two ports and up to 4 ATAPI devices, supports Ultra DMA transfer rates of up to 100 MB/sec
- **BIOS** : AWARD 2 Mb Flash BIOS with ACPI and APM 1.2 power management with console redirection and CMOS backup in onboard EEPROM
- **Watchdog Timer** : 254-level timer generates RESET
- **Expansion** : 16-bit ISA and 32-bit PCI 2.1

1.2 Display

- **Chipset** : integrated AGP2X Trident Blade 2D/3D Video Accelerator (VT8601T)
- **Memory** : up to 8 MB UMA Video RAM
- **CRT** : up to UXGA 1600 x 1200 @ 32bpp
- **Flat Panel** : supports TFT on single channel LVDS (18-bit)

1.3 Multi I/O

- **Serial** : 2 high speed RS-232C ports (COM1/COM2)
- **Parallel** : SPP, EPP and ECP mode (pinout shared with FDD)
- **FDD** : one drive, (pinout shared with LPT1)
- **IrDA** : supports SIR IrDA 1.1 compliant
- **USB** : supports up to 4 ports ver 1.1
- **Keyboard & Mouse** : one PS/2 keyboard and one PS/2 mouse

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1.4 Audio

- Chipset : included in VT82C686B
- Audio Codec : VT1616 AC97 ver. 2.0

1.5 LAN

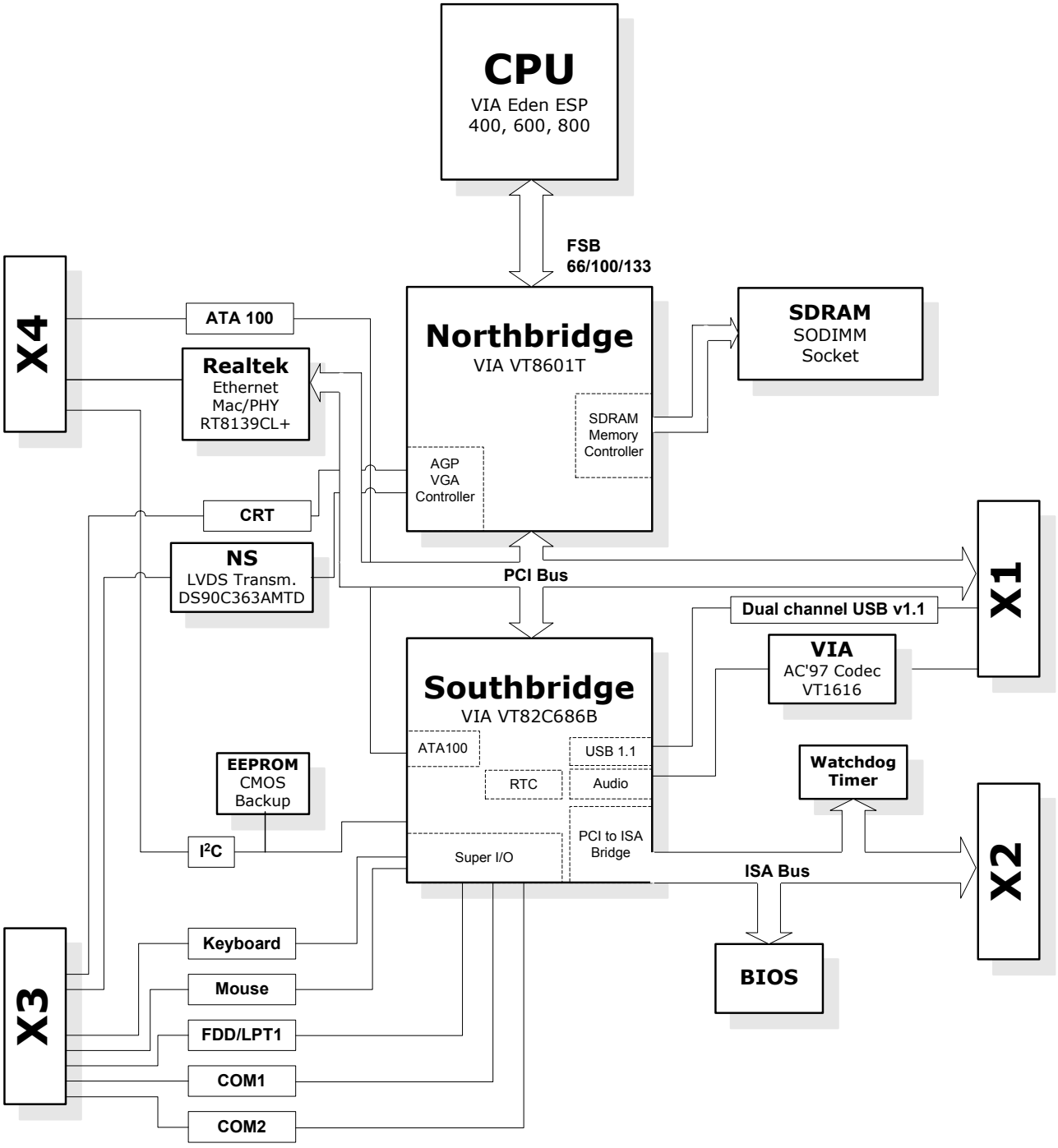
- Chipset: Realtek 8139CL+
- Ethernet Interface : 10/100 Mbps, Wake-on-LAN supported

1.6 Mechanical and Environmental

- Power Requirement (+5V only) :
  10 Watt typical ; (VIA Eden 600 MHz with 256 MB SDRAM)
- Operating Temperature : 0 to 55°C (32 to 140°F)
- Relative Humidity : up to 90% @ 55°C
- ETX Board Dimensions : 95 mm x 114 mm (3.7" x 4.5")
- Weight : 87 grams

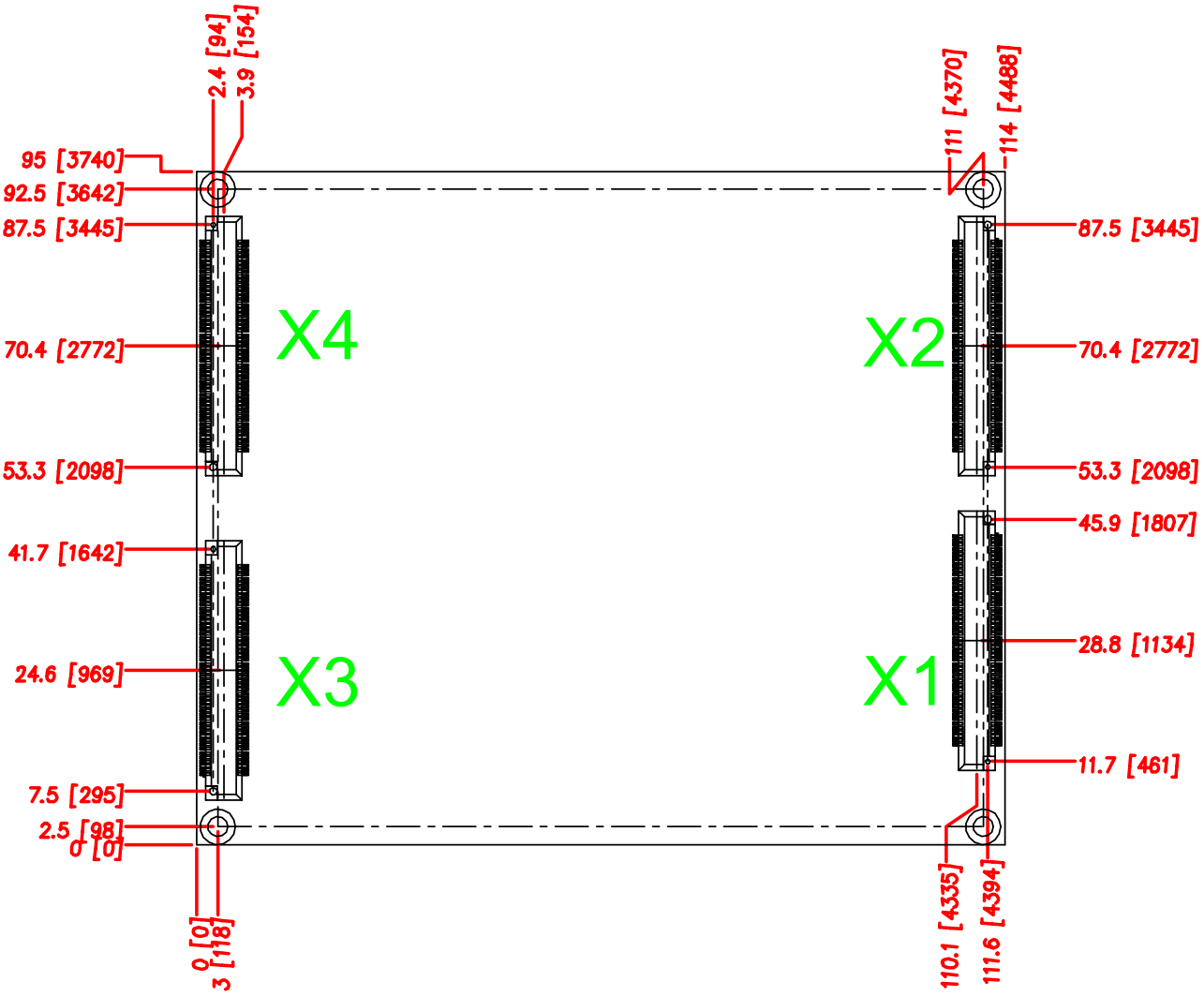
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3 Function diagram



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4 Mechanical Dimensions



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5 Watchdog Timer



The ETX-EV133 includes a watchdog timer (WDT) that consists of a one-second resolution down counter. Once a value is written to the to WDT, the timer automatically starts to count down to 1 (not to zero !). If the counter ever reaches 1, before the software restarts it, the software is presumed to be malfunctioning and the processor's RESET signal is asserted.

The watchdog function can be enabled or disabled by setting the control register at I/O port 440h and 443h.

Status	Action
Enable / Refresh the Watchdog Timer	Write timeout value to address 440h
Disable the Watchdog Timer.	Read 443h

Programming Example :

Enable Watchdog Timer :

Write Timeout value to I/O port 440h

```
mov    dx , 440h
mov    al, <1~255>
out    dx,al
```

Disable Watchdog Timer :

Write any Value to I/O port 443h

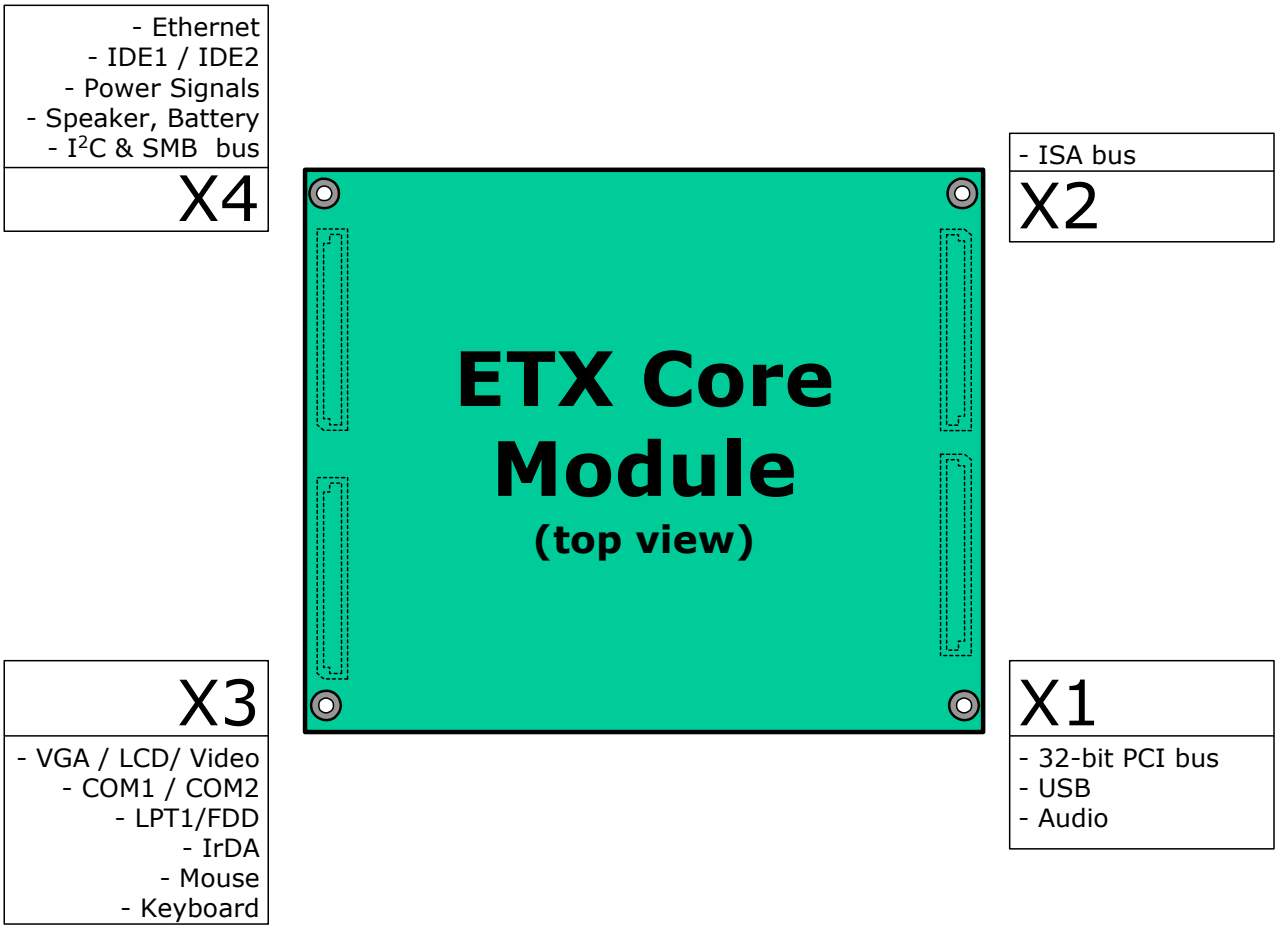
```
mov    dx, 443h
mov    al, 1<any value>
out    dx, al
```

Value	Timeout
1	0sec.
2	1sec.
3	2sec.
4	3sec.
5	4sec.
6	5sec.
7	6sec.
8	7sec.
9	8sec.
A	9sec.
B	10sec.
C	11sec.
D	12sec.
E	13sec.
F	14sec.
.....	.....
FF	254sec.

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6 Connectors

6.1 Connector Location



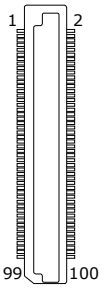
6.2 Pin-Out Compatibillity

All pin-outs on X1, X2, X3 and X4 of the ETX-EV133 comply with pin-out and signal description used in the original : “ETX Specification ver 2.6”. This document includes : description of pin-outs, signal descriptions and mechanical characteristics of the ETX formfactor.

An addtional document called “ ETX Design Guide” is a general introduction to carrier board design for ETX core modules

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6.3 X1 Connector : PCI-bus, USB and Audio



Signals and Pinout

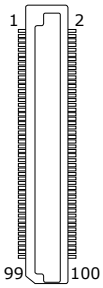
Pin	Signal	Pin	Signal
1	GND	2	GND
3	PCICLK3	4	PCICLK4
5	GND	6	GND
7	PCICLK1	8	PCICLK2
9	REQ3#	10	GNT3#
11	GNT2#	12	3.3V (1)
13	REQ2#	14	GNT1#
15	REQ1#	16	3.3V (1)
17	GNT0#	18	RESERVED
19	VCC	20	VCC
21	SERIRQ	22	REQ0#
23	AD0	24	3.3V (1)
25	AD1	26	AD2
27	AD4	28	AD3
29	AD6	30	AD5
31	C/BE0#	32	AD7
33	AD8	34	AD9
35	GND	36	GND
37	AD10	38	LINEIN_L
39	AD11	40	MICIN
41	AD12	42	LINEIN_R
43	AD13	44	AVCC
45	AD14	46	LINEOUT_L
47	AD15	48	AGND
49	C/BE1#	50	LINEOUT_R

Pin	Signal	Pin	Signal
51	VCC	52	VCC
53	PAR	54	SERR#
55	PERR#	56	RESERVED
57	PME#	58	USB2-
59	LOCK#	60	DEVSEL#
61	TRDY#	62	USB3-
63	IRDY#	64	STOP#
65	FRAME#	66	USB2+
67	GND	68	GND
69	AD16	70	C/BE2#
71	AD17	72	USB3+
73	AD19	74	AD18
75	AD20	76	USB0-
77	AD22	78	AD21
79	AD23	80	USB1-
81	AD24	82	C/BE3#
83	VCC	84	VCC
85	AD25	86	AD26
87	AD28	88	USB0+
89	AD27	90	AD29
91	AD30	92	USB1+
93	PCIRST#	94	AD31
95	INTC#	96	INTD#
97	INTA#	98	INTB#
99	GND	100	GND

(1) pin 12, 16, 24 are for 3.3 V power output, with combined capacity of 500 mA

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6.4 X2 Connector : ISA Bus



Signals and Pinout

Pin	Signal	Pin	Signal
1	GND	2	GND
3	SD14	4	SD15
5	SD13	6	MASTER#
7	SD12	8	DREQ7
9	SD11	10	DACK7#
11	SD10	12	DREQ6
13	SD9	14	DACK6#
15	SD8	16	DREQ5
17	MEMW#	18	DACK5#
19	MEMR#	20	DREQ0
21	LA17	22	DACK0#
23	LA18	24	IRQ14
25	LA19	26	IRQ15
27	LA20	28	IRQ12 (1)
29	LA21	30	IRQ11
31	LA22	32	IRQ10
33	LA23	34	IO16#
35	GND	36	GND
37	SBHE#	38	M16#
39	SA0	40	OSC
41	SA1	42	BALE
43	SA2	44	TC
45	SA3	46	DACK2# (2)
47	SA4	48	IRQ3
49	SA5	50	IRQ4

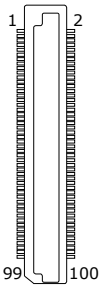
Pin	Signal	Pin	Signal
51	VCC	52	VCC
53	SA6	54	IRQ5
55	SA7	56	IRQ6
57	SA8	58	IRQ7
59	SA9	60	SYSCLK
61	SA10	62	REFSH#
63	SA11	64	DREQ1
65	SA12	66	DACK1#
67	GND	68	GND
69	SA13	70	DREQ3
71	SA14	72	DACK3#
73	SA15	74	IOR#
75	SA16	76	IOW#
77	SA18	78	SA17
79	SA19	80	SMEMR#
81	IOCHRDY	82	AEN
83	VCC	84	VCC
85	SD0	86	SMEMW#
87	SD2	88	SD1
89	SD3	90	NOWS#
91	DREQ2 (2)	92	SD4
93	SD5	94	IRQ9
95	SD6	96	SD7
97	IOCHK#	98	RSTDRV
99	GND	100	GND

(1) IRQ12 is reserved for PS/2 mouse, this pin is NC on ETX-EV133

(2) DREQ2/DACK2# are signals to support an FDD controller on a secondary Super I/O chip, these pins are NC on ETX-EV133

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6.4 X3 Connector : CRT, LCD, Video, COM1/2, LPT1, IrDA, Mouse, Keyboard



Signals and Pinout

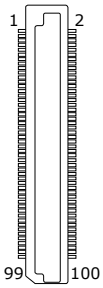
Pin	Signal	Pin	Signal
1	GND	2	GND
3	RED	4	BLUE
5	HSYNC	6	GREEN
7	VSYNC	8	DDC2B_CLK
9	PAL_DETECT#	10	DDC2B_DAT
11	NC	12	NC
13	NC	14	NC
15	GND	16	GND
17	NC	18	NC
19	NC	20	NC
21	GND	22	GND
23	NC	24	NC
25	NC	26	NC
27	GND	28	GND
29	LCDDO4	30	LCDDO7
31	LCDDO5	32	LCDDO6
33	GND	34	GND
35	LCDDO1	36	LCDDO3
37	LCDDO0	38	LCDDO2
39	VCC	40	VCC
41	JILI_DAT (1)	42	FLM
43	JILI_CLK (1)	44	BLON#
45	BIASON	46	PLPWR_EN
47	TV_COMP (1)	48	TV_Y (1)
49	TV_SYNC (1)	50	TV_C (1)

Pin	Signal	Pin	Signal
51	LPT/FLPY#	52	RESERVED
53	VCC	54	GND
55	STB#	56	AFD#
57	RESERVED	58	PD7
59	IRRX	60	ERR#
61	IRTX	62	PD6
63	RXD2	64	INIT#
65	GND	66	GND
67	RTS2#	68	PD5
69	DTR2#	70	SLIN#
71	DCD2#	72	PD4
73	DSR2#	74	PD3
75	CTS2#	76	PD2
77	TXD2	78	PD1
79	RI2#	80	PD0
81	VCC	82	VCC
83	RXD1	84	ACK#
85	RTS1#	86	BUSY#
87	DTR1#	88	PE
89	DCD1#	90	SLCT#
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND

(1) These pins are not connected

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6.5 X4 Connector : IDE1, IDE2, Ethernet, Miscellaneous



Signals and Pinout

Pin	Signal	Pin	Signal
1	GND	2	GND
3	5V_SB	4	PWGIN
5	PS_ON	6	SPEAKER
7	PWRBTN#	8	BATT
9	KBINH	10	LILED
11	RSMRST#	12	ACTLED
13	ROMKBCS# (1)	14	SPDLED
15	EXT_PRG (1)	16	I2CLK
17	VCC	18	VCC
19	OVCR#	20	GPCS# (1)
21	EXTSMI#	22	I2DAT
23	SMBCLK	24	SMBDATA
25	SIDE_CS3#	26	SMBALRT#
27	SIDE_CS1#	28	DASP_S (1)
29	SIDE_A2	30	PIDE_CS3#
31	SIDE_A0	32	PIDE_CS1#
33	GND	34	GND
35	PDIAG_S	36	PIDE_A2
37	SIDE_A1	38	PIDE_A0
39	SIDE_INTRQ	40	PIDE_A1
41	BATLOW#	42	GPE1# (2)
43	SIDE_ACK#	44	PIDE_INTRQ
45	SIORDY	46	PIDE_ACK#
47	SIDE_IOR#	48	PIORDY
49	VCC	50	VCC

Pin	Signal	Pin	Signal
51	SIDE_IOW#	52	PIDE_IOR#
53	SIDE_DRQ	54	PIDE_IOW#
55	SIDE_D15	56	PIDE_DRQ
57	SIDE_D0	58	PIDE_D15
59	SIDE_D14	60	PIDE_D0
61	SIDE_D1	62	PIDE_D14
63	SIDE_D13	64	PIDE_D1
65	GND	66	GND
67	SIDE_D2	68	PIDE_D13
69	SIDE_D12	70	PIDE_D2
71	SIDE_D3	72	PIDE_D12
73	SIDE_D11	74	PIDE_D3
75	SIDE_D4	76	PIDE_D11
77	SIDE_D10	78	PIDE_D4
79	SIDE_D5	80	PIDE_D10
81	VCC	82	VCC
83	SIDE_D9	84	PIDE_D5
85	SIDE_D6	86	PIDE_D9
87	SIDE_D8	88	PIDE_D6
89	GPE2# (3)	90	CBLID_P#
91	RXD-	92	PIDE_D8
93	RXD+	94	SIDE_D7
95	TXD-	96	PIDE_D7
97	TXD+	98	HDRST#
99	GND	100	GND

(1) These pins are not connected

(2) GPE1# for case open detection

(3) GPE2# is for wake up system

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7 System Resources

7.1 Interrupt Assignment

PCI and ISA interrupts supported by the VIA VT82C686B South Bridge are as follows:

ISA IRQ	Edge/ Level	Polarity	Interrupt Source	Notes
NMI	Edge	High	SERR_L asserted	
SMI	Edge	Low	VT82C686B Hardware Monitor	
IRQ0	Edge	High	Timer0	(1)
IRQ1	Edge	High	Keyboard	
IRQ2	Edge	High	Cascade Interrupt from Slave Interrupt Controller	
IRQ3	Edge	High	COM2	(2)
IRQ4	Edge	High	COM1	(2)
IRQ5	Edge	Low	PCI PnP IRQ	
IRQ6	Edge	High	FDC	(2)
IRQ7	Edge	High	LPT1	(2)
IRQ8_L	Edge	Low	Real Time Clock	(2)
IRQ9	Edge	Low	PCI PnP IRQ	
IRQ10	Level	Low	PCI PnP IRQ	
IRQ11	Level	Low	PCI PnP IRQ, USB	(3)
IRQ12	Edge	High	Mouse	(2)
IRQ13	Edge	High	FERR_L asserted	
IRQ14	Edge	High	Primary IDE	(4)
IRQ15	Edge	High	Secondary IDE	(5)

Notes:

1 ▶ Internally generated by the VT82C686B.

2 ▶ Suggested. These interrupts are plug and play compatible and may be routed to any available interrupt.

3 ▶ The USB interrupt is internally routed to the PIRQD# input of the VT82C686B.

4 ▶ This interrupt is routed to the IRQ14 input of the VT82C686B.

5 ▶ This interrupt is routed to the IRQ15 input of the VT82C686B.

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7.2 PCI Bus Arbitration Assignment

PCI Bus Request	PCI Master(s)	IDSEL
Request 0	LAN 8139CL+	AD23
Request 1	Routed to ETX connector X1	*
Request 2	Routed to ETX connector X1	*
Request 3	Routed to ETX connector X1	*
Request 4	Routed to ETX connector X1	*

Note: IDSEL routing depends on the design of the carrier board.

7.3 PCI Interrupt Routing

Device	Net PIRQ0_L	Net PIRQ1_L	Net PIRQ2_L	Net PIRQ3_L
ETX Connector X1	PIRQA#	PIRQB#	PIRQC#	PIRQD#
Audio	PIRQC#			
LAN 8139CL+	PIRQD#			

7.4 Memory Map

Address	Size	Description
00000000~0009FFFF	640K	DOS Application Area
000A0000~000BFFFF	128K	Video Buffer Area
000C0000~000DFFFF	1M	Expansion Area
000F0000~000FFFFF	64K	System BIOS Area
000E0000 ~000EFFFF	64K	Extended System BIOS Area
00100000~DRAM Top	---	System memory area
DRAM Top ~FFFRFFFF	---	Bus area
FFFEFFFF ~ FFFFFFFF	64K	Initialization area

7.5 Direct Memory Access Channels

DMA#	Available	Description
0	Yes	
1	Yes	Unavailable if Sound Blaster is enabled with default configuration
2	No	Used by FDC
3	Yes	Unavailable when LPT is in ECP mode
4	No	Used for Cascade
5	Yes	
6	Yes	
7	Yes	

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7.6 I/O Adddres Map

Address	Size	Description
0000 - 001F	32 bytes	Master DMA controller
0020 - 002D	14 bytes	Master Interrupt Controller
0040 - 005F	32 bytes	Timer/Counter
0060 - 006F	32 bytes	Keyboard Controller
60h	1 byte	KBC data
61h	1 byte	Misc function and Speaker control
64h	1 byte	KBC command / status
0070 - 0077	8 bytes	RTC/CMOS/NMI-Disable
0078 - 007F	8 bytes	Available for system use
0080	1 byte	Reserved (Debug port)
0081 - 008F	16 bytes	DMA page registers
0090 - 0091	2 bytes	Available for system use
0092	1 byte	System Control
0093 - 009F	13 bytes	Available for system use
00A0 - 00BF	32 bytes	Slave Interrupt Controller
00C0 - 00DF	32 bytes	Slave DMA Controller
00E0 - 00FF	32 bytes	Available for system use
0100 - 0CF7		Available for system use
0CF8 -0CFB	4 bytes	PCI configuration address
0CFC - 0CFF	4 bytes	PCI configuration data
0D00 - FFFF		Available for system use

Notes:

1 ▶ I/O space 370-371h is reserved for external I/O controllers .

2 ▶ I/O space 3E8-3EFh is reserved for COM3, and 2E8-2EFh for COM4.

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7.7 System Management Bus and I²C

Internally the SMB bus and I²C bus are one and the same. The VT82C868B Southbridge supports only SMBDAT and SMBCLK lines that are I2C compatible.

The X4 connector has pinouts for both I²C and SMB bus. Both are connected to the same pins on the VT82C868B : the I²C compatible SMB bus. It is advisable to always connect external (carrier board) I²C devices to the I²C pins and SMB devices to the SMB pins to stay compatible with other modules that might support two internal busses (sperate I²C and SMB bus on the Southbridge). Adresses on the SMB/I²C bus already occupied by devices on the module are :

Address	Function	Device
1010 000	Identification Info	SODIMM0
1010 111	CMOS setting backup	EEPROM
inside LAN ID	Control and Status	Ethernet # 1

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8 Phoenix Award BIOS

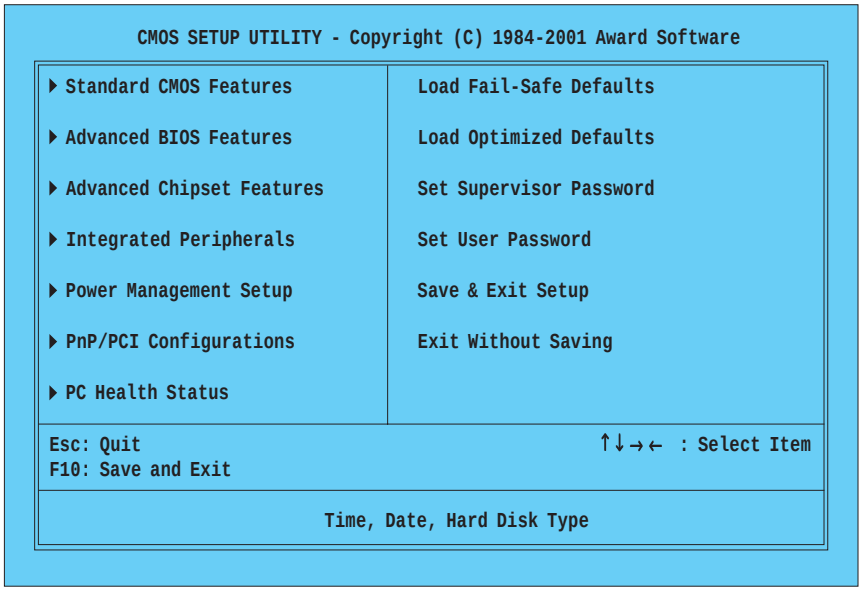
8.1 Description

The module has a Phoenix Award PCI/ISA BIOS ver 6.0 for the system configuration. The Award BIOS setup program is designed to provide the maximum flexibility in configuring the system by offering various options which could be selected for end-user requirements. This chapter is written to assist you in the proper usage of these features.

To access the Phoenix AWARD PCI/ISA BIOS Setup program,

press <Del> key.

The Main Menu will be displayed at this time.



8.2 Main Menu Setup Items

The main menu includes the following main setup categories. Recall that some systems may not include all entries.

Standard CMOS Features *(see paragraph 7.3)*

Use this menu for basic system configuration.

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Advanced BIOS Features *(see paragraph 7.4)*

Use this menu to set the Advanced Features available on your system.

Advanced Chipset Features *(see paragraph 7.5)*

Change values in the chipset registers and optimize your system's performance.

Integrated Peripherals *(see paragraph 7.6)*

Use this menu to specify your settings for integrated peripherals.

Power Management Setup *(see paragraph 7.7)*

Use this menu to specify your settings for power management.

PnP / PCI Configuration *(see paragraph 7.8)*

This entry appears if your system supports PnP / PCI.

PC Health Status *(see paragraph 7.9)*

Use this menu to specify your settings for frequency/voltage control.

Load Fail-Safe Defaults

Loads the BIOS default values for the minimal/stable performance for your system to operate.

Load Optimized Defaults

Loads the BIOS default values that are factory settings for optimal system performance.

Supervisor / User Password

Use this menu to set User and Supervisor Passwords.

Save & Exit Setup

Save CMOS value changes to CMOS and exit setup.

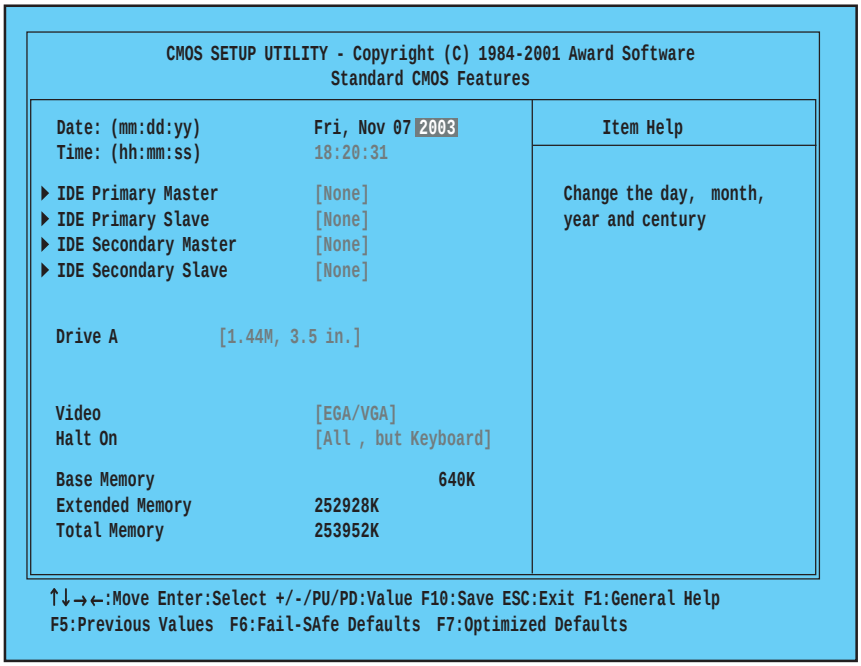
Exit Without Saving

Abandon all CMOS value changes and exit setup.

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8.3 Standard CMOS Features

The main menu includes the following main setup categories. Recall that some systems may not include all entries.



Date

The BIOS determines the day of the week from the other date information; this field is for information only.

Time

The time format is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Press the « or (key to move to the desired field . Press the PgUp or PgDn key to increment the setting, or type the desired value into the field.

IDE Primary and Secondary Master/Slave Items

This selection brings you a configuration menu of the designated Drive (see next page)

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Drive A

The ETX-IV266 can support one single FDD drive. Because FDD and LPT1 share the same pins on the X3 connector, only one of them can be used at the time. Enabling either LPT1 or FDD can be done in the BIOS :

▶ **Integrated Peripherals** ▶ **LPT1 Setting / FDD**

This allows you to setup LPT1 resources or disable LPT1 and set mode to FDD

After enabling the FDD select the correct specifications for the diskette drive

None : No diskette drive installed

360K : 5.25 in5-1/4 inch PC-type standard drive

1.2M : 5.25 in5-1/4 inch AT-type high-density drive

720K : 3.5 in3-1/2 inch double-sided drive

1.44M : 3.5 in3-1/2 inch double-sided drive

2.88M : 3.5 in3-1/2 inch double-sided drive

Video

Select the type of primary video subsystem in your computer. The BIOS usually detects the correct video type automatically. The BIOS supports a secondary video subsystem, but you do not select it in Setup.

Halt On

During the power-on self-test (POST), the computer stops if the BIOS detects a hardware error. You can tell the BIOS to ignore certain errors during POST and continue the boot-up process. These are the selections:

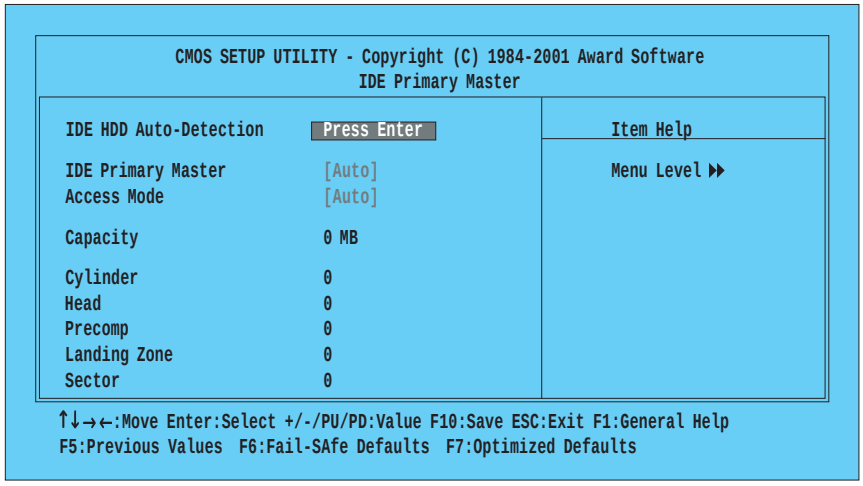
No errors : POST does not stop for any errors.

All errors : If any non-fatal error, POST stops and prompts to take corrective action.

All, But Keyboard : POST does not stop for a keyboard error, but stops for all other error

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IDE Primary and Secondary Master/Slave Items



IDE HDD Auto-detection	Press Enter	Press Enter to auto-detect the HDD on this channel. If detection is successful, it fills the remaining fields on this menu.
IDE Primary Master	None/Auto/Manual	Selecting 'manual' lets you set the remaining fields on this screen. Selects the type of fixed disk. "User Type" will let you select the number of cylinders, heads, etc. Note: PRECOMP=65535 means NONE !
Capacity	Auto Display disk size	Disk drive capacity (Approximated). Note that this size is usually slightly greater than the size of a formatted disk given by a disk checking program.
Access Mode	CHS/LBA/Large/Auto	Choose the access mode for this hard disk

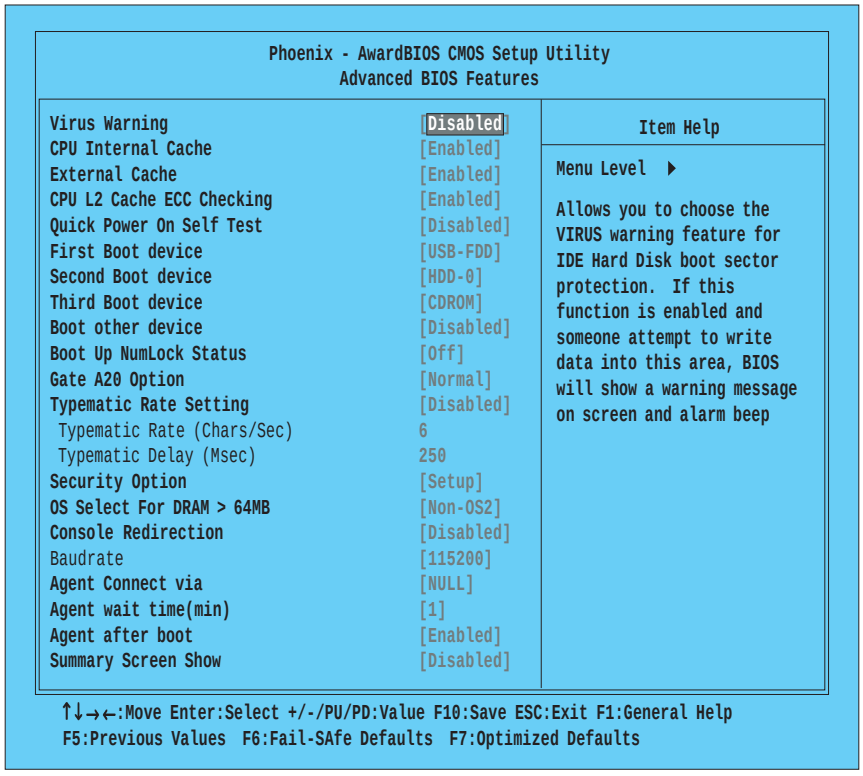
The following options are selectable only if the 'IDE Primary Master' item is set to 'Manual'

Cylinder	Min = 0 Max = 65535	Set the number of cylinders for this hard disk.
Head	Min = 0 Max = 255	Set the number of read/write heads
Precomp	Min = 0 Max = 65535	**** Warning: Setting a value of 65535 means no hard disk
Landing zone	Min = 0 Max = 65535	****
Sector	Min = 0 Max = 255	Number of sectors per track

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8.4 Advanced BIOS Features

This section allows you to configure your system for basic operation. You have the opportunity to select the system's default speed, boot-up sequence, keyboard operation, shadowing, security.



Virus Warning

Allows you to choose the VIRUS Warning feature for IDE Hard Disk boot sector protection. If this function is enabled and someone attempt to write data into this area, BIOS will show a warning message on screen and alarm beep.

Enabled : Activates automatically when the system boots up causing a warning message to appear when anything attempts to access the boot sector or hard disk partition table.
Disabled : No warning message will appear

CPU Internal Cache / CPU External Cache

These two categories speed up memory access. However, it depends on CPU/chipset design.
Enabled : Enable cache, Disabled : Disable cache

CPU L2 Cache ECC Checking

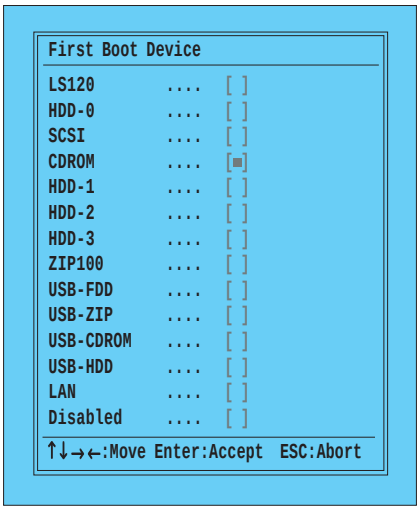
This item allows you to enable/disable CPU L2 Cache ECC checking. Enabled, Disabled.

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Quick Power On Self Test

This category speeds up Power On Self Test (POST) after you power up the computer. If it is set to Enable, BIOS will shorten or skip some check items during POST. Enabled : Enable quick POST. Disabled : Normal POST

First / Second / Third Boot Device



Enter brings you to Boot Device Menu. The BIOS attempts to load the operating system from the selected device.

See menu for possible options

Boot Other Device

When enabled the BIOS will try to boot from second or third option if booting from first device fails. When disabled the BIOS will not use the alternative devices

Boot Up NumLock Status

Select power on state for NumLock. The choice: On/Off

Gate A20 Option

Select if chipset or keyboard controller should control GateA20.
Normal : A pin in the keyboard controller controls GateA20
Fast : Lets chipset control GateA20

Typematic Rate Setting

Key strokes repeat at a rate determined by the keyboard controller. When enabled, the typematic rate and typematic delay can be selected. Choice: Enabled/Disabled.

Typematic Rate (Chars/Sec)

Sets the number of times a second to repeat a key stroke when you hold the key down. The choice: 6, 8, 10, 12, 15, 20, 24, 30.

Typematic Delay (Msec)

Sets the delay time after the key is held down before it begins to repeat the keystroke. The choice: 250, 500, 750, 1000.

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Security Option

Select whether the password is required every time the system boots or only when you enter setup. Chioces :

System : the system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.

Setup : The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

To disable security, select PASSWORD SETTING at Main Menu and then you will be asked to enter password. Do not type anything and just press <Enter>, it will disable security. Once the security is disabled, the system will boot and you can enter Setup freely.

OS Select For DRAM > 64MB

Select the operating system that is running with greater than 64MB of RAM on the system.The choice: Non-OS2, OS2.

Console Redirection

Award's Preboot Agent provides you with console redicrection to let you control a remote PC or embedded system via modem or direct serial connection at boot time. Choice : Enable, Disable.

Baudrate

Select baud rate : 9600, 19200, 38400, 57600 and 115200.

Agent Connect via

Fixed to NULL (Null modem cable), no slection possible.

Agent wait time(min)

Timeout in minutes to install agent if no serial connection can be established

Agent after boot

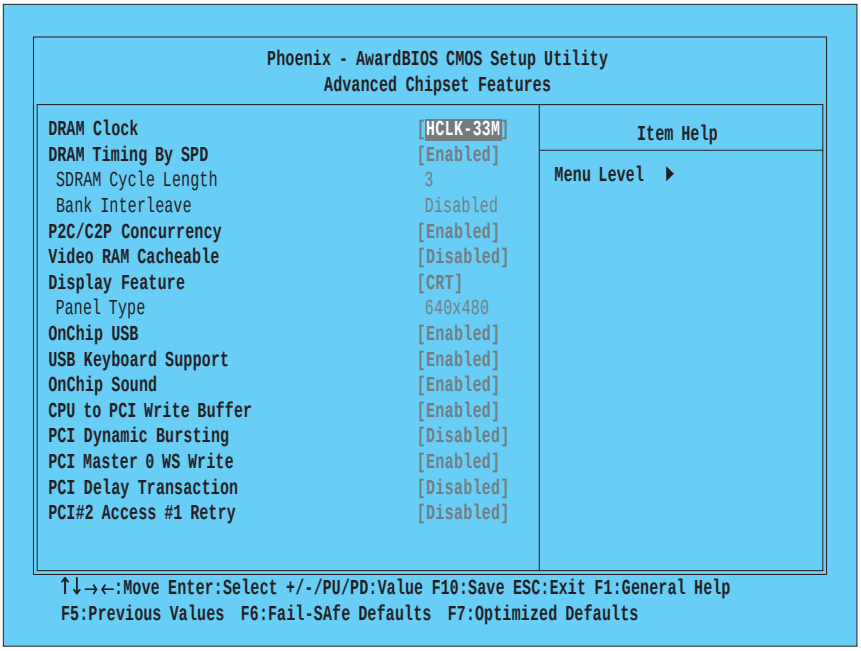
Enable this option to keep the Agent running after OS boot.

Summary Screen Show

Suppress the summary screen. Choice :Enable, Disable

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8.5 Advanced Chipset Features



DRAM Clock

This item allows you to set the DRAM Clock. Options are : Host CLK, HCLK+33M, HCLK-33M or Auto. Please set the item according to the Host (CPU) Clock and DRAM Clock.

DRAM Timing by SPD

If your DIMM memory have SPD (Serial Presence Detect) 8-pin IC on module, you can set this option to Enabled. System will set your DRAM clock and timing from the SPD IC. If the option set as Disabled, DRAM clock and timing must be set from items below. (DRAM Clock, SDRAM Cycle Length and Bank Interleave)

SDRAM Cycle Length

This feature is similar to SDRAM CAS Latency Time. It controls the time delay (in clock cycles - CLKs) that passes before the SDRAM starts to carry out a read command after receiving it. This also determines the number of CLKs for the completion of the first part of a burst transfer. Thus, the lower the cycle length, the faster the transaction. However, some SDRAM cannot handle the lower cycle length and may become unstable. So, set the SDRAM Cycle Length to 2 for optimal performance if possible but increase it to 3 if your system becomes unstable.

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Bank Interleave

This feature enables you to set the interleave mode of the SDRAM interface. Interleaving allows banks of SDRAM to alternate their refresh and access cycles. One bank will undergo its refresh cycle while another is being accessed. This improves performance of the SDRAM by masking the refresh time of each bank.

P2C/C2P Concurrency

This item allows you to enable/disable the PCI to CPU, CPU to PCI concurrency.
Choice: Enabled, Disabled

Video RAM Cacheable

Select Enabled allows caching of the video RAM , resulting in better system performance. However, if any program writes to this memory area, a system error may result.
Choice: Enabled, Disabled.Fast R-W Turn Around

Display Feature

This item allow you configure what type of the external display you are using.
The choices are : CRT or LVDS (Displays cannot be used conccurently)

Panel Type

When LVDS is selected in “Display Feature” than here the flat panel resolution can be selected.
The choices are The choices are : 640x480 ,800x600 and 1024x768.

OnChip USB

This should be enabled if your system has a USB installed on the system board and you want to use it. Even when so equipped, if you add a higher performance controller, you will need to disable this feature. Choice: Enabled, Disabled.

USB Keyboard Support

Select Enabled if your system contains a Universal Serial Bus (USB) controller and you have a USB keyboard. Choice: Enabled, Disabled.

OnChip Sound

This item allows you to control the onboard AC 97 audio. Choice: Enable, Disabled.

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CPU to PCI Write Buffer

When this field is Enabled, writes from the CPU to the PCI bus are buffered, to compensate for the speed differences between the CPU and the PCI bus. When Disabled, the writes are not buffered and the CPU must wait until the write is complete before starting another write cycle.
Choice: Enabled, Disabled.

PCI Dynamic Bursting

This item allows you to enable/ disable the PCI dynamic bursting function.
Choice: Enabled, Disabled

PCI Master 0 WS Write

When Enabled, writes to the PCI bus are executed with zero wait states.

PCI Delay Transaction

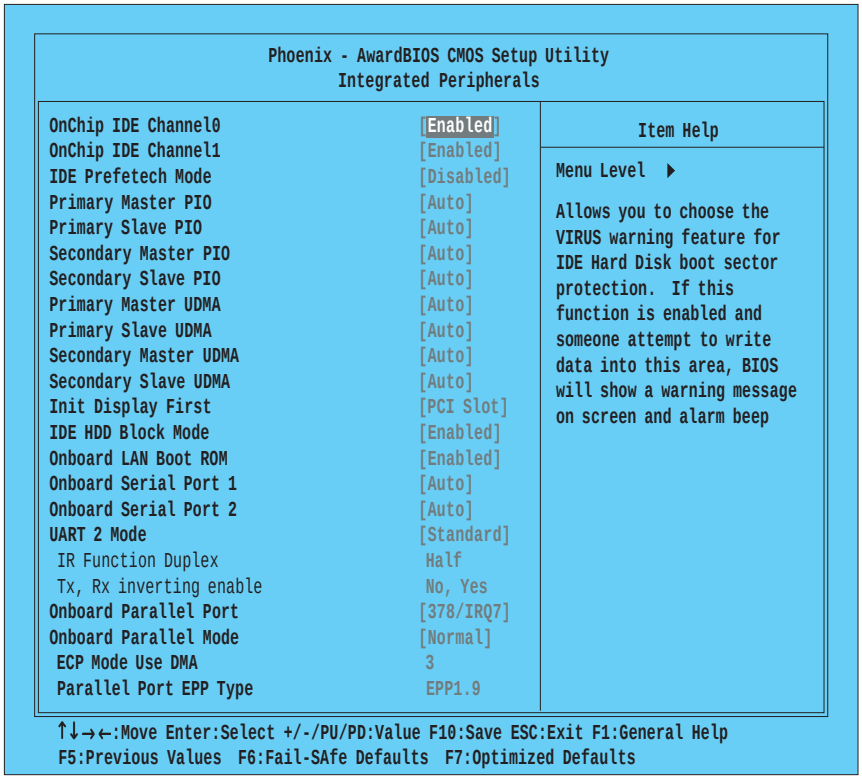
The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select Enabled to support compliance with PCI specification version 2.1.
Choice: Enabled, Disabled

PCI#2 Access #1 Retry

When disabled, PCI#2 will not be disconnected until access finishes (default). When enabled, PCI#2 will be disconnected if max retries are attempted without success.
Choice: Enabled, Disabled

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8.6 Integrated Peripherals



OnChip IDE Channel 0/1

The chipset contains a PCI IDE interface with support for two IDE channels. Select Enabled to activate the primary IDE interface. Select Disabled to deactivate this interface

Primary & Secondary Master/Slave PIO

The four IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance. In Auto mode, the system automatically determines the best mode for each device. Choice: Auto, Mode 0, Mode 1, Mode 2, Mode 3, Mode 4.

Primary & Secondary Master/Slave UDMA

Ultra DMA implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver. If your hard drive and your system software both support Ultra DMA, select Auto to enable BIOS support.

Init Display First

This item allows you to decide to active either PCI Slot or AGP first

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IDE HDD Block Mode

This feature enhances disk performance by allowing multi-sector data transfers and eliminates the interrupt handling time for each sector.

Onboard Serial Port 1 & 2

Select an address and corresponding interrupt for the first/second serial port. The default value for the first serial port is "3F8/IRQ4" and the second serial port is "2F8/IRQ3".

UART 2 Mode

This item allows you to select which mode for the Onboard Serial Port 2.
Choice: Standard, HPSIR, ASKIR

IR Function Duplex

This item allows you to select the IR half/full duplex funcion. Choice: Half, Full.

TX,RX inverting enable

This item allow you to enable the TX, RX inverting which depends on different H/W requirement. This field is not recommended to change its default setting for avoiding any error in your system
Choice: No, No/ No,Yes(Default)/ Yes, No/ Yes, Yes.

LPT1 Setting / FDD

This setting allows you to assign resources to LPT1 or disable the function and allow using an FDD drive. Since share LPT1 and FDD share the same pins on the X3 connector, only one of them can be used at the time.

Onboard Parallel Mode

Select an operating mode for the parallel port. Mode options are Normal, EPP, ECP, ECP/EPP.

ECP Mode Use DMA

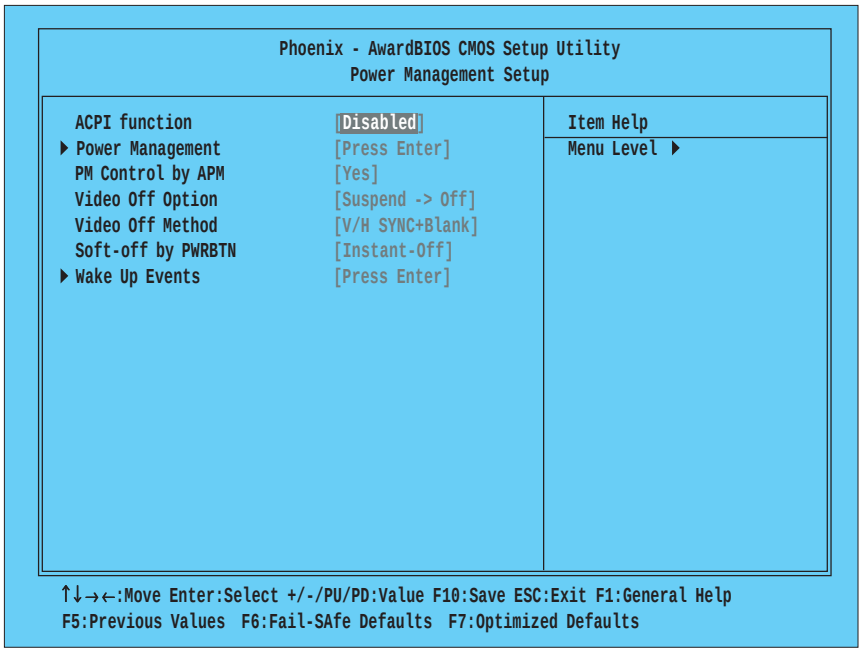
Select a DMA channel if parallel Mode is set as ECP, ECP/EPP.

Parallel Port EPP Type

Select a EPP Type if parallel Port is set as EPP, ECP/EPP.

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8.7 Power Management Setup



ACPI Function

Select Enabled only if your computer's operating system supports ACPI (the Advanced Configuration and Power Interface) specification.

Power Management

There are 4 selections for Power Management, 3 of which have fixed mode :

Disabled (default) No power management. Disables all four modes.

Min. Power Saving Minimum power management. Doze Mode = 1 hr.,

Standby Mode = 1 hr., Suspend Mode = 1 hr.,

Max. Power Saving Maximum power management -- ONLY AVAILABLE FOR SL CPU's.. Doze Mode = 1 min., Standby Mode = 1 min., Suspend Mode = 1 min.

User Defined Allows you to set each mode individually. When not disabled, each of the ranges are from 1 min. to 1 hr.

HDD Power Down is always set independently

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ACPI Suspend Type

S1 (POS) Power On suspend

All devices are powered up except for the clock synthesizer. The Host and PCI clocks are inactive and PIIX4 provides control signals and 32-kHz Suspend Clock (SUSCLK) to allow for DRAM refresh and to turn off the clock synthesizer. The only power consumed in the system is due to DRAM Refresh and leakage current of the powered devices. When the system resumes from POS, PIIX4 can optionally resume without resetting the system, can reset the processor only, or can reset the entire system. When no reset is performed, PIIX4 only needs to wait for the clock synthesizer and processor PLLs to lock before the system is resumed. This takes typically 20 ms.

S3 (STR) Suspend To RAM

Power is removed from most of the system components during STR, except the DRAM. Power is supplied to Suspend Refresh logic in the Host Controller, and RTC and Suspend Well logic in PIIX4. PIIX4 provides control signals and 32-kHz Suspend Clock (SUSCLK) to allow for DRAM refresh and to turn off the clock synthesizer and other power planes.

PM Control By APM

When enabled, an Advanced power Management device will be activated to enhance the Max. Power Saving mode and stop the CPU internal clock. If the Max. Power Saving is not enabled, this will be preset to No.

Video Off Option

Controls what causes the display to be switched off

Suspend -> Off Always On All Mode -> Off

Video Off Method

This determines the manner in which the monitor is blanked.

V/H SYNC+Blank cause the system to turn off the vertical and horizontal synchronization signals and writes blanks to the screen.

Blank Screen This option only writes blanks to the screen.

DPMS Initial display power management signaling.

Modem Use IRQ

Name the interrupt request (IRQ) assigned to the modem (if any) on your system. Activity of the selected IRQ always awakens the system.

Soft-Off By PWRBTN

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The field defines the power-off mode when using an ATX power supply. The Instant-Off mode means powering off immediately when pressing the power button. In the Delay 4 Sec mode, the system powers off when the power button is pressed for more than four seconds or places the system in a very low-power-usage state, with only enough circuitry receiving power to detect power button activity or resume by ring activity when press for less than four seconds. The default is 'Instant-Off'.

State After Power Failure

On : After a power failure, the system will automatically reboot as soon as power is restored.

Off : After a power failure, the system will not reboot when power is restored. The system needs to be turned on again manually.

Auto : After a power failure, the system will automatically reboot as soon power is restored if the PC was turned on when the power failed. If the PC was already turned off when the power failed, the system needs to be turned on again manually.

Wake Up Events

Setting an event on each device listed to awaken the system from a soft off state.

VGA

LPT & COM

HDD & FDD

PCI Master

Power On by PCI Card

Wake Up on LAN/Ring

RTC Alarm Resume

Date (of Month)

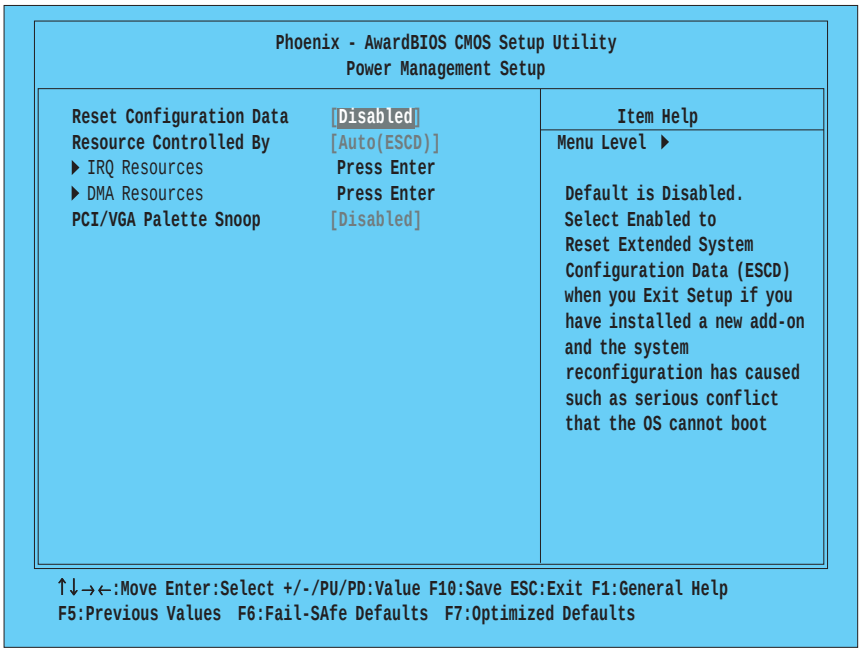
Resume Time (hh:mm:ss)

Primary INTR

IRQs Activity Monitoring

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8.8 PnP/PCI Configurations



This section describes configuring the PCI bus system. PCI, or Personal Computer Interconnect, is a system which allows I/O devices to operate at speeds nearing the speed the CPU itself uses when communicating with its own special components.

Reset Configuration Data

Normally, you leave this field Disabled. Select Enabled to reset ESCD (Extended System Configuration Date) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.

Resource Controlled By

The Award Play and Play BIOS can automatically configure all the boot and Plug-and-Play compatible devices. If you select Auto, all the interrupt request (IRQ) and DMA assignment fields disappear, as the BIOS automatically assigns them.

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IRQ Resources

When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt :

Legacy ISA
Devices compliant with the original PC/AT bus specification, requiring a specific interrupt (such as IRQ4 for serial port 1).

PCI/ISA PnP
Device compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

DMA Resources

When resources are controlled manually, assign each system DMA channel as one of the following types, depending on the type of device using the DMA :

Legacy ISA
Devices compliant with the original PC/AT bus specification, requiring a specific DMA channel.

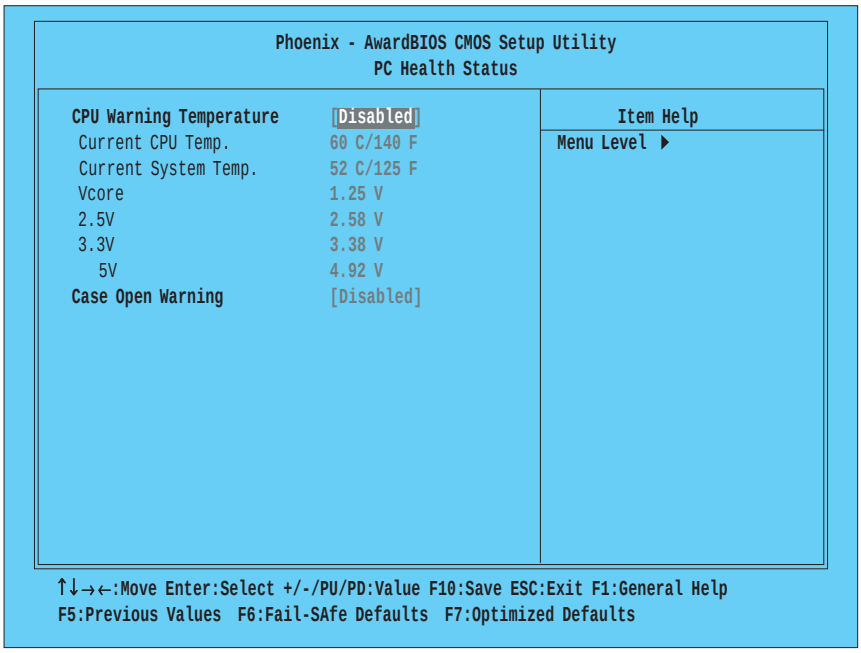
PCI/ISA PnP
Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

PCI/VGA Palette Snoop

Normally this option is always Disabled! Nonstandard VGA display adapters such as overlay cards or MPEG video cards may not show colors properly. Setting Enabled should correct this problem. If this field set Enabled, any I/O access on the ISA bus to the VGA card's palette registers will be reflected on the PCI bus. This will allow overlay cards to adapt to the changing palette colors.

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8.9 PC Health Status



CPU Warning Temperature

Brings up a submenu that lets you assign a temperature level that is not to be exceeded by the CPU. If the CPU temperature goes over this limit a audio warning signal sounds

Current CPU Temp.

Displays the current CPU temperature

Current System Temp.

Displays the current System temperature

Vcore, 2.5V, 3.3V, 5V

Displays the actual voltage levels on the board

Case Open Warning

When enabled an audible signal is generated when pin GPE1# and CBLID_P# on X4 are disconnected.

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8.10 BIOS POST Codes

POST (hex)	Description
CFh	Test CMOS R/W functionality.
C0h	Early chipset initialization: - Disable shadow RAM - Disable L2 cache (socket 7 or below) -Program basic chipset registers
C1h	Detect memory - Auto-detection of DRAM size, type and ECC - Auto-detection of L2 cache (socket 7 or below)
C3h	Expand compressed BIOS code to DRAM
C5h	Call chipset hook to copy BIOS back to E000 & F000 shadow RAM.
0h1	Expand the Xgroup codes locating in physical address 1000:0
02h	Reserved
03h	Initial Superio_Early_Init switch.
04h	Reserved
05h	1. Blank out screen 2. Clear CMOS error flag
06h	Reserved
07h	1. Clear 8042 interface 2. Initialize 8042 self-test
08h	1. Test special keyboard controller for Winbond 977 series Super I/O chips. 2. Enable keyboard interface.
09h	Reserved
0Ah	1. Disable PS/2 mouse interface (optional). 2. Auto detect ports for keyboard & mouse followed by a port & interface swap (optional). 3. Reset keyboard for Winbond 977 series Super I/O chips.
0Bh	Reserved
0Ch	Reserved
0Dh	Reserved
0Eh	Test F000h segment shadow to see whether it is R/W-able or not. If test fails, keep beeping the speaker.
0Fh	Reserved
10h	Auto detect flash type to load appropriate flash R/W codes into the run time area in F000 for ESCD & DMI support.
11h	Reserved
12h	Use walking 1's algorithm to check out interface in CMOS circuitry. Also set real-time clock power status, and then check for override.
13h	Reserved
14h	Program chipset default values into chipset. Chipset default values are MODBINable by OEM customers.
15h	Reserved
16h	Initial Early_Init_Onboard_Generator switch.
17h	Reserved
18h	Detect CPU information including brand, SMI type (Cyrix or Intel) and CPU level (586 or 686).

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POST (hex)	Description
19h	Reserved
1Ah	Reserved
1Bh	Initial interrupts vector table. If no special specified, all H/W interrupts are directed to SPURIOUS_INT_HDLR & S/W interrupts to SPURIOUS_soft_HDLR.
1Ch	Reserved
1Dh	Initial EARLY_PM_INIT switch.
1Eh	Reserved
1Fh	Load keyboard matrix (notebook platform)
20h	Reserved
21h	HPM initialization (notebook platform)
22h	Reserved
23h	1. Check validity of RTC value:e.g. a value of 5Ah is an invalid value for RTC minute. 2. Load CMOS settings into BIOS stack. If CMOS checksum fails, use default value instead. 3. Prepare BIOS resource map for PCI & PnP use. If ESCD is valid, take into consideration of the ESCD's legacy information. 4. Onboard clock generator initialization. Disable respective clock resource to empty PCI & DIMM slots. 5. Early PCI initialization: - Enumerate PCI bus number - Assign memory & I/O resource - Search for a valid VGA device & VGA BIOS, and put it into C000:0.
24h	Reserved
25h	Reserved
26h	Reserved
27h	Initialize INT 09 buffer
28h	Reserved
29h	1. Program CPU internal MTRR (P6 & PII) for 0-640K memory address. 2. Initialize the APIC for Pentium class CPU. 3. Program early chipset according to CMOS setup. 4. Measure CPU speed. 5. Invoke video BIOS.
2Ah	Reserved
2Bh	Reserved
2Ch	Reserved
2Dh	1. Initialize multi-language 2. Put information on screen display, including Award title, CPU type, CPU speed ….
2Eh	Reserved
2Fh	Reserved
30h	Reserved
31h	Reserved
32h	Reserved
33h	Reset keyboard except Winbond 977 series Super I/O chips.
34h	Reserved
35h	Test DMA Channel 0
36h	Reserved
37h	Test DMA Channel 1

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POST (hex)	Description
38h	Reserved
39h	Test DMA Page Registers
3Ah	Reserved
3Bh	Reserved
3Ch	Test 8254 Channel 2
3Dh	Reserved
3Eh	Test 8259 interrupt mask bits for channel 1.
3Fh	Reserved
40h	Test 8259 interrupt mask bits for channel 2.
41h	Reserved
42h	Reserved
43h	Test 8259 functionality.
44h	Reserved
45h	Reserved
46h	Reserved
47h	Initialize EISA slot
48h	Reserved
49h	1. Calculate total memory by testing the last double word of each 64K page. 2. Program writes allocation for AMD K5 CPU.
4Ah	Reserved
4Bh	Reserved
4Ch	Reserved
4Dh	Reserved
4Eh	1. Program MTRR of M1 CPU2. 2.Initialize L2 cache for P6 class CPU & program CPU with proper cacheable range. 3. Initialize the APIC for P6 class CPU.4. On MP platform, adjust the cacheable range to smaller one in case the cacheable ranges between each CPU are not identical.
4Fh	Reserved
50h	Initialize USB
51h	Reserved
52h	Test all memory (clear all extended memory to 0)
53h	Reserved
54h	Reserved
55h	Display number of processors (multi-processor platform)
56h	Reserved
57h	1. Display PnP logo 2. Early ISA PnP initialization 3. Assign CSN to every ISA PnP device.
58h	Reserved
59h	Initialize the combined Trend Anti-Virus code.
5Ah	Reserved
5Bh	Test EISA available memory
5Ch	Reserved
5Dh	1. Initialize Init_Onboard_Super_IO switch. 2. Initialize Init_Onbaord_AUDIO switch.
5Eh	Reserved

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POST (hex)	Description
5Fh	Reserved
60h	Okay to enter Setup utility; i.e. not until this POST stage can users enter the CMOS setup utility.
61h	Reserved
62h	Reserved
63h	Reserved
64h	Reserved
65h	Initialize PS/2 Mouse
66h	Reserved
67h	Prepare memory size information for function call: INT 15h ax=E820h
68h	Reserved
69h	Turn on L2 cache
6Ah	Reserved
6Bh	Program chipset registers according to items described in Setup & Auto-configuration table.
6Ch	Reserved
6Dh	1. Assign resources to all ISA PnP devices. 2. Auto assign ports to onboard COM ports if the corresponding item in Setup is set to "AUTO".
6Eh	Reserved
6Fh	1. Initialize floppy controller 2. Set up floppy related fields in 40:hardware.
70h	Reserved
71h	Reserved
72h	Reserved
73h	Initialize fixed disk controller
74h	Reserved
75h	Detect & install all IDE devices: HDD, LS120, ZIP, CDROM.....
76h	Reserved
77h	Detect serial ports & parallel ports.
78h	Reserved
79h	Reserved
7Ah	Detect & install co-processor
7Bh	Reserved
7Ch	Reserved
7Dh	Reserved
7Eh	Reserved
7Fh	1. Switch back to text mode if full screen logo is supported. - If errors occur, report errors & wait for keys - If no errors occur or F1 key is pressed to continue: wClear EPA or customization logo.
80h	Reserved
81h	Reserved
82h	1. Call chipset power management hook. 2. Recover the text fond used by EPA logo (not for full screen logo) 3. If password is set, ask for password.

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POST (hex)	Description
83h	Save all data in stack back to CMOS
84h	Initialize ISA PnP boot devices
85h	1. USB final Initialization 2. NET PC: Build SYSID structure 3. Switch screen back to text mode 4. Set up ACPI table at top of memory. 5. Invoke ISA adapter ROMs 6. Assign IRQs to PCI devices 7. Initialize APM 8. Clear noise of IRQs.
86h	Reserved
87h	Reserved
88h	Reserved
89h	Reserved
90h	Reserved
91h	Reserved
92h	Reserved
93h	Read HDD boot sector information for Trend Anti-Virus code
94h	1. Enable L2 cache 2. Program boot up speed 3. Chipset final initialization. 4. Power management final initialization 5. Clear screen & display summary table 6. Program K6 write allocation 7. Program P6 class write combining
95h	1. Program daylight saving 2. Update keyboard LED & typematic rate
96h	1. Build MP table 2. Build & update ESCD 3. Set CMOS century to 20h or 19h 4. Load CMOS time into DOS timer tick 5. Build MSIRQ routing table.
FFh	Boot attempt (INT 19h)

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Appendix A : **Heatspreader**

A.1 **Description**

The heatspreader on top of the ETX-EV133 is not a heatsink !

The heatspreader function is to ensure an identical mechanical profile for every type of ETX module. In this way the heatsolution, that is built on top of the heatspreader is compatible with any kind of ETX module not just the ETX-EV133. It enables the second source model for ETX or upgrade path to a higher performance ETX module. Any change in ETX board type does not requirre the complete rebuild of the heat solution in your application.



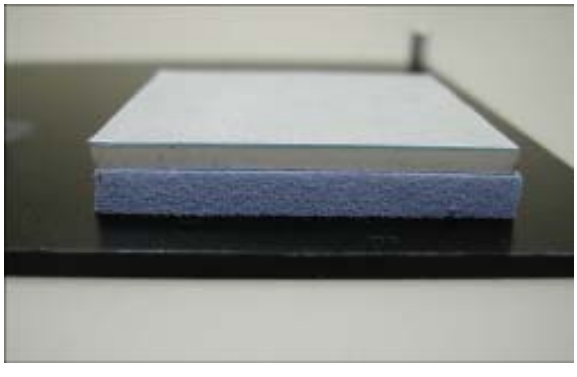
Remove the protective layer before placing the heatspreader on the module !



Heatspreader fitted on ETX-EV133



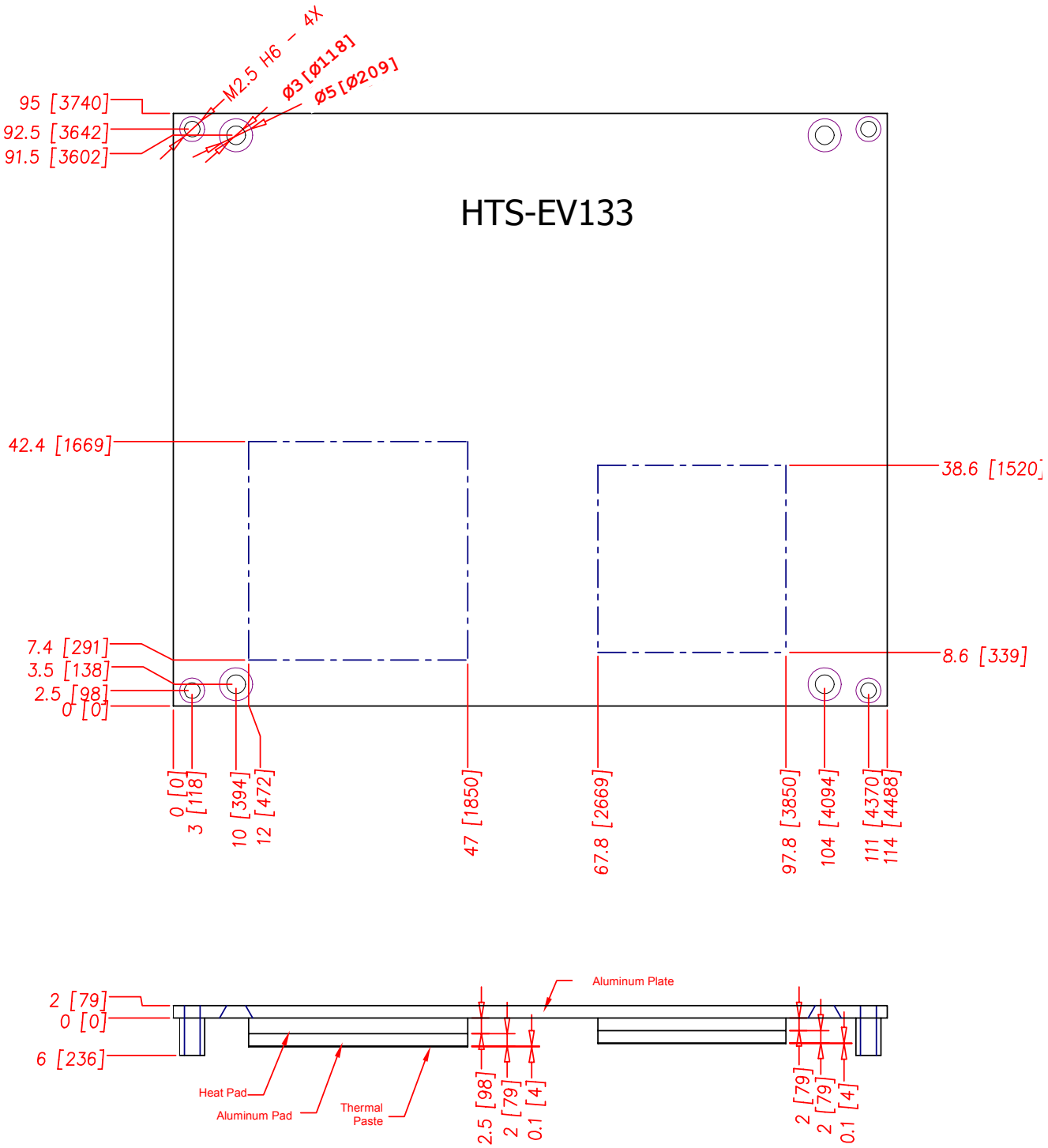
Heatpads for CPU and Northbridge



From bottom to top :
- Protective layer
- Conductive thermal paste
- Aluminum pad
- Flexible heat pad
- Aluminim plate

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A.1 Heatspreader Dimensions



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