ETX

ETX-IM333

User's Manual



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Part Number: 50-1J001-2010

ADLINK TECHNOLOGY INC.

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Revision History

Release	Date	Change
1.00	2005/01/14	Initial release
1.10	2005/03/23	Corrected X3 and X4 pin definitions Added SpeedStep® note to BIOS CPU speed settings
1.20	2005/04/02	Corrected X1, X2, X3, and X4 pin definitions, added FDD pins and LVDS mapping
1.30	2005/07/04	Added ISA support functions on latest version C1 and up PCB boards PCB version C1 and above are lead free Changed product picture on cover
1.40	2006/03/06	Corrected X1, X2, X3, and X4 pin assignments
1.50	2006/10/20	Corrected SMbus table paragraph 7.7 Added Appendix A: Heatspreaders and Heatsinks
1.60	2007/04/10	Updated all resource tables Updated BIOS description
2.00	2007/05/28	Document format conversion
2.10	2007/06/22	Corrected Multi I/O specifications for FDD Corrected WDT register sequence locations Corrected Signal and Pin notes Replaced BIOS Setup Pictures Removed incorrect data from System Management Bus table
2.20	2007/11/09	Layout Revision
2.21	2007/11/15	Removed several notations
2.22	2008/07/25	Correct address

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Preface

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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.



Additional information, aids, and tips that help users perform tasks.



Information to prevent *mino*r physical injury, component damage, data loss, and/or program corruption when trying to complete a task.



Information to prevent *serious* physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

1.1 Description

The ETX-IM333 is an ETX® compatible module specially designed to facilitate speedy development of semi-custom designs. ETX® is an open standard that targets embedded OEM projects. An ETX® core combined with a custom made carrier board delivers a valuable solution that allows OEM customers to get to the market fast. ETX® Core modules are also known as COM (Computer-On-Module) or as SOM (System-On-Module). ETX-IM333 is fully compliant with ETX® component SBC™ Specification V2.6.

The ETX-IM333 is based on the embedded Intel® 855GME Northbridge and ICH4 Southbridge. It supports Intel® Celeron® M and Intel® Pentium® M CPU's between 600 MHz to 1.7 GHz. The CPU-chipset combination is ideal for applications that require high performance, reliability, and long product lifecycles.

The Intel® 855GME chipset graphics memory controller hub (GMCH-M) provides an integrated graphics (250 MHz) controller, and power saving features. The 855GME Northbridge incorporates a DDR memory controller and supports up to 1 GB DDR333 memory in addition to DDR266/200 memory on a single 200-pin SODIMM socket. Display output to CRT and single/dual-channel LVDS is included. As an option, the board also supports TV Out (SDTV and HDTV).

The integrated EIDE controller supports both PIO and UDMA modes, USB 2.0 ports, two serial ports, one parallel port (SPP/ECP/EPP), one PS/2 keyboard/mouse interface port, AC'97 audio interface, fast Ethernet LAN controller, and power management features.

ETX-IM333 is RoHS-compliant and is lead free.

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2 Specifications

2.1 General

- CPU: Intel® Pentium® M or Intel® Celeron® M supports soldered LV/ULV uFCBGA packages or a uFCPGA socket
- Chipset: Intel® 855GME with 400 FSB and Intel® 82801DB I/O Control Hub 4
- Memory: one SODIMM socket for up to 1 GB DDR 200/266/333
- L2 Cache: 512 KB (Celeron-M), 1 MB (Pentium-M), 2 MB (Pentium-M)
- Enhanced IDE: two ports and up to four ATAPI devices, supports Ultra DMA transfer rates of up to 33 MB/sec
- BIOS: Phoenix AWARD PnP 4 Mb Flash with console redirection and CMOS EEPROM backup. USB boot/legacy and PXE support
- Hardware Monitor: integrated in Winbond 83627HF, monitors supply voltages and CPU temperature
- Watchdog: integrated in Winbond 83627HF software programmable 1-255 sec or 1-255 min, generates system reset
- Expansion: 32-bit PCI 2.2 and 8/16-bit ISA (only on C1 PCB version and higher)

2.2 Display

- Chipset: integrated Intel® 855GME Chipset graphics memory controller hub (GMCH-M), supports dual-independent display on CRT and LVDS channels
- Memory: up to 32 MB UMA Video RAM
- CRT: up to QXGA 2048 x 1536
- Flat Panel: supports single/dual-channel LVDS (18-bit) for display resolutions up to 1600 x 1200

2.3 TV-out (optional)

- Chipset: Philips® SAA-7104/05 Advanced Digital Video Encoder
- Output: PAL or NTSC legacy video output up to 1280 X 1024, HDTV supported

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2.4 Audio

- Chipset: integrated in Intel® 82801DB Southbridge
- Audio Codec: VIA VT1616 AC'97 ver. 2.0

2.5 LAN

- Chipset: ICH4 integrated Intel® 82562 compatible 32-bit PCI LAN controller
- Interface: 10/100 Mbps with Wake-on-LAN and Alert on LAN support

2.6 Multi I/O

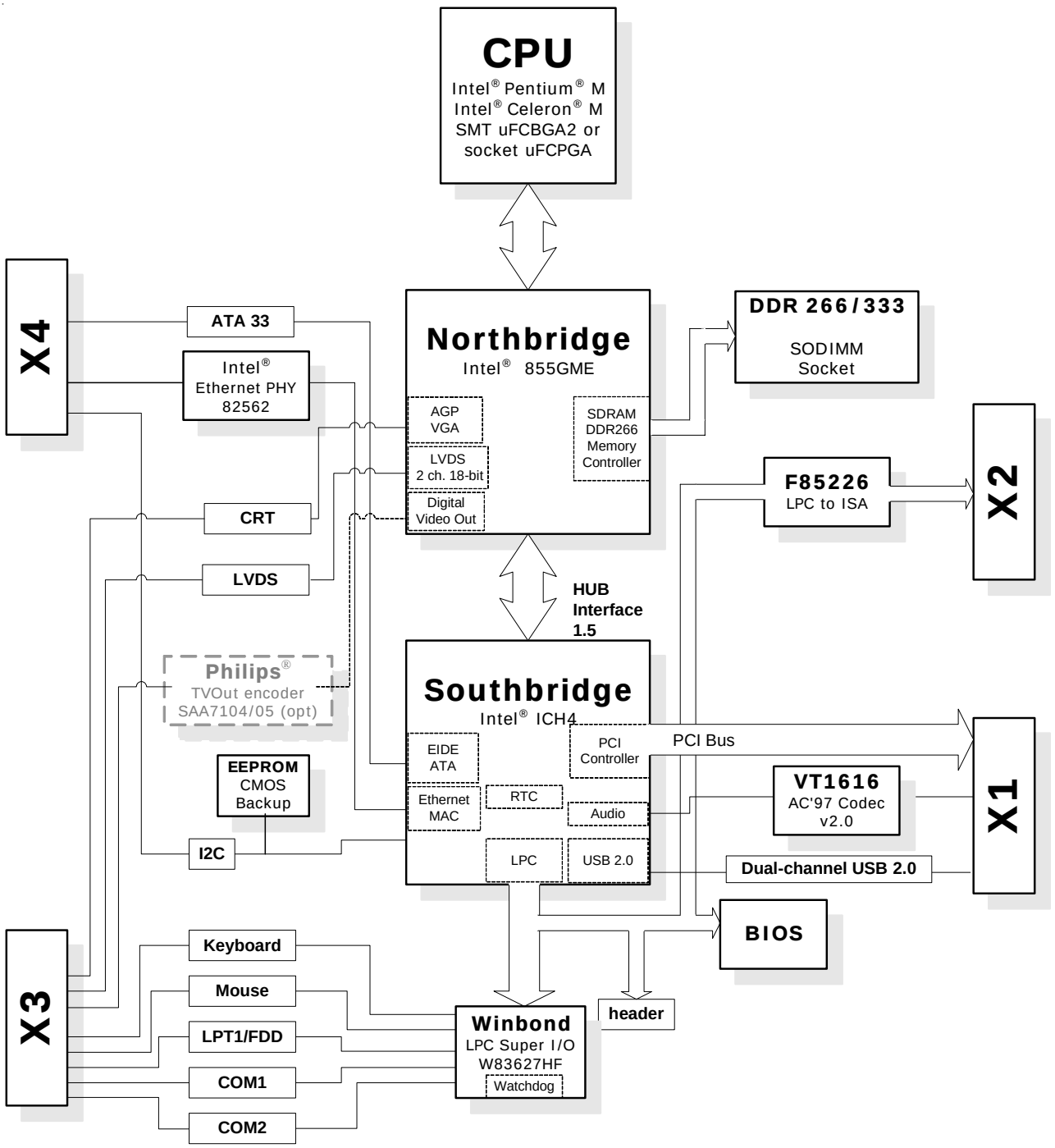
- Serial: two high speed RS-232C ports (COM1/COM2)
- Parallel: SPP, EPP and ECP modes
- FDD: not implemented (shared with parallel port)
- IrDA: supports SIR IrDA 1.1 compliant
- USB: supports up to four ports ver. 2.0 (ver 1.1 backward compatible)
- Keyboard & Mouse: one PS/2 keyboard and one PS/2 mouse

2.7 Mechanical and Environmental

- Power Requirement (+5 V only): 18 Watt typical; (uFCBGA Intel® Pentium® M 1.1 GHz with 512 MB DDR333)
- Operating Temperature: 0° to 55° C (32° to 140° F)
- Relative Humidity: up to 90% at 55° C
- ETX Board Dimensions: 95 mm x 114 mm (3.7" x 4.5")
- Weight: 87 grams

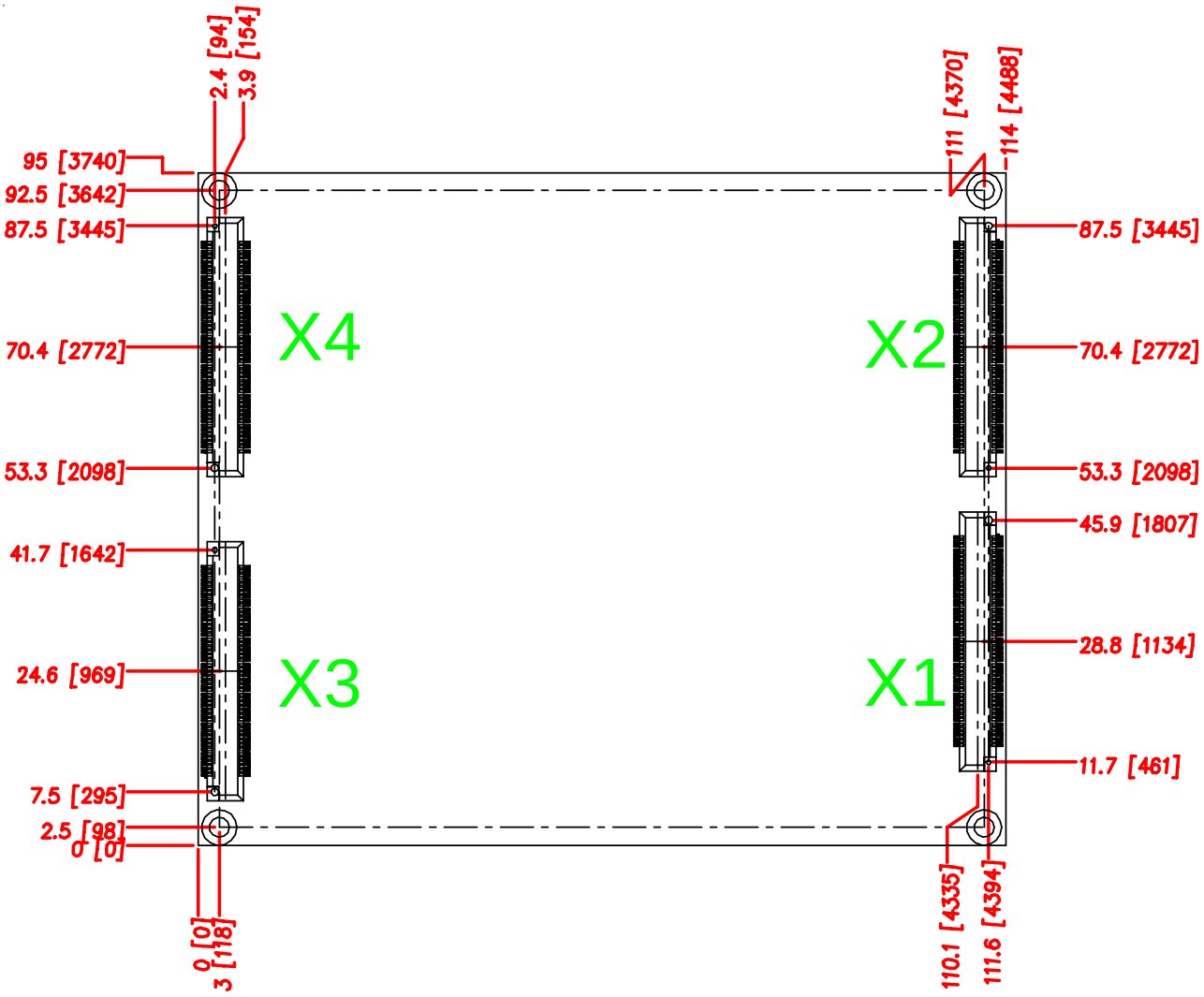
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3 Function Diagram



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4 Mechanical Dimensions



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5 Watchdog Timer



ETX-IM333 implements a watchdog timer (WDT) embedded in the LPC based Winbond 83627HF Super I/O controller.

The Watchdog timer consists of a one-second/minute resolution counter (CRF6 of logical device 8 of 83627HF) and two Watchdog control registers (CRF5 and CRF7 of logical device 8). Once a value is set in the WDT, the timer begins to count down.

Any movement in the keyboard, mouse, or software reset of the value will cause a reload of the timer value. The Watchdog output is connected to "reset". When the system hangs up without software re-trigger, the system will be reset.

The Watchdog timer has a one second granularity up to 255 seconds or a one minute granularity up to 255 minutes. The keyboard and mouse will only reset the WDT if Bit 7 and 6 of CRF7 is set; that is values greater than C0h or 192 decimal.

To configure the registers, the following sequence should be followed :

- 1. Writing 87h to location 4Eh twice to enter the extended function mode
- 2. Configure the registers to set up the WDT
- 3. Writing 0AAh to location 4Eh to exit the extended function mode

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The example program shown on the following pages resets the system after 15 seconds. Both keyboard and mouse interrupts will reload the WDT from CRF6.

```
begin :

;-----------------------------------------------------;
Enter the extend function mode, interrupt double-write
;-----------------------------------------------------

    mov     dx,4eh
    mov     al,87h
    out     dx,al
    out     dx,al
    mov     dx,4eh
    mov     al,2bh      ; CR2B,   bit4-> 0 = WDTO
                        ; bit4-> 1 = GP24
    out     dx,al
    mov     dx,4fh
    mov     al,0c0h
    out     dx,al

    mov     dx,4eh
    mov     al,07h
    out     dx,al
    mov     dx,4fh
    mov     al,08h      ;device 8
    out     dx,al

    mov     dx,4eh
    mov     al,30h
    out     dx,al
    mov     dx,4fh
    mov     al,01h      ;enable device 8
    out     dx,al

    mov     dx,4eh
    mov     al,07h
    out     dx,al
    mov     dx,4fh
    mov     al,08h      ;device 8
    out     dx,al

    mov     dx,4eh
    mov     al,0f7h
```

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```
    out     dx,al       ;device  8,CRF7
    mov     dx,4fh
    mov     al,0c0h
    out     dx,al

    mov     dx,4eh
    mov     al,07h
    out     dx,al
    mov     dx,4fh
    mov     al,08h
    out     dx,al           ;device  8

    mov     dx,4eh
    mov     al,0f5h             ;device  8,  CRF5
    out     dx,al
    mov     dx,4fh
    mov     al,00h          ;bit3  ->  0  =  second
                            ;bit3  ->  1  =  minute
    out     dx,al

    mov     dx,4eh
    mov     al,07h
    out     dx,al
    mov     dx,4fh
    mov     al,08h
    out     dx,al           ;device  8
    mov     dx,4eh
    mov     al,0f6h             ;device  8,  CRF6
    out     dx,al
    mov     dx,4fh
    mov     al,0fh
    out     dx,al

;-------------------------------------
;  Exit  extend  function  mode
;-------------------------------------

    mov     dx,4eh
    mov     al,0aah
    out     dx,al

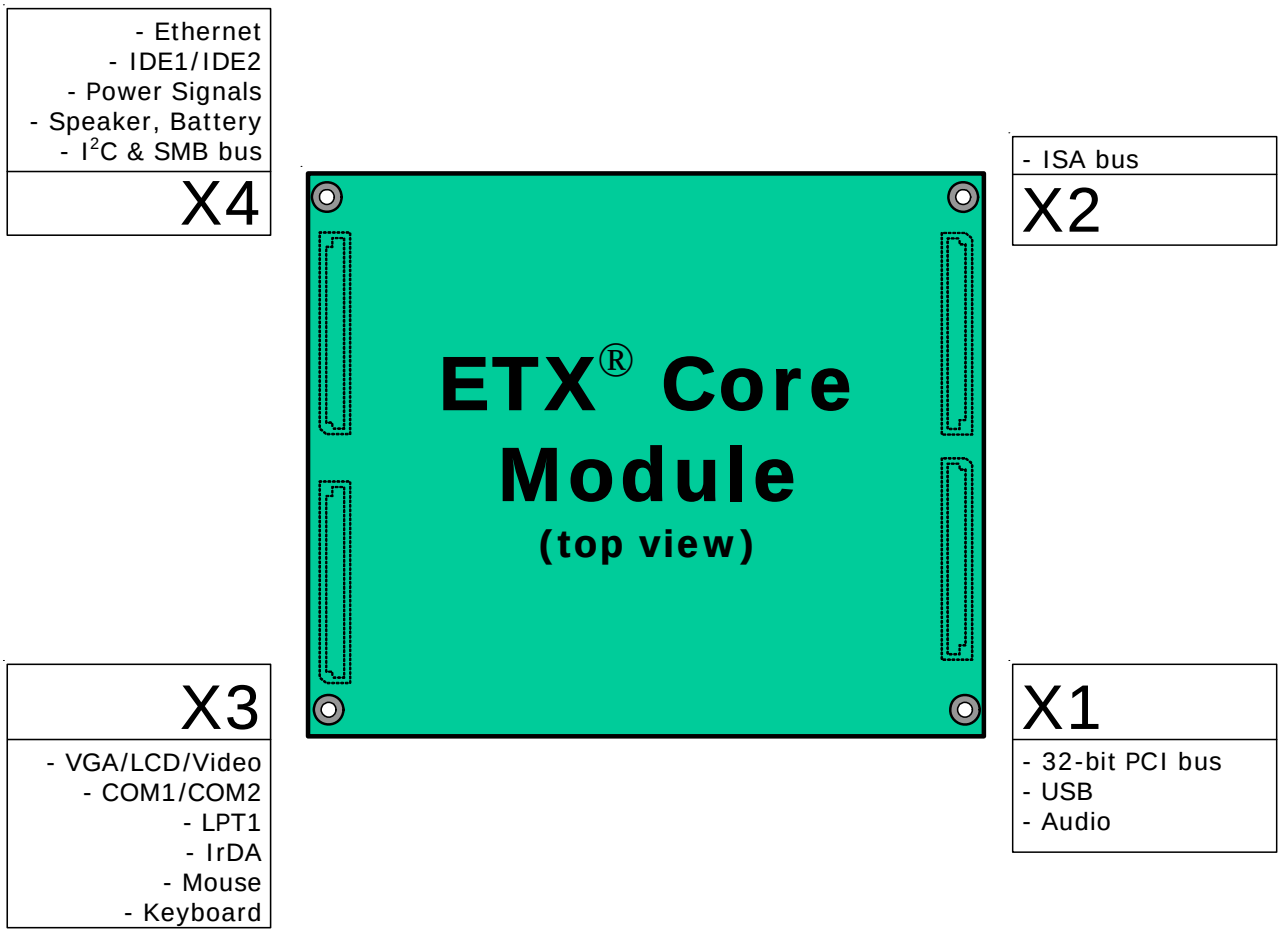
.exit

end
```

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6 Connectors

6.1 Connector Location



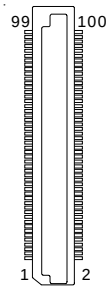
6.2 Pin Compatibility

All pins on X1, X2, X3, and X4 of the ETX-IM333 comply with pin and signal descriptions used in the original: “ETX® Specification ver. 2.6”. This document contains a description of pins, signal descriptions, and mechanical characteristics of the ETX® form factor.

An additional document, “ETX® Design Guide” gives a general introduction to carrier board designs for ETX® modules.

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6.3 X1 Connector: PCI-bus, USB, & Audio



Signals and Pins

Pin	Signal	Pin	Signal
1	GND	2	GND
3	PCICLK3	4	PCICLK4
5	GND	6	GND
7	PCICLK1	8	PCICLK2
9	REQ3#	10	GNT3#
11	GNT2#	12	3V[1]
13	REQ2#	14	GNT1#
15	REQ1#	16	3V[1]
17	GNT0#	18	RSV
19	5VCC	20	5VCC
21	SERIRQ	22	REQ0#
23	AD0	24	3V[1]
25	AD1	26	AD2
27	AD4	28	AD3
29	AD6	30	AD5
31	CBE0#	32	AD7
33	AD8	34	AD9
35	GND	36	GND
37	AD10	38	AUXAL
39	AD11	40	MIC
41	AD12	42	AUXAR
43	AD13	44	ASVCC
45	AD14	46	SDNL
47	AD15	48	ASSGND
49	CBE1#	50	SNDR

Pin	Signal	Pin	Signal
51	5VCC	52	5VCC
53	PAR	54	SERR#
55	GPERR	56	RSV
57	PME#	58	USB2-
59	LOCK#	60	DEVSEL#
61	TRDY#	62	USB3-
63	IRDY#	64	STOP#
65	FRAME#	66	USB2+
67	GND	68	GND
69	AD16	70	CBE2#
71	AD17	72	USB3+
73	AD19	74	AD18
75	AD20	76	USB0N
77	AD22	78	AD21
79	AD23	80	USB1-
81	AD24	82	CBE3#
83	5VCC	84	5VCC
85	AD25	86	AD26
87	AD28	88	USB0+
89	AD27	90	AD29
91	AD30	92	USB1+
93	PCIRST#	94	AD31
95	INTC#	96	INTD#
97	INTA#	98	INTB#
99	GND	100	GND

NOTE:

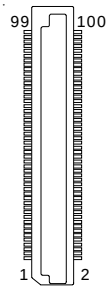
[1]The 3V (3.3 V ±5%) is generated onboard. Pins may be used to power devices on the carrier board up to a maximum load of 500 mA.

CAUTION:

DO NOT CONNECT THE 3V PIN TO AN EXTERNAL 3.3 V SUPPLY POWER

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6.4 X2 Connector: ISA Bus



Signals and Pins

Pin	Signal	Pin	Signal
1	GND	2	GND
3	SD14	4	SD15
5	SD13	6	MASTER#
7	SD12	8	DREQ7
9	SD11	10	DACK7#
11	SD10	12	DREQ6
13	SD9	14	DACK6#
15	SD8	16	DREQ5
17	MEMW#	18	DACK5#
19	MEMR#	20	DREQ0
21	LA17	22	DACK0#
23	LA18	24	IRQ14
25	LA19	26	IRQ15
27	LA20	28	IRQ12[1]
29	LA21	30	IRQ11
31	LA22	32	IRQ10
33	LA23	34	IO16#
35	GND	36	GND
37	SBHE#	38	M16#
39	SA0	40	OSC
41	SA1	42	BALE
43	SA2	44	TC
45	SA3	46	DACK2#
47	SA4	48	IRQ3
49	SA5	50	IRQ4

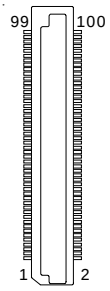
Pin	Signal	Pin	Signal
51	VCC	52	VCC
53	SA6	54	IRQ5
55	SA7	56	IRQ6
57	SA8	58	IRQ7
59	SA9	60	SYSCLK
61	SA10	62	REFSH#
63	SA11	64	DREQ1
65	SA12	66	DACK1#
67	GND	68	GND
69	SA13	70	DREQ3
71	SA14	72	DACK3#
73	SA15	74	IOR#
75	SA16	76	IOW#
77	SA18	78	SA17
79	SA19	80	SMEMR#
81	IOCHRDY	82	AEN
83	VCC	84	VCC
85	SD0	86	SMEMW#
87	SD2	88	SD1
89	SD3	90	NOWS#
91	DREQ2	92	SD4
93	SD5	94	IRQ9
95	SD6	96	SD7
97	IOCHK#	98	RSTDRV
99	GND	100	GND

NOTE:

[1]IRQ12 is reserved for a PS/2 mouse, this pin is not connected on ETX-IM333

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6.5 X3 Connector: CRT, LCD (LVDS), & Video



Signals and Pins

Pin	Signal	Pin	Signal
1	GND	2	GND
3	R	4	B
5	HSY	6	G
7	VSY	8	DDCK
9	NC	10	DDDA
11	LCD16	12	LCD18
13	LCD17	14	LCD19
15	GND	16	GND
17	LCD13	18	LCD15
19	LCD12	20	LCD14
21	GND	22	GND
23	LCD8	24	LCD11
25	LCD9	26	LCD10
27	GND	28	GND
29	LCD4	30	LCD7
31	LCD5	32	LCD6
33	GND	34	GND
35	LCD1	36	LCD3
37	LCD0	38	LCD2
39	5VCC	40	5VCC
41	NC	42	LTGO0
43	NC	44	BLON#
45	NC	46	DIGON
47	COMP	48	Y
49	SYNC[1]	50	C

First LVDS Channel

Signal	LVDS Signal
LCD0	Txout 0-
LCD1	Txout 0+
LCD2	Txout 1-
LCD3	Txout 1+
LCD4	Txout 2-
LCD5	Txout 2+
LCD6	Txclk -
LCD7	Txclk +
LCD8	Txout 3-
LCD9	Txout 3+

Second LVDS Channel

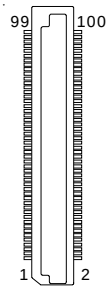
Signal	LVDS Signal
LCD10	Txout 0-
LCD11	Txout 0+
LCD12	Txout 1-
LCD13	Txout 1+
LCD14	Txout 2-
LCD15	Txout 2+
LCD16	Txclk -
LCD17	Txclk +
LCD18	Txout 3-
LCD19	Txout 3+

NOTE:

[1]TV-out signal for horizontal sync output or composite sync for RGB-SCART.

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6.6 X3 Connector: COM1/2, LPT1 or FDD, IrDA, Mouse, & Keyboard



Signals and Pins

LPT Mode

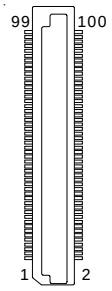
Pin	Signal	Pin	Signal
51	LPT/FLPY#	52	RESERVED
53	5VCC	54	GND
55	STB#	56	AFD#
57	RESERVED	58	PD7
59	IRRX	60	ERR#
61	IRTX	62	PD6
63	RXD2	64	INIT#
65	GND	66	GND
67	RTS2#	68	PD5
69	DTR2#	70	SLIN#
71	DCD2#	72	PD4
73	DSR2#	74	PD3
75	CTS2#	76	PD2
77	TXD2	78	PD1
79	RI2#	80	PD0
81	5VCC	82	5VCC
83	RXD1	84	ACK#
85	RTS1#	86	BUSY
87	DTR1#	88	PE
89	DCD1#	90	SLCT#
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND

FDD Mode

Pin	Signal	Pin	Signal
51	LPT/FLPY#	52	RESERVED
53	5VCC	54	GND
55	RESERVED	56	DENSEL
57	RESERVED	58	RESERVED
59	IRRX	60	HDSEL#
61	IRTX	62	RESERVED
63	RXD2	64	DIR#
65	GND	66	GND
67	RTS2#	68	RESERVED
69	DTR2#	70	STEP#
71	DCD2#	72	DSKCHG#
73	DSR2#	74	RDATA#
75	CTS2#	76	WP#
77	TXD2	78	TRK0#
79	RI2#	80	INDEX#
81	5VCC	82	5VCC
83	RXD1	84	DRV
85	RTS1#	86	MOT
87	DTR1#	88	WDATA#
89	DCD1#	90	WGATE#
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND

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6.7 X4 Connector: IDE1, IDE2, Ethernet, & Miscellaneous



Signals and Pins

Pin	Signal	Pin	Signal
1	GND	2	GND
3	5V_SB	4	PWGIN
5	PS_ON	6	SPEAKER
7	PWRBTN#	8	BATT
9	KBINH	10	LILED#
11	RSMRST#[1]	12	ACTLED#
13	ROMKBCS#[2]	14	SPDLED#
15	EXT_PRG[2]	16	I2CLK[3]
17	5VCC	18	5VCC
19	OVCR#	20	NC
21	EXTSMI#	22	I2DAT[3]
23	SMBCLK[3]	24	SMBDATA[3]
25	S_CS3#	26	SMBALRT#
27	S_CS1#	28	NC
29	S_A2	30	P_CS3#
31	S_A0	32	P_CS1#
33	GND	34	GND
35	PDIAG_S[4]	36	P_A2
37	S_A1	38	P_A0
39	S_INTRQ	40	P_A1
41	BATLOW#[2]	42	GPE1#[2]
43	S_AK#	44	P_INTRQ
45	S_RDY	46	P_AK#
47	S_IOR#	48	P_RDY
49	5VCC	50	5VCC

Pin	Signal	Pin	Signal
51	S_IOW#	52	P_IOR#
53	S_DRQ	54	P_IOW#
55	S_D15	56	P_DRQ
57	S_D0	58	P_D15
59	S_D14	60	P_D0
61	S_D1	62	P_D14
63	S_D13	64	P_D1
65	GND	66	GND
67	S_D2	68	P_D13
69	S_D12	70	P_D2
71	S_D3	72	P_D12
73	S_D11	74	P_D3
75	S_D4	76	P_D11
77	S_D10	78	P_D4
79	S_D5	80	P_D10
81	5VCC	82	5VCC
83	S_D9	84	P_D5
85	S_D6	86	P_D9
87	S_D8	88	P_D6
89	GPE2#[2]	90	CBLID_P#[4]
91	RXD#	92	P_D8
93	RXD	94	S_D7
95	TXD#	96	P_D7
97	TXD	98	HDRST#
99	GND	100	GND

NOTE:

[1]May be affected by external circuitry to reset the power management logic of the ETX module. Most designs do not use and pin is not connected.

[2]Reserved, do not connect

[3]See also: section 7.8 System Management Bus (I2C-compatible)

[4]Available, but not supported on the ETX-IM333

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7 System Resources

7.1 System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
(4 GB - 2 MB)	FFE00000 - FFFFFFFF	2 MB	High BIOS Area
(4 GB - 20 MB) - (4 GB - 19 MB-1) (4 GB - 18 MB) - (4 GB - 17 MB-1)	FEC00000 - FECFFFFF FEE00000 - FEEFFFFF	1 MB 1 MB	APIC Configuration Space
15 MB - 16 MB	F00000 - FFFFFF	1 MB	ISA Hole
960 KB - 1024 KB	F0000 - FFFFF	64 KB	System BIOS Area
896 KB - 960 KB	E0000 - EFFFF	64 KB	Extended System BIOS Area
768 KB - 896 KB	C0000 - DFFFF C0000 - CFFFF: D0000 - D7FFF: D0000 - DFFFF:	128 KB	PCI expansion ROM area[1] On-board VGA BIOS USB option ROM when plugging USB storage on system PXE option ROM when on-board LAN boot ROM is enabled.
640 KB - 768 KB	A0000 - BFFFF	128 KB	Video Buffer & SMM space
0 KB - 640 KB	00000 - 9FFFF	640 KB	DOS Area

NOTE: [1]After running PXE optional ROM, it will resize the range to D0000H - D3FFFH USB and PXE optional ROM can not be run at the same time

7.2 Direct Memory Access Channels

Channel Number	Data Width	System Resource
0	8-bits	Open
1	8-bits	Parallel port[1]
2	8-bits	Diskette drive[1]
3	8-bits	Parallel port[1]
4	-	Reserved - cascade channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

NOTE: [1] DMA channel 1 and 3 are selected when using parallel port. Floppy and parallel port can not be used at the same time

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7.3 I/O Address Map

Address	Size	Description
0000 - 001F	32 bytes	DMA controller
0020 - 0021	2 bytes	Interrupt controller
0024 - 0025	2 bytes	Interrupt controller
0028 - 0029	2 bytes	Interrupt controller
002C - 002D	2 bytes	Interrupt controller
002E - 002F	2 bytes	LPC SIO
0030 - 0031	2 bytes	Interrupt controller
0034 - 0035	2 bytes	Interrupt controller
0038 - 0039	2 bytes	Interrupt controller
003C - 003D	2 bytes	Interrupt controller
0040 - 0043	4 bytes	Counter/Timer
0048 - 004B	4 bytes	Counter/Timer
004E - 004F	2 bytes	LPC SIO configuration port (on-board SIO)
0050 - 0053	4 bytes	Counter/Timer
0060	1 byte	Keyboard controller
0061	1 byte	NMI, speaker control
0063	1 byte	NMI controller
0064	1 byte	Keyboard controller
0065	1 byte	NMI controller
0067	1 byte	NMI controller
0070 - 0071	2 bytes	Real time clock controller
0072 - 0073	2 bytes	Real time clock controller
0074 - 0075	2 bytes	Real time clock controller
0076 - 0077	2 bytes	Real time clock controller
0080 - 0091	18 bytes	DMA controller
0092	1 byte	Reset generator
0093 - 009F	13 bytes	DMA controller
00A0 - 00A1	2 bytes	Interrupt controller
00A4 - 00A5	2 bytes	Interrupt controller
00A8 - 00A9	2 bytes	Interrupt controller
00AC - 00AD	2 bytes	Interrupt controller
00B0 - 00B1	2 bytes	Interrupt controller
00B2 - 00B3	2 bytes	Power Management
00B4 - 00B5	2 bytes	Interrupt controller
00B8 - 00B9	2 bytes	Interrupt controller
00BC - 00BD	2 bytes	Interrupt controller
00C0 - 00DF	32 bytes	DMA controller
00F0 - 00FF	16 bytes	Numeric processor
0170 - 0177	8 bytes	Secondary IDE controller
01F0 - 01F7	8 bytes	Primary IDE controller
0274 - 0277	4 bytes	ISA PnP read port
0278 - 027F	8 bytes	LPT2
0294 - 0297	4 bytes	On-board Sensor index/data port

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02E8 - 02EF	8 bytes	COM4/Video
02F8 - 02FF	8 bytes	COM2
0376 - 0377	2 bytes	Secondary IDE controller
0378 - 037F	8 bytes	LPT1
03B0 - 03BB	12 bytes	Video (monochrome)
03BC - 03BF	4 bytes	LPT3
03C0 - 03DF	32 bytes	Video (VGA)
03E8 - 03EF	8 bytes	COM3
03F0 - 03F5, 03F7	7 bytes	Diskette controller
03F6 - 03F7	2 bytes	Primary IDE controller
03F8 - 03FF	8 bytes	COM1
0400 - 04BF	182 bytes	ACPI & GPIO control registers
04D0 - 04D1	2 bytes	Edge/level triggered PIC
0500 - 051F	32 bytes	On-board SMbus control registers
0CF8 - 0CFF*	8 bytes	PCI configuration registers
0CF9**	1 byte	Reset control register
0B000 - 0B03F***	64 bytes	On-board Ethernet control registers
0C000 - 0C001F***	32 bytes	Control registers of on-board USB controllers
0C400 - 0C401F***	32 bytes	
0C800 - 0C801F***	32 bytes	
0CC00 - 0CC07***	8 bytes	On-board graphic controller configuration registry
0F000 - 0F00F***	16 bytes	On-board IDE controller configuration registry



*DWORD access only
**Byte access only
***I/O ports may vary depending on PCI configuration

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7.4 Interrupt Request (IRQ) Lines

PIC Mode

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
0	Counter 0	N/A	No
1	Keyboard controller	N/A	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 2 (COM2)/PCI/ISA	IRQ3 via SERIRQ, IRQ3 at ISA bus	Note 1
4	Serial Port 1 (COM1)/PCI/ISA	IRQ4 via SERIRQ, IRQ4 at ISA bus	Note 1
5	Parallel Port 2 (LPT2)/PCI/ISA	IRQ5 via SERIRQ, IRQ5 at ISA bus	Note 1
6	Floppy Drive Controller	IRQ6 via SERIRQ	No
7	Parallel Port 1 (LPT1)/PCI/ISA	IRQ7 via SERIRQ, IRQ7 at ISA bus	Note 1
8	Real-time clock	N/A	No
9	SCI / PCI	IRQ9 via SERIRQ, IRQ9 at ISA bus	Notes 1 & 2
10	PCI / ISA	IRQ10 via SERIRQ, IRQ10 at ISA bus	Note 1
11	PCI / ISA	IRQ11 via SERIRQ, IRQ11 at ISA bus	Note 1
12	PS/2 Mouse / PCI / ISA	IRQ12 via SERIRQ, IRQ12 at ISA bus	Note 1
13	Math Processor	N/A	No
14	Primary IDE controller / PCI / ISA	IRQ14 via SERIRQ, IRQ14 at ISA bus	Note 1
15	Secondary IDE controller / PCI / ISA	IRQ15 via SERIRQ, IRQ15 at ISA bus	Note 1



[1]These IRQs may be used by PCI devices when designated on-board device s are disabled. If the IRQ is to be used on the ISA bus, then the IRQ must be assigned to ISA in the BIOS setup menu.

[2]BIOS does not support IRQ 9 on the ISA bus.

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APIC Mode

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
0	Counter 0	N/A	No
1	Keyboard controller	N/A	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 2 (COM2) / PCI / ISA	IRQ3 via SERIRQ, IRQ3 at ISA bus	Note 1
4	Serial Port 1 (COM1) / PCI / ISA	IRQ4 via SERIRQ, IRQ4 at ISA bus	Note 1
5	Parallel Port 2 (LPT2) / PCI / ISA	IRQ5 via SERIRQ, IRQ5 at ISA bus	Note 1
6	Floppy Drive Controller	IRQ6 via SERIRQ	No
7	Parallel Port 1 (LPT1) / PCI / ISA	IRQ7 via SERIRQ, IRQ7 at ISA bus	Note 1
8	Real-time clock	N/A	No
9	SCI / PCI	IRQ9 via SERIRQ, IRQ9 at ISA bus	Notes 1 & 2
10	PCI / ISA	IRQ10 via SERIRQ, IRQ10 at ISA bus	Note 1
11	PCI / ISA	IRQ11 via SERIRQ, IRQ11 at ISA bus	Note 1
12	PS/2 Mouse / PCI / ISA	IRQ12 via SERIRQ, IRQ12 at ISA bus	Note 1
13	Math Processor	N/A	No
14	Primary IDE controller / PCI / ISA	IRQ14 via SERIRQ, IRQ14 at ISA bus	Note 1
15	Secondary IDE controller / PCI / ISA	IRQ15 via SERIRQ, IRQ15 at ISA bus	Note 1
16	N/A	PCI Slot INT A, USB1, VGA controller	Yes
17	N/A	PCI Slot INT B, SMBus, AC97 Audio	Yes
18	N/A	PCI Slot INT C, USB3	Yes
19	N/A	PCI Slot INT D, USB2	Yes
20	N/A	On-board LAN controller	No
21	N/A		No
22	N/A		No
23	N/A	EHCI	No

NOTE:

[1]These IRQs may be used by PCI devices when designated on-board devices are disabled. If the IRQ is to be used on the ISA bus then the IRQ must be assigned to ISA in the BIOS setup menu.

[2]BIOS does not support IRQ 9 on the ISA bus.

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7.5 PCI Configuration Space Map

Bus Number	Device Number	Function Number	Routing	Description
00h	00h	00h	N/A	Intel® 855 GM/GME GMCH Host-Hub Interface Bridge
00h	00h	01h	N/A	Intel® 855 GM/GME GMCH Main Memory Controller
00h	00h	03h	N/A	Intel® 855 GM/GME GMCH Configuration Process Controller
00h	02h	00h	Internal	Intel® Integrated Graphics Device
00h	02h	01h	Internal	Intel® Integrated Graphics Device (Function 1)
00h	1Dh	00h	Internal	Intel® USB UHCI Controller 1
00h	1Dh	01h	Internal	Intel® USB UHCI Controller 2
00h	1Dh	02h	Internal	Intel® USB UHCI Controller 3
00h	1Dh	07h	Internal	Intel® USB EHCI Controller
00h	1Eh	00h	N/A	Intel® Hub Interface to PCI Bridge
00h	1Fh	00h	N/A	Intel® LPC Interface Bridge
00h	1Fh	01h	Internal	Intel® IDE Controller
00h	1Fh	03h	Internal	Intel® SMBus Controller
00h	1Fh	05h	Internal	Intel® AC'97 Audio Controller
01h	08h	00h	Internal	Intel® LAN controller
01h	03h	00h	PIRQA-PIRQD	External PCI Slot 1
01h	04h	00h	PIRQA-PIRQD	External PCI Slot 2
01h	05h	00h	PIRQA-PIRQD	External PCI Slot 3
01h	06h	00h	PIRQA-PIRQD	External PCI Slot 4

7.6 PCI Bus Arbitration Assignment

PCI Bus Request	PCI Master(s)	IDSEL
Request 0	Routed to ETX® connector X1	*
Request 1	Routed to ETX® connector X1	*
Request 2	Routed to ETX® connector X1	*
Request 3	Routed to ETX® connector X1	*

NOTE: IDSEL routing depends on carrier board design.

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7.7 PCI Interrupt Routing Map

PIRQ	INT Line	VGA	UHCI 1	UHCI 2	UHCI 3	EHCI	IDE Native	SMBus	AC'97	PCI Slot 1	PCI Slot 2	PCI Slot 3	PCI Slot 4	LAN
A	INTA	X	X							INTA	INTD	INTC	INTB	
B	INTB							X	X	INTB	INTA	INTD	INTC	
C	INTC				X		X			INTC	INTB	INTA	INTD	
D	INTD			X						INTD	INTC	INTB	INTA	
E														X
F														
G														
H						X								

7.8 System Management Bus (I²C-compatible)

Internally the SMB bus and I2C bus are one and the same. The ICH4 Southbridge supports SMBDAT and SMBCLK lines that are I2C-compatible.

The X4 connector has pins for both the I2C and SMB bus. Both are connected to the same internal bus: the SMB bus. It is advisable to always connect external I2C devices to the I2C pins and SMB devices to the SMB pins to ensure compatibility with other modules that might support two internal busses (a separate I2C and SMB bus).

Address	Function	Device
A0h	Identification Information	SODIMM0 EEPROM
AEh	CMOS setting backup	EEPROM
D2h	Timing	Clock generator
0Fh	SMbus Master	ICH4

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8 Phoenix Award BIOS

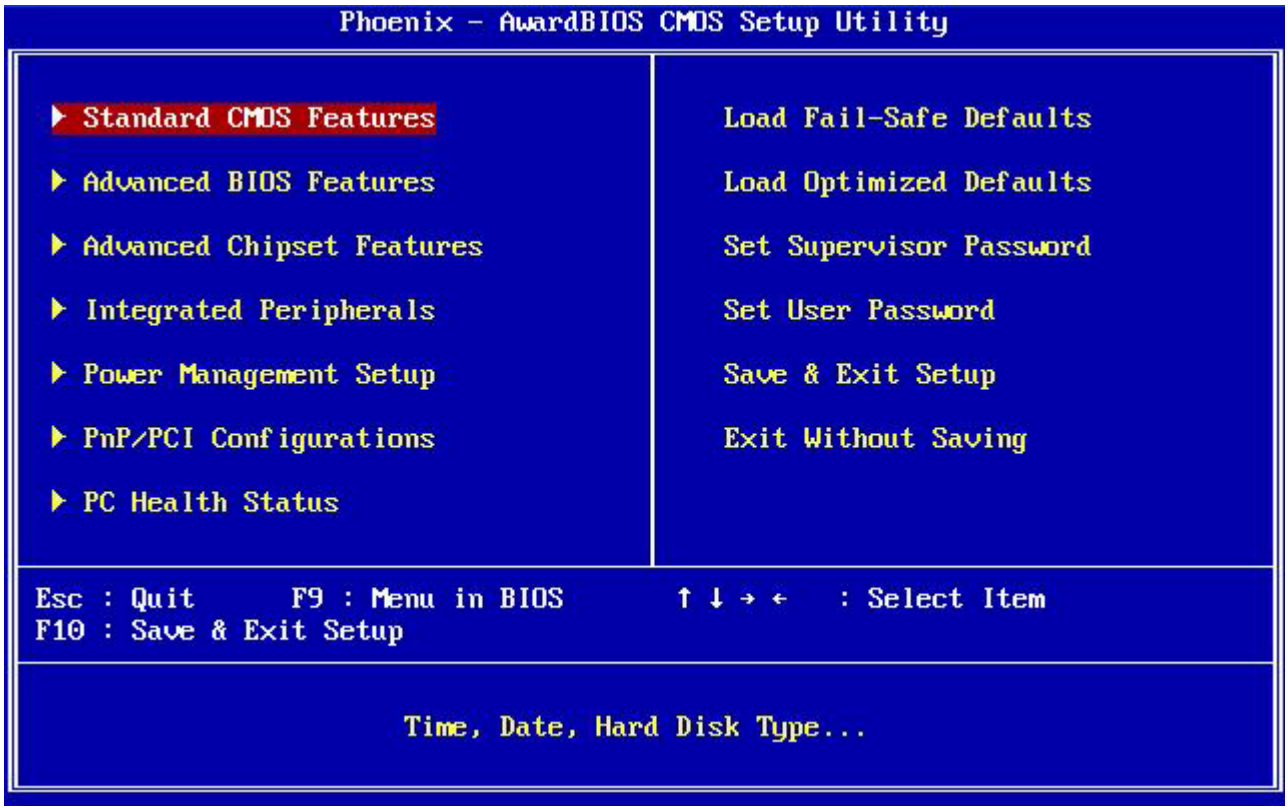
8.1 Description

The module uses a Phoenix Award PCI/ISA BIOS ver 6.0 for system configuration. The Award BIOS setup program is designed to provide maximum flexibility in configuring the system by offering various selectable options to meet end-user requirements. This chapter is written to assist you in the proper usage of these features.

To access the Phoenix AWARD PCI/ISA BIOS Setup program, during initial system power up;

```
Press <Del> key
```

The Main Menu will be displayed.



8.2 Main Menu Setup Items

The main menu includes the following setup categories. Recall that some systems may not include all entries.

Standard CMOS Features (see section 8.3)

Sets basic system configuration.

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Advanced BIOS Features (see section 8.4)

Sets advanced features available on the system.

Advanced Chipset Features (see section 8.5)

Changes values in the chipset registers and optimizes system performance.

Integrated Peripherals (see section 8.6)

Specifies settings for integrated peripherals.

Power Management Setup (see section 8.7)

Specifies settings for power management.

PnP/PCI Configuration (see section 8.8)

Specifies settings for PnP/PCI. (Only applicable if your system supports PnP/PCI)

PC Health Status (see section 8.9)

Monitors CPU and system temperatures.

Frequency/Voltage Control

Specifies frequency/voltage control settings.

Load Fail-Safe Defaults

Loads the BIOS default values for the minimal/stable performance for your system to operate.

Load Optimized Defaults

Loads BIOS default values (factory settings) for optimal system performance.

Supervisor/User Password

Sets User and Supervisor Passwords.

Save & Exit Setup

Saves CMOS value changes to CMOS and exits setup.

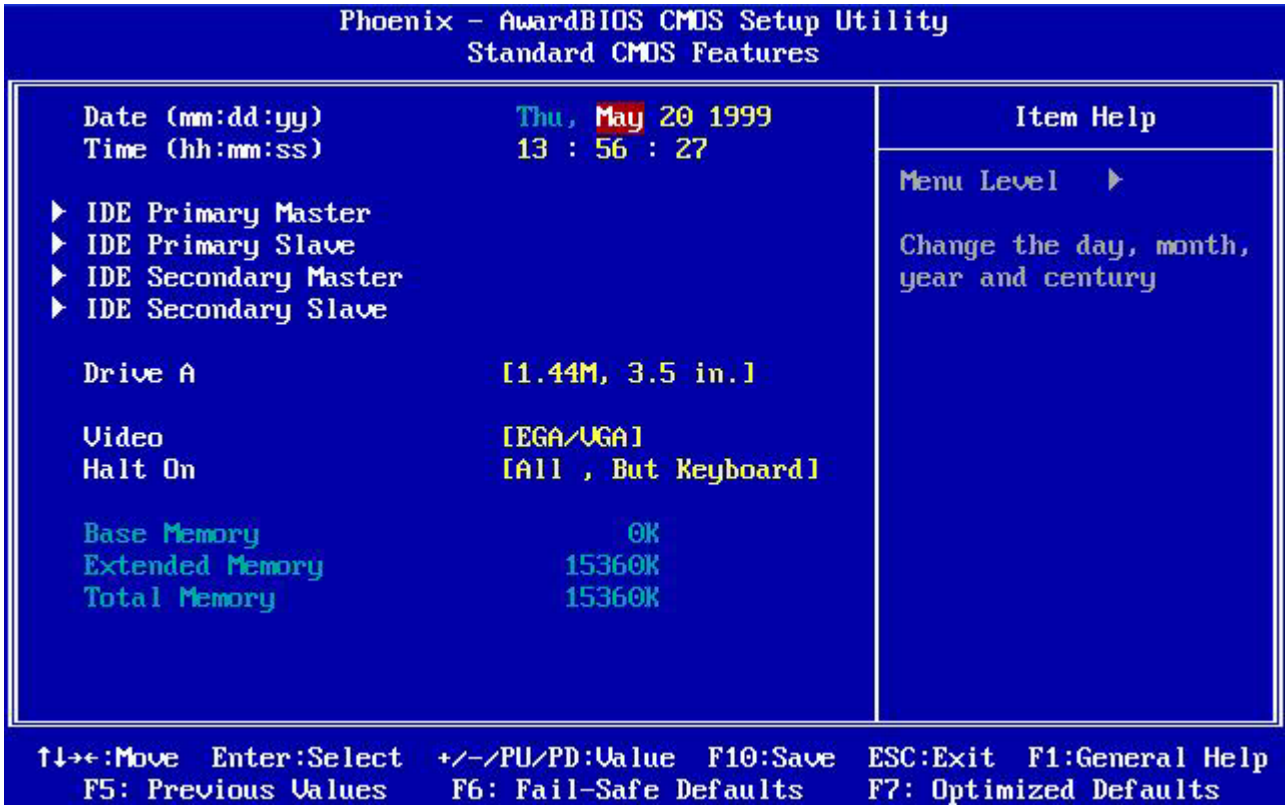
Exit Without Saving

Abandons all CMOS value changes and exits setup.

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8.3 Standard CMOS Features

The main menu includes the following setup categories. Recall that some systems may not include all entries.



Date

The BIOS determines the day of the week from other date information.

Time

The time format is based on the 24-hour military-time clock. For example, 1 P.M. is 13:00:00. Press the LEFT arrow key "«" or (appropriate key to move to the desired field). Press the PgUp or PgDn key to increment the setting, or type the desired value directly into the field.

IDE Primary and Secondary Master/Slave Items

This selection brings up a configuration menu of the designated Drive (see next page)

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Drive A

The ETX-IM333 can support one single FDD drive. Because FDD and LPT1 share the same pins on the X3 connector, only one of them can be used at a time. LPT1 or FDD can be enabled in the following BIOS menu:

▶ Integrated Peripherals ▶ Super I/O Device ▶ LPT1 Setting/FDD

Allows enabling/disabling of LPT1 resources or switching to FDD mode. After enabling the FDD, select the correct specifications for the diskette drive:

None: No diskette drive installed

360 KB: 5.25 inch PC-type standard drive

1.2 MB: 5.25 inch AT-type high-density drive

720 KB: 3.5 inch double-sided drive

1.44 MB: 3.5 inch double-sided drive

2.88 MB: 3.5 inch double-sided drive IDE Primary and Secondary Master/Slave Items

Video

Selects the type of primary video subsystem in your computer. The BIOS usually detects the correct video type automatically. The BIOS supports a secondary video subsystem, but is not selected in Setup.

Halt On

During the Power On Self Test (POST), the computer stops if the BIOS detects a hardware error. The BIOS can be instructed to ignore certain errors during POST and continue the bootup process. The options are as follows:

No errors: POST does not stop for any errors.

All errors: POST stops for any nonfatal error and will prompt the user to take any corrective measures.

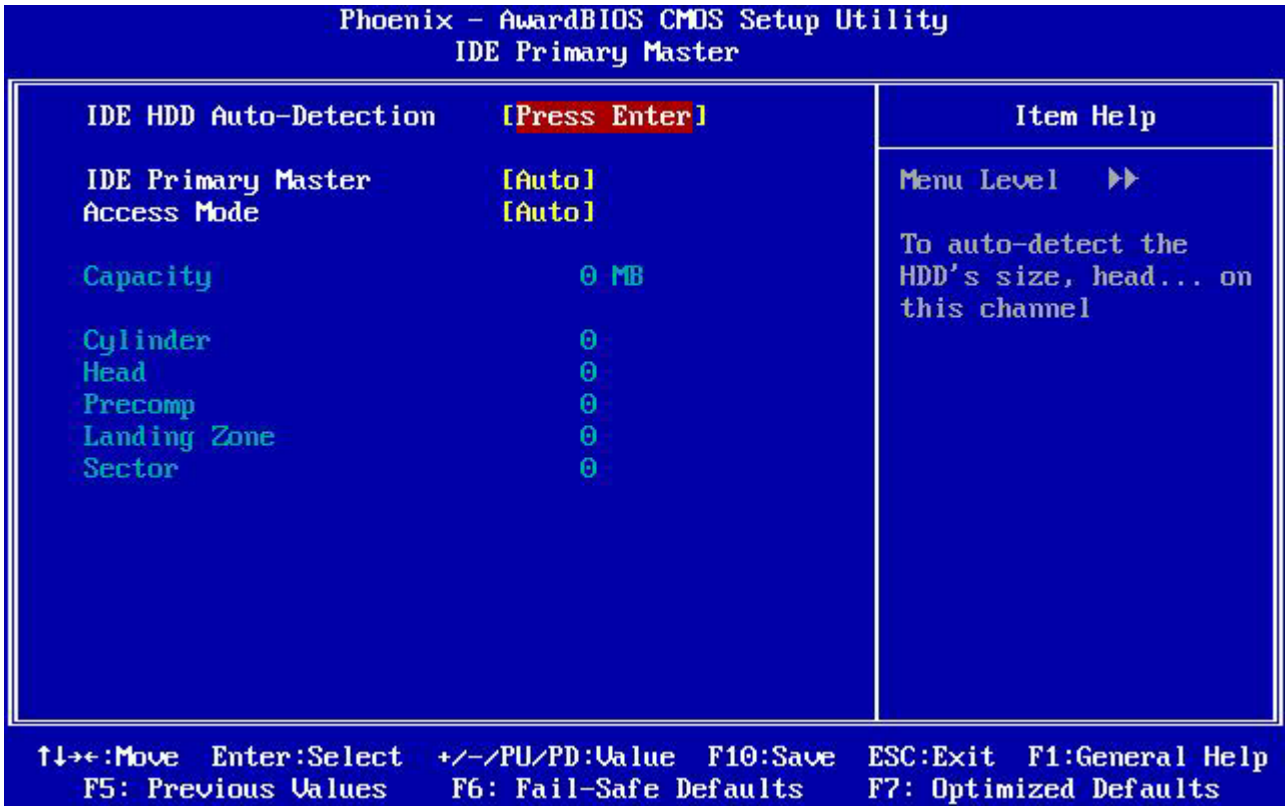
All, But Keyboard: POST does not stop for a keyboard error, but stops for all other errors.

All, But Diskette: POST does not stop for diskette drive errors, but stops for all other errors.

All, But Disk/Key: POST does not stop for a keyboard or disk errors, but stops for all other errors.

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IDE Primary and Secondary Master/Slave Items



IDE HDD Auto-detection:	Press Enter	Press Enter to auto-detect the HDD on this channel. If detection is successful, it fills the remaining fields on this menu.
IDE Primary Master:	None/Auto/Manual	Selecting 'manual' allows the user to set the remaining fields on this screen. Selects the type of fixed disk. "User Type" will let you select the number of cylinders, heads, etc.

NOTE: PRECOMP=65535 means NONE.

Capacity:	Auto display disk size	Disk drive capacity (approximated).

NOTE: Disk size is usually slightly greater than the size of a formatted disk given by a disk checking program.

Access Mode:	CHS/LBA/Large/Auto	Selects the access mode for a hard disk

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The following options are selectable only if the 'IDE Primary Master' item is set to 'Manual'

Cylinder:	Min = 0 Max = 65535	Sets the number of cylinders for a hard disk.
Head:	Min = 0 Max = 255	Sets the number of read/write heads
Precomp:	Min = 0 Max = 65535	



Setting a value of 65535 means no hard disk

Landing zone: Min = 0 Max = 65535



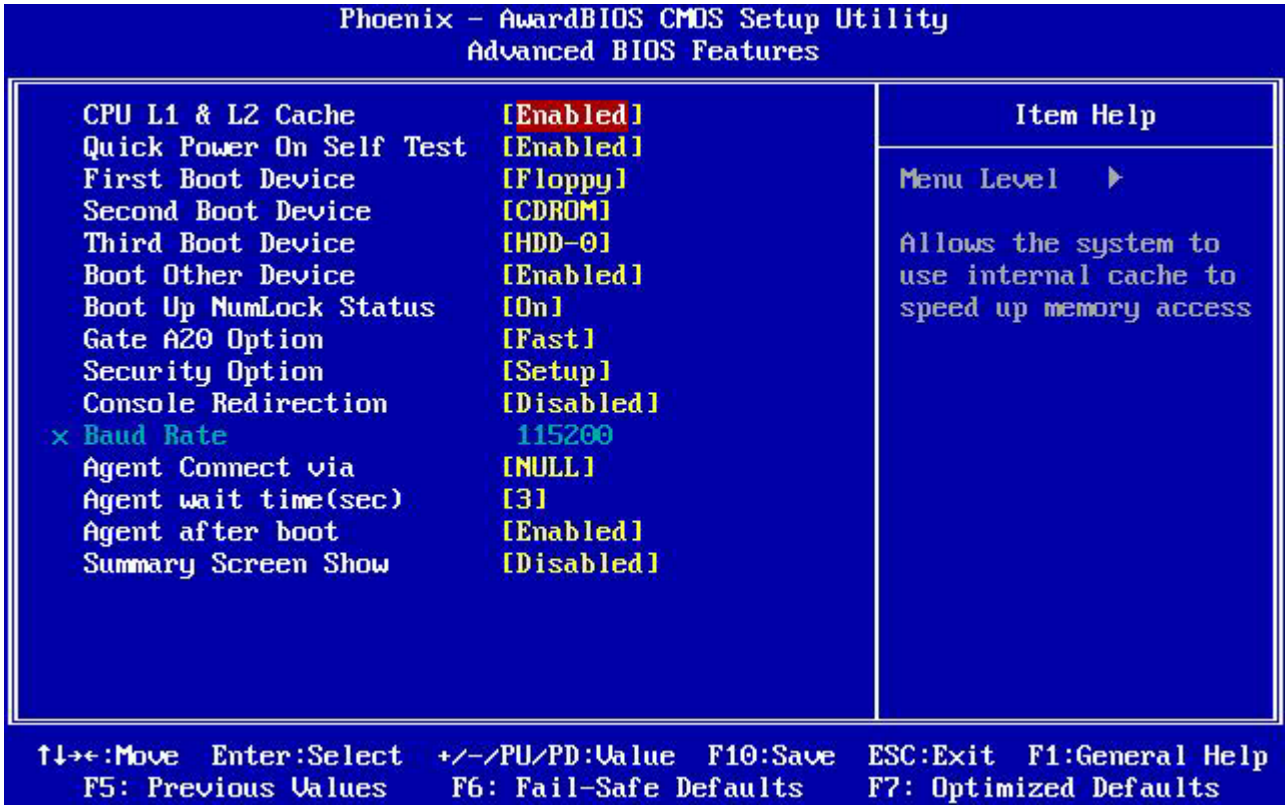
Setting a value of 65535 means no hard disk

Sector: Min = 0 Max = 255 Number of sectors per track

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8.4 Advanced BIOS Features

This section allows users to configure the system for basic operation. The following features can be selected: system default speed, bootup sequence, keyboard operation, shadowing, security, CPU internal cache, and CPU external cache.



CPU L1 & L2 Cache

Enables/disables CPU L1 and L2 Cache. Options: Enabled/Disabled

Quick Power On Self Test

Speeds up the Power On Self Test (POST). If enabled, BIOS will shorten or skip some check items during POST (default setting: Disabled). Options: Enabled/Disabled

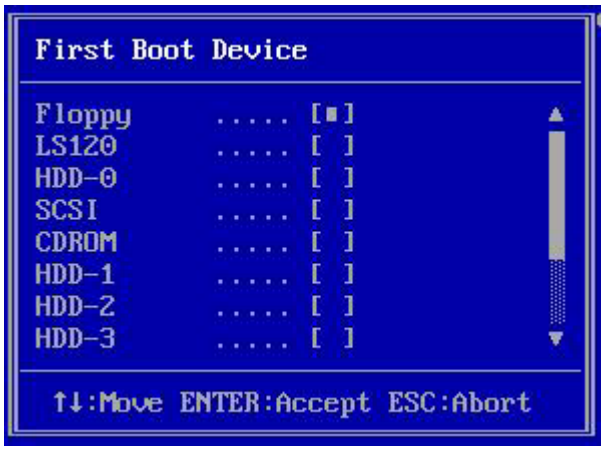
First/Second/Third Boot Device

Pressing “Enter” brings up the Boot Device Menu. The BIOS attempts to load the operating system from the selected device (see menu for options).

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Boot Other Device

Enables the BIOS to boot from a second or third device if booting from first device fails. When disabled the BIOS will not attempt booting from alternative devices:
Options: Enabled/Disabled



Boot-Up NumLock Status

Selects power on state for NumLock.
Options: On/Off

Gate A20 Option

Selects if chipset or keyboard controller should control Gate A20.
Normal: A keyboard controller pin controls Gate A20
Fast: Chipset controls Gate A20

Security Option

Selects whether a password is required every time the system boots or only when setup is entered.
Options:

System: The system will not boot and access to Setup will be denied if an incorrect password is entered at the prompt.

Setup : The system will boot, but access to Setup will be denied if an incorrect password is not entered at the prompt.

To disable security, select PASSWORD SETTINGS in Main Menu. The user will then be prompted to enter the password. To disable security, DO NOT type anything, only press <Enter>. Once security is disabled, the system will boot and setup can be entered freely.

Console Redirection

Allows remote access by another computer to get POST messages and order commands through serial port access.

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Baud Rate

When using console redirection, the serial port baud rate settings must be synchronized between target and monitoring computer.



An error message, “Award Preboot Agent Installation Failed” will display if the BIOS cannot properly connect the two computers.

Agent Connect via...

A non-selectable item. Only supports NULL mode. NULL mode allows users to connect two computers via a null modem cable to achieve a direct connection.

Agent Wait Time (sec)

Allows users to select the wait time to detect a successful connection.

Agent After Boot

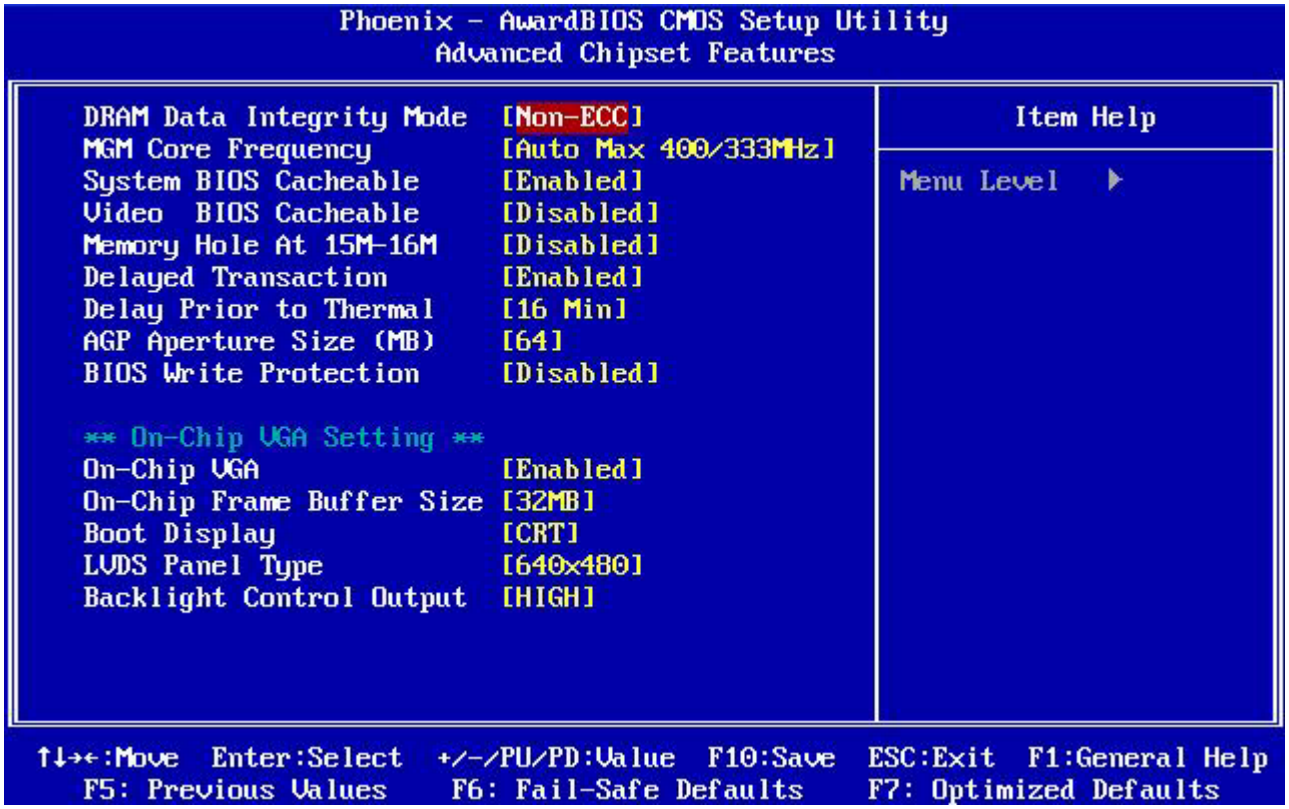
Allows users to monitor and control text-based applications such as DOS after POST.

Summary Screen Show

Suppresses the summary screen. Options: Enable/Disable

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8.5 Advanced Chipset Features



DRAM Data Integrity Mode

ECC (Error Checking and Correction) enables the memory controller to detect and correct single-bit soft memory errors. The memory controller will also be able to detect double-bit errors though it will not be able to correct them. This provides increased data integrity and system stability (available only with special ECC memory modules).

NOTE: Display may flicker when integrated graphics and ECC support are enabled.

Memory with ECC enabled requires more system memory resources. This will cause the integrated graphics engine to have less memory bandwidth for access to the graphics frame buffer. Display flicker and flashing may occur when ECC is enabled under high-resolution graphics modes.

MGM Core Frequency

Selects FSB Speed/Memory Speed/GFX Low/GFX high core frequency (default setting: Auto Max 266 MHz)

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System BIOS Cacheable

Enables caching of the system BIOS ROM at F0000h-FFFFFh, resulting in better system performance.



If a program writes to this memory area, a system error may result.

Video BIOS Cacheable

Enables caching of video RAM, resulting in better system performance. Options: Enabled/ Disabled.



If a program writes to this memory area, a system error may result.

Delayed Transaction

The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. If enabled this feature supports compliance with PCI specification version 2.1.

Delay Prior to Thermal

When the Thermal Monitor is in automatic mode and the thermal sensor detects that the processor has reached its maximum safe operating temperature, it will activate the Thermal Control Circuit (TCC). The TCC will then modulate the clock cycles by inserting null cycles, typically at a rate of 50 to 70% of the total number of clock cycles. This results in the processor "resting" 50 to 70% of the time.

As the die temperature drops, the TCC will gradually reduce the number of null cycles until no more are required to keep the die temperature below the safe point. The thermal sensor then turns the TCC off. This mechanism allows the processor to dynamically adjust its duty cycles to ensure its die temperature remains within safe limits.

The Delay Prior To Thermal BIOS feature controls the activation of the Thermal Monitor's automatic mode. It allows the user to determine when the CPU's Thermal Monitor should be activated in automatic mode after the system boots. For example, with the default value of 16 minutes, the BIOS activates the Thermal Monitor in automatic mode 16 minutes after the system starts booting up.

Generally, the Thermal Monitor should not be activated immediately on booting as the

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processor will be under heavy load during the booting process. This causes a sharp rise in die temperature from its cold state. Because it takes time for the thermal output to radiate from the die to the heat sink, the thermal sensor will register the sudden spike in die temperature and prematurely activate the TCC. This unnecessarily reduces the processor's performance during the bootup process.

Therefore, to ensure optimal booting performance, the activation of the Thermal Monitor must be delayed for a set period of time.

It is recommended that this BIOS feature is set to the lowest value (in minutes) that exceeds the time it takes to fully boot up the system. For example, if it takes 5 minutes to fully boot up system, selecting 8 minutes is preferable.

You should not select a delay value that is unnecessarily long. Without the Thermal Monitor, the processor may heat up to a critical temperature (approximately 135° C), at which point the thermal sensor shuts down the processor by removing the core voltage within 0.5 seconds.

AGP Aperture Size (MB)

Selects the size of the Accelerated Graphics Port (AGP) aperture. The aperture is a portion of the PCI memory address range dedicated for graphics memory address space. Host cycles that reach the aperture range are forwarded to the AGP without any translation (default setting: 64 MB).
Options: 4 MB, 8 MB, 16 MB, 32 MB, 65 MB, 128 MB, and 256 MB.

BIOS Write Protection

A security feature that prohibits the user from writing data to the BIOS (default setting: Disabled)
Options: Enabled/Disabled

Onchip VGA

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Enables/disables the integrated VGA core (default setting: Enabled).

Onchip Framebuffer Size

Configures how much system memory to allocate to the integrated GPU. The amount allocated to the GPU is deducted from the amount of system memory available to the operating system and programs.

For example: a resolution of 1600 x 1200 and color depth of 32-bit,
amounts to 1600 x 1200 x 32-bits = 61,440,000-bits or 7.68 MB.
Under these conditions, the memory should be set to 8 MB.

Display Feature

Allows user to configure the type of external display used.
Options: CRT/LVDS+CRT/TV



Displays can not be used concurrently. TV option only for ETX-IM333 with on-board TV out.

LVDS Panel Display

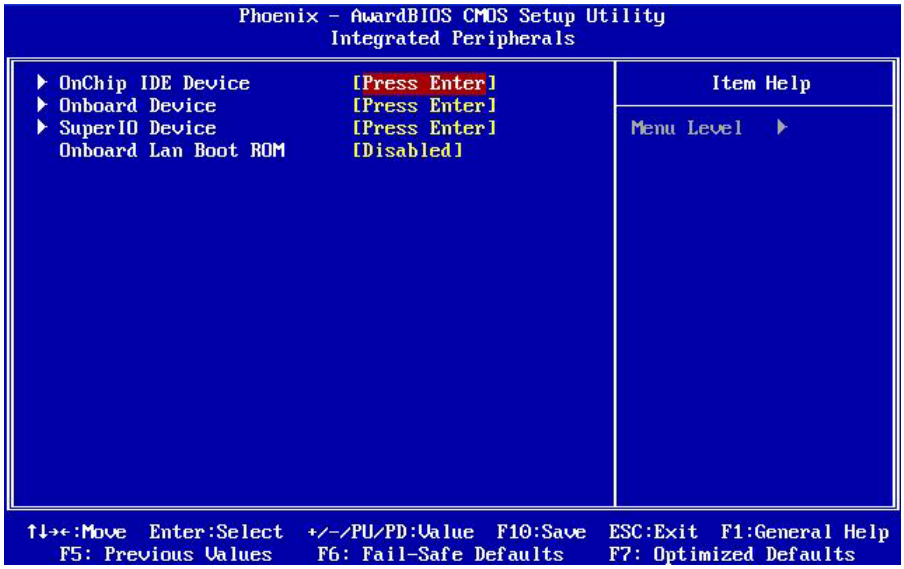
Enables flat panel resolution selection of LVDS Displays.
Options: 640 x 480, 800 x 600, 1024 x 768, and 1280 x 1024.

Backlight Control Output

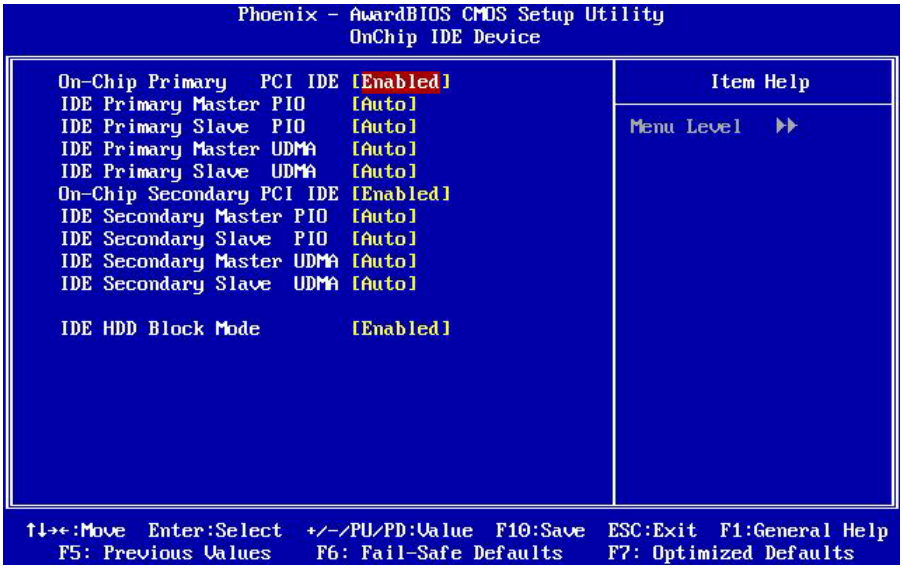
Allows the users to configure the state of the BLON# before initializing the graphics controller. This selection is only for earlier ETX-IM333 versions. The backlight is fully controlled by hardware on ETX-IM333 versions later than C2` .

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8.6 Integrated Peripherals



OnChip IDE Device (submenu)



OnChip Primary/Secondary PCI IDE

The chipset contains a PCI IDE interface with support for two IDE channels. Select Enabled to activate the primary/secondary IDE interface. Select Disabled to deactivate these interfaces.

Primary & Secondary Master/Slave PIO

The four IDE PIO (Programmed Input/Output) fields allow users to set a PIO mode (0 to 4) for each of the four IDE devices that the on-board IDE interface supports. Modes 0 through 4 provide successively increased performance. In Auto mode, the system automatically determines the best mode for each device. Options: Auto, Mode 0, Mode 1, Mode 2, Mode 3, and Mode 4.

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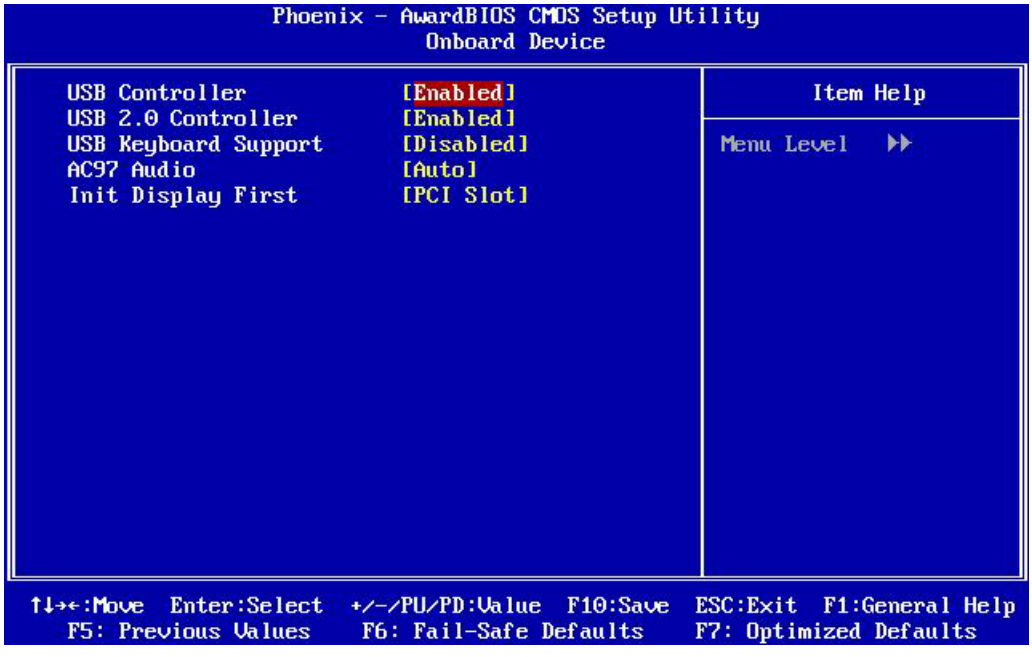
IDE Primary & Secondary Master/Slave UDMA

Ultra DMA implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver. If your hard drive and your system software both support Ultra DMA, select Auto to enable BIOS support.

IDE HDD Block Mode

Enhances disk performance by allowing multi-sector data transfers and eliminates the interrupt handling time for each sector.

On-board Device (submenu)



USB Controller

Enables USB functionality. Options: Enabled/Disabled

NOTE: Enabling only results in USB 1.1 functionality, NOT USB 2.0 functionality. Enabling the USB 2.0 controller allows USB 2.0 functionality.

USB 2.0 Controller

Enables USB 2.0 functionality. Options: Enabled/Disabled

USB Keyboard Support

Enables USB keyboard functionality (your system must have a Universal Serial Bus (USB) controller to enable). Options: Enabled/Disabled

AC '97 Audio

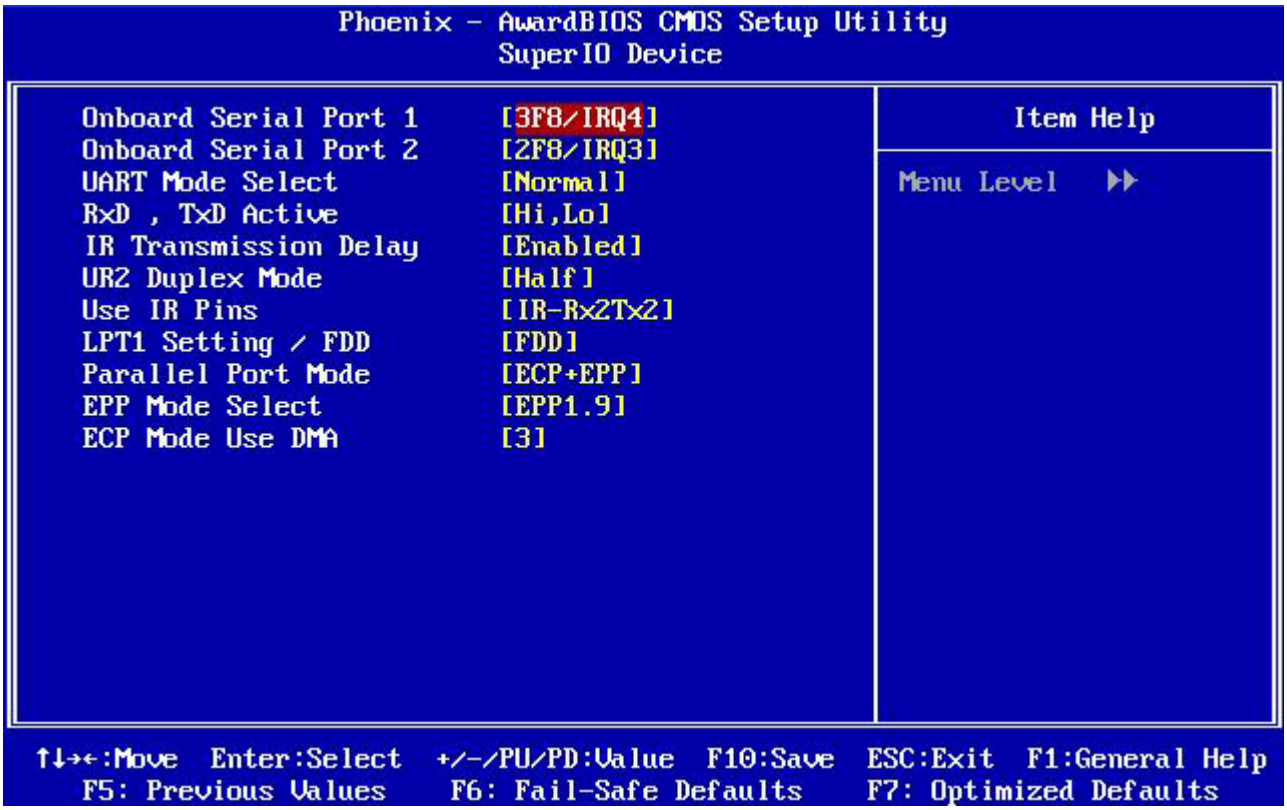
Controls on-board AC '97 audio. Options: Enable/Disabled

Init Display First

Selects whether to boot the system using the embedded AGP graphics core or a PCI graphics card.

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Super I/O Device



On-board Serial Port 1/2

Selects the address and interrupt for serial ports.

UART Mode Select

Selects the IR (Infra-Red) mode. The on-board serial port 2 offers IrDA and ASKIR modes. Use this menu to select the mode supported by your external IR device.

NOTE: Choosing the wrong IR mode will prevent your computer from communicating with an external IR device.

RxD, TxD Active

Sets the infrared reception (RxD) and transmission (TxD) polarity.

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IR Transmission Delay

Enables/Disables IR transmission delay.



UART Mode must be selected.

UR2 Duplex Mode

Controls the operating modes between receiving and transmitting IrDA or ASKIR signals.
Options: Half Mode enables asynchronous bidirectional transmission and reception.
Full Mode enables synchronous bidirectional transmission and reception.

LPT1/FDD Settings

Assigns resources to LPT1 or an FDD drive. LPT1 and FDD share the same pins on the X3 connector and only one may be used at a time.

EPP Mode Select

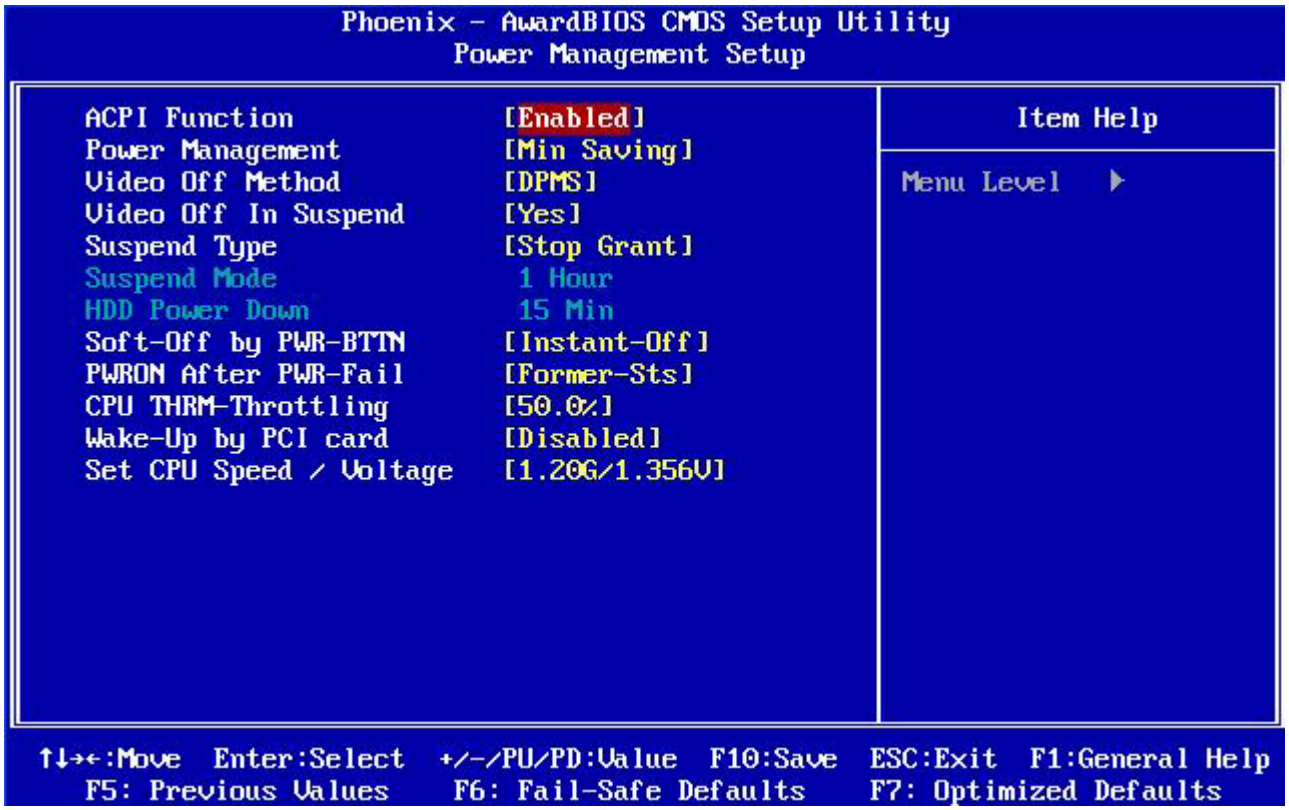
Selects the version of EPP transfer protocol that the parallel port should use. Users may choose the EPP 1.7 or EPP 1.9 version. Generally, EPP 1.9 is the preferred setting because it supports newer EPP 1.9 devices and most EPP 1.7 devices, while offering other advantages such as support for longer cables. However, certain EPP 1.7 devices can not work properly with an EPP 1.9 port. EPP 1.9 is recommended for general use, however, if there are problems connection to parallel port devices, switch to EPP 1.7

ECP Mode Use DMA

Determines which DMA channel the parallel port should use when it is in ECP mode. The ECP mode uses the DMA protocol to achieve data transfer rates of up to 2.5 Mbits/s and provides symmetric bidirectional communications.

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8.7 Power Management Setup



ACPI Function

Enabled only if the operating system supports ACPI (Advanced Configuration and Power Interface) specifications.

Power Management

User Define: Allows the user to set Suspend Mode manually.

Min. Power Saving: Minimum power management. Suspend Mode = 1 hr.

Max. Power Saving: Maximum power management. Suspend Mode = 1 min.

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Video Off Method

Determines the manner in which the monitor is cleared.

Blank Screen: This option only clears the screen of images.

V/H SYNC+Blank: Causes the system to turn off the vertical and horizontal synchronization signals and writes blanks to the screen.

DPMS Support: Display Power Management Signaling support

Video Off in Suspend

When enabled, video is turned off in suspend mode.

Suspend Mode

Selects the Suspend Type. Options: PWRON Suspend/Stop Grant.

Suspend Type

When enabled, all devices except CPU are turned off after a set period of system inactivity.

HDD Power Down

When enabled, after a selected period of drive inactivity, the hard disk drive turns off while all other devices remain active.

Soft-Off By PWR-BTTN

Defines the power-off mode when using an ATX power supply. The Instant-Off mode immediately turns off the system when the power button is pressed. In Delay 4 Sec. mode, the system turns off when the power button is held down for more than four seconds. If pressed for less than 4 seconds, the system goes into low power standby.

PWRON After PWR-Failure

On: After a power failure, the system will automatically reboot as soon as power is restored.

Off: After a power failure, the system will not reboot when power is restored. The system must be turned on manually.

Former Sts: After a power failure, the system will automatically reboot as soon as power is restored if the PC was turned on when the power failed. If the PC was already turned off when the power failed, the system needs to be turned on manually.

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CPU THRM-Throttling

A safety feature against overheating that throttles a processor back as it reaches its maximum operating temperature. Throttling does not change the processor speed but instead reduces the number of available processing cycles, thereby reducing the heat dissipation of the CPU. This cools down the CPU. Once the CPU has once again reached a safe operating temperature, thermal throttling is automatically disabled, and normal full speed processing resumes.
Options: Disabled, 87.5%, 75.0%, 62.5%, 50.0%, 37.5%, 25.0%, and 12.5%

Wake-Up by PCI Card

This field should be set to Enabled only if your PCI card (e.g. LAN or modem card) uses the PCI PME (Power Management Event) signal to remotely wake up the system. Accessing the PCI card will cause the system to wake up. Refer to the card's documentation for more information. If set to Disabled, the system will not wake up if the PCI card is accessed.

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Set CPU Speed/Voltage

This setting is only available for Intel® Pentium® M 1.6, 1.8, and 2.0 GHz CPUs (both soldered and socket types).

To reduce overall power consumption or set a hard limit for thermal reasons, this BIOS setting lets you lower the CPU Speed/Voltage. The OS itself cannot override settings in the BIOS, but some SpeedStep® related software may. Please read Warning below.

Although the BIOS supports all Intel® Pentium® M and Intel® Celeron® M CPU's, CPU Speed/ Voltage switching is only supported for the Intel® Pentium® M CPUs shown in the table below. Upon bootup, the BIOS auto-detects the CPU type and speed and inserts the correct Speed/ Voltage table into the BIOS selection menu.

The default Speed/Voltage settings are shown in **red bold**. These values are used when either "Load Failsafe Defaults" or "Load Optimized Defaults" are applied. Higher Speed/ Voltage settings must be set manually.

Intel® Pentium® M 1.6 GHz	Intel® Pentium® M 1.8 GHz	Intel® Pentium® M 2.0 GHz
1.60 GHz/1.484 V	1.80 GHz/1.324 V	2.00 GHz/1.324 V
1.40 GHz/1.420 V	1.60 GHz/1.276 V	1.80 GHz/1.276 V
1.20 GHz/1.276 V *	**1.40 GHz/1.212 V** *	1.60 GHz/1.228 V
1.00 GHz/1.164 V	1.20 GHz/1.164 V	**1.40 GHz/1.180 V** *
800 MHz/1.036 V	1.00 GHz/1.100 V	1.20 GHz/1.132 V
600 MHz/0.956 V	800 MHz/1.052 V	1.00 GHz/1.084 V
	600 MHz/0.988 V	800 MHz/1.036 V
		600 MHz/0.988 V

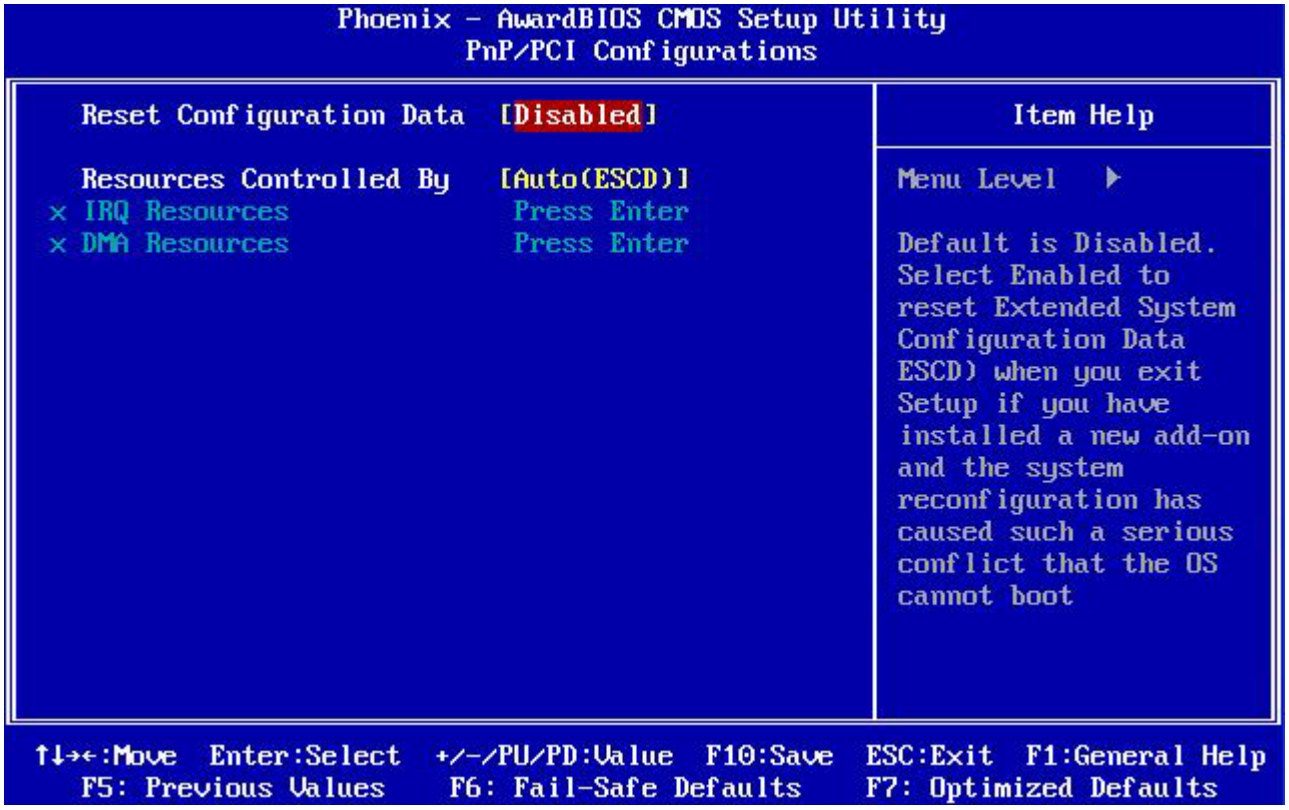
* Recommended max. speed/voltage when using heatspreader. These values are used when either "Load Failsafe Defaults" or "Load Optimized Defaults" are applied.



When certain operating systems are installed, such as Windows® XP with Service Pack 2, the above BIOS settings may be automatically overridden by native support for dynamic voltage and frequency switching. This means that the CPU may be switched to a higher frequency and voltage than is specified by the BIOS.

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8.8 PnP/PCI Configurations



This section describes configuring the PCI bus system. PCI, or Personal Computer Interconnect, is a system which allows I/O devices to operate at speeds nearing the speed the CPU itself uses when communicating with its own special components.

Reset Configuration Data

Resets the ESCD (Extended System Configuration Date) if an error message occurs after installing a new device.

Resource Controlled By

The Award Plug and Play BIOS can automatically configure all boot and Plug-and-Play compatible devices. If Auto is selected, all interrupt requests (IRQ) and DMA assignment fields disappear, as the BIOS automatically assigns them.

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IRQ Resources

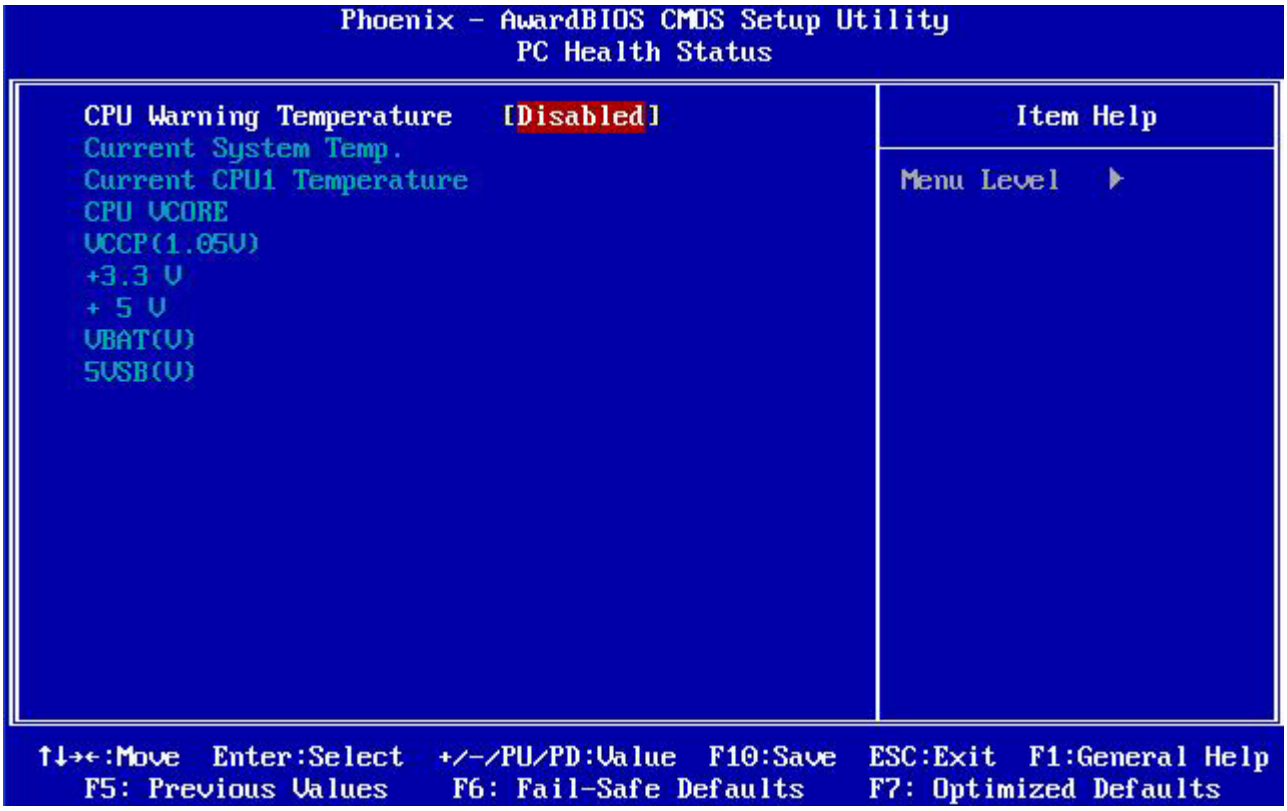
When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt:

Legacy ISA
Devices compliant with the original PC/AT bus specification, requiring a specific interrupt (such as IRQ4 for serial port 1).

PCI/ISA PnP
Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

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8.9 PC Health Status



CPU Warning Temperature

Brings up a submenu that lets the user assign a temperature level that is not to be exceeded by the CPU. If the CPU temperature goes over this limit, an audible warning signal sounds.

Current System Temp.

Displays the current system temperature.

Current CPU1 Temp.

Displays the current CPU temperature.

CPU VCORE, VCCP (1.05 V), + 3.3 V, + 5 V, VBAT (V), and 5 VSBV

Displays the actual voltage levels on the board.

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8.10 BIOS POST Messages

If BIOS detects an error during the Power On Self-Test (POST), it will prompt the user by either sounding a beep or displaying a message. If a message is displayed, it will be accompanied by:

PRESS <F1> TO CONTINUE, OR <DEL> TO ENTER SETUP

POST Beep

Currently, there are two types of beep codes in the BIOS :

- This first beep code indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by two short beeps.
- The second beep code indicates that a DRAM error has occurred. This beep code consists of a repeated single long beep.

Error Messages

One or more of the following messages may be displayed if the BIOS detects an error during the POST.

- CMOS CHECKSUM ERROR - DEFAULTS LOADED
  Checksum of CMOS is incorrect. This may indicate that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.
- DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER
  No boot device was found. This could mean that either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Drive A: and press <Enter>. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Reboot the system.
- DISKETTE DRIVES OR TYPES MISMATCH ERROR - RUN SETUP
  Type of diskette drive installed in the system is different from the CMOS definition. Run Setup to reconfigure the drive type correctly.
- DISPLAY SWITCH IS SET INCORRECTLY
  Display switch on the motherboard can be set to either monochrome or color. This indicates the switch is set to a different setting than indicated in Setup. Determine which setting is correct, then either turn off the system and change the jumper, or enter Setup and

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change the VIDEO selection.

- FLOPPY DISK CNTRLR ERROR OR NO CNTRLR PRESENT
  Cannot find or initialize the floppy drive controller. Make sure the controller is installed correctly and firmly. If there are no floppy drives installed, be sure the Diskette Drive selection in Setup is set to NONE.

- KEYBOARD ERROR OR NO KEYBOARD PRESENT
  Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during system boot. If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause the BIOS to ignore the missing keyboard and continue system boot.

- OFFENDING ADDRESS NOT FOUND
  This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

- OFFENDING SEGMENT
  This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem has been isolated.

- PRESS A KEY TO REBOOT
  This will be displayed at the bottom of the screen when an error occurs that requires you to reboot. Press any key and the system will reboot.

- PRESS F1 TO DISABLE NMI, F2 TO REBOOT
  When the BIOS detects a Non-Maskable Interrupt (NMI) condition during boot, you can choose to disable the NMI and continue to boot, or you can reboot the system with NMI enabled.

- RAM PARITY ERROR - CHECKING FOR SEGMENT
  Indicates a parity error in Random Access Memory.

- SYSTEM HALTED, PRESS (CTRL-ALT-DEL) TO REBOOT
  Indicates the present boot attempt has been aborted and the system must be rebooted. Press and hold down the <CTRL> and <ALT> keys and press <DEL>.

- MEMORY TEST FAIL
  BIOS reports the memory test as failed if the on-board memory test results in an error.

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8.11 BIOS POST Codes

Normal POST Codes

POST (hex)	Name	Description
C0	Chipset & CPU Test	OEM Specific-Cache control Processor Status (1FLAGS) Verification. Tests the following processor status flags: Carry, zero, sign, and overflow. The BIOS sets each flag, verifies they are set, then turns each flag off and verifies it is off. Reads/Writes/Verifies all CPU registers except SS, SP and BP with data pattern FF and 00. RAM must be periodically refreshed to keep memory from decaying. This function ensures that the memory refresh function is working properly.
C1	Memory presence	First block memory detects. OEM Specific-Test to check amount of on-board memory. Early chipset initialization memory detection. OEM chipset routines. Clears, tests and resets first 64 KB of memory.
C2	Early memory initi	OEM Specific-Board Initialization
C3	Extended memory DRAM select	OEM Specific extended memory selection initialization. Cyrix CPU Initialization. Cache initialization.
C4	Special display handling	OEM Specific- Display/Video Switch Handling so that Switch Handling display switch errors never occurs
C5	Early shadow	OEM Specific-Early shadow enable for fast boot
C6	Cache presence test	External cache size detection
CF	CMOS check	Checks CMOS

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POST (hex)	Name	Description
1	Force load default	Loads chipset defaults
2	Reserved	
3	Early Super I/O init	Initializes early Super I/O
4	Reserved	
5	Blank video	Resets video controller
6	Reserved	
7	Init KBC	Initializes keyboard controller
8	KB test	Tests Keyboard
9	Reserved	
A	Mouse init	Initializes mouse
B	On-board audio init	Initializes on-board audio controller
C	Reserved	
D	Reserved	
E	ROM CheckSum check	Checks the integrity of the entire BIOS ROM
F	Reserved	
10	Auto-detect EEPROM	Checks flash type and copies flash write/erase routines to 0F000h segments
11	Reserved	
12	CMOS check	Checks CMOS circuitry and resets CMOS
13	Reserved	
14	Chipset default load	Programs the chipset registers with CMOS values
15	Reserved	
16	Clock init	Initializes on-board clock generator
17	Reserved	
18	Identify the CPU	Checks CPU ID and initializes L1/L2 cache
19	Reserved	
1A	Reserved	
1B	Setup interrupt	Initializes first 120 interrupt vector table vectors with SPURIOUS_INT_HDLR and initializes INT 00h-1Fh according to INT_TBL
1C	Reserved	
1D	Early PM init	First step initialization if single CPU on-board
1E	Reserved	
1F	Re-init KB	Re-initializes KB
20	Reserved	
21	HPM init	Initializes HPM (if HPM supported)
22	Reserved	
23	Test CMOS interface and battery status	Verifies if CMOS is working correctly and detects bad battery. If failed, loads CMOS defaults and loads into chipset
24	Reserved	
25	Reserved	
26	Reserved	
27	KBC final Init	Final Initialization for KBC and BIOS data setup
28	Reserved	
29	Init video Interface	Reads CMOS location 14h to detect and Initialize Video Adapter

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POST (hex)	Name	Description
2A	Reserved	
2B	Reserved	
2C	Reserved	
2D	Video memory test	Tests video memory, writes sign-on message to screen sets up shadow RAM, and enables shadow RAM according to setup
2E	Reserved	
2F	Reserved	
30	Reserved	
31	Reserved	
32	Reserved	
33	PS2 mouse setup	Sets up PS2 mouse and reset KB
34	Reserved	
35	Test DMA Controller 0	Tests DMA channel 0
36	Reserved	
37	Test DMA Controller 1	Tests DMA channel 1
38	Reserved	
39	Test DMA page Registers	Tests DMA page registers
3A	Reserved	
3B	Reserved	
3C	Test timer Counter 2	Tests 8254 Timer 0 counter 2
3D	Reserved	
3E	Test 8259-1 mask bits	Verifies 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines
3F	Reserved	
40	Test 8259-2 mask bits	Verify 8259 Channel 2 masked interrupts by alternately turning off and on the interrupt lines
41	Reserved	
42	Reserved	
43	Test stuck 8259's interrupt bits Test 8259 interrupt functionality	Turns off interrupts then verifies if interrupt mask register is on Forces an interrupt and verifies the interrupt event
44	Reserved	
45	Reserved	
46	Reserved	
47	Set EISA mode	If EISA nonvolatile memory checksum is good, executes EISA initialization. If not, executes ISA tests and clears EISA mode flag.
48	Reserved	
49	Size base and extended memory	Tests fbase memory from 256 KB to 640 KB and extended memory above 1 MB

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POST (hex)	Name	Description
4A	Reserved	
4B	Reserved	
4C	Reserved	
4D	Reserved	
4E	Base and Extended Memory Test	Tests base memory from 256 KB to 640 KB and extended memory above 1 MB using various patterns.
4F	Reserved	
50	USB init	Initializes USB controller
51	Reserved	
52	Memory Test	Tests all memory above 1 MB using Virtual 8086 mode, page mode and clears the memory
53	Reserved	
54	Reserved	
55	CPU display	Detects CPU speed and displays CPU vendor specific version strings and turns on all necessary CPU features
56	Reserved	
57	PnP Init	Displays PnP logo and PnP early initialization
58	Reserved	
59	Setup Virus Protect	Sets up virus protection according to setup
5A	Reserved	
5B	Awdflash Load	If required, will auto load Awdflash.exe in POST
5C	Reserved	
5D	Onboard I/O Init	Initializes onboard Super I/O
5E	Reserved	
5F	Reserved	
60	Setup enable	Displays setup message and enables setup functions
61	Reserved	
62	Reserved	
63	Check PS2 Mouse	Detects if mouse is present
64	Reserved	
65	Initialize & Install Mouse	Initializes mouse and installs interrupt vectors
66	Reserved	
67	ACPI init	ACPI subsystem initialization
68	Reserved	
69	Setup Cache Controller	Initializes cache controller
6A	Reserved	
6B	Setup Entering	Enters setup, system checks and auto configuration settings
6C	Reserved	
6D	Initialize Floppy Drive & Controller	Initializes floppy disk drive controller and any installed drives
6E	Reserved	

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POST (hex)	Name	Description
6F	FDD install	Installs FDD and sets up BIOS data parameters
70	Reserved	
71	Reserved	
72	Reserved	
73	Initialize Hard Drive & Controller	Initializes hard drive controller and any installed drives
74	Reserved	
75	Install HDD	Detects and installs IDE devices
76	Reserved	
77	Detect & Initialize Serial/Parallel Ports	Initializes any serial and parallel ports (also game ports)
78	Reserved	
79	Reserved	
7A	Detect & Initialize Math Co-processor	Initializes math co-processor
7B	Reserved	
7C	HDD Check for Write protection	Checks HDD write protection
7D	Reserved	
7E	Reserved	
7F	POST error check	Checks POST errors and displays them and asks for user intervention
80	Reserved	
81	Reserved	
82	Security Check	Asks for password security (optional)
83	Write CMOS	Writes all CMOS values back to RAM and clears screen
84	Pre-boot Enable	Enables parity checker NMI, and cache before boot
85	Initialize Option ROMs	Initialize any option ROMs present from C8000h to EFFFFh.
86	Reserved	
87	Reserved	
88	Reserved	
89	Reserved	
8A	Reserved	
8B	Reserved	
8C	Reserved	
8D	Reserved	
8E	Reserved	
8F	Reserved	
90	Reserved	
91	Reserved	

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POST (hex)	Name	Description
92	Reserved	
93	Boot medium detection	Reads and stores boot partition head and cylinder values in RAM
94	Final Init	Final configuration before boot
95	Special KBC patch	Sets system speed for boot Sets up NumLock status according to Setup
96	Boot Attempt	Sets low stack Boots via INT 19h.
FF	Boot	

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Appendix A: **Heatspreaders and Heatsinks**

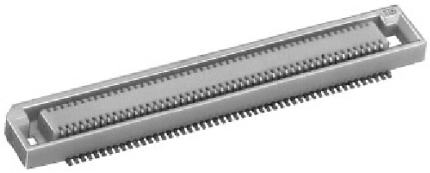
A. 1 **Carrier Board ETX connecter heights** (Hirose FX8/FX8C Receptacles)

For different stacking heights, the receptacles for ETX carrier boards are available in two heights, 3 mm and 9.5 mm. When 3 mm receptacles are chosen, the carrier board should be free of components.

FX8-100S-SV

100-pin board-to-board connector for 3 mm board stacking

This connector can be used with :
- 3 mm through-hole standoffs (SMT type)
- 3 mm threaded standoffs (DIP type)



FX8C-100S-SV5

100-pin board-to-board connector for 9.5 mm board stacking

This connector can be used with :
- 9.5 mm through-hole standoffs (SMT type)
- 9.5 mm threaded standoffs (DIP type)



FX8C/FX8 Common Spec

- Current capacity 0.4 A per pin
- Rated voltage 100 V AC
- Insulation resistance 100 M or greater @ 250 V DC
- Withstand voltage 300 V AC r.m.s.
- Contact resistance 45 m or less @ 100 mA DC
- Insulation PPS resin (Light brown, UL94V-0)
- Contacts phosphor bronze (gold plated contacts and leads)

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A. 2 **Heatspreader Introduction**

The heatspreader function is to ensure an identical mechanical profile for every ETX module. In this way the heat solution, that is built on top of the heatspreader is compatible with any ETX module not just the ETX-IM333 (or ETX-IM266).



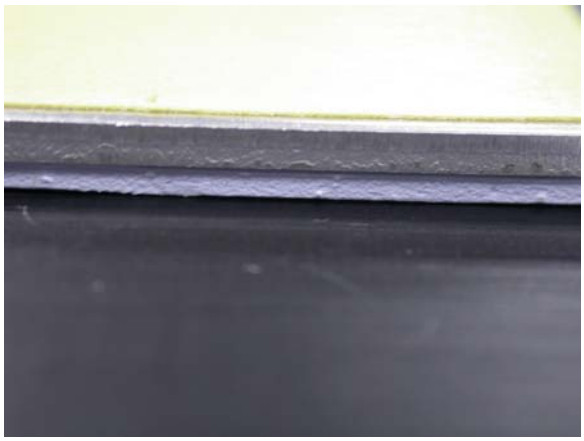
Remove the protective layer from CPU and Northbridge pads before placing the heatspreader on the module !



Heatspreader placed on ETX-IM333 (ETX-IM266) with free space to mount SODIMM memory



Heatpads for BGA type CPU's and Northbridge



From top to bottom:
- Face change (yellow)
- Aluminum pad (silver)
- Flexible heat pad (light blue)
- Aluminum heatspreader plate (black)

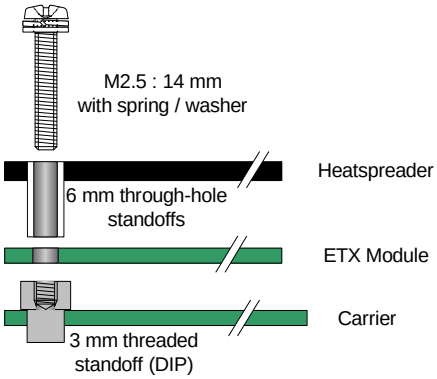
WARNING: Only for BGA type LV and ULV CPU's under 15 Watts

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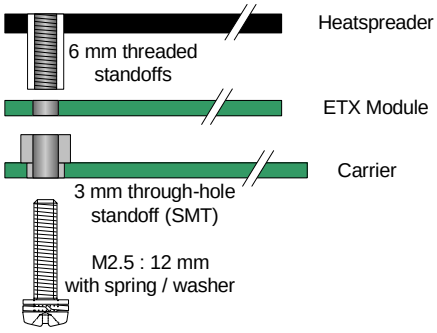
A. 3 **Mounting procedures**

There are several standard ways to mount an ETX board with heatspreader on a carrier board. ETX boards may be mounted with 9 mm ETX connectors on the carrier board or standard 3 mm connectors. Mounting may also choose between two different types of heatspreaders, threaded standoffs which require inserting screws from under the carrier; or TOP mounting using through hole heatspreader standoffs and the carrier board standoffs are thread.

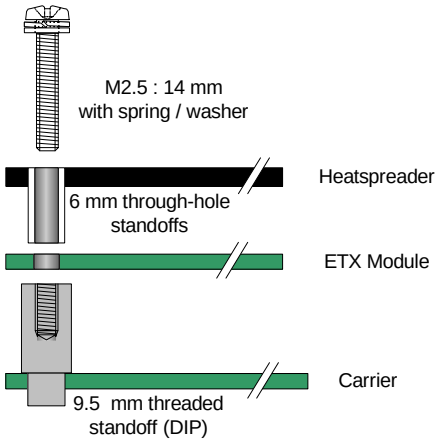
Top Mounting
3 mm Hirose FX8-100S-SV
Carrier Board Connectors



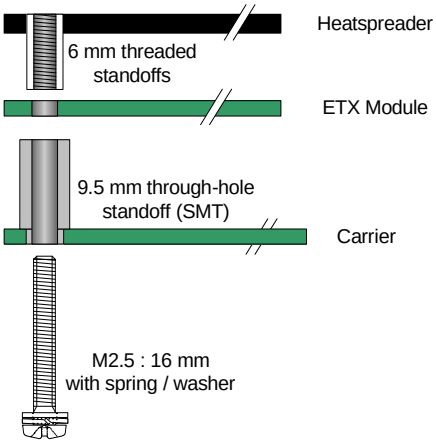
Bottom Mounting
3 mm Hirose FX8-100S-SV
Carrier Board Connectors



Top Mounting
9 mm Hirose FX8C-100S-SV5
Carrier Board Connectors



Bottom Mounting
9 mm Hirose FX8C-100S-SV5
Carrier Board Connectors



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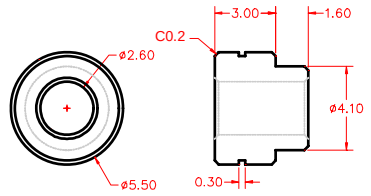
A. 4 **Standoff types**

For different mounting procedures there are different, readily available standoffs. Note that threaded standoffs are all DIP type and the through-hole types are all SMT type. Other types not listed can be made available upon request.

33-72000-0030

3 mm through-hole standoff (SMT type)

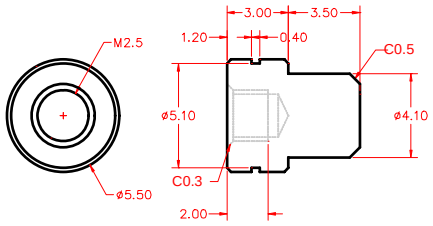
for HTS-IM333 with 3 mm Hirose carrier board connectors



33-72011-0030

3 mm threaded standoff (DIP type)

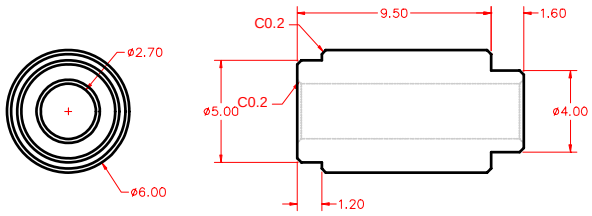
for HTS-IM333-T with 3 mm Hirose carrier board connectors



33-72007-9P50

9.5 mm through-hole standoff (SMT type)

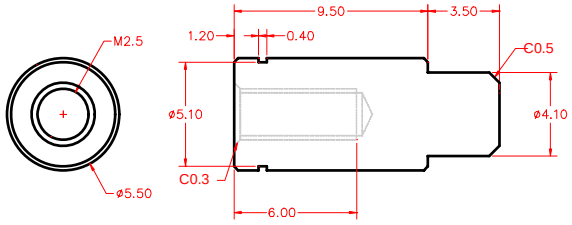
for HTS-IM333 with 9 mm Hirose carrier board connectors



33-72011-9P50

9.5 mm threaded standoff (DIP type)

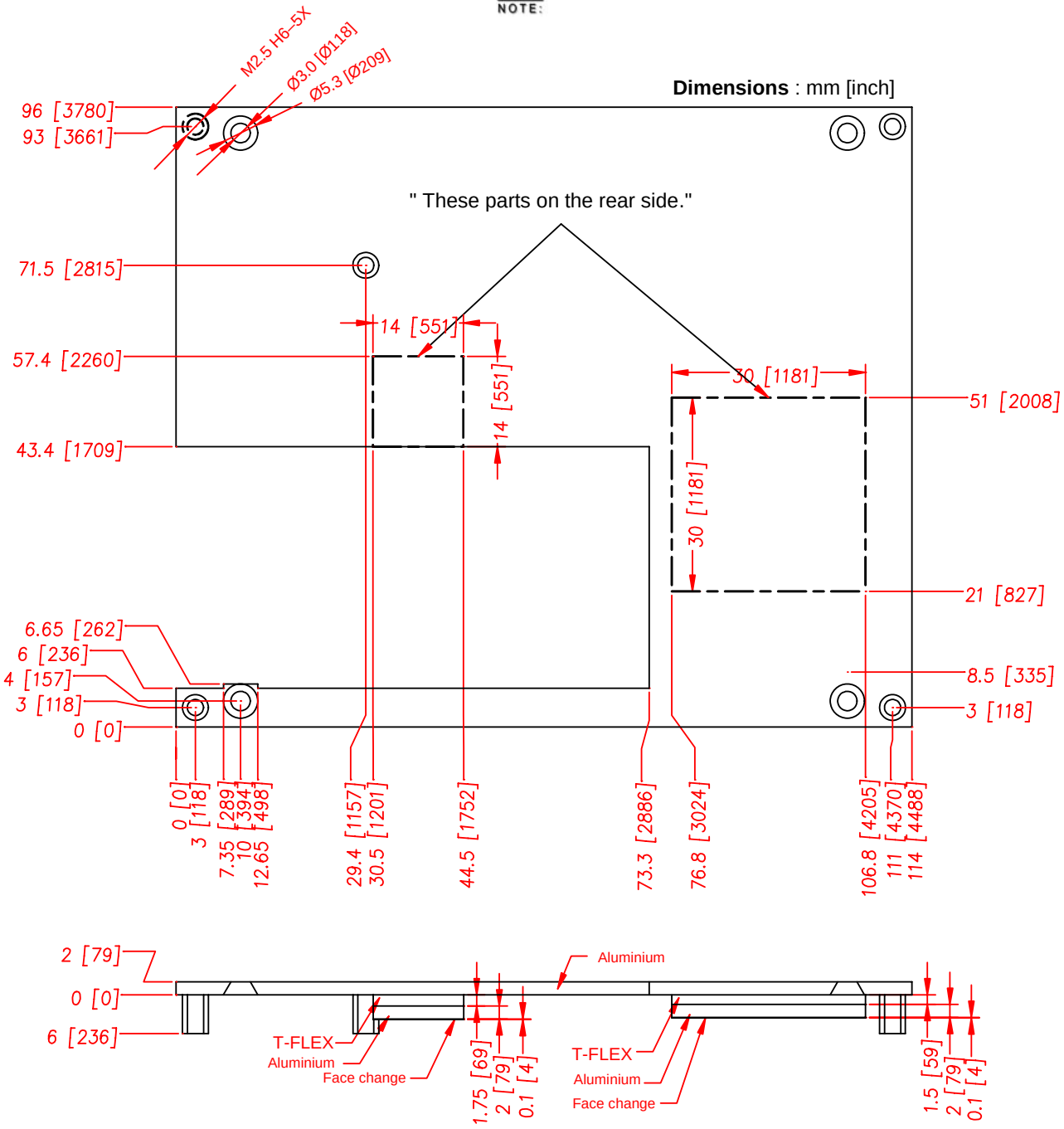
for HTS-IM333-T with 9 mm Hirose carrier board connectors



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A. 5 **Heatspreader Dimensions for HTS-IM333-B** (threaded standoffs)

NOTE: Only for BGA type LV and ULV PU's below 15 Watts

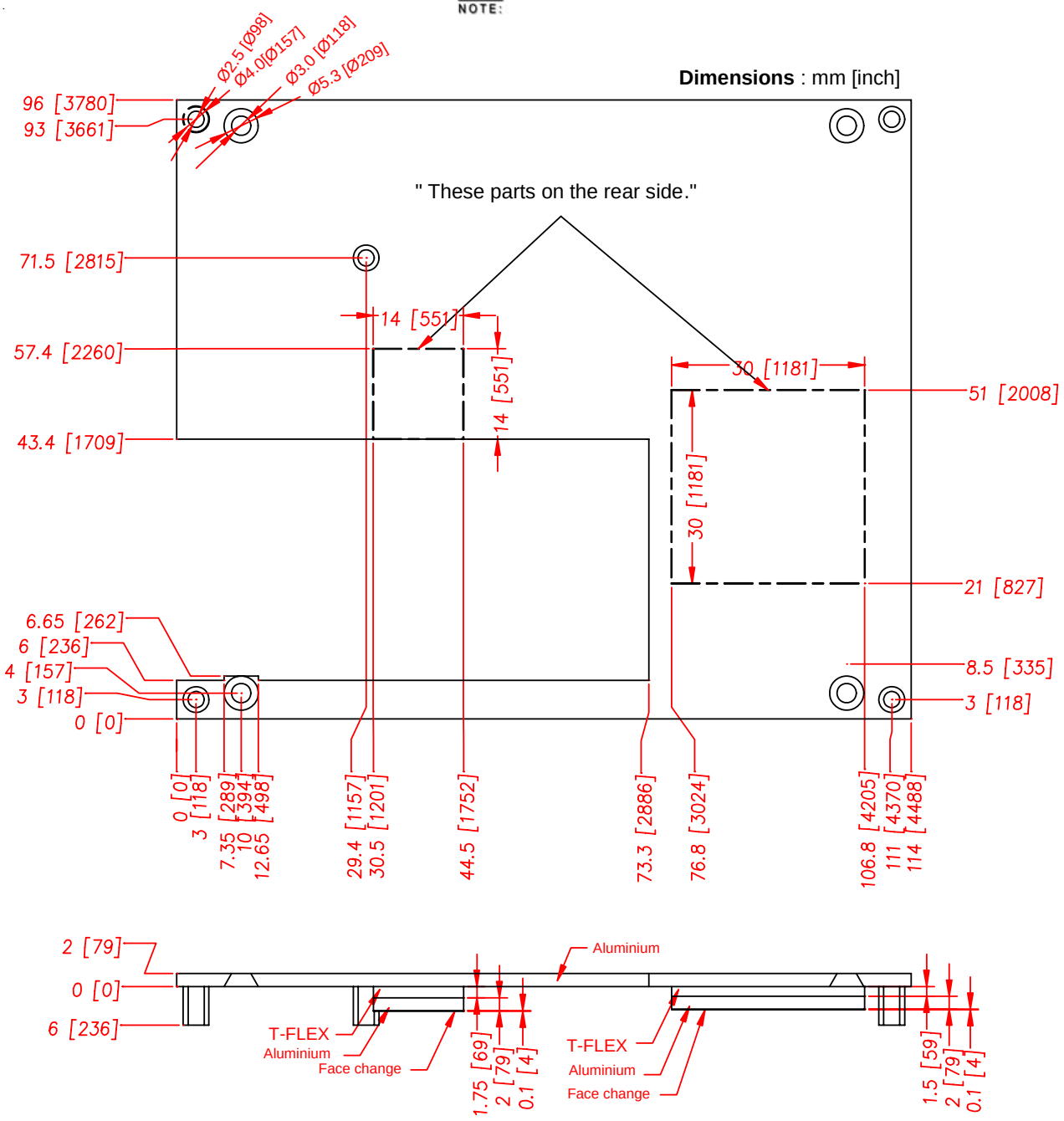


- The heatspreader comes included with four M2.5 at 12 mm with washer/spacer
- The above heatspreader can be used with ETX-IM333 and ETX-IM266 models.

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A. 6 **Heatspreader Dimensions for HTS-IM333-BT** (through-hole standoffs)

NOTE: Only for BGA type LV and ULV PU's below 15 Watts



- The heatspreader comes included with four M2.5 at 14 mm with washer/spacer, If using 9 mm standoffs on the carrier board, M2.5 at 18 mm with washer/spring are required and must be ordered separately.
- The above heatspreader can be used with ETX-IM333 and ETX-IM266 models.

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A. 7 **THSF-IM333:** High Performance Heatsink with Fan

The THSF-IM333-S (socket type CPU) and THSF-IM333-B (BGA, soldered type CPU) are high performance heatsinks that can easily support CPU types with thermal outputs of up to 35 Watts. The fan on the heatsink requires a 12 Volt power source.
The THSF-IM333 only supports “bottom mounting”and can be used with either ETX-IM333 or with ETX-IM266 models which are mechanically identical.



Aluminum body, with copper CPU head and 12 V high performance fan



THSF-IM333 installed on ETX-IM333 and ETX-carrier board.

NOTE: Supports all CPUs, either BGA or Socket type

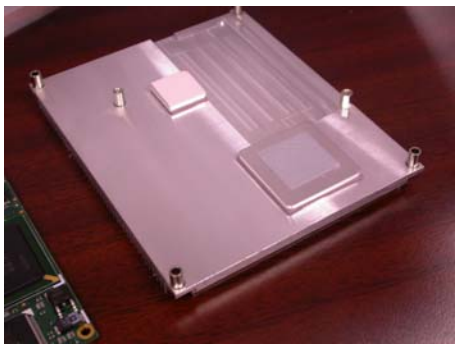
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A. 8 **THS-IM333 Series:** Low Profile Heatsinks

The THS-IM333 Heatsink Series (for BGA type CPUs only) are low profile heatsinks that are optimized for reduced height applications. Although the heatsinks are fanless they still require some airflow to efficiently cool applications. The heatsinks are available in two cooling fin orientations and have both top and bottom mounting options (threaded- vs through-hole standoffs. THS-IM333 Series can be used with either ETX-IM333 and ETX-IM266 models which are mechanically identical.



THSF-IM333-T heatsink with ETX-IM333-P1400



Pads for CPU and Northbridge



Heatsink mounted on ETX-IM333

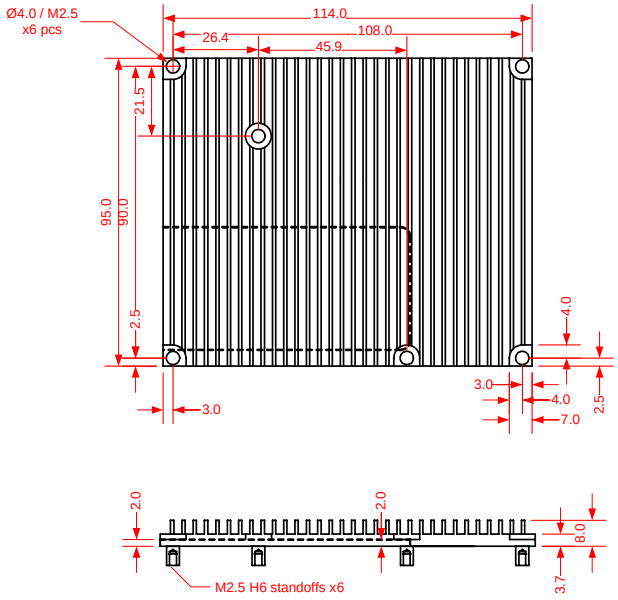
NOTE: Only for BGA type CPU's below 22 Watts

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A. 9 **Dimensions for THS-IM333 Series**

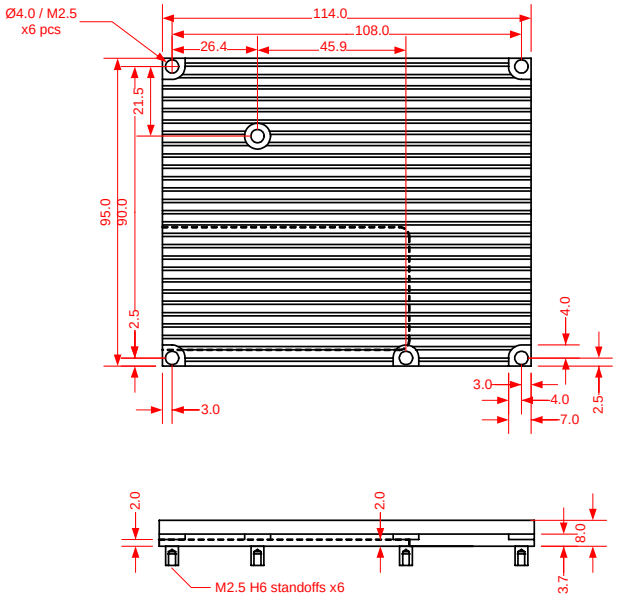
THS-IM333

Heatsink with short fins and threaded standoffs for bottom mounting



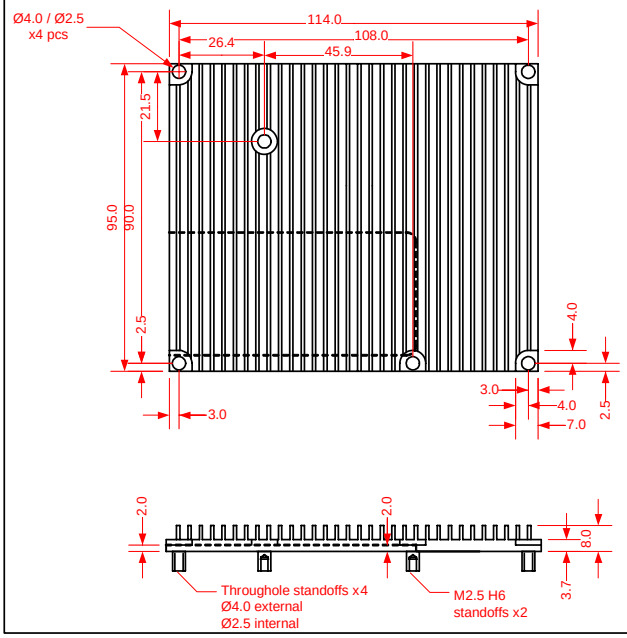
THS-IM333-L

Heatsink with long fins and threaded standoffs for bottom mounting



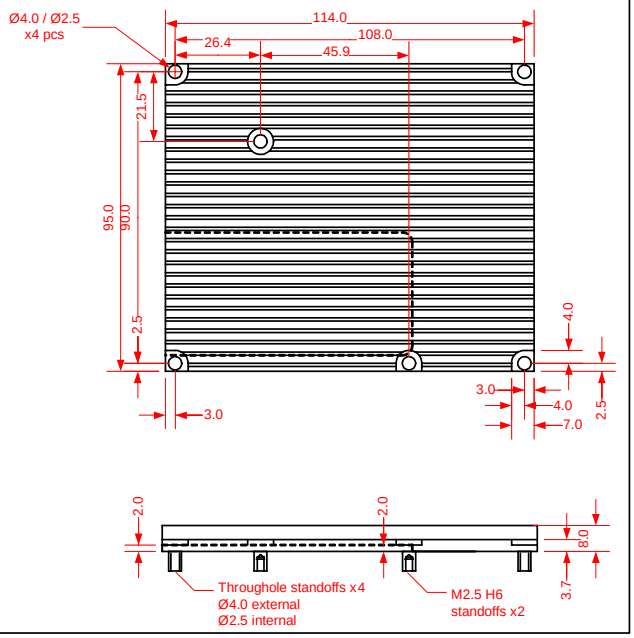
THS-IM333-T

Heatsink with short fins and through-hole standoffs for top mounting



THS-IM333-TL

Heatsink with long fins and and through-hole standoffs for top mounting



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Important Safety Instructions

For user safety, please read and follow all instructions, warnings, cautions, and notes marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:

  - Turn off power and unplug any power cords/cables.

- To avoid electrical shock and/or damage to equipment:

  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.
- A Lithium-type battery may be provided for uninterrupted, backup or emergency power.



Risk of explosion if battery is replaced by an incorrect type. Dispose of used batteries according to the instructions.

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- Equipment must be serviced by authorized technicians when:

  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

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Getting Service

Contact us should you require any service or assistance.

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