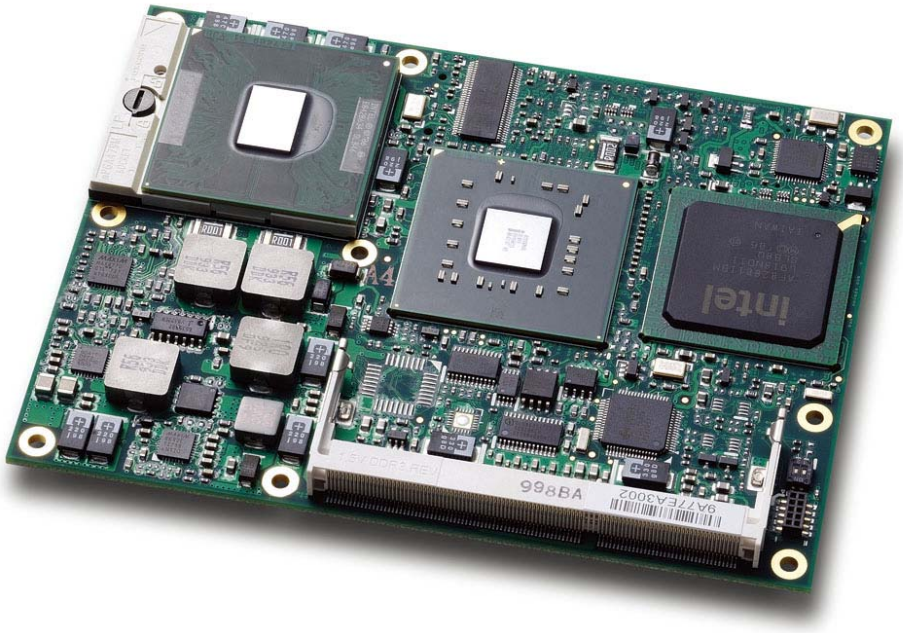
COM Express

Express-MG

User's Manual



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ADLINK TECHNOLOGY INC.

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Preface

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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.



Additional information that help users perform tasks.



Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.



Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

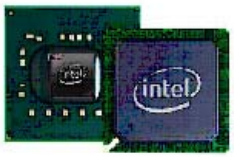
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1 Introduction

1.1 Description

The Express-MG is a COM Express compliant module specially designed to facilitate speedy development of semi-custom designs. The COM Express standard embodies the convergence of the latest technology standards based on serial differential signaling such as PCI Express, USB 2.0, SATA, LVDS and Serial DVO implemented on a compact, 95mm x 125mm, Computer-on-Module. Signals are brought out through two 220-pin board-to-board connectors that permit data transmission rates of up to 5GHz. Mounting holes connect the module with a custom-made, application specific carrier boards which provide protection from shock and vibration.

The Express-MG combines a socket type Penryn Core™2 Duo CPU with Intel's Mobile GM45 Express Chipset. The chipset consisting of GM45/ICH9M North- and Southbridge supports up to 8 GB, dual channel DDR3 800/1066MHz memory on two stacked SODIMM sockets.



The Mobile Intel® GM45 Express chipset integrates a Mobile Intel® Graphics Media Accelerator 4500MHD that provides VGA, single/dual channel 24-bit LVDS and TV-out (SDTV and HDTV). The GMA 4500MHD includes support for DirectX 10, Shader Model 4.0, and provides an increase in performance over previous chipsets. Intel® Clear Video Technology together with HDCP support allows for smooth Blu-Ray playback. In addition to the onboard integrated graphics, a PCI Express x16 graphics link is available for connection to high end PCI Express x16 graphics chipsets or general purpose x8, x4 or x1 PCI Express devices. The PCI Express Graphics (PEG) x16 bus pinout can alternatively be used for two SDVO, two HDMI or three DisplayPort interfaces to connect to DVI, TMDS or TV-out device controllers.

The module comes with a single onboard Gigabit Ethernet port and four SATA ports. It has optional legacy IDE support through a SATA-to-PATA controller, 32-bit PCI and LPC. The module allows connection of up to five additional PCI Express x1 devices on the Southbridge.

The Express-MG comes equipped with a AMIBIOS®8 and supports many embedded features such as remote console, CMOS backup, CPU and system monitoring, watchdog timer for NMI or RESET, operation over battery power, and extended power modes.

The Express-MG is a RoHS compliant and lead-free product.

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2 Specifications

2.1 General

- **CPU:** **Penryn Core PGA type**
  Intel® Core™2 Duo T9400, FSB 1066, 2.53 GHz with 6-MB L2 cache, 35 W
  Intel® Core™2 Duo P8400, FSB 1066, 2.26 GHz with 3-MB L2 cache, 25 W
  Intel® Celeron T3100, FSB 800, 1.90 GHz with 1-MB L2 cache, 35 W
  Intel® Celeron® 575, FSB 667, 2.00 GHz with 1-MB L2 cache, 31 W
- **Memory:** Dual SODIMM socket memory (one on top, one on bottom) supporting dual channel memory bandwidth, for max 8 GB of non-ECC, 800/1067 MHz DDR3
- **Chipset:** Intel® GM45 Express Graphic Memory Controller Hub and Intel® I/O Controller Hub ICH9M
- **L2 Cache:** 1 MB (Celeron®), 2/4 MB (Core™2 Duo)
- **BIOS:** AMIBIOS®8 with CMOS backup in 8 Mbit SPI BIOS
- **Hardware Monitor:** Supply voltages and CPU temperature
- **Watchdog Timer:** Programmable timer ranges to generate RESET
- **Expansion Busses:**
  - Graphics PCI Express x16 bus for SDVO/HDMI/DisplayPort or General Purpose PCI Express x8, x4, or x1
  - 6 PCI Express x1 (0/1/2/3/4 are free, 5 is occupied by GbE LAN, 0/1/2/3 PCIe x1 can be optionally configured as 1 x4)
  - 32-bit PCI 2.3 at 33MHz, supporting 4 bus masters
  - LPC, SMBus (system), I2C (user)

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2.2 Video

- **Chipset:** GM45 GMCH integrated Mobile Intel® Graphics Media Accelerator X4500 with core render clock 533-MHz @ 1.05 V core
- **Integrated Video Feature Support:**
  - Intel® Dynamic Video Memory Technology (Intel® DVMT 5.0)
  - Video capture via x1 concurrent PCI Express port
  - PAVP (Protected Audio-Video Path) support for Protected Intel HD Audio Playback
  - High performance MPEG-2 decoding
  - WMV9 (VC-1) and H.264 (AVC) support
  - Hardware acceleration for MPEG2 VLD/iDCT
  - Microsoft DirectX10 support
  - OpenGL 2.1 support
  - Blu-ray support @ 40 Mb/s
  - Hardware motion compensation
  - Intermediate Z in classic rendering
- **VGA Interface:** Analog VGA support up to QXGA, 300MHz DAC
- **LVDS Interface:** Single or dual channel 18/24-bit at 25~112 MHz
- **TV-out:** NTSC/PAL up to 1024x768 resolution supported, HDTV 480p/720p/1080i/1080p modes support (without Macrovision)

2.3 Audio

- **Chipset:** Integrated in Intel® I/O Controller Hub 9 Mobile (ICH9M)
- **Audio Codec:** On carrier (ALC888)
- **HDMI:** Same audio routed to HDMI interface

2.4 LAN

- **Chipset**: Integrated in Intel® ICH9M with Intel® 82567LM PHY
- **Interface:** 10/100/1000 Mbps Ethernet

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2.5 Multi I/O

- **PATA:** SATA-to-PATA JM20330 controller on SATA channel 3, Master only
- **SATA**: Four ports SATA 3 Gb/s
- **USB**: Supports up to eight ports USB 2.0

2.6 Super I/O

- Connected to LPC bus on carrier if needed

2.7 TPM (Trusted Platform Module)

- **Chipset**: Infineon SLB9635TT1.2
- **Type:** TPM 1.2

2.8 Power Specifications

- **Input Power:** AT mode (12 V +/- 5%) and ATX mode (12 V and 5 Vsb +/- 5%)
- **Power States:** Supports S0, S1, S3, S4, S5
- **Power Consumption:** 8.5 W (with Core™2 Duo T9400 and 2 GB memory, typical)
- **Smart Battery Support:** Yes

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2.10 Operating Systems

- **Standard Support**

  - Windows XP 32/64-bit
  - Windows Vista 32/64-bit
  - Windows Server 2003/2008

- **Extended Support (BSP)**

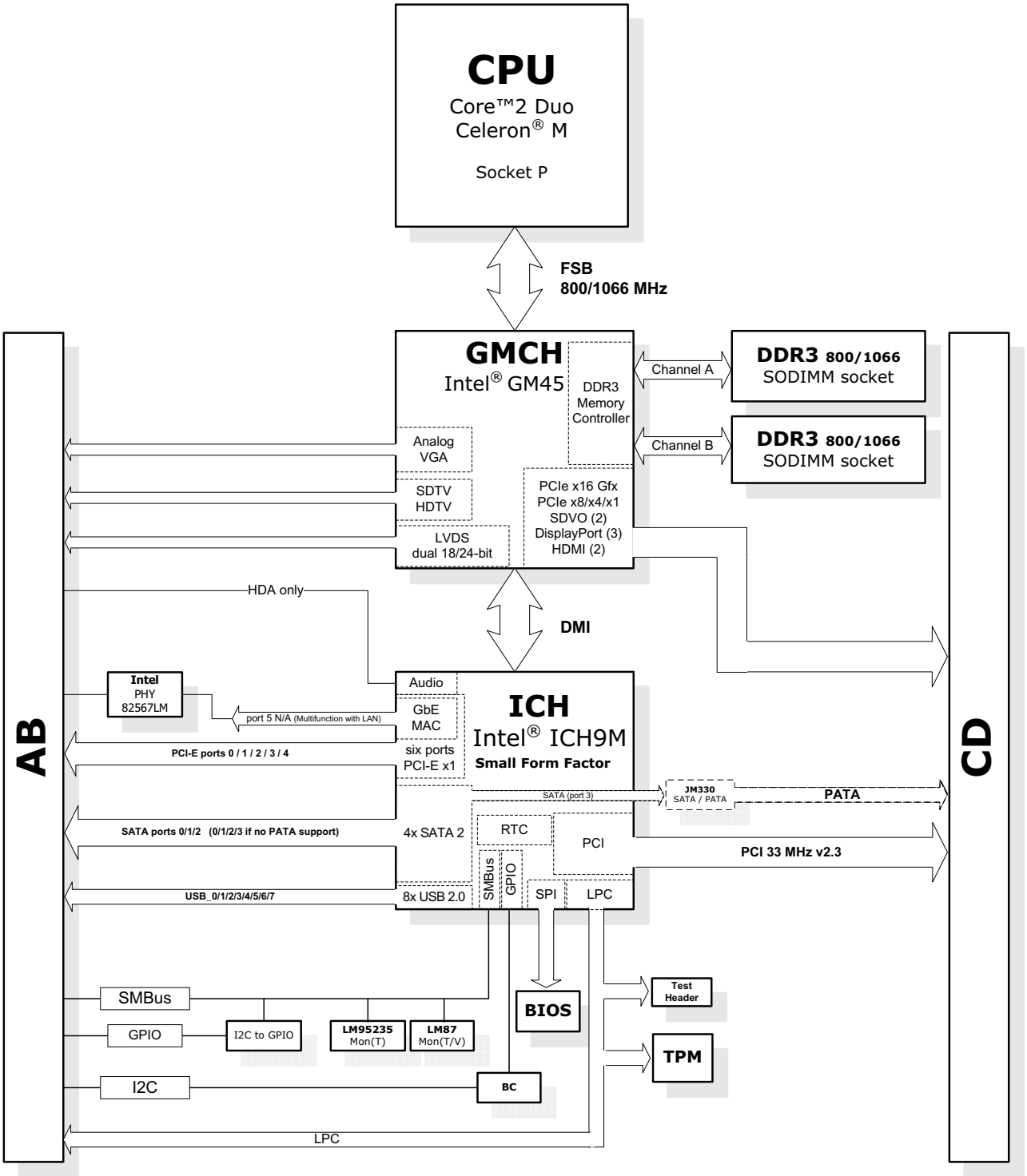
  - Embedded XP BSP
  - WinCE 6.0 BSP
  - AIDI I2C Library for Win32, WinCE and Linux

2.11 Mechanical and Environmental

- **Form Factor and Type:** PICMG COM.0, Standard COM Express® Type 2
- **Dimensions:** 95 x 125 mm
- **Standard Operating Temperature:** 0°C to 60°C
- **Relative Humidity:** up to 90% at 60°C

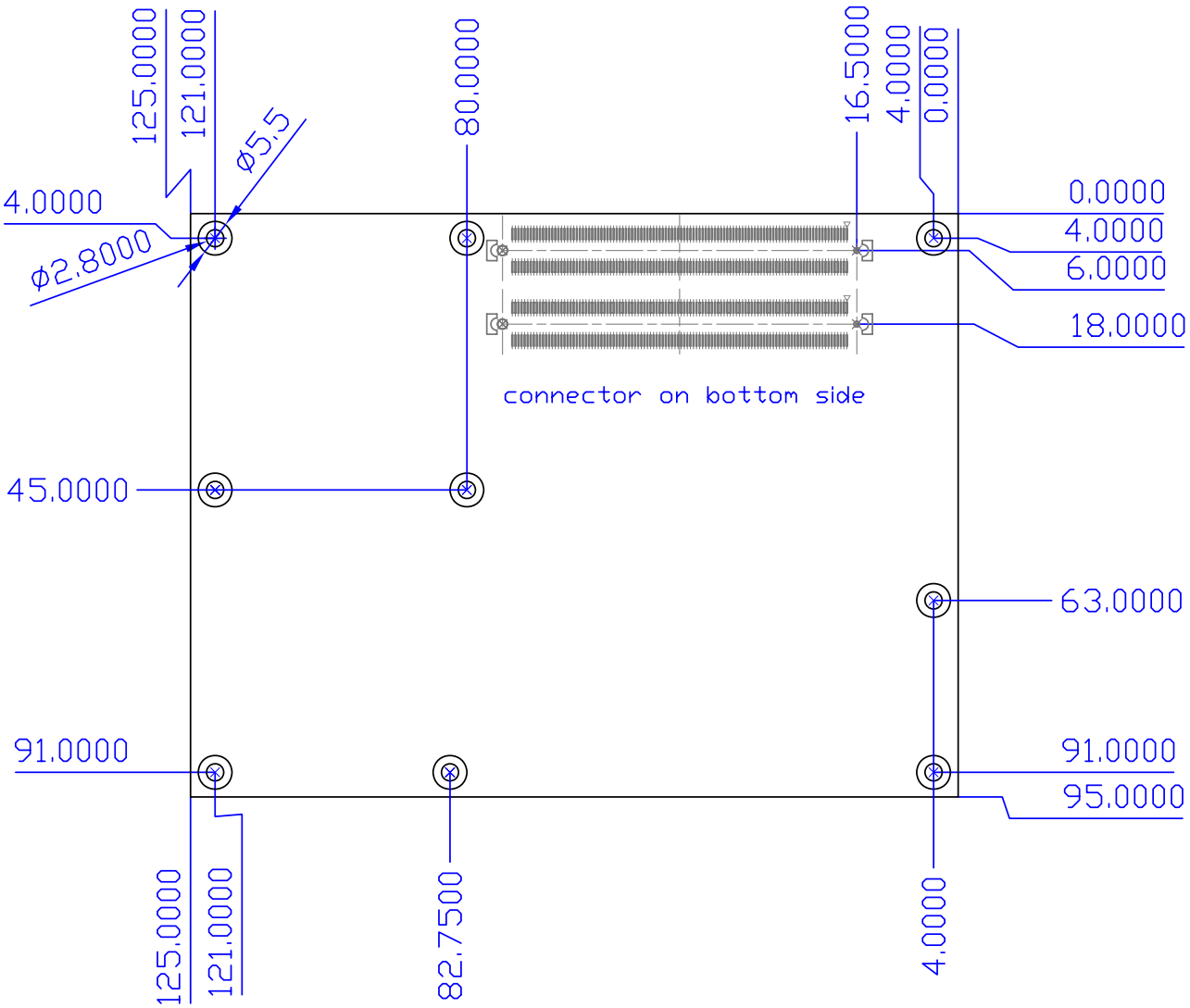
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3 Functional Diagram



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4 Mechanical Dimensions



TOP VIEW

All ∅ tolerances ± 0.05 mm
Other tolerances ± 0.2 mm

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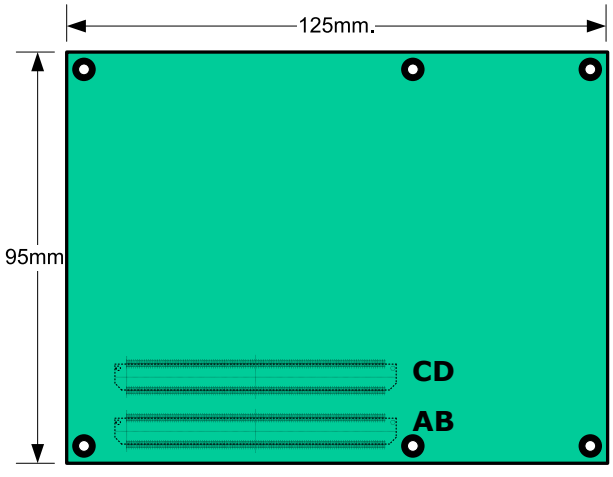
5 Pinout and Signal Descriptions

5.1 COM Express® Type 2

All pinouts on AB and CD connector of the Express-MG comply with pinout and signal descriptions used in the original **PICMG® COM.0 R1.0: COM Express® Module Base Specification**. This document contains a pinouts, signal descriptions, and mechanical characteristics of the COM Express® form factor.

An additional document, " Express® Design Guide" gives a general introduction to carrier board designs for COM Express® (Express®) modules.

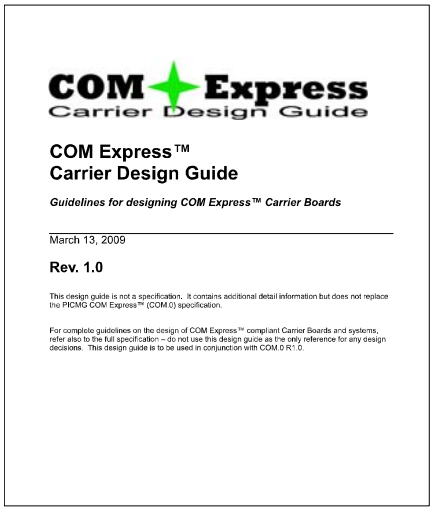
AB Connector
1 Gigabit Ethernet port
LPC interface
4 Serial ATA channels
High Definition Audio
8 USB 2.0 ports
5 PCI Express Lanes x1
Dual 24-bit LVDS channels
Analog VGA
TV-out ports (SDTV/HDTV)
8 GPIO pins
SMB and I²C bus
+12V primary power input
+5V standby and 3V RTC



CD Connector
Parallel ATA, IDE port alternate definition assigns this to 2 additional Gigabit Ethernet ports
32-bit PCI v2.3 bus alternate definition assigns this to 10 additional PCI Express x1 lanes
PCI Express x16 for Graphics these pins can also be assigned to two SDVO extensions (multiplexed)
Power / Thermal control
+12V primary power input

5.2 Carrier Board Design Guide

The PICMG COM Express Carrier Design Guide is a 160-page document that provides information on designing a custom carrier board for COM Express modules. The design guide includes reference schematics for the external circuitry required to implement the various COM Express peripheral functions, explains how to extend the supported buses, and how to add additional peripherals and expansion slots to a COM Express-based system. You can download the document Carrier Design Guide at: http://www.adlinktech.com/ccps/picmg_comdg_100.pdf


COM Express
Carrier Design Guide

COM Express™
Carrier Design Guide

Guidelines for designing COM Express™ Carrier Boards

March 13, 2009

Rev. 1.0

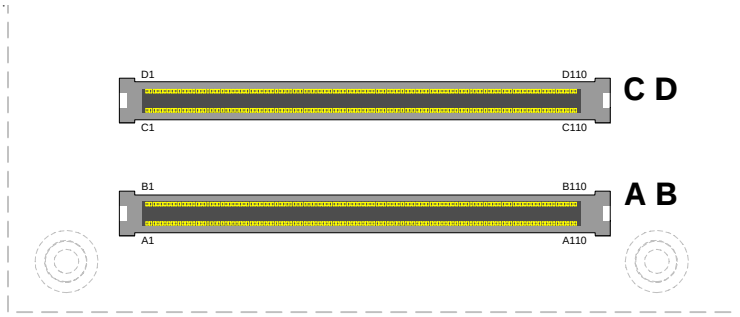
This design guide is not a specification. It contains additional detail information but does not replace the PICMG COM Express™ (COM.0) specification.

For complete guidelines on the design of COM Express™ compliant Carrier Boards and systems, refer also to the full specification – do not use this design guide as the only reference for any design decisions. This design guide is to be used in conjunction with COM.0 R1.0.

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5.3 Pin Definitions

Pinouts for:
Basic form factor, Type 2



Row A			Row B	
Pin No.	Pin Name		Pin No.	Pin Name
A1	GND (FIXED)		B1	GND (FIXED)
A2	GBE0_MDI3-		B2	GBE0_ACT#
A3	GBE0_MDI3+		B3	LPC_FRAME#
A4	GBE0_LINK100#		B4	LPC_AD0
A5	GBE0_LINK1000#		B5	LPC_AD1
A6	GBE0_MDI2-		B6	LPC_AD2
A7	GBE0_MDI2+		B7	LPC_AD3
A8	GBE0_LINK#		B8	LPC_DRQ0#
A9	GBE0_MDI1-		B9	LPC_DRQ1#
A10	GBE0_MDI1+		B10	LPC_CLK
A11	GND (FIXED)		B11	GND (FIXED)
A12	GBE0_MDI0-		B12	PWRBTN#
A13	GBE0_MDI0+		B13	SMB_CK
A14	GBE0_CTREF		B14	SMB_DAT
A15	SUS_S3#		B15	SMB_ALERT#
A16	SATA0_TX+		B16	SATA1_TX+
A17	SATA0_TX-		B17	SATA1_TX-
A18	SUS_S4#		B18	SUS_STAT#
A19	SATA0_RX+		B19	SATA1_RX+
A20	SATA0_RX-		B20	SATA1_RX-
A21	GND (FIXED)		B21	GND (FIXED)
A22	SATA2_TX+		B22	SATA3_TX+ (2)
A23	SATA2_TX-		B23	SATA3_TX- (2)
A24	SUS_S5#		B24	PWR_OK
A25	SATA2_RX+		B25	SATA3_RX+ (2)
A26	SATA2_RX-		B26	SATA3_RX- (2)
A27	BATLOW#		B27	WDT
A28	ATA_ACT#		B28	AC_SDIN2
A29	AC_SYNC		B29	AC_SDIN1
A30	AC_RST#		B30	AC_SDIN0
A31	GND (FIXED)		B31	GND (FIXED)
A32	AC_BITCLK		B32	SPKR
A33	AC_SDOUT		B33	I2C_CK
A34	BIOS_DISABLE#		B34	I2C_DAT
A35	THRMTRIP#		B35	THRM#
A36	USB6-		B36	USB7-
A37	USB6+		B37	USB7+
A38	USB_6_7_OC#		B38	USB_4_5_OC#
A39	USB4-		B39	USB5-
A40	USB4+		B40	USB5+
A41	GND (FIXED)		B41	GND (FIXED)
A42	USB2-		B42	USB3-
A43	USB2+		B43	USB3+
A44	USB_2_3_OC#		B44	USB_0_1_OC#
A45	USB0-		B45	USB1-
A46	USB0+		B46	USB1+
A47	VCC_RTC		B47	EXCD1_PERST#
A48	EXCD0_PERST#		B48	EXCD1_CPPE#
A49	EXCD0_CPPE#		B49	SYS_RESET#
A50	LPC_SERIRQ		B50	CB_RESET#

Row C			Row D	
Pin No.	Pin Name		Pin No.	Pin Name
C1	GND FIXED)		D1	GND FIXED)
C2	IDE_D7		D2	IDE_D5
C3	IDE_D6		D3	IDE_D10
C4	IDE_D3		D4	IDE_D11
C5	IDE_D15		D5	IDE_D12
C6	IDE_D8		D6	IDE_D4
C7	IDE_D9		D7	IDE_D0
C8	IDE_D2		D8	IDE_REQ
C9	IDE_D13		D9	IDE_IOW#
C10	IDE_D1		D10	IDE_ACK#
C11	GND (FIXED)		D11	GND (FIXED)
C12	IDE_D14		D12	IDE_IRQ
C13	IDE_IORDY		D13	IDE_A0
C14	IDE_IOR#		D14	IDE_A1
C15	PCI_PME#		D15	IDE_A2
C16	PCI_GNT2#		D16	IDE_CS1#
C17	PCI_REQ2#		D17	IDE_CS3#
C18	PCI_GNT1#		D18	IDE_RESET#
C19	PCI_REQ1#		D19	PCI_GNT3#
C20	PCI_GNT0#		D20	PCI_REQ3#
C21	GND (FIXED)		D21	GND (FIXED)
C22	PCI_REQ0#		D22	PCI_AD1
C23	PCI_RESET#		D23	PCI_AD3
C24	PCI_AD0		D24	PCI_AD5
C25	PCI_AD2		D25	PCI_AD7
C26	PCI_AD4		D26	PCI_C/BE0#
C27	PCI_AD6		D27	PCI_AD9
C28	PCI_AD8		D28	PCI_AD11
C29	PCI_AD10		D29	PCI_AD13
C30	PCI_AD12		D30	PCI_AD15
C31	GND (FIXED)		D31	GND (FIXED)
C32	PCI_AD14		D32	PCI_PAR
C33	PCI_C/BE1#		D33	PCI_SERR#
C34	PCI_PERR#		D34	PCI_STOP#
C35	PCI_LOCK#		D35	PCI_TRDY#
C36	PCI_DEVSEL#		D36	PCI_FRAME#
C37	PCI_IRDY#		D37	PCI_AD16
C38	PCI_C/BE2#		D38	PCI_AD18
C39	PCI_AD17		D39	PCI_AD20
C40	PCI_AD19		D40	PCI_AD22
C41	GND (FIXED)		D41	GND (FIXED)
C42	PCI_AD21		D42	PCI_AD24
C43	PCI_AD23		D43	PCI_AD26
C44	PCI_C/BE3#		D44	PCI_AD28
C45	PCI_AD25		D45	PCI_AD30
C46	PCI_AD27		D46	PCI_IRQC#
C47	PCI_AD29		D47	PCI_IRQD#
C48	PCI_AD31		D48	PCI_CLKRUN#
C49	PCI_IRQA#		D49	NC
C50	PCI_IRQB#		D50	PCI_CLK

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Row A			Row B	
Pin No.	Pin Name		Pin No.	Pin Name
A51	GND (FIXED)		B51	GND (FIXED)
A52	PCIE_TX5+ (1)		B52	PCIE_RX5+ (1)
A53	PCIE_TX5- (1)		B53	PCIE_RX5- (1)
A54	GPI0		B54	GPO1
A55	PCIE_TX4+		B55	PCIE_RX4+
A56	PCIE_TX4-		B56	PCIE_RX4-
A57	GND		B57	GPO2
A58	PCIE_TX3+		B58	PCIE_RX3+
A59	PCIE_TX3-		B59	PCIE_RX3-
A60	GND (FIXED)		B60	GND (FIXED)
A61	PCIE_TX2+		B61	PCIE_RX2+
A62	PCIE_TX2-		B62	PCIE_RX2-
A63	GPI1		B63	GPO3
A64	PCIE_TX1+		B64	PCIE_RX1+
A65	PCIE_TX1-		B65	PCIE_RX1-
A66	GND		B66	WAKE0#
A67	GPI2		B67	WAKE1#
A68	PCIE_TX0+		B68	PCIE_RX0+
A69	PCIE_TX0-		B69	PCIE_RX0-
A70	GND (FIXED)		B70	GND (FIXED)
A71	LVDS_A0+		B71	LVDS_B0+
A72	LVDS_A0-		B72	LVDS_B0-
A73	LVDS_A1+		B73	LVDS_B1+
A74	LVDS_A1-		B74	LVDS_B1-
A75	LVDS_A2+		B75	LVDS_B2+
A76	LVDS_A2-		B76	LVDS_B2-
A77	LVDS_VDD_EN		B77	LVDS_B3+
A78	LVDS_A3+		B78	LVDS_B3-
A79	LVDS_A3-		B79	LVDS_BKLT_EN
A80	GND (FIXED)		B80	GND (FIXED)
A81	LVDS_A_CK+		B81	LVDS_B_CK+
A82	LVDS_A_CK-		B82	LVDS_B_CK-
A83	LVDS_I2C_CK		B83	LVDS_BKLT_CTRL
A84	LVDS_I2C_DAT		B84	VCC_5V_SBY
A85	GPI3		B85	VCC_5V_SBY
A86	KBD_RST#		B86	VCC_5V_SBY
A87	KBD_A20GATE		B87	VCC_5V_SBY
A88	PCIE0_CK_REF+		B88	RSVD
A89	PCIE0_CK_REF-		B89	VGA_RED
A90	GND (FIXED)		B90	GND (FIXED)
A91	RSVD		B91	VGA_GRN
A92	RSVD		B92	VGA_BLU
A93	GPO0		B93	VGA_HSYNC
A94	RSVD		B94	VGA_VSYNC
A95	RSVD		B95	VGA_I2C_CK
A96	GND		B96	VGA_I2C_DAT
A97	VCC_12V		B97	TV_DAC_A
A98	VCC_12V		B98	TV_DAC_B
A99	VCC_12V		B99	TV_DAC_C
A100	GND (FIXED)		B100	GND (FIXED)
A101	VCC_12V		B101	VCC_12V
A102	VCC_12V		B102	VCC_12V
A103	VCC_12V		B103	VCC_12V
A104	VCC_12V		B104	VCC_12V
A105	VCC_12V		B105	VCC_12V
A106	VCC_12V		B106	VCC_12V
A107	VCC_12V		B107	VCC_12V
A108	VCC_12V		B108	VCC_12V
A109	VCC_12V		B109	VCC_12V
A110	GND (FIXED)		B110	GND (FIXED)

Row C			Row D	
Pin No.	Pin Name		Pin No.	Pin Name
C51	GND (FIXED)		D51	GND (FIXED)
C52	PEG_RX0+		D52	PEG_TX0+
C53	PEG_RX0-		D53	PEG_TX0-
C54	TYPE0#		D54	PEG_LANE_RV#
C55	PEG_RX1+		D55	PEG_TX1+
C56	PEG_RX1-		D56	PEG_TX1-
C57	TYPE1#		D57	TYPE2#
C58	PEG_RX2+		D58	PEG_TX2+
C59	PEG_RX2-		D59	PEG_TX2-
C60	GND (FIXED)		D60	GND (FIXED)
C61	PEG_RX3+		D61	PEG_TX3+
C62	PEG_RX3-		D62	PEG_TX3-
C63	RSVD		D63	DDPC_CTRLCLK
C64	RSVD		D64	DDPC_CTRLDATA
C65	PEG_RX4+		D65	PEG_TX4+
C66	PEG_RX4-		D66	PEG_TX4-
C67	RSVD (1)		D67	GND
C68	PEG_RX5+		D68	PEG_TX5+
C69	PEG_RX5-		D69	PEG_TX5-
C70	GND (FIXED)		D70	GND (FIXED)
C71	PEG_RX6+		D71	PEG_TX6+
C72	PEG_RX6-		D72	PEG_TX6-
C73	SDVO_DATA		D73	SDVO_CLK
C74	PEG_RX7+		D74	PEG_TX7+
C75	PEG_RX7-		D75	PEG_TX7-
C76	GND		D76	GND
C77	RSVD		D77	IDE_CBLID#
C78	PEG_RX8+		D78	PEG_TX8+
C79	PEG_RX8-		D79	PEG_TX8-
C80	GND (FIXED)		D80	GND (FIXED)
C81	PEG_RX9+		D81	PEG_TX9+
C82	PEG_RX9-		D82	PEG_TX9-
C83	RSVD		D83	MCH_CFG_20
C84	GND		D84	GND
C85	PEG_RX10+		D85	PEG_TX10+
C86	PEG_RX10-		D86	PEG_TX10-
C87	GND		D87	GND
C88	PEG_RX11+		D88	PEG_TX11+
C89	PEG_RX11-		D89	PEG_TX11-
C90	GND (FIXED)		D90	GND (FIXED)
C91	PEG_RX12+		D91	PEG_TX12+
C92	PEG_RX12-		D92	PEG_TX12-
C93	GND		D93	GND
C94	PEG_RX13+		D94	PEG_TX13+
C95	PEG_RX13-		D95	PEG_TX13-
C96	GND		D96	GND
C97	RSVD		D97	PEG_ENABLE#
C98	PEG_RX14+		D98	PEG_TX14+
C99	PEG_RX14-		D99	PEG_TX14-
C100	GND (FIXED)		D100	GND (FIXED)
C101	PEG_RX15+		D101	PEG_TX15+
C102	PEG_RX15-		D102	PEG_TX15-
C103	GND		D103	GND
C104	VCC_12V		D104	VCC_12V
C105	VCC_12V		D105	VCC_12V
C106	VCC_12V		D106	VCC_12V
C107	VCC_12V		D107	VCC_12V
C108	VCC_12V		D108	VCC_12V
C109	VCC_12V		D109	VCC_12V
C110	GND (FIXED)		D110	GND (FIXED)

NOTE:

(1) The 6th PCI Express x1 port (PCIE5) is occupied by the onboard LAN controller. For six PCI Express x1 port support from the Express-MG, please contact ADLINK for the no onboard LAN version.
(2) The 4th SATA port (SATA3) is occupied by the onboard SATA/PATA bridge. For 4x SATA port support from the Express-MG, please contact ADLINK for the four SATA port version.

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5.4 Signal Descriptions

Row A

Pin	Signal	Description	Type	PU/PD	Comment
A1	GND	Ground	PWR	-	-
A2	GBE0_MDI3-	Ethernet Media Dependent Interface -	I/O - DP	-	-
A3	GBE0_MDI3+	Ethernet Media Dependent Interface +	I/O - DP	-	-
A4	GBE0_LINK100#	Ethernet Speed LED (100Mb)	OD	-	On at 100Mb/s
A5	GBE0_LINK1000#	Ethernet Speed LED (1000Mb)	OD	-	On at 1000Mb/s
A6	GBE0_MDI2-	Ethernet Media Dependent Interface -	I/O - DP	-	-
A7	GBE0_MDI2+	Ethernet Media Dependent Interface +	I/O - DP	-	-
A8	GBE0_LINK#	LAN Link LED	O-3.3		-
A9	GBE0_MDI1-	Ethernet Media Dependent Interface -	I/O - DP	-	-
A10	GBE0_MDI1+	Ethernet Media Dependent Interface +	I/O - DP	-	-
A11	GND	Ground	PWR	-	-
A12	GBE0_MDI0-	Ethernet Media Dependent Interface -	I/O - DP	-	-
A13	GBE0_MDI0+	Ethernet Media Dependent Interface +	I/O - DP	-	-
A14	GBE0_CTREF	ETHCTREF	O-1,8	-	-
A15	SUS_S3#	PM_SLP_S#3	O-3.3	-	-
A16	SATA0_TX+	SATA0_TX+ | SATA 0 Transmit Data +	O - DP	-	-
A17	SATA0_TX-	SATA0_TX- | SATA 0 Transmit Data -	O - DP	-	-
A18	SUS_S4#	PM_SLP_S#4	O-3.3	-	-
A19	SATA0_RX+	SATA0_RX+ | SATA 0 Receive Data +	I - DP	-	-
A20	SATA0_RX-	SATA0_RX - | SATA 0 Receive Data -	I - DP	-	-
A21	GND	Ground	PWR	-	-
A22	SATA2_TX+	SATA2_TX+ | SATA 2 Transmit Data +	O - DP	-	-
A23	SATA2_TX-	SATA2_TX- | SATA 2 Transmit Data -	O - DP	-	-
A24	SUS_S5#	PM_SLP_S#5	O-3.3	-	-
A25	SATA2_RX+	SATA2_RX+ | SATA 2 Receive Data +	I - DP	-	-
A26	SATA2_RX-	SATA2_RX- | SATA 2 Receive Data -	I - DP	-	-
A27	BATLOW#	PM_BATLOW# | Battery Low	I-3.3	PU 8k2 3.3Vsb	-
A28	ATA_ACT#	ATA_LED# | SATA LED	O-3.3	PU 10k 3.3V	int. PU 15k in ICH9
A29	AC_SYNC	AC_SYNC | AC'97 Sync	O-3.3	-	int. PD 20k in ICH9
A30	AC_RST#	AC_RST# | AC'97 Reset	O-3.3	-	int. PD 20k in ICH9
A31	GND	Ground	PWR	-	
A32	AC_BITCLK	AC_BITCLK | AC'97 Clock	O-3.3	-	int. PD 20k in ICH9
A33	AC_SDOUT	AC_SDATAOUT | AC'97 Data	O-3.3	-	int. PD 20k in ICH9
A34	BIOS_DISABLE#	BIOS_DISABLE#	I-3.3	PU 10k 3.3V	-
A35	THRMTRIP#	PM_THRMTRIP#_CON	O-3.3	PU 10k 3.3V	-
A36	USB6-	USB_PN6 | USB Data – Port6	I/O - DP	-	int. PD 15k in ICH9
A37	USB6+	USB_PP6 | USB Data + Port6	I/O - DP	-	int. PD 15k in ICH9
A38	USB_6_7_OC#	USB_OC#_6_7 | USB OverCurrent Port 6/7	I-3.3	PU 10k 3.3Vsb	-
A39	USB4-	USB_PN4 | USB Data - Port4	I/O - DP	-	int. PD 15k in ICH9
A40	USB4+	USB_PP4 | USB Data + Port4	I/O - DP	-	int. PD 15k in ICH9
A41	GND	Ground	PWR	-	-
A42	USB2-	USB_PN2 | USB Data - Port2	I/O - DP	-	int. PD 15k in ICH9
A43	USB2+	USB_PP2 | USB Data + Port2	I/O - DP	-	int. PD 15k in ICH9
A44	USB_2_3_OC#	USB_OC#_2_3 | USB OverCurrent Port 2/3	I-3.3	PU 10k 3.3Vsb	
A45	USB0-	USB_PN0 | USB Data - Port0	I/O - DP	-	int. PD 15k in ICH9
A46	USB0+	USB_PP0 | USB Data + Port0	I/O - DP	-	int. PD 15k in ICH9
A47	VCC_RTC	V_BAT	PWR	-	-
A48	EXCD0_PERST#	Express Card Support [0]]card reset	O-3.3	PU 10k 3.3Vsb	-
A49	EXCD0_CPPE#	Express Card Support [0]] capable c. request	I-3.3	PU 10k 3.3V	-
A50	LPC_SERIRQ	INT_SERIRQ | Serial Interrupt Request	IO-3.3	PU 8k2 3.3V	-
A51	GND	Ground	PWR	-	-
A52	PCIE5_TX+	BOM option (LAN on PCIe 5)	NC	-	Optional : O - DP
A53	PCIE5_TX-	BOM option (LAN on PCIe 5)	NC	-	Optional : O - DP
A54	GPI0	General Purpose Input 0	I-3.3	PU 10k 3.3Vsb	-
A55	PCIE4_TX+	PCI Express 4 Transmit +	O - DP	-	-

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Signal Descriptions (cont'd)

Row A

Pin	Signal	Description	Type	PU/PD	Comment
A56	PCIE4_TX-	PCI Express 4 Transmit -	O - DP	-	-
A57	GND	Ground	PWR	-	-
A58	PCIE3_TX+	PCI Express 3 Transmit +	O - DP	-	-
A59	PCIE3_TX-	PCI Express 3 Transmit -	O - DP	-	-
A60	GND	Ground	PWR	-	-
A61	PCIE2_TX+	PCI Express 2 Transmit +	O - DP	-	-
A62	PCIE2_TX-	PCI Express 2 Transmit -	O - DP	-	-
A63	GPI1	General Purpose Input 1	I-3.3	PU 10k 3.3Vsb	-
A64	PCIE1_TX+	PCI Express 1 Transmit +	O - DP	-	-
A65	PCIE1_TX-	PCI Express 1 Transmit -	O - DP	-	-
A66	GND	Ground	PWR	-	-
A67	GPI2	General Purpose Input 2	I-3.3	PU 10k 3.3Vsb	-
A68	PCIE0_TX+	PCI Express 0 +	O - DP	-	-
A69	PCIE0_TX-	PCI Express 0 -	O - DP	-	-
A70	GND	Ground	PWR	-	-
A71	LVDS_A0+	LVDS_AP0 | LVDS Channel A	O - DP	-	-
A72	LVDS_A0-	LVDS_AN0 | LVDS Channel A	O - DP	-	-
A73	LVDS_A1+	LVDS_AP1 | LVDS Channel A	O - DP	-	-
A74	LVDS_A1-	LVDS_AN1 | LVDS Channel A	O - DP	-	-
A75	LVDS_A2+	LVDS_AP2 | LVDS Channel A	O - DP	-	-
A76	LVDS_A2-	LVDS_AN2 | LVDS Channel A	O - DP	-	-
A77	LVDS_VDD_EN	LVDS_VDDEN | LVDS Panel Power	O-2,5	PD 100k	-
A78	LVDS_A3+	LVDS_AP3 | LVDS Channel A	O - DP	-	-
A79	LVDS_A3-	LVDS_AN3 | LVDS Channel A	O - DP	-	-
A80	GND	Ground	PWR	-	-
A81	LVDS_A_CK+	LVDS_CLKAP | LVDS Channel A	O - DP	-	-
A82	LVDS_A_CK-	LVDS_CLKAN | LVDS Channel A	O - DP	-	-
A83	LVDS_I2C_CK	LVDS_DDCPCLK | JILI I2C Clock	IO-3.3	PU 10k 3.3V	-
A84	LVDS_I2C_DAT	LVDS_DDCPDATA | JILI I2C Data	IO-3.3	PU 10k 3.3V	-
A85	GPI3	General Purpose Input 3	I-3.3	PU 10k 3.3Vsb	-
A86	KBD_RST#	H_RCIN# | Keyboard Reset	I-3.3	PU 10k 3.3V	-
A87	KBD_A20GATE	H_A20GATE	I-3.3	PU 8k2 3.3V	-
A88	PCIE_CK_REF+	CLK_PCIE_REF P	O - DP	-	-
A89	PCIE_CK_REF-	CLK_PCIE_REF N	O - DP	-	-
A90	GND	Ground	PWR	-	-
A91	RSVD		NC	-	-
A92	RSVD		NC	-	-
A93	GPO0	General Purpose Output 0	O-3.3	PU 10k 3.3Vsb	-
A94	RSVD		NC	-	-
A95	RSVD		NC	-	-
A96	GND	Ground	PWR	-	-
A97	VCC_12V	Power 12V	PWR	-	-
A98	VCC_12V	Power 12V	PWR	-	-
A99	VCC_12V	Power 12V	PWR	-	-
A100	GND	Ground	PWR	-	-
A101	VCC_12V	Power 12V	PWR	-	-
A102	VCC_12V	Power 12V	PWR	-	-
A103	VCC_12V	Power 12V	PWR	-	-
A104	VCC_12V	Power 12V	PWR	-	-
A105	VCC_12V	Power 12V	PWR	-	-
A106	VCC_12V	Power 12V	PWR	-	-
A107	VCC_12V	Power 12V	PWR	-	-
A108	VCC_12V	Power 12V	PWR	-	-
A109	VCC_12V	Power 12V	PWR	-	-
A110	GND	Ground	PWR	-	-

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Signal Descriptions (cont'd)

Row B

Pin	Signal	Description	Type	PU/PD	Comment
B1	GND	Ground	PWR	-	-
B2	GBE0_ACT#	LAN_ACTLED# | Ethernet Activity LED	OD	PU 1k 3.3V	-
B3	LPC_FRAME#	LPC_FRAME# | LPC Frame Indicator	O-3.3	-	-
B4	LPC_AD0	LPC_AD0 | LPC Adress & DATA Bus	IO-3.3	-	int. PU 20k in ICH9
B5	LPC_AD1	LPC_AD1 | LPC Adress & DATA Bus	IO-3.3	-	int. PU 20k in ICH9
B6	LPC_AD2	LPC_AD2 | LPC Adress & DATA Bus	IO-3.3	-	int. PU 20k in ICH9
B7	LPC_AD3	LPC_AD3 | LPC Adress & DATA Bus	IO-3.3	-	int. PU 20k in ICH9
B8	LPC_DRQ0#	SIO_DRQ#0 | LPC Serial DMA Request 0	I-3.3	-	int. PU 20k in ICH9
B9	LPC_DRQ1#	SIO_DRQ#1 | LPC Serial DMA Request 1	I-3.3	-	int. PU 20k in ICH9
B10	LPC_CLK	CLK_SIOEXTPCI	O-3.3	-	-
B11	GND	Ground	I-3.3	-	-
B12	PWRBTN#	Power Button	I-5	PU 10k 3.3Vsb	-
B13	SMB_CK	SMBUS Clock	O-3.3	PU 1k2 3.3V	-
B14	SMB_DAT	SMBUS Data	IO-3.3	PU 1k2 3.3V	-
B15	SMB_ALERT#	SMB_ALERT#	I-3.3	PU 10k 3.3Vsb	-
B16	SATA1_TX+	SATA1_TX+ | SATA 1 Transmit Data +	O - DP	-	-
B17	SATA1_TX-	SATA1_TX- | SATA 1 Transmit Data -	O - DP	-	-
B18	SUS_STAT#	PM_SUS_STAT#	O-3.3	-	-
B19	SATA1_RX+	SATA1_RX+ | SATA 1 Receive Data +	I - DP	-	-
B20	SATA1_RX-	SATA1_RX - | SATA 1 Receive Data -	I - DP	-	-
B21	GND	Ground	PWR	-	-
B22	SATA3_TX+	BOM option (PATA bridge on SATA3)	NC	-	Optional : O - DP
B23	SATA3_TX-	BOM option (PATA bridge on SATA3)	NC	-	Optional : O - DP
B24	PWR_OK	Power OK	I,3.3	PU 10k 3.3V	-
B25	SATA3_RX+	BOM option (PATA bridge on SATA3)	NC	-	Optional : I - DP
B26	SATA3_RX-	BOM option (PATA bridge on SATA3)	NC	-	Optional : I - DP
B27	WDT	Watch Dog Timer	O-3.3		-
B28	AC_SDIN2	AC_SDATAIN2	I-3.3	-	int. PD 20k in ICH9
B29	AC_SDIN1	AC_SDATAIN1	I-3.3	-	int. PD 20k in ICH9
B30	AC_SDIN0	AC_SDATAIN0	I-3.3	-	int. PD 20k in ICH9
B31	GND	Ground	PWR	-	
B32	SPKR	AC_SPKR	O-3.3	-	int. PD 20k in ICH9
B33	I2C_CK	I2CLK	O-3.3	PU 10k 3.3V	-
B34	I2C_DAT	I2DAT	IO-3.3	PU 10k 3.3V	-
B35	THRM#	PM THRM# CON | Over Temperature	I-3.3	PU 8k2 3.3V	-
B36	USB7-	USB_PN7 | USB Data – Port7	I/O - DP	-	int. PD 15k in ICH9
B37	USB7+	USB_PP7 | USB Data + Port7	I/O - DP	-	int. PD 15k in ICH9
B38	USB_4_5_OC#	USB_OC#_4_5 | USB OverCurrent Port	I-3.3	PU 10k 3.3Vsb	
B39	USB5-	USB_PN5 | USB Data- Port5	I/O - DP	-	int. PD 15k in ICH9
B40	USB5+	USB_PP5 | USB Data+ Port5	I/O - DP	-	int. PD 15k in ICH9
B41	GND	Ground	I-3.3	-	-
B42	USB3-	USB_PN3 | USB Data- Port3	I/O - DP	-	int. PD 15k in ICH9
B43	USB3+	USB_PP3 | USB Data+ Port3	I/O - DP	-	int. PD 15k in ICH9
B44	USB_0_1_OC#	USB_OC#_0_1 | USB OverCurrent Port	I-3.3	PU 10k 3.3Vsb	-
B45	USB1-	USB_PN1 | USB Data- Port1	I/O - DP	-	int. PD 15k in ICH9
B46	USB1+	USB_PP1 | USB Data+ Port1	I/O - DP	-	int. PD 15k in ICH9
B47	EXCD1_PERST#	Express Card Support [1]|card reset	O-3.3	PU 10k 3.3Vsb	-
B48	EXCD1_CPPE#	Express Card Support [1]| capable c.	I-3.3	PU 10k 3.3V	-
B49	SYS_RESET#	ETX_SYS_RESET# | Reset Input	I-3.3	PU 10k 3.3Vsb	-
B50	CB_RESET#	PCI_RST# | PCI Bus Reset	O-3.3	-	-
B51	GND	Ground	PWR	-	-
B52	PCIE5_RX+	BOM option (LAN on PCIe 5)	NC	-	Optional: I - DP
B53	PCIE5_RX-	BOM option (LAN on PCIe 5)	NC	-	Optional: I - DP
B54	GPO1	General Purpose Output 1	O-3.3	PU 10k 3.3Vsb	-
B55	PCIE4_RX+	PCI Express 4 Recieve +	I - DP	-	-

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Signal Descriptions (cont'd)

Row B

Pin	Signal	Description	Type	PU/PD	Comment
B56	PCIE4_RX-	PCI Express 4 Receive -	I - DP	-	-
B57	GPO2	General Purpose Output 2	O-3.3	PU 10k 3.3Vsb	-
B58	PCIE3_RX+	PCI Express 3 Recieve +	I - DP	-	-
B59	PCIE3_RX-	PCI Express 3 Receive -	I - DP	-	-
B60	GND	Ground	PWR	-	-
B61	PCIE2_RX+	PCI Express 2 Receive +	I - DP	-	-
B62	PCIE2_RX-	PCI Express 2 Receive -	I - DP	-	-
B63	GPO3	General Purpose Output 3	O-3.3	PU 10k 3.3Vsb	-
B64	PCIE1_RX+	PCI Express 1 Receive +	I - DP	-	-
B65	PCIE1_RX-	PCI Express 1 Receive -	I - DP	-	-
B66	WAKE0#	PCIE_WAKEI#	I-3.3	PU 1k 3.3Vsb	-
B67	WAKE1#	WAKE1#	I-3.3	PU 10k 3.3Vsb	-
B68	PCIE0_RX+	PCI Express 0 Receive +	I - DP	-	-
B69	PCIE0_RX-	PCI Express 0 Receive -	I - DP	-	-
B70	GND	Ground	PWR	-	-
B71	LVDS_B0+	LVDS_BP0 | LVDS Channel B Data0+	O - DP	-	-
B72	LVDS_B0-	LVDS_BN0 | LVDS Channel B Data0-	O - DP	-	-
B73	LVDS_B1+	LVDS_BP1 | LVDS Channel B Data1+	O - DP	-	-
B74	LVDS_B1-	LVDS_BN1 | LVDS Channel B Data1-	O - DP	-	-
B75	LVDS_B2+	LVDS_BP2 | LVDS Channel B Data2+	O - DP	-	-
B76	LVDS_B2-	LVDS_BN2 | LVDS Channel B Data2-	O - DP	-	-
B77	LVDS_B3+	LVDS_BP3 | LVDS Channel B Data3+	O - DP	-	-
B78	LVDS_B3-	LVDS_BN3 | LVDS Channel B Data3-	O - DP	-	-
B79	LVDS_BKLT_EN	LVDS Panel Backlight Enable	O-3.3	PD 100k	-
B80	GND	Ground	PWR	-	-
B81	LVDS_B_CK+	LVDS_CLKBP | LVDS Channel B	O - DP	-	-
B82	LVDS_B_CK-	LVDS_CLKBM | LVDS Channel B	O - DP	-	-
B83	LVDS_BKLT_CTRL	Backlight Brightness	O-3.3	PD 100k	-
B84	VCC_5V_SBY	5V Standby	PWR	-	-
B85	VCC_5V_SBY	5V Standby	PWR	-	-
B86	VCC_5V_SBY	5V Standby	PWR	-	-
B87	VCC_5V_SBY	5V Standby	PWR	-	-
B88	RSVD	NC	NC	-	-
B89	VGA_RED	Analog Video RGB-RED	OA	PD 150R	-
B90	GND	Ground	PWR	-	-
B91	VGA_GRN	Analog Video RGB-GREEN	OA	PD 150R	-
B92	VGA_BLU	Analog Video RGB-BLUE	OA	PD 150R	-
B93	VGA_HSYNC	Analog Video H-Sync	O-3.3	-	-
B94	VGA_VSYNC	Analog Video V-Sync	O-3.3	-	-
B95	VGA_I2C_CK	Display Data Channel - Clock	O-3.3	PU 2k2 3.3V	-
B96	VGA_I2C_DAT	Display Data Channel - Data	IO-3.3	PU 2k2 3.3V	-
B97	TV_DAC_A	Composite CVBS	OA	PD 150R	-
B98	TV_DAC_B	TV Luminance Signal	OA	PD 150R	-
B99	TV_DAC_C	TV Chrominance Signal	OA	PD 150R	-
B100	GND	Ground	PWR	-	-
B101	VCC_12V	Power 12V	PWR	-	-
B102	VCC_12V	Power 12V	PWR	-	-
B103	VCC_12V	Power 12V	PWR	-	-
B104	VCC_12V	Power 12V	PWR	-	-
B105	VCC_12V	Power 12V	PWR	-	-
B106	VCC_12V	Power 12V	PWR	-	-
B107	VCC_12V	Power 12V	PWR	-	-
B108	VCC_12V	Power 12V	PWR	-	-
B109	VCC_12V	Power 12V	PWR	-	-
B110	GND	Ground	PWR	-	-

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Signal Descriptions (cont'd)

Row C

Pin	Signal	Description	Type	PU/PD	Comment
C1	GND	Ground	PWR	-	-
C2	IDE_D7	IDE Data Bus	IO	PD 10k	-
C3	IDE_D6	IDE Data Bus	IO	-	-
C4	IDE_D3	IDE Data Bus	IO	-	-
C5	IDE_D15	IDE Data Bus	IO	-	-
C6	IDE_D8	IDE Data Bus	IO	-	-
C7	IDE_D9	IDE Data Bus	IO	-	-
C8	IDE_D2	IDE Data Bus	IO	-	-
C9	IDE_D13	IDE Data Bus	IO	-	-
C10	IDE_D1	IDE Data Bus	IO	-	-
C11	GND	Ground	PWR	-	-
C12	IDE_D14	IDE Data Bus	IO	-	-
C13	IDE_IORDY	IDE I/O Ready	I-3.3	PU 4K7 3.3V	-
C14	IDE_IOR#	I/O read line to IDE device	O-3.3		-
C15	PCI_PME#	PCI Power Management Event	IO-3.3		int. PU 20k in ICH9
C16	PCI_GNT2#	PCI Bus Grant 2	O-3.3		int. PU 20k in ICH9
C17	PCI_REQ2#	PCI Bus Request 2	I-3.3	PU 8K2 3.3V	-
C18	PCI_GNT1#	PCI Bus Grant 1	O-3.3		int. PU 20k in ICH9
C19	PCI_REQ1#	PCI Bus Request 1	I-3.3	PU 8K2 3.3V	-
C20	PCI_GNT0#	PCI Bus Grant 0	O-3.3		int. PU 20k in ICH9
C21	GND	Ground	PWR		-
C22	PCI_REQ0#	PCI Bus Reqest 0	I-3.3	PU 8K2 3.3V	-
C23	PCI_RESET#	PCI Bus Reset	O-3.3	-	-
C24	PCI_AD0	PCI Adress & Data Bus line	IO-3.3	-	-
C25	PCI_AD2	PCI Adress & Data Bus line	IO-3.3	-	-
C26	PCI_AD4	PCI Adress & Data Bus line	IO-3.3	-	-
C27	PCI_AD6	PCI Adress & Data Bus line	IO-3.3	-	-
C28	PCI_AD8	PCI Adress & Data Bus line	IO-3.3	-	-
C29	PCI_AD10	PCI Adress & Data Bus line	IO-3.3	-	-
C30	PCI_AD12	PCI Adress & Data Bus line	IO-3.3	-	-
C31	GND	Ground	PWR	-	-
C32	PCI_AD14	PCI Adress & Data Bus line	IO-3.3	-	-
C33	PCI_C/BE1#	PCI Bus Command and Byte enables	IO-3.3	-	-
C34	PCI_PERR#	PCI Bus Grant Error	IO-3.3	PU 8K2 3.3V	-
C35	PCI_LOCK#	PCI Bus Lock	IO-3.3	PU 8K2 3.3V	-
C36	PCI_DEVSEL#	PCI Bus Device Select	IO-3.3	PU 8K2 3.3V	-
C37	PCI_IRDY#	PCI Bus Bus Initiator Ready	IO-3.3	PU 8K2 3.3V	-
C38	PCI_C/BE2#	PCI Bus Command and Byte enables	IO-3.3		-
C39	PCI_AD17	PCI Adress & Data Bus line	IO-3.3	-	-
C40	PCI_AD19	PCI Adress & Data Bus line	IO-3.3	-	-
C41	GND	Ground	PWR	-	-
C42	PCI_AD21	PCI Adress & Data Bus line	IO-3.3	-	-
C43	PCI_AD23	PCI Adress & Data Bus line	IO-3.3	-	-
C44	PCI_C/BE3#	PCI Bus Command and Byte enables	IO-3.3	-	-
C45	PCI_AD25	PCI Adress & Data Bus line	IO-3.3	-	-
C46	PCI_AD27	PCI Adress & Data Bus line	IO-3.3	-	-
C47	PCI_AD29	PCI Adress & Data Bus line	IO-3.3	-	-
C48	PCI_AD31	PCI Adress & Data Bus line	IO-3.3		-
C49	PCI_IRQA#	PCI Bus Interrupt Request A	I-3.3	PU 8K2 3.3V	-
C50	PCI_IRQB#	PCI Bus Interrupt Request B	I-3.3	PU 8K2 3.3V	-
C51	GND	Ground	PWR		-
C52	PEG_RX0+	PCIe 0 Recieve + / SDVO TV clock +	I - DP		both modes supported
C53	PEG_RX0-	PCIe 0 Recieve - / SDVO TV clock -	I - DP	-	both modes supported
C54	TYPE0#	Module type ID pin 0	STO	-	not connected
C55	PEG_RX1+	PCIe 1 Recieve + / SDVO B Interrupt +	I - DP	-	both modes supported

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Signal Descriptions (cont'd)

Row C

Pin	Signal	Description	Type	PU/PD	Comment
C56	PEG_RX1-	PCIe 1 Recieve - / SDVO B interrupt -	I - DP	-	both modes supported
C57	TYPE1#	Module type ID pin 1	STO	-	not connected
C58	PEG_RX2+	PCIe 2 Recieve + / SDVO Field stall +	I - DP	-	both modes supported
C59	PEG_RX2-	PCIe 2 Recieve - / SDVO Field stall -	I - DP	-	both modes supported
C60	GND	Ground	PWR	-	-
C61	PEG_RX3+	PCIe 3 Recieve +	I - DP	-	-
C62	PEG_RX3-	PCIe 3 Recieve -	I - DP	-	-
C63	RSVD	Rx from Board Controller	I-3.3	-	-
C64	RSVD	Tx from Board Controller	O-3.3	-	-
C65	PEG_RX4+	PCIe 4 Recieve +	I - DP	-	-
C66	PEG_RX4-	PCIe 4 Recieve -	I - DP	-	-
C67	RSVD	FAN_PWM_CTRL	0-5	-	-
C68	PEG_RX5+	PCIe 5 Recieve + / SDVO C Interrupt +	I - DP	-	both modes supported
C69	PEG_RX5-	PCIe 5 Recieve - / SDVO C interrupt -	I - DP	-	both modes supported
C70	GND	Ground	PWR	-	-
C71	PEG_RX6+	PCIe 6 Recieve +	I - DP	-	-
C72	PEG_RX6-	PCIe 6 Recieve -	I - DP	-	-
C73	SDVO_DATA	SDVO_CTRLDATA	IO-2,5	-	-
C74	PEG_RX7+	PCIe 7 Recieve +	I - DP	-	-
C75	PEG_RX7-	PCIe 7 Recieve -	I - DP	-	-
C76	GND	Ground	PWR	-	-
C77	RSVD	FAN_TACH	I-5	-	-
C78	PEG_RX8+	PCIe 8 Recieve +	I - DP	-	-
C79	PEG_RX8-	PCIe 8 Recieve -	I - DP	-	-
C80	GND	Ground	PWR	-	-
C81	PEG_RX9+	PCIe 9 Recieve +	I - DP	-	-
C82	PEG_RX9-	PCIe 9 Recieve -	I - DP	-	-
C83	RSVD	Physical Presence	I-3.3	PU 10k 3.3Vsb	-
C84	GND	Ground	PWR	-	-
C85	PEG_RX10+	PCIe 10 Recieve +	I - DP	-	-
C86	PEG_RX10-	PCIe 10 Recieve -	I - DP	-	-
C87	GND	Ground	PWR	-	-
C88	PEG_RX11+	PCIe 11 Recieve +	I - DP	-	-
C89	PEG_RX11-	PCIe 11 Recieve –	I - DP	-	-
C90	GND	Ground	PWR	-	-
C91	PEG_RX12+	PCIe 12 Recieve +	I - DP	-	-
C92	PEG_RX12-	PCIe 12 Recieve -	I - DP	-	-
C93	GND	Ground	PWR	-	-
C94	PEG_RX13+	PCIe 13 Recieve +	I - DP	-	-
C95	PEG_RX13-	PCIe 13 Recieve -	I - DP	-	-
C96	GND	Ground	PWR	-	-
C97	RSVD	NC	NC	-	-
C98	PEG_RX14+	PCIe 14 Recieve +	I - DP	-	-
C99	PEG_RX14-	PCIe 14 Recieve -	I - DP	-	-
C100	GND	Ground	PWR	-	-
C101	PEG_RX15+	PCIe 15 Recieve +	I - DP	-	-
C102	PEG_RX15-	PCIe 15 Recieve -	I - DP	-	-
C103	GND	Ground	PWR	-	-
C104	VCC_12V	Power 12V	PWR	-	-
C105	VCC_12V	Power 12V	PWR	-	-
C106	VCC_12V	Power 12V	PWR	-	-
C107	VCC_12V	Power 12V	PWR	-	-
C108	VCC_12V	Power 12V	PWR	-	-
C109	VCC_12V	Power 12V	PWR	-	-
C110	GND	Ground	PWR	-	-

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Signal Descriptions (cont'd)

Row D

Pin	Signal	Description	Type	PU/PD	Comment
D1	GND	Ground	PWR	-	-
D2	IDE_D5	IDE Data Bus	IO	-	-
D3	IDE_D10	IDE Data Bus	IO	-	-
D4	IDE_D11	IDE Data Bus	IO	-	-
D5	IDE_D12	IDE Data Bus	IO	-	-
D6	IDE_D4	IDE Data Bus	IO	-	-
D7	IDE_D0	IDE Data Bus	IO	-	-
D8	IDE_REQ#	IDE Device DMA Request.	IO	PD 5k6	int. PD 11.5k in ICH9
D9	IDE_IOW#	IDE IO Write	O-3.3	-	-
D10	IDE_ACK#	IDE DMA Acknowledge	O-3.3	-	-
D11	GND	Ground	PWR	-	-
D12	IDE_IRQ	IDE Interrupt Request	I-3.3	PD 10k	-
D13	IDE_A0	IDE Adress Bus	O-3.3	-	-
D14	IDE_A1	IDE Adress Bus	O-3.3	-	-
D15	IDE_A2	IDE Adress Bus	O-3.3	-	-
D16	IDE_CS1#	IDE Chip Select for 1F0h to 1FFh range	O-3.3	-	-
D17	IDE_CS3#	IDE Chip Select for 3F0h to 3FFh range	O-3.3	-	-
D18	IDE_RESET#	IDE Reset Output to Device	O-3.3	-	-
D19	PCI_GNT3#	PCI Bus Grant 3	O-3.3	-	int. PU 20k in ICH9
D20	PCI_REQ3#	PCI Bus Reqest 3	I-3.3	PU 8K2 3.3V	-
D21	GND	Ground	PWR	-	-
D22	PCI_AD1	PCI Adress & Data Bus line	IO-3.3	-	-
D23	PCI_AD3	PCI Adress & Data Bus line	IO-3.3	-	-
D24	PCI_AD5	PCI Adress & Data Bus line	IO-3.3	-	-
D25	PCI_AD7	PCI Adress & Data Bus line	IO-3.3	-	-
D26	PCI_C/BE0#	PCI Bus Command and Byte enables 0	IO-3.3	-	-
D27	PCI_AD9	PCI Adress & Data Bus line	IO-3.3	-	-
D28	PCI_AD11	PCI Adress & Data Bus line	IO-3.3	-	-
D29	PCI_AD13	PCI Adress & Data Bus line	IO-3.3	-	-
D30	PCI_AD15	PCI Adress & Data Bus line	IO-3.3	-	-
D31	GND	Ground	PWR	-	-
D32	PCI_PAR	PCI Bus Parity	IO-3.3	-	-
D33	PCI_SERR#	PCI Bus System Error	IO-3.3	PU 8K2 3.3V	-
D34	PCI_STOP#	PCI Bus Stop	IO-3.3	PU 8K2 3.3V	-
D35	PCI_TRDY#	PCI Bus Target Ready	IO-3.3	PU 8K2 3.3V	-
D36	PCI_FRAME#	PCI Bus Cycle Frame	IO-3.3	PU 8K2 3.3V	-
D37	PCI_AD16	PCI Adress & Data Bus line	IO-3.3	-	-
D38	PCI_AD18	PCI Adress & Data Bus line	IO-3.3	-	-
D39	PCI_AD20	PCI Adress & Data Bus line	IO-3.3	-	-
D40	PCI_AD22	PCI Adress & Data Bus line	IO-3.3	-	-
D41	GND	Ground	PWR	-	-
D42	PCI_AD24	PCI Adress & Data Bus line	IO-3.3	-	-
D43	PCI_AD26	PCI Adress & Data Bus line	IO-3.3	-	-
D44	PCI_AD28	PCI Adress & Data Bus line	IO-3.3	-	-
D45	PCI_AD30	PCI Adress & Data Bus line	IO-3.3	-	-
D46	PCI_IRQC#	PCI Bus Interrupt Request C	I-3.3	PU 8K2 3.3V	-
D47	PCI_IRQD#	PCI Bus Interrupt Request D	I-3.3	PU 8K2 3.3V	-
D48	PCI_CLKRUN#	PCI Clock Run	I-3.3	PU 8K2 3.3V	-
D49	PCI_M66EN#	Control PCI Speed 33/66 Mhz	I-3.3	-	Fixed to 33 Mhz
D50	PCI_CLK	PCI Clock	O-3.3	PD 10k	-
D51	GND	Ground	PWR	-	-
D52	PEG_TX0+	PCIe 0 Transmit + / SDVO B [RED] +	O - DP	-	both modes supported
D53	PEG_TX0-	PCIe 0 Transmit - / SDVO B [RED] -	O - DP	-	both modes supported
D54	PEG_LANE_RV#	PCIe Lane Reversal	I-3.3	-	-
D55	PEG_TX1+	PCIe 1 Transmit + / SDVO B [GRN] +	O - DP	-	both modes supported

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Signal Descriptions (cont'd)

Row D

Pin	Signal	Description	Type	PU/PD	Comment
D56	PEG_TX1-	PCIe 1 Transmit - / SDVO B [GRN] -	O - DP	-	both modes supported
D57	TYPE2#	Module type ID pin 2	STO	-	not connected
D58	PEG_TX2+	PCIe 2 Transmit + / SDVO B [BLU] +	O - DP	-	both modes supported
D59	PEG_TX2-	PCIe 2 Transmit - / SDVO B [BLU] -	O - DP	-	both modes supported
D60	GND	Ground	PWR	-	-
D61	PEG_TX3+	PCIe 3 Transmit + / SDVO B Clock +	O - DP	-	both modes supported
D62	PEG_TX3-	PCIe 3 Transmit - / SDVO B Clock -	O - DP	-	both modes supported
D63	RSVD	DDPC_CTRLCLK	IO-3,3	-	-
D64	RSVD	DDPC_CTRLDATA	IO-3,3	-	-
D65	PEG_TX4+	PCIe 4 Transmit + / SDVO C [RED] +	O - DP	-	both modes supported
D66	PEG_TX4-	PCIe 4 Transmit - / SDVO C [RED] -	O - DP	-	both modes supported
D67	GND	Ground	PWR	-	-
D68	PEG_TX5+	PCIe 5 Transmit + / SDVO C [GRN] +	O - DP	-	both modes supported
D69	PEG_TX5-	PCIe 5 Transmit - / SDVO C [GRN] -	O - DP	-	both modes supported
D70	GND	Ground	PWR	-	-
D71	PEG_TX6+	PCIe 6 Transmit + / SDVO C [BLU] +	O - DP	-	both modes supported
D72	PEG_TX6-	PCIe 6 Transmit - / SDVO C [BLU] -	O - DP	-	both modes supported
D73	SDVO_CLK	SDVO_CTRLCLK	IO-2,5	-	-
D74	PEG_TX7+	PCIe 7 Transmit + / SDVO C Clock +	O - DP	-	both modes supported
D75	PEG_TX7-	PCIe 7 Transmit - / SDVO C Clock -	O - DP	-	both modes supported
D76	GND	Ground	PWR	-	-
D77	IDE_CBLID#	IDE Cable Indicator Signal	I-3.3	PD 10k	-
D78	PEG_TX8+	PCIe 8 Transmit +	O - DP	-	-
D79	PEG_TX8-	PCIe 8 Transmit -	O - DP	-	-
D80	GND	Ground	PWR	-	-
D81	PEG_TX9+	PCIe 9 Transmit +	O - DP	-	-
D82	PEG_TX9-	PCIe 9 Transmit -	O - DP	-	-
D83	RSVD	MCH_CFG_20	O-3.3	PU 4K7 3.3V	-
D84	GND	Ground	PWR	-	-
D85	PEG_TX10+	PCIe 10 Transmit +	O - DP	-	-
D86	PEG_TX10-	PCIe 10 Transmit -	O - DP	-	-
D87	GND	Ground	PWR	-	-
D88	PEG_TX11+	PCIe 11 Transmit +	O - DP	-	-
D89	PEG_TX11-	PCIe 11 Transmit -	O - DP	-	-
D90	GND	Ground	PWR	-	-
D91	PEG_TX12+	PCIe 12 Transmit +	O - DP	-	-
D92	PEG_TX12-	PCIe 12 Transmit -	O - DP	-	-
D93	GND	Ground	PWR	-	-
D94	PEG_TX13+	PCIe 13 Transmit +	O - DP	-	-
D95	PEG_TX13-	PCIe 13 Transmit -	O - DP	-	-
D96	GND	Ground	PWR	-	-
D97	PEG_ENABLE#	PCIe Enable	I-3.3	PU 43K2 3.3V	-
D98	PEG_TX14+	PCIe 14 Transmit +	O - DP	-	-
D99	PEG_TX14-	PCIe 14 Transmit -	O - DP	-	-
D100	GND	Ground	PWR	-	-
D101	PEG_TX15+	PCIe 15 Transmit +	O - DP	-	-
D102	PEG_TX15-	PCIe 15 Transmit -	O - DP	-	-
D103	GND	Ground	PWR	-	-
D104	VCC_12V	Power 12V	PWR	-	-
D105	VCC_12V	Power 12V	PWR	-	-
D106	VCC_12V	Power 12V	PWR	-	-
D107	VCC_12V	Power 12V	PWR	-	-
D108	VCC_12V	Power 12V	PWR	-	-
D109	VCC_12V	Power 12V	PWR	-	-
D110	GND	Ground	PWR	-	-

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Signal Descriptions (cont'd)

Signal Type Legend	
IO-2,5	Bi-directional 2,5 V Input/Output
IO-3,3	Bi-directional 3,3 V Input/Output
IO-5	Bi-directional 5 V Input/Output
I-3,3	3,3 V Input
I-5	5 V Input
O-2,5	2,5 V Output
O-3,3	3,3 V Output
O-5	5 V Output
IO	Input/Output
OA	Analog Output
OD	Digital Output
I/O - DP	Differential Pair Input/Output
O - DP	Differential Pair Output
I - DP	Differential Pair Input
PWR	Power or Ground
STO	Strapping Output
PU	Pull Up Resistor
PD	Pull Down Resistor
NC	Not Connected / Reserved

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6 Embedded Functions

All embedded board functions on ADLINK's Computer on Modules are supported at the operating system level using the ADLINK Intelligent Device Interface (AIDI) library. The AIDI API programming interface is compatible and identical across all ADLINK Computer on Modules and all supported operating systems. The AIDI library includes a demo program to demonstrate the library's functionallity.

6.1 Watchdog Timer

The Express-MG implements a Watchdog timer that can be used to automatically detect software execution problems or system hangs and reset the board if necessary. The Watchdog timer consists of a counter that counts down from an initial value to zero. When the system is operating normally, the software that sets the intial value periodically resets the counter so that the it never reaches zero. If the counter reaches zero before the software resets it, the system is presumed to be malfunctioning and a reset signal is asserted.

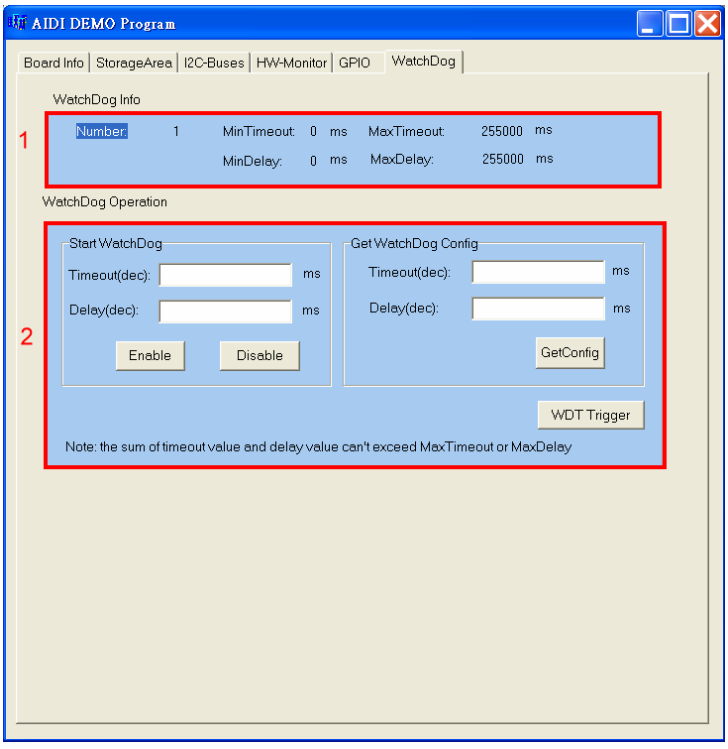


The AIDI Library Watchdog functions support Watchdog control of the board. If the Watchdog begins countdown and reaches zero, it will access the CPU's RESET signal to reset the system. This application must call another function named AidiWDogTrigger that triggers the Watchdog to restart to prevent system reset.

AIDI Demo Program
- Watchdog Tab

The AIDI Demo Program allows retrieval of the current Watchdog status and updating of the Watchdog settings.

If the Watchdog is enabled, the user can click the *WDT Trigger* button to manually reset the counter and prevent the system from resetting.



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6.2 GPIO

GPIO library support is limited to GPIO signals that originate from the Computer on Module and extended to the carrier board. COM Express modules support 4 GPO and 4 GPI signals. Some of ADLINK's COM Express boards can configure all 8 ports for GPI or GPO use.

GPIO signals can be monitored and controlled by using the ADLINK Intelligent Device Interface (AIDI) library that is compatible and identical across all ADLINK COM Express modules and all supported operating systems.

The COM Express type 2 standard assigns the following pins for either GPI or GPO.

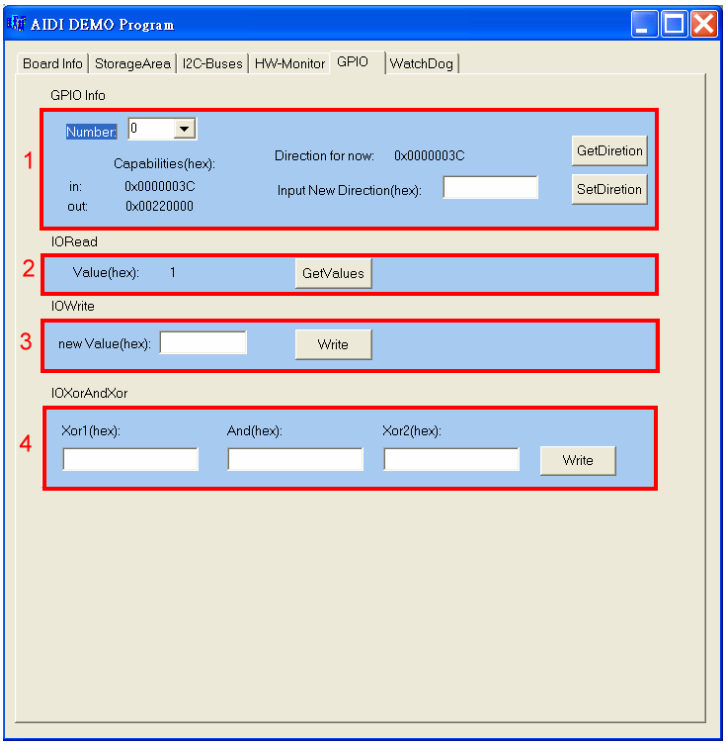
Pin	Signal Type #	AIDI ID (bit)	Remark
A54	GPI0	0	Express-MG can configure this pin for GPI or GPO
A63	GPI1	1	Express-MG can configure this pin for GPI or GPO
A67	GPI2	2	Express-MG can configure this pin for GPI or GPO
A85	GPI3	3	Express-MG can configure this pin for GPI or GPO
A93	GPO0	4	Express-MG can configure this pin for GPI or GPO
B54	GPO1	5	Express-MG can configure this pin for GPI or GPO
B57	GPO2	6	Express-MG can configure this pin for GPI or GPO
B63	GPO3	7	Express-MG can configure this pin for GPI or GPO

AIDI Demo Program - GPIO Tab

The AIDI Demo Program displays current GPI or GPO status and allows reading of GPI and writing to GPO.

The table above links logical port numbers in AIDI to physical port numbers on the COM Express board-to-board connector.

For boards that support *multi-direction* the "SetDirection" button can configure the port for either GPI or GPO.



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6.3 Hardware Monitoring

To ensure system health of your embedded system ADLINK's COM Express modules come with built in support for monitoring and control of CPU and system temperatures, fan speed and critical module voltage levels.

The AIDI Library provides simple APIs at the application level to support these functions and adds alarm functions when voltage or temperature levels exceeds the upper or lower limit set by the user.

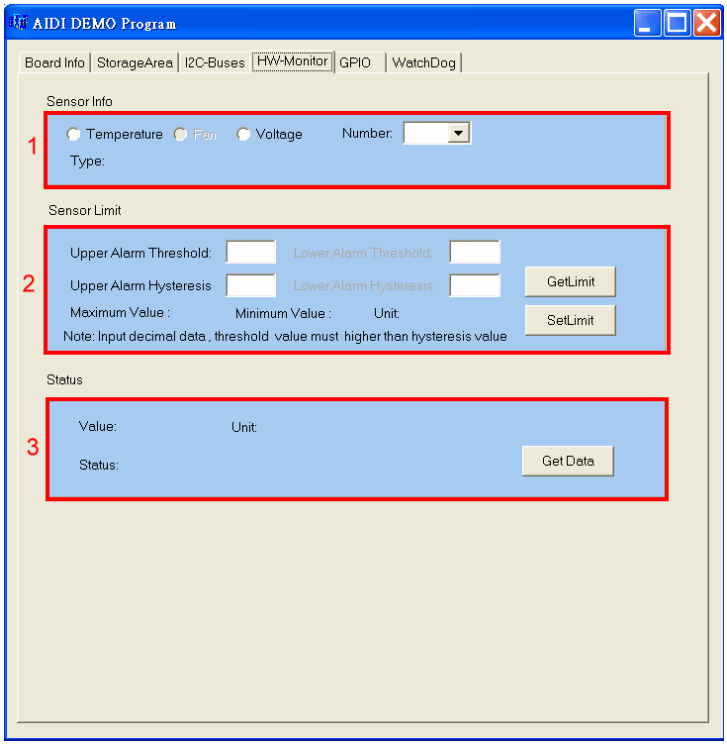
On the Express-MG the following monitored values can be read from the module: CPU temperature, system temperature, Vcore, 1.8V, 5V, 3.3V and 12V.

AIDI Demo Program
- HW Monitor Tab

Field 1 displays detected sensors (number).

Field 2 allows setting of upper and lower alarm limits.

Field 3 displays read out information of sensors.



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7 System Resources

7.1 System Memory Map

Address Range (dec.)	Address Range (hex)	Size	Description
(4GB-2MB)	FFE00000 - FFFFFFFF	2 MB	High BIOS Area
(4GB-18MB) - (4GB-17MB-1)	FEE00000 - FEEFFFFF	1 MB	FSB Interrupt Memory Space
(4GB-20MB) - (4GB-19MB-1)	FEC00000 - FECFFFFF	1 MB	APIC Configuration Space
960 K - 1024 K	F0000 - FFFFF	64 KB	System BIOS Area
896 K - 960 K	E0000 - EFFFF	64 KB	Extended System BIOS Area
768 K - 896 K	C0000 - DFFFF	128 KB	PCI expansion ROM area C0000-CFFFF: Onboard VGA BIOS D0000 - D1FFF: Intel 82567LM PXE option ROM when onboard boot LAN ROM is enable
640 K - 768 K	A0000 - BFFFF	128 KB	Video Buffer & SMM space
0 K - 640 K	00000 - 9FFFF	640 KB	DOS Area

7.2 Direct Memory Access Channels

Channel Number	Data Width	System Resource	Comment
0	8-bits	Parallel port	Note (1)
1	8-bits	Parallel port	Note (1)
2	8-bits	Diskette drive	Note (1)
3	8-bits	Parallel port	Note (1)
4		Reserved - cascade channel	
5	16-bits	Open	
6	16-bits	Open	
7	16-bits	Open	



(1) DMA channel 0/1/3 is selected when using parallel port. Floppy and parallel port cannot be used at the same time.

7.3 I/O Map

Hex Range	Description
000-01F	DMA controller 1, 8237A-5 equivalent
020-02D and 030-03F	Interrupt controller 1, 8259 equivalent
02E-02F	LPC SIO (W83627HG-AW) configuration index/data registers
040-05F	Timer, 8254-2 equivalent
060, 062, 064, 066, 068-06F	8742 equivalent (keyboard)
061, 063, 065, 067	NMI control and status

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I/O Map cont'd

Hex Range	Description
070-07F	Real Time Clock Controller(bit 7 -NMI mask)
080-091	DMA page register
93-9F	DMA page registers continued
0A0-0B1 and 0B4-0BF	Interrupt controller 2, 8259 equivalent
0B2h	APM Control I/O Address
0B3h	APM Status I/O Address
0C0-0DF	DMA controller 2, 8237A-5 equivalent
0F0	Co-processor error register
0F1	N/A
0F2-0F3	N/A
0F4	IDE ID port
0F5-0F7	N/A
0F8	IDE Index port
0F9-0FB	N/A
0FC	IDE Data port
0FD-0FF	N/A
170-177 and 376	Secondary IDE Channel
180-181	Default AIM4 SRAM control register (may be remapped)
1F0-1F7 and 3F6	Primary IDE Controller (AT Drive)
290	SIO_PME_BASE_ADDRESS
2E8 - 2EF	Serial port 4
2F8 - 2FF	Serial port 3
370-377	Secondary Floppy Disk Controller
378 - 37F	Printer Port (LPT 1)
3B0-3BF	Mono/VGA mode video
3C0-3DF	VGA registers
3E8-3EF	Serial port 2
3F0-3F7	Primary Floppy disk controller
3F8-3FF	Serial port 1
400	SMBUS IO base
4D0	Master PIC Edge/Level Trigger register
4D1	Slave PIC Edge/Level Trigger register
500	GPIO base address for SB
800	alias for ACPI I/O base address.
830	SMI Control Registers.
860	alias for ICH TCO base address
CF9	Reset Control register (8 bit I/O)
CF8-CFC	The PCI config space index/data ports
0A00~0AFF	Reserved for SIO functions base address (ex: HardWare Monitor /GPIO etc)

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7.4 Interrupt Request (IRQ) Lines

PIC Mode

IRQ#	Typical Interrupt Resource	Connected	Available
0	Counter 0	N/A	No
1	Keyboard controller	N/A	No
2	No	N/A	No
3	No	N/A	No
4	Serial Port 1 (COM1) / PCI / ISA	IRQ4 via SERIRQ, IRQ4 at ISA bus	Note (1)
5	No	N/A	No
6	Floppy Drive Controller	IRQ6 via SERIRQ	No
7	No	N/A	No
8	Real-time clock	N/A	No
9	SCI / PCI	IRQ9 via SERIRQ, IRQ9 at ISA bus	Note (1), (2)
10	No	N/A	No
11	No	N/A	No
12	PS/2 Mouse / PCI / ISA	IRQ12 via SERIRQ, IRQ12 at ISA bus	Note (1)
13	Math Processor	N/A	No
14	Primary IDE controller / PCI / ISA	IRQ14 via SERIRQ, IRQ14 at ISA bus	Note (1)
15	No	N/A	No



(1) These IRQs can be used for PCI devices when onboard device is disabled. If IRQ is from ISA, user must reserve IRQ for ISA in BIOS setup menu.
(2) BIOS does not open IRQ 9 setting for ISA bus.

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APIC Mode

IRQ#	Typical Interrupt Resource	Connected	Available
0	Counter 0	N/A	No
0	Counter 0	N/A	No
1	Keyboard controller	N/A	No
2	No	N/A	No
3	No	N/A	No
4	Serial Port 1 (COM1) / PCI / ISA	IRQ4 via SERIRQ, IRQ4 at ISA bus	Note (1)
5	No	N/A	No
6	Floppy Drive Controller	IRQ6 via SERIRQ	No
7	No	N/A	No
8	Real-time clock	N/A	No
9	SCI / PCI	IRQ9 via SERIRQ, IRQ9 at ISA bus	Note (1), (2)
10	No	N/A	No
11	No	N/A	No
12	PS/2 Mouse / PCI / ISA	IRQ12 via SERIRQ, IRQ12 at ISA bus	Note (1)
13	Math Processor	N/A	No
14	Primary IDE controller / PCI / ISA	IRQ14 via SERIRQ, IRQ14 at ISA bus	Note (1)
15	No	Secondary IDE controller PCI/ISA	No
16	N/A	PCIE Port 0/1/2/3/4/5 UHCI Controller 4/6, P.E.G Root Port, I.G.D, PCI Slot 0	Yes
17	N/A	PCIE Port 0/1/2/3/4/5, P.E.G Root Port, PCI Slot 1	Yes
18	N/A	PCIE Port 0/1/2/3/4/5 UHCI Controller 3, P.E.G Root Port, SATA Host controller, SMBus Controller, Thermal Controller, EHCI Controller #2, PCI Slot 2	Yes
19	N/A	PCIE Port 0/1/2/3/4/5 UHCI Controller 2/7, P.E.G Root Port, SATA Host controller, SATA Host controller#1, PCI Slot 3	Yes
20	N/A	ICH9 internal GBE controller	No
21	No	UHCI Controller 5	No
22	No	HDA	No
23	N/A	UHCI Controller 1/6, EHCI Controller 1	No



(1) These IRQs can be used for PCI devices when onboard device is disabled. If IRQ is from ISA, user must reserve IRQ for ISA in BIOS setup menu.
(2) BIOS does not open IRQ 9 setting for ISA bus.

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7.5 PCI Configuration Space Map

Bus No.	Device No.	Function No.	Routing	Description
00h	00h	00h	N/A	Intel GM45 GMCH Host Hub InterfaceBridge
00	01H	00H	Internal	P.E.G. Root Port
02	00H	0FFH	N/A	P.E.G. Port
00h	02h	00h	Internal	Intel Integrated Graphics Device
00h	02h	01h	Internal	Intel Integrated Graphics Device (Function 1)
00h	19h	00h	Internal	GbE Controller (Disable)
00h	1Ah	00h	Internal	Intel USB UHCI Controller 4
00h	1Ah	01h	Internal	Intel USB UHCI Controller 5
00h	1Ah	02h	Internal	Intel USB UHCI Controller 7
00h	1Ah	07h	Internal	Intel USB EHCI Controller 2
00h	1Bh	00h	Internal	High Definition Audio controller
00h	1Ch	00h	Internal	Intel ICH Express Root port 0
00h	1Ch	01h	Internal	Intel ICH Express Root port 1
00h	1Ch	03h	Internal	Intel ICH Express Root port 3
00h	1Ch	04h	Internal	Intel ICH Express Root port 4
00h	1Dh	00h	Internal	Intel USB UHCI Controller 1
00h	1Dh	01h	Internal	Intel USB UHCI Controller 2
00h	1Dh	02h	Internal	Intel USB UHCI Controller 3
00h	1Dh	03h	Internal	Intel USB UHCI Controller 6
00h	1Dh	07h	Internal	Intel USB EHCI Controller 1
00h	1Eh	00h	N/A	Intel Hub Interface to PCI Bridge
00h	1Fh	00h	N/A	Intel LPC Interface Bridge
00h	1Fh	02h	Internal	Intel SATA Host /Raid controller
00h	1Fh	03h	Internal	Intel SMBus Controller
00h	1Fh	05h	Internal	Intel Host SATA controller1
04h	00h	0FFH	Internal	PCIE Port #0
05h	00h	0FFH	Internal	PCIE Port #1
06h	00h	0FFH	Internal	PCIE Port #2
07h	00h	0FFH	Internal	PCIE Port #3
08h	00h	0FFH	Internal	PCIE Port #4
09h	00h	0FFH	Internal	PCIE Port #5
01h	04h	00h	Intemal	PCI Slot 0
01h	05h	00h	Intemal	PCI Slot 1
01h	06h	00h	Intemal	PCI Slot 2
01h	07h	00h	Intemal	PCI Slot 3

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7.6 PCI Interrupt Routing Map

PIRQ	INT Line	P.E.G. Root Port	VGA	SATA Controller	SATA Controller1	SMBus Controller	Thermal Controller	UHCI 1	UHCI 2	UHCI 3
A	INTA	INTA	X							
B	INTB	INTB								
C	INTC	INTC		X		X	X			X
D	INTD	INTD		X	X				X	
E										
F										
G										
H								X		

PIRQ	INT Line	UHCI 4	UHCI 5	UHCI 6	UHCI 7	EHCI 1	EHCI 2	HDA	Intel GBE	PCIE port 0	PCIE port 1	PCIE port 2
A	INTA	X		X						INTA	INTB	INTC
B	INTB									INTB	INTC	INTD
C	INTC						X			INTC	INTD	INTA
D	INTD				X					INTD	INTA	INTB
E									X			
F			X									
G								X				
H						X						

PIRQ	INT Line	PCIE port 3	PCIE port 4	PCIE port 5	PCI Slot 0	PCI Slot 1	PCI Slot 2	PCI Slot 3
A	INTA	INTD	INTA	INTB	X			
B	INTB	INTA	INTB	INTC		X		
C	INTC	INTB	INTC	INTD			X	
D	INTD	INTC	INTD	INTA				X
E								
F								
G								
H								

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8 BIOS Setup Utility

The following chapter describes basic navigation for the AMIBIOS8 BIOS setup utility for the ADLINK Express-MG COM Express module.

8.1 Starting the BIOS

To enter the setup screen, follow these steps:

1. Power on the motherboard
2. Press the < Delete > key on your keyboard when you see the following text prompt:

   < Press DEL or Delete to run Setup >

3. After you press the < Delete > key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu, such as Chipset and Power menus.



NOTE: In most cases, the < Delete > key is used to invoke the setup screen. There are several cases that use other keys, such as < F1 >, < F2 >, and so on.

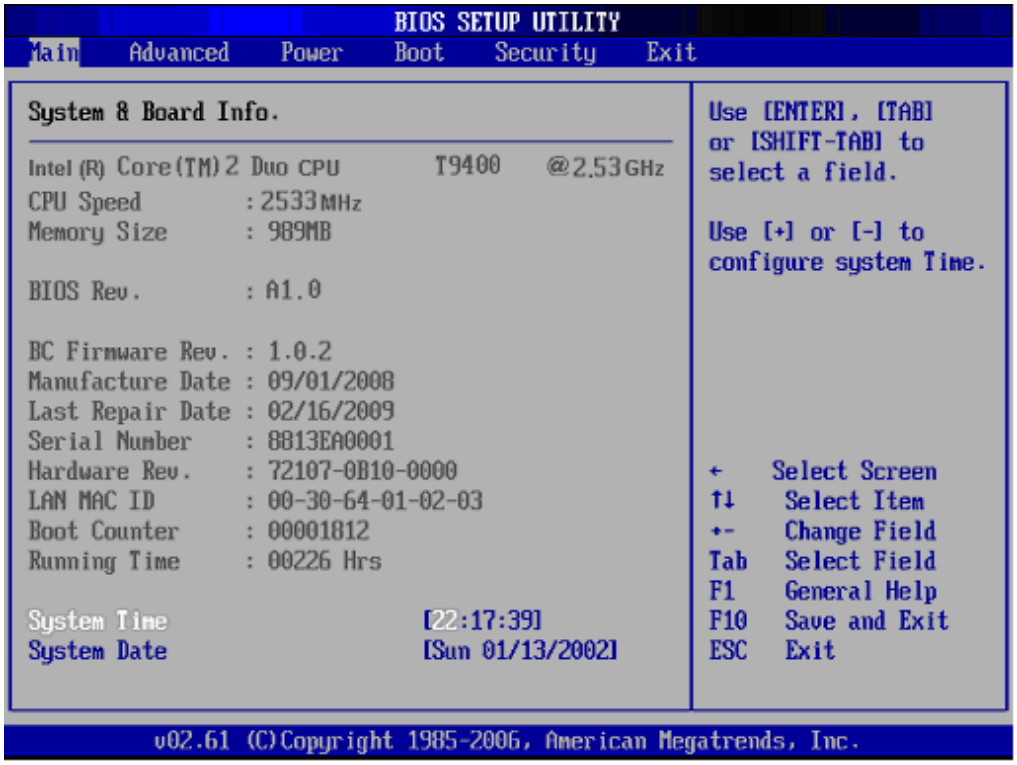
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8.1.1 Main Setup Menu

The main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in this user's guide.

The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed" options cannot be configured, "Blue" options can be.

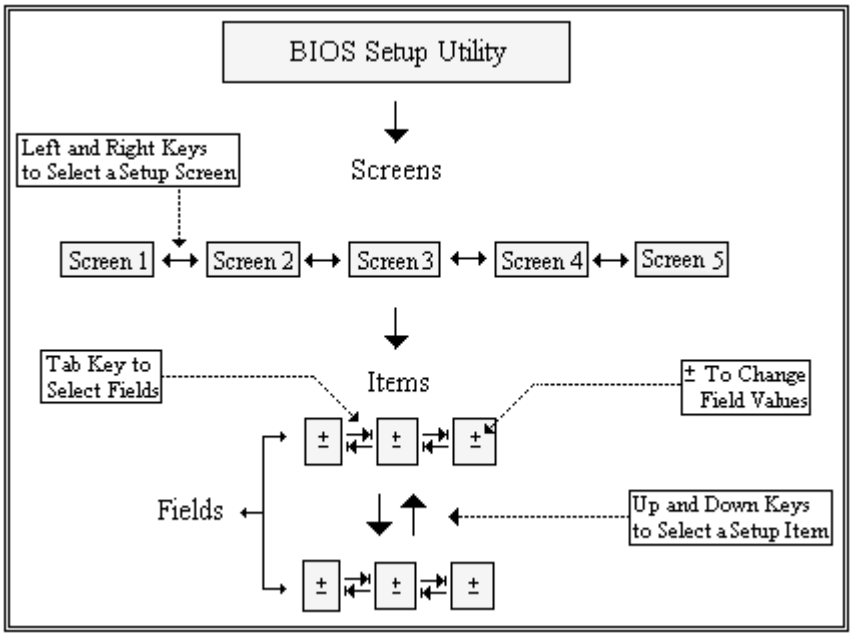
The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.



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8.1.2 Navigation

The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process.
These keys include < F1 >, < F10 >, < Enter >, < ESC >, < Arrow > keys, and so on.



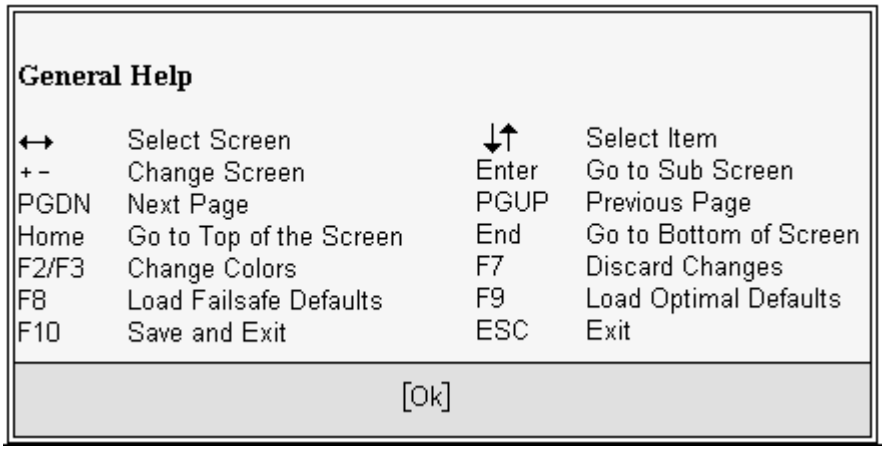
NOTE: There is a hot key legend located in the right frame on most setup screens.

Hot Key	Description
→←	Left/Right The *Left and Right* < Arrow > keys allow you to select a setup screen. For example: Main screen, Advanced screen, Chipset screen, and so on.
↑↓	Up/Down The *Up and Down* < Arrow > keys allow you to select a setup item or sub-screen.
+ −	Plus/Minus The *Plus and Minus* < Arrow > keys allow you to change the field value of a particular setup item. For example: Date and Time.
Tab	The < Tab > key allows you to select setup fields.

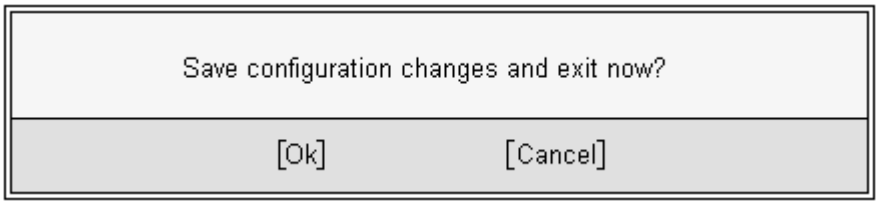
NOTE: The < F8 > key on your keyboard is the Fail-Safe key. It is not displayed on the key legend by default. To set the Fail-Safe settings of the BIOS, press the < F8 > key on your keyboard. It is located on the upper row of a standard 101 keyboard. The Fail-Safe settings allow the motherboard to boot up with the least amount of options set. This can lessen the probability of conflicting settings.

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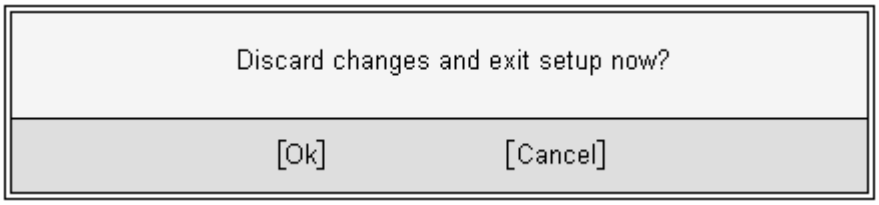
Hot Key	Description
F1	The < F1 > key allows you to display the *General Help screen*. Press the < F1 > key to open the *General Help screen*.



F10	The < F10 > key allows you to save any changes you have made and exit Setup. Press the < F10 > key to save your changes. The following screen will appear:



	Press the < Enter > key to save the configuration and exit. You can also use the < Arrow > key to select *Cancel* and then press the < Enter > key to abort this function and return to the previous screen.
ESC	The < Esc > key allows you to discard any changes you have made and exit the Setup. Press the < Esc > key to exit the setup without saving your changes. The following screen will appear:

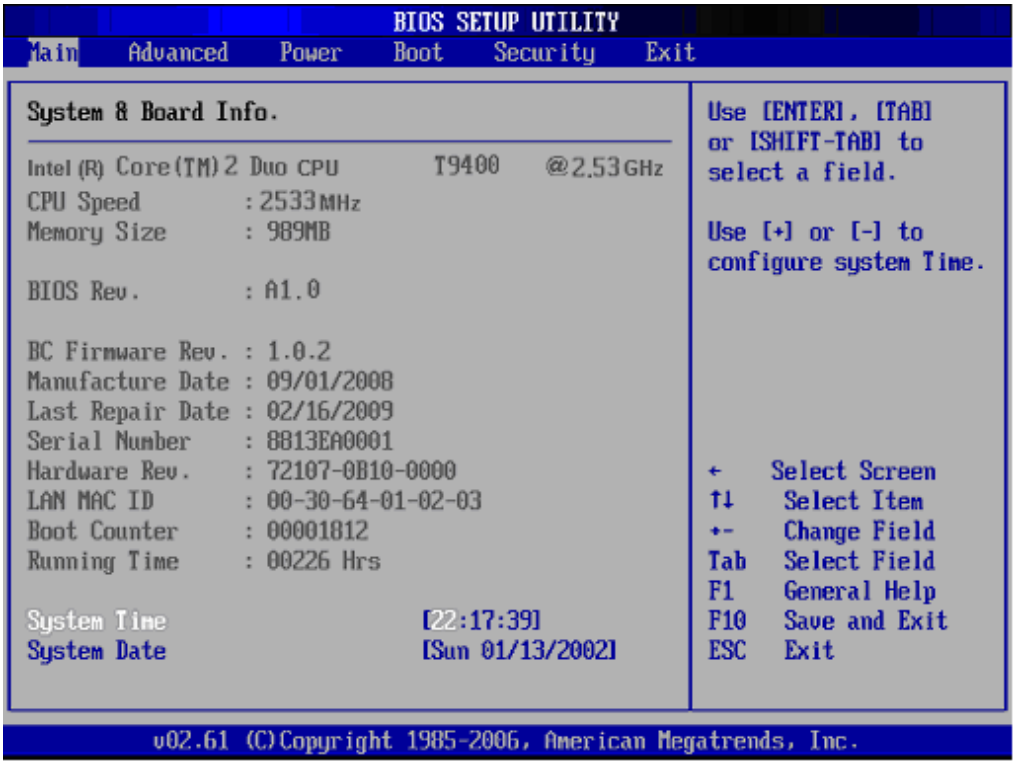


	Press the < Enter > key to discard changes and exit. You can also use the < Arrow > key to select *Cancel* and then press the < Enter > key to abort this function and return to the previous screen.
Enter	The < Enter > key allows you to display or change the setup option listed for a particular setup item. The < Enter > key can also allow you to display the setup sub-screens.

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8.2 Main Setup

When you first enter the Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the *Main* tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



8.2.1 System Time/System Date

Use this option to change the system time and date. Highlight *System Time* or *System Date* using the < `Arrow` > keys. Enter new values using the keyboard. Press the < `Tab` > key or the < `Arrow` > keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

NOTE: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

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8.2.2 System & Board Info

The Main BIOS setup screen reports processor, memory and board information.

BIOS Rev.

Displays the current BIOS revision.

BC Firmware Rev.

Displays the current firmware revision of board controller (BC).

Manufacture Date

Displays the date which the board was manufactured.

Last Repair Date

Displays the date on which the board was last repaired.

Serial Number

Displays the serial number of board.

Hardware Rev.

The hardware revision is in XXXXX-YYYY-ZZZZ format. XXXXX represents the ADLINK internal P/N for this board. YYYY is the board PCB version and ZZZZ represents a special configuration of the board.

LAN MAC ID

Displays the MAC address of onboard Ethernet controller.

Boot Counter

Displays the number of times the board has been booted-up since production (max. 16777215).

Running Time

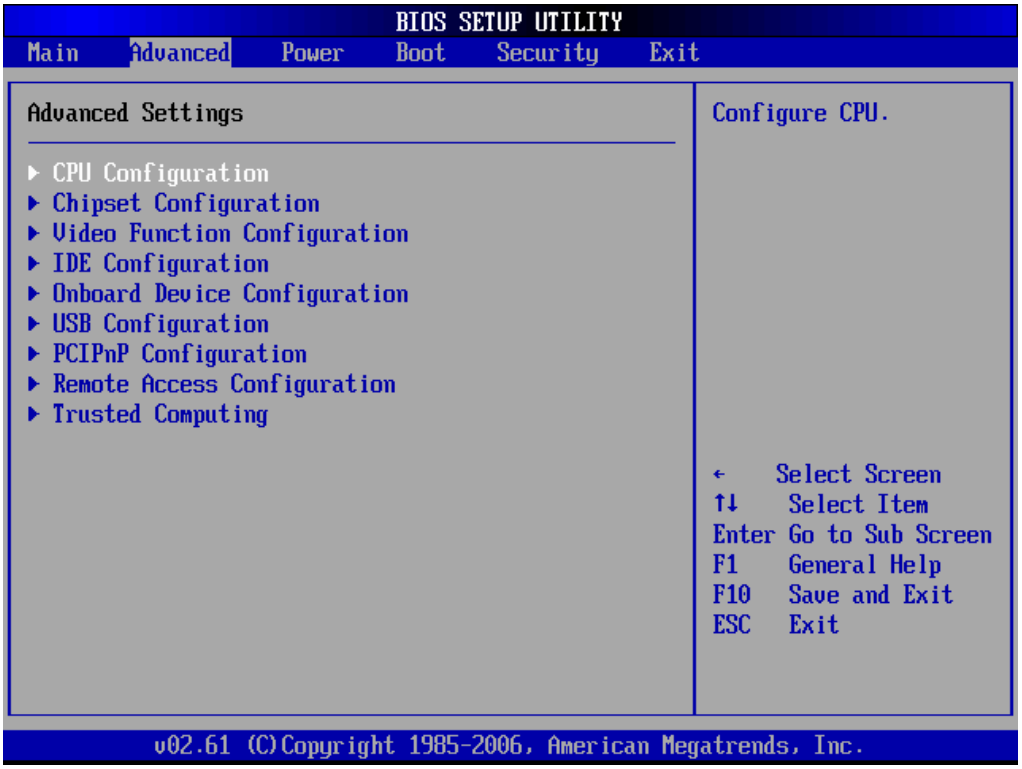
Displays the total time the board has been in operation since production. The units are in hours and the maximum value is 65535.

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8.3 Advanced BIOS Setup

Select the *Advanced* tab from the setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as Chipset Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the < `Arrow` > keys. The Advanced BIOS Setup screen is shown below.

The sub menus are described on the following pages.



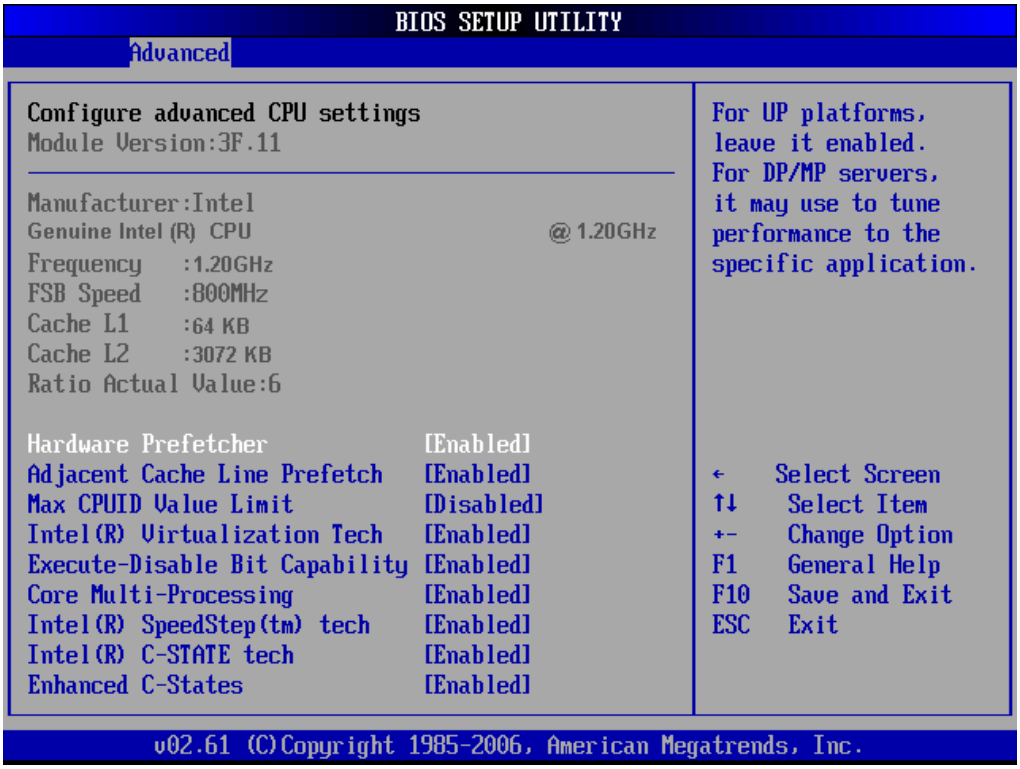
WARNING: Setting incorrect or conflicting values in Advanced BIOS Setup may cause system malfunctions.

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8.3.1 CPU Configuration

CPU Configuration Settings

You can use this screen to select options for the CPU Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the *CPU Configuration* screen is shown below.



Hardware Prefetcher

This feature is used for reducing the waiting time of DRAM. The hardware prefetcher looks for streams of data and tries to predict what data will be needed next by the processor and proactively tries to fetch these data.

Adjacent Cache Line Prefetch

This feature is used to enable optimal use of sequential memory access for performance purposes. Disable this setting for applications requiring high use of random memory access.

Max CPUID Value Limit

When the computer is boots, the operating system executes its CPUID instruction to identify the processor and its capabilities. Before it can do so, it must first query the processor to find out the highest input value the CPUID recognizes. This determines the kind of basic

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information CPUID can provide the operating system. This option allows you to circumvent problems with older operating systems.

When Enabled, the processor will limit the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When Disabled, the processor will return the actual maximum CPUID input value of the processor when queried.

Execute Disable Bit

This is an Intel hardware-based security feature that can help reduce system exposure to viruses and malicious code. It allows the processor to classify areas in memory where application code can or cannot execute. When a malicious worm attempts to insert code in the buffer, the processor disables its code execution, preventing damage and worm propagation. To use Execute Disable Bit you must have a PC or server with a processor with Execute Disable Bit capability and a supporting operating system.

Intel SpeedStep Tech.

This option enables or disables Intel SpeedStep Technology.

Intel C-STATE Tech.

Intel C-STATE Technology is responsible for activating the processor's own power consumption management. It allows the CPU to save more power under idle mode.

Enhanced C-States

Enhanced C-states are available on newest mobile processors. When this option is enabled, the CPU is automatically put into the lowest frequency/voltage mode when it enters a given C-state.

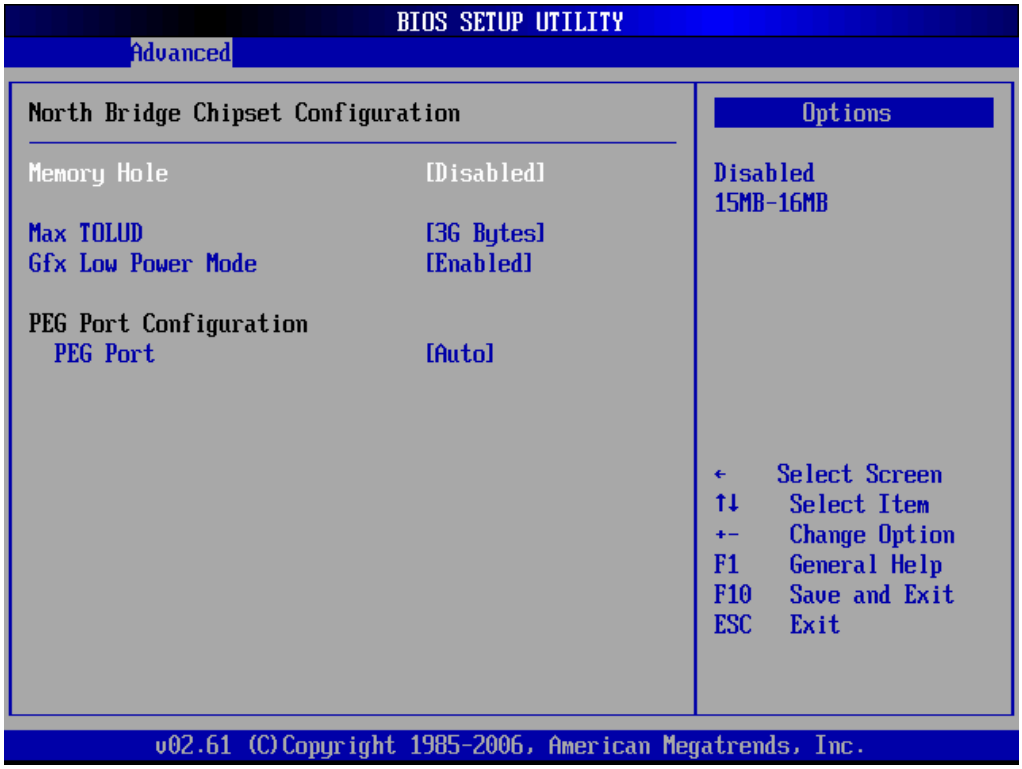
MPS Revision

It specifies the version of the Multi-Processor Specification (MPS) that the CPU board will use. 1.4 is the suggestion.

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8.3.2 Chipset Configuration

Chipset Configuration Settings



Memory Hole

This option selects whether or not to open a memory hole. The memory hole will be located at 15MB-16MB of system memory.

Max TOLUD

Sets the maximum top of low usable DRAM.

Gfx Low Power Mode

This option is applicable for SFF only to enable low power mode.

PEG Port

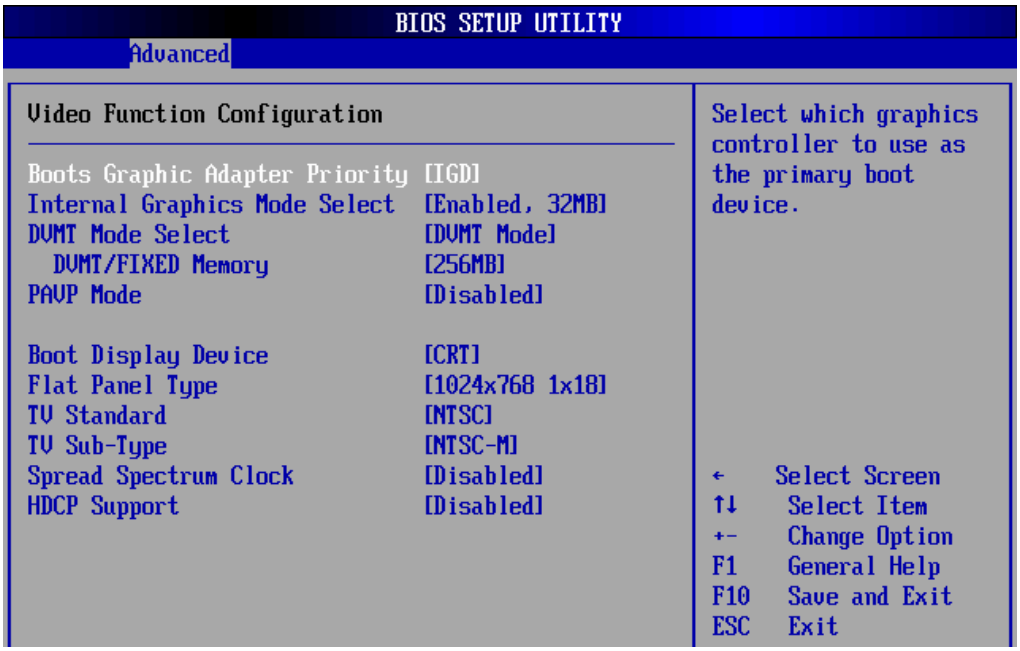
Set this option to [Auto] to enable auto negotiation with a PEG device, [Enabled] to open the PEG port, or [Disabled] to disable the PEG port.

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8.3.3 Video Function Configuration

Video Function Configuration Settings

You can use this screen to select options for Video Function configuration settings. The video function BIOS Setup screen is shown below.



Boots Graphic Adapter Priority

Select which graphics controller to use as the primary boot display device. IGD = Integrated Graphic device. PEG/PCI = external PCI/Express graphic device.

Internal Graphics Mode Select

Select the amount of system memory which is used by internal graphics device.

DVMT Mode Select

Unified Memory Architecture (UMA) is a concept whereby system memory is shared by both CPU and graphics processor. While this reduces cost, it also reduces the system's performance by taking up a large portion of memory for the graphics processor. Intel's Dynamic Video Memory Technology (DVMT) takes that concept further by allowing the system to dynamically allocate memory resources according to the demands of the system at any point in time. The key idea in DVMT is to improve the efficiency of the memory allocated to either system or graphics processor.

When set to **Fixed Mode**, the graphics driver will reserve a fixed portion of the system memory as graphics memory. When set to **DVMT Mode**, the graphics chip will dynamically allocate system memory as graphics memory, according to system and graphics

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requirements. When set to **Combo Mode**, the graphics driver will allocate a fixed amount of memory as dedicated graphics memory, as well as allow more system memory to be dynamically allocated between the graphics processor and the operating system.

DVMT/FIXED Memory

Sets the amount of memory according to DVMT Mode Select.

PAVP Mode

PAVP (Protected Audio Video Path) is a feature to ensure a robust and secure content protection path for high-definition video playback including Blu-ray discs on the Microsoft Windows Vista operating system. It can reduce processor utilization by off-loading the video decode onto the chipset to free up the processor to perform other tasks. Select Lite mode if want to use the PAVP feature.

Boot Display Device

Selects the display interface you want to make active on boot-up.

Flat Panel Type

When LVDS is selected from Boot Display Device, this option allows you to select resolution settings for correct timing to the LVDS interface you want to use. The supported resolutions are: 640x480 18-bit 1Ch, 800x600 18-bit 1Ch, 1024x768 18-bit 1Ch, 1024x768 24-bit 1Ch, 1280x800 24-bit 1Ch, 1280x1024 18-bit 2Ch, 1280x1024 24-bit 2Ch, 1400x1050 18-bit 2Ch, 1400x1050 24-bit 2Ch, 1600x1200 18-bit 2Ch, 1600x1200 24-bit 2Ch, 1680x1050 18-bit 2Ch, 1680x1050 24-bit 2Ch, 1920x1200 18-bit 2Ch, 1920x1200 24-bit 2Ch, 2048x1536 24-bit 2Ch.

Boot Display Device

Selects the display interface you want to make active on boot-up.

TV Standard

Selects the TV standard.

TV Sub-Type

Selects sub-type of the TV standard.

Spread Spectrum Clock

This option enables/disables the spread spectrum of Gfx.

HDCP Support

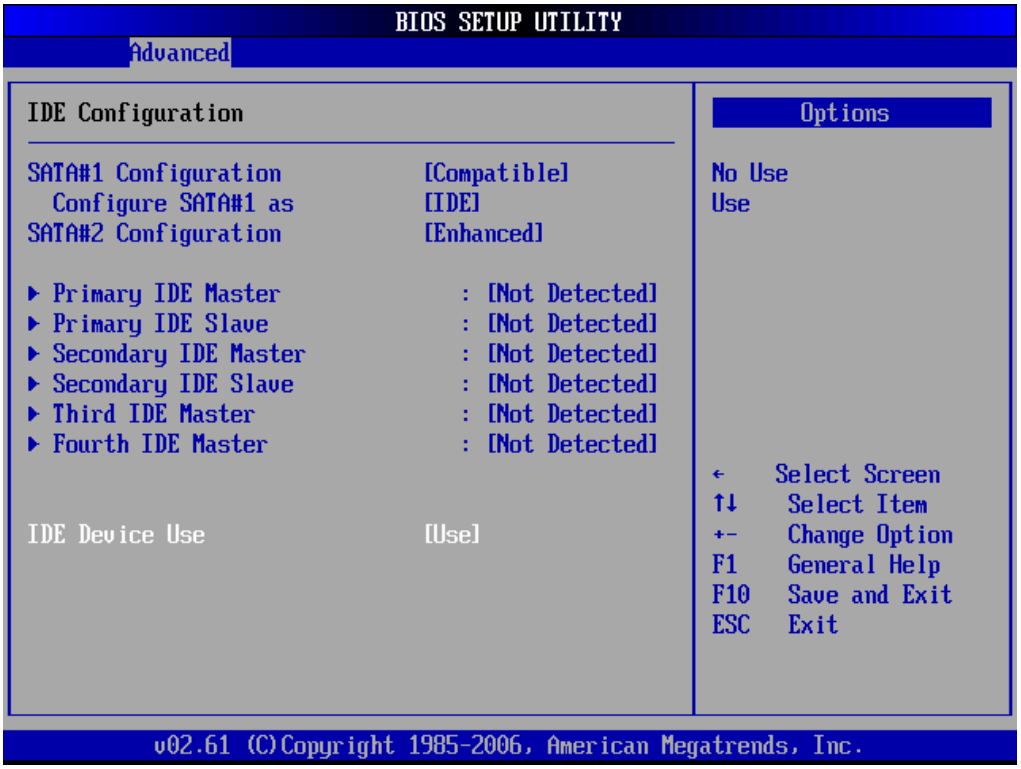
Enables/Disables High-bandwidth Digital Content Protection (HDCP) support.

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8.3.4 IDE Configuration

IDE Configuration Settings

You can use this screen to select options for the IDE Configuration Settings. An example of the *IDE Configuration* screen is shown below.



SATA#1 Configuration

This item specifies whether SATA Channel 1 is initialized in Compatible or Enhanced mode of operation. The settings are **Disabled**, **Compatible** and **Enhanced**.

Configure SATA#1 as

When running in Compatible/Enhanced mode, the SATA Channel 1 can be configured as a legacy IDE channel, RAID (RAID0, RAID1 only), and AHCI mode.

SATA#2 Configuration

This item specifies whether the SATA Channel 2 is initialized in Enhanced mode of operation.

Primary IDE Master/Slave, Secondary IDE Master/Slave

Select one of the hard disk drives to configure it. Press < Enter > to access its sub menu.

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Hot Plug

This option enables/disables the AHCI hotswap function (only visible when ***Configure SATA#1 as*** is set to AHCI).

IDE Device Use

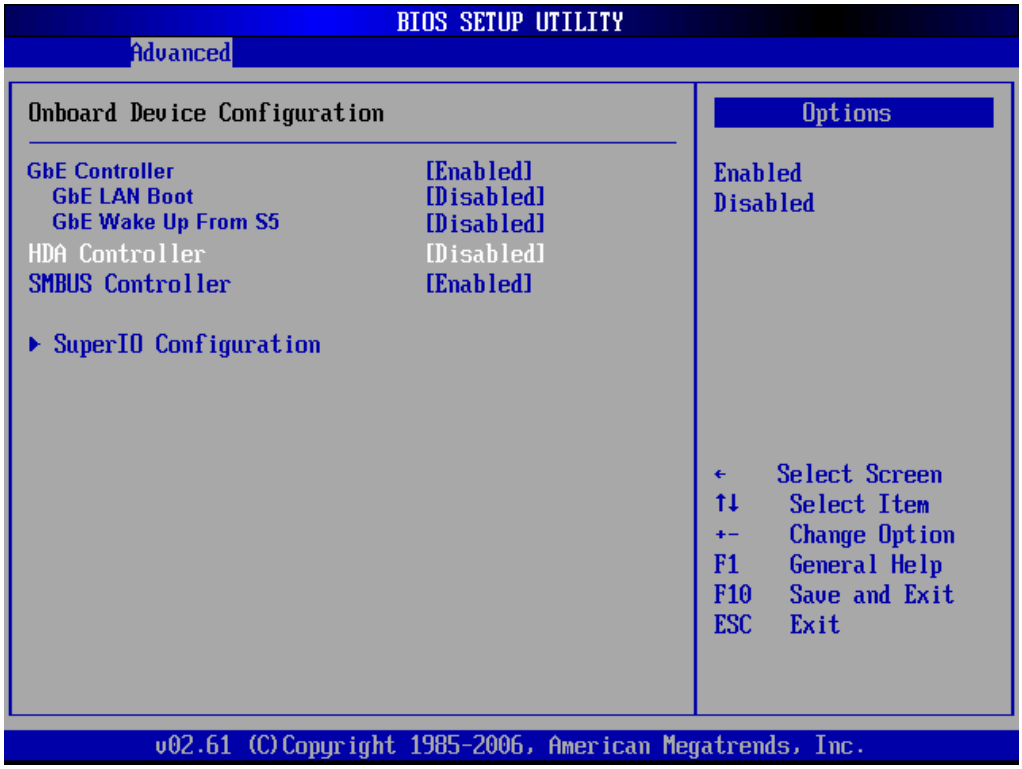
Set this option to determine if IDE devices are used.

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8.3.5 Onboard Device Configuration

Onboard Device Configuration Settings

You can use this screen to specify options for the Onboard Device Configuration settings. The screen is shown below.



GbE Controller

Set this value to Enable/Disable the onboard GbE controller.

GbE LAN Boot

Set this value to Enable/Disable the PXE function of the onboard GbE controller.

GbE Wake Up From S5

Set this value to Enable/Disable the GbE wake up system from S5 power mode.

HDA Controller

Set this value to Enable/Disable the onboard HDA Controller.

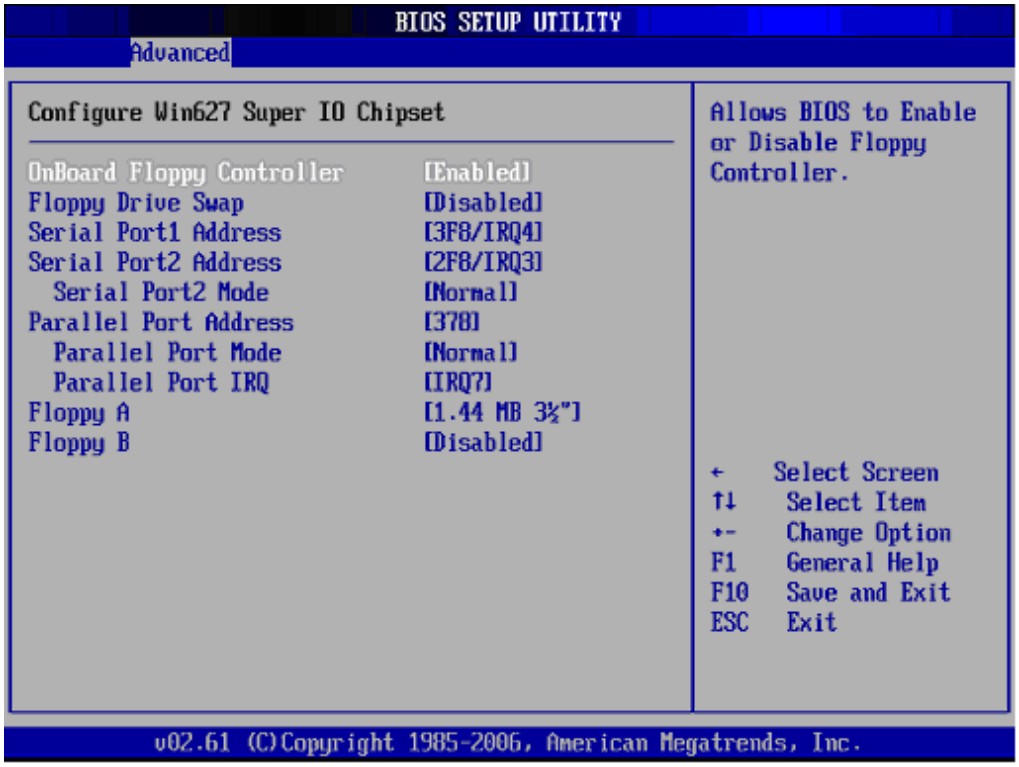
SMBusController

Set this value to Enable/Disable the SMBus controller.

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SuperIO Configuration Screen

SuperIO configuration screen is a sub-menu of Onboard Device Configuration. You can use this screen to select options for the Super IO settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below. The visibility of this SuperIO configuration screen depends on the presence of an onboard SuperIO (Winbond W83627HF). If the Express-MG is used on a carrier w/o a SIO chip, the legacy-free mode will take effect.



OnBoard Floppy Controller

This option enables/disables the Super IO's floppy controller.

Floppy Drive Swap

This option allows you to determine whether or not to enable Floppy Drive Swap function. Enabling it will swap floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A.

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Serial Port1 Address

This option specifies the base I/O port address and Interrupt Request address of serial port 1.

Option	Description
Disabled	Set this value to prevent the serial port from accessing any system resources. When this option is set to Disabled, the serial port physically becomes unavailable.
3F8/IRQ4	Set this value to allow the serial port to use 3F8 as its I/O port address and IRQ 4 for the interrupt address.
3E8/IRQ4	Set this value to allow the serial port to use 3E8 as its I/O port address and IRQ 4 for the interrupt address.
2F8/IRQ3	Set this value to allow the serial port to use 2F8 as its I/O port address and IRQ 3 for the interrupt address.
2E8/IRQ3	Set this value to allow the serial port to use 2E8 as its I/O port address and IRQ 3 for the interrupt address.

Serial Port2 Address

This option specifies the base I/O port address and Interrupt Request address of Serial Port2. The settings of Serial Port2 are the same as Serial Port1. However, the setting used by Serial Port1 will not be available for Serial Port2. For example, if Serial Port1 uses 3F8/IRQ4, the option, the 3F8/IRQ4 will not appear in the options of Serial Port2.

Serial Port2 Mode

This option allows the BIOS to select a mode for Serial Port2. The settings are Normal, IrDA, and ASK IR.

Parallel Port Address

This option lets to configure the SuperIO's parallel port address.

Parallel Port Mode

This option specifies the parallel port mode.

Option	Description
Normal	Set this value to allow the standard parallel port mode to be used.
EPP	The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bidirectional data transfer driven by the host device.
ECP	The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Megabits per second. ECP provides symmetric Bidirectional communication.
EPP+ECP	Allows the parallel port to support both the ECP and EPP modes simultaneously.

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Parallel Port IRQ

This option specifies the IRQ used by the parallel port.

Option	Description
IRQ5	Set this value to allow the serial port to use Interrupt 5.
IRQ7	Set this value to allow the serial port to use Interrupt 7. The majority of parallel ports on computer systems use IRQ7 and I/O Port 378H as the standard setting.

Floppy Drive A/B:

Move the cursor to these fields via up and down < `arrow` > keys. Select the floppy type. The Optimal and Fail-Safe settings for floppy drive A: is *1.44 MB 3½".*

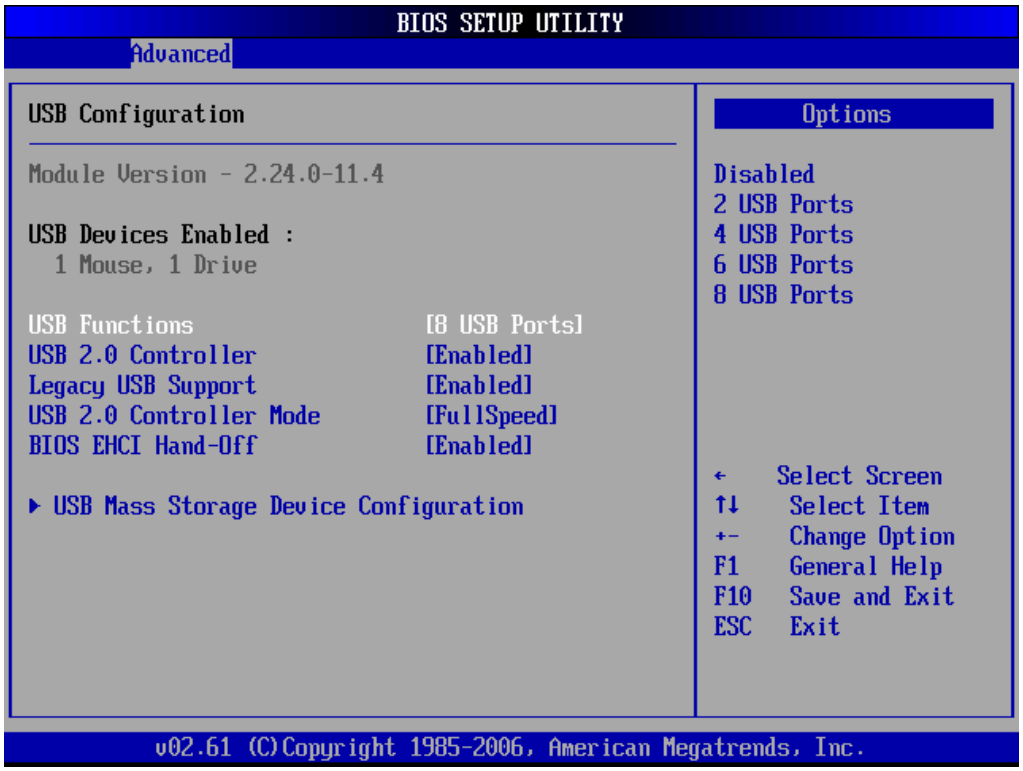
Option	Description
Disabled	Set this value to prevent the use of the selected floppy disk drive channel. This option should be set if no floppy disk drive is installed on the specified channel.
360 KB 5 ¼"	Set this value if the floppy disk drive attached to the corresponding channel is a 360 KB 5¼" floppy disk drive.
1.2 MB 5 ¼"	Set this value if the floppy disk drive attached to the corresponding channel is a 1.2 MB 5¼" floppy disk drive.
720 KB 3 ½"	Set this value if the floppy disk drive attached to the corresponding channel is a 720 KB 3½" floppy disk drive.
1.44 MB 3 ½"	Set this value if the floppy disk drive attached to the corresponding channel is a 1.44 MB 3½" floppy disk drive. This is the default setting for *Floppy Drive A*.
2.88 MB 3 ½"	Set this value if the floppy disk drive attached to the corresponding channel is a 2.88 MB 3½" floppy disk drive.

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8.3.6 USB Configuration

USB Configuration Settings

You can use this screen to specify options for the USB configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.



USB Function

Set this value to allow the system to Disable, Enable, and select a set number of onboard USB ports.

USB 2.0 Controller

This option depends on the setting of USB Function above. If USB Function is set to Disabled, this option will have no effect. Enabled will open USB 2.0 functionality to all USB ports.

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Legacy USB Support

Legacy USB Support refers to USB mouse and keyboard support. Normally if this option is not enabled, any attached USB mouse or keyboard will not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or keyboard can control the system even when there is no USB driver loaded on the system. Set this value to enable or disable the Legacy USB Support (see below).

Option	Description
Disabled	Set this value to prevent the use of any USB device in DOS or during system boot.
Enabled	Set this value to allow the use of USB devices during boot and while using DOS.
Auto	This option auto detects USB Keyboards or Mice and if found, allows them to be utilized during boot and while using DOS.

USB 2.0 Controller Mode

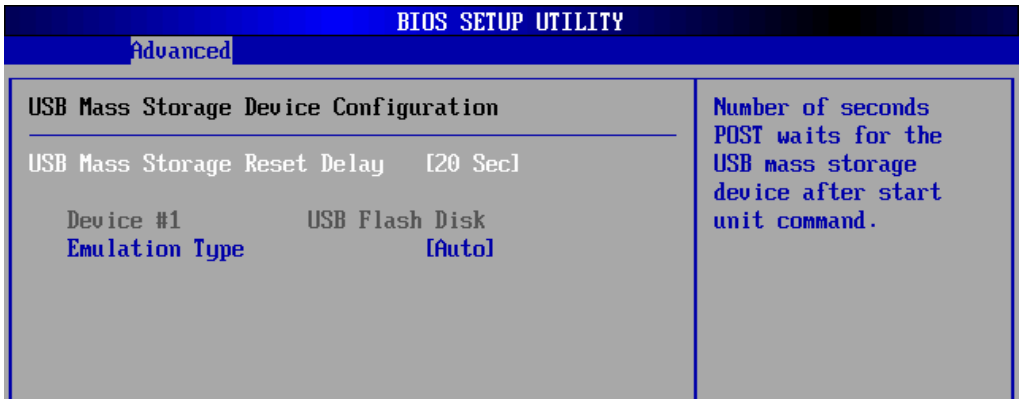
The USB 2.0 Controller Mode configures the data rate of the USB port. The options are FullSpeed (12 Mbps) and HiSpeed (480 Mbps).

BIOS EHCI hand-off

This option provides a work around for OSes without ECHI hand-off support. The EHCI ownership change should be claimed by the EHCI driver.

USB Mass Storage Device Configuration

This is a submenu for configuring the USB Mass Storage Class Devices when BIOS finds they are in use on the USB ports. Emulation Type can be set according to the type of attached USB mass storage device(s). If set to Auto, USB devices less than 530MB will be emulated as Floppy and those greater than 530MB will remain as hard drive. The Forced FDD option can be used to force a hard disk type drive (such as a Zip drive) to boot as FDD.

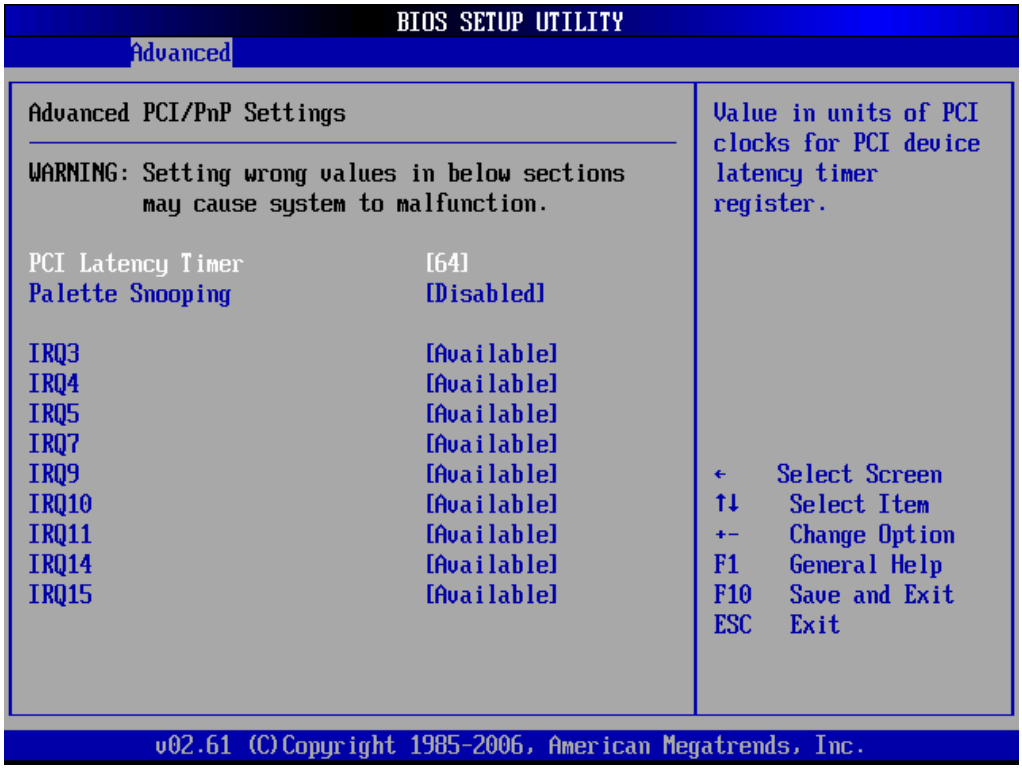


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8.3.7 PCIPnP Configuration

PCIPnP Configuration Settings

You can display a Plug and Play BIOS Setup option by highlighting it using the < Arrow > keys to select an item. The Plug and Play BIOS Setup screen is shown below.



PCI Latency Timer

Set this value to allow the PCI Latency Timer to be adjusted. This option sets the latency of all PCI devices on the PCI bus.

Palette Snooping

Set this value to allow the system to modify the Palette Snooping settings.

Disabled - should not be changed unless the VGA card manufacturer requires Palette Snooping to be Enabled.

Enabled - This setting informs the PCI devices that an ISA based Graphics device is installed in the system. It does this so the ISA based Graphics card will function correctly. This does not necessarily indicate a physical ISA adapter card. The graphics chipset can be mounted on a PCI card. Always check with your adapter card's manuals first, before modifying the setting in the BIOS.

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IRQ

Set this value to allow the IRQ settings to be modified.

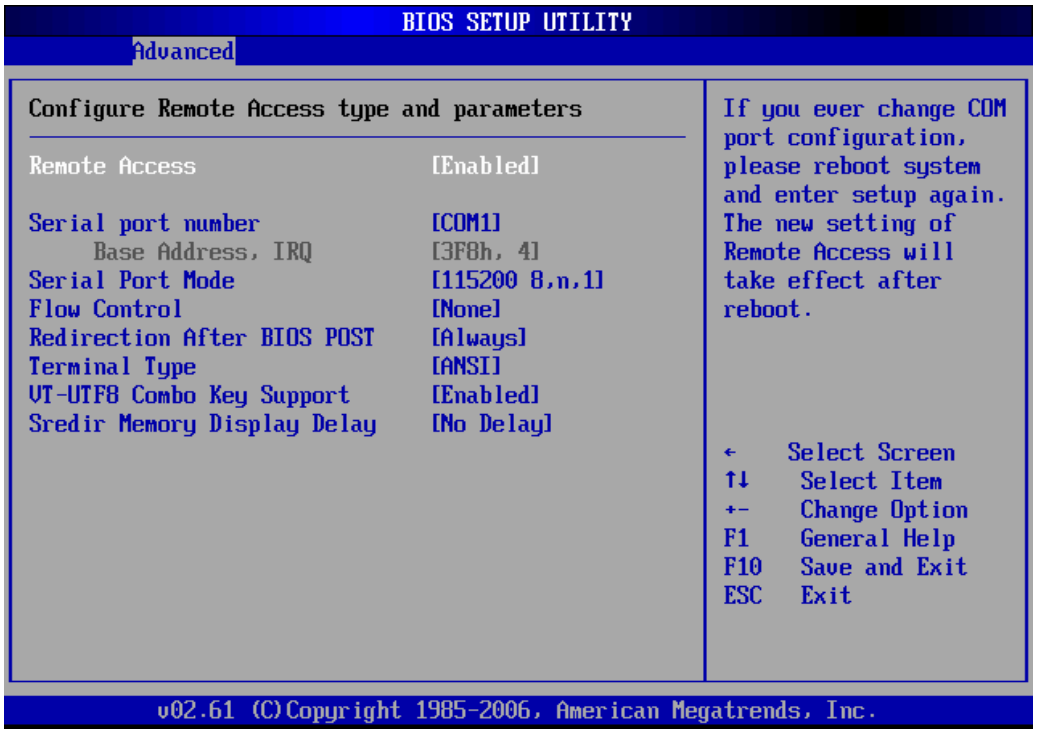
Available - This setting allows the specified IRQ to be used by a PCI/PnP device.

Reserved - This setting allows the specified IRQ to be used by a legacy ISA device.

8.3.8 Remote Access Configuration

Remote Access (Console Redirection)

Remote Access (or Console Redirection) allows you to control a system from a remote location by re-directing keyboard input and text output through the serial port.. This screen will not be visible if the module is used on a carrier board w/o a SuperIO chip, due to lack of serial port support.



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Remote Access

Select this option to Enable or Disable the BIOS remote access feature here.



Enabling Remote Access requires a dedicated serial port connection. Once both serial ports are configured to disabled, you should set this value to Disabled or it may cause an abnormal boot.

Serial Port Number

Select the serial port you want to use for the remote access interface. You can set the value for this option to either COM1 or COM2.



If you have changed the resource assignment of the serial ports in Advanced>Onboard Device Configuration>SuperIO Configuration, you must Save Changes and Exit, reboot the system, and enter the setup menu again in order to see those changes reflected in the available Remote Access options.

Serial Port Mode

Select the baud rate you want the serial port to use for console redirection. The options are 115200 8,n,1; 57600 8,n,1; 19200 8,n,1; and 09600 8,n,1.

Flow Control

Set this option to select Flow Control for console redirection. The settings for this value are None, Hardware, or Software.

Redirection After BIOS POST

This option allows you to set Redirection configuration after BIOS POST. The settings for this value are Disabled, Boot Loader, or Always.

Option	Description
Disabled	Set this value to turn off the redirection after POST
Boot Loader	Set this value to allow the redirection to be active during POST and Boot Loader.
Always	Set this value to allow the redirection to be always active.

Terminal Type

This option is used to select either VT100/VT-UTF8 or ANSI terminal type. The settings for this value are ANSI, VT100, or VT-UTF8.

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VT-UTF8 Combo Key Support

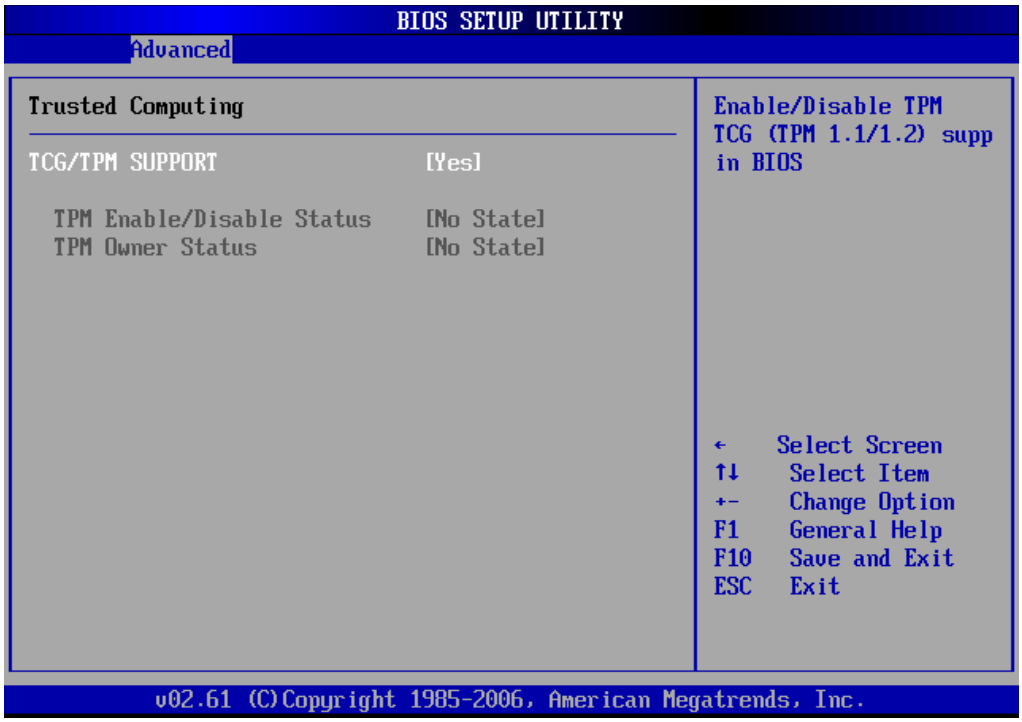
This option enables VT-UTF8 Combination Key Support for ANSI/VT100 terminals. The settings for this value are Enabled or Disabled.

Sredir Memory Display Delay

This option gives the delay in seconds to display memory information. The options for this value are No Delay, Delay 1 Sec, Delay 2 Sec, or Delay 4 Sec.

8.3.9 Trusted Computing

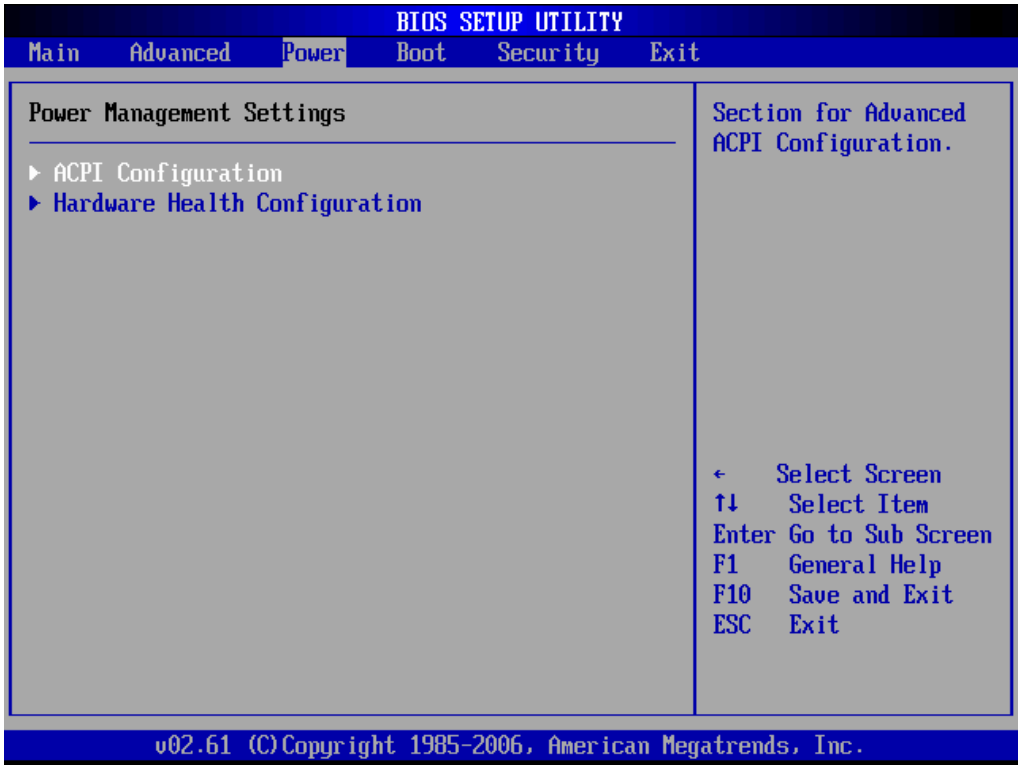
Trusted Computing is an industry standard to make personal computers more secure through a dedicated hardware chip, called a Trusted Platform Module (TPM). This option allows you to enable or disable the TPM support.



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8.4 Power Management

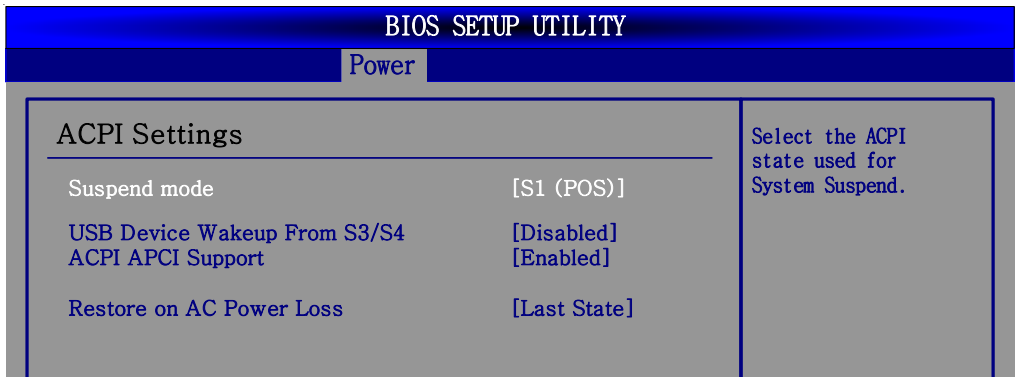
Select the Power tab from the setup screen to enter the power management BIOS Setup screen. You can select any of the items in the left frame of the screen, such as ACPI Configuration, to go to the sub menu for that item. The power management BIOS Setup screen is shown below.



8.4.1 ACPI Configuration

You can use this screen to select options for the ACPI Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on this page. The screen is shown below.

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Suspend Mode

This setting selects either **S1 (POS)** or **S3 (STR)** system suspend mode.

Option	Description
S1 (POS)	Power On Suspend - Under this setting the CPU is not executing instructions, all power resources that supply system level reference of S0 are off, system memory context is maintained, devices that reference power resources that are on are on, and devices that can wake-up the system can cause the CPU to continue to execute from where it left off.
S3 (STR)	Suspend to RAM - Under this setting the system enters a low power state instead of being completely shut off. This allows the computer system to boot up in a few seconds.

USB Device Wakeup From S3/S4

Enable/Disable USB device wake-up from S3/S4 mode.

ACPI APIC Support

This setting allows you to enable or disable ACPI APIC support. The ACPI APIC table pointer is included in the RSDT pointer list.

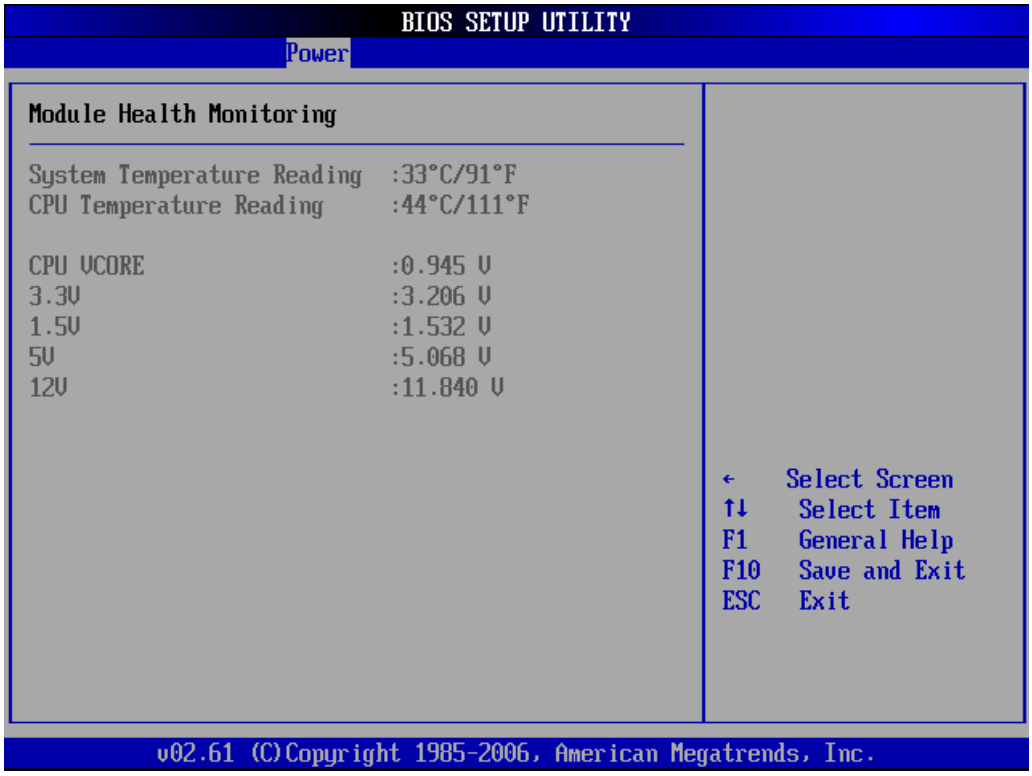
Restore on AC Power Loss

Determines what state the computer enters when AC power is restored after a power loss. The options for this value are Last State, Power On and Power Off.

Option	Description
Power Off	Set this value to always power off the system while AC power is restored.
Power On	Set this value to always power on the system while AC power is restored.
Last State	Set this value to power off/on the system depending on the last system power state while AC power is restored.

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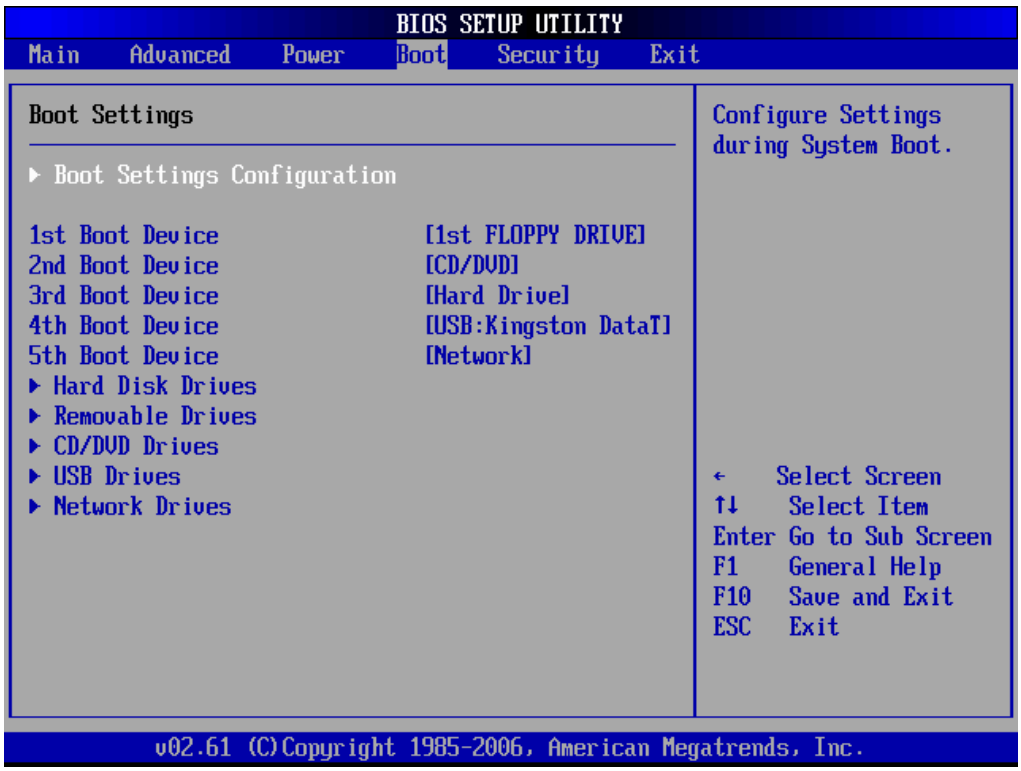
8.4.2 Hardware Health Configuration



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8.5 Boot Setup

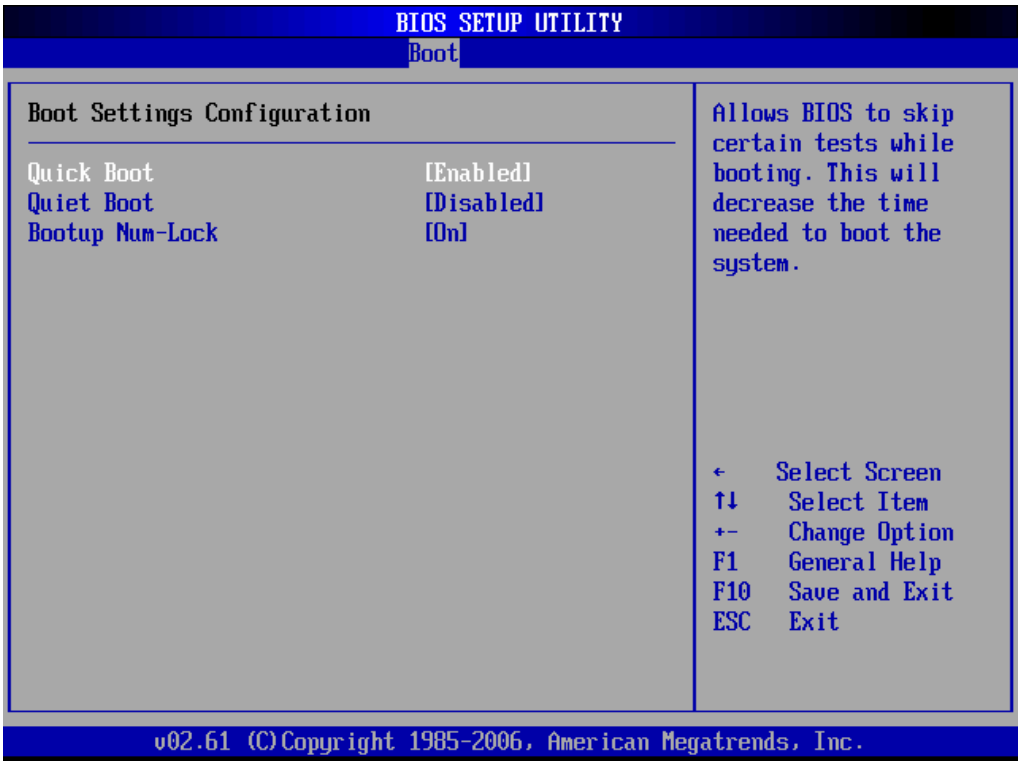
Select the Boot tab from the setup screen to enter the Boot BIOS Setup screen. You can select any of the items in the left frame of the screen, such as Boot Device Priority, to go to the sub menu for that item. You can display an Boot BIOS Setup option by highlighting it using the < Arrow > keys. The Boot Settings screen is shown below:



Boot Settings Configuration

Use this screen to select options for the Boot Settings Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages. The screen is shown below.

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Quick Boot

Disabled - Set this value to allow the BIOS to perform all POST tests.
Enabled - Set this value to allow the BIOS to skip certain POST tests to boot faster.

Quiet Boot

Disabled - Set this value to allow the computer system to display the POST messages.
Enabled - Set this value to allow the computer system to display the OEM logo.

Bootup Num-Lock

Set this value to allow the Number Lock setting to be modified during boot up.
Off - This option does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard will light up when the Number Lock is engaged.
On - Set this value to allow the Number Lock on the keyboard to be enabled automatically when the computer system is boot up. This allows the immediate use of 10-keys numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard will be lit.

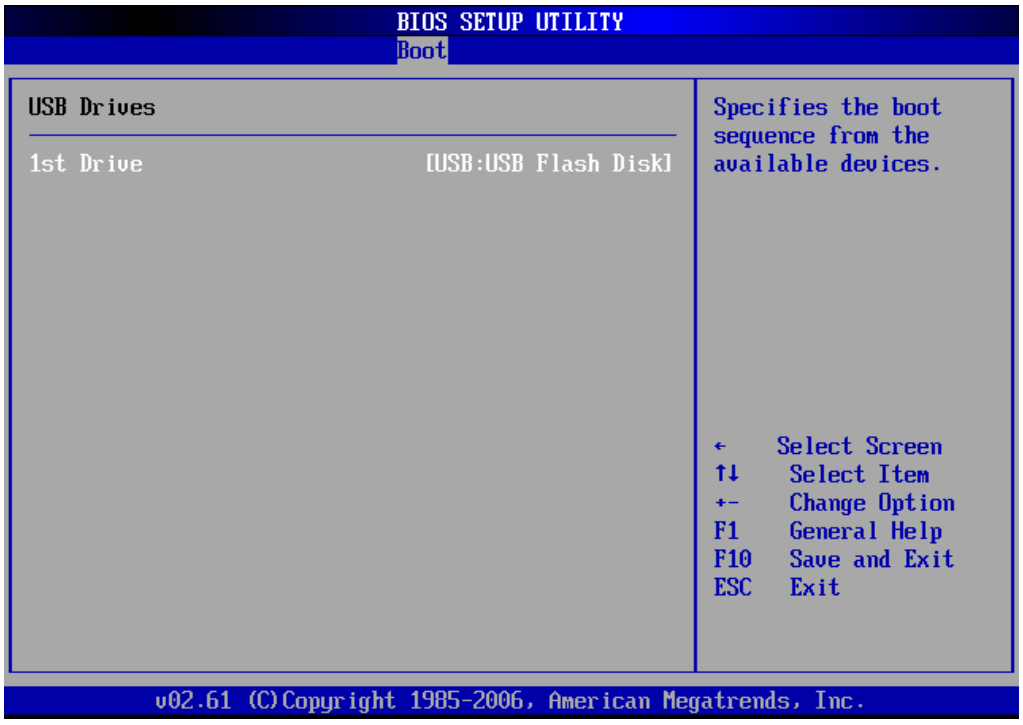
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Boot Device Priority

Set the boot device options to determine the sequence in which the computer checks which device to boot from.

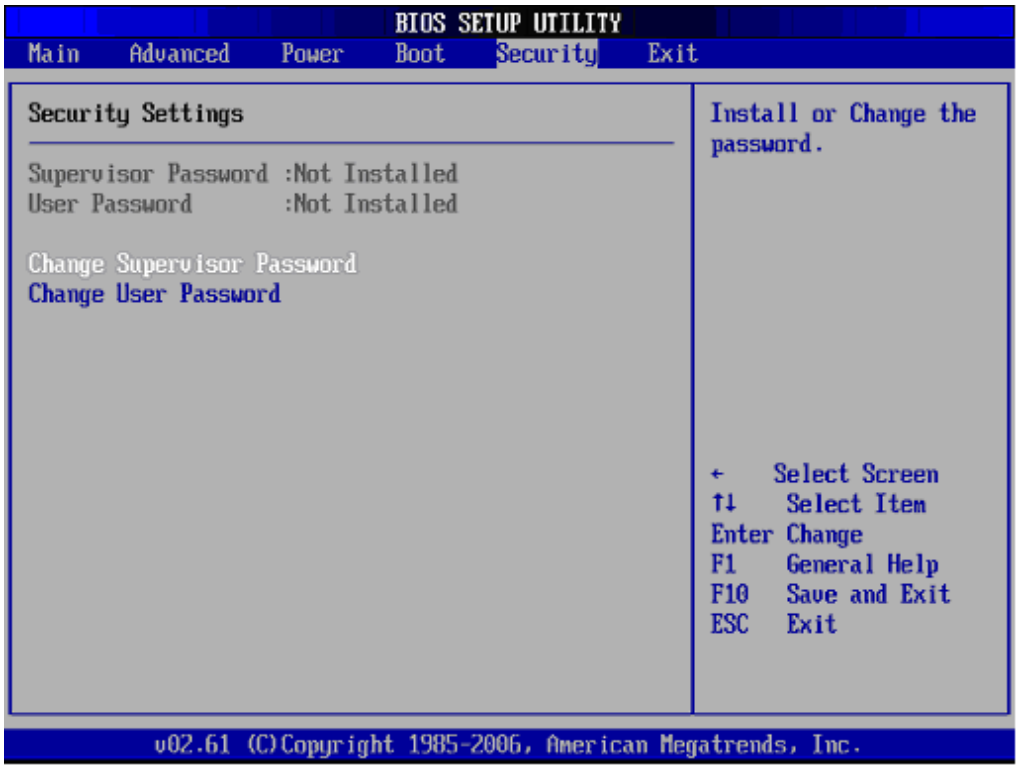
Boot Device Groups

The Boot devices are listed in groups by device type. First press <Enter> to enter the sub-menu. Then you may use the arrow keys to select the desired device, then press <+>, <-> or <PageUp>, <PageDown> key to move it up/down in the priority list. For example, USB storage disks will be listed as “USB Drives” in the sub-menu as below. Only the first device in each device group will be available for selection in the Boot Device Priority option.



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8.6 Security Setup



8.6.1 Password Support

Two Levels of Password Protection

Provides both a Supervisor and a User password. If you use both passwords, the Supervisor password must be set first.

The system can be configured so that all users must enter a password every time the system boots or when Setup is executed, using either or either the Supervisor password or User password.

The Supervisor and User passwords activate two different levels of password security. If you select password support, you are prompted for a one to six character password. Type the password on the keyboard. The password does not appear on the screen when typed. Make sure you write it down. If you forget it, you must drain NVRAM and re-configure.

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Remember the Password

Keep a record of the new password when the password is changed. If you forget the password, you must erase the system configuration information in NVRAM.

Select Security Setup from the Setup main BIOS setup menu. Security Setup options, such as password protection and virus protection, are described in this section. To access the sub menu for the following items, select the item and press < Enter >:o Change Supervisor Password

- Change Supervisor Password

- Change User Password

Supervisor Password

Indicates whether a supervisor password has been set.

User Password

Indicates whether a user password has been set.

Change Supervisor Password

Select this option and press < Enter > to access the sub menu. You can use the sub menu to change the supervisor password.

Change User Password

Select this option and press < Enter > to access the sub menu. You can use the sub menu to change the user password.

8.6.2 Change Supervisor Password

Select Change Supervisor Password from the Security Setup menu and press < Enter >.

```
Enter New Password:
```

Type the password and press < Enter >. The screen does not display the characters entered. Retype the password as prompted and press < Enter >. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after setup completes.

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8.6.3 Change User Password

Select Change User Password from the Security Setup menu and press < Enter >.

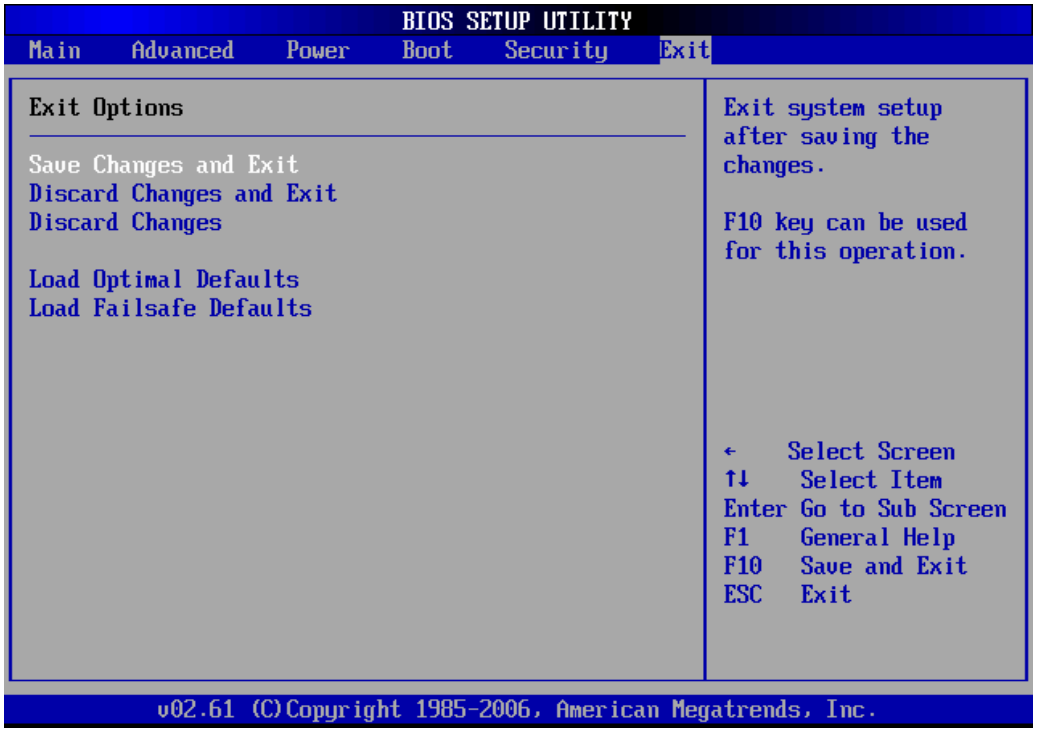
```
Enter New Password:
```

Type the password and press < Enter >. The screen does not display the characters entered. Retype the password as prompted and press < Enter >. If the password confirmation is incorrect, an error message appears. The password is stored in NVRAM after setup completes.

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8.7 Exit Menu

Select the *Exit* tab from the setup screen to enter the Exit BIOS Setup screen. You can display an Exit BIOS Setup option by highlighting it using the < Arrow > keys. The Exit BIOS Setup screen is shown below.



Save Changes and Exit

When you have completed the system configuration changes, select this option to leave Setup and reboot the computer so the new system configuration parameters can take effect. Select Exit Saving Changes from the Exit menu and press < Enter >.

```
Save Configuration Changes and Exit Now?

[Ok]  [Cancel]
```

appears in the window. Select Ok to save changes and exit.

Discard Changes and Exit

Select this option to quit Setup without making any permanent changes to the system configuration. Select Exit Discarding Changes from the Exit menu and press <Enter>.

```
Discard Changes and Exit Setup Now?

[Ok]  [Cancel]
```

appears in the window. Select *Ok* to discard changes and exit.

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Discard Changes

Select Discard Changes from the Exit menu and press < Enter >.

Select *Ok* to discard changes.

Load Optimal Defaults

Automatically sets all Setup options to a complete set of default settings when you Select this option. The Optimal settings are designed for maximum system performance, but may not work best for all computer applications. In particular, do not use the Optimal Setup options if your computer is experiencing system configuration problems.

Select Load Optimal Defaults from the Exit menu and press < Enter >.

Select *Ok* to load optimal defaults.

Load Failsafe Defaults

Automatically sets all Setup options to a complete set of default settings when you Select this option. The Failsafe settings are designed for maximum system stability, but not maximum performance. Select the Fail-Safe Setup options if your computer is experiencing system configuration problems.

Select Load Fail-Safe Defaults from the Exit menu and press < Enter >.

```
Load Fail-Safe Defaults?

[Ok]  [Cancel]
```

appears in the window. Select Ok to load Fail-Safe defaults.

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9 BIOS Checkpoints, Beep Codes

This section of this document lists checkpoints and beep codes generated by AMIBIOS. The checkpoints defined in this document are inherent to the AMIBIOS generic core, and do not include any chipset or board specific checkpoint definitions.

Checkpoints and Beep Codes Definition

A checkpoint is either a byte or word value output to I/O port 80h. The BIOS outputs checkpoints throughout bootblock and Power-On Self Test (POST) to indicate the task the system is currently executing. Checkpoints are very useful for debugging problems that occur during the preboot process.

Beep codes are used by the BIOS to indicate a serious or fatal error. They are used when an error occurs before the system video has been initialized, and generated by the system board speaker.

Viewing BIOS Checkpoints

Viewing all checkpoints generated by the BIOS requires a checkpoint card, also referred to as a "POST Card" or "POST Diagnostic Card". These are ISA or PCI add-in cards that show the value of I/O port 80h on a LED display.

Some computers display checkpoints in the bottom right corner of the screen during POST. This display method is limited, since it only displays checkpoints that occur after the video card has been activated.

Keep in mind that not all computers using AMIBIOS enable this feature. In most cases, a checkpoint card is the best tool for viewing AMIBIOS checkpoints.



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9.1 Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS:



Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs from add-in PCI devices.

Checkpoint	Description
Before D0	If boot block debugger is enabled, CPU cache-as-RAM functionality is enabled at this point. Stack will be enabled from this point.
D0	Early Boot Strap Processor (BSP) initialization like microcode update, frequency and other CPU critical initialization. Early chipset initialization is done.
D1	Early super I/O initialization is done including RTC and keyboard controller. Serial port is enabled at this point if needed for debugging. NMI is disabled. Perform keyboard controller BAT test. Save power-on CPUID value in scratch CMOS. Go to flat mode with 4GB limit and GA20 enabled.
D2	Verify the boot block checksum. System will hang here if checksum is bad.
D3	Disable CACHE before memory detection. Execute full memory sizing module. If memory sizing module not executed, start memory refresh and do memory sizing in Boot block code. Do additional chipset initialization. Re-enable CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM. Copies compressed boot block code to memory in right segments. Copies BIOS from ROM to RAM for faster access. Performs main BIOS checksum and updates recovery status accordingly.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. If BIOS recovery is necessary, control flows to checkpoint E0. See Bootblock Recovery Code Checkpoints section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See POST Code Checkpoints section of document for more information.
DC	System is waking from ACPI S3 state
E1-E8, EC-EE	OEM memory detection/configuration error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next.

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9.2 Bootblock Recovery Code Checkpoints

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS:



Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs From add-in PCI devices.

Checkpoint	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L1 cache is enabled.
E9	Set up floppy controller and data. Attempt to read from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
F5	Disable L1 cache.
FA	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
F4	The recovery file size does not equal the found flash part size.
FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

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9.3 POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS preboot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS:



Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs From add-in PCI devices.

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer.Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
07	Fixes CPU POST interface calling pointer.
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start -- Disable Cache – Init Local APIC
C1	Set up boot strap processor Information
C2	Set up boot strap processor for POST
C5	Enumerate and set up application processors
C6	Re-enable cache for boot strap processor
C7	Early CPU Init Exit
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
20	Relocate System Management Interrupt vector for all CPU in the system.
24	Uncompress and initialize any platform specific BIOS modules. GPNV is initialized at this checkpoint.
2A	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.

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POST Code Checkpoints cont'd:

Checkpoint	Description
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information. USB controllers are initialized at this point.
39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, ... etc.) successfully installed in the system and update the BDA, EBDA...etc.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory. Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to the user and gets the user response for error.
87	Execute BIOS setup if needed / requested. Check boot password if installed.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disable NMI as selected
90	Initialization of system management interrupt by invoking all handlers. *Please note this checkpoint comes right after checkpoint 20h*
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module. Display boot option popup menu.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector.
AB	Prepare BBS for Int 19 boot. Init MP tables.
AC	End of POST initialization of chipset registers. De-initializes the ADM module.
B1	Save system context for ACPI. Prepare CPU for OS boot including final MTRR values.
00	Passes control to OS Loader (typically INT19h).

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9.4 OEM POST Error Checkpoints

Checkpoints from the range 61h to 70h are reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next.

9.5 DIM Code Checkpoints

The Device Initialization Manager (DIM) gets control at various times during BIOS POST to initialize different system busses. The following table describes the main checkpoints where the DIM module is accessed:



Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs from add-in PCI devices.

Checkpoint	Description
2A	Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function 1); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI- PCI bridges, and noncompliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all onboard peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.

While control is in the different functions, additional checkpoints are output to port 80h as a word value to identify the routines under execution. The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two fields. The details of the high byte of these checkpoints are as follows:

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HIGH BYTE XY

The upper nibble ‘X’ indicates the function number that is being executed. ‘X’ can be from 0 to 7.

0 = func#0, disable all devices on the BUS concerned.
1 = func#1, static devices initialization on the BUS concerned.
2 = func#2, output device initialization on the BUS concerned.
3 = func#3, input device initialization on the BUS concerned.
4 = func#4, IPL device initialization on the BUS concerned.
5 = func#5, general device initialization on the BUS concerned.
6 = func#6, error reporting for the BUS concerned.
7 = func#7, add-on ROM initialization for all BUSes.
8 = func#8, BBS ROM initialization for all BUSes.

The lower nibble ‘Y’ indicates the BUS on which the different routines are being executed. ‘Y’ can be from 0 to 5.

0 = Generic DIM (Device Initialization Manager).
1 = Onboard System devices.
2 = ISA devices.
3 = EISA devices.
4 = ISA PnP devices.
5 = PCI devices.

9.6 ACPI Runtime Checkpoints

ACPI checkpoints are displayed when an ACPI capable operating system either enters or leaves a sleep state. The following table describes the type of checkpoints that may occur during ACPI sleep or wake events:



Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs from add-in PCI devices.

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9.7 Boot Block Beep Codes

No. of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
3	Base Memory error
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

9.8 POST BIOS Beep Codes

No. of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
3	Base memory read/write test error
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

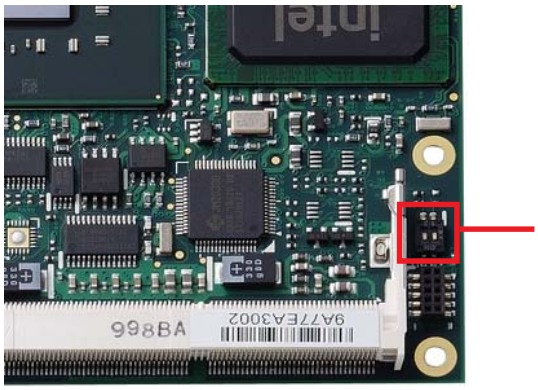
9.9 Troubleshooting POST BIOS Beep Codes

No. of Beeps	Description
1, 2 or 3	Reseat the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards except the video adapter. - If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. - If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem happens again. This will reveal the malfunctioning card.
8	If the system video adapter is an add-in card, replace or reseat the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

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Appendix A: **SDVO/DP/HDMI Switches**

Switches SW1 and SW2 are used to set the Concurrent DisplayPort Configuration Strap Controls of the Express-MG. These settings control SDVO, PCI Express Graphics, DisplayPort (DP), and HDMI output.



*DP Port-B, HDMI Port-B, PCI Express Graphics (default)**

	Pin1	Pin2
SW1	OFF	ON
SW2	ON	OFF

*DP Port-C, HDMI Port-C, PCI Express Graphics**

	Pin1	Pin2
SW1	OFF	ON
SW2	ON	ON

*DP Port-D, HDMI Port-D, PCI Express Graphics**

	Pin1	Pin2
SW1	ON	ON
SW2	ON	OFF

*Set JP6 on the Express-BASE Carrier Board to *PEG Enabled* (short pins 2 & 3).

*SDVO***

	Pin1	Pin2
SW1	ON	ON
SW2	OFF	OFF

**Set JP6 on the Express-BASE Carrier Board to *PEG Disabled* (short pins 1 & 2). Set Boot Display Device in BIOS to *CRT + SDVO* or *SDVO*.

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Important Safety Instructions

For user safety, please read and follow all instructions, **warnings**, **cautions**, and **notes** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:

  - Turn off power and unplug any power cords/cables.

- To avoid electrical shock and/or damage to equipment:

  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.
- A Lithium-type battery may be provided for uninterrupted, backup or emergency power.



Risk of explosion if battery is replaced by an incorrect type. Dispose of used batteries according to the instructions.

- Equipment must be serviced by authorized technicians when:

  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

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Contact us should you require any service or assistance.

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