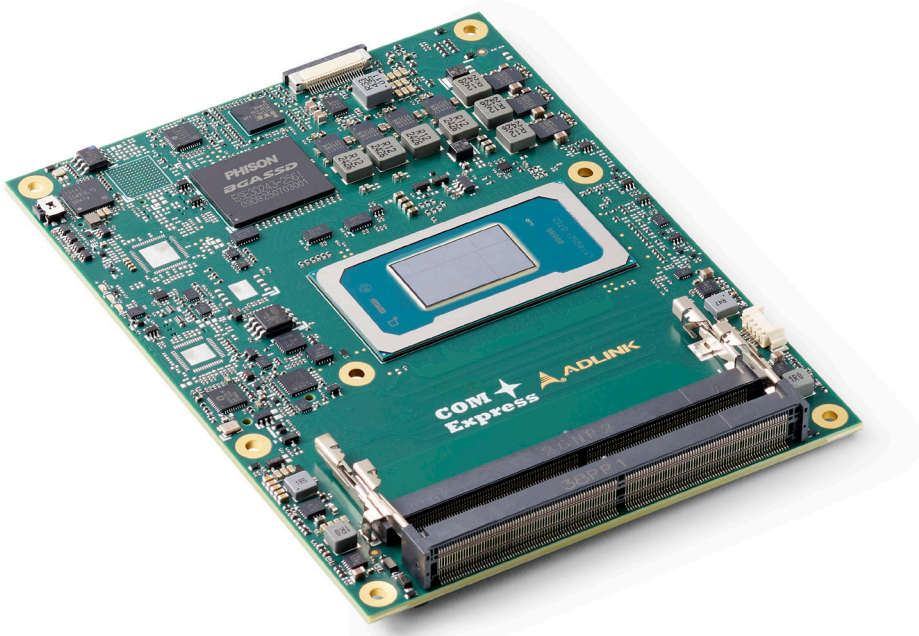
Express-PTL

User's Guide



COM Express®

Revision: 0.2 Preliminary
Date: 2026-09-03
Part Number: 50M-72141-1000

ADLINK
LEADING EDGE AI COMPUTING

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Revision History

Revision	Description	Date	Author
0.1	Preliminary release	2026-07-02	CC
0.2	System resource, BIOS settings, and BIOS checkpoints updated	2026-09-03	AL

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Preface

Disclaimer

Information in this document is provided in connection with ADLINK products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in ADLINK´s Terms and Conditions of Sale for such products, ADLINK assumes no liability whatsoever, and ADLINK disclaims any express or implied warranty, relating to sale and/or use of ADLINK products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. If you intend to use ADLINK products in or as medical devices, you are solely responsible for all required regulatory compliance, including, without limitation, Title 21 of the CFR (US), Directive 2007/47/EC (EU), and ISO 13485 & 14971, if any. ADLINK may make changes to specifications and product descriptions at any time, without notice.

Environmental Responsibility

ADLINK is committed to fulfil its social responsibility to global environmental preservation through compliance with the European Union's Restriction of Hazardous Substances (RoHS) directive and Waste Electrical and Electronic Equipment (WEEE) directive. Environmental protection is a top priority for ADLINK. We have enforced measures to ensure that our products, manufacturing processes, components, and raw materials have as little impact on the environment as possible. When products are at their end of life, our customers are encouraged to dispose of them in accordance with the product disposal and/or recovery programs prescribed by their nation or company.





California Proposition 65 Warning: This product can expose you to chemicals including acrylamide, arsenic, benzene, cadmium, Tris(1,3-dichloro-2-propyl)phosphate (TDCPP), 1,4-Dioxane, formaldehyde, lead, DEHP, styrene, DINP, BBP, PVC, and vinyl materials, which are known to the State of California to cause cancer, and acrylamide, benzene, cadmium, lead, mercury, phthalates, toluene, DEHP, DIDP, DnHP, DBP, BBP, PVC, and vinyl materials, which are known to the State of California to cause birth defects or other reproductive harm. For more information go to www.P65Warnings.ca.gov.

Trademarks

Product names mentioned herein are used for identification purposes only and may be trademarks / registered trademarks of respective companies. The terms HDMI, HDMI High-Definition Multimedia Interface, HDMI trade dress and the HDMI Logos are trademarks or registered trademarks of HDMI Licensing Administrator, Inc.

Copyright © 2026 ADLINK Technology Incorporated

This document contains proprietary information protected by copyright. All rights are reserved. No part of this manual may be reproduced by any mechanical, electronic, or other means in any form without prior written permission of the manufacturer.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Safety Instructions

For user safety, please read and follow all Instructions, **WARNING**s, **CAUTION**s, and **NOTE**s marked in this manual and on the associated equipment before handling/operating the equipment.

Read these safety instructions carefully.

- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Conventions

The following conventions may be used throughout this manual, denoting special levels of information



Note: This information adds clarity or specifics to text and illustrations.



Caution: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.



Warning: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Getting Service

Ask an Expert: https://www.adlinktech.com/en/Askanexpert

ADLINK Technology, Inc.
No. 66, Huaya 1st Rd., Guishan District, Taoyuan City 333411, Taiwan
Tel: +886-3-216-5088
Fax: +886-3-328-5706
Email: service@adlinktech.com

Ampro ADLINK Technology, Inc.
6450 Via Del Oro, San Jose, CA 95119-1208, USA
Tel: +1-408-360-0200
Toll Free: +1-800-966-5200 (USA only)
Fax: +1-408-600-1189
Email: info@adlinktech.com

ADLINK Technology (China) Co., Ltd.
300 Fang Chun Rd., Zhangjiang Hi-Tech Park, Pudong New Area, Shanghai, 201203, China
Tel: +86-21-5132-8988
Fax: +86-21-5132-3588
Email: market@adlinktech.com

ADLINK Technology GmbH
Hans-Thoma-Strasse 8-10, 68163 Mannheim, Germany
Tel: +49-621-43214-0
Fax: +49-621 43214-30
Email: emea@adlinktech.com

Please visit the Contact page at www.adlinktech.com for information on how to contact the ADLINK regional office nearest you.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Table of Contents

Revision History 2

Preface 3

List of Figures 11

1. Introduction 12

2. Specifications 13
   - 2.1. Core System 13
   - 2.2. Video 14
     - 2.2.1 Display interface Support 15
   - 2.3. Audio 16
   - 2.4. Expansion Buses 16
   - 2.5. GbE Ethernet 17
   - 2.6. Multi I/O and Storage 17
   - 2.7. Trusted Platform Module (TPM) 19
   - 2.8. NVMe SSD 19
   - 2.9. SEMA Board Controller 19
   - 2.10. Debug 19
   - 2.11. Power 19
   - 2.12. Mechanical and Environmental 20

3. Block Diagram 21

4. Pinout and Signal Descriptions 22
   - 4.1. Pin Summary 22
   - 4.2. Signal Terminology Descriptions 27
   - 4.3. AB Connector Signal Descriptions 28
     - 4.3.1 Audio 28
     - 4.3.2 Analog VGA 29
     - 4.3.3 LVDS or eDP 30
     - 4.3.4 Gigabit Ethernet 33
     - 4.3.5 SATA 34
     - 4.3.6 PCI Express 35

Copyright © 2026 ADLINK Technology, Inc.
ADLINK LEADING EDGE AI COMPUTING

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.3.7 LPC Bus 37
4.3.8 USB 38
4.3.9 SPI Bus (BIOS only) 40
4.3.10 Miscellaneous 41
4.3.11 SMBus 42
4.3.12 I²C Bus 42
4.3.13 General Purpose I/O (GPIO) 43
4.3.14 Serial Interface Signals 43
4.3.15 Power and System Management 44
4.3.16 Power and Ground 45
4.4. CD Connector Signal Descriptions 46
4.4.1 USB 3.0 Extensions 46
4.4.2 PCI Express 47
4.4.3 DDI1 Port 48
4.4.4 DDI2 Port 51
4.4.5 DDI3 Port 54
4.4.6 PCIe Graphics Port (PEG) 57
4.4.7 Module Type Definition 60
4.4.8 Power and Ground 61

5. Additional Features 62
5.1. Debug Connector 63
5.2. Status LEDs 64
5.3. Exception Codes 66
5.4. Fan Connector 67
5.5. BIOS Default Reset Button 68
5.6. BIOS Boot Select 69

6. System Resource 70
6.1. System Resource Map 70
6.2. I/O Map 72
6.3. Interrupt Request (IRQ) Lines 75
6.4. PCI Configuration Space Map 77
6.5. PCI Interrupt Routing Map 78

7. BIOS Settings 80
7.1. Menu Structure 80
7.2. Main 81
7.2.1 Bios Information 81
7.2.2 System Information 81

Copyright © 2026 ADLINK Technology, Inc.
ADLINK LEADING EDGE AI COMPUTING
LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

7.2.3 Board Information 82
7.2.4 System Data and Time 83
7.3. Advanced 83
7.3.1 RC ACPI Settings 83
7.3.2 Intel(R) Time Coordinated Computing 83
7.3.3 CPU Configuration 84
7.3.4 Power & Performance 87
7.3.5 Graphics Configuration 90
7.3.6 SATA Configuration 92
7.3.7 Power Management 93
7.3.8 System Management 94
7.3.9 Thermal Management 96
7.3.10 AMI Graphic Output Protocol Policy 99
7.3.11 Watchdog Timer 99
7.3.12 USB Configuration 100
7.3.13 Super IO Configuration 101
7.3.14 Serial Port Console Redirection 106
7.3.15 Miscellaneous 108
7.3.16 Network Stack Configuration 108
7.3.17 NVMe Configuration 108
7.3.18 Trusted Computing 109
7.4. Chipset 110
7.4.1 Chipset > System Agent (SA) Configuration 110
7.4.2 Chipset > PCH-IO Configuration 115
7.5. Security 124
7.5.1 Secure->Secure Boot 124
7.6. Boot 125
7.7. Save & Exit 126
7.8. MEBx (Corporate only) 126

8. BIOS Checkpoints, Beep Codes (update it before product go to mass production) 127
8.1 Status Code Ranges 128
8.2 Standard Status Codes 128
8.2.1 SEC Phase 128
8.2.2 PEI Phase 129
8.2.3 DXE Status Codes 133
8.2.4 DXE Beep Codes 137
8.2.5 ACPI/ASL Checkpoint 137
8.3 OEM-reserved Checkpoint Ranges 138

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

9. Software Support 139
9.1. Windows 139
9.2. Ubuntu 24.04. LTS 139
9.3. Yocto Linux 64-bit 139
9.4. SEMA API 139

10. Mechanical and Thermal 140
10.1. Module Dimensions – Top View 140
10.2. Module Dimensions – Bottom View 141
10.3. Module Dimensions – Side View 142
10.4. Height of Processor and Static Compressive Load 142
10.5. Thermal Solutions (update it before product go to mass production) 143
10.5.1 HTS-B 143
10.5.2 HTS-BT 143
10.5.3 THS-B 143
10.5.4 THS-BT 143
10.5.5 THSF-B 143
10.5.6 THSH-B 143
10.6. Board to Board Connectors 144
10.7. Mounting Method 146
10.8. Standoff Types 147
10.9. Installation (update it before product mass production) 148

Copyright © 2026 ADLINK Technology, Inc.
ADLINK LEADING EDGE AI COMPUTING
LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

List of Figures

Figure 1 – Module functional block diagram 21
Figure 2 – Module rear side row and pin numbering (the picture update later) 22
Figure 3 – Module feature locations 62
Figure 4 – cExpress-MTL and Debug Module 63

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

1. Introduction

Warning: this is an EA (early available) engineering manual, meaning contents might not properly reflect the actual/final version of the product

The Express-PTL is a COM Express® COM.0 R3.1 Basic Size Type 6 module based on the intel® Core Ultra series 3 platform that uses new Intel 18A process providing industry leading performance/watt and up to 180 TOPs AI prowess. The new-generation Core™ Ultra processors (formerly "Panther Lake H") support up to 16 cores (Ultra 7) at maximum 25W TDP, with performance cores, efficiency cores, and low-power efficiency cores improving multi-tasking ability. P-core drives high-performance and single-threaded tasks, E-core manages multi-threaded background processes to enhance overall system efficiency, and low-power E-core resides in the SoC tile to handle ultra-light tasks and maximize battery life.

Up to 2x DDR5 CSO-DIMMs, the module supports a maximum of 128GB memory capacity at up to 7200 MT/s. The SoC integrates the new intel X^e3 graphics enhancing graphic performance nearly 1.5 times than its predecessor. All CPU SKU offer built-in NPU to strengthen AI accelerator with up to 50 TOPs.

Following PICMG R3.1 specifications to provide all-around PCIe Gen4 support, 2.5G Ethernet connectivity, and USB 4.0 support (USB 4.0 function based on bios setting change and carrier design), the module delivers high-performance and powerful image processing capabilities at a low power consumption, making it ideal for applications requiring high computing power and fast response, including, but not limited to, video storage analytics, medical image presentation and analysis, intelligent surveillance, industrial automation and control, and smart robotics.

Panther Lake provides 25W TDP for all CPU SKU with two types of cTDP (12-45W and 15-65W) that can be chosen from. Low SoC power consumption means more suitable for use on portable devices, such as handheld ultrasound devices and drones. Integrated with a powerful GPU, a new NPU for dedicated AI acceleration, along with its built-in PCIe gen 4 NVMe storage, it effectively reduces system cost while improving the system's AI processing ability.

Input/output features include up to 20 PCIe Gen4 lanes, 1x onboard 2.5-Gigabit Ethernet port, 4x USB 3.2/2.0 ports with up to 10Gb/s, 4x SATA 6 Gb/s ports, 4x independent displays with up to 8K resolution. Additionally, functions like General Purpose SPI (GP_SPI), 1x MIPI-CSI connector to support camera and on board NVMe storage up to 1T capacity, SMBus and I2C, etc. are also supported. The module is equipped with SPI AMI EFI BIOS with CMOS backup, supporting embedded features such as remote console, hardware monitor, and watchdog timer. It packs 2x BIOS ROMs on board to for backup implementation.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

2. Specifications

2.1. Core System

CPU

Intel® Core™ Ultra Processors Series 3 (formerly "Panther Lake H")

- Intel® Core™ Ultra X9 388H 5.1/2.1GHz, 12Xe, 25W with 15-65W cTDP (16C/16T, vPro)
- Intel® Core™ Ultra 9 386H 4.9/2.1GHz, 4Xe, 25W with 15-65W cTDP (16C/16T, vPro)
- Intel® Core™ Ultra X7 368H 5.0/2.0GHz, 12Xe, 25W with 15-65W cTDP (16C/16T, vPro)
- Intel® Core™ Ultra 7 366H 4.8/2.0GHz, 4Xe, 25W with 15-65W cTDP (16C/16T, vPro)
- Intel® Core™ Ultra 7 365 4.8/2.4GHz, 4Xe, 25W with 12-45W cTDP (8C/8T, vPro)
- Intel® Core™ Ultra X7 358H 4.8/1.9GHz, 12Xe, 25W with 15-65W cTDP (16C/16T)
- Intel® Core™ Ultra 7 356H 4.7/1.9GHz, 4Xe, 25W with 15-65W cTDP (16C/16T)
- Intel® Core™ Ultra 7 355 4.7/2.3GHz, 4Xe, 25W with 12-45W cTDP (8C/8T)
- Intel® Core™ Ultra 5 338H 4.6/1.9GHz, 12Xe, 25W with 15-65W cTDP (12C/12T, vPro)
- Intel® Core™ Ultra 5 336H 4.5/1.9GHz, 4Xe, 25W with 15-65W cTDP (12C/12T, vPro)
- Intel® Core™ Ultra 5 335 4.5/2.2GHz, 4Xe, 25W with 12-45W cTDP (8C/8T, vPro)
- Intel® Core™ Ultra 5 325 4.4/2.1GHz, 4Xe, 25W with 12-45W cTDP (8C/8T)
- Intel® Core™ Ultra 5 332 4.3/2.5GHz, 2Xe, 25W with 12-45W cTDP (6C/6T, vPro)
- Intel® Core™ Ultra 5 322 4.3/2.5GHz, 2Xe, 25W with 12-45W cTDP (6C/6T)

Wide-Temperature Range

- Intel® Core™ Ultra X7 358HR TBD/TBD GHz, 12Xe, 25W with 15-65W cTDP (16C/16T, vPro)
- Intel® Core™ Ultra 7 366HR TBD/TBD GHz, 4Xe, 25W with 15-65W cTDP (16C/16T, vPro)

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

- Intel® Core™ Ultra 7 365RE TBD/TBD GHz, 4Xe, 25W with 12-45W cTDP (8C/8T, vPro)
- Intel® Core™ Ultra 5 336HRE TBD/TBD GHz, 4Xe, 25W with 15-65W cTDP (12C/12T, vPro)
- Intel® Core™ Ultra 5 335RE TBD/TBD GHz, 4Xe, 25W with 12-45W cTDP (8C/8T, vPro)

Memory

Up to 128GB DDR5, dual memory channel in 2x SODIMM sockets, maximum 64GB per socket, IBECC

Up to 7200 MT/s memory speed

2x SODIMM sockets on top side.

Cache (L3)

18MB: 388H, 386H, 368H, 366H, 358H, 356H, 338H, 336H, 358HR, 366HRE, 336HRE

12MB: 365, 355, 335, 325, 332, 322, 365RE, 335RE

Embedded BIOS

AMI Aptio V UEFI with CMOS backup in 32 MB SPI BIOS

2.2. Video

GPU

Intel® X^{e}3 Graphics architecture with up to 12 Cores

Display Interface

4 independent and simultaneous combinations of DisplayPort/HDMI®/LVDS/eDP/VGA and display alternative mode through USB4/Thunderbolt4 graphics outputs (4x 4K @60Hz, up to 8K@60Hz). (eDP optional in place of LVDS, VGA optional in place of DDI 3)

Playback of high-definition content including Blu-ray Disc and Blu-ray Disc 3D content using HDMI (1.4a spec compliant with 3D)

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Graphics Acceleration

DirectX 12 Video Acceleration (DXVA)/Open GL 4.6/Vulkan 1.2 and one VPL support for accelerated video processing

Video Decode

8K60 12b 4:4:4 HEVC

8K60 10b 4:4:4 AV1 (Windows support only)

8K60 10b 4:4:4 VP9

8K30 10b 4:2:0 VVC

4K60 10b 4:2:2 AVC

Video Encode

8K60 12b 4:4:4 HEVC

8K60 10b 4:4:4 AV1 (Windows support only)

4K60 8b 4:2:0 AVC

Note: Availability of features is dependent on the operating system used (Windows 10 64-bit, Linux 64-bit).

2.2.1 Display interface Support

DDI x3: Digital Display Ports (DDI) support DisplayPort 2., HDMI 2.1 or DVI.

LVDS: Single/dual channel 18/24-bit LVDS through eDP to LVDS IC, supports DE mode and Hsync/Vsync mode.

Max. Resolution 1920x1200@60Hz in dual mode. Pixel clock frequency up to 112 MHz. VESA and JEIDA panel data formats supported.

VGA: VGA BOM option support in place of DDI 3; max. resolution 1920x1200@60Hz

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

2.3. Audio

Intel® HD Audio integrated
Located on carrier Express-BASE6 or Express-BASE6 R3.1 (ALC886 standard support)

2.4. Expansion Buses

8 PEG Express Gen4: PEG Lane 0-7 (based on CPU SKU, H484 and H404 ET SKU support))

PCIe reference clock can be PCIE_CK_REF6 (pin B29/B30).

4 PEG Express Gen4: One PEG Express Gen 4 at PEG Lane 8-11

4 PCI Express Gen4: Lanes 0-3 (four controllers, configurable to 1 x4, 2 x2 and 4 x1)

2 PCI Express Gen4: Lane 4-5 (one controller only, configurable to 1 x2 and 2 x1)

Note: 1. PCIe Gen4 support also depends on carrier board design.

2. PEG lane 8-11 can be adjust at bios setup manual and sacrifice SATA [0:4] can combines as 1 PEG GEN 4 x4.

3. PEF 0-7 and 8-11 are recommended to be used for discrete graphics and storage purposes only.

Other: SMBus (system), I^2C (user), LPC bus (via eSPI to LPC bridge IC).

I^2C from CPU is supported by BOM option and project basis

SMBus from EC (embedded controller) is supported by BOM option and project basis

Additional GP_SPI (general purpose SPI by project basis)

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

2.5. GbE Ethernet

Intel® Ethernet Controller I226 Series (V, IT or LM version)

Up to 2.5GbE, 1000/100/10 Mbit/s connections

IT version supports TSN feature on Linux OS, GbE0_SDP available if TSN support enabled (TBD)

Note: Ethernet can be sacrificed and configured as PCIe port 7

2.6. Multi I/O and Storage

USB4 x2: Build option (HW and BIOS) supported by project basis in place of DDI channels. Maximum 2x USB4 by using DDI 1 and DDI 2 channels.

USB4 support also requires re-timer and PD on carrier.

Note: Capable of **TBT4**. Please contact your local ADLINK representative for details.

USB 3.2 Gen2 x4: USB port 0, 1, 2, 3 support

USB 2.0 x4: USB port 4, 5, 6, 7 support

SuperSpeed, High-Speed, Full-Speed and Low-Speed USB signaling

Up to 10Gb/s and also depends on carrier board design

USB_OC pins share the same source, from SoC.

Note: 1. Carrier board must be designed for Gen2 operation.

2. USB 0,1,2,3 are backward compatible with USB 2.0/1.1.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

SATA x4: Speed up to 6Gb/s (SATA 0,1,2,3)

Note: SATA port can be changed as one PEG[8:11] by bios setup menu.

UART

2x UART interfaces SER0 and SER1 RX/TX on module

Console Redirection COM 1 or COM 2 selectable in BIOS

SER0, SER1 from CPU UART are supported by BOM option and project basis

Up to 4 serial ports supported by standard BIOS, including Super I/O on carrier board

COM Port	Description	IRQ	Address	Console Redirection Support
COM 1	Supported by module (SER0, A98/A99), via embedded controller	4	0x3F8	Yes
COM 2	Supported by module (SER1, A101/A102), via embedded controller	3	0x2F8	Yes
COM 3	Supported by Super I/O (W83627DHG) on carrier board	5	0x240	Yes
COM 4	Supported by Super I/O (W83627DHG) on carrier board	7	0x248	Yes

GPIO ~~or SD~~

4 GPO and 4 GPI (GPI with interrupt, TBC)

GPI and GPO from CPU GPIO are supported by BOM option and project basis

MIPI-CSI x1: 4 Lanes MIPI-CSI interface and supports camera video capture up to 750MP/s

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

2.7. Trusted Platform Module (TPM)

Chipset: Infineon solution

Type: TPM 2.0 (SPI bus-based)

2.8. NVMe SSD

NVMe SSD x1: Support PCIe Gen 4 x4 and a max. capacity of up to 1TB

2.9. SEMA Board Controller

Supports: Voltage/current monitoring, power sequence debug support, AT/ATX mode control, logistics and forensic information, general purpose I2C, failsafe BIOS (dual BIOS, opt. support), watchdog timer and fan control

2.10. Debug

30-pin flat cable connector for use with DB-30 x86 debug module
Supports embedded controller access, SPI BIOS flashing, internal power rail test points, debug LEDs

2.11. Power

Power Modes: AT and ATX mode (AT mode startup controlled by SEMA Board Controller)

Standard Voltage Input: AT: 12V±5% or ATX: 12V±5% / 5Vsb ±5%

Wide Voltage Input: AT: 8.5-20V or ATX: 8.5-20V / 5Vsb ±5% (only for standard operating temperature)

Power Management: ACPI 5.0 compliant

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Power States: C0-C6, S0, S5, S5 ECO mode (Wake-on-USB S3/S4, WoL S3/S4/S5). ECO Mode support for deep S5 for 5Vsb power saving

Power Consumption
Please contact our ADLINK representative for the document "COM Express Module Power Consumption."

2.12. Mechanical and Environmental

Form Factor and specification

PICMG COM Express Rev 3.1 (COM.0 R3.1), Type 6, Compact size 95 x 95 mm

Operating Temperature

Standard	0°C to 60°C	Storage: -20°C to 80°C
Extreme Rugged (TBC)	-40°C to 85°C	Storage: -40°C to 85°C

Humidity

5-90% RH operating, non-condensing, 5-95% RH storage (and operating with conformal coating)

Shock and Vibration

IEC 60068-2-64 and IEC-60068-2-27
MIL-STD-202F, Method 213B, Table 213-I, Condition A and Method 214A, Table 214-I, Condition D

HALT Tested

Thermal Stress, Vibration Stress, Thermal Shock and Combined Test

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3. Block Diagram

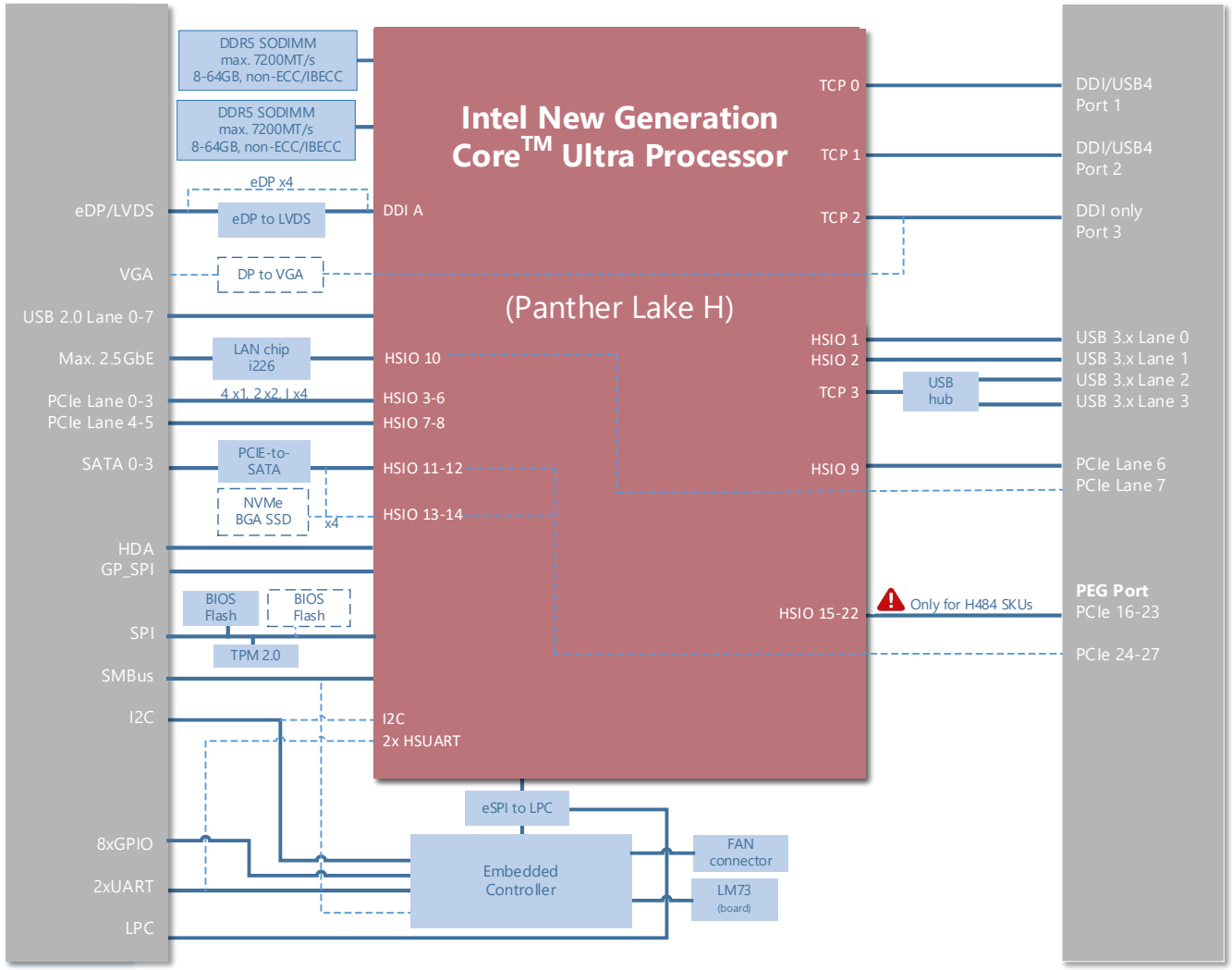


Figure 1 – Module functional block diagram

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4. Pinout and Signal Descriptions

4.1. Pin Summary

The table below is a comprehensible list of all signal pins supported on the dual 220-pin COM Express connectors as defined for Type 6 in the PICMG COM.0 R3.1 specification. Signals described in the specification but not supported on the Express-PTL are strikethrough ~~STRIKETHROUGH~~

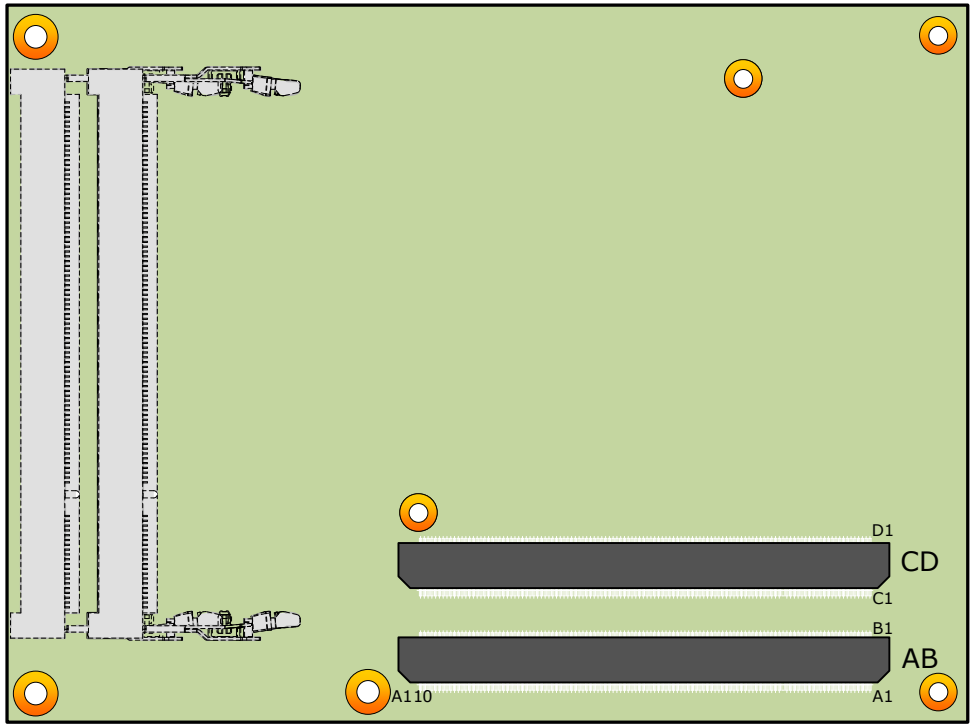


Figure 2 – Module rear side row and pin numbering (the picture update later)

Note: The 1x SO-DIMM sockets (grey color) are located on top side.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Row A			Row B			Row C			Row D	
A1	GND (fixed)		B1	GND (fixed)		C1	GND (fixed)		D1	GND (fixed)
A2	GBE0_MDI3-		B2	GBE0_ACT#		C2	GND		D2	GND
A3	GBE0_MDI3+		B3	LPC_FRAME#/ESPI_CS0#		C3	USB_SSRX0-		D3	USB_SSTX0-
A4	GBE0_LINK_MID#		B4	LPC_AD0/ESPI_IO_0		C4	USB_SSRX0+		D4	USB_SSTX0+
A5	GBE0_LINK_MAX#		B5	LPC_AD1/ESPI_IO_1		C5	GND		D5	GND
A6	GBE0_MDI2-		B6	LPC_AD2/ESPI_IO_2		C6	USB_SSRX1-		D6	USB_SSTX1-
A7	GBE0_MDI2+		B7	LPC_AD3/ESPI_IO_3		C7	USB_SSRX1+		D7	USB_SSTX1+
A8	GBE0_LINK#		B8	LPC_DRQ0#/ESPI_ALERT0#		C8	GND		D8	GND
A9	GBE0_MDI1-		B9	LPC_DRQ1#/ESPI_ALERT1#		C9	USB_SSRX2-		D9	USB_SSTX2-
A10	GBE0_MDI1+		B10	LPC_CLK/ESPI_CK		C10	USB_SSRX2+		D10	USB_SSTX2+
A11	GND (fixed)		B11	GND (fixed)		C11	GND (fixed)		D11	GND (fixed)
A12	GBE0_MDI0-		B12	PWRBTN#		C12	USB_SSRX3-		D12	USB_SSTX3-
A13	GBE0_MDI0+		B13	SMB_CK		C13	USB_SSRX3+		D13	USB_SSTX3+
A14	~~GBE0_CTREF~~		B14	SMB_DAT		C14	GND		D14	GND
A15	SUS_S3#		B15	SMB_ALERT#		C15	USB4_1_LSTX		D15	DDI1_CTRLCLK_AUX+ /USB4_1_AUX+
A16	SATA0_TX+		B16	SATA1_TX+		C16	USB4_1_LSRX		D16	DDI1_CTRLDATA_AUX- /USB4_1_AUX-
A17	SATA0_TX-		B17	SATA1_TX-		C17	USB4_RT_ENA		D17	USB4_PD_I2C_ALERT#
A18	SUS_S4#		B18	SUS_STAT#/ESPI_RESET#		C18	GND		D18	PMCALERT#
A19	SATA0_RX+		B19	SATA1_RX+		C19	PCIE_RX6+		D19	PCIE_TX6+
A20	SATA0_RX-		B20	SATA1_RX-		C20	PCIE_RX6-		D20	PCIE_TX6-
A21	GND (fixed)		B21	GND (fixed)		C21	GND (fixed)		D21	GND (fixed)
A22	SATA2_TX+		B22	SATA3_TX+		C22	PCIE_RX7+		D22	PCIE_TX7+
A23	SATA2_TX-		B23	SATA3_TX-		C23	PCIE_RX7-		D23	PCIE_TX7-
A24	SUS_S5#		B24	PWR_OK		C24	DDI1_HPD		D24	GND
A25	SATA2_RX+		B25	SATA3_RX+		C25	SML0_CLK		D25	GND
A26	SATA2_RX-		B26	SATA3_RX-		C26	SML0_DAT		D26	DDI1_PAIR0+ /USB4_1_SSTX0+
A27	BATLOW#		B27	WDT		C27	SML1_CLK		D27	DDI1_PAIR0- /USB4_1_SSTX0-
A28	(S)ATA_ACT#		B28	~~HDA_SDIN2~~/SNDW0_CLK		C28	SML1_DAT		D28	GND
A29	HDA_SYNC		B29	HDA_SDIN1/SNDW0_DAT		C29	USB4_PD_I2C_CLK		D29	DDI1_PAIR1+ /USB4_1_SSRX0+
A30	HDA_RST#		B30	HDA_SDIN0		C30	USB4_PD_I2C_DAT		D30	DDI1_PAIR1- /USB4_1_SSRX0-

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

A31	GND (fixed)		B31	GND (fixed)		C31	GND (fixed)		D31	GND (fixed)
A32	HDA_BITCLK		B32	SPKR		C32	DDI2_CTRLCLK_AUX+/USB4_2_AUX+		D32	DDI1_PAIR2+ /USB4_1_SSTX1+
A33	HDA_SDOUT		B33	I2C_CK		C33	DDI2_CTRLDATA_AUX/USB4_2_AUX-		D33	DDI1_PAIR2- /USB4_1_SSTX1-
A34	BIOS_DIS0#		B34	I2C_DAT		C34	DDI2_DDC_AUX_SEL		D34	DDI1_DDC_AUX_SEL
A35	THRMTRIP#		B35	THRM#		C35	USB4_2_LSTX		D35	USB4_2_LSRX

Row A			Row B			Row C			Row D	
A36	USB6-		B36	USB7-		C36	DDI3_CTRLCLK_AUX+		D36	DDI1_PAIR3+ /USB4_1_SSRX1+
A37	USB6+		B37	USB7+		C37	DDI3_CTRLDATA_AUX-		D37	DDI1_PAIR3- /USB4_1_SSRX1-
A38	USB_6_7_OC#		B38	USB_4_5_OC#		C38	DDI3_DDC_AUX_SEL		D38	GND
A39	USB4-		B39	USB5-		C39	DDI3_PAIR0+		D39	DDI2_PAIR0+ /USB4_2_SSTX0+
A40	USB4+		B40	USB5+		C40	DDI3_PAIR0-		D40	DDI2_PAIR0- /USB4_2_SSTX0-
A41	GND (fixed)		B41	GND (fixed)		C41	GND (fixed)		D41	GND (fixed)
A42	USB2-		B42	USB3-		C42	DDI3_PAIR1+		D42	DDI2_PAIR1+ /USB4_2_SSRX0+
A43	USB2+		B43	USB3+		C43	DDI3_PAIR1-		D43	DDI2_PAIR1- /USB4_2_SSRX0-
A44	USB_2_3_OC#		B44	USB_0_1_OC#		C44	DDI3_HPD		D44	DDI2_HPD
A45	USB0-		B45	USB1-		C45	GP_SPI_CS#		D45	GND
A46	USB0+		B46	USB1+		C46	DDI3_PAIR2+		D46	DDI2_PAIR2+ /USB4_2_SSTX1+
A47	VCC_RTC		B47	ESPI_EN#		C47	DDI3_PAIR2-		D47	DDI2_PAIR2- /USB4_2_SSTX1-
A48	RSMRST_OUT#		B48	~~USB0_HOST_PRSNT~~		C48	RSVD		D48	GND
A49	GBE0_SDP*		B49	SYS_RESET#		C49	DDI3_PAIR3+		D49	DDI2_PAIR3+ /USB4_2_SSRX1+
A50	LPC_SERIRQ/ESPI_CS1#		B50	CB_RESET#		C50	DDI3_PAIR3-		D50	DDI2_PAIR3- /USB4_2_SSRX1-
A51	GND (fixed)		B51	GND (fixed)		C51	GND (fixed)		D51	GND (fixed)
A52	PCIE_TX5+		B52	PCIE_RX5+		C52	PEG_RX0+		D52	PEG_TX0+
A53	PCIE_TX5-		B53	PCIE_RX5-		C53	PEG_RX0-		D53	PEG_TX0-
A54	GPI0		B54	GPO1		C54	TYPE0#		D54	PEG_LANE_RV#

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

A55	PCIE_TX4+		B55	PCIE_RX4+		C55	PEG_RX1+		D55	PEG_TX1+
A56	PCIE_TX4-		B56	PCIE_RX4-		C56	PEG_RX1-		D56	PEG_TX1-
A57	GND		B57	GPO2		C57	TYPE1#		D57	TYPE2#
A58	PCIE_TX3+		B58	PCIE_RX3+		C58	PEG_RX2+		D58	PEG_TX2+
A59	PCIE_TX3-		B59	PCIE_RX3-		C59	PEG_RX2-		D59	PEG_TX2-
A60	GND (fixed)		B60	GND (fixed)		C60	GND (fixed)		D60	GND (fixed)
A61	PCIE_TX2+		B61	PCIE_RX2+		C61	PEG_RX3+		D61	PEG_TX3+
A62	PCIE_TX2-		B62	PCIE_RX2-		C62	PEG_RX3-		D62	PEG_TX3-
A63	GPI1		B63	GPO3		C63	GND		D63	GND
A64	PCIE_TX1+		B64	PCIE_RX1+		C64	GND		D64	GND
A65	PCIE_TX1-		B65	PCIE_RX1-		C65	PEG_RX4+		D65	PEG_TX4+
A66	GND		B66	WAKE0#		C66	PEG_RX4-		D66	PEG_TX4-
A67	GPI2		B67	WAKE1#		C67	~~RAPID_SHUTDOWN~~		D67	GND
A68	PCIE_TX0+		B68	PCIE_RX0+		C68	PEG_RX5+		D68	PEG_TX5+
A69	PCIE_TX0-		B69	PCIE_RX0-		C69	PEG_RX5-		D69	PEG_TX5-
A70	GND (fixed)		B70	GND (fixed)		C70	GND (fixed)		D70	GND (fixed)

Row A			Row B			Row C			Row D	
A71	LVDS_A0+ / eDP_TX2+		B71	LVDS_B0+		C71	PEG_RX6+		D71	PEG_TX6+
A72	LVDS_A0- / eDP_TX2-		B72	LVDS_B0-		C72	PEG_RX6-		D72	PEG_TX6-
A73	LVDS_A1+ / eDP_TX1+		B73	LVDS_B1+		C73	GND		D73	GND
A74	LVDS_A1- / eDP_TX1-		B74	LVDS_B1-		C74	PEG_RX7+		D74	PEG_TX7+
A75	LVDS_A2+ / eDP_TX0+		B75	LVDS_B2+		C75	PEG_RX7-		D75	PEG_TX7-
A76	LVDS_A2- / eDP_TX0-		B76	LVDS_B2-		C76	GND		D76	GND
A77	LVDS_VDD_EN / eDP_VDD_EN		B77	LVDS_B3+		C77	GND		D77	GND
A78	LVDS_A3+		B78	LVDS_B3-		C78	PEG_RX8+		D78	PEG_TX8+
A79	LVDS_A3-		B79	LVDS_BKLT_EN		C79	PEG_RX8-		D79	PEG_TX8-
A80	GND (fixed)		B80	GND (fixed)		C80	GND (fixed)		D80	GND (fixed)
A81	LVDS_A_CK+ / eDP_TX3+		B81	LVDS_B_CK+		C81	PEG_RX9+		D81	PEG_TX9+
A82	LVDS_A_CK- / eDP_TX3-		B82	LVDS_B_CK-		C82	PEG_RX9-		D82	PEG_TX9-
A83	LVDS_I2C_CK / eDP_AUX+		B83	LVDS_BKLT_CTRL / eDP_BKLT_CTRL		C83	GND		D83	GND
A84	LVDS_I2C_DAT / eDP_AUX-		B84	VCC_5V_SBY		C84	GND		D84	GND
A85	GPI3		B85	VCC_5V_SBY		C85	PEG_RX10+		D85	PEG_TX10+
A86	GP_SPI_MOSI		B86	VCC_5V_SBY		C86	PEG_RX10-		D86	PEG_TX10-
A87	eDP_HPD		B87	VCC_5V_SBY		C87	GND		D87	GND

Copyright © 2026 ADLINK Technology, Inc.
ADLINK LEADING EDGE AI COMPUTING
LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

A88	PCIE_CK_REF+		B88	BIOS_DIS1#		C88	PEG_RX11+		D88	PEG_TX11+
A89	PCIE_CK_REF-		B89	VGA_RED		C89	PEG_RX11-		D89	PEG_TX11-
A90	GND (fixed)		B90	GND (fixed)		C90	GND (fixed)		D90	GND (fixed)
A91	SPI_POWER		B91	VGA_GRN		C91	PEG_RX12+		D91	PEG_TX12+
A92	SPI_MISO		B92	VGA_BLU		C92	PEG_RX12-		D92	PEG_TX12-
A93	GPO0		B93	VGA_HSYNC		C93	GND		D93	GND
A94	SPI_CLK		B94	VGA_VSYNC		C94	PEG_RX13+		D94	PEG_TX13+
A95	SPI_MOSI		B95	VGA_I2C_CK		C95	PEG_RX13-		D95	PEG_TX13-
A96	~~TPM_PP~~		B96	VGA_I2C_DAT		C96	GND		D96	GND
A97	TYPE10#		B97	SPI_CS#		C97	GND		D97	GND
A98	SER0_TX		B98	GP_SPI_MISO		C98	PEG_RX14+		D98	PEG_TX14+
A99	SER0_RX		B99	GP_SPI_CK		C99	PEG_RX14-		D99	PEG_TX14-
A100	GND (fixed)		B100	GND (fixed)		C100	GND (fixed)		D100	GND (fixed)
A101	SER1_TX		B101	FAN_PWMOUT		C101	PEG_RX15+		D101	PEG_TX15+
A102	SER1_RX		B102	FAN_TACHIN		C102	PEG_RX15-		D102	PEG_TX15-
A103	LID#		B103	SLEEP#		C103	GND		D103	GND
A104	VCC_12V		B104	VCC_12V		C104	VCC_12V		D104	VCC_12V
A105	VCC_12V		B105	VCC_12V		C105	VCC_12V		D105	VCC_12V

Row A			Row B			Row C			Row D	
A106	VCC_12V		B106	VCC_12V		C106	VCC_12V		D106	VCC_12V
A107	VCC_12V		B107	VCC_12V		C107	VCC_12V		D107	VCC_12V
A108	VCC_12V		B108	VCC_12V		C108	VCC_12V		D108	VCC_12V
A109	VCC_12V		B109	VCC_12V		C109	VCC_12V		D109	VCC_12V
A110	GND (fixed)		B110	GND (FIXED)		C110	GND (FIXED)		D110	GND (FIXED)

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.2. Signal Terminology Descriptions

Meaning of the terms used for signal description tables

Term	Description
I	Input to the module
O	Output from the module
I/O	Bi-directional Input / Output
OD	Open drain output from the module
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I/O $3.3V_{SB}$	Input or output 3.3V tolerant active in standby state
DDC	Display Data Channel
PCIE	PCI Express compatible differential signal
PEG	PCI Express Graphics
SATA	Serial ATA specification Revision 2.6 and 3
LVDS	Low Voltage Differential Signal - 330 mV nominal; 450 mV maximum differential signal
P	Power Input / Output
REF	Reference voltage output. May be sourced from a Module power plane.
PDS	Pull-down strap. A Module output pin that is either tied to GND or is not connected. Used to signal Module capabilities to the Carrier Board.
PU	PU (pull-up) resistor on module
PD	PD (pull-down) resistor on module

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.3. AB Connector Signal Descriptions

4.3.1 Audio

Name	Pin #	Description	I/O	PU / PD	Comment
AC_RST# / HDA_RST#	A30	Reset output to CODEC, active low.	O 3.3VSB		
AC_SYNC / HDA_SYNC	A29	Sample-synchronization signal to the CODEC(s).	O 3.3VSB		PCH internal PD 5Kohm
AC_BITCLK / HDA_BITCLK	A32	Serial data clock generated by the external CODEC(s).	I/O 3.3VSB		
AC_SDOUT / HDA_SDOUT	A33	Serial TDM data output to the CODEC.	O 3.3VSB		PCH internal PD 5Kohm
AC_SDIN[2:0] / HDA_SDIN[2:0]	~~B28~~ B29 B30	Serial TDM data inputs from up to 3 CODECs.	I/O 3.3VSB		PCH internal PD 5Kohm

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.3.2 Analog VGA

Name	Pin #	Description	I/O	PU / PD	Comment
VGA_RED	B89	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	
VGA_GRN	B91	Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3V		
VGA_VSYNC	B94	Vertical sync output to VGA monitor	O 3.3V		
VGA_I2C_CK	B95	DDC clock line (I²C port dedicated to identifying VGA monitor capabilities)	I/O OD 3.3V	PU 2k2 3.3V	
VGA_I2C_DAT	B96	DDC data line.	I/O OD 3.3V	PU 2k2 3.3V	

Note: VGA is BOM option support (in place of DDI 3) by project basis

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.3.3 LVDS or eDP

The module default supports a single or dual channel LVDS display panel with up to 24-bit colors. A BOM option that removes the eDP to LVDS bridge IC and outputs the eDP signals directly is available. eDP vs LVDS pin mapping is described below.

Pin #	LVDS mode	eDP mode
A71	LVDS_A0+	eDP_TX2+
A72	LVDS_A0-	eDP_TX2-
A73	LVDS_A1+	eDP_TX1+
A74	LVDS_A1-	eDP_TX1-
A75	LVDS_A2+	eDP_TX0+
A76	LVDS_A2-	eDP_TX0-
A78	LVDS_A3+	-
A79	LVDS_A3-	-
A81	LVDS_A_CK+	eDP_TX3+
A82	LVDS_A_CK-	eDP_TX3-
B71	LVDS_B0+	-
B72	LVDS_B0-	-
B73	LVDS_B1+	-
B74	LVDS_B1-	-
B75	LVDS_B2+	-
B76	LVDS_B2-	-
B77	LVDS_B3+	-
B78	LVDS_B3-	-
B81	LVDS_B_CK+	-
B82	LVDS_B_CK-	-
A77	LVDS_VDD_EN	eDP_VDD_EN
B79	LVDS_BKLT_EN	eDP_BKLT_EN
B83	LVDS_BKLT_CTRL	eDP_BKLT_CTRL
A83	LVDS_I2C_CK	eDP_AUX+
A84	LVDS_I2C_DAT	eDP_AUX-
A87	-	eDP_HPD

Note: LVDS is the default mode and eDP is a BOM option

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.3.3.1. Single/Dual Channel LVDS (default)

Name	Pin #	Description	I/O	PU / PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS Channel A differential clock	O LVDS		
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	B71 B72 B73 B74 B75 B76 B77 B78	LVDS Channel B differential pairs	O LVDS		
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS Channel B differential clock	O LVDS		
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 100K	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V	PD 100K	
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V	PD 100K	
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control.	O 3.3V	PU 2k2 3.3V	
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 2k2 3.3V	

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.3.3.2. 4-lane eDP

Name	Pin #	Description	I/O	PU / PD	Comment
eDP_TX3+ eDP_TX3- eDP_TX2+ eDP_TX2- eDP_TX1+ eDP_TX1- eDP_TX0+ eDP_TX0-	A81 A82 A71 A72 A73 A74 A75 A76	eDP differential pairs	O PCIE		AC coupled off module
eDP_VDD_EN	A77	eDP power enable	O 3.3V	PD 100K	
eDP_BKLT_EN	B79	eDP backlight enable	O 3.3V	PD 100K	
eDP_BKLT_CTRL	B83	eDP backlight brightness control	O 3.3V	PD 100K	
eDP_AUX+	A83	eDP AUX+	I/O PCIE		AC coupled off module
eDP_AUX-	A84	eDP AUX-	I/O PCIE		AC coupled off module
eDP_HPD	A87	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	PD 100K on this pin when eDP is supported

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.3.4 Gigabit Ethernet

Name	Pin #	Description	I/O	PU / PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: **1000 / 100 / 10** MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	I/O Analog		Twisted pair signals for external transformer.
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.	OD 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.	OD 3.3VSB		
GBE0_LINK100# *	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.	OD 3.3VSB		
GBE0_LINK1000# *	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	OD 3.3VSB		
~~GBE0_CTREF~~	~~A14~~	~~Reference voltage for Carrier Board Ethernet channel 1 and 2 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be 250 mA or less.~~	~~REF~~ ~~GND min~~ ~~3.3V max~~		Not supported
GBE0_SDP	A49	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as 1pps signal.	IO 3.3VSB	GBE0_SDP	Depends on the selection of LAN controller. i225-IT support this pin

Note: This product supports up to 2.5GbE. The LAN LED behavior is optimized for maximum 2.5GbE speed.
GBE0_LINK1000# will be active for 2.5GbE speed indication.
GBE0_LINK100# will be active for 1GbE speed indication or lower.
GBE0_ACT# and GBE0_LINK# share the same source from the LAN controller.
For 100Mbit/sec and 10Mbit/sec speed, the LAN LED will be OFF.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.3.5 SATA

Name	Pin #	Description	I/O	PU / PD	Comment
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		AC coupled on Module
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		AC coupled on Module
SATA2_TX+ SATA2_TX-	A22 A23	Serial ATA channel 2, Transmit Output differential pair.	O SATA		Not supported
SATA2_RX+ SATA2_RX-	A25 A26	Serial ATA channel 2, Receive Input differential pair.	I SATA		Not supported
SATA3_TX+ SATA3_TX-	B22 B23	Serial ATA channel 3, Transmit Output differential pair.	O SATA		Not supported
SATA3_RX+ SATA3_RX-	B25 B26	Serial ATA channel 3, Receive Input differential pair.	I SATA		Not supported
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	O 3.3V	PU 10K 3.3V	AC coupled on Module

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.3.6 PCI Express

Name	Pin #	Description	I/O	PU / PD	Comment
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.3.6.1. PCH HSIO Lane Assignments

Name	HSIO name on SOC / Switch IC	Comment
PCIE0	HSIO 3	
PCIE1	HSIO 4	
PCIE2	HSIO 5	
PCIE3	HSIO 6	
PCIE4	HSIO 7	
PCIE5	HSIO 8	
PCIE6	HSIO 9	
PCIE7	HSIO 10	

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.3.7 LPC Bus

Name	Pin #	Description	I/O	PU / PD	Comment
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	B4 B5 B6 B7	LPC multiplexed address, command and data bus	I/O 3.3VSB		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3VSB		
LPC_DRQ0# LPC_DRQ1#	B8 B9	LPC serial DMA request	I 3.3V		Not connected
LPC_SERIRQ	A50	LPC serial interrupt	I/O 3.3VSB	PU 8.2K 3.3VSB	
LPC_CLK	B10	LPC clock output –33MHz nominal	O 3.3VSB		The LPC_CLK frequency is 24MHz on this platform

Note: LPC Bus is supported by an eSPI to LPC bridge IC

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.3.8 USB

Name	Pin #	Description	I/O	PU / PD	Comment
USB0+ USB0-	A46 A45	USB differential data pairs for Port 0	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB1+ USB1-	B46 B45	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB2+ USB2-	A43 A42	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB3+ USB3-	B43 B42	USB differential data pairs for Port 2	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB4+ USB4-	A40 A39	USB differential data pairs for Port 3	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB5+ USB5-	B40 B39	USB differential data pairs for Port 4	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB6+ USB6-	A37 A36	USB differential data pairs for Port 5	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB7+ USB7-	B37 B37	USB differential data pairs for Port 6	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1 (see *Note)	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on carrier
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3 (see *Note)	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on carrier
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5 (see *Note)	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on carrier
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7 (see *Note)	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on carrier
~~USB0_HOST_PRSNT~~	~~B48~~	~~Module USB client may detect the presence of a USB host on USB0. A high value indicates that a host is present.~~	~~I 3.3VSB~~		Not supported

***Note**: A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.3.9 SPI Bus (BIOS only)

Name	Pin #	Description	I/O	PU / PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3VSB	PU 10K 3.3VSB	
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier	O P 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I	PU 10K 3.3VSB	Carrier shall pull to GND or leave not- connected.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I	PU 10K 3.3VSB	Carrier shall pull to GND or leave not- connected

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.3.10 Miscellaneous

Name	Pin #	Description	I/O	PU / PD	Comment
SPKR	B32	Output for audio enunciator, the "speaker" in PC-AT systems	O 3.3V		
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V	PU 100K 3.3V	
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3VSB		
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3VSB	PU 10K 3.3V	
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD 3.3V		There shall be PD on carrier board
FAN_TACHIN	B102	Fan tachometer input for a fan with a two-pulse output.	I OD 3.3V	PU 47K 3.3V	
~~TPM_PP~~	~~A96~~	~~Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.~~	~~I 3.3V~~	~~PD 100K~~	~~PD only when TPM on module. Modules implementing a TPM shall pull down~~

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.3.11 SMBus

Name	Pin #	Description	I/O	PU / PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line. Power sourced through 3.3V standby rail and main power rails.	I/O OD 3.3VSB	PU 8.2K 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line. Power sourced through 3.3V standby rail and main power rails.	I/O OD 3.3VSB	PU 8.2K 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 3.3V standby rail and main power rails.	I 3.3VSB	PU 10K 3.3VSB	

4.3.12 I^2C Bus

Name	Pin #	Description	I/O	PU / PD	Comment
I2C_CK	B33	General purpose I^2C port clock output/input	I/O OD 3.3VSB	PU 2.2K 3.3VSB	Source SEMA BMC as default (chipset by BOM option)
I2C_DAT	B34	General purpose I^2C port data I/O line	I/O OD 3.3VSB	PU 2.2K 3.3VSB	Source SEMA BMC as default (chipset by BOM option)

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.3.13 General Purpose I/O (GPIO)

Name	Pin #	Description	I/O	PU / PD	Comment
GPO[0]	A93	General purpose output pins.	O 3.3V	PD 8.2K	After hardware RESET output low
GPO[1]	B54	General purpose output pins.	O 3.3V	PD 8.2K	After hardware RESET output low
GPO[2]	B57	General purpose output pins.	O 3.3V	PD 8.2K	After hardware RESET output low
GPO[3]	B63	General purpose output pins.	O 3.3V	PD 8.2K	After hardware RESET output low
GPI[0]	A54	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 8.2K 3.3V	
GPI[1]	A63	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 8.2K 3.3V	
GPI[2]	A67	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 8.2K 3.3V	
GPI[3]	A85	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 8.2K 3.3V	

4.3.14 Serial Interface Signals

Name	Pin #	Description	I/O	PU / PD	Comment
SER0_TX	A98	General purpose serial port transmitter	O CMOS 3.3V		Power rail tolerance 5V, 12V There shall be PD on carrier board
SER0_RX	A99	General purpose serial port receiver	I CMOS 3.3V	PU 10K 3.3V	Power rail tolerance 5V, 12V
SER1_TX	A101	General purpose serial port transmitter	O CMOS 3.3V		Power rail tolerance 5V, 12V There shall be PD on carrier board
SER1_RX	A102	General purpose serial port receiver	I CMOS 3.3V	PU 10K 3.3V	Power rail tolerance 5V, 12V

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.3.15 Power and System Management

Name	Pin #	Description	I/O	PU / PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge.	I 3.3VSB	PU 10K 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low request for module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.	I 3.3VSB	PU 10K 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow carrier-based FPGAs or other configurable devices time to be programmed.	I 3.3VSB	PU 10K 3.3VSB	Should have weak pull up.
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as "PS_ON") may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB	PD 100K	
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB	PD 100K	
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB	PD 100K	
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 10K 3.3VSB	
WAKE1#	B67	General purpose wake-up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 10K 3.3VSB	Connect to WAKE 0#
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low or may be used to signal some other external power-management event.	I 3.3VSB	PU 10K 3.3VSB	
LID#	A103	LID button. Low active signal used by the ACPI operating system for a LID switch.	I OD 3.3VSB	PU 47K 3.3VSB	Emulated on GPIO (BIOS)
SLEEP#	B103	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I OD 3.3VSB	PU 47K 3.3VSB	Emulated on GPIO (BIOS)
RAPID_ SHUTDOWN	C67	~~Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for ≥ 20 µs.~~	I CMOS 5VSB		Not supported

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.3.16 Power and Ground

Name	Pin #	Description	I/O	PU / PD	Comment
VCC_12V	A104, A105, A106, A107, A108, A109, B104, B105, B106, B107, B109	Primary power input supports wide range 5— 20V input. All available VCC_12V pins on the connector(s) shall be used.	P		8.5-20 V
VCC_5V_SBY	B84, B85, B86, B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		5Vsb ±5%
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path.	P		

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.4. CD Connector Signal Descriptions

4.4.1 USB 3.0 Extensions

Name	Pin #	Description	I/O	PU / PD	Comment
USB_SSRX0- USB_SSRX0+	C3 C4	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB0	I PCIE		AC coupled off module
USB_SSTX0- USB_SSTX0+	D3 D4	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB0	O PCIE		AC coupled on module
USB_SSRX1- USB_SSRX1+	C6 C7	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB1	I PCIE		AC coupled off module
USB_SSTX1- USB_SSTX1+	D6 D7	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB1	O PCIE		AC coupled on module
USB_SSRX2- USB_SSRX2+	C9 C10	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB2	I PCIE		AC coupled off module
USB_SSTX2- USB_SSTX2+	D9 D10	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB2	O PCIE		AC coupled on module
USB_SSRX3- USB_SSRX3+	C12 C13	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB3	I PCIE		AC coupled off module
USB_SSTX3- USB_SSTX3+	D12 D13	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB3	O PCIE		AC coupled on module

4.4.1.1. USB Root Segmentation

All USB interfaces are derived from the xHCI controller.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.4.2 PCI Express

Name	Pin #	Description	I/O	PU / PD	Comment
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair.	I PCIE		AC coupled off Module

4.4.2.1. PCH HSIO Lane Assignments

Refer to Section 4.3.6.1 PCH HSIO Lane Assignments on page **Error! Bookmark not defined.**.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.4.3 DDI1 Port

Name	Pin #	DisplayPort (DP)	HDMI
DDI1_PAIR0+ DDI1_PAIR0-	D26 D27	DP1_LANE0+ DP1_LANE0-	TMDS1_DATA2+ TMDS1_DATA2-
DDI1_PAIR1+ DDI1_PAIR1-	D29 D30	DP1_LANE1+ DP1_LANE1-	TMDS1_DATA1+ TMDS1_DATA1-
DDI1_PAIR2+ DDI1_PAIR2-	D32 D33	DP1_LANE2+ DP1_LANE2-	TMDS1_DATA0+ TMDS1_DATA0-
DDI1_PAIR3+ DDI1_PAIR3-	D36 D37	DP1_LANE3+ DP1_LANE3-	TMDS1_CLK+ TMDS1_CLK-
DDI1_PAIR4+ DDI1_PAIR4-	C25 C26	-	-
DDI1_PAIR5+ DDI1_PAIR5-	C29 C30	-	-
DDI1_PAIR6+ DDI1_PAIR6-	C15 C16	-	-
DDI1_HPD	C24	DP1_HPD	HDMI1_HPD
DDI1_CTRLCLK_AUX+	D15	DP1_AUX+	HMDI1_CTRLCLK
DDI1_CTRLCLK_AUX-	D16	DP1_AUX-	HMDI1_CTRLDATA
DDI1_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL	DDI1_DDC_AUX_SEL

Note: Dual Mode (HDMI and DisplayPort on the same pins) implementations may be realized. This is desirable for SOCs that natively implement this capability. With such SOCs, the primary Dual Mode implementation challenge is that the HDMI_CTRL_DAT and HDMI_CTRL_CK lines are DC coupled, but the DP_AUX+ /- pair must be AC coupled. A set of FET switches is usually used to sort this out. The FET gates can be controlled by the AUX_SEL pin function.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.4.3.1. DisplayPort (DP) Mode

Name	Pin #	Description	I/O	PU / PD	Comment
DP1_LANE0+ DP1_LANE0- DP1_LANE1+ DP1_LANE1- DP1_LANE2+ DP1_LANE2- DP1_LANE3+ DP1_LANE3-	D26 D27 D29 D30 D32 D33 D36 D37	DP Port 1, differential pair data lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
DP1_HPD	C24	DP Port 1, detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	Module must tolerate high level in stand-by mode. The carrier board shall include a blocking FET on DP1_HPD to prevent back-drive current from damaging the Module.
DP1_AUX+	D15	DP Port 1, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PD 100K	AC coupled on Module
DP1_AUX-	D16	DP Port 1, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PU 100K	AC coupled on Module
DDI1_DDC_AUX_SEL	D34	Strapping Signal to select HDMI or DP output 1M pull-down to logic ground enables HDMI Floating enables DisplayPort mode	I 3.3V	PD 1M	DP mode enabled

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.4.3.2. HDMI Mode

Name	Pin #	Description	I/O	PU / PD	Comment
TMDS1_DATA2+ TMDS1_DATA2- TMDS1_DATA1+ TMDS1_DATA1- TMDS1_DATA0+ TMDS1_DATA0-	D26 D27 D29 D30 D32 D33	HDMI / DVI Port, Differential Pair Data Lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
TMDS1_CLK+ TMDS1_CLK-	D36 D37	HDMI Port, Differential Pair Clock Lines			
HDMI_HPD	C24	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	
HDMI1_CTRLCLK	D15	I2C_CLK Line for HDMI	I/O PCIE	PU 2.2K	AC couple on Module
HDMI1_CTRLDATA	D16	I2C_DAT Line for HDMI	I/O PCIE	PU 2.2K	AC couple on Module
DDI1_DDC_AUX_SEL	D34	Strapping Signal to select HDMI or DP output 1M pull-down to logic ground enables HDMI Leve this signal floating enables DisplayPort mode	I 3.3V	PD 1M	HDMI mode enabled

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.4.4 DDI2 Port

Name	Pin #	DisplayPort (DP)	HDMI
DDI2_PAIR0+ DDI2_PAIR0-	D39 D40	DP2_LANE0+ DP2_LANE0-	TMDS2_DATA2+ TMDS2_DATA2-
DDI2_PAIR1+ DDI2_PAIR1-	D42 D43	DP2_LANE1+ DP2_LANE1-	TMDS2_DATA1+ TMDS2_DATA1-
DDI2_PAIR2+ DDI2_PAIR2-	D46 D47	DP2_LANE2+ DP2_LANE2-	TMDS2_DATA0+ TMDS2_DATA0-
DDI2_PAIR3+ DDI2_PAIR3-	D49 D50	DP2_LANE3+ DP2_LANE3-	TMDS2_CLK+ TMDS2_CLK-
DDI2_HPD	D44	DP2_HPD	HDMI2_HPD
DDI2_CTRLCLK_AUX+	C32	DP2_AUX+	HMDI2_CTRLCLK
DDI2_CTRLCLK_AUX-	C33	DP2_AUX-	HMDI2_CTRLDATA
DDI2_DDC_AUX_SEL	C34	DDI2_DDC_AUX_SEL	DDI2_DDC_AUX_SEL

Note:
Dual Mode (HDMI and DisplayPort on the same pins) implementations may be realized. This is desirable for SOCs that natively implement this capability. With such SOCs, the primary Dual Mode implementation challenge is that the HDMI_CTRL_DAT and HDMI_CTRL_CK lines are DC coupled, but the DP_AUX+ /- pair must be AC coupled. A set of FET switches is usually used to sort this out. The FET gates can be controlled by the AUX_SEL pin function.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.4.4.1. DisplayPort (DP) Mode

Name	Pin #	Description	I/O	PU / PD	Comment
DP2_LANE0+ DP2_LANE0- DP2_LANE1+ DP2_LANE1- DP2_LANE2+ DP2_LANE2- DP2_LANE3+ DP2_LANE3-	D39 D40 D42 D43 D46 D47 D49 D50	DP Port 2, differential pair data lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
DP2_HPD	D44	DP Port 2, detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	Module must tolerate high level in stand-by mode. The carrier board shall include a blocking FET on DP1_HPD to prevent back-drive current from damaging the Module.
DP2_AUX+	C32	DP Port 2, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PD 100K	AC coupled on Module
DP2_AUX-	C33	DP Port 2, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PU 100K	AC coupled on Module
DDI2_DDC_AUX_SEL	C34	Strapping Signal to select HDMI or DP output 1M pull-down to logic ground enables HDMI Floating enables DisplayPort mode	I 3.3V	PD 1M	DP mode enabled

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.4.4.2. HDMI Mode

Name	Pin #	Description	I/O	PU / PD	Comment
TMDS2_DATA2+ TMDS2_DATA2- TMDS2_DATA1+ TMDS2_DATA1- TMDS2_DATA0+ TMDS2DATA0-	D39 D40 D42 D43 D46 D47	HDMI / DVI Port, Differential Pair Data Lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
TMDS2_CLK+ TMDS2_CLK-	D49 D50	HDMI Port, Differential Pair Clock Lines			
HDM2_HPD	D44	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	
HDMI2_CTRLCLK	C32	I2C_CLK Line for HDMI	I/O PCIE	PU 2.2K	AC couple on Module
HDMI2_CTRLDATA	C33	I2C_DAT Line for HDMI	I/O PCIE	PU 2.2K	AC couple on Module
DDI2_DDC_AUX_SEL	C34	Strapping Signal to select HDMI or DP output 1M pull-down to logic ground enables HDMI Leve this signal floating enables DisplayPort mode	I 3.3V	PD 1M	HDMI mode enabled

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.4.5 DDI3 Port

Name	Pin #	DisplayPort (DP)	HDMI
DDI3_PAIR0+ DDI3_PAIR0-	C39 C40	DP3_LANE0+ DP3_LANE0-	TMDS3_DATA2+ TMDS3_DATA2-
DDI3_PAIR1+ DDI3_PAIR1-	C42 C43	DP3_LANE1+ DP3_LANE1-	TMDS3_DATA1+ TMDS3_DATA1-
DDI3_PAIR2+ DDI3_PAIR2-	C46 C47	DP3_LANE2+ DP3_LANE2-	TMDS3_DATA0+ TMDS3_DATA0-
DDI3_PAIR3+ DDI3_PAIR3-	C49 C50	DP3_LANE3+ DP3_LANE3-	TMDS3_CLK+ TMDS3_CLK-
DDI3_HPD	C44	DP3_HPD	HDMI3_HPD
DDI3_CTRLCLK_AUX+	C36	DP3_AUX+	HMDI3_CTRLCLK
DDI3_CTRLCLK_AUX-	C37	DP3_AUX-	HMDI3_CTRLDATA
DDI3_DDC_AUX_SEL	C38	DDI3_DDC_AUX_SEL	DDI3_DDC_AUX_SEL

Note:
Dual Mode (HDMI and DisplayPort on the same pins) implementations may be realized. This is desirable for SOCs that natively implement this capability. With such SOCs, the primary Dual Mode implementation challenge is that the HDMI_CTRL_DAT and HDMI_CTRL_CK lines are DC coupled, but the DP_AUX+ /- pair must be AC coupled. A set of FET switches is usually used to sort this out. The FET gates can be controlled by the AUX_SEL pin function.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.4.5.1. DisplayPort (DP) Mode

Name	Pin #	Description	I/O	PU / PD	Comment
DP3_LANE0+ DP3_LANE0- DP3_LANE1+ DP3_LANE1- DP3_LANE2+ DP3_LANE2- DP3_LANE3+ DP3_LANE3-	C39 C40 C42 C43 C46 C47 C49 C50	DP Port 3, differential pair data lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
DP3_HPD	C44	DP Port 3, detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	Module must tolerate high level in stand-by mode. The carrier board shall include a blocking FET on DP1_HPD to prevent back-drive current from damaging the Module.
DP3_AUX+	C36	DP Port 3, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PD 100K	AC coupled on Module
DP3_AUX-	C37	DP Port 3, Bidirectional Channel used for Link Management and Device Control	I/O PCIE	PU 100K	AC coupled on Module
DDI3_DDC_AUX_SEL	C38	Strapping Signal to select HDMI or DP output 1M pull-down to logic ground enables HDMI Floating enables DisplayPort mode	I 3.3V	PD 1M	DP mode enabled

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.4.5.2. HDMI Mode

Name	Pin #	Description	I/O	PU / PD	Comment
TMDS3_DATA2+ TMDS3_DATA2- TMDS3_DATA1+ TMDS3_DATA1- TMDS3_DATA0+ TMDS3_DATA0-	C39 C40 C42 C43 C46 C47	HDMI / DVI Port, Differential Pair Data Lines	O PCIE		AC coupled off Module 100 nF DC blocking capacitors shall be placed on the Carrier
TMDS3_CLK+ TMDS3_CLK-	C49 C50	HDMI Port, Differential Pair Clock Lines			
HDM3_HPD	C44	Detection of Hot Plug / Unplug and notification of the link layer	I 3.3V	PD 100K	
HDMI3_CTRLCLK	C36	I2C_CLK Line for HDMI	I/O PCIE	PU 2.2K	AC couple on Module
HDMI3_CTRLDATA	C37	I2C_DAT Line for HDMI	I/O PCIE	PU 2.2K	AC couple on Module
DDI3_DDC_AUX_SEL	C38	Strapping Signal to select HDMI or DP output 1M pull-down to logic ground enables HDMI Leve this signal floating enables DisplayPort mode	I 3.3V	PD 1M	HDMI mode enabled

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.4.6 PCIe Graphics Port (PEG)

Name	Pin #	Description	I/O	PU / PD	Comment
PEG_TX0+ PEG_TX0-	D52 D53	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX0+ PEG_RX0-	C52 C53	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX1+ PEG_TX1-	D55 D56	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX1+ PEG_RX1-	C55 C56	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX2+ PEG_TX2-	D58 D59	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX2+ PEG_RX2-	C58 C59	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX3+ PEG_TX3-	D61 D62	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX3+ PEG_RX3-	C61 C62	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX4+ PEG_TX4-	D65 D66	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX4+ PEG_RX4-	C65 C66	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX5+ PEG_TX5-	D68 D69	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX5+ PEG_RX5-	C68 C69	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX6+	D71	PCI Express Graphics transmit differential pairs.	O PCIE		AC coupled on Module

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Name	Pin #	Description	I/O	PU / PD	Comment
PEG_TX6-	D72	These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6			
PEG_RX6+ PEG_RX6-	C71 C72	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX7+ PEG_TX7-	D74 D75	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX7+ PEG_RX7-	C74 C75	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX8+ PEG_TX8-	D78 D79	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX8+ PEG_RX8-	C78 C79	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX9+ PEG_TX9-	D81 D82	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX9+ PEG_RX9-	C81 C82	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX10+ PEG_TX10-	D85 D86	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX10+ PEG_RX10-	C85 C86	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX11+ PEG_TX11-	D88 D89	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX11+ PEG_RX11-	C88 C89	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX12+ PEG_TX12-	D91 D92	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Name	Pin #	Description	I/O	PU / PD	Comment
PEG_RX12+ PEG_RX12-	C91 C92	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX13+ PEG_TX13-	D94 D95	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX13+ PEG_RX13-	C94 C95	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX14+ PEG_TX14-	D98 D99	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX14+ PEG_RX14-	C98 C99	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_TX15+ PEG_TX15-	D101 D102	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	O PCIE		AC coupled on Module
PEG_RX15+ PEG_RX15-	C101 C102	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_TX[16:31]+ and – in Module pin-out Type 6	I PCIE		AC coupled off Module
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the Carrier Board to reverse lane order.	I 3.3V		

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.4.7 Module Type Definition

Name	Pin #	Description	I/O	PU / PD	Comment
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module. The pins are tied on the Module to either ground (GND) or are no-connects (NC). For Pin-out Type 1 and Type 10 that lack a CD connector, these pins are not present (X) **TYPE2# TYPE1# TYPE0#** X X X Pinout Type 1 X X X Pinout Type 10 NC NC NC Pinout Type 2 NC NC GND Pinout Type 3 NC GND NC Pinout Type 4 NC GND GND Pinout Type 5 GND NC NC Pinout Type 6 GND NC GND Pinout Type 7 The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g. deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.			Type 6
TYPE10#	A97	In case of a type 10 module this pin signal is tied to GND through a 47K resistor on the module.			No PD

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.4.8 Power and Ground

Name	Pin #	Description	I/O	PU / PD	Comment
VCC_12V	C104, C105, C106, C107, C108, C109, D104, D105, D106, D107, D108, D109	Primary power input supports wide range 5~ 20V input. All available VCC_12V pins on the connector(s) shall be used.	P		8.5-20 V
GND	C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70, C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path.	P		

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

5. Additional Features

This chapter describes connectors, LEDs, switches and additional items located on the module and not necessarily included in the PICMG standard specification. The locations of these items are shown below:

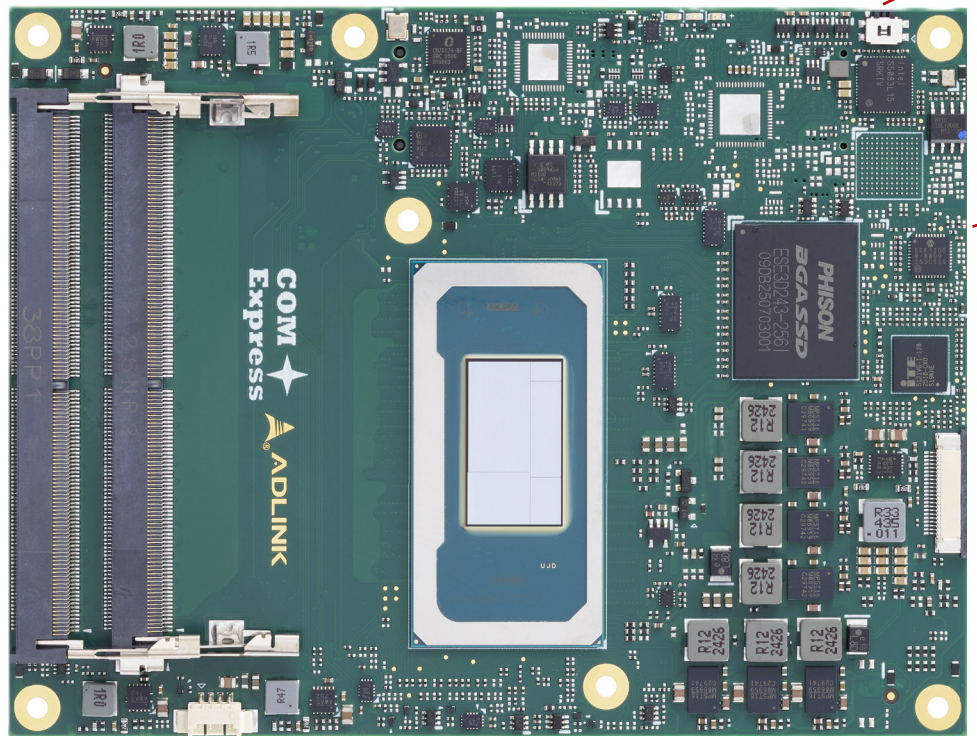


Figure 3 – Module feature locations

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

5.1. Debug Connector

This connector is particular useful during carrier design and bring up phase. It offers access to the following critical parts of the module:

- Test points measurement of internal power rails
- I2C bus for BIOS POST code readout
- SPI BIOS programming interface
- Embedded Controller programming interface

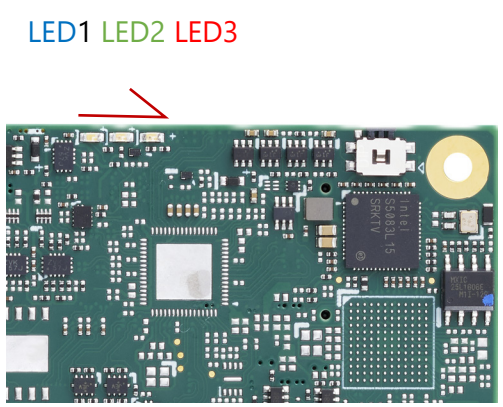
The debug board for Express-PTL usage is DB30-x86

Figure 4 – cExpress-MTL and Debug Module

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

5.2. Status LEDs

Status LED's are mounted on the module to facilitate easier maintenance.



Name	Color	Connection	Function
LED1	Blue	BMC output	Power Sequence Status Code (BMC) Power Changes, RESET (see Exception Codes below)
LED2	Green	Power Source 3Vcc	S0 LED ON S3/S4/S5 LED OFF ECO mode LED OFF

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

LED3	Red	BMC output and same signal as WDT (B27) on BtB connector	Module power up WD LED = LED OFF Watchdog counting WD LED = Keep Last State Watchdog timed out WD LED = LED ON Watchdog RESET WD LED = LED ON Rebooted after WD RESET WD LED = LED ON Rebooted after PWRBTN WD LED = LED OFF Rebooted after RESET BTN WD LED = LED OFF Note: Only a RESET not initiated by the BMC can clear the WD LED (user action)

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

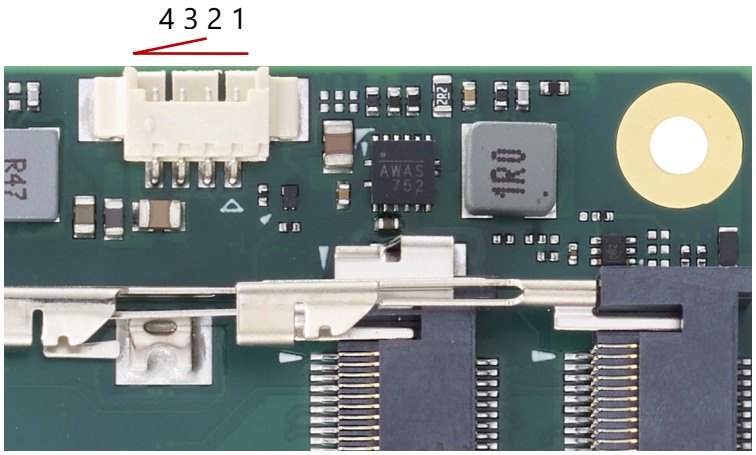
5.3. Exception Codes

Exception Code	Error Message
0	NOERROR
3	NO_SLP_S5
4	NO_SLP_S4
5	NO_SLP_S3
6	BIOS_FAIL
7	RESET_FAIL
9	NO_CB_PWROK
10	CRITICAL_TEMP
11	POWER_FAIL
12	VOLTAGE_FAIL
13	RSMRST_FAIL
14	NO_VDDQ_PG
16	NO_VCORE_PG
17	NO_SYS_GD
19	NO_V3P3A
21	NO_PWRSRC_GD

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

5.4. Fan Connector

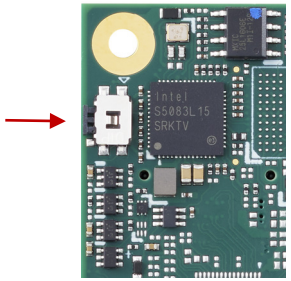
Connector type: JVE 24W1125A-04M00



Name	Description
1	FAN_PWMOUT
2	FAN_TACHIN
3	GND
4	12V

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

5.5. BIOS Default Reset Button



To perform a hardware reset of BIOS default settings, perform the following steps:

1. Shut down the system.
2. Keep the BIOS Setup Defaults Reset Button pressed and boot up the system. You can release the button when the BIOS prompt screen appears
3. The BIOS prompt screen will display a confirmation that BIOS defaults have been reset and request that you reboot the system.



Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

5.6. BIOS Boot Select

The module has two BIOS chips (BOM option) and BIOS operation can be configured to "PICMG" and dual-BIOS "Failsafe" modes using BIOS Select and Mode Configuration Switch, Pin 2.

Setting the module to PICMG mode will configure the BIOS chips on the module as SPI0 and SPI1. In PICMG mode, a BIOS chip cannot be placed in the SPI0 slot on the carrier.

In dual-BIOS Failsafe mode, both BIOS chips on the module are configured as SPI1. Only one of the two is connected to the SPI bus at any given time. In case of failure of the primary SPI1 BIOS, the system will reboot and switch to the secondary SPI1 BIOS on the module. In Failsafe mode, the SPI0 BIOS socket on the carrier can be populated.

In either mode, BIOS Select and Mode Configuration Switch Pin 1 is used to select whether to boot from SPI0 or SPI1.

Mode	Pin 1	Pin 2
Boot from SPI0 (default)	On	-
Boot from SPI1	Off	-
Set BIOS to PICMG mode (default)	-	On
Set BIOS to Failsafe BIOS mode	-	Off

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

6. System Resource

6.1. System Resource Map

Address Range (hex)	Description
3FFFFF00000h-3FFFFF7FFFFh	High Definition Audio Controller
3FFFFC00000h-3FFFFDFFFFFh	High Definition Audio Controller
FED00000h-FED003FFh	High precision event timer
DFFFF000h-DFFFFFFFh	Intel(R) Active Management Technology – SOL(COM)
94300000h-943FFFFFh	Intel(R) Ethernet Controller I226-IT
94400000h-94403FFFh	Intel(R) Ethernet Controller I226-IT
13010000000h-13010FFFFFFh	Intel(R) Graphics
10000000000h-1000FFFFFFFh	Intel(R) Graphics
3FFFFFC0000h-3FFFFFDFFFFh	Intel(R) Innovation Platform Framework Processor Participant
1301455C000h-1301455CFFFh	Intel(R) Management Engine Interface #1
3FFFC000000h-3FFFDFFFFFFh	Intel(R) NPU
3FFFFFEF000h-3FFFFFEFFFFh	Intel(R) NPU
3FFFFFF0000h-3FFFFFFFFFFh	Intel(R) Platform Monitoring Technology (PMT) Driver
4000590000h-400059FFFFh	Intel(R) Serial IO Generic GPIO Host Controller
40005A0000h-40005AFFFFh	Intel(R) Serial IO Generic GPIO Host Controller
40005B0000h-40005BFFFFh	Intel(R) Serial IO Generic GPIO Host Controller
40005C0000h-40005CFFFFh	Intel(R) Serial IO Generic GPIO Host Controller
40005D0000h-40005DFFFFh	Intel(R) Serial IO Generic GPIO Host Controller

Copyright © 2026 ADLINK Technology, Inc.
ADLINK LEADING EDGE AI COMPUTING
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Address Range (hex)	Description
3FFFFFE9000h-3FFFFFE9FFFh	Inter(R) Serial IO I2C Host Controller – E378
3FFFFFEB000h-3FFFFFEBFFFh	Inter(R) Serial IO I2C Host Controller – E379
3FFFFFEC000h-3FFFFFECFFFh	Inter(R) Serial IO I2C Host Controller – E37A
13014559000h-13014559FFFh	Inter(R) Serial IO SPI Host Controller – E327
3FFFFFEE000h-3FFFFFEEFFFh	Intel(R) Serial IO Uart Host Controller – E325
3FFFFFED000h3FFFFFEDFFFh	Inter(R) Silicon Security Engine Interface
13014558000h-130145580FFh	Inter(R) SMBus Controller – E322
FE010000-FE010FFFh	Intel(R) SPI (Flash) Controller – E323
FE001210h-FE001247h	Inter(R) Time-Aware GPIO device - 1023
FE001310h-FE001347h	Inter(R) Time-Aware GPIO device - 1024
13014530000h-1301453FFFFh	Intel(R) USB 3.20 eXtensible Host Controller – 1.20(Microsoft)
13014520000h-1301452FFFFh	Intel(R) USB 3.20 eXtensible Host Controller – 1.20(Microsoft)
FEDC0000h-FEDC7FFFh	Motherboard resources
FA000000h-FD000FFFh	Motherboard resources
00000000h-00000FFFh	Motherboard resources
E0000000h-EFFFFFFFh	Motherboard resources
FED20000h-FED7FFFFh	Motherboard resources
FC800000h-FC81FFFFh	Motherboard resources
FED45000h-FED8FFFFh	Motherboard resources
FEE00000h-FEEFFFFFh	Motherboard resources
5D692000h-5D6A1FFFh	Motherboard resources
80800000h-DFFFFFFFh	PCI Express Root Complex

Copyright © 2026 ADLINK Technology, Inc.
ADLINK LEADING EDGE AI COMPUTING
LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Address Range (hex)	Description
A00000-BFFFFh	PCI Express Root Complex
8C000000h-93FFFFFFh	PCI Express Root Port
94200000-944FFFFFh	PCI Express Root Port
94500000-945FFFFFh	PCI Express Root Port
84000000h-8BFFFFFFh	PCI Express Root Port
94500000h-945FFFFFh	Standard NVM Express Controller
3FFFFA00000h-3FFFFBFFFFh	USB Synopsys Controller
3FFFFFEA000h-3FFFFFEAFFFh	USB Synopsys Controller
13014480000h-130144BFFFFh	USB4(TM) Host Router (Microsoft)
13014562000h-13014562FFFh	USB4(TM) Host Router (Microsoft)
130144C0000h-130144FFFFFh	USB4(TM) Host Router (Microsoft)
13014563000h-13014563FFFh	USB4(TM) Host Router (Microsoft)

6.2. I/O Map

Hex Range	Device
000h-CF7h	PCI Express Root Complex
020h-021h	Programmable Interrupt controller
024h-025h	Programmable Interrupt controller
028h-029h	Programmable Interrupt controller
02Ch-02Dh	Programmable Interrupt controller
030h-031h	Programmable Interrupt controller
034h-035h	Programmable Interrupt controller

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Hex Range	Device
038h-039h	Programmable Interrupt controller
03Ch-03Dh	Programmable Interrupt controller
040h-043h	System timer
050h-053h	System timer
061h-061h	Motherboard resources
062h-062h	Microsoft ACPI-Compliant Embedded Controller
063h-063h	Motherboard resources
065h-065h	Motherboard resources
066h-066h	Microsoft ACPI-Compliant Embedded Controller
067h-067h	Motherboard resources
070h-070h	Motherboard resources
080h-080h	Motherboard resources
092h-092h	Motherboard resources
0A0h-0A1h	Programmable Interrupt controller
0A4h-0A5h	Programmable Interrupt controller
0A8h-0A9h	Programmable Interrupt controller
0ACh-0ADh	Programmable Interrupt controller
0B0h-0B1h	Programmable Interrupt controller
0B2h-0B3h	Motherboard resources
0B4h-0B5h	Programmable Interrupt controller
0B8h-0B9h	Programmable Interrupt controller
0BCh-0BDh	Programmable Interrupt controller

Copyright © 2026 ADLINK Technology, Inc.
ADLINK LEADING EDGE AI COMPUTING
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Hex Range	Device
0F0h-0F0h	Numeric data processor
200h-201h	Motherboard resources
240h-247h	Communications Port (COM3)
248h-24Fh	Communications Port (COM4)
2F8h-2FFh	Communications Port (COM2)
3F8h-3FFh	Communications Port (COM1)
4D0h-4D1h	Programmable Interrupt controller
680h-69Fh	Motherboard resources
A00h-A1Fh	Motherboard resources
A20h-A2FH	Motherboard resources
A30h-A3Fh	Motherboard resources
A40h-A4Fh	Motherboard resources
A50h-A5Fh	Motherboard resources
A60h-A6Fh	Motherboard resources
D00h-FFFFh	PCI Express Root Complex
164Eh-164Fh	Motherboard resources
1854h-1857h	Motherboard resources
2000h-20FEh	Motherboard resources
EFA0h-EFBFh	Intel(R) SMBus Controller – E322
FFF8h-FFFFh	Intel(R) Active Management Technology – SOL(COM)

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

6.3. Interrupt Request (IRQ) Lines

APIC Mode

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
0	System timer	N/A	No
3	Communications Port (COM2)	IRQ3 via SERIRQ	COM2
4	Communications Port (COM1)	IRQ4 via SERIRQ	COM1
5	Communications Port (COM3)	IRQ5 via SERIRQ	COM3
7	Communications Port (COM4)	IRQ7 via SERIRQ	COM4
13	Numeric data processor	N/A	No
14	Intel Serial IO Generic GPIO Host Controller	N/A	No
16	High Definition Audio Controller	N/A	No
16	Intel(R) Serial IO UART Host Controller – E325	N/A	No
17	USB Synopsys Controller	N/A	No
18	Intel(R) Serial IO SPI Host Controller – E327	N/A	No
19	Intel(R) Active Management Technology – SOL (COM)	N/A	No
27	Intel(R) Serial IO I2C Host Controller – E378	N/A	No
28	Intel(R) Serial IO I2C Host Controller – E379	N/A	No
33	Intel(R) Serial IO I2C Host Controller – E37A	N/A	No
055-204	Microsoft ACPI-Compliant System		
256-511	Microsoft ACPI-Compliant System	N/A	No
-64	Intel(R) Innovation Platform Framework Processor Participant	N/A	No
-63	PCI Express Root Port	N/A	No

Copyright © 2026 ADLINK Technology, Inc.
ADLINK LEADING EDGE AI COMPUTING
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
-62	PCI Express Root Port	N/A	No
-61	Intel(R) Silicon Security Engine Interface	N/A	No
-60	Intel(R) NPU	N/A	No
-59	Intel(R) Management Engine Interface #1	N/A	No
-58~-54	Inter(R) Ethernet Controller I226-V	N/A	No
-53	Intel(R) USB 3.20 eXtensible Host Controller – 1.20 (Microsoft)	N/A	No
-52~-21	USB4(TM) Host Router (Microsoft)	N/A	No
-20	Intel(R) USB 3.20 eXtensible Host Controller – 1.20 (Microsoft)	N/A	No
-19	Intel(R) Graphics	N/A	No
-18	Intel(R) Platform Monitoring Technology (PMT) Driver	N/A	No
-17~-5	Standard NVM Express Controller	N/A	No
-4~-2	PCI Express Root Port	N/A	No

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

6.4. PCI Configuration Space Map

Bus Number	Device Number	Function Number	Routing	Description
00h	00h	00h	Internal	Intel Corporation Host Bridge
00h	02h	00h	Internal	Intel Corporation VGA Controller
00h	04h	00h	Internal	Intel Corporation Data Acquisition/Signal Processing Controller
00h	06h	00h	Internal	Intel Corporation PCI To PCI Bridge (PCIE)
00h	06h	01h	Internal	Intel Corporation PCI To PCI Bridge (PCIE)
00h	07h	00h	Internal	Intel Corporation PCI To PCI Bridge (PCIE)
00h	07h	01h	Internal	Intel Corporation PCI To PCI Bridge (PCIE)
00h	0Ah	00h	Internal	Intel Corporation Data Acquisition/Signal Processing Controller(PCIE)
00h	0Bh	00h	Internal	Intel Corporation PCI To PCI Bridge(PCIE)
00h	0Dh	00h	Internal	Intel Corporation XHCI USB Controller
00h	0Dh	02h	Internal	Intel Corporation USB Controller
00h	0Dh	03h	Internal	Intel Corporation USB Controller
00h	14h	00h	Internal	Intel Corporation XHCI USB Controller
00h	14h	01h	Internal	Intel Corporation USB Controller
00h	14h	02h	Internal	Intel Corporation RAM Controller
00h	15h	00h	Internal	Intel Corporation Controller
00h	15h	01h	Internal	Intel Corporation Controller
00h	15h	02h	Internal	Intel Corporation Controller
00h	16h	00h	Internal	Intel Corporation Communication Device
00h	16h	03h	Internal	Intel Corporation Serial Device

Copyright © 2026 ADLINK Technology, Inc.
ADLINK LEADING EDGE AI COMPUTING
LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Bus Number	Device Number	Function Number	Routing	Description
00h	18h	00h	Internal	Intel Corporation Communication Device
00h	1Ch	03h	Internal	Intel Corporation PCI-toPCI Bridge (PCIE)
00h	1Eh	00h	Internal	Intel Corporation Communication Device
00h	1Eh	02h	Internal	Intel Corporation Controller
00h	1Fh	00h	Internal	Intel Corporation ISA Bridge
00h	1Fh	03h	Internal	Intel Corporation HD Audio Device
00h	1Fh	04h	Internal	Intel Corporation SMBus Controller
00h	1Fh	05h	Internal	Intel Corporation Controller
01h	00h	00h	Internal	Mass Storage Controller
02h	00h	00h	Internal	ASMedia Technology AHCI Controller (PCIE)
57h	00h	00h	Internal	Intel Corporation Ethernet Controller (PCIE)

6.5. PCI Interrupt Routing Map

INT Line	PCIE Port1	PCIE Port 5	PCIE Port 6	PCIE Port 7	PCIE Port 8	LPC/eSPI Interface	SMBus Controller	USB 3.0 xHCI Controller
Int0	INTA:16	INTB:16				INTA:16		INTA:16
Int1	INTB:17	INTC:17				INTB:17		INTB:17
Int2	INTC:18	INTD:18				INTC:18	INTC:18	INTC:18
Int3	INTD:19	INTA:17				INTD:19		INTD:19

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

INT Line	TCSS xHCI Controller					
Int0	INTA:16					
Int1						
Int2						
Int3						

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

7. BIOS Settings

7.1. Menu Structure

This section presents the six primary menus of the BIOS Setup Utility. Use the following table as a quick reference for the contents of the BIOS Setup Utility. The subsections in this section describe the submenus and setting options for each menu item. The default setting options are presented in bold, and the function of each setting is described in the right-hand column of the respective table.

Main	Advanced	Chipset	Security	Boot	Save & Exit	MEBx
BIOS Information System Information Board Information System Date System Time	RC ACPI Settings ► Intel(R) Time Coordinated Computing ► CPU Configuration ► Power & Performance ► Graphics Configuration ► SATA Configuration ► Power Management ► PCH-FW Configuration ► System Management ► Thermal Management ► AMI Graphic Output Protocol Policy ► Watchdog Timer ► USB Configuration ► Super IO Configuration ► Serial Port Console Redirection ► Miscellaneous ► Network Stack Configuration ► NVME Configuration ► Trusted Computing ► Asmedia AHCI Controller ► Intel Ethernet Controller ►	System Agent (SA) Configuration ► PCH-IO Configuration ►	Password Description Secure Boot Menu ►	Boot Configuration	Save Options Default Options Boot Override	Mebx Configure(Corporate only)

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

7.2. Main

The Main Menu provides read-only information about your system and also allows you to set the system date and time. Refer to the tables below the screenshot of this menu for details on the submenus and settings.

7.2.1 Bios Information

Feature	Options	Description
BIOS Vender	Info only	American Megatrends
BIOS Version	Info only	Displays Core version
Build Date	Info only	Displays compliancy information
MRC Version	Info only	Displays compliancy information
GOP Driver Version	Info only	Displays Intel Graphic Version
ME FW Version	Info only	Displays Intel CSME Version

7.2.2 System Information

Board Information	Info only	Description
Project Name	Info only	Displays Project Name
CPU Board Version	Info only	Displays CPU Signature
CPU Brand String	Info only	Displays CPU Brand Name
Stepping	Info only	Displays CPU Stepping
CPU Frequency	Info only	Displays CPU Frequency
Total Memory	Info only	Displays installed memory size
Memory Frequency	Info only	Displays memory frequency

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

PCH SKU	Info only	Displays PCH Information.
PMC FW Information	Info only	Display PMC FW Information
Board Information	Submenu	

7.2.3 Board Information

Board Information	Info only	Description
Serial Number	Read only	Displays SMC serial Number
Manufacturing Date	Read only	Displays SMC manufacturing date.
Last Repair Date	Read only	Displays SMC last repair date.
MAC ID	Read only	Displays SMC MAC ID.
UUID	Read only	Display UUID
Runtime Statistics	Info only	
Total Runtime	Read only	The returned value specifies the total time in minutes the system is running in S0 state.
Current Runtime	Read only	The returned value specifies the time in seconds the system is running in S0 state. This counter is cleared when the system is removed from the external power supply.
Power Cycles	Read only	The returned value specifies the number of times the external power supply has been shut down.
Boot Cycles	Read only	The Bootcounter is increased after a HW- or SW-Reset or after a successful power-up.
Boot Reason	Read only	The boot reason is the event which causes the reboot of the system.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

7.2.4 System Data and Time

Feature	Options	Description
System Date	Weekday, MM/DD/YYYY	Requires the alpha-numeric entry of the day of the week, day of the month, calendar month, and all 4 digits of the year, indicating the century and year (Fri XX/XX/20XX)
System Time	HH/MM/SS	Presented as a 24-hour clock setting in hours, minutes, and seconds
Access Level	Info only	

7.3. Advanced

This menu contains the settings for most of the user interfaces in the system.

7.3.1 RC ACPI Settings

Feature	Options	Description
RC ACPI Settings	Info only	
Native ASPM	Auto, Enabled, **Disabled**	Enabled – OS Controlled ASPM, Disabled – BIOS Controlled ASPM

7.3.2 Intel(R) Time Coordinated Computing

Feature	Options	Description
Intel(R) Time Coordinated Computing (Intel(R) TCC)	Info only	
Intel(R) TCC Mode	**Disabled,** Enabled	Enable or Disable Intel(R) TCC Mode. When enabled, this will modify system settings to improve real-time performance. The full list of settings and their current state are displayed below when Intel(R) TCC mode is enabled.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

7.3.3 CPU Configuration

Feature	Options	Description
Efficient-core Information	Submenu	
Performance-core	Submenu	
ID	Info only	Display CPU information.
Brand String	Info only	Display CPU information.
Stepping	Info Only	Display CPU information.
Microcode Revision	Info Only	Display CPU information.
VMX	Info only	Display Intel Virtualization Technology support or not.
SMX/TXT	Info only	Display Intel SMX Technology support or not.
TXT Crash Code	Info only	Display CPU information.
TXT SPAD	Info only	Display CPU information.
Boot Guard Status	Info only	Display CPU information.
Boot Guard ACM Policy Status	Info only	Display CPU information.
Boot Guard SACM Information	Info only	Display CPU information.
CPU Flex Ratio Override	**Disabled**, Enabled	Enable/Disable CPU Flex Ratio Programming.
CPU Flex Ratio Settings	**37**	Set CPU Flex Ratio when CPU Flex Ratio Override Enabled.
Intel (VMX) Virtualization Technology	Disabled, **Enabled**	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.
AVX	**Enabled**, Disabled	Enable/Disable the AVX and AVX2 Instructions

Copyright © 2026 ADLINK Technology, Inc.
ADLINK LEADING EDGE AI COMPUTING
LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Feature	Options	Description
Active Performance-cores	**All,** 3, 2, 1	Number of P-cores to enable in each processor package. Note: P-Cores must be greater than zero as per Reset HAS.
Active Efficient-cores	**All,** 3, 2, 1	Number of E-cores to enable in each processor package. Note: Number of P-cores, E-cores and LP E-cores are looked at together. When all are {0,0,0}, Pcode will enable all cores.
Active LP Efficient-cores	**All,** 3, 2, 1	Number of LP E-cores off ring. Note: Number of P-cores, E-cores and LP E-cores are looked at together. When all are {0,0,0}, Pcode will enable all cores.
BIST	**Disabled**, Enabled	Enable/Disable BIST (Built-In Self Test) on reset
AP threads Idle Manner	HALT Loop, **MWAIT Loop**, RUN Loop	AP threads Idle Manner for waiting signal to run
AES	Disabled, **Enabled**	Enable/Disable AES (Advanced Encryption Standard)
MachineCheck	Disabled, **Enabled**	Enable/Disable Machine Check
MonitorMWait	Disabled, **Enabled**	Enable/Disable MonitorMWait, if Disable MonitorMwait, the AP threads Idle Manner should not set in MWAIT Loop
Intel Trusted Execution Technology	**Disabled**, Enabled	Enables utilization of additional hardware capabilities provided by Intel (R) Trusted Execution Technology. Changes require a full power cycle to take effect.
Alias Check Request	**Disabled**, Enabled	Enables Txt Alias Checking capability\n\nChanges require full Txt capability before it will take effect.\n\n It is a one time only change, next reboot will be reset.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Feature	Options	Description
DPR Memory Size (MB)	**4**	Reserve DPR memory size (0-255) MB
Reset AUX Content	YES, **No**	Reset TPM Aux content. Txt may not functional after AUX content gets reset.
X2APIC Enable	Disabled, **Enabled**	Enable/Disable X2APIC Operating Mode.\nWhen this option is configured as 'Enabled', 'VT-d' option must be 'Enabled'.\nThis option will be grayed out when 'VT-d' option is configured as 'Disabled'.

7.3.3.1. CPU Configuration > Efficient-core Information

Feature	Options	Description
L1 Data Cache	Info only	
L1 Instruction Cache	Info only	
L2 Cache	Info only	Display CPU information.
L3 Cache	Info only	Display CPU information.

7.3.3.2. CPU Configuration > Performance-core Information

Feature	Options	Description
L1 Data Cache	Info only	
L1 Instruction Cache	Info only	
L2 Cache	Info only	Display CPU information.
L3 Cache	Info only	Display CPU information.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

7.3.4 Power & Performance

7.3.4.1. CPU – Power Management Control

Feature	Options	Description
Boot Max Frequency	Disabled **Enabled**	Enable/Disable Boot Maximum Frequency in CPU strap.
Boot Performance Mode	Max Battery, Max Non-Turbo Performance, **Turbo Performance**	Select the performance state that the BIOS will set starting from reset vector.
Intel(R) SpeedStep(tm)	Disabled, **Enabled**	Allows more than two frequency ranges to be supported.
Race To Halt (RTH)	Disabled, **Enabled**	Enable/Disable Race To Halt feature. RTH will dynamically increase CPU frequency in order to enter pkg C-State faster to reduce overall power. (RTH is controlled through MSR 1FC bit 20)
Intel(R) Speed Shift Technology	Disabled, **Enabled**	Enable/Disable Intel(R) Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware-controlled P-states.
Resource Priority Feature	Disabled, **Enabled**	Enable/Disable Resource Priority Feature support.
HwP Autonomous Per Core P State	Disabled, **Enabled**	Disable Autonomous PCPS (Bit 30 = 1, command 0x11) Autonomous will request the same value for all cores all the time. Enable PCPS (default Bit 30 = 0, command 0x11)
HwP Autonomous EPP Grouping	Disabled, **Enabled**	Enable EPP grouping (default Bit 29 =0, command 0x11) Autonomous will request the same values for all cores with same EPP. Disable EPP grouping (Bit 29 =1 , command 0x11) autonomous will not necessarily request same values for all cores with same EPP.
HwP Lock	Disabled, **Enabled**	Enable/Disable HWP Lock support in Misc Power Management MSR.
Turbo Mode	Disabled, **Enabled**	Enable/Disable processor Turbo Mode (requires EMTTM enabled too). AUTO means enabled.
View/Configure Turbo Options	Submenu	

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Feature	Options	Description
Current Turbo Settings		
Max Turbo Power Limit	Info only	
Min Turbo Power Limit	Info only	
Package Base Power Limit	Info only	
Power Limit 1	Info only	
Power Limit 2	Info only	
Energy Efficient P-state	Disabled, **Enabled**	Enable/Disable Energy Efficient P-state feature. When set to 0, will disable access to ENERGY_PERFORMANCE_BIAS MSR and CPUID Function 6 ECX[3] will read 0 indicating no support for Energy Efficient policy setting. When set to 1 will enable access to ENERGY_PERFORMANCE_BIAS MSR 1B0h and CPUID Fun
Package Power Limit MSR Lock	**Disabled**, Enabled	Enable/Disable locking of Package Power Limit settings. When enabled, PACKAGE_POWER_LIMIT MSR will be locked and a reset will be required to unlock the register.
Energy Efficient Turbo	Disabled, **Enabled**	Enable/Disable Energy Efficient Turbo Feature. This feature will opportunistically lower the turbo frequency to increase efficiency. Recommended only to disable in overclocking situations where turbo frequency must remain constant. Otherwise, leave enabled.
Config Base Power Configurations	Submenu	
Config Base Power Configurations		
Enable Configurable Base Power	Applies to non-cTDP, **Applies to cTDP**	Applies TDP initialization settings based on non-cTDP or cTDP. Default is 1: Applies to cTDP; if 0 then applies non-cTDP and BIOS will bypass cTDP initialization flow
Configurable Base Power Boot Mode	**Nominal(Base Power)**, Min Assured Power, Max Assured Power	Assured Power (cTDP) Mode as Nominal/Maximum/Minimum Base Power (TDP) selection.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Feature	Options	Description
Configurable Base Power Lock	Enabled, **Disabled**	Assured Power (cTDP) Mode Lock sets the Lock bits on TURBO_ACTIVATION_RATIO and BASE_POWER_CONTROL.Note: When CTDP (Assured Power) Lock is enabled Custom Config Base Power (cTDP) Count will be forced to 1 and Custom ConfigTDP Boot Index will be forced to 0.
Config Base Power(cTDP) Levels	Info only	
Config Base Power Turbo	Info only	
Activation Ratio	Info only	
Power Limit 1	Info only	
Power Limit 2	Info only	
ConfigTDP Setting		
Config Base Power (cTDP) Nominal	Info only	
Minimum Assured Power	Info only	
Maximum Assured Power	Info only	
Power Limit 1	**0**	Power Limit 1 in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0=no custom override. For 12.5W,enter 12500. Overclocking SKU: Value must be between Max and Min Power Limits. Other SKUs: This value must be between Min Power Limit and Processor Base Power (TDP) Limit.
Power Limit 2	**0**	Power Limit 2 value in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Processor applies control policies such that the package power does not exceed this limit.
Power Limit 1 Time Window*	**0**	Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0 = default value (28 sec for Mobile and 8 sec for Desktop). Defines time window which TDP value should be maintained.
Config Base Power Turbo Activation Ratio	0	Custom value for Turbo Activation Ratio. Needs to be configured with valid values from LFM to Max Turbo. 0 means don't use custom value.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Feature	Options	Description
CPU VR Settings	Submenu	
CPU VR Settings		
PSYS Slope	0	PSYS Slope defined in 1/100 increments. Range is 0-200. For a 1.25 slope, enter 125. 0 = AUTO.
ThETA Ibatt Feature	**Disabled**, Enabled	

7.3.5 Graphics Configuration

Feature	Options	Description
Data format and Color Depth	VESA 24 bpp JEIDA 24 bpp **JEIDA/vesa 18 bpp**	Data format and Color Depth select
LVDS Output Mode	Dual LVDS bus **Single LVDS bus**	Single/Dual mode select
DE Polarity	**Active High** Active Low	DE Polarity select
Vsync Polarity	**Active High** Active Low	Vsync Polaity select
Hsync Polarity	**Active High** Active Low	Hsync Polarity select
Spreading depth	**No Spreading** 0.5% 1.0% 1.5% 2.0%	Clock frequency center spreading depth.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

	2.5%	
Integrated Display Configuration	Info only	
eDP/LVDS	**Disabled** Enabled	Enable/Disable eDP/LVDS
LFP Panel Type	**VBIOS Default** 640x480 800x600 1024x768 1280x1024 1400x1050 LVDS1 1400x1050 LVDS2 1600x1200 1366x768 1680x1050 1920x1200 1440x900 1600x900 1024x768 1280x800 1920x1080 2048x1536	Select LFP panel used by Internal Graphics Device by selecting the appropriate setup item.
LVDS Backlight Mode	EC Mode **GTT Mode**	Select LVDS Backlight control function.
LVDS Backlight	Submenu(EC Mode)	
LVDS Backlight Brightness	Value Range (0-255)	A change takes effect immediately. The value range starts by 0 and ends of 255.
DDI port 1	No Device Display Port HDMI **DisplayPort with HDMI/DVI Compatibility**	DDI port 1 function choose to DisplayPort or HDMI

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

DDI port 2	No Device Display Port HDMI **DisplayPort with HDMI/DVI Compatibility**	DDI port 2 function choose to DisplayPort or HDMI
DDI port 3	No Device Display Port HDMI **DisplayPort with HDMI/DVI Compatibility**	DDI port 3 function choose to DisplayPort or HDMI

7.3.6 SATA Configuration

Feature	Options	Description
ASMedia SATA Configuration		
SATA Controller Speed	Gen1 Gen2 **Gen3**	Indicates the maximum speed the SATA controller can support.
Port 1 Hot Plug	Disabled, **Enabled**	ASMedia SATA Port 1 Hot Plug Enable/Disable
SATA Controller Speed	Gen1 Gen2 **Gen3**	Indicates the maximum speed the SATA controller can support.
Port 2 Hot Plug	Disabled, **Enabled**	ASMedia SATA Port 2 Hot Plug Enable/Disable
SATA Controller Speed	Gen1 Gen2 **Gen3**	Indicates the maximum speed the SATA controller can support.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Port 3 Hot Plug	Disabled, **Enabled**	ASMedia SATA Port 3 Hot Plug Enable/Disable
SATA Controller Speed	Gen1 Gen2 **Gen3**	Indicates the maximum speed the SATA controller can support.
Port 4 Hot Plug	Disabled, **Enabled**	ASMedia SATA Port 4 Hot Plug Enable/Disable

7.3.7 Power Management

Feature	Options	Description
Power Management		
ACPI Settings	Submenu	
Enable ACPI Auto Configuration	**Disabled**, Enabled	Enables or Disables BIOS ACPI Auto Configuration.
Enable Hibernation	Disabled, **Enabled**	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may not be effective with some operating systems.
ACPI Sleep State*	Suspend Disabled, **S3 (Suspend to RAM)**	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
LID Function	**Disabled**, Enabled	Enable/Disable LID Function
Sleep Function	Disabled, **Enabled**	Enable/Disable Sleep Button Function
ECO Mode*	**Disabled**, Enabled	Reduces the power consumption of the system, but after a shut down, you have to wait at least 5 seconds before you can restart the system.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Power-Up Mode*	**Turn On,** Remain Off, Last State	Turn On:
ATTENTION: The Power-Up Mode only has effect when the module is in ATX-Mode.		
Power Consumption	Submenu	
Power Consumption		
Main Current	Read only	Displays input current.
Current Input Power	Read only	Displays input power.
RTC	Read only	Displays the sensed voltage based on hardware design.
5VSB	Read only	Displays the sensed voltage based on hardware design
VIN	Read only	Displays the sensed voltage based on hardware design
3.3V	Read only	Displays the sensed voltage based on hardware design
VMEM	Read only	Displays the sensed voltage based on hardware design
3.3VSB	Read only	Displays the sensed voltage based on hardware design
VCORE	Read only	Displays the sensed voltage based on hardware design

7.3.8 System Management

Feature	Options	Description
System Management		
SEMA Firmware Version	Info only	
SEMA BIOS Specification	Info only	
SEMA Flags	Submenu	
SEMA Features	Info only	

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Feature	Options	Description
Bios Select	Info only	
ATX/AT-Mode	Info only	
SEMA Features:		
Uptime & Power Cycles Counter	Read only	
System Restart Event	Read only	
4096 Bytes User-Flash	Read only	
Runtime Watchdog	Read only	
Temperatures	Read only	
Voltage Monitor	Read only	
Display Backlight Control	Read only	
Power-up Watchdog	Read only	
Power Monitor (Current Sense)	Read only	
Boot Counter	Read only	
Dual-BIOS	Read only	
I2C Bus 1	Read only	
I2C Bus 2	Read only	
I2C Bus 4	Read only	
CPU Fan	Read only	
AT/ATX Mode	Read only	
ACPI Thermal Trigger	Read only	
Power-up to Last State	Read only	
Backlight Restore	Read only	

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Feature	Options	Description
Ext - GPIO	Read only	
Other BMC	Read only	
Error Log	Read only	
Wake-by-BMC	Read only	
Soft Fan	Read only	
Parameter Memory	Read only	
Ext-GPIO Input Interrupt Support	Read only	
Ext-GPIO 8 Pins	Read only	
Switch BIOS immediately Support	Read only	

7.3.9 Thermal Management

Feature	Options	Description
Thermal Management		
Critical Trip Point	**Disabled** 80 C 90 C 95 C	The value is the temperature threshold of the Critical Trip Point.
Passive Cooling Trip Point	**Disabled** 70C 80C 90C	The value is the temperature threshold of the Passive Cooling Trip Point.
Active Cooling Trip Point	40 C 50 C 60 C 70 C **Refer to BMC**	This value is the temperature threshold of the active cooling trip point.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Feature	Options	Description
Watchdog ACPI Event Shutdown	**Disabled** Enabled	Watchdog ACPI Event Shutdown Enabled/Disabled
Temperature and Fan Speed	Submenu	
Temperature and Fan Speed		
CPU Temperature	Info Only	
Current	Info Only	Display Current CPU Temperature
Startup	Info Only	Display Startup CPU Temperature
Min	Info Only	Display Min CPU Temperature
Max	Info Only	Display Max CPU Temperature
Board Temperature	Info Only	
Current	Info Only	Display Current Board Temperature
Startup	Info Only	Display Startup Board Temperature
Min	Info Only	Display Min Board Temperature
Max	Info Only	Display Max Board Temperature
CPU Fan Speed	Info Only	
Smart Fan	Submenu	
Smart Fan		
CPU Smart FanTemperature Source	**CPU Sensor** Board Sensor	CPU Smart FanTemperature Source
CPU Fan Mode	**AUTO**, Off, On, Soft	Select CPU Fan control mode.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Feature	Options	Description
Trigger Point 1	Info-only	
Trigger Temperature	40	Set the temperature value for trigger point 1 to control CPU fan.
PWM Level	30	When configured sensor reaches the trigger temperature value, set PWM level for this condition.
Trigger Point 2	Info-only	
Trigger Temperature	50	Set the temperature value for trigger point 2 to control CPU fan.
PWM Level	40	When configured sensor reaches the trigger temperature value, set PWM level for this condition.
Trigger Point 3	Info-only	
Trigger Temperature	60	Set the temperature value for trigger point 3 to control CPU fan.
PWM Level	63	When configured sensor reaches the trigger temperature value, set PWM level for this condition.
Trigger Point 4	Info-only	
Trigger Temperature	70	Set the temperature value for trigger point 4 to control CPU fan.
PWM Level	100	When configured sensor reaches the trigger temperature value, set PWM level for this condition.

Copyright © 2026 ADLINK Technology, Inc.
ADLINK LEADING EDGE AI COMPUTING
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

7.3.10 AMI Graphic Output Protocol Policy

Feature	Options	Description
Intel(R) Graphics Controller		
Intel(R) GOP Driver [26.0.xx]		
Output Select	HDMI	Auto detect Output Interface
Output Select*	HDMI/DP/eDP	Manual select Output Interface
Brightness Setting	[Max-Value, Min-Value, Step-Value, Step-Value] = [0xFFFFFFFF, 0x00000000, 0x00000001, Brightness Setting]	Item shown when eDP detected Set Gop Brightness value
BIST Enable	**Disabled**, Enabled	Item shown when eDP detected Starts or stops the BIST on the integrated display panel.

7.3.11 Watchdog Timer

Feature	Options	Description
Watchdog Timer		
Power-Up watchdog	**Disabled** Enabled	The Power Up Watchdog resets the system after a certain amount of time after power up. Press F12 during start up to disable the Power Up Watchdog.
ATTENTION: Pressing F12 during start up disables the Power Up Watchdog.	Info only	
RunTime Watchdog	**Disabled** Enabled	The RunTime Watchdog resets the system after a certain amount of time after power up.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

7.3.12 USB Configuration

Feature	Options	Description
USB Configuration		
USB Module Version	Info Only	Display USB Module Version
USB Controllers:	Info Only	Display USB Controllers is XHCI or EHCI.
USB Devices:	Info Only	Display attachment USB devices.
XHCI Hand-off	**Enabled** Disabled	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	Disabled **Enabled**	Enable / Disable USB Mass Storge Driver Support.
USB hardware delays and time-outs:		
USB transfer rime-out	1 sec 5sec 10sec **20 sec**	The time-out value for Control, Bulk, and Interrupt transfers.
Device reset time-out	10 sec **20 sec** 30 sec 40 sec	USB mass storage device Start Unit command time-out.
Device power-up delay	**Auto** Manual	Maximum time the device will take before it properly reports itself to the Hot Controller. 'Auto' uses default value: for a Root po\rt it is 100ms, for a Hub port the delay is taken form Hub descriptor.
Mass Storage Device:	Info only	

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

7.3.13 Super IO Configuration

Feature	Options	Description
Super IO Configuration	Info only	
ITE5121 Super IO Configuration	submenu	
Nct6126dSec Super IO Configuration	submenu	

7.3.13.1. Super IO Configuration > IT5121E Super IO Configuration

Feature	Options	Description
IT5121E Super IO Configuration	Info only	
Super IO Chip	Info only	
Serial Port 1 Configuration	submenu	
Serial Port 2 Configuration	submenu	

7.3.13.1.1. Super IO Configuration > IT5121E Super IO Configuration > Serial Port 1 Configuration

Feature	Options	Description
Serial Port 1 Configuration	Info only	
Serial Port 1 Configuration	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	IO=3F8h; IRQ=4	Fixed configuration of serial port.
Change Settings	**Auto** IO=3F8h; IRQ=4 IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2F8h;	Select an optimal setting for Super IO device.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Feature	Options	Description
	IRQ=3,4,5,6,7,9,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12	
Change Settings	**Normal** High Speed	Select an optimal setting for Super IO Device.

7.3.13.1.2. Super IO Configuration > IT5121E Super IO Configuration > Serial Port 2 Configuration

Feature	Options	Description
Serial Port 2 Configuration	Info only	
Serial Port 2 Configuration	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	IO=2F8h; IRQ=3	Fixed configuration of serial port.
Change Settings	**Auto** IO=2F8h; IRQ=3 IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12	Select an optimal setting for Super IO device.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

7.3.13.2. Super IO Configuration > Nct6126dSec Super IO Configuration

Feature	Options	Description
Nct6126dSec Super IO Configuration	Info only	
Super IO Chip	Info only	
Serial Port 1 Configuration	submenu	
Serial Port 2 Configuration	submenu	

7.3.13.2.1. Super IO Configuration > Nct6126dSec Super IO Configuration > Serial Port 1 Configuration

Feature	Options	Description
Serial Port 1 Configuration	Info only	
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	IO=240h; IRQ=5	Fixed configuration of serial port.
Change Settings	**Auto** IO=240h; IRQ=10 IO=240h; IRQ=3,4,5,6,7,10,11,12 IO=248h; IRQ=3,4,5,6,7,10,11,12 IO=250h; IRQ=3,4,5,6,7,10,11,12 IO=258h; IRQ=3,4,5,6,7,10,11,12 IO=260h; IRQ=3,4,5,6,7,10,11,12 IO=268h;	Select an optimal setting for Super IO device.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Feature	Options	Description
	IRQ=3,4,5,6,7,10,11,12	
UART Mode	**RS232** RS485 RS422	Change UART mode.
Feature	**Options**	**Description**
Serial Port 1 Configuration	Info only	
Serial Port 1 Configuration	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	IO=3F8h; IRQ=4	Fixed configuration of serial port.
Change Settings	**Auto** IO=3F8h; IRQ=4 IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12	Select an optimal setting for Super IO device.
Change Settings	**Normal** High Speed	Select an optimal setting for Super IO Device.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

7.3.13.2.2. Super IO Configuration > Nct6126dSec Super IO Configuration > Serial Port 2 Configuration

Feature	Options	Description
Serial Port 2 Configuration	Info only	
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	IO=248h; IRQ=7	Fixed configuration of serial port.
Change Settings	**Auto** IO=248h; IRQ=10 IO=240h; IRQ=3,4,5,6,7,10,11,12 IO=248h; IRQ=3,4,5,6,7,10,11,12 IO=250h; IRQ=3,4,5,6,7,10,11,12 IO=258h; IRQ=3,4,5,6,7,10,11,12 IO=260h; IRQ=3,4,5,6,7,10,11,12 IO=268h; IRQ=3,4,5,6,7,10,11,12	Select an optimal setting for Super IO device.
UART Mode	**RS232** RS485 RS422	Change UART mode.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

7.3.14 Serial Port Console Redirection

Feature	Options	Description
COM0/1/2/3	Info Only	
Console Redirection	**Disabled,** Enabled	To enable or disable console redirection of COMx.
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.
Serial Port for Out-of-Band Management/Windows Emergency Management Service (EMS)	Info only	
Console Redirection EMS	**Disabled**, Enabled	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	
Out-of-Band Mgmt Port	**COM0**, COM1, COM2, COM3	Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.
Terminal Type EMS	VT100, VT100Plus, **VT-UTF8**, ANSI	VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation.
Bits per seconds EMS	9600, 19200, 57600, **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Flow Control EMS	**None**, Hardware RTS/CTS, Software Xon/Xoff	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
Data Bits EMS	Info only	
Parity EMS	Info only	

Copyright © 2026 ADLINK Technology, Inc.
ADLINK LEADING EDGE AI COMPUTING
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Stop Bits EMS	Info only	

7.3.14.1.Serial Port Console Redirection > Console Redirection Settings

Feature	Options	Description
COM0/1/2/3	Info only	
Console Redirection Settings	Info only	
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7 **8**	Data Bits.
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection..
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

7.3.15 Miscellaneous

Feature	Options	Description
Miscellaneous	Info only	
I2C Speed Control	**100 Kbps** 400 Kbps	I2C Speed Control
SMBUS Select Configuration	From EC **FrOM PCH**	SMBUS select configuration from PCH or EC.
WOL From S5	OFF **ON**	This Config to control power on/off LAN in S5 State by SEMA(EC)
Smart Battery Function	**Disabled** Enabled Auto	Enable/Disable Smart Battery function. Auto: disable Smart Battery function if charger IC not be detected.

7.3.16 Network Stack Configuration

Feature	Options	Description
Network Stack	**Disabled** Enabled	Enable/Disable UEFI network stack.

7.3.17 NVMe Configuration

Feature	Options	Description
Seg:Bus:Dev:Func	Info only	
Model Number	Info only	
Total Size	Info only	

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Feature	Options	Description
Vendor ID	Info only	
Device ID	Info only	
Namespace	Info only	
Self Test Option	**Short** Extended	Select either Short or Extended Self Test. Short option will take couple of minutes and extended option will take several minutes to complete.
Self Test Action	**Controller Only Test** Controller and NameSpace Test	Select either to test Controller alone or Controller and NameSpace. Selecting Controller and Namespace option will take lot longer to complete the test.
Run Device Self Test		Perform device self test for the corresponding Option and Action selected by user. Pressing the 'Esc' key will abort the test. Result shown below is the recent result logged in the device.

7.3.18 Trusted Computing

Feature	Options	Description
Security Device Support	**Disabled**, Enabled	Enables or Disables BIOS support for security device.When its disabled, O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.
PH Randomization	Disabled, **Enabled**	Enables or Disables Platform Hierarchy randomization. DO NOT ENABLE THIS QUESTION IN PRODUCTION PLATFORMS. THIS IS FOR DEVELOPMENT TESTING. OVERRIDE ChangePlatformAuth ELINK for production platforms supporting TXT.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

7.4. Chipset

Feature	Options	Description
System Agent (SA) Configuration	submenu	
PCH-IO Configuration	submenu	

7.4.1 Chipset > System Agent (SA) Configuration

Feature	Options	Description
Memory Configuration	submenu	Memory Configuration Parameters
Graphics Configuration	submenu	Graphics Configuration
VMD setup menu	submenu	VMD Configuration settings
VT-d setup menu	submenu	VT-d Configuration settings
CRID Support	Enabled**, Disabled**	Enable/Disable SA CRID and TCSS CRID control for Intel SIPP
IPU Device (B0:D5:F0)	**Enabled,** Disabled	Enable/Disable SA IPU Device \nThis option will be grayed out when IPU is fused off from silicon.
NPU Device (B0:D11:F0)	Enabled**, Disabled**	Enable/Disable NPU (Neural Processing Unit) Device.
MIPI Camera Configuration	Submenu	

7.4.1.1. Chipset > System Agent (SA) Configuration > Memory Configuration

Feature	Options	Description
Memory RC Version	**Info-only**	
Memory Frequency	**Info-only**	
Memory Timings (tCL-tRCD-tRP-tRAS)	**Info-only**	
Controller x Channel x Slot x	**Info-only**	
Size	**Info-only**	
Number of Ranks	**Info-only**	

Copyright © 2026 ADLINK Technology, Inc.
ADLINK LEADING EDGE AI COMPUTING
LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Manufacturer	**Info-only**	
Maximum Memory Frequency	**Auto** 1067 1333 1600 1867 2133 2400 2667 2933 3200 3467 3600 3733 4000 4200 4267 4400 4600 4800 5000 5200 5400 5600 6000 6400 6800 7200 7467 8000 8533 9600 10667	Maximum Memory Frequency Selections in Mhz.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Max TOLUD	**Dynamic** 1 GB 1.25 GB 1.5 GB 1.75 GB 2 GB	Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller
SAGV	Enabled**,** **Disabled**	System Agent Geyserville. Disabled or Enabled.
Gear Ratio	**Auto**, Gear2, Gear4	Gear ratio when SAGV is disabled.
In-Band ECC Support	**Disabled**, Enabled	Enable/Disable In-Band ECC. Will be enabled if memory hav symmetric configuration.

7.4.1.2. Chipset > System Agent (SA) Configuration > Graphics Configuration

Feature	Options	Description
Display Configuration	Info only	
Media Configuration	Info only	
GT Configuration	Info only	
Display Configuration	Submenu	
Intel Graphics Pei Display Peim	Enabled, **Disabled**	Enable/Disable Pei (Early) Display
Intel Graphics PreMem SOL	Disabled, Text Mode, **Graphics Mode**, eSOL Text Mode, eSOL Graphics Mode	Choose PreMem SOL Mode
VDD Enable	Disabled, **Enabled**	Enable/Disable forcing of VDD in the BIOS

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

GOP Config Driver Enable	**Enabled**, Disabled	Enable/Disable GOP Config Driver
GT Configuration	Submenu	
Configure GT for use		Enable/Disable GT configuration in BIOS.
GT RC1p Support	Enabled**,** **Disabled**	Enable/Disable RC1p support. If GT RC1p is enabled, send a RC1p frequency request to PMA if other conditions being met
RC6(Render Standby)	Disabled**,** **Enabled**	Check to enable render standby support
Reduce XeCores	**Enabled,** Disabled	Enable/Disable Reduce XeCores
Media Configuration	Submenu	
Configure Media for use	**Enabled**, Disabled	Enable/Disable Media configuration in BIOS
Media RC1p Support	Enabled, **Disabled**	Enable/Disable RC1p support. If Media RC1p is enabled, send a RC1p frequency request to PMA if other conditions being met
MC6(Media Standby)	Disabled, **Enabled**	Check to enable Media standby support
Primary Display	**Auto**, IGPU, HG	Select AUTO set IGD to be Primary Display if no external Graphics Device connected otherwise external Graphics Device detected on first PCIe port will be Primary Display or Select IGPU for IGD to be Primary Display Or Select HG for Hybrid Gfx.
Skip Scanning of External Gfx Card	**Disabled**, Enabled	If Enable, it will not scan for External Gfx Card on PCIE Ports
Internal Graphics	**Auto**, Disabled, Enabled	Keep IGPU enabled based on the setup options
PAVP Enable	**Enabled**, Disabled	Enable/Disable PAVP

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

DVMT Pre-Allocated	0M, 32M, 64M, 96M, **128M**, 4M, 8M, 12M, 16M, 20M, 24M, 28M, 32M/F7, 36M, 40M, 44M, 48M, 52M, 56M, 60M	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.
Memory Bandwidth Compression	**Enabled**, Disabled	Enable/Disable Memory Bandwidth Compression.\n Enabling reserves small fraction of RAM to enable GPU memory bandwidth compression.\n Disabling Memory Bandwidth Compression can reduce supported feature set, performance and power efficiency

7.4.1.3. Chipset > System Agent (SA) Configuration > VMD setup menu

Feature	Options	Description
Enable VMD controller	**Disabled**, Enabled	Enable/Disable to VMD controller

7.4.1.4. Chipset > System Agent (SA) Configuration > VT-d setup menu

Feature	Options	Description
Pre-boot DMA Protection	**Disabled**, Enabled	Enable DMA Protection in Pre-boot environment (If DMAR table is installed in DXE and If VTD_INFO_PPI is installed in PEI.)
Nested Support	**Default**, Disabled	Defeature Nested Capability
Posted Interrupt Support	**Default**, Disabled	Defeature Posted Interrupt Capability
DMA Control Guarantee	Disabled, **Enabled**	Enable/Disable DMA_CONTROL_GUARANTEE bit
TBT Performance Boost	**Enabled**, Disabled	Enable/Disable TBT Performance Boost through PCode mailbox

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

7.4.1.5. Chipset > System Agent (SA) Configuration > MIPI Camera Configuration

Feature	Options	Description
CVS (Computer Vision Sensing) Support	**Disabled**, Enabled	Disable/Enable CVS
Control Logic 1	**Disabled**, Enabled	Control Logic 1
Control Logic 2	**Disabled**, Enabled	Control Logic 2
Control Logic 3	**Disabled**, Enabled	Control Logic 3
Control Logic 4	**Disabled**, Enabled	Control Logic 4
Camera1	**Disabled**, Enabled	Camera1
Camera2	**Disabled**, Enabled	Camera2
Camera3	**Disabled**, Enabled	Camera3
Camera4	**Disabled**, Enabled	Camera4

7.4.2 Chipset > PCH-IO Configuration

Feature	Options	Description
PCIE Configuration	Submenu	
USB Configuration	Submenu	
Security Configuration	Submenu	
HD Audio Configuration	Submenu	
SerialIO Configuration	Submenu	

Copyright © 2026 ADLINK Technology, Inc.
ADLINK LEADING EDGE AI COMPUTING
LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

PCH LAN Controller	Info only	
Port 80 Redirection	LPC Bus, PCIE Bus	Control where the Port 80h cycles are sent.
Enhance Port 80h LPC Decoding	**Disabled**, Enabled	Support the word/dword decoding of port 80h behind LPC
Enable TCO Timer	**Disabled**, Enabled	Enable/Disable TCO timer. When disabled, it disables PCH ACPI timer, stops TCO timer, and ACPI WDAT table will not be published.
SPD Write Disable	**TRUE**, FALSE	Enable/Disable setting SPD Write Disable. For security recommendations, SPD write disable bit must be set.

7.4.2.1. Chipset > PCH-IO Configuration > PCIE Configuration

Feature	Options	Description
Port8xh Decode	**Disabled**, Enabled	PCI Express Port8xh Decode Enable/Disable.
Compliance Test Mode	**Disabled**, Enabled	Enable when using Compliance Load Board
PCIe AER _OSC Setting	**Enabled,** Disabled	
PCIE Ports 0-3 Configuration	4x1 Port, 1x2 2x1 Port, 1x2 2x1 Port Reversed, 2x2 Port, 2x2 Port Reversed, **1x4 Port**, 1x4 Port Reversed	Please make sure the system boots completed after changing the configuration. Do not attempt to Shut Down Your Computer, doing that may lead to system malfunction.
PCIE Ports 4-7 Configuration	**4x1** Port, 1x2 2x1 Port, 1x2 2x1 Port Reversed, 2x2 Port, 2x2 Port Reversed, 1x4 Port, 1x4 Port Reversed	Please make sure the system boots completed after changing the configuration. Do Not Attempt to Shut Down Your Computer, doing that may lead to system malfunction.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

PEG Ports [0:7] Configuration	2x4 Port, 1x4LR,1x4LR Port, 1x4,1x4LR Port, 1x8 Port, **1x8LR Port**	Please make sure the system boots completed after changing the configuration. Do Not Attempt to Shut Down Your Computer, doing that may lead to system malfunction.
PEG Ports [8:11] Configuration	**2x2 Port**, 2x2LR Port, 1x4 Port, 1x4LR Port	Please make sure the system boots completed after changing the configuration. Do Not Attempt to Shut Down Your Computer, doing that may lead to system malfunction.
PCI Express Root Port PXPA1(PCIe 0)/PXPA2(PCIe 1)/PXPA3(PCIe 2)/PXPA4(PCIe 3)/ PXPB1(PCIe 4)/PXPB2(PCIe 5)/PXPB3(PCIe 6)/PXPB4(PCIe 7 for i226)/ PXPC1(PEG[8:11])/PXPC2(PEG[8:11]) PXPD(PEG[0:7])/PXPE(PEG[0:7]) for H484 only	Submenu	Control the PCI Express Root Port.
PCIE clocks	Submenu	

7.4.2.1.1. Chipset > PCH-IO Configuration > PCIE Configuration > PCI Express Root Port PXPA1/ PXPA2/ PXPA3/ PXPA4/ PXPB1/ PXPB2/ PXPB3/ PXPB4/ PXPC1/ PXPC2/ PXPD/PXPE

/Feature	Options	Description
PCI Express Root Port PXPxx	Disabled, **Enabled**	Control the PCI Express Root Port.
Connection Type	Built-in, **Slot**	Built-In: a built-in device is connected to this rootport. SlotImplemented bit will be clear. Slot: this rootport connects to user-accessible slot. SlotImplemented bit will be set.
ASPM	Disabled, L0s, L1, L0sL1, **Auto**	Set the ASPM Level: Force L0s - Force all links to L0s state. AUTO - BIOS auto configure. DISABLE - Disables ASPM.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

L1 Substates	Disabled, L1.1, **L1.1 & L1.2**	PCI Express L1 Substates settings.
ACS	Disabled, **Enabled**	Enable/Disable Access Control Services Extended Capability
PTM	Disabled, **Enabled**	Enable/Disable Precision Time Measurement
FOM Scoreboard Control Policy	**Auto**, Gen3, Gen4, Gen3/Gen4	Select the FOM Scoreboard Control Policy, when set to Auto, speed is based on TLS
URR	Disabled, **Enabled**	PCI Express Unsupported Request Reporting Enable/Disable.
FER	Disabled, **Enabled**	PCI Express Device Fatal Error Reporting Enable/Disable.
NFER	Disabled, **Enabled**	PCI Express Device Non-Fatal Error Reporting Enable/Disable.
CER	Disabled, **Enabled**	PCI Express Device Correctable Error Reporting Enable/Disable.
SEFE	**Disabled**, Enabled	Root PCI Express System Error on Fatal Error Enable/Disable.
SENFE	**Disabled**, Enabled	Root PCI Express System Error on Non-Fatal Error Enable/Disable.
SECE	**Disabled**, Enabled	Root PCI Express System Error on Correctable Error Enable/Disable.
PME SCI	**Disabled**, Enabled	PCI Express PME SCI Enable/Disable.
Hot Plug	**Disabled**, Enabled	PCI Express Hot Plug Enable/Disable.
Advanced Error Reporting	Disabled**,** **Enabled**	Advanced Error Reporting Enable/Disable
PCIe Speed	**Auto**, Gen1,	Configure PCIe Speed

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

	Gen2, Gen3, Gen4	
Detect Timeout	**0**	The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.
CompletionTimeout Value	**Default**, 50us to 100us, 1ms to 10ms, 16ms to 55ms, 65ms to 210ms, 260ms to 900ms, 1s to 3.5s, 4s to 13s, 17s to 64s, Disable	PCH PCIE Completion Timeout
LTR	Disabled, **Enabled**	PCH PCIE Latency Reporting Enable/Disable
Snoop Latency Override	Disabled, **Manual**	Non Snoop Latency Override for PCH PCIE.Disabled: Disable override.Manual: Manually enter override values.
Snoop Latency Value	**65**	LTR Snoop Latency value of PCIE, recommended value is 65us so default value to this BIOS knob is 65
Snoop Latency Multiplier	1 ns, 32ns, **1024 ns,** 32768 ns, 1048576 ns, 33554432ns	LTR Snoop Latency Multiplier of PCIE, recommended value is 65us so default value to this BIOS knob is 1024ns which will be multiplied with LTR Value
Non Snoop Latency Override	Disabled, **Manual**	Non Snoop Latency Override for PCH PCIE.Disabled: Disable override.Manual: Manually enter override values.
Non Snoop Latency Value	**65**	LTR Non Snoop Latency value of PCIE, recommended value is 65us so default value to this BIOS knob is 65
Non Snoop Latency Multiplier	1 ns, 32ns, **1024 ns,**	LTR Non Snoop Latency Multiplier of PCIE, recommended value is 65us

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

	32768 ns, 1048576 ns, 33554432ns	
LTR Override Spec Compliant	Spec Compliant – 400ns, **Desired Value – from BIOS option**	By default is Desired Value.When Desired Value is selected, LTR value will be programmed with recommended value. When Spec Compliant is selected, it will program 400ns LTR value and may block platform PG.
P2P Support	Disabled, **Enabled**	Program P2P Support Registers according to setup option
Assertion on Link Down GPIOs	Disabled, **Enabled**	GPIO Assertion on Link Down
PCIe EQ override	Submenu	Choose your own PCIe EQ settings, only for users who have a thorough understanding of equalization process
PCIe EQ override	**Disabled**, Enabled	

7.4.2.1.2. Chipset > PCH-IO Configuration > PCIE Configuration > PCIE clocks

Feature	Options	Description
Clock0 assignment	**Platform-POR,** Enabled, Disabled	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock0	**Platform-POR,** Disabled	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock1 assignment	**Platform-POR,** Enabled, Disabled	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock1	**Platform-POR,** Disabled	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock2 assignment	**Platform-POR,** Enabled, Disabled	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

ClkReq for Clock2	**Platform-POR,** Disabled	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock3 assignment	**Platform-POR,** Enabled, Disabled	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock3	**Platform-POR,** Disabled	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock4 assignment	**Platform-POR,** Enabled, Disabled	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock4	**Platform-POR,** Disabled	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock5 assignment	**Platform-POR,** Enabled, Disabled	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock5	**Platform-POR,** Disabled	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock6 assignment	**Platform-POR,** Enabled, Disabled	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock6	**Platform-POR,** Disabled	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.

7.4.2.2. Chipset > PCH-IO Configuration > USB Configuration

Feature	Options	Description
USB Configuration	Info only	
USB Overcurrent	Disabled, **Enabled**	Select 'Disabled' for pin-based debug. If pin-based debug is enabled but USB overcurrent is not disabled, USB DbC does not work.
USB Overcurrent Lock	Disabled,	Select 'Enabled' if Overcurrent functionality is used. Enabling this will make xHCI controller consume the Overcurrent mapping data

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

	Enabled	
USB Audio Offload	Disabled, **Enabled**	Enable/Disable USB Audio Offload functionality
USB Port Disable Override	**Disabled**, Select Per-Pin	Selectively Enable/Disable the corresponding USB port from reporting a Device Connection to the controller.

7.4.2.3. Chipset > PCH-IO Configuration > Security Configuration

Feature	Options	Description
RTC Memory Lock	Disabled, **Enabled**	Enable will lock bytes 38h-3Fh in the lower/upper 128-byte bank of RTC RAM
BIOS Lock	**Disabled,** Enabled	Enable/Disable the PCH BIOS Lock Enable feature. Required to be enabled to ensure SMM protection of flash.
Force unlock on all GPIO pads	**Disabled,** Enabled	If Enabled BIOS will force all GPIO pads to be in unlocked state

7.4.2.4. Chipset > PCH-IO Configuration > HD Audio Configuration

Feature	Options	Description
HD Audio	Disabled, **Enabled,**	Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled Enabled = HDA will be unconditionally enabled.

7.4.2.5. Chipset > PCH-IO Configuration > Serial I/O Configuration

Feature	Options	Description
I2C0 Controller	**Disbled,** Enabled	Enables/Disables Seriallo Controller, If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device. The following devices depend on each other: I2C0 and I2C1,2,3 UART0 and UART1,SPI0,1 I2C4, I2C5 and UART2 I3C0 and I3C2 UART 0 (00:30:00) cannot be disabled when:1. Child device is enabled like CNVi Bluetooth (_SB.PC00.UA00.BTH0) UART 0 (00:30:00) cannot be enabled when:1. I2S Audio codec is enabled (_SB.PC00.I2C0.HDAC)

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

I2C1 Controller	**Disbled,** Enabled	Enables/Disables Seriallo Controller, If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device. The following devices depend on each other: I2C0 and I2C1,2,3 UART0 and UART1,SPI0,1 I2C4, I2C5 and UART2 I3C0 and I3C2 UART 0 (00:30:00) cannot be disabled when:1. Child device is enabled like CNVi Bluetooth (_SB.PC00.UA00.BTH0) UART 0 (00:30:00) cannot be enabled when:1. I2S Audio codec is enabled (_SB.PC00.I2C0.HDAC)
I2C2 Controller	**Disbled,** Enabled	Enables/Disables Seriallo Controller, If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device. The following devices depend on each other: I2C0 and I2C1,2,3 UART0 and UART1,SPI0,1 I2C4, I2C5 and UART2 I3C0 and I3C2 UART 0 (00:30:00) cannot be disabled when:1. Child device is enabled like CNVi Bluetooth (_SB.PC00.UA00.BTH0) UART 0 (00:30:00) cannot be enabled when:1. I2S Audio codec is enabled (_SB.PC00.I2C0.HDAC)
SPI0 Controller	**Disbled,** Enabled	Enables/Disables Seriallo Controller, If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device. The following devices depend on each other: I2C0 and I2C1,2,3 UART0 and UART1,SPI0,1 I2C4, I2C5 and UART2 I3C0 and I3C2 UART 0 (00:30:00) cannot be disabled when:1. Child device is enabled like CNVi Bluetooth (_SB.PC00.UA00.BTH0) UART 0 (00:30:00) cannot be enabled when:1. I2S Audio codec is enabled (_SB.PC00.I2C0.HDAC)
SPI1 Controller	**Disbled,** Enabled	Enables/Disables Seriallo Controller, If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device. The following devices depend on each other: I2C0 and I2C1,2,3 UART0 and UART1,SPI0,1 I2C4, I2C5 and UART2 I3C0 and I3C2 UART 0 (00:30:00) cannot be disabled when:1. Child device is enabled like CNVi Bluetooth (_SB.PC00.UA00.BTH0) UART 0 (00:30:00) cannot be enabled when:1. I2S Audio codec is enabled (_SB.PC00.I2C0.HDAC)
UART0 Controller	**Disbled,** Enabled	Enables/Disables Seriallo Controller, If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device. The following devices depend on each other: I2C0 and I2C1,2,3 UART0 and UART1,SPI0,1 I2C4, I2C5 and UART2 I3C0 and I3C2 UART 0 (00:30:00) cannot be disabled when:1. Child device is enabled like CNVi Bluetooth (_SB.PC00.UA00.BTH0) UART 0 (00:30:00) cannot be enabled when:1. I2S Audio codec is enabled (_SB.PC00.I2C0.HDAC)
UART2 Controller	**Disbled,** Enabled	Enables/Disables Seriallo Controller, If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device. The following devices depend on each other: I2C0 and I2C1,2,3 UART0 and UART1,SPI0,1 I2C4, I2C5 and UART2 I3C0 and I3C2 UART 0 (00:30:00) cannot be disabled when:1. Child device is enabled like CNVi Bluetooth (_SB.PC00.UA00.BTH0) UART 0 (00:30:00) cannot be enabled when:1. I2S Audio codec is enabled (_SB.PC00.I2C0.HDAC)
GPIO IRQ Route	**IRQ14**,	Route all GPIOs to one of the IRQ.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

	IRQ15	
SerialIO timing parameters	**Disabled,** Enabled	Enables additional timing parameters for all SeraialIO controllers.\nDefaults can be changed in each controller setting.\nPlatform restart required to apply changes

7.5. Security

Feature	Options	Description
Administrator Password	Enter password	Set Administrator Password
User Password	Enter password	Set User Password
Secure Boot	submenu	

7.5.1 Secure->Secure Boot

Feature	Options	Description
Secure Mode	Info only	
Secure Boot	**Disabled** Enabled	The Secure Boot feature is Active if Secure Boot is Enabled, the Platform Key(PK) is enrolled, and the system is in User mode. The mode change requires platform reset
Secure Boot Mode	**Standard** Custom	The Secure Boot mode options: Standard or Custom. In Custom mode, the Secure Boot Policy variables can be configured by a physically present user without full authentication.
Restore Factory Keys	Info only	Force System to User Mode. Install factory default Secure Boot key databases
Reset To Setup Mode	Info only	
Expert Key Management	Submenu	Enables expert users to modify Secure Boot Policy variables without full authentication

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

7.6. Boot

Feature	Options	Description
Boot Configuration	Info only	
Setup Prompt Timeout	**1**	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
Bootup NumLock State	On **Off**	Select the keyboard NumLock state
Quiet Boot	Disabled **Enabled**	Enables or disables Quiet Boot option
Fast Boot	Disabled **Enabled**	Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot option.
SATA Support	**Last Boot SATA Devices Only** All Sata Devices	If Last Boot SATA Devices Only, Only last boot SATA device will be available in Post. If All SATA Devices, all SATA devices will be available in OS and Post.
VGA Support	Auto **EFI Driver**	If Auto, only install Legacy OpRom with Legacy OS and logo would NOT be shown during post. EFI driver will still be installed with EFI OS.
USB Support	Disabled **Full Initial** Partial Initial	If disabled, all USB devices will NOT be available until after OS boot. If Partial Initial, USB Mass Storage and specific USB port/device will NOT be available before OS boot. If enabled, all USB devices will be available in OS and Post.
PS2 Devices Support	Disabled **Enabled**	If disabled, PS2 devices will be skipped.
NetWork Stack Driver Support	**Disabled** Enabled	If Disabled, NetWork Stack Driver will be skipped.
Redirection Support	Disabled **Enabled**	If disable, Redirection function will be disabled.
FIXED Boot ORDER Priorities	Info only	
Boot Option # number	Info only	Set the system boot order

Copyright © 2026 ADLINK Technology, Inc.
ADLINK LEADING EDGE AI COMPUTING
LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

7.7. Save & Exit

Feature	Options	Description
Save Changes and Exit		Exit system setup after saving the changes.
Discard Changes and Exit		Exit system setup without saving any changes.
Save Changes and Reset		Reset the system after saving the changes.
Discard Changes and Reset		Reset system setup without saving any changes.
Save Changes		Save changes done so far to any of the setup options.
Discard Changes		Discard Changes done so far to any of the setup options.
Restore Defaults		Restore/Load Default values for all the setup options.
Save as User Defaults		Save the changes done so far as User Defaults
Restore User Defaults		Restore the User Defaults to all the setup options.
Boot Override	Launch UEFI device	

7.8. MEBx (Corporate only)

Feature	Options	Description
Intel(R) ME Password	Enter password to configure ME	MEBx Login

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

8. BIOS Checkpoints, Beep Codes (update it before product go to mass production)

A status code is a data value used to provide diagnostic information about the boot process. Progress codes are status codes that signify successful progression to a following initialization step. Error codes signify error conditions encountered in the process of system initialization. The Aptio 5.x core can be configured to send status codes to a variety of sources. The two most commonly used types of status codes are checkpoint codes and beep codes. Checkpoint codes are byte length data values. Checkpoints are typically output to I/O port 80h, but the Aptio 5.x core can be configured to send checkpoints to a variety of sources. The Aptio 5.x core outputs checkpoints throughout the boot process to indicate the task the system is currently executing. Checkpoints are very useful in aiding software developers or technicians in debugging problems that occur during the pre-boot process on production hardware. A beep code is a series of short sound signals. Beep codes are typically error codes that do not occur during normal boot process.

Note: Beep codes are not the only sounds generated during the boot process. Some firmware components may use sounds to notify the user about other events such as detection of a hot-pluggable device. These sounds are typically generated using a frequency that is different from the frequency of the beep codes

Viewing Checkpoints

Checkpoints generated by the Aptio firmware can be viewed using a PCI checkpoint card, also referred to as a "POST Card" or "POST Diagnostic Card". These PCI add-on cards show the value of I/O port 80h on an LED display.

Aptio V Checkpoint and Beep Codes

Download the Aptio V Checkpoint and Beep Codes from the AMI website at: www.ami.com/download/aptio-v-checkpoint-and-beep-codes

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

8.1 Status Code Ranges

Status Code Range	Description
0x01 – 0x0F	SEC execution
0x10 – 0x2F	PEI CAR execution
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0xCF	DXE execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

8.2 Standard Status Codes

8.2.1 SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Status Code	Description
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization

SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

8.2.2 PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12 – 0x14	Reserved for CPU
0x15	Pre-memory North Bridge initialization is started

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Status Code	Description
0x16 – 0x18	Reserved for North Bridge
0x19	Pre-memory South Bridge initialization is started
0x1A – 0x1C	Reserved for South Bridge
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38 – 0x3A	Reserved for North Bridge initialization
0x3B	Post-Memory South Bridge initialization is started
0x3C -0x3E	Reserved for South Bridge
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Status Code	Description
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Status Code	Description
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

8.2.2.1 PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

8.2.3 DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64 – 0x67	Reserved for CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B – 0x6F	Reserved for North Bridge DXE initialization (North Bridge module specific)

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Status Code	Description
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73 – 0x77	Reserved for South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Status Code	Description
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Status Code	Description
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

8.2.4 DXE Beep Codes

# of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met (out of resource)

8.2.5 ACPI/ASL Checkpoint

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Status Code	Description
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

8.3 OEM-reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

9. Software Support

9.1. Windows

Windows 11 IoT Enterprise 2024 LTSC (2H' 24)

9.2. Ubuntu 24.04. LTS

Kernel version 6.17.0-19-generic

9.3. Yocto Linux 64-bit

https://github.com/ADLINK/meta-adlink-x86-64bit (TBC)

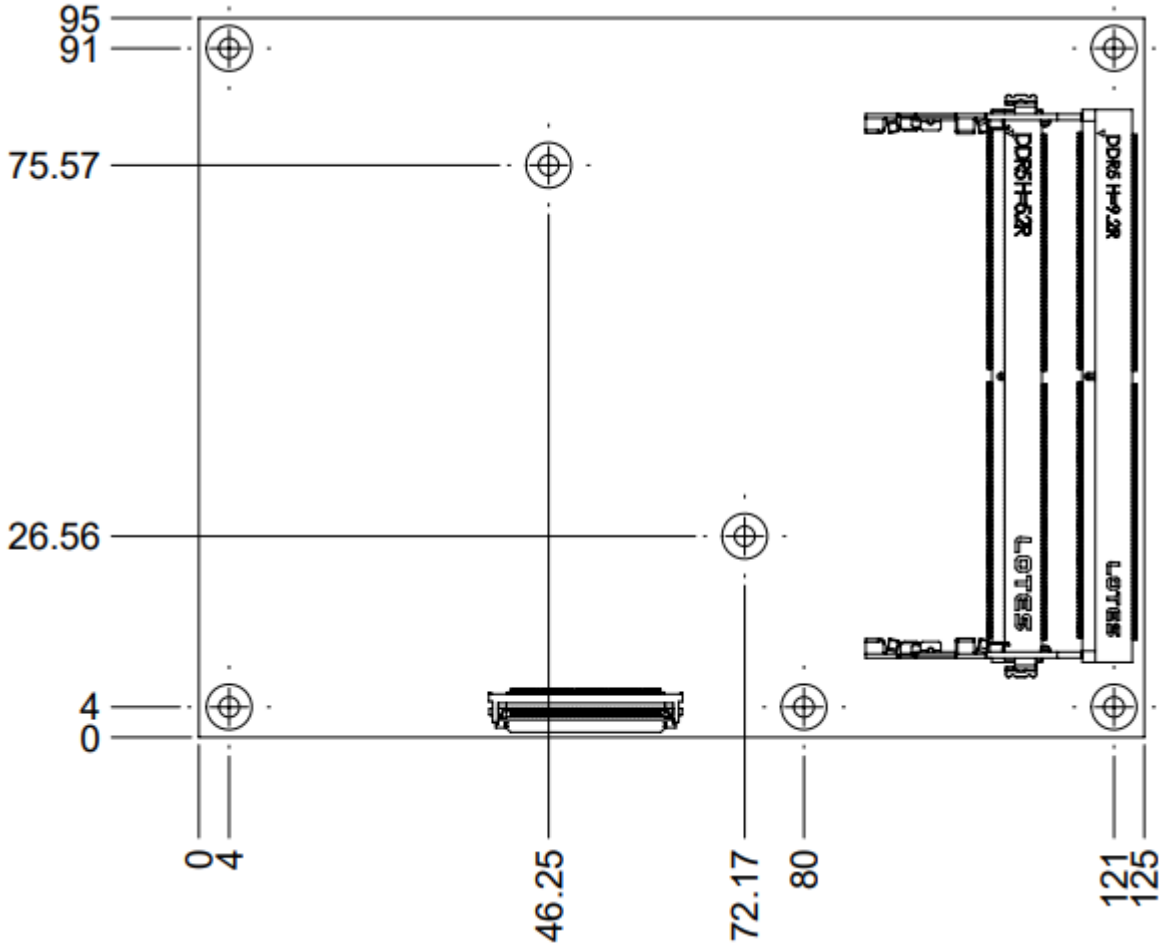
9.4. SEMA API

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

10. Mechanical and Thermal

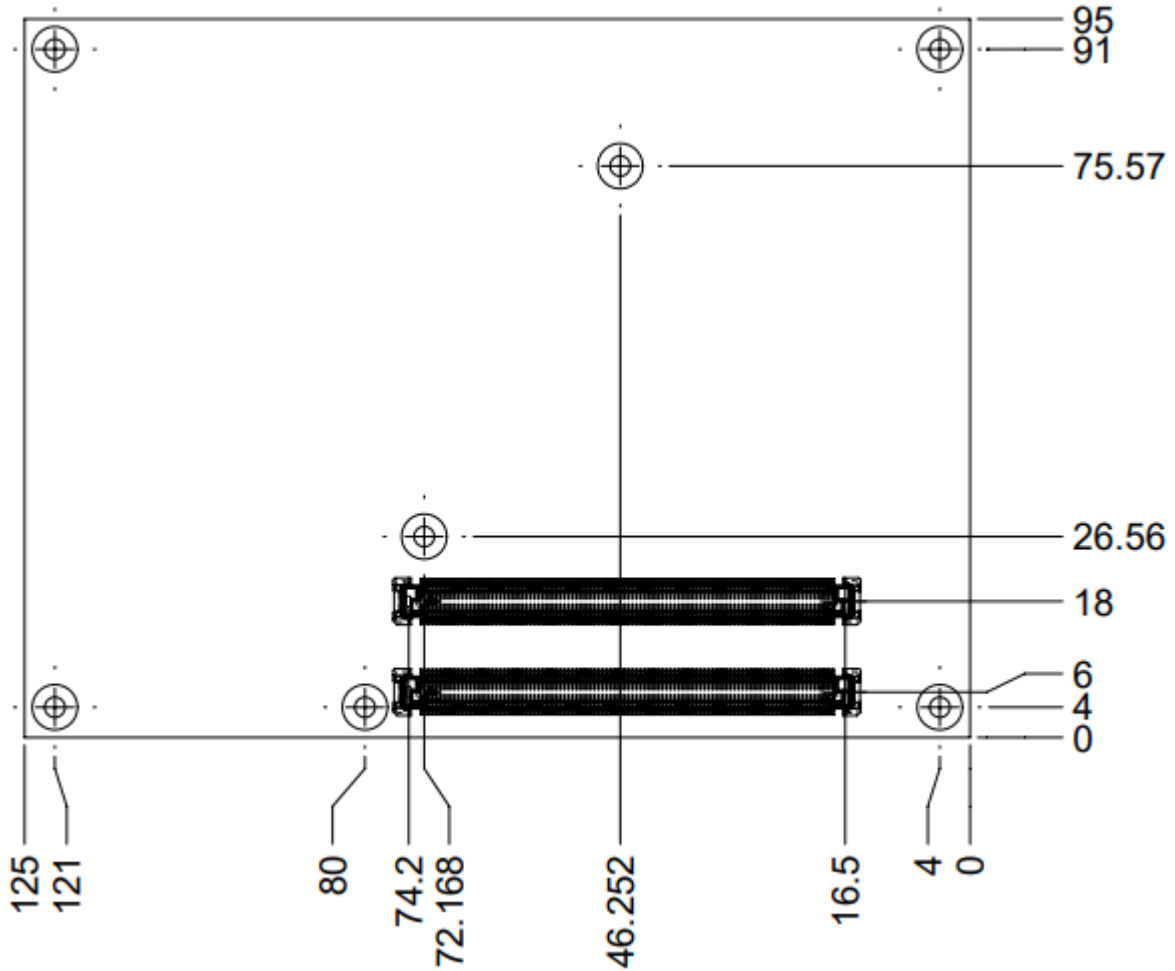
All dimensions are shown in mm with a tolerance of +/- 0.25mm unless otherwise noted.

10.1. Module Dimensions – Top View



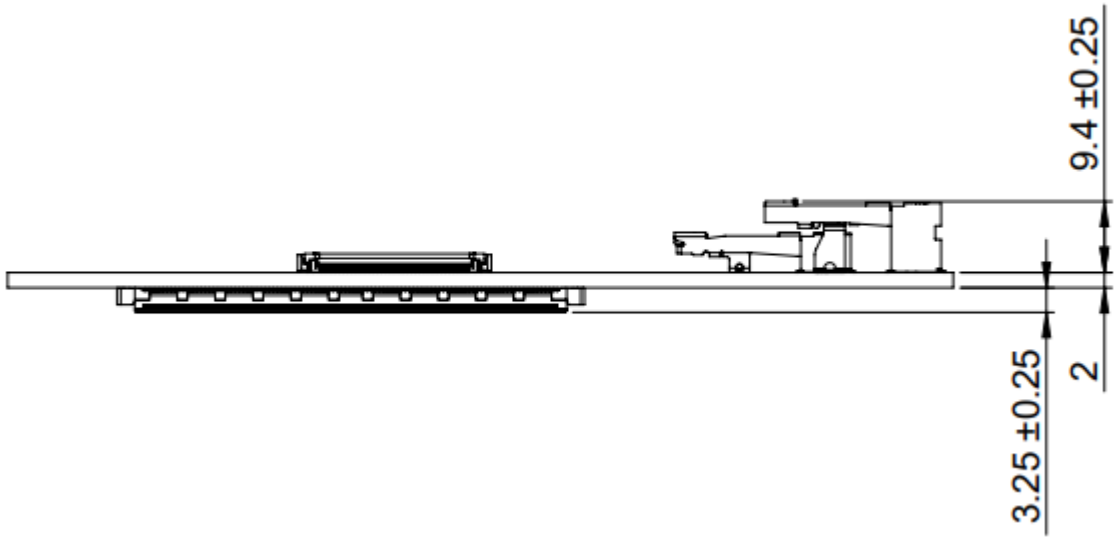
Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

10.2. Module Dimensions – Bottom View



Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

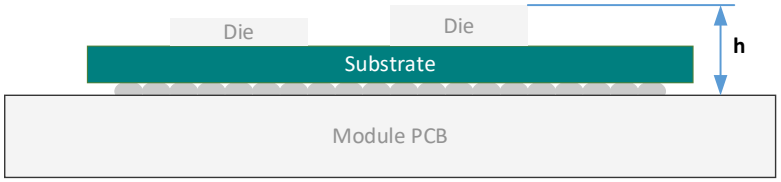
10.3. Module Dimensions – Side View



10.4. Height of Processor and Static Compressive Load

Processor Height Tolerance

The tolerance of the processor height is one of the key factors to consider when designing your thermal solution, as illustrated below. Please contact our ADLINK representative for further details.



	Typical	Tolerance
h	1.28 mm	+/- 0.1mm

Static Compressive Load

Another key factor to consider is the static compressive load. The CExpress-MTL module exhibits a processor maximum pressure die of 40 lbf.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

10.5. Thermal Solutions (update it before product go to mass production)

10.5.1 HTS-B

10.5.2 HTS-BT

10.5.3 THS-B

10.5.4 THS-BT

10.5.5 THSF-B

10.5.6 THSH-B

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

10.6. Board to Board Connectors

To allow for different stacking heights, the receptacles for COM Express carrier boards are available in two heights: 5 mm and 8 mm. When 5-mm receptacles are chosen, the carrier board should be free of components.

Tyco 3-1827253-6, Tyco 2357787-1

ept 401-51101-51, ept 401-51103-51

Foxconn QT002206-2141-3H, Foxconn QT5GB26-44703-3H

- 220-pin board-to-board connector with 0.5mm for a stacking height of **5 mm**.
- This connector can be used with 5-mm through-hole standoffs (SMT type).

Tyco 3-6318491-6, Tyco 2357798-1

ept 401-55101-51, ept 401-55103-51

Foxconn QT002206-4141-3H, Foxconn QT5GB26-74703-3H

- 220-pin board-to-board connector with 0.5mm for a stacking height of **8 mm**.
- This connector can be used with 8-mm through-hole standoffs (SMT type).

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

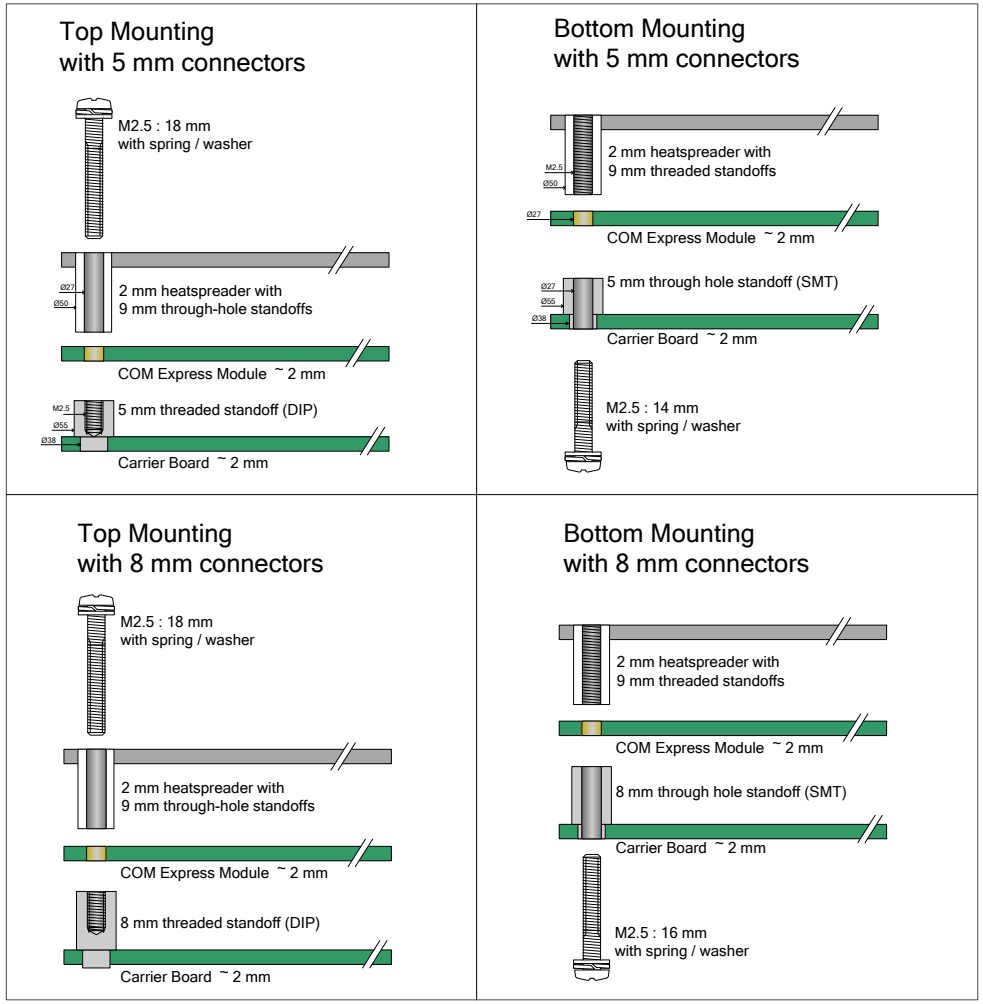
Common Specifications

- Current capacity: 0.5A per pin
- Rated voltage: 50V AC
- Insulation resistance: 100M or greater @ 500 VDC
- Temperature rating: -40°C to 85°C
- UL certification (ECBT2.E28476)
- Copper alloy (contacts)
- Housing: thermo-plastic molded compound (L.C.P.)

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

10.7. Mounting Method

There are several standard ways to mount the COM Express module with a thermal solution onto a carrier board. In addition to the 5-mm or 8-mm board-to-board connectors, there are also top and bottom mounting. In top mounting, the threaded standoffs are on the carrier board and the thermal solution is attached with through-hole standoffs. In bottom mounting, the threaded standoffs are on the thermal solution and the carrier board has through-hole standoffs.

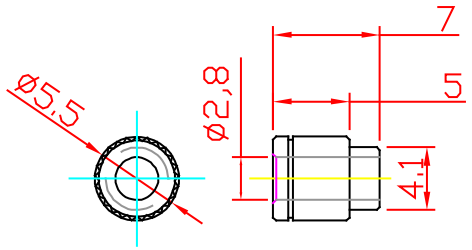


Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

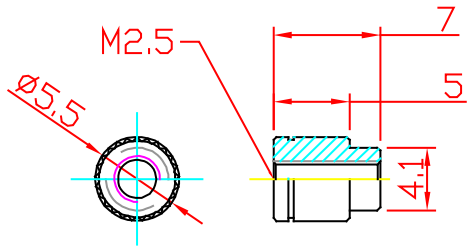
10.8. Standoff Types

The standoffs available for top and bottom mounting methods are shown below. Note that threaded standoffs are DIP type and through-hole standoffs are SMT type. Other types not listed are available upon request.

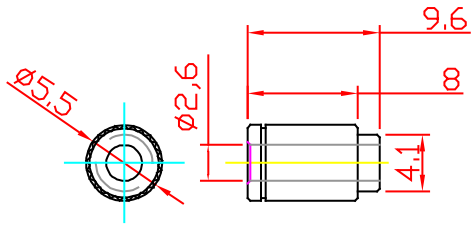
5mm through-hole standoff (SMT type)
P/N: 33-72000-0050



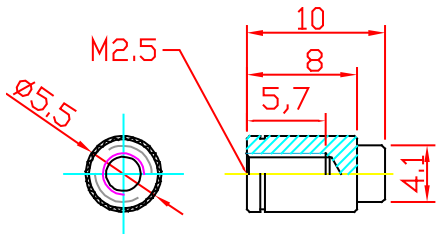
5mm threaded standoff (DIP type)
P/N: 33-72016-0050



8mm through-hole standoff (SMT type)
P/N: 33-72000-0080



8mm threaded standoff (DIP type)
P/N: 33-72015-0050



Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

10.9. Installation (update it before product mass production)

Install a heat spreader or heat sink using the following instructions. The images below are for illustration purpose only.

1. Before mounting the heatsink, install the required memory modules onto the SODIMM socket(s) on the COM Express module.

2. Remove the protective membranes from the thermal pads. All thermal pads have a protective membrane (module dependent)

3. Assemble the heatsink onto the COM Express module. Use the 3x M2.5, L=6mm screws provided to fasten the heatsink to the module. The number of screw holes and screws are module dependent, picture below is for illustration only



4. Place the COM Express module and heatsink assembly onto the connectors on the carrier board as exemplified below.Then press down on the module until it is firmly seated on the carrier board.

5. Use the 5x M2.5, L=16mm screws provided to secure the COM Express module to the carrier board from the solder side.

6. If you are installing a heatsink with a fan, plug the fan connector into the carrier board as shown.

Copyright © 2026 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000