Express-VR7

User's Guide

AMD



COM Express®

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Revision History

Revision	Description	Date	Author
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For user safety, please read and follow all Instructions, **WARNING**s, **CAUTION**s, and **NOTE**s marked in this manual and on the associated equipment before handling/operating the equipment.

Read these safety instructions carefully.

- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

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Conventions

The following conventions may be used throughout this manual, denoting special levels of information

Note: This information adds clarity or specifics to text and illustrations.

Caution: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.

Warning: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

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1. Introduction

Warning: this is an EA (early available) engineering manual, meaning contents might not properly reflect the actual/final version of the product

The Express-VR7 is a COM Express® COM.0 R3.1 Basic Size Type 7 module based on the new-generation and data-communication-focused AMD® Ryzen Embedded processors (formerly "V3000") supporting up to 8 cores (Zen3) at maximum 45W TDP, up to 2x DDR5 SO-DIMMs supporting a maximum of 64GB memory capacity at up to 4800 MT/s. All-around PCIe Gen4 support and integrated 10G Ethernet connectivity makes it suit for high-performance, low-power-consumption, and fast-response-required applications, including, but not limited to, edge networking equipment, 5G infrastructure at the edge, video storage analytics, intelligent surveillance, and industrial automation and control.

Additional extended operating temperature SKUs at 15W TDP (10W configurable), combined with dual-channel ECC memory features makes it fitting for fanless architecture and mission-critical applications in extreme environments.

An integrated AMD® 10G Ethernet controller supports two 10GBASE-KR interfaces, with relevant sideband signals effectively reducing hardware and firmware complexity for system integration. The Express-VR7 is designed to serve customers requiring optimized computing capability per watt and high speed connectivity who want to outsource the custom core logic of their systems for reduced development time.

Input/output features include 14 PCIe Gen4 lanes, a single onboard 2.5-Gigabit Ethernet port, 4x USB 3.0/2.0 ports up to 10Gb/s, and 2x SATA 6 Gb/s ports. Additional General Purpose SPI (GP_SPI) and remoted management dedicated IPMB are offered by project basis. Support for SMBus and I2C is also provided. The module is equipped with SPI AMI EFI BIOS with CMOS backup, supporting embedded features such as remote console, hardware monitor, and watchdog timer.

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2. Specifications

2.1. Core System

CPU

AMD® Zen3 based Ryzen Embedded Processor (formerly "V3000")

- AMD® V3C48 3.3/3.8GHz, 45W with 35-54W cTDP (8C/16T)
- AMD® V3C44 3.5/3.8GHz, 45W with 35-54W cTDP (4C/8T)
- AMD® V3C18I 1.9/3.8GHz, 15W with 10-25W cTDP (8C/16T) (eTEMP)
- AMD® V3C18 1.9/3.8GHz, 15W with 10-25W cTDP (8C/16T)
- AMD® V3C16 2.0/3.8GHz, 15W with 10-25W cTDP (6C/12T)
- AMD® V3C14 2.3/3.8GHz, 15W with 10-25W cTDP (4C/8T)

Memory

Up to 64GB DDR5, dual memory channel in 2x SODIMM sockets, maximum 32GB per socket, ECC or non-ECC

Up to 4800 MT/s memory speed (dependent on SKUs)

2x SODIMM sockets on top side

Cache (L3)

16MB: V3C48, V3C18I, V3C18, V3C16

8MB: V3C44, V3C14

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Embedded BIOS

AMI Aptio V UEFI with CMOS backup in 32 MB SPI BIOS, dual BIOS by build option

2.2. Expansion Buses

8 PCI Express Gen4: Lane 16-23 (two controllers, configurable to 1 x8 or 2 x4)

PCIe reference clock can be PCIE_CK_REF1 (pin B29/B30) or PCIE_CK_REF (pin A88/A89). PCIE_CK_REF1 recommended

4 PCI Express Gen4: Lanes 0-3 (four controllers, configurable to 1 x4, 2 x2/x1) (4 x1 usage supported but requires prior inquiries)

2 PCI Express Gen4: Lane 4-5 (one controller only, configurable to 1 x2/x1)

Note: Preferred Link Configuration on PCIE 0-3 defined by PICMG is 1 x4 or 1 x2 or 1 x1. PCIe Gen4 support also depends on carrier board design

Other: SMBus (system), I^2C (user), LPC bus (via eSPI to LPC bridge IC).

I^2C from CPU is supported by BOM option and project basis

SMBus from EC (embedded controller) is supported by BOM option and project basis

Additional GP_SPI (general purpose SPI by project basis)

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2.3. 10G-KR Ethernet

AMD® Ethernet Controller integrated on CPU

2x 10GBASE-KR and sideband signals

PHY on carrier and PHY firmware are required for 10G SFP+ and Copper 10GBASE-T applications

The recommended PHY for SFP+ is InPhi CS4227, for 10GBASE-T is Marvell AQR113C. The enablement of other PHY may require platform supplier support. The reference 10G adapter card ADLINK offering are named as CEI-CS4227-2x10G-SFP+ and CEI-AQR113C-2x10GBASE-T

10G Ethernet Controller firmware is combined into BIOS code and stored on the same SPI ROM, on COM Express module

10G Ethernet Controller firmware has three type

- one for SFP+ (CS4227 on carrier)
- one for 10GBASE-T (AQR113C on carrier)
- one for KR only usage (no PHY on carrier)

The default setting is TBC. Different type can be selected on BIOS menu (advance -> AMD PBS section)

10G_SDP 0-3 are supported by project basis. 10G_SDP 0-1 optionally works as PPS input and 10G_SDP 2-3 optionally works as PPS output

Note: please contact our local ADLINK representative for information below. (1) Detailed information about circuit design between the Ethernet controller, Optical Fiber/Copper PHY and firmware. (2) Additional MDC/MDIO is offered for specific use case based on 10GBASE-T, by project basis. (3) SGMII offering for specific use case and by project basis. (TBC) (4) 10G_SDP support is by project basis

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2.4. GbE Ethernet

Intel® Ethernet Controller I226 Series

Up to 2.5GbE, 1000/100/10 Mbit/s connections

GBE0_SDP are supported on select SKU and by project basis (TBC)

2.5. Multi I/O and Storage

USB

4x USB 3.0/2.0/1.1 (USB 0, 1, 2, 3)

SuperSpeed, High-Speed, Full-Speed and Low-Speed USB signaling

Up to 10Gb/s and also depends on carrier board design

USB_OC pins share the same source, from SoC.

SATA

2x SATA 6Gb/s (SATA 0,1)

UART

2x UART interfaces SER0 and SER1 RX/TX on module

Console Redirection COM 1 or COM 2 selectable in BIOS

SER0, SER1 from CPU UART are supported by BOM option and project basis

Up to 4 serial ports supported by standard BIOS, including Super I/O on carrier board

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COM Port	Description	IRQ	Address	Console Redirection Support
COM 1	Supported by module (SER0, A98/A99), via embedded controller	4	0x3F8	Yes
COM 2	Supported by module (SER1, A101/A102), via embedded controller	3	0x2F8	Yes
COM 3	Supported by Super I/O (W83627DHG) on carrier board	5	0x240	Yes
COM 4	Supported by Super I/O (W83627DHG) on carrier board	7	0x248	Yes

GPIO ~~or SD~~

4 GPO and 4 GPI (GPI with interrupt, TBC)

GPI and GPO from CPU GPIO are supported by BOM option and project basis

2.6. Trusted Platform Module (TPM)

Chipset: Infineon solution

Type: TPM 2.0 (SPI bus-based)

TPM chip is supported by project basis

2.7. SEMA Board Controller

Supports: Voltage/current monitoring, power sequence debug support, AT/ATX mode control, logistics and forensic information, ~~flat panel control~~, general purpose I2C, failsafe BIOS (dual BIOS, opt. support), watchdog timer and fan control

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2.8. IPMB (Intelligent Platform Management Bus)

An IPMB ("Intelligent Platform Management Bus") port is defined for platform management functions. The IPMB is used (optionally) with a Carrier based BMC (Board Management Controller) Master. On the Module, the IPMB should be routed to and used with a MMC (Module Management Controller). The Module IPMB is a slave port and uses I2C signaling.

IPMB through a MMC is build option support and by project basis

The conjunction between Module MMC and Carrier BMC is still in developing (TBC)

2.9. Debug

40-pin flat cable connector for use with DB40-HPC debug module

Supports embedded controller access, SPI BIOS flashing, internal power rail test points, debug LEDs, and BIOS POST code LED

2.10. Power

Power Modes: AT and ATX mode (AT mode startup controlled by SEMA Board Controller)

Standard Voltage Input: AT: 12V±5% or ATX: 12V±5% / 5Vsb ±5%

Wide Voltage Input: AT: 8.5-20V or ATX: 8.5-20V / 5Vsb ±5% (only for standard operating temperature)

Power Management: ACPI 5.0 compliant

Power States: C0-C3, S0, S5, S5 ECO mode (Wake-on-USB S3, WoL S3/S5)

ECO Mode support for deep S5 for 5Vsb power saving

Power Consumption
Please contact your ADLINK representative for the document "COM Express Module Power Consumption".

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2.11. Mechanical and Environmental

Form Factor and specification

PICMG COM Express Rev 3.1 (COM.0 R3.1), Type 7, Basic size 125 x 95 mm

Operating Temperature

Standard	0°C to 60°C	Storage: -20°C to 80°C
Extreme Rugged	-40°C to 85°C	Storage: -40°C to 85°C (build option by project basis, selected SoC SKUs)

Humidity

5-90% RH operating, non-condensing, 5-95% RH storage (and operating with conformal coating)

Shock and Vibration

IEC 60068-2-64 and IEC-60068-2-27
MIL-STD-202F, Method 213B, Table 213-I, Condition A and Method 214A, Table 214-I, Condition D

HALT tested

Thermal Stress, Vibration Stress, Thermal Shock and Combined Test

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3. Block Diagram

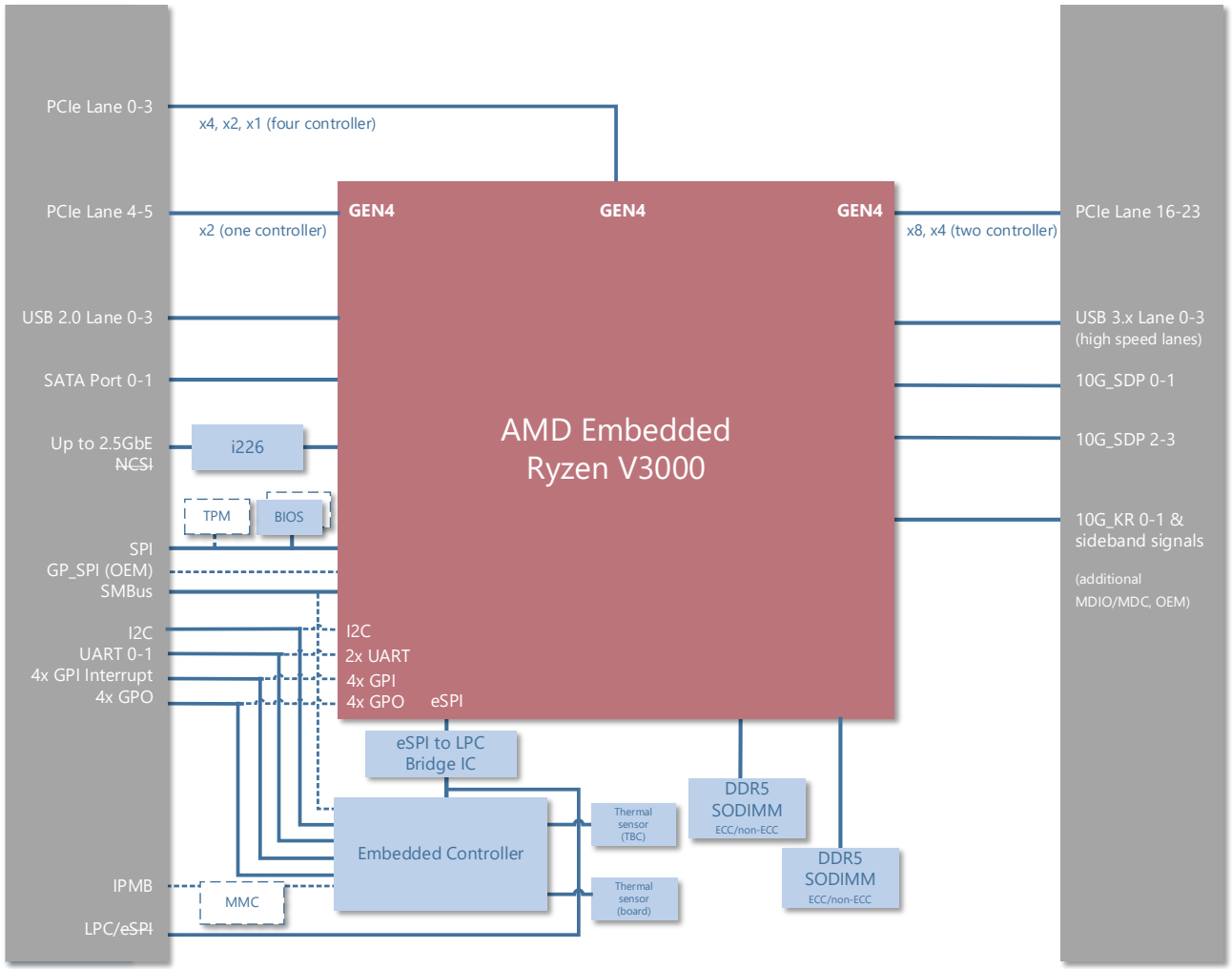


Figure 1 – Module functional block diagram

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4. Pinout and Signal Descriptions

4.1. Pin Summary

The table below is a comprehensible list of all signal pins supported on the dual 220-pin COM Express connectors as defined for Type 7 in the PICMG COM.0 R3.1 specification. Signals described in the specification but not supported on the Express-VR7 are strikethrough ~~STRIKETHROUGH~~

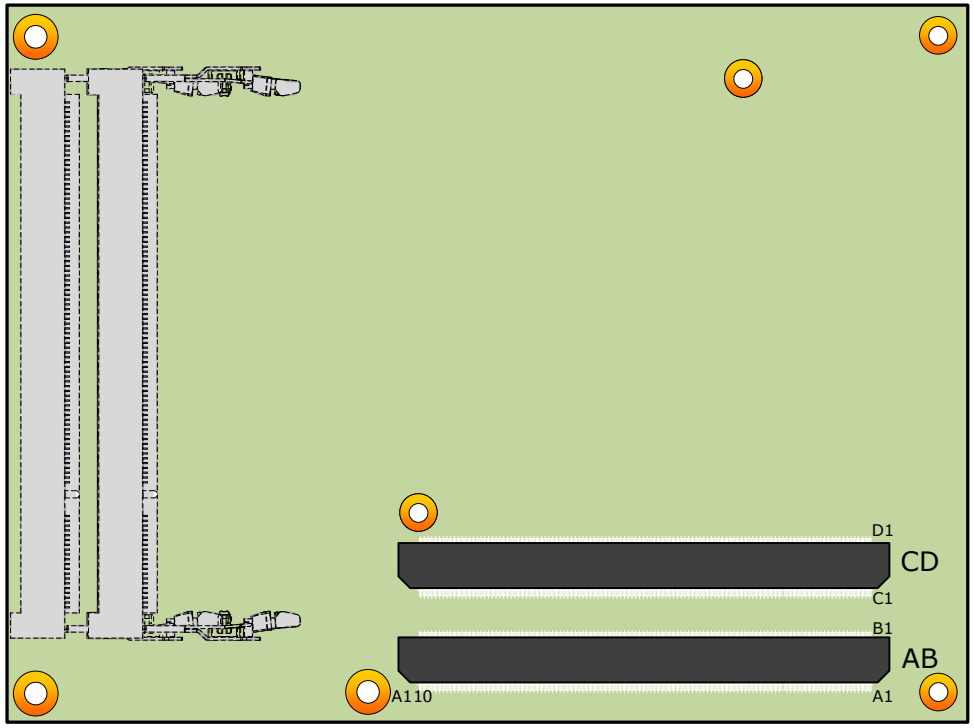


Figure 2 - Module rear side row and pin numbering

Note: The 2x SO-DIMM sockets (grey color) are located on top side.

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Row A			Row B			Row C			Row D	
A1	GND (fixed)		B1	GND (fixed)		C1	GND (fixed)		D1	GND (fixed)
A2	GBE0_MDI3-		B2	GBE0_ACT#		C2	GND		D2	GND
A3	GBE0_MDI3+		B3	LPC_FRAME#		C3	USB_SSRX0-		D3	USB_SSTX0-
A4	**GBE0_LINK_MID#**		B4	LPC_AD0		C4	USB_SSRX0+		D4	USB_SSTX0+
A5	**GBE0_LINK_MAX#**		B5	LPC_AD1		C5	GND		D5	GND
A6	GBE0_MDI2-		B6	LPC_AD2		C6	USB_SSRX1-		D6	USB_SSTX1-
A7	GBE0_MDI2+		B7	LPC_AD3		C7	USB_SSRX1+		D7	USB_SSTX1+
A8	GBE0_LINK#		B8	~~LPC_DRQ0#~~		C8	GND		D8	GND
A9	GBE0_MDI1-		B9	~~LPC_DRQ1#~~		C9	USB_SSRX2-		D9	USB_SSTX2-
A10	GBE0_MDI1+		B10	LPC_CLK		C10	USB_SSRX2+		D10	USB_SSTX2+
A11	GND (fixed)		B11	GND (fixed)		C11	GND (fixed)		D11	GND (fixed)
A12	GBE0_MDI0-		B12	PWRBTN#		C12	USB_SSRX3-		D12	USB_SSTX3-
A13	GBE0_MDI0+		B13	SMB_CK		C13	USB_SSRX3+		D13	USB_SSTX3+
A14	~~GBE0_CTREF~~		B14	SMB_DAT		C14	GND		D14	GND
A15	SUS_S3#		B15	SMB_ALERT#		C15	**RSVD10G**		D15	**RSVD10G**
A16	SATA0_TX+		B16	SATA1_TX+		C16	**RSVD10G**		D16	**RSVD10G**
A17	SATA0_TX-		B17	SATA1_TX-		C17	10G_SDP2*		D17	10G_SDP3*
A18	SUS_S4#		B18	~~SUS_STAT#~~		C18	GND		D18	GND
A19	SATA0_RX+		B19	SATA1_RX+		C19	~~PCIE_RX6+~~		D19	~~PCIE_TX6+~~
A20	SATA0_RX-		B20	SATA1_RX-		C20	~~PCIE_RX6-~~		D20	~~PCIE_TX6-~~
A21	GND (fixed)		B21	GND (fixed)		C21	GND (fixed)		D21	GND (fixed)
A22	~~PCIE_TX15+~~		B22	~~PCIE_RX15+~~		C22	~~PCIE_RX7+~~		D22	~~PCIE_TX7+~~
A23	~~PCIE_TX15-~~		B23	~~PCIE_RX15-~~		C23	~~PCIE_RX7-~~		D23	~~PCIE_TX7-~~
A24	SUS_S5#		B24	PWR_OK		C24	**RSVD10G**		D24	**RSVD10G**
A25	~~PCIE_TX14+~~		B25	~~PCIE_RX14+~~		C25	GND		D25	GND
A26	~~PCIE_TX14-~~		B26	~~PCIE_RX14-~~		C26	~~10G_KR_RX3+~~		D26	~~10G_KR_TX3+~~
A27	BATLOW#		B27	WDT		C27	~~10G_KR_RX3-~~		D27	~~10G_KR_TX3-~~
A28	(S)ATA_ACT#		B28	GND		C28	GND		D28	GND
A29	RSVD		B29	**PCIE_CK_REF1+**		C29	~~10G_KR_RX2+~~		D29	~~10G_KR_TX2+~~
A30	RSVD		B30	**PCIE_CK_REF1-**		C30	~~10G_KR_RX2-~~		D30	~~10G_KR_TX2-~~
A31	GND (fixed)		B31	GND (fixed)		C31	GND (fixed)		D31	GND (fixed)
A32	**IPMB_CLK***		B32	SPKR		C32	**RSVD10G**		D32	**RSVD10G / GP_SPI_CLK***
A33	**IPMB_DAT***		B33	I2C_CK		C33	**RSVD10G**		D33	**RSVD10G / GP_SPI_MOSI***
A34	BIOS_DIS0#		B34	I2C_DAT		C34	**RSVD10G**		D34	**RSVD10G / GP_SPI_MISO***
A35	THRMTRIP#		B35	THRM#		C35	**CEI_RST#**		D35	**CEI_PRSNT#**

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Row A			Row B			Row C			Row D	
A36	~~PCIE_TX13+~~		B36	~~PCIE_RX13+~~		C36	**RSVD10G**		D36	RSVD / **GP_SPI_CS#***
A37	~~PCIE_TX13-~~		B37	~~PCIE_RX13-~~		C37	**RSVD10G**		D37	RSVD
A38	GND		B38	GND		C38	**RSVD10G**		D38	**RSVD10G**
A39	~~PCIE_TX12+~~		B39	~~PCIE_RX12+~~		C39	**CEI_SDA**		D39	**CEI_SCL**
A40	~~PCIE_TX12-~~		B40	~~PCIE_RX12-~~		C40	10G_SDP0*		D40	10G_SDP1*
A41	GND (fixed)		B41	GND (fixed)		C41	GND (fixed)		D41	GND (fixed)
A42	USB2-		B42	USB3-		C42	10G_KR_RX1+		D42	10G_KR_TX1+
A43	USB2+		B43	USB3+		C43	10G_KR_RX1-		D43	10G_KR_TX1-
A44	USB_2_3_OC#		B44	USB_0_1_OC#		C44	GND		D44	GND
A45	USB0-		B45	USB1-		C45	**RSVD10G / 10G_PHY_MDC_SCL1***		D45	**RSVD10G / 10G_PHY_MDIO_SDA1***
A46	USB0+		B46	USB1+		C46	**CEI_MDC**		D46	**CEI_MDIO**
A47	VCC_RTC		B47	~~ESPI_EN#~~		C47	**CEI_INT#**		D47	**ETH_PHY_INT#**
A48	**RSMRST_OUT#**		B48	~~USB0_HOST_PRSNT~~		C48	GND		D48	GND
A49	GBE0_SDP*		B49	SYS_RESET#		C49	10G_KR_RX0+		D49	10G_KR_TX0+
A50	LPC_SERIRQ		B50	CB_RESET#		C50	10G_KR_RX0-		D50	10G_KR_TX0-
A51	GND (fixed)		B51	GND (fixed)		C51	GND (fixed)		D51	GND (fixed)
A52	PCIE_TX5+		B52	PCIE_RX5+		C52	PCIE_RX16+		D52	PCIE_TX16+
A53	PCIE_TX5-		B53	PCIE_RX5-		C53	PCIE_RX16-		D53	PCIE_TX16-
A54	GPI0		B54	GPO1		C54	TYPE0#		D54	GND
A55	PCIE_TX4+		B55	PCIE_RX4+		C55	PCIE_RX17+		D55	PCIE_TX17+
A56	PCIE_TX4-		B56	PCIE_RX4-		C56	PCIE_RX17-		D56	PCIE_TX17-
A57	GND		B57	GPO2		C57	TYPE1#		D57	TYPE2#
A58	PCIE_TX3+		B58	PCIE_RX3+		C58	PCIE_RX18+		D58	PCIE_TX18+
A59	PCIE_TX3-		B59	PCIE_RX3-		C59	PCIE_RX18-		D59	PCIE_TX18-
A60	GND (fixed)		B60	GND (fixed)		C60	GND (fixed)		D60	GND (fixed)
A61	PCIE_TX2+		B61	PCIE_RX2+		C61	PCIE_RX19+		D61	PCIE_TX19+
A62	PCIE_TX2-		B62	PCIE_RX2-		C62	PCIE_RX19-		D62	PCIE_TX19-
A63	GPI1		B63	GPO3		C63	GND		D63	GND
A64	PCIE_TX1+		B64	PCIE_RX1+		C64	GND		D64	GND
A65	PCIE_TX1-		B65	PCIE_RX1-		C65	PCIE_RX20+		D65	PCIE_TX20+
A66	GND		B66	WAKE0#		C66	PCIE_RX20-		D66	PCIE_TX20-
A67	GPI2		B67	WAKE1#		C67	~~RAPID_SHUTDOWN~~		D67	GND
A68	PCIE_TX0+		B68	PCIE_RX0+		C68	PCIE_RX21+		D68	PCIE_TX21+
A69	PCIE_TX0-		B69	PCIE_RX0-		C69	PCIE_RX21-		D69	PCIE_TX21-
A70	GND (fixed)		B70	GND (fixed)		C70	GND (fixed)		D70	GND (fixed)

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Row A			Row B			Row C			Row D	
A71	~~PCIE_TX8+~~		B71	~~PCIE_RX8+~~		C71	PCIE_RX22+		D71	PCIE_TX22+
A72	~~PCIE_TX8-~~		B72	~~PCIE_RX8-~~		C72	PCIE_RX22-		D72	PCIE_TX22-
A73	GND		B73	GND		C73	GND		D73	GND
A74	~~PCIE_TX9+~~		B74	~~PCIE_RX9+~~		C74	PCIE_RX23+		D74	PCIE_TX23+
A75	~~PCIE_TX9-~~		B75	~~PCIE_RX9-~~		C75	PCIE_RX23-		D75	PCIE_TX23-
A76	GND		B76	GND		C76	GND		D76	GND
A77	~~PCIE_TX10+~~		B77	~~PCIE_RX10+~~		C77	GND		D77	GND
A78	~~PCIE_TX10-~~		B78	~~PCIE_RX10-~~		C78	~~PCIE_RX24+~~		D78	~~PCIE_TX24+~~
A79	GND		B79	GND		C79	~~PCIE_RX24-~~		D79	~~PCIE_TX24-~~
A80	GND (fixed)		B80	GND (fixed)		C80	GND (fixed)		D80	GND (fixed)
A81	~~PCIE_TX11+~~		B81	~~PCIE_RX11+~~		C81	~~PCIE_RX25+~~		D81	~~PCIE_TX25~~
A82	~~PCIE_TX11-~~		B82	~~PCIE_RX11-~~		C82	~~PCIE_RX25-~~		D82	~~PCIE_TX25-~~
A83	GND		B83	GND		C83	GND		D83	GND
A84	~~NCSI_TX_EN~~		B84	VCC_5V_SBY		C84	GND		D84	GND
A85	GPI3		B85	VCC_5V_SBY		C85	~~PCIE_RX26+~~		D85	~~PCIE_TX26+~~
A86	RSVD		B86	VCC_5V_SBY		C86	~~PCIE_RX26-~~		D86	~~PCIE_TX26-~~
A87	GND		B87	VCC_5V_SBY		C87	GND		D87	GND
A88	PCIE0_CK_REF+		B88	BIOS_DIS1#		C88	~~PCIE_RX27+~~		D88	~~PCIE_TX27+~~
A89	PCIE0_CK_REF-		B89	~~NSCI_RX_ER~~		C89	~~PCIE_RX27-~~		D89	~~PCIE_TX27-~~
A90	GND (fixed)		B90	GND (fixed)		C90	GND (fixed)		D90	GND (fixed)
A91	SPI_POWER		B91	~~NCSI_CLK_IN~~		C91	~~PCIE_RX28+~~		D91	~~PCIE_TX28+~~
A92	SPI_MISO		B92	~~NCSI_RXD1~~		C92	~~PCIE_RX28-~~		D92	~~PCIE_TX28-~~
A93	GPO0		B93	~~NCSI_RXD0~~		C93	GND		D93	GND
A94	SPI_CLK		B94	~~NCSI_CRS_DV~~		C94	~~PCIE_RX29+~~		D94	~~PCIE_TX29+~~
A95	SPI_MOSI		B95	~~NCSI_TXD1~~		C95	~~PCIE_RX29-~~		D95	~~PCIE_TX29-~~
A96	~~TPM_PP~~		B96	~~NCSI_TXD0~~		C96	GND		D96	GND
A97	~~TYPE10#~~		B97	SPI_CS#		C97	GND		D97	GND
A98	SER0_TX		B98	~~NCSI_ARB_IN~~		C98	~~PCIE_RX30+~~		D98	~~PCIE_TX30+~~
A99	SER0_RX		B99	~~NCSI_ARB_OUT~~		C99	~~PCIE_RX30-~~		D99	~~PCIE_TX30-~~
A100	GND (fixed)		B100	GND (fixed)		C100	GND (fixed)		D100	GND (fixed)
A101	SER1_TX		B101	FAN_PWMOUT		C101	~~PCIE_RX31+~~		D101	~~PCIE_TX31+~~
A102	SER1_RX		B102	FAN_TACHIN		C102	~~PCIE_RX31-~~		D102	~~PCIE_TX31-~~
A103	LID#		B103	SLEEP#		C103	GND		D103	GND
A104	VCC_12V		B104	VCC_12V		C104	VCC_12V		D104	VCC_12V
A105	VCC_12V		B105	VCC_12V		C105	VCC_12V		D105	VCC_12V

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Row A			Row B			Row C			Row D	
A106	VCC_12V		B106	VCC_12V		C106	VCC_12V		D106	VCC_12V
A107	VCC_12V		B107	VCC_12V		C107	VCC_12V		D107	VCC_12V
A108	VCC_12V		B108	VCC_12V		C108	VCC_12V		D108	VCC_12V
A109	VCC_12V		B109	VCC_12V		C109	VCC_12V		D109	VCC_12V
A110	GND (fixed)		B110	GND (FIXED)		C110	GND (FIXED)		D110	GND (FIXED)

Note:

1. 10G SFP+ or 10GBASE-T support is based on CEI mode (sideband signal arrangement related) and requires PHY (CS4227 or AQR113C) along with on-carrier firmware, for SFP+ or 10GBASE-T applications. A reference design will be offered. Please contact our ADLINK representative for availability.

2. Another PCIe clock (PCIE_CK_REF1) defined by PICMG COM.0 R3.1 can be used for PCIe lane 16-23. Check pin B29, B30.

3. Features listed below are supported by project basis (1) IPMB function (2) GBE0_SDP with specific LAN controller (3) 10G_SDP 0-3. (4) GP_SPI, general purpose SPI. (5) Additional MDC/MDIO (10G_PHY_MDC_SCL1, 10G_PHY_MDIO_SDA1). All these project basis support features are still in development stage.

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4.2. Signal Terminology Descriptions

Meaning of the terms used for signal description tables

Term	Description
I	Input to the module
O	Output from the module
I/O	Bi-directional Input / Output
OD	Open drain output from the module
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I/O $3.3V_{SB}$	Input or output 3.3V tolerant active in standby state
DDC	Display Data Channel
PCIE	PCI Express compatible differential signal
PEG	PCI Express Graphics
SATA	Serial ATA specification Revision 2.6 and 3
LVDS	Low Voltage Differential Signal - 330 mV nominal; 450 mV maximum differential signal
P	Power Input / Output
REF	Reference voltage output. May be sourced from a Module power plane.
PDS	Pull-down strap. A Module output pin that is either tied to GND or is not connected. Used to signal Module capabilities to the Carrier Board.
PU	PU (pull-up) resistor on module
PD	PD (pull-down) resistor on module

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4.3. AB Connector Signal Descriptions

4.3.1 Network Controller Sideband Interface (NC-SI)

Name	Pin #	Description	I/O	PU / PD	Comment
~~NCSI_CLK_IN~~	~~B91~~	~~Clock reference for receive, transmit and control interface~~	~~I 3.3VSB~~	~~PD 10K~~	Not supported
~~NCSI_RXD[1:0]~~	~~B92~~ ~~B93~~	~~Receive Data (from NC to BMC)~~	~~O~~ ~~3.3VSB~~	~~PU 10K~~ ~~3.3VSB~~	Not supported
~~NCSI_TXD[1:0]~~	~~B95~~ ~~B96~~	~~Transmit Data (from BMC to NC)~~	~~I 3.3VSB~~	~~PU 10K~~ ~~3.3VSB~~	Not supported
~~NCSI_CRS_DV~~	~~B94~~	~~Carrier Sense/Receive Data valid to MC, indicating that the transmitted data from NC to BMC is valid~~	~~O~~ ~~3.3VSB~~	~~PD 10K~~	Not supported
~~NCSI_TX_EN~~	~~A84~~	~~Transmit enable~~	~~I 3.3VSB~~	~~PD 10K~~	Not supported
~~NCSI_RX_ER~~	~~B89~~	~~Receive error~~	~~O~~ ~~3.3VSB~~		Not supported
~~NCSI_ARB_IN~~	~~B98~~	~~Network Controller hardware arbitration input~~	~~I 3.3VSB~~		Not supported
~~NCSI_ARB_OUT~~	~~B99~~	~~Network Controller hardware arbitration output~~	~~O~~ ~~3.3VSB~~		Not supported

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4.3.2 Gigabit Ethernet

Name	Pin #	Description	I/O	PU / PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: 1000 / 100 / 10 MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	I/O Analog		Twisted pair signals for external transformer.
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.	OD 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.	OD 3.3VSB		
GBE0_LINK_MID#	A4	Gigabit Ethernet Controller MID Speed Link indicator. Active low. If active, the link is established but at a speed lower than the maximum speed supported by the Ethernet controller. Note that based on capabilities of the Ethernet controller used this signal might not be active for all possible lower link speeds. Was GBE0_LINK100# in COM Express Rev. 3.0.	OD 3.3VSB		
GBE0_LINK_MAX#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low. Gigabit Ethernet Controller MAX Speed Link Indicator. Active low. If active, the link is established at the maximum link speed supported by the controller. Was GBE0_LINK1000# in COM Express Rev. 3.0.	OD 3.3VSB		
~~GBE0_CTREF~~	~~A14~~	~~Reference voltage for Carrier Board Ethernet channel 1 and 2 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be 250 mA or less.~~	~~REF~~ ~~GND min~~ ~~3.3V max~~		Not supported
GBE0_SDP	A49	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as 1pps signal.	IO 3.3VSB		Depends on the selection of LAN controller, project basis

Note: GBE0_ACT# and GBE0_LINK# share the same pin from LAN controller.

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4.3.3 SATA

Name	Pin #	Description	I/O	PU / PD	Comment
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		AC coupled on Module
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		AC coupled on Module
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	O 3.3V	PU 10K 3.3V	

4.3.3.1. I/O Assignments

Name	Physical Lane on CPU	Comment
SATA0	Lane 10	
SATA1	Lane 11	

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4.3.4 PCI Express

Name	Pin #	Description	I/O	PU / PD	Comment
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		AC coupled off Module
~~PCIE_TX8+ PCIE_TX8-~~	~~A71 A72~~	~~PCI Express channel 8, Transmit Output differential pair.~~	~~O PCIE~~		Not supported
~~PCIE_RX8+ PCIE_RX8-~~	~~B71 B72~~	~~PCI Express channel 8, Receive Input differential pair.~~	~~I PCIE~~		Not supported
~~PCIE_TX9+ PCIE_TX9-~~	~~A74 A75~~	~~PCI Express channel 9, Transmit Output differential pair.~~	~~O PCIE~~		Not supported

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Name	Pin #	Description	I/O	PU / PD	Comment
~~PCIE_RX9+ PCIE_RX9-~~	~~B74 B75~~	~~PCI Express channel 9, Receive Input differential pair.~~	~~I PCIE~~		Not supported
~~PCIE_TX10+ PCIE_TX10-~~	~~A77 A78~~	~~PCI Express channel 10, Transmit Output differential pair.~~	~~O PCIE~~		Not supported
~~PCIE_RX10+ PCIE_RX10-~~	~~B77 B78~~	~~PCI Express channel 10, Receive Input differential pair.~~	~~I PCIE~~		Not supported
~~PCIE_TX11+ PCIE_TX11-~~	~~A81 A82~~	~~PCI Express channel 11, Transmit Output differential pair.~~	~~O PCIE~~		Not supported
~~PCIE_RX11+ PCIE_RX11-~~	~~B81 B82~~	~~PCI Express channel 11, Receive Input differential pair.~~	~~I PCIE~~		Not supported
~~PCIE_TX12+ PCIE_TX12-~~	~~A39 A40~~	~~PCI Express channel 12, Transmit Output differential pair.~~	~~O PCIE~~		Not supported
~~PCIE_RX12+ PCIE_RX12-~~	~~B39 B40~~	~~PCI Express channel 12, Receive Input differential pair.~~	~~I PCIE~~		Not supported
~~PCIE_TX13+ PCIE_TX13-~~	~~A36 A37~~	~~PCI Express channel 13, Transmit Output differential pair.~~	~~O PCIE~~		Not supported
~~PCIE_RX13+ PCIE_RX13-~~	~~B36 B37~~	~~PCI Express channel 13, Receive Input differential pair.~~	~~I PCIE~~		Not supported
~~PCIE_TX14+ PCIE_TX14-~~	~~A25 A26~~	~~PCI Express channel 14, Transmit Output differential pair.~~	~~O PCIE~~		Not supported
~~PCIE_RX14+ PCIE_RX14-~~	~~B25 B26~~	~~PCI Express channel 14, Receive Input differential pair.~~	~~I PCIE~~		Not supported
~~PCIE_TX15+ PCIE_TX15-~~	~~A22 A23~~	~~PCI Express channel 15, Transmit Output differential pair.~~	~~O PCIE~~		Not supported
~~PCIE_RX15+ PCIE_RX15-~~	~~B22 B23~~	~~PCI Express channel 15, Receive Input differential pair.~~	~~I PCIE~~		Not supported
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		
PCIE_CLK_REF1+ PCIE_CLK_REF1-	B29 B30	Second reference clock output for higher speed PCI Express implementation on Lanes 16 to 31, for Type 7 implementations only	O PCIE		

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Note: Both of PCIE_CLK_REF1 and PCIE_CLK_REF can be used for PCIe lane 16-23 but PCIE_CLK_REF1 preferred

PCI Express lane configuration as below

Connector	PCIe Lanes #	Ref. Clk #		Preferred Link Configurations		
		Preferred	Optional			
A / B	0	Ref_0	Ref_0 / Ref_1	x1	x2	x4
	1	Ref_0	Ref_0 / Ref_1	x1*		
	2	Ref_0	Ref_0 / Ref_1	x1*	x2*	
	3	Ref_0	Ref_0 / Ref_1	x1*		
	4	Ref_0	Ref_0 / Ref_1	x1	x2	
	5	Ref_0	Ref_0 / Ref_1			
C / D	16	Ref_1	Ref_0 / Ref_1	x1	x2	x4
	17	Ref_1	Ref_0 / Ref_1			
	18	Ref_1	Ref_0 / Ref_1			
	19	Ref_1	Ref_0 / Ref_1			
	20	Ref_1	Ref_0 / Ref_1	x1	x2	x4
	21	Ref_1	Ref_0 / Ref_1			
	22	Ref_1	Ref_0 / Ref_1			
	23	Ref_1	Ref_0 / Ref_1			

Note: PCIe Lane 1, 2, 3 can be used as x1 but requires prior inquiries. PCIe Lane 2-3 can be used as one x2 but requires prior inquiries

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4.3.4.1. I/O Assignments

Name	Physical Lane on CPU	Comment
PCIE0	Lane 12	
PCIE1	Lane 13	
PCIE2	Lane 14	
PCIE3	Lane 15	
PCIE4	Lane 16	
PCIE5	Lane 17	
PCIE16	Lane 7	
PCIE17	Lane 6	
PCIE18	Lane 5	
PCIE19	Lane 4	
PCIE20	Lane 3	
PCIE21	Lane 2	
PCIE22	Lane 1	
PCIE23	Lane 0	

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4.3.5 LPC Bus

Name	Pin #	Description	I/O	PU / PD	Comment
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	B4 B5 B6 B7	LPC multiplexed address, command and data bus	I/O 3.3VSB		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3VSB		
~~LPC_DRQ0#~~ ~~LPC_DRQ1#~~	~~B8~~ ~~B9~~	~~LPC serial DMA request~~	~~I 3.3V~~		Not supported
LPC_SERIRQ	A50	LPC serial interrupt	I/O 3.3VSB	PU 8.2K 3.3VSB	
LPC_CLK	B10	LPC clock output –33MHz nominal	O 3.3VSB		The LPC_CLK frequency is 24MHz on this platform

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4.3.6 USB

Name	Pin #	Description	I/O	PU / PD	Comment
USB0+ USB0-	A46 A45	USB differential data pairs for Port 0	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB1+ USB1-	B46 B45	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB2+ USB2-	A43 A42	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB3+ USB3-	B43 B42	USB differential data pairs for Port 2	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1 (see *Note)	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on carrier
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3 (see *Note)	I 3.3VSB	PU 10K 3.3VSB	Do not pull high on carrier
~~USB0_HOST_PRSNT~~	~~B48~~	~~Module USB client may detect the presence of a USB host on USB0. A high value indicates that a host is present.~~	~~I 3.3VSB~~		Not supported

***Note**: A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.

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4.3.7 SPI Bus (BIOS only)

Name	Pin #	Description	I/O	PU / PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3VSB	PU 10K 3.3VSB	
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier	O P 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I	PU 10K 3.3VSB	Carrier shall pull to GND or leave not connected.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I	PU 10K 3.3VSB	Carrier shall pull to GND or leave not connected

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4.3.8 Miscellaneous

Name	Pin #	Description	I/O	PU / PD	Comment
SPKR	B32	Output for audio enunciator, the "speaker" in PC-AT systems	O 3.3V	PU 10K 3.3V	
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V		
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3VSB		
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3VSB	PU 10K 3.3VSB	
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD 3.3V		There shall be PD on carrier board
FAN_TACHIN	B102	Fan tachometer input for a fan with a two-pulse output.	I OD 3.3V	PU 47K 3.3V	
~~TPM_PP~~	~~A96~~	~~Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.~~	~~I 3.3V~~	~~PD 100K~~	~~PD only when TPM on module. Modules implementing a TPM shall pull down~~ Not Supported

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4.3.9 SMBus

Name	Pin #	Description	I/O	PU / PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line. Power sourced through 3.3V standby rail and main power rails.	I/O OD 3.3VSB	PU 2.2K 3.3VSB	Equivalent resistor is 2.2K
SMB_DAT#	B14	System Management Bus bidirectional data line. Power sourced through 3.3V standby rail and main power rails.	I/O OD 3.3VSB	PU 2.2K 3.3VSB	Equivalent resistor is 2.2K
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 3.3V standby rail and main power rails.	I 3.3VSB	PU 10K 3.3VSB	

Note: SMBus source from SoC's SMBus is default setting. SMBus source from EC is by build option supported by project basis.

4.3.10 I2C Bus

Name	Pin #	Description	I/O	PU / PD	Comment
I2C_CK	B33	General purpose I^2C port clock output/input	I/O OD 3.3VSB	PU 2.2K 3.3VSB	
I2C_DAT	B34	General purpose I^2C port data I/O line	I/O OD 3.3VSB	PU 2.2K 3.3VSB	

Note: I2C source from EC is default setting. I2C source from SoC's I2C is by build option supported by project basis.

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4.3.11 General Purpose I/O (GPIO)

Name	Pin #	Description	I/O	PU / PD	Comment
GPO[0]	A93	General purpose output pins.	O 3.3V	PD 10K 3.3V	After hardware RESET output low
GPO[1]	B54	General purpose output pins.	O 3.3V	PD 10K 3.3V	After hardware RESET output low
GPO[2]	B57	General purpose output pins.	O 3.3V	PD 10K 3.3V	After hardware RESET output low
GPO[3]	B63	General purpose output pins.	O 3.3V	PD 10K 3.3V	After hardware RESET output low
GPI[0]	A54	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[1]	A63	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[2]	A67	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	
GPI[3]	A85	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10K 3.3V	

Note: GPI/GPO source from EC is default setting. GPI/GPO source from SoC's GPIOs is by build option supported by project basis.

4.3.12 Serial Interface Signals

Name	Pin #	Description	I/O	PU / PD	Comment
SER0_TX	A98	General purpose serial port transmitter	O CMOS 3.3V		Power rail tolerance 5V, 12V There shall be PD on carrier board
SER0_RX	A99	General purpose serial port receiver	I CMOS 3.3V	PU 10K 3.3V	Power rail tolerance 5V, 12V
SER1_TX	A101	General purpose serial port transmitter	O CMOS 3.3V		Power rail tolerance 5V, 12V There shall be PD on carrier board
SER1_RX	A102	General purpose serial port receiver	I CMOS 3.3V	PU 10K 3.3V	Power rail tolerance 5V, 12V

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Note: SER0, SER1 source from EC is default setting. SER0, SER1 source from SoC's HSUART is by build option by supported by project basis. HSUART has driver support limitation.

4.3.13 IPMB (Optional)

Name	Pin #	Description	I/O	PU / PD	Comment
IPMB_CLK	A32	Clock I/O line for the multi-master IPMB port. If the IPMB interface is used, an additional lower value pull-up is located on the Carrier.	I/O OD 3.3VSB	PU 47K 3.3VSB	
IPMB_DAT	A33	Data I/O line for the multi-master IPMB port. If the IPMB interface is used, an additional lower value pull-up is located on the Carrier.	I/O OD 3.3VSB	PU 47K 3.3VSB	

Note: IPMB via a Module MMC is supported by project basis and it is still in development (TBC)

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4.3.14

4.3.14 Power and System Management

Name	Pin #	Description	I/O	PU / PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge.	I 3.3VSB	PU 10K 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low request for module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.	I 3.3VSB	PU 10K 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V	PU 10K 3.3V	
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow carrier-based FPGAs or other configurable devices time to be programmed.	I 3.3VSB	PU 10K 3.3VSB	Should have weak pull up.
~~SUS_STAT#~~	~~B18~~	~~Indicates imminent suspend operation; used to notify LPC devices.~~	~~O 3.3VSB~~		Not supported
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as "PS_ON") may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB		
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		Connect to SUS_S4#
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 10K 3.3VSB	
WAKE1#	B67	General purpose wake-up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 10K 3.3VSB	Connect to WAKE 0#
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low or may be used to signal some other external power-management event.	I 3.3VSB	PU 10K 3.3VSB	
LID#	A103	LID button. Low active signal used by the ACPI operating system for a LID switch.	I OD 3.3VSB		
SLEEP#	B103	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I OD 3.3VSB		

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~~RAPID_ SHUTDOWN~~	~~C67~~	~~Trigger for Rapid Shutdown. Must be driven to 5V though a <=50-ohm source impedance for ≥ 20 µs.~~	~~I CMOS 5VSB~~		Not supported
RSMRST_OUT	A48	USB devices that are to be powered in the S5 / S4 / S3 Suspend states should not have their 5V VBUS power enabled before RSMRST_OUT# transitions to the hi state.	O CMOS 3.3VSB		

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4.3.15 Power and Ground

Name	Pin #	Description	I/O	PU / PD	Comment
VCC_12V	A104, A105, A106, A107, A108, A109, B104, B105, B106, B107, B109	Primary power input supports wide range 5 – 20V input. All available VCC_12V pins on the connector(s) shall be used.	P		8.5-20V
VCC_5V_SBY	B84, B85, B86, B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		5Vsb ±5%
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A38, A41, A51, A57, A60, A66, A70, A73, A76, A79, A80, A83, A87, A90, A100, A110, B1, B11, B21, B28, B31, B38, B41, B51, B60, B70, B73, B76, B79, B80, B83, B90, B100, B110	Ground - DC power and signal and AC signal return path.	P		

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4.4. CD Connector Signal Descriptions

4.4.1 USB 3.0 Extensions

Name	Pin #	Description	I/O	PU / PD	Comment
USB_SSRX0- USB_SSRX0+	C3 C4	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB0	I PCIE		AC coupled off module
USB_SSTX0- USB_SSTX0+	D3 D4	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB0	O PCIE		AC coupled on module
USB_SSRX1- USB_SSRX1+	C6 C7	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB1	I PCIE		AC coupled off module
USB_SSTX1- USB_SSTX1+	D6 D7	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB1	O PCIE		AC coupled on module
USB_SSRX2- USB_SSRX2+	C9 C10	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB2	I PCIE		AC coupled off module
USB_SSTX2- USB_SSTX2+	D9 D10	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB2	O PCIE		AC coupled on module
USB_SSRX3- USB_SSRX3+	C12 C13	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB3	I PCIE		AC coupled off module
USB_SSTX3- USB_SSTX3+	D12 D13	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB3	O PCIE		AC coupled on module

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4.4.2 PCI Express

Name	Pin #	Description	I/O	PU / PD	Comment
~~PCIE_TX6+~~ ~~PCIE_TX6-~~	~~D19~~ ~~D20~~	~~PCI Express channel 6, Transmit Output differential pair.~~	~~O PCIE~~		Not supported
~~PCIE_RX6+~~ ~~PCIE_RX6-~~	~~C19~~ ~~C20~~	~~PCI Express channel 6, Receive Input differential pair.~~	~~I PCIE~~		Not supported
~~PCIE_TX7+~~ ~~PCIE_TX7-~~	~~D22~~ ~~D23~~	~~PCI Express channel 7, Transmit Output differential pair.~~	~~O PCIE~~		Not supported
~~PCIE_RX7+~~ ~~PCIE_RX7-~~	~~C22~~ ~~C23~~	~~PCI Express channel 7, Receive Input differential pair.~~	~~I PCIE~~		Not supported

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4.4.3 10G-KR Ethernet

Name	Pin #	Description	I/O	PU / PD	Comment
10G_KR_RX0+ 10G_KR_RX0- 10G_KR_RX1+ 10G_KR_RX1-	C49 C50 C42 C43	10GBASE-KR ports, Receive Input differential pairs	I KR		AC coupled on Module
10G_KR_TX0+ 10G_KR_TX0- 10G_KR_TX1+ 10G_KR_TX1-	D49 D50 D42 D43	10GBASE-KR ports, Transmit Output differential pairs	O KR		AC coupled on Carrier
~~10G_KR_RX2+~~ ~~10G_KR_RX2-~~ ~~10G_KR_RX3+~~ ~~10G_KR_RX3-~~	~~C29~~ ~~C30~~ ~~C26~~ ~~C27~~	~~10GBASE-KR ports, Receive Input differential pairs~~	~~I KR~~		Not supported
~~10G_KR_TX2+~~ ~~10G_KR_TX2-~~ ~~10G_KR_TX3+~~ ~~10G_KR_TX3-~~	~~D29~~ ~~D30~~ ~~D26~~ ~~D27~~	~~10GBASE-KR ports, Transmit Output differential pairs~~	~~O KR~~		Not supported
CEI_INT#	C47	Active low interrupt input to Module from Carrier based I2C I/O expander	I 3.3VSB	PU 10K 3.3VSB	
CEI_MDIO	D46	MDIO data – for PHY setup	I/O 3.3VSB	PU 1K 3.3VSB	TBD, it will be fine tune during development stage
CEI_MDC	C46	MDIO clock - for PHY setup	O 3.3VSB	PU 1K 3.3VSB	TBD, it will be fine tune during development stage
10G_SDP0 10G_SDP1 10G_SDP2 10G_SDP3	C40 D40 C17 D17	Software-Definable Pins	I/O 3.3VSB		

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Name	Pin #	Description	I/O	PU / PD	Comment
CEI_SDA	C39	I2C data – for SFP setup, serialized status LEDs and miscellaneous serialized signals	I/O OD 3.3VSB	PU 10K 3.3VSB	TBD, it will be fine tune during development stage
CEI_SCL	D39	I2C clock for CEI I2C port	O OD 3.3VSB	PU 10K 3.3VSB	TBD, it will be fine tune during development stage
CEI_RST#	C35	Active low reset output from Module to Carrier based I/O expander	O 3.3VSB	PD 10K	
~~CEI_PRSNT#~~	~~D35~~	~~Input signal from Carrier indicating presence of CEI compliant hardware on the Carrier~~	~~I 3.3VSB~~		Not supported
ETH_PHY_INT#	D47	Second active low interrupt input to Module from Carrier based I2C I/O expander	I 3.3VSB	PU 2K 3.3VSB	

Several RSVD10G pins listed on pin-out summary table should be left not connected

Note: Please contact our local ADLINK representative for information below. (1) Detailed information about circuit design between the Ethernet controller, Optical Fiber/Copper PHY and firmware. (2) Additional MDC/MDIO is offered for specific use case based on 10GBASE-T, by project basis. (3) SGMII offering for specific use case and by project basis. (4) 10G_SDP support is by project basis.

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4.4.4 PCI Express

Name	Pin #	Description	I/O	PU / PD	Comment
PCIE_TX16+ PCIE_TX16-	D52 D53	PCI Express channel 16, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX16+ PCIE_RX16-	C52 C53	PCI Express channel 16, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX17+ PCIE_TX17-	D55 D56	PCI Express channel 17, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX17+ PCIE_RX17-	C55 C56	PCI Express channel 17, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX18+ PCIE_TX18-	D58 D59	PCI Express channel 18, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX18+ PCIE_RX18-	C58 C59	PCI Express channel 18, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX19+ PCIE_TX19-	D61 D62	PCI Express channel 19, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX19+ PCIE_RX19-	C61 C62	PCI Express channel 19, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX20+ PCIE_TX20-	D65 D66	PCI Express channel 20, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX20+ PCIE_RX20-	C65 C66	PCI Express channel 20, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX21+ PCIE_TX21-	D68 D69	PCI Express channel 21, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX21+ PCIE_RX21-	C68 C69	PCI Express channel 21, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX22+ PCIE_TX22-	D71 D72	PCI Express channel 22, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX22+ PCIE_RX22-	C71 C72	PCI Express channel 22, Receive Input differential pair.	I PCIE		AC coupled off Module
PCIE_TX23+ PCIE_TX23-	D74 D75	PCI Express channel 23, Transmit Output differential pair.	O PCIE		AC coupled on Module
PCIE_RX23+ PCIE_RX23-	C74 C75	PCI Express channel 23, Receive Input differential pair.	I PCIE		AC coupled off Module

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~~PCIE_TX24+ PCIE_TX24-~~	~~D78 D79~~	~~PCI Express channel 24, Transmit Output differential pair.~~	~~O PCIE~~		Not supported
~~PCIE_RX24+ PCIE_RX24-~~	~~C78 C79~~	~~PCI Express channel 24, Receive Input differential pair.~~	~~I PCIE~~		Not supported
~~PCIE_TX25+ PCIE_TX25-~~	~~D81 D82~~	~~PCI Express channel 25, Transmit Output differential pair.~~	~~O PCIE~~		Not supported
~~PCIE_RX25+ PCIE_RX25-~~	~~C81 C82~~	~~PCI Express channel 25, Receive Input differential pair.~~	~~I PCIE~~		Not supported
~~PCIE_TX26+ PCIE_TX26-~~	~~D85 D86~~	~~PCI Express channel 26, Transmit Output differential pair.~~	~~O PCIE~~		Not supported
~~PCIE_RX26+ PCIE_RX26-~~	~~C85 C86~~	~~PCI Express channel 26, Receive Input differential pair.~~	~~I PCIE~~		Not supported
~~PCIE_TX27+ PCIE_TX27-~~	~~D88 D89~~	~~PCI Express channel 27, Transmit Output differential pair.~~	~~O PCIE~~		Not supported
~~PCIE_RX27+ PCIE_RX27-~~	~~C88 C89~~	~~PCI Express channel 27, Receive Input differential pair.~~	~~I PCIE~~		Not supported
~~PCIE_TX28+ PCIE_TX28-~~	~~D91 D92~~	~~PCI Express channel 28, Transmit Output differential pair.~~	~~O PCIE~~		Not supported
~~PCIE_RX28+ PCIE_RX28-~~	~~C91 C92~~	~~PCI Express channel 28, Receive Input differential pair.~~	~~I PCIE~~		Not supported
~~PCIE_TX29+ PCIE_TX29-~~	~~D94 D95~~	~~PCI Express channel 29, Transmit Output differential pair.~~	~~O PCIE~~		Not supported
~~PCIE_RX29+ PCIE_RX29-~~	~~C94 C95~~	~~PCI Express channel 29, Receive Input differential pair.~~	~~I PCIE~~		Not supported
~~PCIE_TX30+ PCIE_TX30-~~	~~D98 D99~~	~~PCI Express channel 30, Transmit Output differential pair.~~	~~O PCIE~~		Not supported
~~PCIE_RX30+ PCIE_RX30-~~	~~C98 C99~~	~~PCI Express channel 30, Receive Input differential pair.~~	~~I PCIE~~		Not supported
~~PCIE_TX31+ PCIE_TX31-~~	~~D101 D102~~	~~PCI Express channel 31, Transmit Output differential pair.~~	~~O PCIE~~		Not supported
~~PCIE_RX31+ PCIE_RX31-~~	~~C101 C102~~	~~PCI Express channel 31, Receive Input differential pair.~~	~~I PCIE~~		Not supported

Note: Both of PCIE_CLK_REF1 and PCIE_CLK_REF can be used for PCIe lane 16-23 but PCIE_CLK_REF1 preferred.

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4.4.4.1. I/O Assignments

Please refer to 4.3.4.1

4.4.5 GP_SPI

Name	Pin #	Description	I/O	PU / PD	Comment
GP_SPI_CS#	D36	Chip select from Module SPI Master to Carrier SPI Slave	O 3.3VSB		
GP_SPI_MISO	D34	Data in to Module SPI Master from Carrier SPI Slave "Master In Slave Out"	I 3.3VSB		
GP_SPI_MOSI	D33	Data out from Module SPI Master to Carrier SPI Slave "Master Out Slave In"	O 3.3VSB		
GP_SPI_CLK	D32	Clock from Module SPI Master to Carrier SPI Slave	O 3.3VSB		

Note: GP_SPI supported by project basis

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4.4.6

4.4.6 Module Type Definition

Name	Pin #	Description	I/O	PU / PD	Comment
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module. The pins are tied on the Module to either ground (GND) or are no-connects (NC). For Pin-out Type 1 and Type 10 that lack a CD connector, these pins are not present (X) **TYPE2# TYPE1# TYPE0#** X X X Pinout Type 1 X X X Pinout Type 10 NC NC NC Pinout Type 2 NC NC GND Pinout Type 3 NC GND NC Pinout Type 4 NC GND GND Pinout Type 5 GND NC NC Pinout Type 6 GND NC GND Pinout Type 7 The Carrier Board ***should*** implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.			Type 7
TYPE10#	A97	In case of a type 10 module this pin signal is tied to GND through a 47K resistor on the module.			No PD

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4.4.7 Power and Ground

Name	Pin #	Description	I/O	PU / PD	Comment
VCC_12V	C104, C105, C106, C107, C108, C109, D104, D105, D106, D107, D108, D109	Primary power input supports wide range 5~ 20V input. All available VCC_12V pins on the connector(s) shall be used.	P		8.5-20V
GND	C1, C2, C5, C8, C11, C14, C18, C21, C25, C28, C31, C41, C44, C48, C51, C60, C63, C64, C70, C73, C76, C77, C80, C83, C84, C87, C90, C93, C96, C97, C100, C103, C110, D1, D2, D5, D8, D11, D14, D18, D21, D25, D28, D31, D41, D44, D48, D51, D54, D60, D63, D64, D67, D70, D73, D76, D77, D80, D83, D84, D87, D90, D93, D96, D97, D100, D103, D110	Ground - DC power and signal and AC signal return path.	P		

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5. Additional Features

This chapter describes connectors, LEDs, switches and additional items located on the module and not necessarily included in the PICMG standard specification. The locations of these items are shown below:

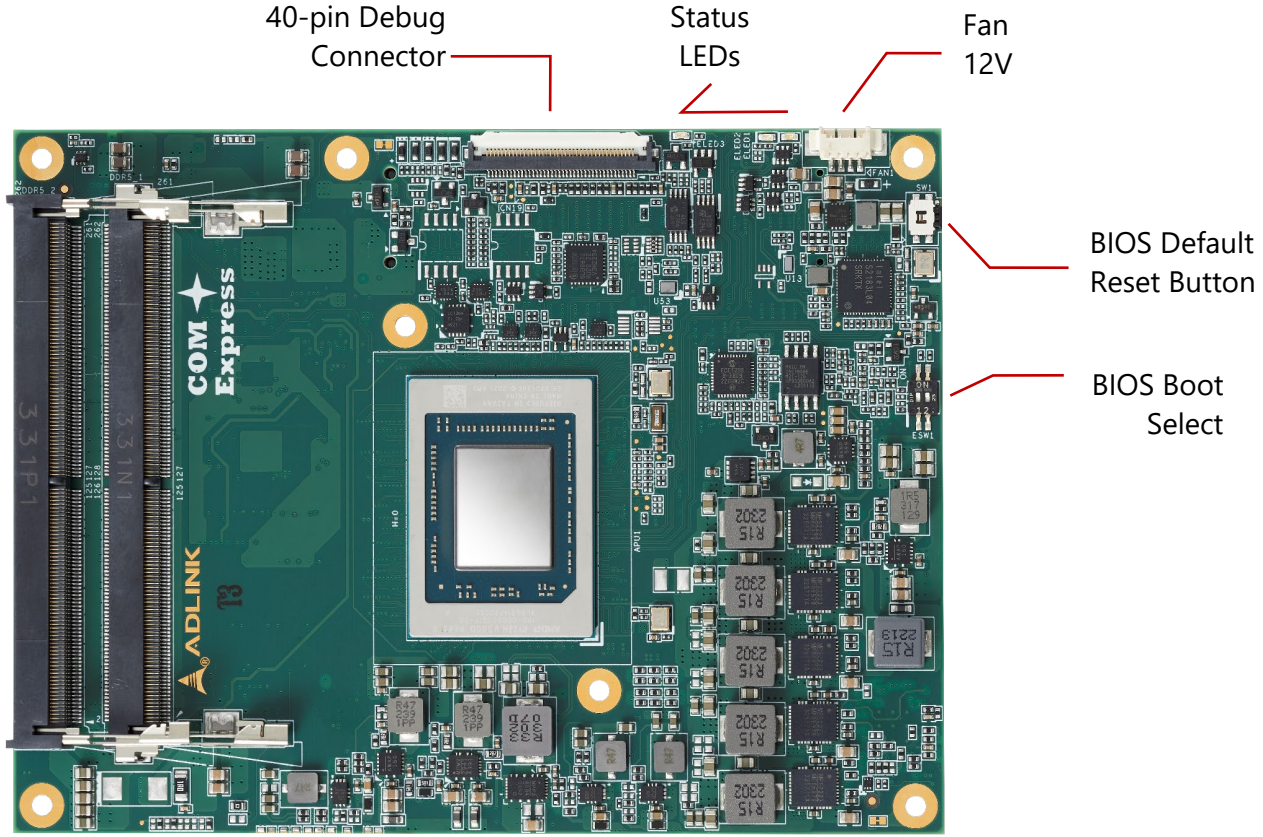


Figure 3 – Module feature locations

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5.1. Debug Connector

This connector is particular useful during carrier design and bring up phase. It offers access to the following critical parts of the module:

- Test points measurement of internal power rails
- I2C bus for BIOS POST code readout
- SPI BIOS programming interface
- Embedded Controller programming interface

The debug board for Express-VR7 usage is DB40-HPC

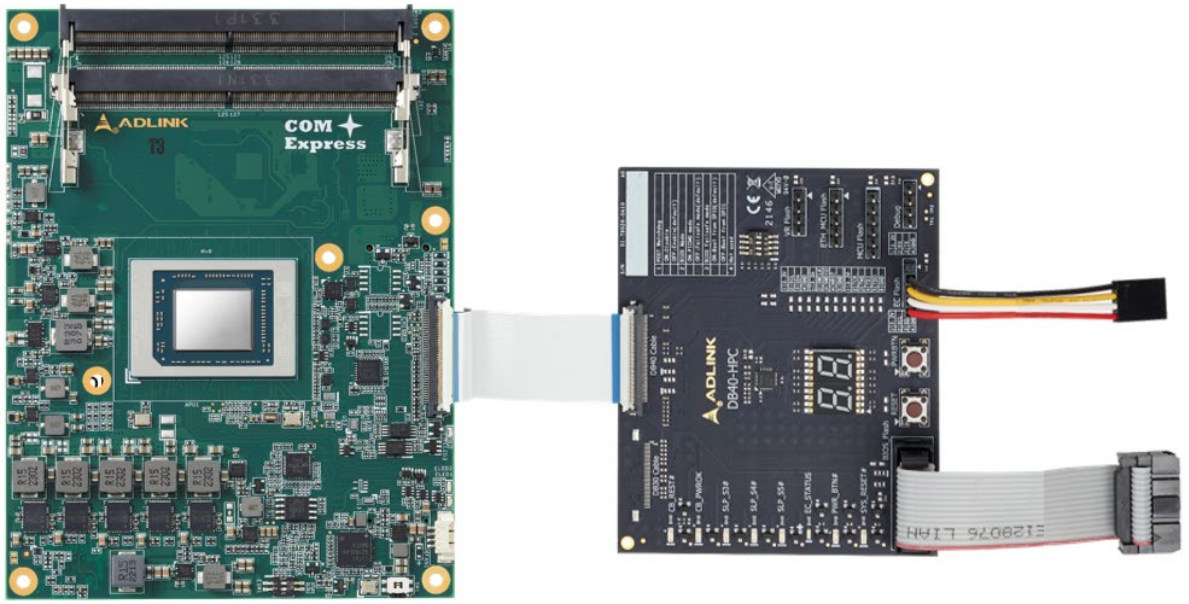
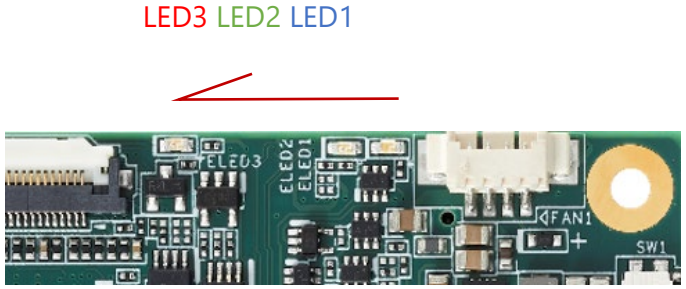


Figure 4 – Express-VR7 and Debug Module

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5.2. Status LEDs

Status LED's are mounted on the module to facilitate easier maintenance.



Name	Color	Connection	Function
LED1	Blue	BMC output	Power Sequence Status Code (BMC) Power Changes, RESET (see Exception Codes below)
LED2	Green	Power Source 3Vcc	S0 LED ON S3/S4/S5 LED OFF ECO mode LED OFF
LED3	Red	BMC output and same signal as WDT (B27) on BtB connector	Module power up WD LED = LED OFF Watchdog counting WD LED = Keep Last State Watchdog timed out WD LED = LED ON Watchdog RESET WD LED = LED ON Rebooted after WD RESET WD LED = LED ON Rebooted after PWRBTN WD LED = LED OFF Rebooted after RESET BTN WD LED = LED OFF Note: Only a RESET not initiated by the BMC can clear the WD LED (user action)

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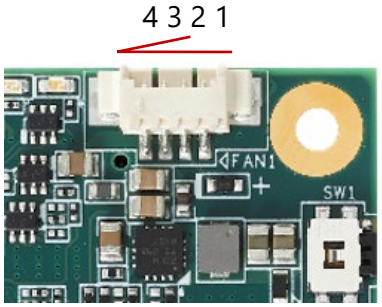
5.3. Exception Codes

Exception Code	Error Message
0	NOERROR
3	NO_SLP_S5
4	NO_SLP_S4
5	NO_SLP_S3
6	BIOS_FAIL
7	RESET_FAIL
9	NO_CB_PWROK
10	CRITICAL_TEMP
11	POWER_FAIL
12	VOLTAGE_FAIL
13	RSMRST_FAIL
14	NO_VDDQ_PG
16	NO_VCORE_PG
17	NO_SYS_GD
19	NO_V3P3A
21	NO_PWRSRC_GD

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5.4. Fan Connector

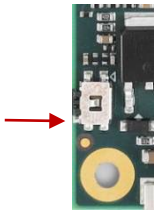
Connector type: JVE 24W1125A-04M00



Name	Description
1	FAN_PWMOUT
2	FAN_TACHIN
3	GND
4	12V

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5.5. BIOS Default Reset Button



To perform a hardware reset of BIOS default settings, perform the following steps:

1. Shut down the system.
2. Keep the BIOS Setup Defaults Reset Button pressed and boot up the system. You can release the button when the BIOS prompt screen appears
3. The BIOS prompt screen will display a confirmation that BIOS defaults have been reset and request that you reboot the system.



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5.6. BIOS Boot Select

The module has two BIOS chips (BOM option) and BIOS operation can be configured to "PICMG" and dual-BIOS "Failsafe" modes using BIOS Select and Mode Configuration Switch, Pin 2.

Setting the module to PICMG mode will configure the BIOS chips on the module as SPI0 and SPI1. In PICMG mode, a BIOS chip cannot be placed in the SPI0 slot on the carrier.

In dual-BIOS Failsafe mode, both BIOS chips on the module are configured as SPI1. Only one of the two is connected to the SPI bus at any given time. In case of failure of the primary SPI1 BIOS, the system will reboot and switch to the secondary SPI1 BIOS on the module. In Failsafe mode, the SPI0 BIOS socket on the carrier can be populated.

In either mode, BIOS Select and Mode Configuration Switch Pin 1 is used to select whether to boot from SPI0 or SPI1.

Mode	Pin 1	Pin 2
Boot from SPI0 (default)	On	-
Boot from SPI1	Off	-
Set BIOS to PICMG mode (default)	-	On
Set BIOS to Failsafe BIOS mode	-	Off

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6. BIOS Checkpoints, Beep Codes

A status code is a data value used to provide diagnostic information about the boot process. Progress codes are status codes that signify successful progression to a following initialization step. Error codes signify error conditions encountered in the process of system initialization. The Aptio 5.x core can be configured to send status codes to a variety of sources. The two most commonly used types of status codes are checkpoint codes and beep codes. Checkpoint codes are byte length data values. Checkpoints are typically output to I/O port 80h, but the Aptio 5.x core can be configured to send checkpoints to a variety of sources. The Aptio 5.x core outputs checkpoints throughout the boot process to indicate the task the system is currently executing. Checkpoints are very useful in aiding software developers or technicians in debugging problems that occur during the pre-boot process on production hardware. A beep code is a series of short sound signals. Beep codes are typically error codes that do not occur during normal boot process.

Note: Beep codes are not the only sounds generated during the boot process. Some firmware components may use sounds to notify the user about other events such as detection of a hot-pluggable device. These sounds are typically generated using a frequency that is different from the frequency of the beep codes

Viewing Checkpoints

Checkpoints generated by the Aptio firmware can be viewed using a PCI checkpoint card, also referred to as a "POST Card" or "POST Diagnostic Card". These PCI add-on cards show the value of I/O port 80h on an LED display.

Aptio V Checkpoint and Beep Codes

Download the Aptio V Checkpoint and Beep Codes from the AMI website at: www.ami.com/download/aptio-v-checkpoint-and-beep-codes

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7. Software Support

7.1. Yocto Linux

https://github.com/ADLINK/meta-adlink-amd

7.2. Ubuntu 20.04.3 LTS

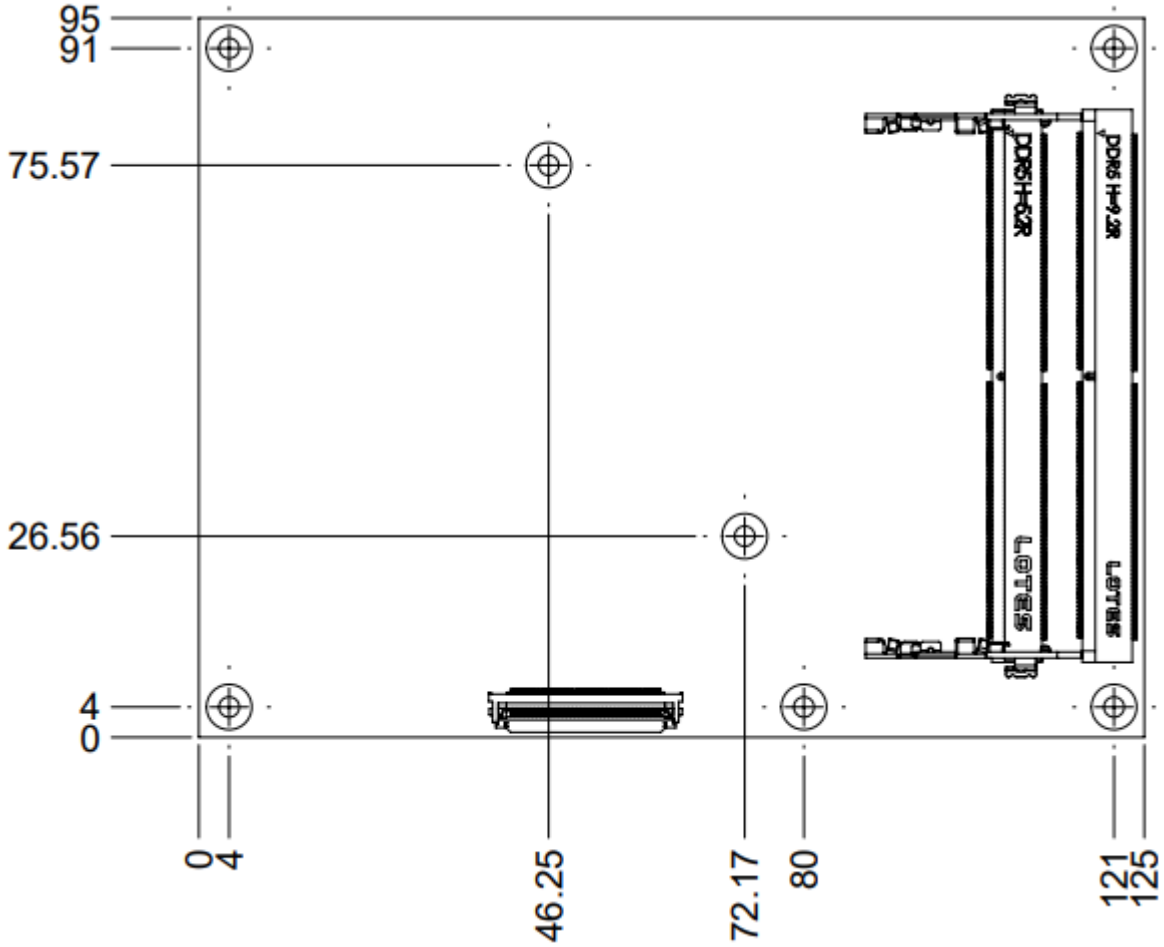
7.3. SEMA API

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8. Mechanical and Thermal

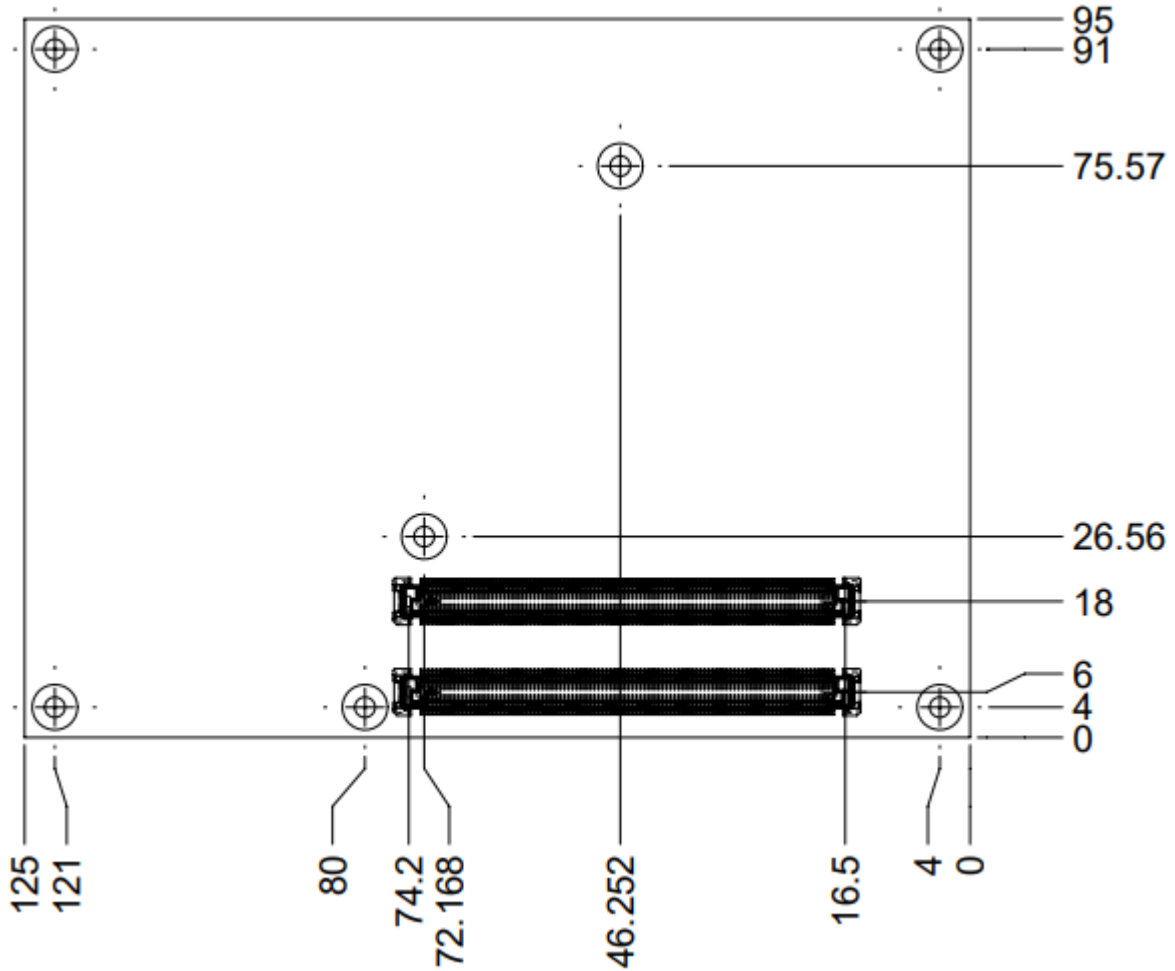
All dimensions are shown in mm with a tolerance of +/- 0.25mm unless otherwise noted.

8.1. Module Dimensions – Top View



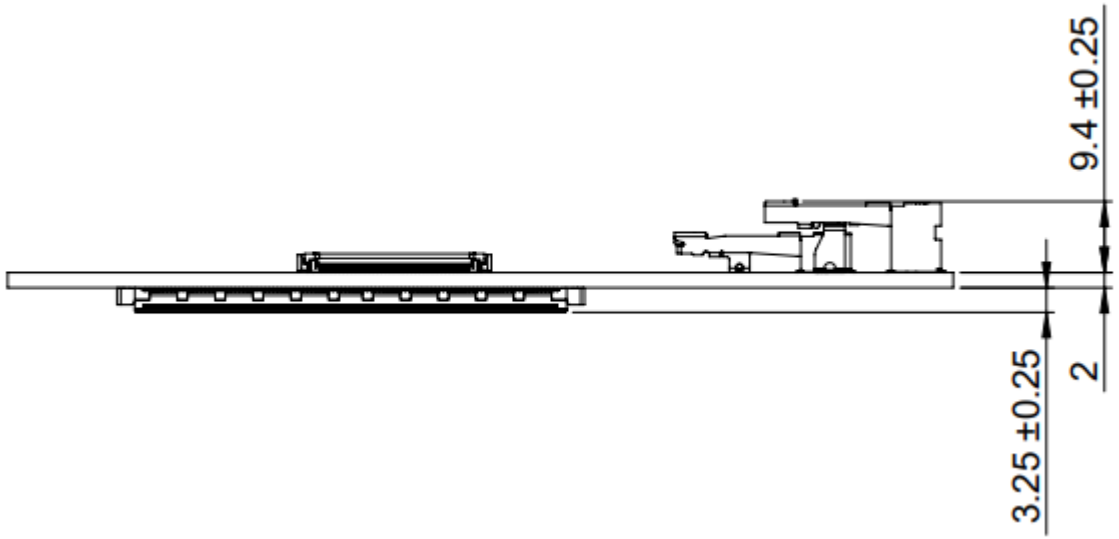
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8.2. Module Dimensions – Bottom View



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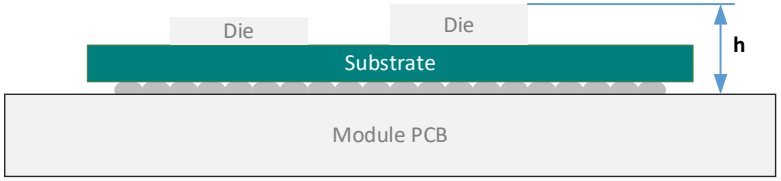
8.3. Module Dimensions – Side View



8.4. Height of Processor and Static Compressive Load

Processor Height Tolerance

The tolerance of the processor height is one of the key factors to consider when designing your thermal solution, as illustrated below. Please contact our ADLINK representative for further details.



	Typical	Tolerance
h	1.28 mm	+/- 0.1mm

Static Compressive Load

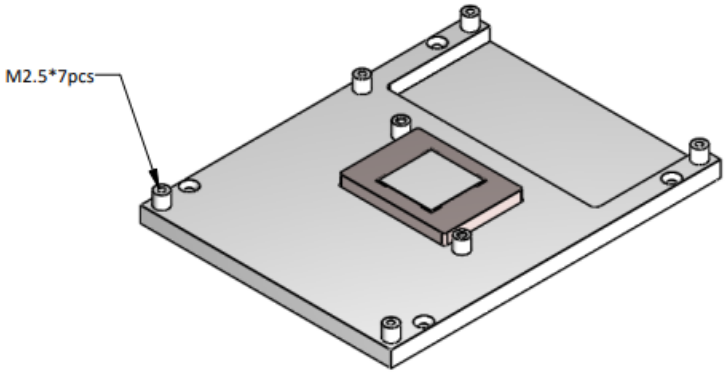
Another key factor to consider is the static compressive load. The Express-VR7 module exhibits a processor maximum pressure die of 40 lbf.

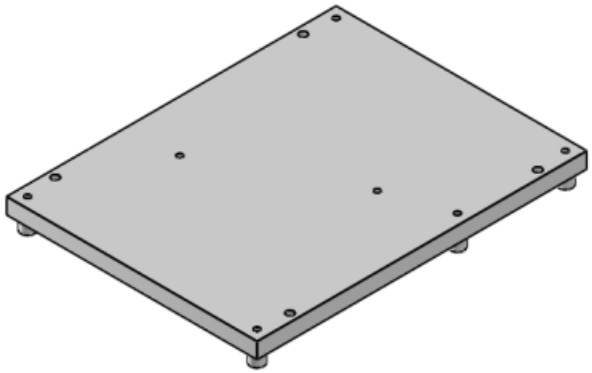
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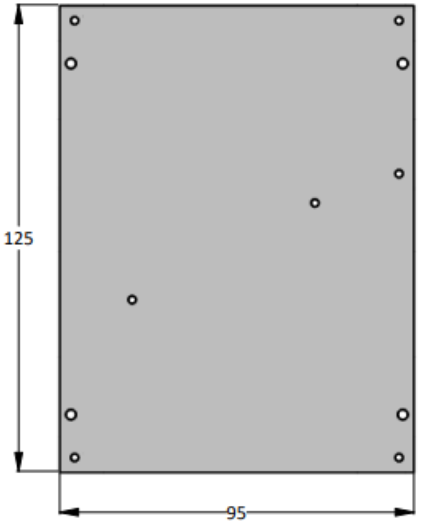
8.5. Thermal Solutions

8.5.1 HTS-B

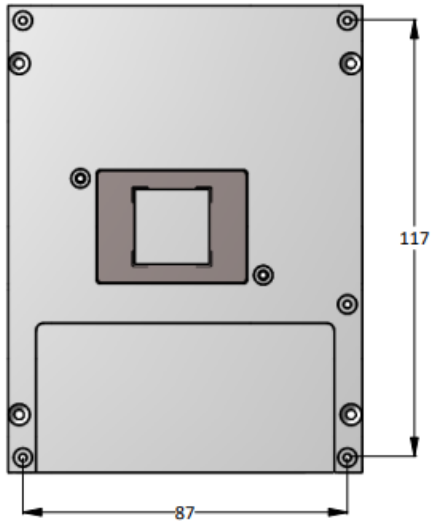






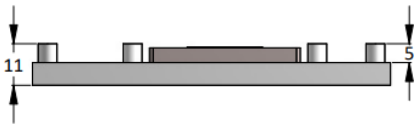


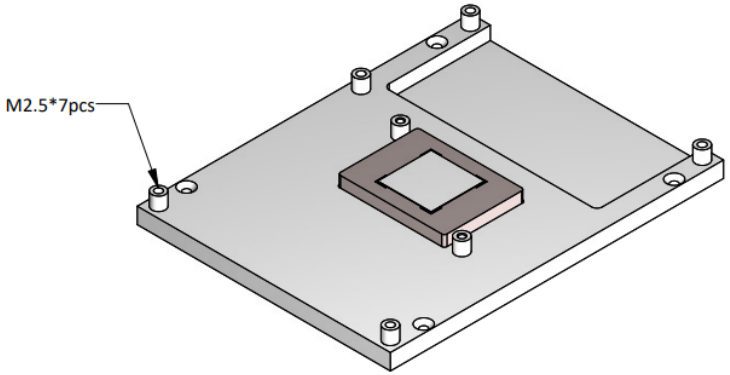


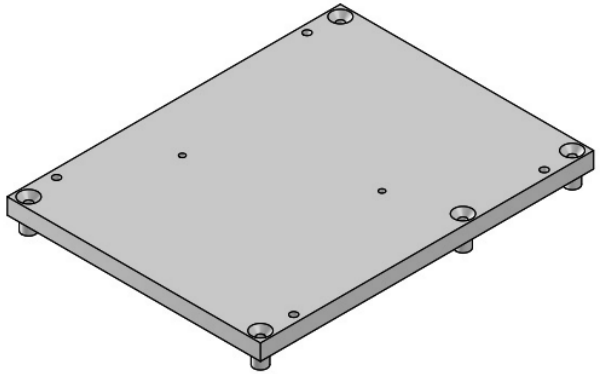


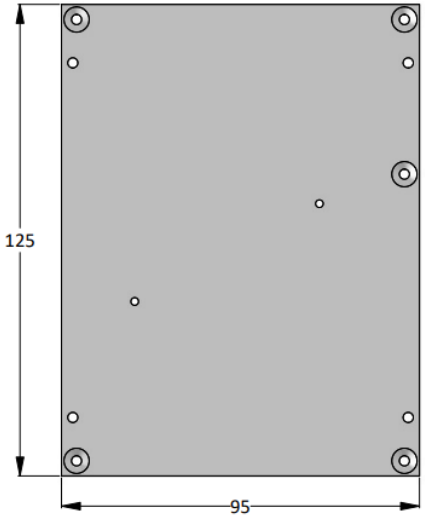
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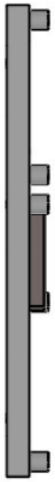
8.5.2 HTS-BT

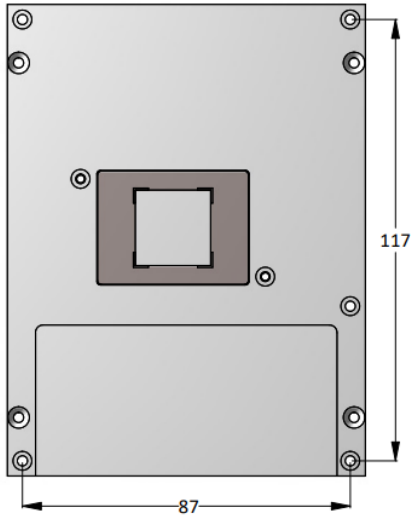






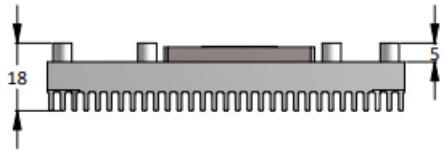


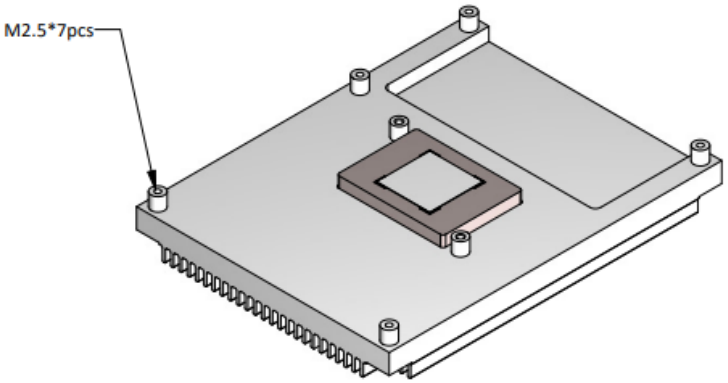


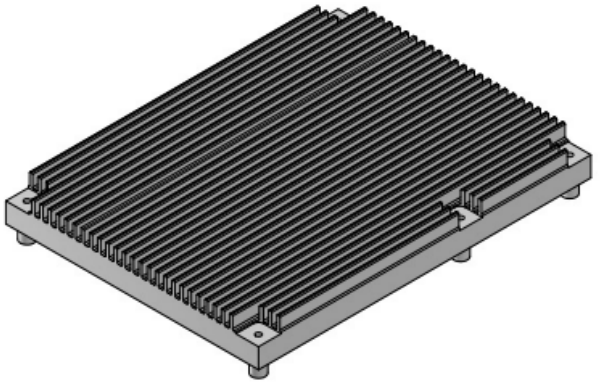


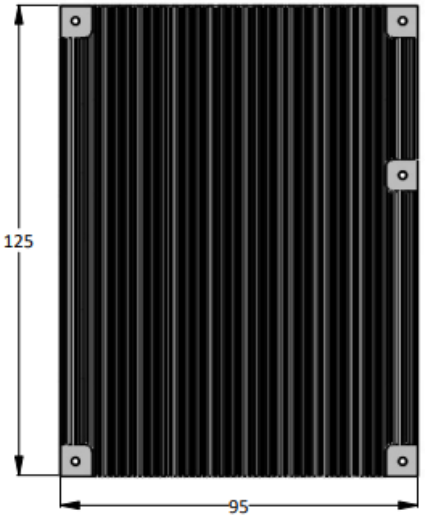
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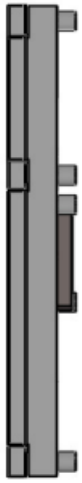
8.5.3 THS-B

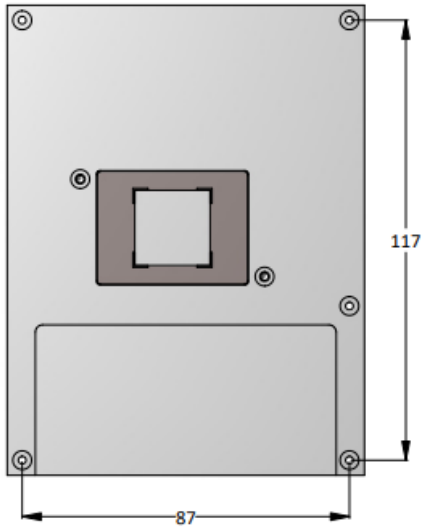






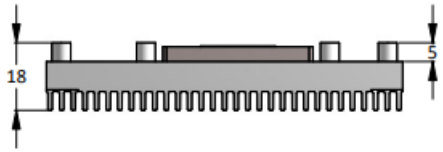


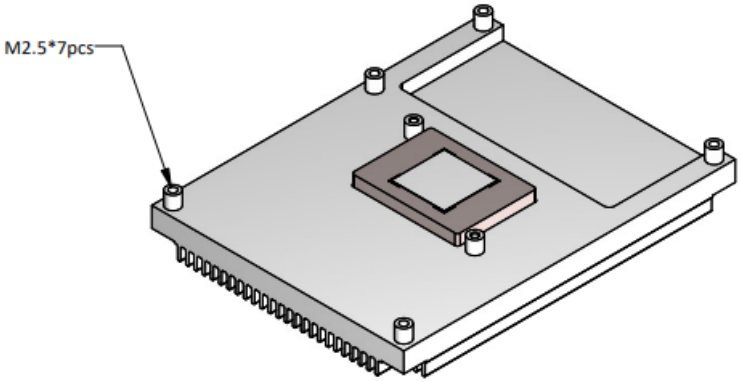


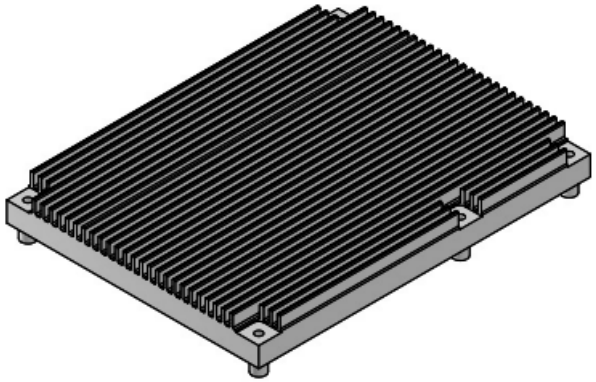


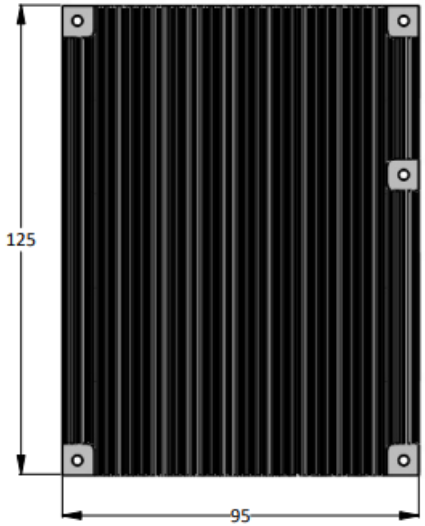
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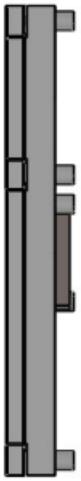
8.5.4 THS-BT

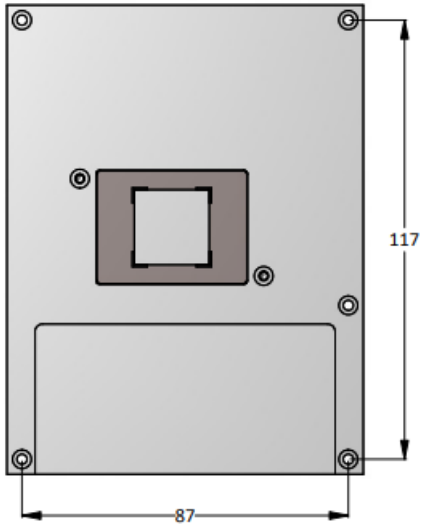






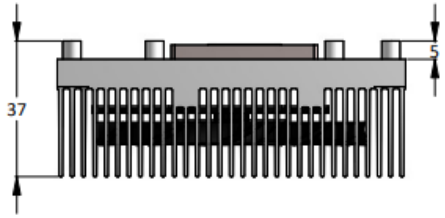


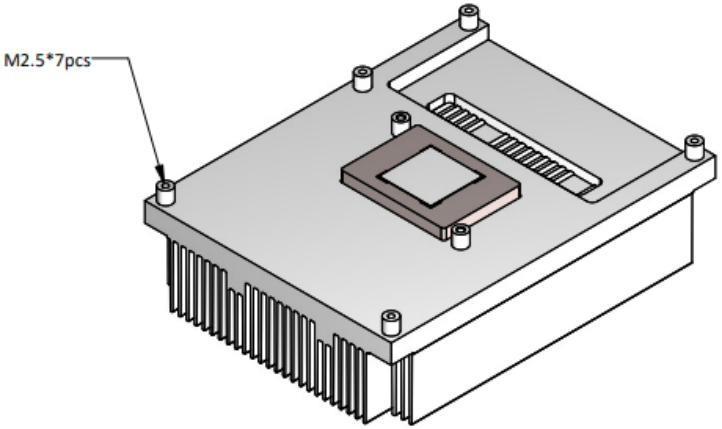


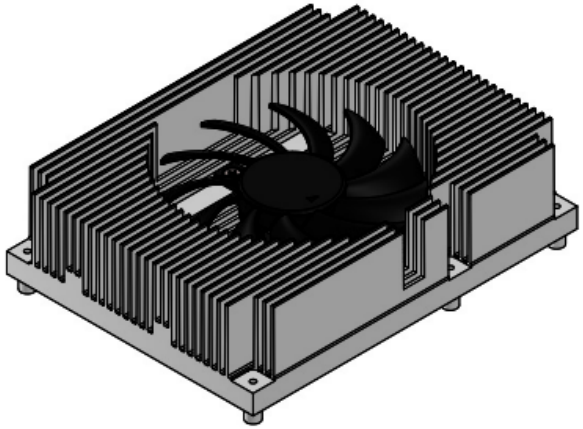


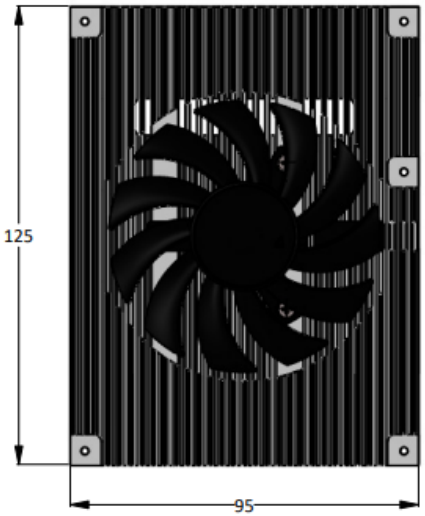
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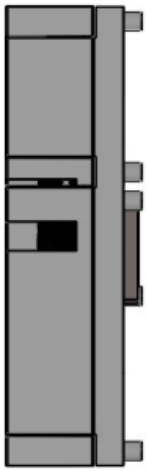
8.5.5 THSF-B

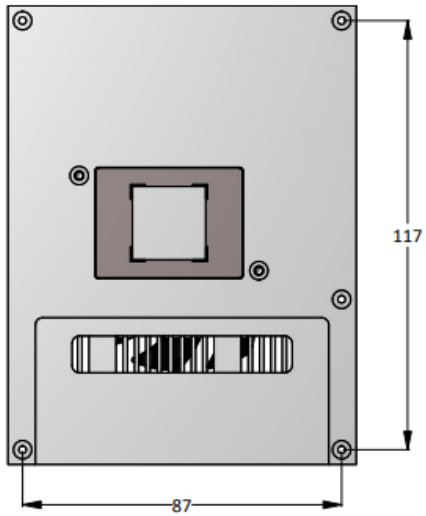






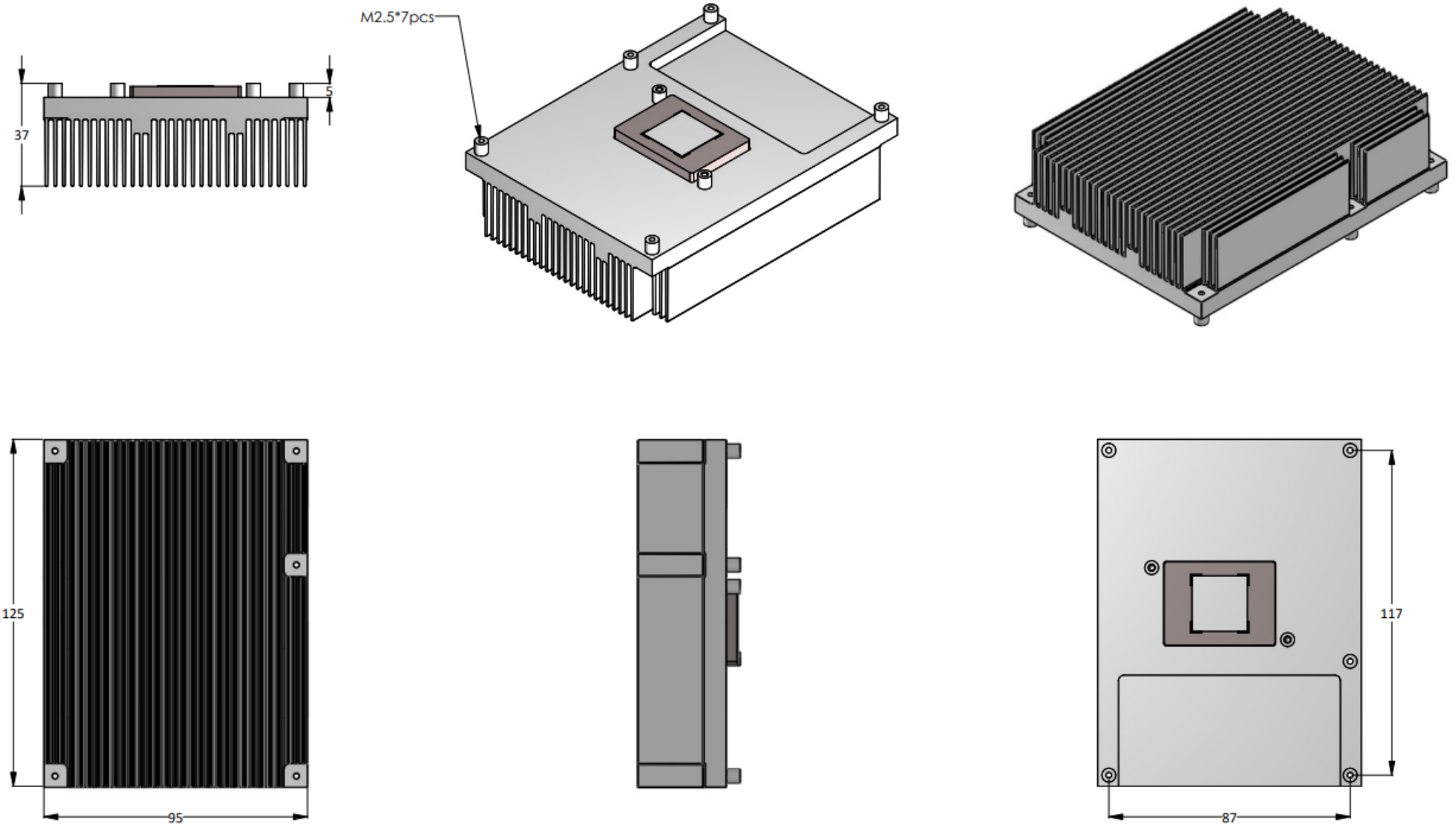






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8.5.6 THSH-B



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8.6. Board to Board Connectors

To allow for different stacking heights, the receptacles for COM Express carrier boards are available in two heights: 5 mm and 8 mm. When 5-mm receptacles are chosen, the carrier board should be free of components.

Tyco 3-1827253-6, Tyco 2357787-1

ept 401-51101-51, ept 401-51103-51

Foxconn QT002206-2141-3H, Foxconn QT5GB26-44703-3H

- 220-pin board-to-board connector with 0.5mm for a stacking height of **5 mm**.
- This connector can be used with 5-mm through-hole standoffs (SMT type).

Tyco 3-6318491-6, Tyco 2357798-1

ept 401-55101-51, ept 401-55103-51

Foxconn QT002206-4141-3H, Foxconn QT5GB26-74703-3H

- 220-pin board-to-board connector with 0.5mm for a stacking height of **8 mm**.
- This connector can be used with 8-mm through-hole standoffs (SMT type).

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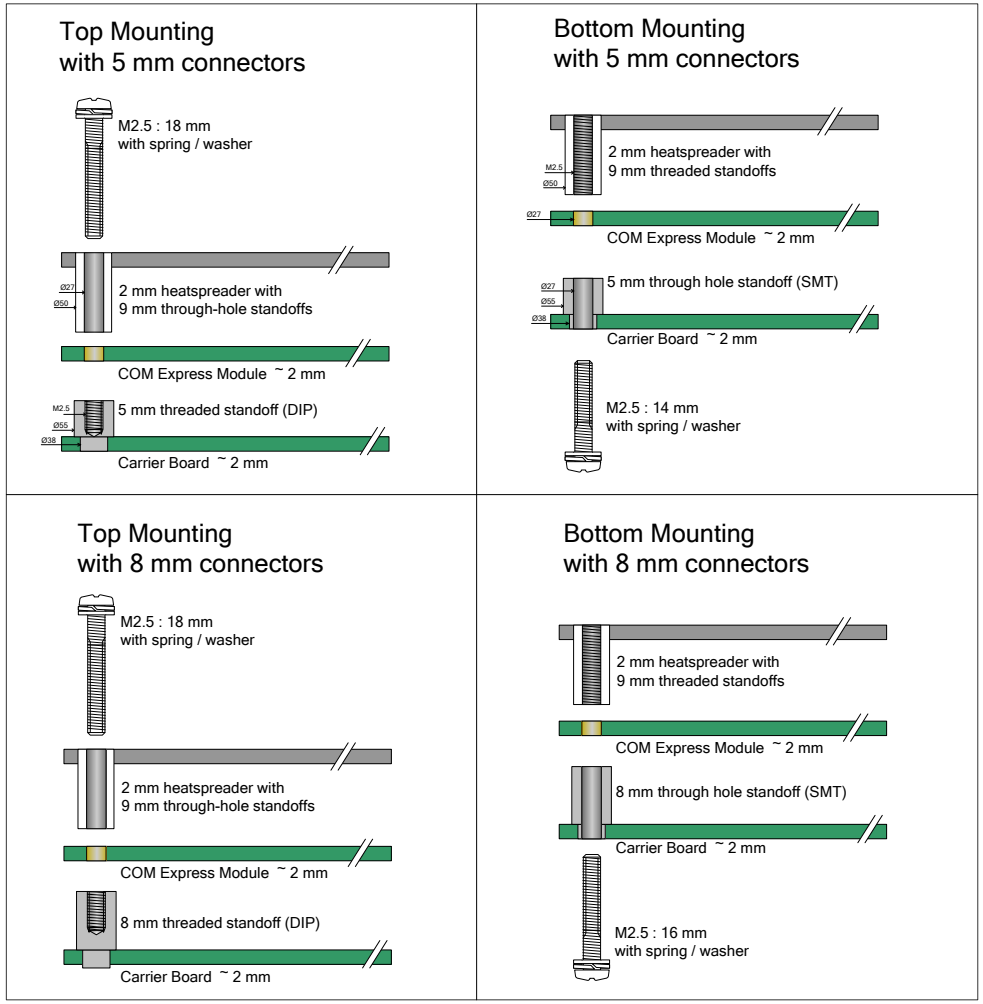
Common Specifications

- Current capacity: 0.5A per pin
- Rated voltage: 50V AC
- Insulation resistance: 100M or greater @ 500 VDC
- Temperature rating: -40°C to 85°C
- UL certification (ECBT2.E28476)
- Copper alloy (contacts)
- Housing: thermo-plastic molded compound (L.C.P.)

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8.7. Mounting Method

There are several standard ways to mount the COM Express module with a thermal solution onto a carrier board. In addition to the 5-mm or 8-mm board-to-board connectors, there are also top and bottom mounting. In top mounting, the threaded standoffs are on the carrier board and the thermal solution is attached with through-hole standoffs. In bottom mounting, the threaded standoffs are on the thermal solution and the carrier board has through-hole standoffs.

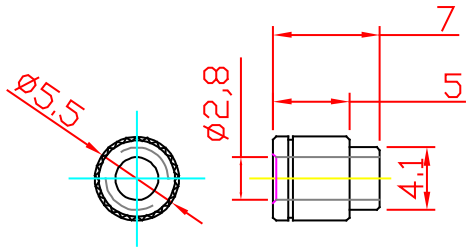


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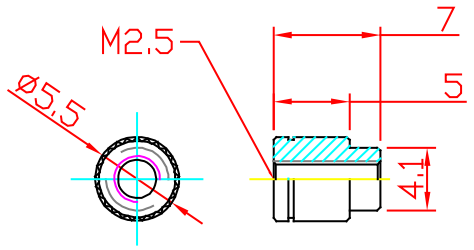
8.8. Standoff Types

The standoffs available for top and bottom mounting methods are shown below. Note that threaded standoffs are DIP type and through-hole standoffs are SMT type. Other types not listed are available upon request.

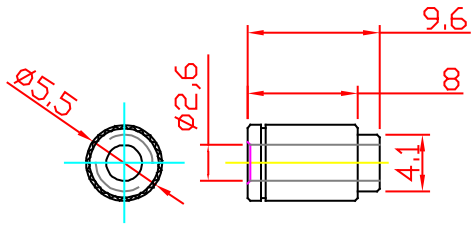
5mm through-hole standoff (SMT type)
P/N: 33-72000-0050



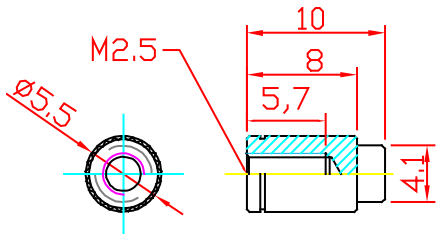
5mm threaded standoff (DIP type)
P/N: 33-72016-0050



8mm through-hole standoff (SMT type)
P/N: 33-72000-0080



8mm threaded standoff (DIP type)
P/N: 33-72015-0050



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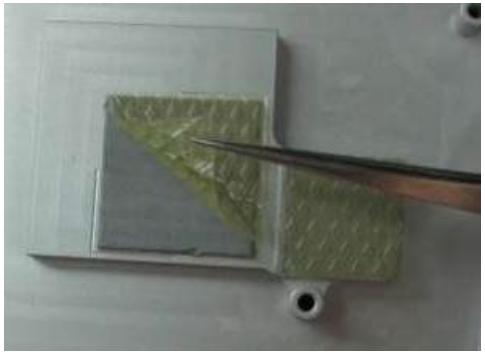
8.9. Installation

Install a heat spreader or heat sink using the following instructions. The images below are for illustration purpose only.

1. Before mounting the heatsink, install the required memory modules onto the SODIMM socket(s) on the COM Express module.

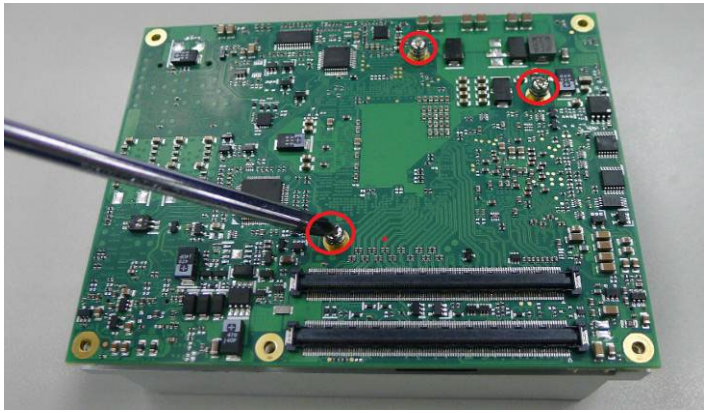


2. Remove the protective membranes from the thermal pads. All thermal pads have a protective membrane (module dependent)



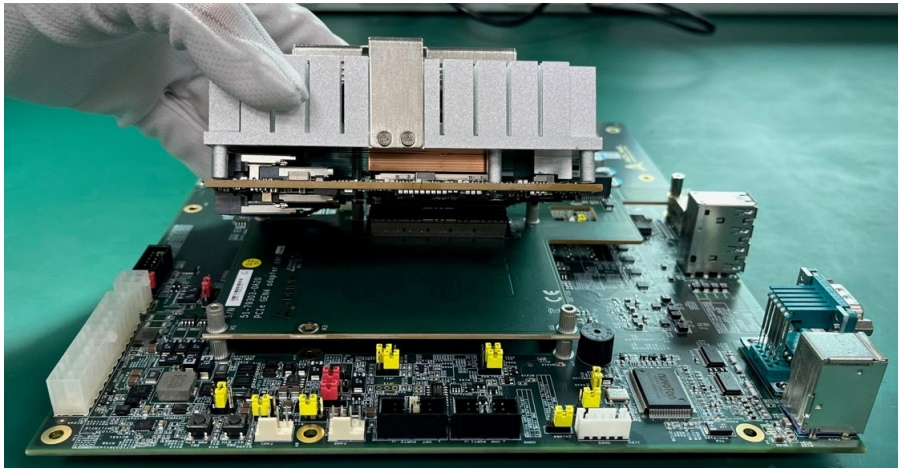
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3. Assemble the heatsink onto the COM Express module. Use the 3x M2.5, L=6mm screws provided to fasten the heatsink to the module. The number of screw holes and screws are module dependent, picture below is for illustration only





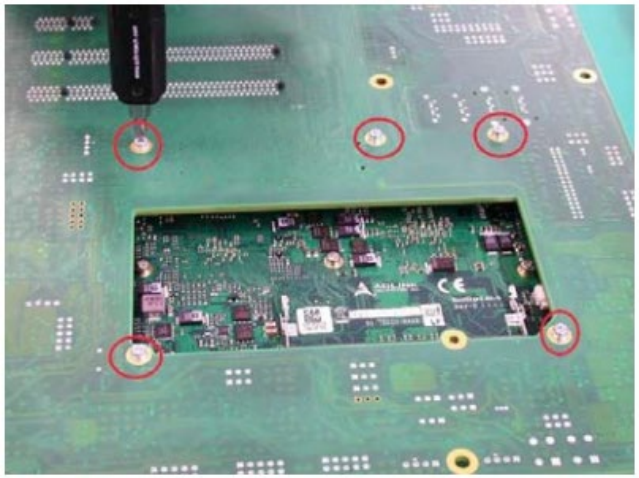
4. Place the COM Express module and heatsink assembly onto the connectors on the carrier board as exemplified below.



Then press down on the module until it is firmly seated on the carrier board.

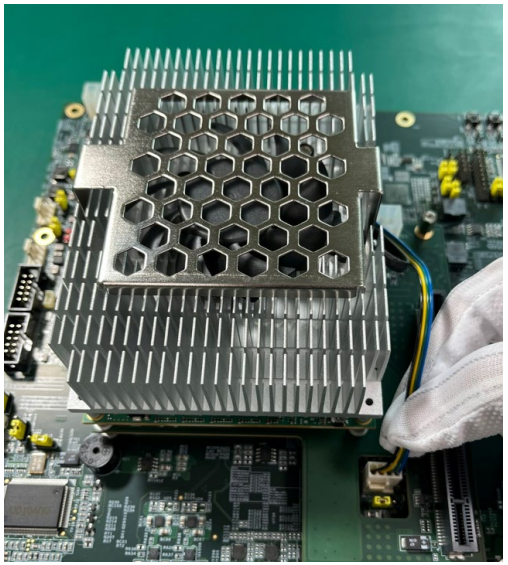
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5. Use the 5x M2.5, L=16mm screws provided to secure the COM Express module to the carrier board from the solder side.





6. If you are installing a heatsink with a fan, plug the fan connector into the carrier board as shown.



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