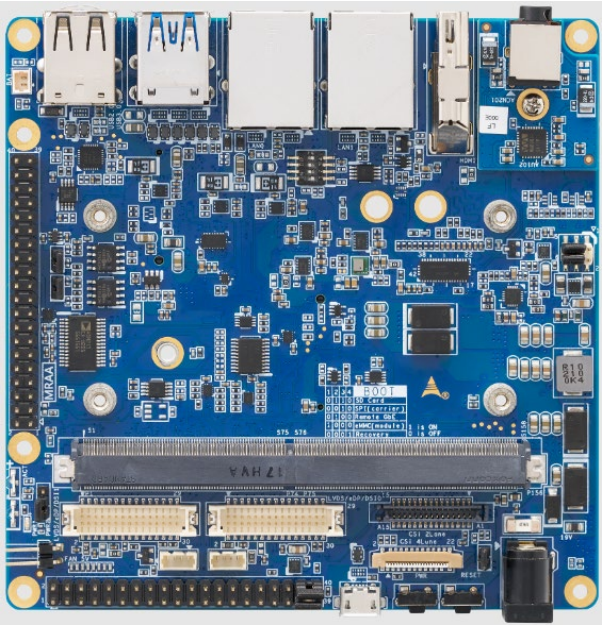
# I-Pi SMARC

User's Guide



SMARC module

| | |
|---|---|
| Revision: | Rev. 0.5 |
| Date: | 2024-07-10 |
| Part Number: | 50M-77A07-1000 |

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# Revision History

| Revision | Description | Date |
|---|---|---|
| 0.1 | Preliminary release | 2024-03-26 |
| 0.2 | Pin definitions updated | 2024-05-14 |
| 0.3 | Images updated | 2024-06-14 |
| 0.4 | Illustrations and labels updated | 2024-07-05 |
| 0.5 | Fan pin definitions added | 2024-07-10 |



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# Preface

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## Safety Instructions

For user safety, please read and follow all Instructions, **WARNING**s, **CAUTION**s, and **NOTE**s marked in this manual and on the associated equipment before handling/operating the equipment.

Read these safety instructions carefully.

- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.


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## Conventions

The following conventions may be used throughout this manual, denoting special levels of information

**Note**: This information adds clarity or specifics to text and illustrations.

**Caution**: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.

**Warning**: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.


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# 1. Introduction

## 1.1 The SMARC Formfactor

The SMARC ("Smart Mobility ARChitecture") is a versatile small form factor Computer-on-Module (COM) definition targeting applications that require low power, low costs, and high performance. SMARC modules typically use Arm SoCs similar to those used in handheld devices such as tablet computers and smart phones. Other low-power SoCs and CPUs, such as tablet-oriented x86 devices and other RISC CPUs may be used as well. SMARC modules' power envelope is typically under 6W.

SMARC has two sizes defined: 82x50 mm and 82x80 mm.

SMARC module PCBs have 314 edge fingers that mate with a low-profile 314 pin 0.5 mm pitch right angle connector (the connector is sometimes identified as a 321-pin connector, where 7 pins are used by the key).

Computer-on-Modules are used as building blocks for portable and stationary embedded systems. The core elements, including CPU, DRAM, boot flash, power sequencing, CPU power supplies, GbE, and a single channel LVDS display transmitter are concentrated on the module, which is used along with an application-specific carrier board that implements other features, such as audio codecs, touch controllers, wireless devices, etc. The modular approach allows scalability, accelerated time-to-market and upgradability while still maintaining low costs, low power, and small physical size.

SGeT STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

SMARC module and carrier specifications are available online at https://www.sget.org/standards/smarc.html


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# 2. Specifications

## 2.1 Boot Modes

The standard boot mode of the I-Pi SMARC Plus is configured as an SD-card boot. Other boot options are supported by a boot-selector switch located on the carrier.

## 2.2 Power Supply

The I-Pi SMARC Plus is powered by a 5.5 mm barrel connector, the supply voltage is 19V DC.

## 2.3 Mechanical and Environmental

**Form Factor**

SGET SMARC Specifications 2.1

**Dimension**

110 x 110 mm

**Operating Temperature**

Standard: 0°C to 60°C Rugged: -40°C to 85°C

**Humidity**

5-90% RH operating, non-condensing

**Shock and Vibration**

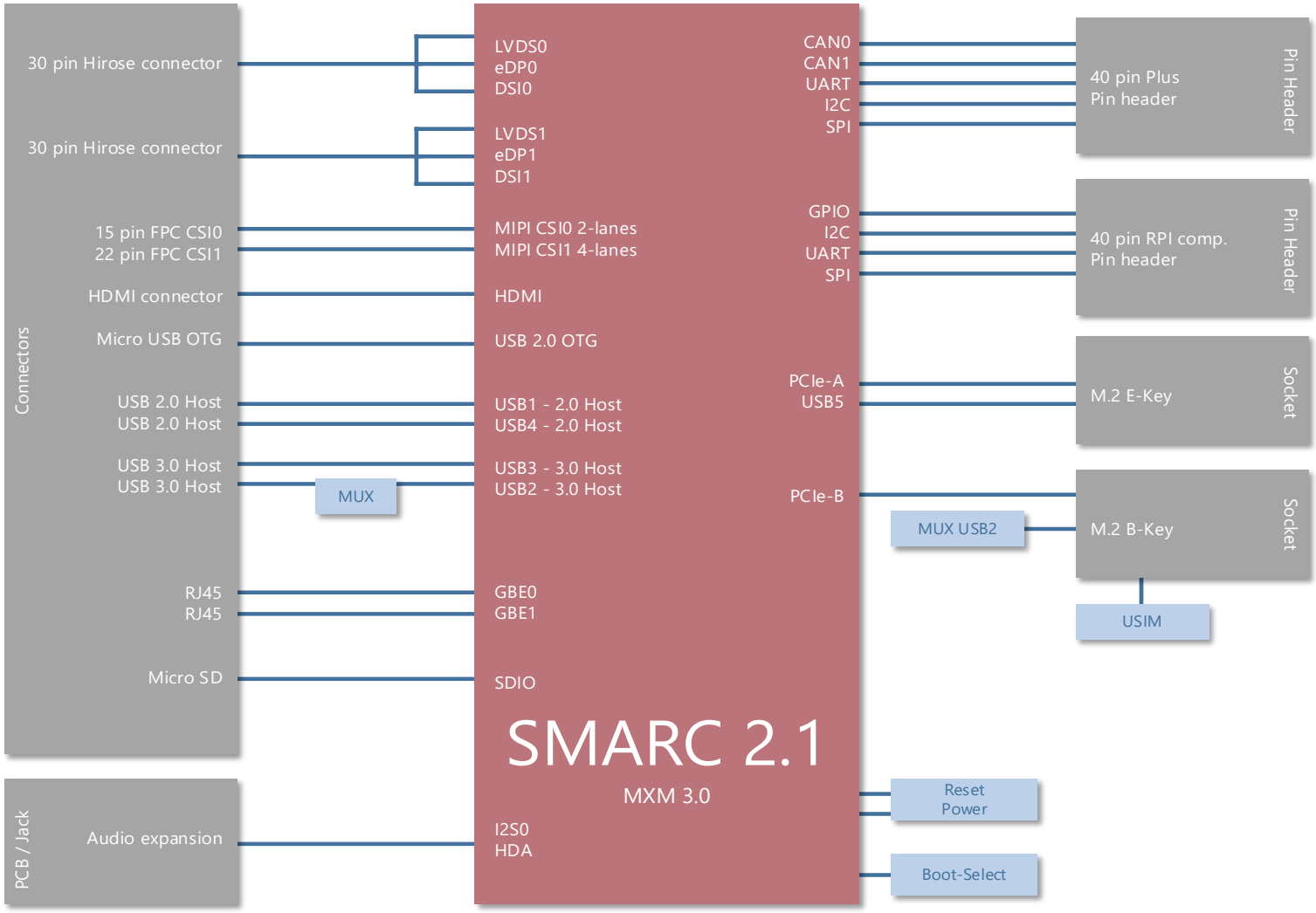
IEC 60068-2-64 and IEC-60068-2-27, MIL-STD-202 F, Method 213B, Table 213-I,

Condition A and Method 214A, Table 214-I, Condition D


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# 3. Block Diagram



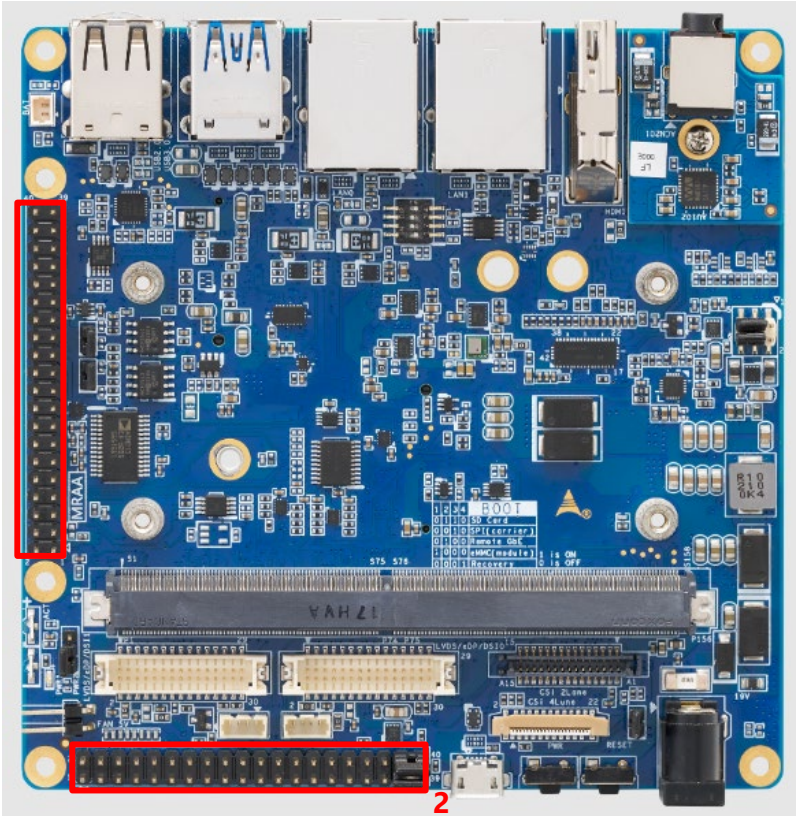


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## 3.1 Pin Header Summary

**1**- 40 pin I/O header (RPI compatible)

| | | | |
|---|---|---|---|
| 3.3V | 1 | 2 | 5V |
| I2C_DAT | 3 | 4 | 5V |
| I2C_CK | 5 | 6 | GND |
| GPIO06 | 7 | 8 | UART0_TX |
| GND | 9 | 10 | UART0_RX |
| GPIO08 | 11 | 12 | GPIO07 |
| GPIO09 | 13 | 14 | GND |
| GPIO10 | 15 | 16 | GPIO11 |
| 3.3V | 17 | 18 | GPIO12 |
| SPI0_MOSI (TX) | 19 | 20 | GND |
| SPI0_MISO (RX) | 21 | 22 | GPIO13 |
| SPI0_SCLK | 23 | 24 | SPI_0_CS0# |
| GND | 25 | 26 | SPI_0_CS1# |
| I2C__DAT | 27 | 28 | I2C_CK |
| GPIO1_0 / PWM | 29 | 30 | GND |
| GPIO1_1 / PWM | 31 | 32 | GPIO1_2 / PWM |
| GPIO1_3 / PWM | 33 | 34 | GND |
| GPIO1_4 / PWM | 35 | 36 | GPIO1_5 / PWM |
| GPIO1_6 / PWM | 37 | 38 | GPIO1_7 / PWM |
| GND | 39 | 40 | GPIO2_8 / PWM |




**2**- 40 pin Plus header

| | | | |
|---|---|---|---|
| SER1 RX | 1 | 2 | SER3 RX |
| SER1 TX | 3 | 4 | SER3 TX |
| GND | 5 | 6 | GND |
| SER2 RX | 7 | 8 | SER2 RTS# |
| SER2 TX | 9 | 10 | SER2 CTS# |
| GND | 11 | 12 | GND |
| CAN0_H | 13 | 14 | CAN1_H |
| CAN0_L | 15 | 16 | CAN1_L |
| GND | 17 | 18 | GND |
| SPI1_HOLD_N | 19 | 20 | SPI1_WP_N |
| SPI1_CS0_N | 21 | 22 | SPI1_CS1_N |
| GND | 23 | 24 | VCC_SPI1 |
| SPI1_CLK | 25 | 26 | GND |
| SPI1_IO0_MOSI | 27 | 28 | SPI1_IO1_MISO |
| SPI1_IO3 | 29 | 30 | SPI1_IO2 |
| ESPI_ALERT0 # | 31 | 32 | ESPI_ALERT1# |
| ESPI RESET_N | 33 | 34 | GND |
| HDMI#_SEL_H | 35 | 36 | M.2 USB3.0 MUX SEL_H |
| HDMI#_SEL | 37 | 38 | M.2 USB 3.0 MUX SEL |
| GND | 39 | 40 | GND |

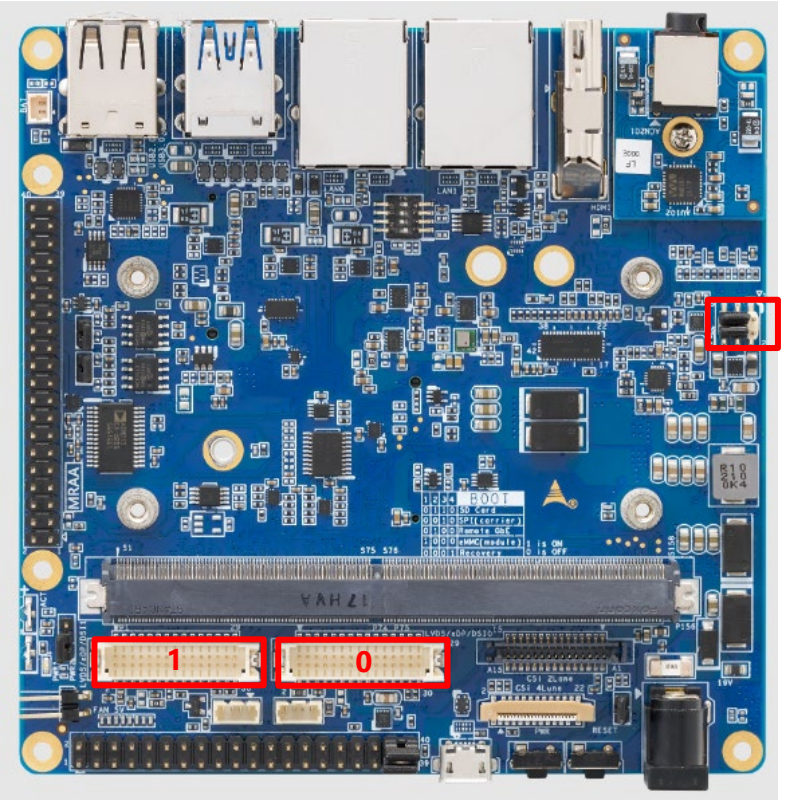

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# 4. Connector Pinout and Signal Descriptions

LVDS/eDP/DSI pin-headers

| | | | |
|---|---|---|---|
| PNLPWR | 2 | 1 | LVDS1_EDP1_DSI1_D0_CN_P |
| PNLPWR | 4 | 3 | LVDS1_EDP1_DSI1_D0_CN_N |
| +VDD_PANEL1_EDID | 6 | 5 | GND |
| +VDD_PANEL1 | 8 | 7 | LVDS1_EDP1_DSI1_D1_CN_P |
| +VDD_PANEL1 | 10 | 9 | LVDS1_EDP1_DSI1_D1_CN_N |
| GND | 12 | 11 | GND |
| LVDS_BKLT1_CTRL | 14 | 13 | LVDS1_EDP1_DSI1_D2_CN_P |
| LVDS_BKLT1_EN | 16 | 15 | LVDS1_EDP1_DSI1_D2_CN_N |
| GND | 18 | 17 | GND |
| LVDS_BKLT1_EN | 20 | 19 | LVDS1_EDP1_DSI1_D3_CN_P |
| LCD1_VDD_EN_3V3 | 22 | 21 | LVDS1_EDP1_DSI1_D3_CN_N |
| eDP1_HPD_DSI1_TE_3V3 | 24 | 23 | GND |
| DDC1_DAT | 26 | 25 | LVDS1_EDP1_DSI1_CK_CN_P |
| DDC1_CK | 28 | 27 | LVDS1_EDP1_DSI1_CK_CN_N |
| GND | 30 | 29 | GND |



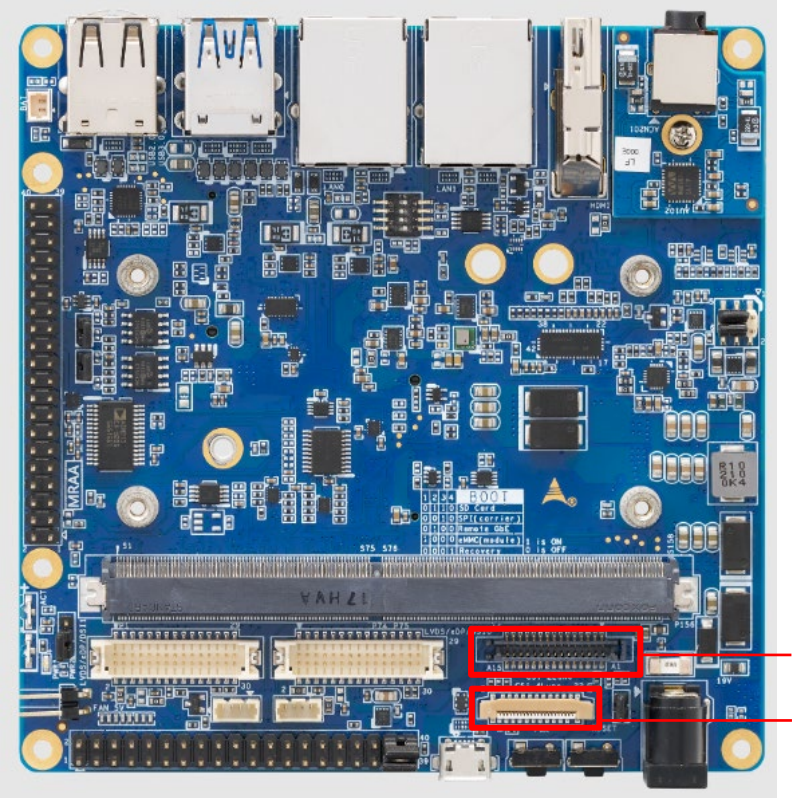

1-3 → 5V backlight
3-5 → 3.3V backlight
Default setting → 5V

| | | | |
|---|---|---|---|
| PNLPWR | 2 | 1 | LVDS0_EDP0_DSI0_D0_CN_P |
| PNLPWR | 4 | 3 | LVDS0_EDP0_DSI0_D0_CN_N |
| +VDD_PANEL0_EDID | 6 | 5 | GND |
| +VDD_PANEL0 | 8 | 7 | LVDS0_EDP0_DSI0_D1_CN_P |
| +VDD_PANEL0 | 10 | 9 | LVDS0_EDP0_DSI0_D1_CN_N |
| GND | 12 | 11 | GND |
| LVDS_BKLT0_CTRL | 14 | 13 | LVDS0_EDP0_DSI0_D2_CN_P |
| LVDS_BKLT0_EN | 16 | 15 | LVDS0_EDP0_DSI0_D2_CN_N |
| GND | 18 | 17 | GND |
| LVDS_BKLT0_EN | 20 | 19 | LVDS0_EDP0_DSI0_D3_CN_P |
| LCD0_VDD_EN_3V3 | 22 | 21 | LVDS0_EDP0_DSI0_D3_CN_N |
| eDP0_HPD_DSI0_TE_3V3 | 24 | 23 | GND |
| DDC0_DAT | 26 | 25 | LVDS0_EDP0_DSI0_CK_CN_P |
| DDC0_CK | 28 | 27 | LVDS0_EDP0_DSI0_CK_CN_N |
| GND | 30 | 29 | GND |

Both connectors use the same pin-out, connector 1 on the left, connector 0 on the right.


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CSI connectors




CSI0

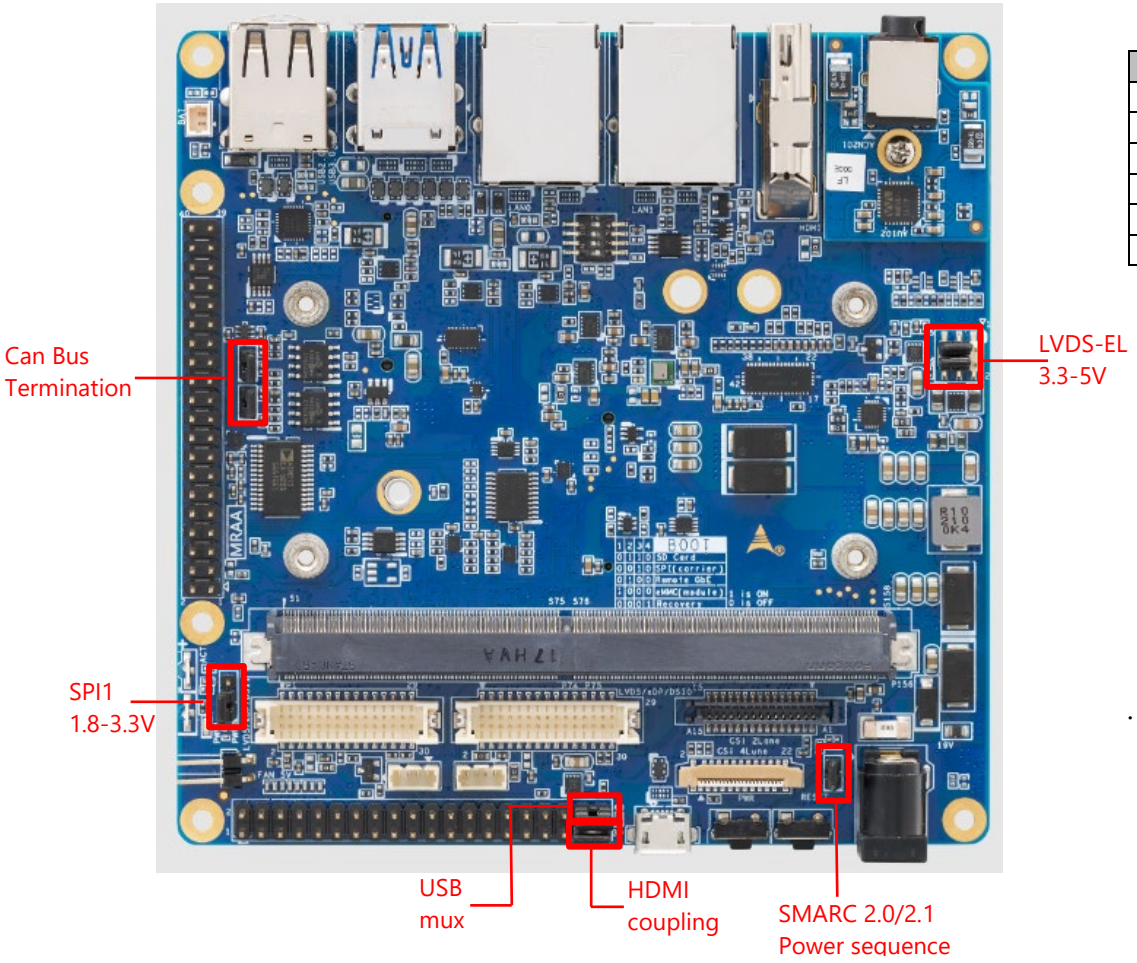
| Pin# | Name | Type | Description |
|---|---|---|---|
| 1 | CAM_3V3 | Power | 3.3V Power |
| 2 | CAM0_I2C_DAT_3V | Bidirection | I2C SDA |
| 3 | CAM0_I2C_CK_3V | Bidirection | I2C SCL |
| 4 | CAM0_MCK_3V_R | Input | Camera Main Clock |
| 5 | CAM0_GPIO0_3V | Input | GPIO for LED |
| 6 | CAM0_GPIO2_3V | Input | GPIO for Enable |
| 7 | CSI0_CK_P | Output | MIPI Clock Lane Positive |
| 8 | CSI0_CK_N | Output | MIPI Clock Lane Negative |
| 9 | GND | Power | Ground |
| 10 | CSI1_D1_P | Output | MIPI Data Lane 1 Positive |
| 11 | CSI1_D1_N | Output | MIPI Data Lane 1 Negative |
| 12 | GND | Power | Ground |
| 13 | CSI1_D0_P | Output | MIPI Data Lane 0 Positive |
| 14 | CSI1_D0_N | Output | MIPI Data Lane 0 Negative |
| 15 | GND | Power | Ground |

CSI1

| Pin# | Name | Type | Description |
|---|---|---|---|
| 1 | CAM_3V3 | Power | 3.3V Power |
| 2 | CAM1_I2C_DAT_3V | Bidirection | I2C SDA |
| 3 | CAM1_I2C_CK_3V | Bidirection | I2C SCL |
| 4 | CAM1_MCK_3V_R | Input | Camera Main Clock |
| 5 | CAM1_GPIO3_3V | Input | GPIO for LED |
| 6 | CAM1_GPIO1_3V | Input | GPIO for Enable |
| 7 | GND | Power | Ground |
| 8 | CSI1_D3_P | Output | MIPI Data Lane 3 Positive |
| 9 | CSI1_D3_N | Output | MIPI Data Lane 3 Negative |
| 10 | GND | Power | Ground |
| 11 | CSI1_D2_P | Output | MIPI Data Lane 2 Positive |
| 12 | CSI1_D2_N | Output | MIPI Data Lane 2 Negative |
| 13 | GND | Power | Ground |
| 14 | CSI1_CK_P | Output | MIPI Clock Lane Positive |
| 15 | CSI1_CK_N | Output | MIPI Clock Lane Negative |
| 16 | GND | Power | Ground |
| 17 | CSI1_D1_P | Output | MIPI Data Lane 1 Positive |
| 18 | CSI1_D1_N | Output | MIPI Data Lane 1 Negative |
| 19 | GND | Power | Ground |
| 20 | CSI1_D0_P | Output | MIPI Data Lane 0 Positive |
| 21 | CSI1_D0_N | Output | MIPI Data Lane 0 Negative |
| 22 | GND | Power | Ground |


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## Jumper settings

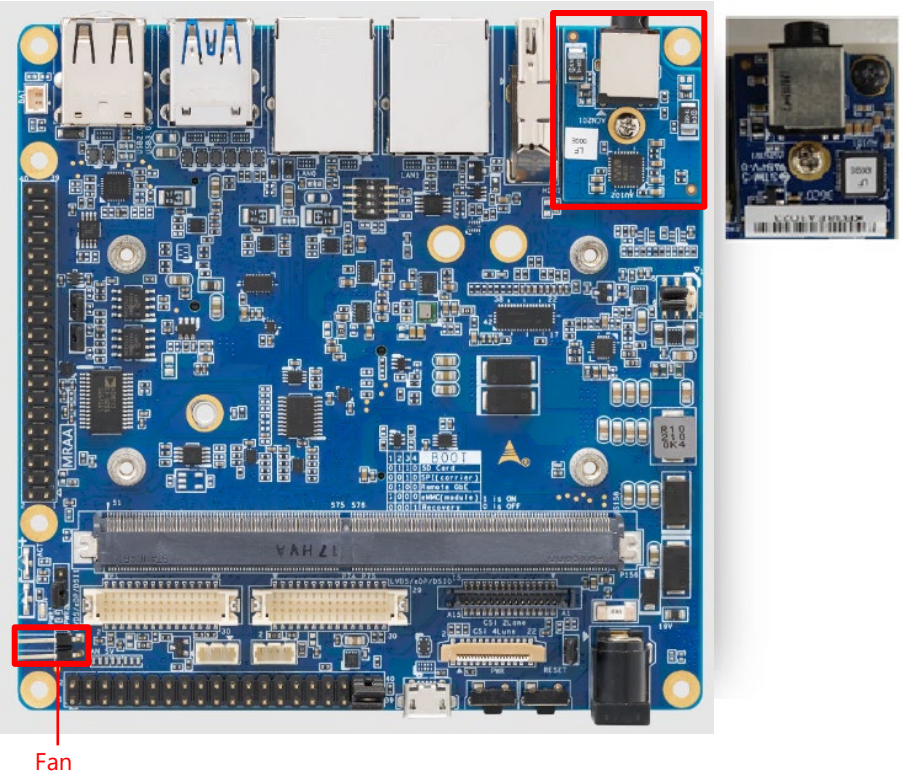



| Interface | Setting |
|---|---|
| Can bus | On = Terminated 120 Ohm |
| LVDS backlight | 1-3 = 5V \| 3-5 = 3.3V |
| SPI1 voltage | 1-2 = 1.8V \| 2-3 = 3.3V |
| USB mux | 36-38 = M.2 \| 38-40 = USB |
| HDMI coupling | 35-37 = AC \| 37-39 = DC |
| SMARC power sequence | On = 2.1 \| Off = 2.0 |


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Audio codec mezzanine






The I-Pi SMARC Plus is equipped with an interchangeable audio codec.

Multiple codecs are available in I2S, HDA or SoundWire.

The board uses a one-screw fixation that sits the codecs in a board-to-board connector.

Fan

| Pin# | Setting |
|---|---|
| 1 | P_VBUS_V5 |
| 2 | GND |


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# 5. Connectors and Signal Descriptions

## 5.1 HDMI

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| HDMI_D2+<br>HDMI_D2-<br>HDMI_D1+<br>HDMI_D1-<br>HDMI_D0+<br>HDMI_D0- | P92<br>P93<br>P95<br>P96<br>P98<br>P99 | HDMI port, differential pair data lines | O TMDS HDMI | | Runtime | | AC coupled off module |
| HDMI_CK+<br>HDMI_CK- | P101<br>P102 | HDMI port, differential pair clock lines | O TMDS HDMI | | Runtime | | AC coupled off module |
| HDMI_CTRL_CK | P105 | I2C_CLK line dedicated to HDMI | O OD COMS | 1.8V | Runtime | PU 2.2 | Level shifter FET and 5V PU resistor shall be placed between the module and the HDMI connector. |
| HDMI_CTRL_DAT | P106 | I2C_DAT line dedicated to HDMI | I/O OD COMS | 1.8V | Runtime | PU 2.2K | Level shifter FET and 5V PU resistor shall be placed between the module and the HDMI connector. |
| HDMI_HPD | P104 | HDMI Hot plug active high detection signal that serves as an interrupt request | I CMOS | 1.8V | Standby | | |


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## 5.2 LVDS

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| LVDS0_0+<br>LVDS0_0-<br>LVDS0_1+<br>LVDS0_1 -<br>LVDS0_2+<br>LVDS0_2-<br>LVDS0_3+<br>LVDS0_3- | S125<br>S126<br>S128<br>S129<br>S131<br>S132<br>S137<br>S138 | Primary LVDS channel differential pair data lines | O LVDS LCD | | Runtime | | |
| LVDS0_CK+<br>LVDS0_CK- | S134<br>S135 | Primary LVDS channel differential pair clock lines | O LVDS LCD | | Runtime | | |
| LCD0_VDD_EN | S133 | Primary LVDS channel power enable, active high | O CMOS | 1.8V | Runtime | | |
| LCD0_BKLT_EN | S127 | Primary LVDS channel backlight enable, active high | O CMOS | 1.8V | Runtime | | |
| LCD0_BKLT_PWM | S141 | Primary LVDS channel brightness control through pulse width modulation (PWM) | O CMOS | 1.8V | Runtime | | |
| LVDS1_0+<br>LVDS1_0-<br>LVDS1_1+<br>LVDS1_1 -<br>LVDS1_2+<br>LVDS1_2-<br>LVDS1_3+<br>LVDS1_3- | S111<br>S112<br>S114<br>S115<br>S117<br>S118<br>S120<br>S121 | Secondary LVDS channel differential pair data lines | O LVDS LCD | | Runtime | | Not supported |
| LVDS1_CK+<br>LVDS1_CK- | S108<br>S109 | Secondary LVDS channel differential pair clock lines. | O LVDS LCD | | Runtime | | Not supported |
| LCD1_VDD_EN | S116 | Secondary panel power enable, active high | O CMOS | 1.8V | Runtime | | Not supported |
| LCD1_BKLT_EN | S107 | Secondary panel backlight enable, active high | O CMOS | 1.8V | Runtime | | Not supported |


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| | | | | | | | |
|---|---|---|---|---|---|---|---|
| LCD1_BKLT_PWM | S122 | Secondary panel brightness control through pulse width modulation (PWM) | O CMOS | 1.8V | Runtime | | Not supported |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| I2C_LCD_DAT | S140 | DDC data line used for flat panel detection and control | I/O OD CMOS | 1.8V | Runtime | PU 2k2 | Possible conflict if 2 LVDS panels are used |
| I2C_LCD_CK | S139 | DDC clock line used for flat panel detection and control | O OD CMOS | 1.8V | Runtime | PU 2k2 | Possible conflict if 2 LVDS panels are used |

## 5.3 DSI

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| DSI0_D0+<br>DSI0_D0-<br>DSI0_D1+<br>DSI0_D1-<br>DSI0_D2+<br>DSI0_D2-<br>DSI0_D3+<br>DSI0_D3- | S125<br>S126<br>S128<br>S129<br>S131<br>S132<br>S137<br>S138 | Primary DSI panel differential pair data lines | O LVDS D-PHY | | Runtime | | |
| DSI0_CLK+<br>DSI0_CLK- | S134<br>S135 | Primary DSI panel differential pair clock lines. | O LVDS D-PHY | | Runtime | | |
| LCD0_VDD_EN | S133 | Primary panel power enable, active high | O CMOS | 1.8V | Runtime | | |
| LCD0_BKLT_EN | S127 | Primary panel backlight enable, active high | O CMOS | 1.8V | Runtime | | |
| LCD0_BKLT_PWM | S141 | Primary panel brightness control through pulse width modulation (PWM) | O CMOS | 1.8V | Runtime | | |
| DSI0_TE | S144 | Primary DSI panel tearing effect sigal | I CMOS | 1.8V | Runtime | | |


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## 5.4 MIPI Camera support

### 5.4.1 MIPI CSI0

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| CSI0_RX0+<br>CSI0_RX0-<br>CSI0_RX1+<br><br>CSI0_RX1- | S11<br>S12<br>S14<br>S15 | CSI0 differential input (point to point) | I LVDS D-PHY / I LVDS M-PHY | | Runtime | | |
| CSI0_CK+<br>CSI0_CK- | S8<br>S9 | CSI0 differential clock intput (point to point) | I LVDS D-PHY | | Runtime | | |
| I2C_CAM0_DAT / ~~CSI0_TX-~~ | S7 | I2C data for serial camera data support link or differential data lane | I/O OD CMOS / O LVDS M-PHY | 1.8V | Runtime | PU 2.2K | MIPI-CSI 2.0 uses I2C_CAM0_DAT<br>MIPI-CSI 3.0 uses CSI0_TX- |
| I2C_CAM0_CK / ~~CSI0_TX+~~ | S5 | I2C clock for serial camera data support link or differential data lane | O OD CMOS / O LVDS M-PHY | 1.8V | Runtime | PU 2.2K | MIPI-CSI 2.0 uses I2C_CAM0_CK<br>MIPI-CSI 3.0 uses CSI0_TX+ |
| CAM0_PWR# / GPIO0 | P108 | Camera 0 Power Enable, active low output. | O CMOS | 1.8V | Runtime | | |
| CAM0_RST# / GPIO2 | P110 | Camera 0 reset, active low output | O CMOS | 1.8V | Runtime | | |
| CAM_MCK | S6 | Master clock output | O CMOS | 1.8V | Runtime | | This signal is used by both CSI0 and CSI1 |


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### 5.4.2 MIPI CSI1 (Camera)

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| CSI1_RX0+<br>CSI1_RX0-<br>CSI1_RX1+<br>CSI1_RX1-<br>CSI1_RX2+<br>CSI1_RX2-<br>CSI1_RX3+<br>CSI1_RX3- | P7<br>P8<br>P10<br>P11<br>P13<br>P14<br>P16<br>P17 | CSI1 differential input (point to point) | I LVDS D-PHY / I LVDS M-PHY | | Runtime | | |
| CSI1_CK+<br>CSI1_CK- | P3<br>P4 | CSI1 differential clock input (point to point) | I LVDS D-PHY | | Runtime | | |
| I2C_CAM1_DAT / ~~CSI1_TX-~~ | S2 | I2C data for serial camera data support link or differential data lane | I/O OD CMOS / O LVDS M-PHY | 1.8V | Runtime | PU 2.2K | MIPI-CSI 2.0 mode uses I2C_CAM1_DAT<br>MIPI-CSI 3.0 mode uses CSI1_TX- |
| I2C_CAM1_CK / ~~CSI1_TX+~~ | S1 | I2C clock for serial camera data support link or differential data lane | O OD CMOS / O LVDS M-PHY | 1.8V | Runtime | PU 2.2K | MIPI-CSI 2.0 mode uses I2C_CAM1_CK<br>MIPI-CSI 3.0 mode uses CSI1_TX+ |
| CAM1_PWR# / GPIO1 | P109 | Camera 0 Power Enable, active low output. | O CMOS | 1.8V | Runtime | | CAM1_PWR# is default, GPIO1 can be enabled through DVT |
| CAM1_RST# / GPIO3 | P111 | Camera 0 reset, active low output | O CMOS | 1.8V | Runtime | | CAM1_PWR# is default, GPIO3 can be enabled through DVT |
| CAM_MCK | S6 | Master clock output | O CMOS | 1.8V | Runtime | | This signal is used by both CSI0 and CSI1 |


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## 5.5 Audio

### 5.5.1 I2S

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| I2S0_LRCK | S39 | I2S0 Left & Right synchronization clock | I/O CMOS | 1.8V | Runtime | | Module Output if CPU acts in Master Mode<br>Module Input if CPU acts in Slave Mode |
| I2S0_SDOUT | S40 | I2S0 Digital audio Output | O CMOS | 1.8V | Runtime | | |
| I2S0_SDIN | S41 | I2S0 Digital audio Input | I CMOS | 1.8V | Runtime | | |
| I2S0_CK | S42 | I2S0 Digital audio clock | I/O CMOS | 1.8V | Runtime | | Module Output if CPU acts in Master Mode<br>Module Input if CPU acts in Slave Mode |
| I2S2_LRCK | S50 | I2S2 Left & Right synchronization clock | I/O CMOS | 1.8V | Runtime | | Module Output if CPU acts in Master Mode<br>Module Input if CPU acts in Slave Mode |
| I2S2_SDOUT | S51 | I2S2 Digital audio Output | O CMOS | 1.8V | Runtime | | |
| I2S2_SDIN | S52 | I2S2 Digital audio Input | I CMOS | 1.8V | Runtime | | |
| I2S2_CK | S53 | I2S2 Digital audio clock | I/O CMOS | 1.8V | Runtime | | Module Output if CPU acts in Master Mode<br>Module Input if CPU acts in Slave Mode |
| AUDIO_MCK | S38 | Master clock output to I2S codec(s) | O CMOS | 1.8V | Runtime | | |

**Note**:

1. I2S signals are routed to the Audio Expansion Board pin header.
2. Support for I2S1 signalling pins has been removed during update to SMARC 2.0 specification.


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### 5.5.2 HDA

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| HDA_SYNC / I2S2_LRCK | S50 | High Definition Audio Sample synchronization clock to codec | I/O CMOS | 1.8V / 1.5V | Runtime | | SMARC HDA Audio signalling supports 1.5V or 1.8V.<br><br>Please check with your module vendor if 1.5V or 1.8V is supported and use an audio codec that is capable to support the regarding I/O voltage. This specification ignores the discrepancy between the 1.5V and 1.8V signalling, as the chance of damage in mismatched systems is negligible.<br><br>The SMARC HD Audio pins are shared with the I2S2 pins, which are defined to be 1.8V only. |
| HDA_SDO / I2S2_SDOUT | S51 | High Definition Audio data out to codec | O CMOS | 1.8V / 1.5V | Runtime | | |
| HDA_SDI / I2S2_SDIN | S52 | High Definition Audio data in from codec | I/O CMOS | 1.8V / 1.5V | Runtime | | |
| HDA_CK / I2S2_CK | S53 | High Definition Audio clock to codec | O CMOS | 1.8V / 1.5V | Runtime | | |
| HDA_RST# / GPIO4 | P112 | High Definition Audio reset output to codec, low active. | O CMOS | 1.8V / 1.5V | Runtime | | |

**Note**: HDA signals are routed to the Audio Expansion Board pin header.


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## 5.6 USB Ports

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| USB0+<br>USB0- | P60<br>P61 | USB differential data pairs for port 0 | I/O<br>USB | USB | Standby | | |
| USB0_EN_OC# | P62 | USB over-current sense for port 0 | I/O OD<br>CMOS | 3.3Vsb /<br>3.3V | Standby | PU 10k | Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation. |
| USB0_VBUS_DET | P63 | USB port 0 host power detection, when this port is used as a device. | I<br>USB VBUS 5V | USB VBUS 5V | Standby | | Can be connected to a USB client port VBUS pin |
| USB0_OTG_ID | P64 | Input pin to announce OTG device insertion on USB 2.0 port | I<br>CMOS | 3.3Vsb /<br>3.3V | Standby | | |
| USB1+<br>USB1- | P65<br>P66 | USB differential data pairs for port 1 | I/O<br>USB | USB | Standby | | |
| USB1_EN_OC# | P67 | USB over-current sense for port 1 | I/O OD<br>CMOS | 3.3Vsb / 3.3V | Standby | PU 10k | Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation. |
| USB2+<br>USB2- | P69<br>P70 | USB differential data pairs for port 2 | I/O<br>USB | USB | Standby | | |
| USB2_SSRX+<br>USB2_SSRX- | S74<br>S75 | Receive signal differential pairs for SuperSpeed on port 2 | I<br>USB SS | USB SS | Standby | | Coupling caps for RX pairs are on the USB Device |
| USB2_SSTX+<br>USB2_SSTX- | S71<br>S72 | Transmit signal differential pairs for SuperSpeed on port 2 | O<br>USB SS | USB SS | Standby | | Coupling caps for TX pairs are on the Module |
| USB2_EN_OC# | P71 | USB over-current sense for port 2 | I/O OD<br>CMOS | 3.3Vsb / 3.3V | Standby | PU 10k | Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation. |
| USB3+<br>USB3- | S68<br>S69 | USB differential data pairs for port 3 | I/O<br>USB | USB | Standby | | |
| USB3_SSRX+<br>USB3_SSRX- | S65<br>S66 | Receive signal differential pairs for SuperSpeed on port 3 | I<br>USB SS | USB SS | Standby | | Coupling caps for RX pairs are on the USB Device |


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| | | | | | | | |
|---|---|---|---|---|---|---|---|
| USB3_SSTX+<br>USB3_SSTX- | S62<br>S63 | Transmit signal differential pairs for SuperSpeed on port 3 | O<br>USB SS | USB SS | Standby | | Coupling caps for TX pairs are on the Module |
| USB3_EN_OC# | P74 | USB over-current sense for port 3 | I/O OD<br>CMOS | 3.3Vsb /<br>3.3V | Standby | PU 10k | Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation. |
| USB3_VBUS_DET | S37 | USB port 3 host power detection, when this port is used as a device. | I<br>USB VBUS 5V | USB VBUS 5V | Standby | | |
| USB3_OTG_ID | S104 | Input pin to announce OTG device insertion on USB 3.0 port | I<br>CMOS | 3.3Vsb /<br>3.3V | Standby | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| USB4+<br>USB4- | S35<br>S36 | USB differential data pairs for port 4 | I/O<br>USB | USB | Standby | | |
| USB4_EN_OC# | P76 | USB over-current sense for port 4 | I/O OD<br>CMOS | 3.3Vsb / 3.3V | Standby | PU 10k | Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation. |

**Note**: USB0 is directly connected to the SoC, USB1/2/3/4 might come over a USB hub on the SMARC module.


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## 5.7 PCIe Ports

two PCIe Gen 2.1 ports (PCIE_A and PCIE_B).

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| PCIE_A_TX+<br>PCIE_A_TX- | P89<br>P90 | Differential PCIe link A transmit data pair | O LVDS PCIE | | Runtime | | Series AC coupled on module |
| PCIE_A_RX+<br>PCIE_A_RX- | P86<br>P87 | Differential PCIe link A receive data pair | I LVDS PCIE | | Runtime | | Series AC coupled off module |
| PCIE_A_REFCK+<br>PCIE_A_REFCK- | P83<br>P84 | Differential PCIe Link A reference clock output | O LVDS PCIE | | Runtime | | |
| PCIE_A_RST# | P75 | PCIe Port A reset output | O CMOS | 3.3V | Runtime | | |
| ~~PCIE_A_CKREQ#~~ | ~~P78~~ | ~~PCIe Port A clock request~~ | ~~I OD CMOS~~ | ~~3.3V~~ | ~~Runtime~~ | - | No need for this signal because module provides onboard PCIe clock |
| PCIE_B_TX+<br>PCIE_B_TX- | S90<br>S91 | Differential PCIe link B transmit data pair | O LVDS PCIE | | Runtime | | Series AC coupled on module |
| PCIE_B_RX+<br>PCIE_B_RX- | S87<br>S88 | Differential PCIe link B receive data pair | I LVDS PCIE | | Runtime | | Series AC coupled off module |
| PCIE_B_REFCK+<br>PCIE_B_REFCK- | S84<br>S85 | Differential PCIe Link B reference clock output | O LVDS PCIE | | Runtime | | |
| PCIE_B_RST# | S76 | PCIe Port B reset output | O CMOS | 3.3V | Runtime | | |
| ~~PCIE_B_CKREQ#~~ | ~~P77~~ | ~~PCIe Port B clock request~~ | ~~I OD CMOS~~ | ~~3.3V~~ | ~~Runtime~~ | | No need for this signal because module provides onboard PCIe clock |
| PCIE_WAKE# | S146 | PCIe wake up interrupt to host – common to PCIe links A, B, C, D | I OD CMOS | 3.3V | Runtime | PU 10k | |

**Note**: The module provides PCIe clock generators for PCIE_A and PCIE_B, thus not external clock source on the carrier is needed.


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## 5.8 LAN Ports

### 5.8.1 1st LAN

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| GBE0_MDI0+<br>GBE0_MDI0-<br>GBE0_MDI1+<br>GBE0_MDI1-<br>GBE0_MDI2+<br>GBE0_MDI2-<br>GBE0_MDI3+<br>GBE0_MDI3- | P30<br>P29<br>P27<br>P26<br>P24<br>P23<br>P20<br>P19 | Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following:<br>1000 / 100 / 10<br>MDI[0]+/- B1_DA+/- TX+/- TX+/-<br>MDI[1]+/- B1_DB+/- RX+/- RX+/-<br>MDI[2]+/- B1_DC+/-<br>MDI[3]+/- B1_DD+/- | GBE MDI | | Runtime | | Twisted pair signals for external transformer. |
| GBE0_LINK100# | P21 | Link Speed Indication LED for GBE 0 100Mbps | O OD CMOS | 3.3V | Runtime | | Shall be able to sink 24mA or more Carrier LED current |
| GBE0_LINK1000# | P22 | Link Speed Indication LED for GBE 0 1000Mbps | O OD CMOS | 3.3V | Runtime | | Shall be able to sink 24mA or more Carrier LED current |
| GBE0_LINK_ACT# | P25 | Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity | O OD CMOS | 3.3V | Runtime | | Shall be able to sink 24mA or more Carrier LED current |
| ~~GBE0_CTREF~~ | ~~P28~~ | ~~Center-Tap reference voltage for Carrier board Ethernet magnetic (if required by the Module GBE PHY)~~ | ~~Analog~~ | ~~0 to 3.3V max~~ | Runtime | - | - |
| GBE0_SDP | P6 | IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol) | IO CMOS | 3.3V | Runtime | | |


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### 5.8.2 2nd LAN

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| GBE1_MDI0+<br>GBE1_MDI0-<br>GBE1_MDI1+<br>GBE1_MDI1-<br>GBE1_MDI2+<br>GBE1_MDI2-<br>GBE1_MDI3+<br>GBE1_MDI3- | S17<br>S18<br>S20<br>S21<br>S23<br>S24<br>S26<br>S27 | Gigabit Ethernet Controller 1: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following:<br>1000 100 10<br>MDI[0]+/- B1_DA+/- TX+/- TX+/-<br>MDI[1]+/- B1_DB+/- RX+/- RX+/-<br>MDI[2]+/- B1_DC+/-<br>MDI[3]+/- B1_DD+/- | GBE MDI | | Runtime | | Twisted pair signals for external transformer. |
| GBE1_LINK100# | S19 | Link Speed Indication LED for GBE 1 100Mbps | O OD CMOS | 3.3V | Runtime | | Shall be able to sink 24mA or more Carrier LED current |
| GBE1_LINK1000# | S22 | Link Speed Indication LED for GBE 1 1000Mbps | O OD CMOS | 3.3V | Runtime | | Shall be able to sink 24mA or more Carrier LED current |
| GBE1_LINK_ACT# | S31 | Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity | O OD CMOS | 3.3V | Runtime | | Shall be able to sink 24mA or more Carrier LED current |
| ~~GBE1_CTREF~~ | ~~S28~~ | ~~Center-Tap reference voltage for Carrier board Ethernet magnetic `(if required by the Module GBE PHY)`~~ | ~~Analog~~ | ~~0 to 3.3V max~~ | ~~Runtime~~ | | |
| GBE1_SDP | P5 | IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol) | IO CMOS | 3.3V | Runtime | | |

**Note**: The number of functional LAN ports is dependent on the module used.


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## 5.9 SDIO

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| SDIO_D0<br>SDIO_D1<br>SDIO_D2<br>SDIO_D3 | P39<br>P40<br>P41<br>P42 | SDIO Data lines. These signals operate in push-pull mode. | I/O CMOS | 1.8V or 3.3V | Runtime | | SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly |
| SDIO_WP | P33 | SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards. | I OD CMOS | 3.3V | Runtime | PU 10k | Pulled up on module |
| SDIO_CMD | P34 | SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode. | I/O CMOS | 1.8V or 3.3V | Runtime | | SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly |
| SDIO_CD# | P35 | SDIO Card Detect.<br>This signal indicates when a SDIO/MMC card is present. | I OD CMOS | 3.3V | Runtime | PU 10k | Pulled up on module |
| SDIO_CK | P36 | SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. | O CMOS | 1.8V or 3.3V | Runtime | | |
| SDIO_PWR_EN | P37 | SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device. | O CMOS | 3.3V | Runtime | | should be driven low in STB Mode by the module |


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## 5.10 SPI & ESPI

### 5.10.1 SPI0

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| SPI0_CS0# | P43 | SPI0 Master Chip Select 0 | O CMOS | 1.8V | Standby | | This signal can be used to select carrier SPI as boot device |
| SPI0_CS1# | P31 | SPI0 Master Chip Select 1 | O CMOS | 1.8V | Standby | | |
| SPI0_CK | P44 | SPI0 Clock | O CMOS | 1.8V | Standby | | |
| SPI0_DIN | P45 | SPI0 Master input / Slave output | I CMOS | 1.8V | Standby | | also referred to as MISO |
| SPI0_DO | P46 | SPI0 Master output / Slave input | O CMOS | 1.8V | Standby | | also referred to as MOSI |
| SPI1_CS0# | P54 | SPI1 Master Chip Select 0 | O CMOS | 1.8V | Standby | | See ESPI |
| SPI1_CS1# | P55 | SPI1 Master Chip Select 1 | O CMOS | 1.8V | Standby | | See ESPI |
| SPI1_CK | P56 | SPI1 Clock | O CMOS | 1.8V | Standby | | See ESPI |
| SPI1_DIN | P57 | SPI1 Master input / Slave output | I CMOS | 1.8V | Standby | | See ESPI |
| SPI1_DO | P58 | SPI1 Master output / Slave input | O CMOS | 1.8V | Standby | | See ESPI |

**Note**: SPI0 on RPI header, SPI1 on plus header. See jumper settings for SPI voltage.


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### 5.10.2 ESPI

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| ESPI_CS0# | P54 | ESPI1 Master Chip Select 0 | O CMOS | 1.8V | Standby | | |
| ~~ESPI_CS1#~~ | P55 | ESPI1 Master Chip Select 1 | O CMOS | 1.8V | Standby | | |
| ESPI_CK | P56 | ESPI Master Clock output | O CMOS | 1.8V | Standby | | |
| ESPI_RESET# | S58 | ESPI Reset | O CMOS | 1.8V | Standby | | Reset the eSPI interface for both master and slaves.<br><br>eSPI Reset# is typically driven from eSPI master to eSPI slaves |
| ESPI_ALERT0#<br>~~ESPI_ALERT1#~~ | S43<br>S44 | ESPI ALERT | I OD CMOS | 1.8V | Standby | | This pin is used by eSPI slave to request service from eSPI.master.Alert# is an open-drain output from the slave.<br>This pin is optional for Single Master-Single Slave configuration where I/O[1] can be used to signal the Alert event. |
| ESPI_IO_0<br>ESPI_IO_1<br>~~ESPI_IO_2~~<br>~~ESPI_IO_3~~ | P58<br>P57<br>~~S56~~<br>~~S57~~ | ESPI Master Data Input / Output. | I/O CMOS | 1.8V | Standby | | ESPI_IO_0 can also be used as SPI1_DO (MOSI)<br>ESPI_IO_1 can also be used as SPI1_DIN (MISO)<br><br>In Single I/O mode, ESPI_IO_0 is the eSPI master output / eSPI slave input (MOSI) whereas ESPI_IO_1 is the SPI master input / eSPI slave output (MISO). |


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## 5.11 General Purpose I2C

The SMARC specification supports a total of 6 different I2C busses on its pinout. Most of these busses are designated for specific functions such as I2C for camera management, I2C for EDID on HDMI, LVDS panels or I2C for PMIC. Just one I2C bus is for general purpose.

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| I2C_GP_DAT | S49 | General purpose I2C data signal | I/O OD CMOS | 1.8V | Runtime | PU 2k2 | |
| I2C_GP_CK | S48 | General purpose I2C clock signal | O OD CMOS | 1.8V | Runtime | PU 2k2 | |

Most of the other I2C busses are described in their designated function tables rather than in a single big list.

Below is an overview of all I2C busses and where to find them.

| Name | Pin # | Description | Where to find |
|---|---|---|---|
| I2C_LCD_DAT | S140 | DDC data line used for flat panel detection and control | LVDS / DSI / eDP tables |
| I2C_LCD_CK | S139 | DDC clock line used for flat panel detection and control | LVDS / DSI / eDP tables |
| HDMI_CTRL_CK | P105 | I2C_CLK line dedicated to HDMI | HDMI table |
| HDMI_CTRL_DAT | P106 | I2C_DAT line dedicated to HDMI | HDMI table |
| I2C_CAM0_DAT | S7 | I2C data for serial camera data support link | MIPI CSI table |
| I2C_CAM0_CK | S5 | I2C clock for serial camera data support link | MIPI CSI table |
| I2C_CAM1_DAT | S2 | I2C data for serial camera data support link | MIPI CSI table |
| I2C_CAM1_CK | S1 | I2C clock for serial camera data support link | MIPI CSI table |
| I2C_PM_DAT | P122 | Power management I2C bus DATA (SMBus for x86) | Power and System Management |
| I2C_PM_CK | P121 | Power management I2C bus CLK (SMBus for x86) | Power and System Management |


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## 5.12 GPIO

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| GPIO0 / CAM0_PWR# | P108 | General purpose I/O pin 0. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module. | Default use is GPIO0, alternative use is Camera 0 Power Enable - active low, through DTS |
| GPIO1 / CAM1_PWR# | P109 | General purpose I/O pin 1. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | Default use is is GPIO1 alternative use is Camera 1 Power Enable - active low, through DTS |
| GPIO2 / CAM0_RST# | P110 | General purpose I/O pin 2. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | Default use is GPIO2, alternative use is Camera 0 Reset - active low, through DTS |
| GPIO3 / CAM1_RST# | P111 | General purpose I/O pin 3. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | Default use is GPIO3, alternative use is Camera 1 Reset - active low, through DTS |
| GPIO4 / ~~HDA_RST#~~ | P112 | General purpose I/O pin 4. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | |
| GPIO5 / ~~PWM_OUT~~ | P113 | General purpose I/O pin 5. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | |
| GPIO6 | P114 | General purpose I/O pin 6. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | |
| GPIO7 | P115 | General purpose I/O pin 7. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | |
| GPIO8 | P116 | General purpose I/O pin 8. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | |
| GPIO9 | P117 | General purpose I/O pin 9. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | |
| GPIO10 | P118 | General purpose I/O pin 10. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | |
| GPIO11 | P119 | General purpose I/O pin 11. | I/O CMOS | 1.8V | Runtime | PU 470K on the Module | |
| ~~GPIO12~~ | ~~S142~~ | ~~General purpose I/O pin 12~~ | ~~I/O CMOS~~ | ~~1.8V~~ | ~~Runtime~~ | ~~PU 470K on the Module~~ | |
| ~~GPIO13~~ | ~~S123~~ | ~~General purpose I/O pin 13~~ | ~~I/O CMOS~~ | ~~1.8V~~ | ~~Runtime~~ | ~~PU 470K on the Module~~ | |

**Note**: All GPIO are on RPI header.


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## 5.13 UART

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| SER0_TX | P129 | Asynchronous serial data output port 0 | O CMOS | 1.8V | Runtime | | |
| SER0_RX | P130 | Asynchronous serial data input port 0 | I CMOS | 1.8V | Runtime | | |
| ~~SER0_RTS#~~ | ~~P131~~ | ~~"Request to Send" handshake line for port 0~~ | ~~O CMOS~~ | ~~1.8V~~ | ~~Runtime~~ | | |
| ~~SER0_CTS#~~ | ~~P132~~ | ~~"Clear to Send" handshake line for port 0~~ | ~~I CMOS~~ | ~~1.8V~~ | ~~Runtime~~ | | |
| SER1_TX | P134 | Asynchronous serial data output port 1 | O CMOS | 1.8V | Runtime | | |
| SER1_RX | P135 | Asynchronous serial data input port 1 | I CMOS | 1.8V | Runtime | | |
| SER2_TX | P136 | Asynchronous serial data output port 2 | O CMOS | 1.8V | Runtime | - | - |
| SER2_RX | P137 | Asynchronous serial data input port 2 | I CMOS | 1.8V | Runtime | - | - |
| SER2_RTS# | P138 | "Request to Send" handshake line for port 2 | O CMOS | 1.8V | Runtime | - | - |
| SER2_CTS# | P139 | "Clear to Send" handshake line for port 2 | I CMOS | 1.8V | Runtime | - | - |
| SER3_TX | P140 | Asynchronous serial data output port 3 | O CMOS | 1.8V | Runtime | | |
| SER3_RX | P141 | Asynchronous serial data input port 3 | I CMOS | 1.8V | Runtime | | |

**Note**: SER0 on RPI header, SER1,2,3 on plus header.


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## 5.14 CAN Bus

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| CAN0_TX | P143 | CAN port 0 Transmit output | O CMOS | 1.8V | Runtime | | |
| CAN0_RX | P144 | CAN port 0 Receive input | I CMOS | 1.8V | Runtime | | |
| CAN1_TX | P145 | CAN port 1 Transmit output | O CMOS | 1.8V | Runtime | | |
| CAN1_RX | P146 | CAN port1 Receive input | I CMOS | 1.8V | Runtime | | |

**Note:** Can 0,1 are located on plus header.

## 5.15 Miscellaneous

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| TEST# | S157 | Held low by Carrier to invoke Module vendor specific test function(s). | I CMOS | 1.8V | Runtime | PU on Module. Driven by OD on Carrier | Module must implement PU but actual value is depended on particular module design. Carrier Board should leave this pin floating for normal operation |
| WDT_TIME_OUT# | S145 | Watch-Dog-Timer Output, low active. | O CMOS | 1.8V | Runtime | | Driven only during runtime |


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## 5.16 Power and System Management

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| BATLOW# | S156 | Battery low indication to Module. Carrier to float the line in inactive state. | I OD CMOS | 1.8V | Runtime | PU 10K | Driven by OD on Carrier.<br>Pulled up on module. |
| CARRIER_PWR_ON | S154 | Carrier board circuits (apart from power management and power path circuits) should not be powered up until the Module asserts the CARRIER_PWR_ON signal. | O CMOS | 1.8Vsb / 1.8V | - | | 1.8Vsb is only used for signaling, not a power source to the module |
| CARRIER_STBY# | S153 | The Module shall drive this signal low when the system is in a standby power state. | O CMOS | 1.8Vsb / 1.8V | - | | |
| CHARGER_PRSNT# | S152 | Held low by Carrier if DC input for battery charger is present. | I OD CMOS | 1.8V | Runtime | PU 4.7K | Driven by OD on Carrier.<br>Pulled up on module. |
| CHARGING# | S151 | Held low by Carrier during battery charging. Carrier to float the line when charge is complete. | I OD CMOS | 1.8V | Runtime | PU 4.7K | Driven by OD on Carrier.<br>Pulled up on module. |
| VIN_PWR_BAD# | S150 | Power bad indication from Carrier board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) shall not be enabled while this signal is held low by the Carrier. | I OD CMOS | 1.8V | Runtime | PU 2.2K | Driven by OD on Carrier<br>Module must implement PU but actual value is depended on particular module design. |
| SLEEP# | S149 | Sleep indicator from Carrier board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state.Active low, level sensitive. Should be de-bounced on the Module. | I OD CMOS | 1.8V | Runtime | PU 4.7K | Driven by OD on Carrier.<br>Pulled up on module. |
| LID# | S148 | Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module. | I OD CMOS | 1.8V | Runtime | PU 4.7K | Driven by OD on Carrier.<br>Pulled up on module. |
| POWER_BTN# | P128 | Power-button input from Carrier board. Carrier to float the line in in-active state. Active low, level sensitive. Should be debounced on the Module. | I OD CMOS | 1.8V | Runtime | PU 4.7K | Driven by OD on Carrier.<br>Pulled up on module. |
| RESET_OUT# | P126 | General purpose reset output to Carrier board. | O CMOS | 1.8V | Runtime | | |


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| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| RESET_IN# | P127 | Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise. | I OD CMOS | 1.8V | Runtime | PU 4.7K | Driven by OD on Carrier. Pulled up on module. |
| I2C_PM_DAT | P122 | Power management I2C bus DATA | I/O OD CMOS | 1.8V | Runtime | PU 2k2 | On x86 systems these serve as SMB DATA. Pulled up on module. |
| I2C_PM_CK | P121 | Power management I2C bus CLK | O OD CMOS | 1.8V | Runtime | PU 2k2 | On x86 systems these serve as SMB CLK. Pulled up on module. |
| ~~SMB_ALERT_1V8#~~ | P1 | ~~SMBus Alert# (interrupt) signal~~ | ~~I OD CMOS~~ | ~~1.8V~~ | ~~Runtime~~ | ~~PU 2k2~~ | ~~only used on x86 design~~ |


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### 5.16.1 Boot Select

| Name | Pin # | Description | I/O Type | I/O Level | Power Domain | PU / PD | Comments |
|---|---|---|---|---|---|---|---|
| BOOT_SEL0#<br>BOOT_SEL1#<br>BOOT_SEL2# | P123<br>P124<br>P125 | Input straps determine the Module boot | I OD CMOS | 1.8Vsb | Standby | PU 4.7K | Driven by OD on Carrier.<br>Pulled up on module.<br><br>Only booting from EMMc and SDcard is supported |
| ~~FORCE_RECOV#~~ | S155 | | ~~I OD CMOS~~ | ~~1.8Vsb~~ | ~~Standby~~ | ~~PU 10K~~<br>- | ~~Driven by OD on Carrier.~~<br>~~Pulled up on module.~~<br><br>~~Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked. Pulled high on the Module. For SOCs that do not implement a USB based Force Recovery functions, then a low on the Module FORCE_RECOV# pin may invoke the SOC native Force Recovery mode – such as over a Serial Port. For x86 systems this signal may be used to load BIOS defaults. Pulled up on Module. Driven by OD part on Carrier.~~ |

| Boot select switch | | | | |
|---|---|---|---|---|
| 1 | 2 | 3 | 4 | BOOT |
| 0 | 1 | 1 | 0 | SD card |
| 0 | 0 | 1 | 0 | SPI |
| 0 | 1 | 0 | 0 | Remote Gbe |
| 1 | 0 | 0 | 0 | eMMC (SoM) |
| 0 | 0 | 0 | 1 | Force Recovery |

**Note**: Boot selector switch is located between the SoM and LAN ports.


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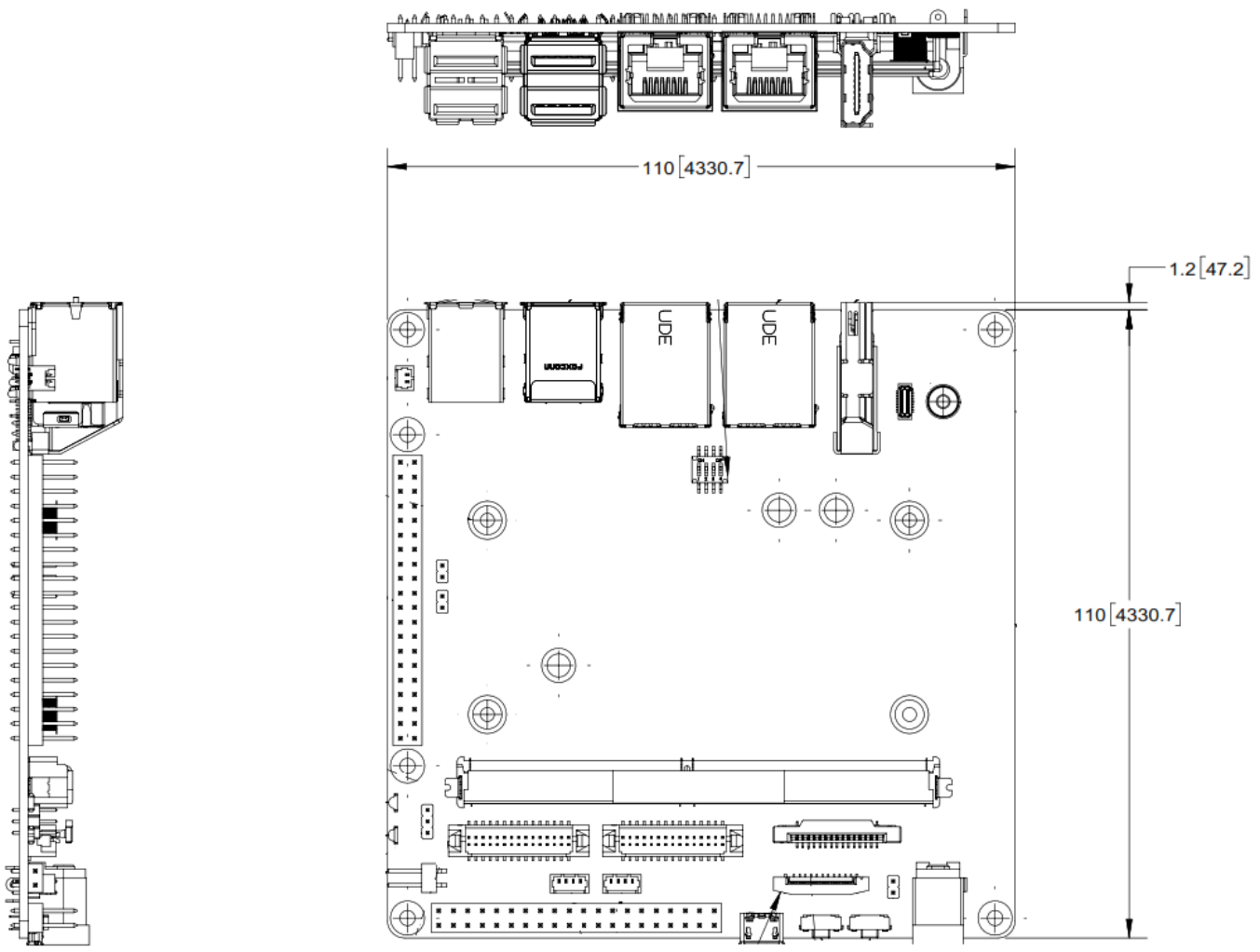
### 5.16.2 Power

| Name | Pin # | Description | I/O Type | Power Rail / Tolerance | PU / PD | Comments |
|---|---|---|---|---|---|---|
| VDD_IN | P147, P148, P149, P150, P151, P152, P153, P154, P155, P156 | Module power input voltage 4.75 min to 5.25V max | P Not defined within Signal Terminolgy Descriptions. Should we define a specific rail? | 3 to 5.25V / 5V | | |
| GND | P2, P9, P12, P15, P18, P32, P38, P47, P50, P53, P59, P68, P79, P82, P85, P88, P91, P94, P97, P100, P103, P120, P133, P142, S3, S10, S16, S25, S34, S47, S61, S64, S67, S70, S73, S80, S83, S86, S89, S92, S101, S110, S119, S124, S130, S136, S143, S158 | Module signal and power return, and GND reference | P Not defined within Signal Terminolgy Descriptions. Should we define a specific rail? | Ground | | |
| ~~VDD_RTC~~ | ~~S147~~ | ~~Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based Lithium cell or Super Cap.~~ | ~~P Not defined within Signal Terminolgy Descriptions. Should we define a specific rail?~~ | [2 to 3.25] / 3.25V | | |

**Note**: The DC jack's input voltage level is19V DC.


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# 6. Mechanical




**Note**: Carrier fixation holes are made for M3 screws. SMARC modules are fixed by M3 screws, with lengths dependent on the heatsink used.


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