LEC-AL

Technical Reference

Low Energy Computer On Module with
Embedded Intel® Atom™, Pentium®, and Celeron® Processors



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Preface

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Revision History

Revision	Date	Description of Change(s)
1.1	3/13/2018	Initial Release
1.2	9/18/2018	Revised GPIO signals in section 3.13 and Table 3-2; changed eSPI support to SPI support; added BMC blink code descriptions to Table 4-47

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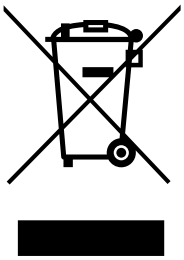
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Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

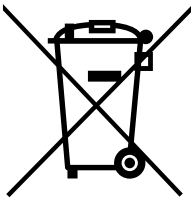
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Battery Labels (for products with battery)









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The following conventions may be used throughout this manual, denoting special levels of information.



This information adds clarity or specifics to text and illustrations.



This information indicates the possibility of ***minor*** physical injury, component damage, data loss, and/or program corruption.



This information warns of possible ***serious*** physical injury, component damage, data loss, and/or program corruption.

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Important Safety Instructions

For user safety, please read and follow all **Instructions**, **WARNINGs**, **CAUTIONs,** and **NOTEs** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

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Table of Contents

Preface ..... **ii**

1 Product Overview **1**
1.1 Description 1
1.2 Features 2
1.3 Block Diagram 4
1.4 Ordering Information 5
1.5 Specifications 5
1.5.1 Physical 5
1.5.2 Electrical 5
1.5.3 Environmental 6
1.5.4 Mechanical 7
1.5.5 Power 8
1.5.6 Cooling 9
1.6 Getting Started 11
1.6.1 Mounting the Heat Spreader to the Module 11
1.6.2 Mounting the Module on the carrier 12
1.6.3 Starting Up the System 13

2 Hardware **15**
2.1 Major Components (ICs) 15
2.2 Connectors, Switches, and LEDs 17
2.3 Component Features 19
2.3.1 CPU 19
2.3.2 SDRAM 19
2.3.3 I210 LAN Controller (I211 controller on some models) 19
2.3.4 BMC 19
2.3.5 LM73 Temperature Sensor 20
2.3.6 PTN3460I eDP-to-LVDS Converter 20
2.3.7 PCA9535A GPIO Expander 20
2.3.8 SMBus Slave Addresses 20
2.3.9 eMMC NAND Flash 20

3 Interfaces **21**
3.1 Display Interfaces 21
3.1.1 18/24-Bit LVDS LCD (Primary Display) 21
3.1.2 DisplayPort++/HDMI (Secondary Display) 22
3.1.3 DisplayPort++ (Tertiary Display) 22
3.2 Camera MIPI-CSI 23
3.2.1 Camera Add-On Card Support 23
3.3 Audio (HDA) 24
3.4 PCI Express (PCIe) 24
3.5 Gigabit Ethernet 24

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3.6 USB Ports 25
3.6.1 USB 2.0 25
3.6.2 USB 3.0 25
3.7 SATA 25
3.8 I2C Bus 25
3.9 SPI 25
3.10 Serial (UART) 25
3.11 I2S 26
3.12 SD/SDIO Interface 26
3.13 GPIO 26
3.14 LPC Debug Interface 26
3.15 SMARC Interface Signals 27
3.16 Debug (DB40) Connector Signals 51

4 Utilities 53
4.1 BIOS Setup 53
4.1.1 Starting the BIOS Setup Utility 54
4.1.2 Main Menu 54
4.1.3 Advanced Menu 57
4.1.4 Chipset Menu 71
4.1.5 Security Menu 84
4.1.6 Boot Menu 85
4.1.7 Save & Exit Menu 86
4.2 SEMA functions 87
4.2.1 Board Specific SEMA functions 88
4.3 Watchdog Timer 89
4.4 Temperature Sensors 89
4.5 Programming Examples 89

Appendix A System Resources 91

Appendix B Technical Support 97

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1 Product Overview

1.1 Description

The LEC-AL Computer-On-Module (COM) combines the SMARC® 2.0 standard with the latest Intel® Atom™ E-Series and Pentium® and Celeron® N-series System-on-Chips (SoCs), providing ideal solutions for low power consumption and high performance requirements. The module provides the high integration, high performance, low power, and ruggedness favored by Internet-of-Things (IoT) applications such as retail transactional clients, digital signage, and in-vehicle infotainment systems.

The LEC-AL module utilizes the latest Intel E-series and N-series SoCs, which are based on the Intel 64 Architecture, the new HD Graphics 500/505 engine, and a faster, 4-vector image processing unit. The SoCs are manufactured on Intel's industry-leading, tri-gate 14nm process, improving system performance by supporting more than 4 GB of both virtual and physical memory. The module primarily targets embedded intelligent systems used in several vertical market segments such as healthcare, industrial controllers and real-time systems, retail systems, edge IOT gateways, in-vehicle infotainment systems, printers, thin clients, industrial and ruggedized tablets, and many others. The LEC-AL supports contemporary, high-bandwidth interfaces such as Ultra HD HDMI, dual-channel LVDS, PCI Express Gen2, Gigabit Ethernet, USB 2.0/3.0, SATA Gen3, enhanced MIPI CSI camera, and a state-of-the-art HD Audio interface. The module generates its own LVDS (18/24bit), TMDS, and Display Port ++ video signals using eDP and DDI output from the SoC.

Two SPI Flash chips implement a fail-safe BIOS, allowing the user to boot the module even if current BIOS settings have corrupted the system.

Under the management of the BMC chip (Board Management Controller), the SEMA utility (Smart Embedded Management Agent) provides system control, security, and failure protection—counting, monitoring, and measuring hardware and software events, and using the SMBus to send corrective commands to the SoC.

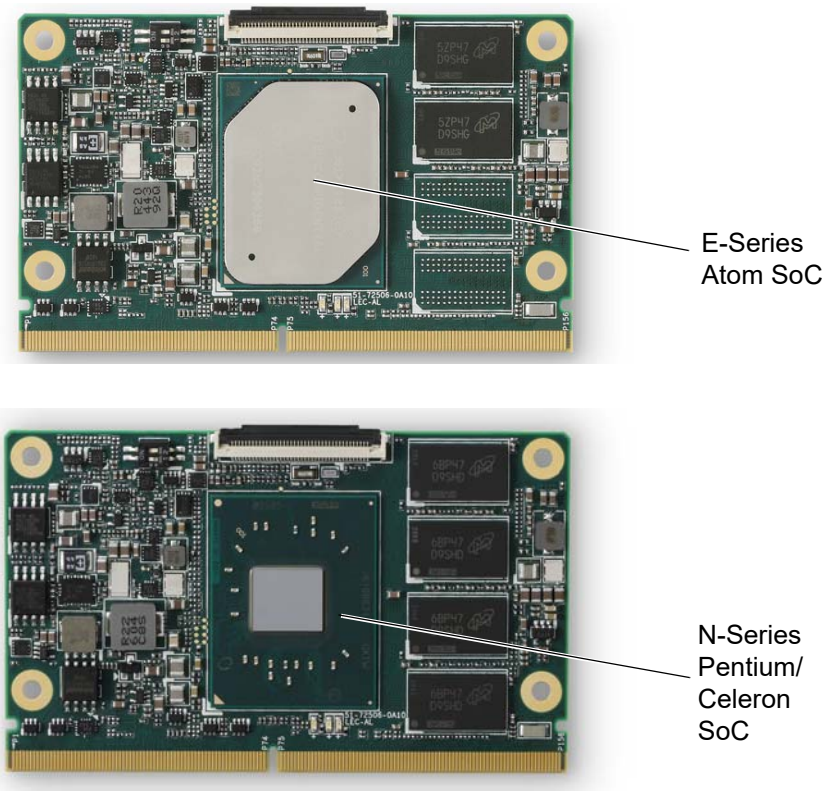


Figure 1-1: Overview of LEC-AL with Intel E-Series and N-Series SoCs

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1.2 Features

CPU

Intel® Atom™ E39xx series and Pentium® N4200 and Celeron® N3350, x86 dual-core or quad-core SoCs (System on Chips) with integrated memory, graphics, and I/O.

- E3950 12W TDP, Atom Quad-Core; 2.0GHz burst freq; up to 1866 MT/s; 650MHz graphics burst freq
- E3940 9.5W TDP, Atom Quad-Core; 1.80GHz burst freq; up to 1866 MT/s; 600MHz graphics burst freq
- E3930 6.5W TDP, Atom Dual-Core; 1.80GHz burst freq; up to 1866 MT/s; 550MHz graphics burst freq
- N4200 6W TDP, Pentium Quad-Core; 2.5GHz burst freq; up to 1866 MT/s; 750MHz graphics burst freq
- N3350 6W TDP, Celeron Dual-Core; 2.4GHz burst freq; up to 1866 MT/s; 650MHz graphics burst freq

NOTE: Other CPU SKUs can be made available on request.

- Memory
  - Up to 8GB non-ECC, unbuffered soldered, DDR3L
  - 1866MHz
  - Dual channel
- Interface Standard
  - SMARC, board-to-board, Rev 2.0
- SATA
  - One 6Gb/s, Gen 3 port
  - Advanced Host Controller Interface (AHCI)
- USB
  - Five USB 2.0 host ports
  - One USB 2.0 client port
  - Two USB 3.0 host ports
- Ethernet
  - Single-port, gigabit Ethernet controller
  - Integrated GbE MAC, PHY, and MDI ports
  - 10T/100TX/1000T signals using the PCIe x1 bus
- Serial UART
  - Two high-speed, 2-wire port
  - Two high-speed, 4-wire port
  - Base frequency 50MHz
- I2C
  - One I2C bus
  - Four I2C ports
  - One SMBus
- SPI
  - One internal SPI controller
  - Two SPI flash devices for BIOS storage
  - One SPI interface routed to the SMARC connector

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- Video
  - LVDS (Primary) or eDP (Primary BOM option)
  - DisplayPort++/HDMI (Secondary)
  - DisplayPort++ (Tertiary)
- Audio
  - One HDA (High Definition Audio) interface (through HDA/I2S2 pins)
  - One internal HDA controller on the SoC
  - Multi-channel audio stream support
  - 32-bit sample depth
  - Sample rate up to 192 kHz
  - One LPE (Low Power Engine) I2S interface
- Camera
  - Two MIPI-CSI camera interfaces
  - Camera, CSI0 (2 lanes)
  - Camera, CSI1 (4 lanes)

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1.3 Block Diagram

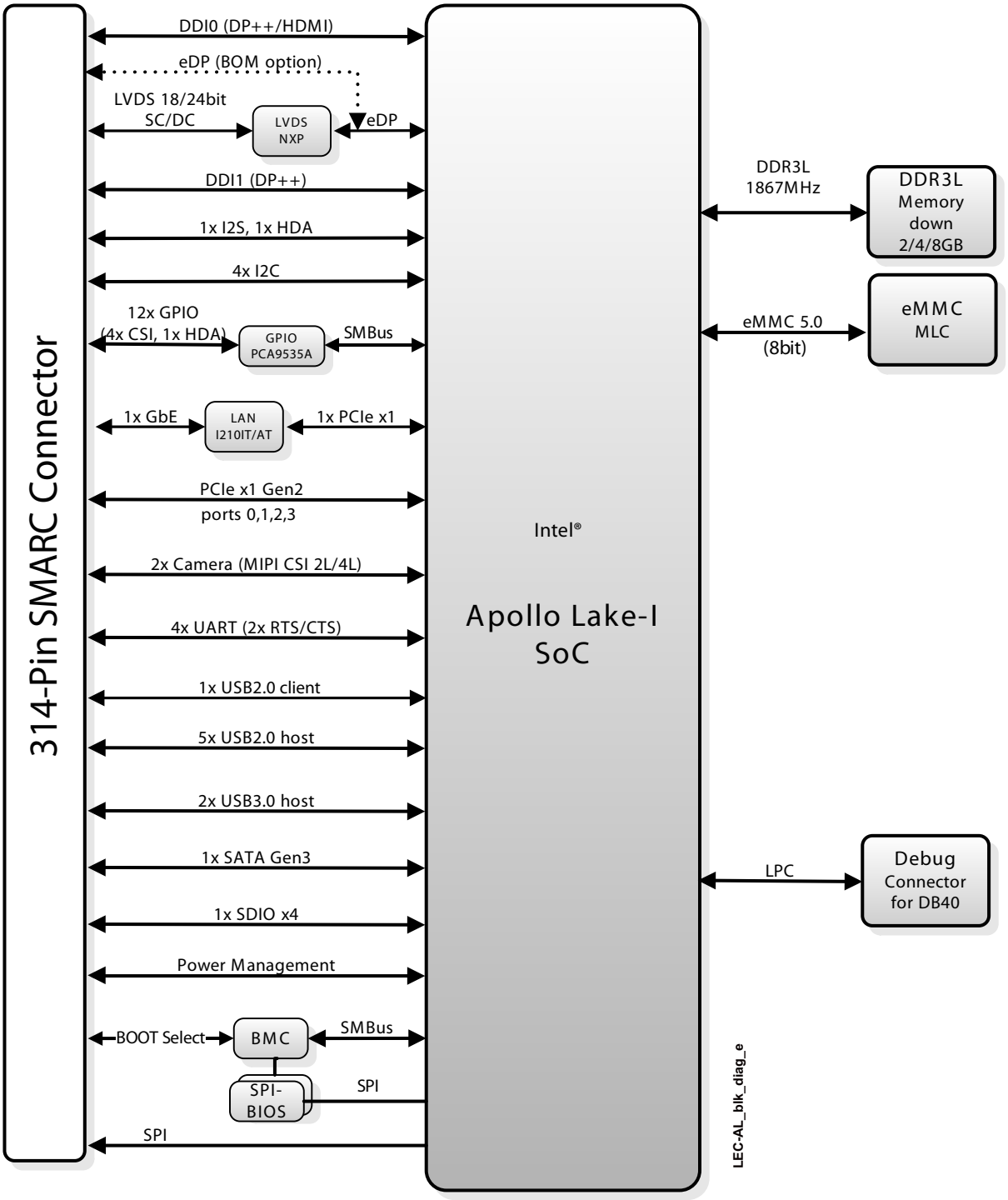


Figure 1-2: LEC-AL functional block diagram

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1.4 Ordering Information

Table 1-1: LEC-AL Standard Models (others on request)

Model Number	Description
LEC-AL-E3930-2G-8G-ER	SMARC short size module with Intel Atom E3930, dual core, 2GB DDR3L, 8GB eMMC, -40°C to 85°C
LEC-AL-E3940-4G-32G-ER	SMARC short size module with Intel Atom E3940, quad core, 4GB DDR3L, 32GB eMMC, -40°C to 85°C
LEC-AL-E3950-8G-32G-ER	SMARC short size module with Intel Atom E3950, quad core, 8GB DDR3L, 32GB eMMC, -40°C to 85°C
LEC-AL-N3350-4G-8G-CT	SMARC short size module with Intel Celeron N3350, dual core, 4GB DDR3L, 8GB eMMC, 0°C to 60°C
LEC-AL-N4200-8G-32G-CT	SMARC short size module with Intel Pentium N4200, quad core, 8GB DDR3L, 32GB eMMC, 0°C to 60°C
LEC-AL-HS1	Heat spreader for LEC-AL-E3930 / E3940 / E3950
LEC-AL-HS2	Heat spreader for LEC-AL-N3350 / N4200

1.5 Specifications

1.5.1 Physical

Table 1-2 lists the physical dimensions of the module.

Table 1-2: Weight and Footprint Dimensions

Dimension	Measurement	
Weight	0.020 kg	Overall height is measured from the upper board surface to the top of the highest permanent component on the upper board surface. This measurement does not include the cooling solution.
Height (overall)	2.29mm	
Board thickness	1.20mm	
Width	50.00mm	
Length	82.00mm	

1.5.2 Electrical

Table 1-3 specifies the electrical characteristics of the module.

Table 1-3: Electrical Specifications

Parameter	Value
Voltage Input Standard RTC	▶ +3V DC min to +5.25V DC max, =/- 50mV ripple ▶ 3.0V, 2.0V to 3.3V (battery), +/- 20mV ripple
Power States	▶ C0, C1, C2 processor power states ▶ S0 (active), S1 (sleep), S2 (extended sleep), S3 (standby [suspend to RAM]), S4 (suspend-to-disk), and S5 (soft-off and wake-on-LAN) system power states

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1.5.3 Environmental

Table 1-4 defines the environmental conditions under which the module is qualified to operate and to be stored.

Table 1-4: Temperature and Humidity

Parameter	Temperature
Temperature	
Standard	▶ 0°C to +60°C
Extended	▶ -40°C to +85°C
Storage	▶ -55°C to 85°C
Humidity	
Operating	▶ 5% to 90% relative humidity, non-condensing
Non-operating	▶ 5% to 95% relative humidity, non-condensing

Table 1-5 provides shock and vibration tests performed on the board.

Table 1-5: Shock and Vibration

Parameter	Result
Shock Test	MIL-STD-202F, Method 213B, Table 213-I, Condition A
Random Vibration Test	MIL-STD-202F, Method 214A, Table 214-I, Condition D

Table 1-6 presents the average times between system failures.

Table 1-6: Mean Time Between Failures

Parameter	Value
MTBF at 40°C	372,124 hrs (according to MIL calculation)
MTBF at 85°C	89,750 hrs (according to MIL calculation)

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1.5.4 Mechanical

Figure 1-3 provides the mechanical dimensions of the LEC-AL.

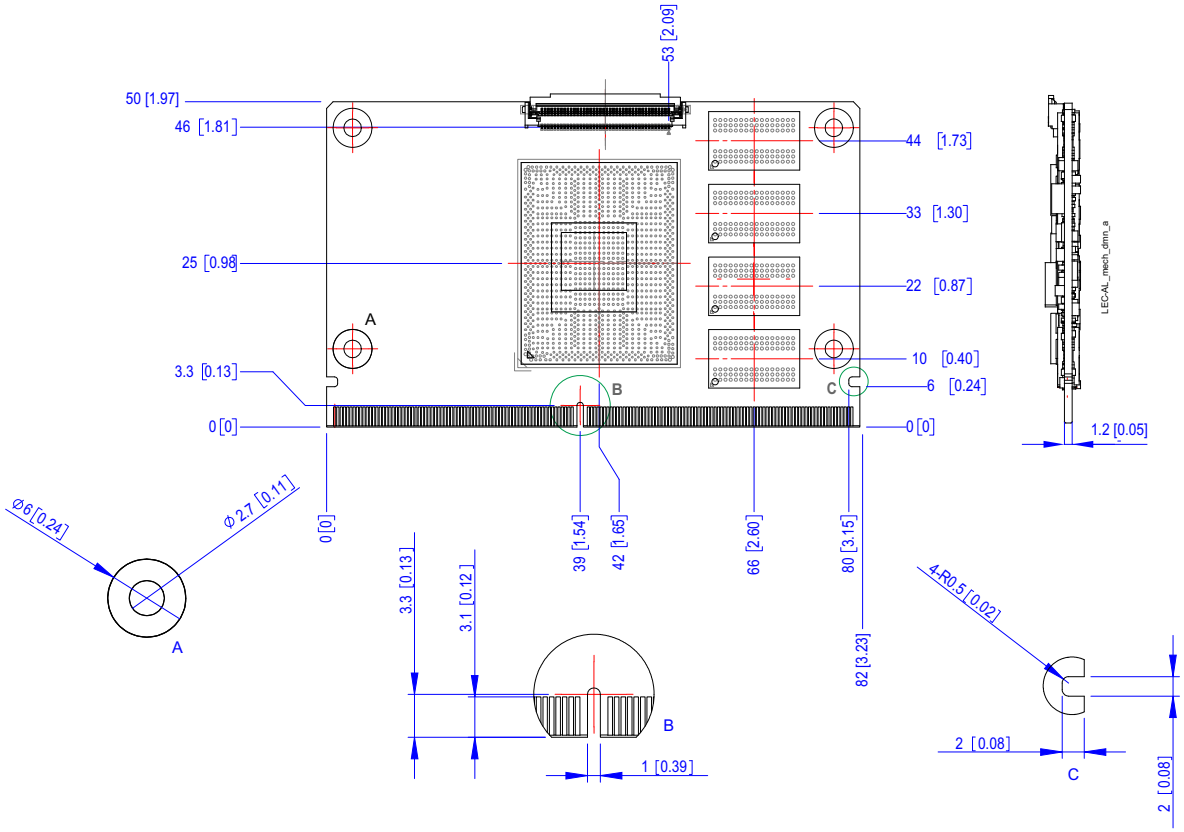


Figure 1-3: Mechanical dimensions (top side)

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1.5.5 Power

Table 1-7 provides the power requirements for this module under certain load configurations.

Table 1-7: Power Supply Requirements

Parameter	12W, E3950 Atom SoC	9W, E3940 Atom SoC	6W, E3930 Atom SoC	6W, N4200 Pentium SoC	6W, N3350 Celeron SoC
Input Type	Regulated DC voltage	Regulated DC voltage	Regulated DC voltage	Regulated DC voltage	Regulated DC voltage
Typical Idle Current and Power (EIST enabled; 250GB SSD; under Windows 7)	0.52A (2.60W) @ 5V	0.52A (2.60W) @ 5V	0.51A (2.55W) @ 5V	0.53A (2.65W) @ 5V	0.51A (2.55W) @ 5V
Typical Operating Mode Current and Power (EIST enabled; 250GB SSD; under Windows 7)	3.10A (15.50W) @ 5V	2.10A (10.50W) @ 5V	1.80A (9.00W) @ 5V	0.56A (2.80W) @ 5V	1.72A (8.60W) @ 5V
Maximum Operating Mode Current and Power (EIST enabled; 250GB SSD; under Windows 7; Intel TAT tool v5.0.1022)	5.20A (26.00W) @ 5V	3.10A (15.50W) @ 5V	1.80A (9.00W) @ 5V	1.85A (9.25W) @ 5V	1.71A (8.55W) @ 5V
System S3 mode (EIST enabled; 250GB SSD; under Windows 7)	0.12A (0.60W) @ 5VSB	0.07A (0.35W) @ 5VSB	0.10A (0.50W) @ 5VSB	0.11A (0.55W) @ 5VSB	0.11A (0.55W) @ 5VSB
System S4 mode (EIST enabled; 250GB SSD; under Windows 7)	0.08A (0.40W) @ 5VSB	0.05A (0.25W) @ 5VSB	0.08A (0.40W) @ 5VSB	0.08A (0.40W) @ 5VSB	0.07A (0.35W) @ 5VSB
System S5 mode with ECO disabled (EIST enabled; 250GB SSD; under Windows 7)	0.08A (0.40W) @ 5VSB	0.05A (0.25W) @ 5VSB	0.07A (0.35W) @ 5VSB	0.08A (0.40W) @ 5VSB	0.07A (0.35W) @ 5VSB

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1.5.6 Cooling

The LEC-AL is designed to operate at its maximum CPU speeds and requires a thermal solution to cool the CPU. ADLINK offers two heat spreaders for cooling. Each LEC-AL module requires one of the two heat spreaders (either the LEC-AL-HS1 or the LEC-AL-HS2) depending on the featured CPU.



Make sure to use the specified heat spreader for the selected module. Proper cooling for the module is not guaranteed if you do not use the correct heat spreader.

The heat spreader is not a complete cooling solution and requires another form of cooling, such as a fan to keep the ICs within their operating temperature specifications.

The heat spreader provides a neutral plane to connect a custom heatsink solution designed with a custom enclosure. If a custom heatsink is used, it is recommended to mount it to the ADLINK heat spreader. This facilitates future module upgrades without the need to re-design the custom heatsink.

Refer to the following two subsections (1 and 2) for descriptions of the two ADLINK heat spreaders.

1. The LEC-AL-HS1 heat spreader must be used for the LEC-AL-E3950/40/30 modules. As can be seen in Figure 1-1, the Intel Atom E39xx SoCs come with mounted Intel heat spreaders, which look like metallic lids and add 2mm to the heights of the SoCs. The LEC-AL-HS1 heat spreader is designed for the extra heights of these SoCs. See Figure 1-4 for a mechanical overview of the LEC-AL-HS1 heat spreader.

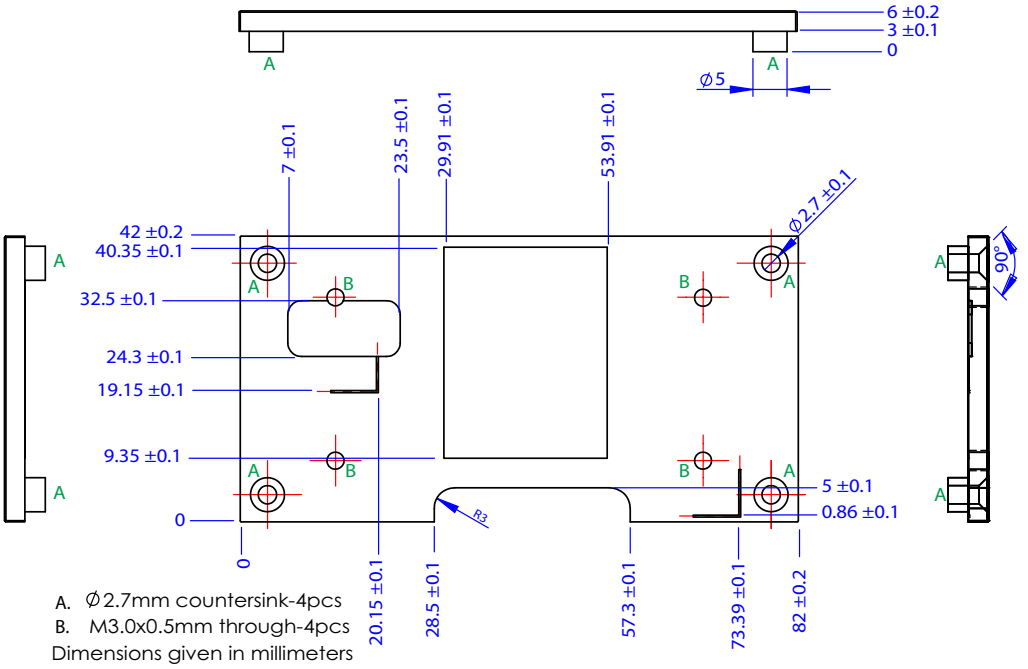


Figure 1-4: LEC-AL-HS1 Heat Spreader Mechanical Overview.

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2. The LEC-AL-HS2 heat spreader is designed for the LEC-AL-N4200/N3350 modules and must be used for these lower profile SoCs. As can be seen in Figure 1-1, the Intel Pentium and Celeron N4200/N3350 SoCs come without mounted Intel heat spreaders, and their profiles are 2mm lower than the Atom E39xx SoCs. See Figure 1-5 for a mechanical overview of the LEC-AL-HS2 heat spreader.

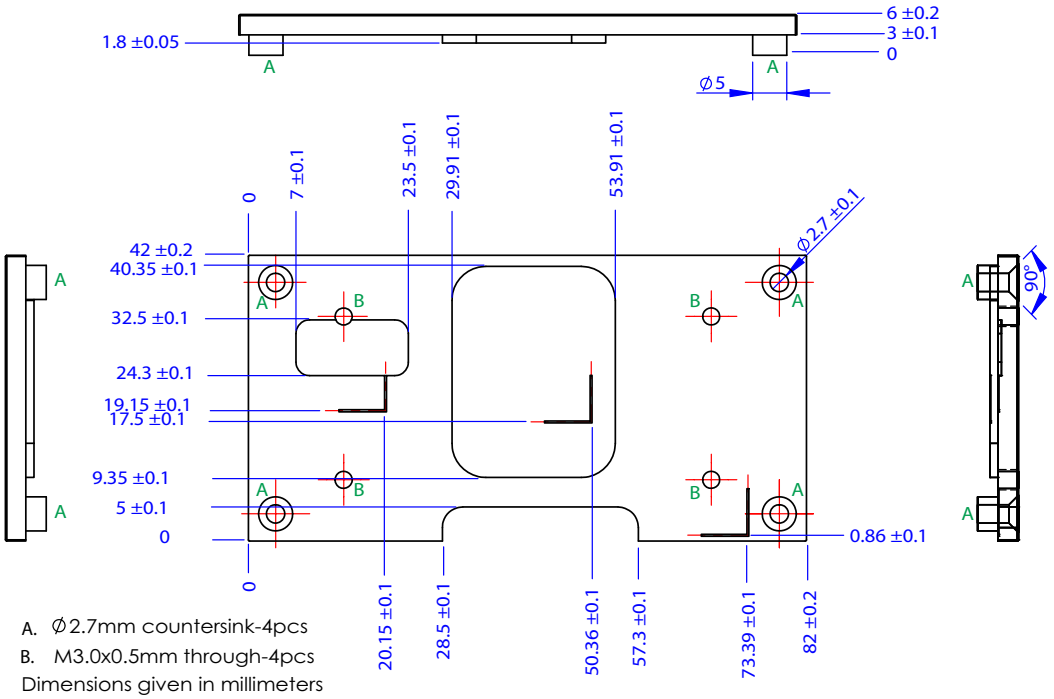


Figure 1-5: LEC-AL-HS2 Heat Spreader, Module Assembly.

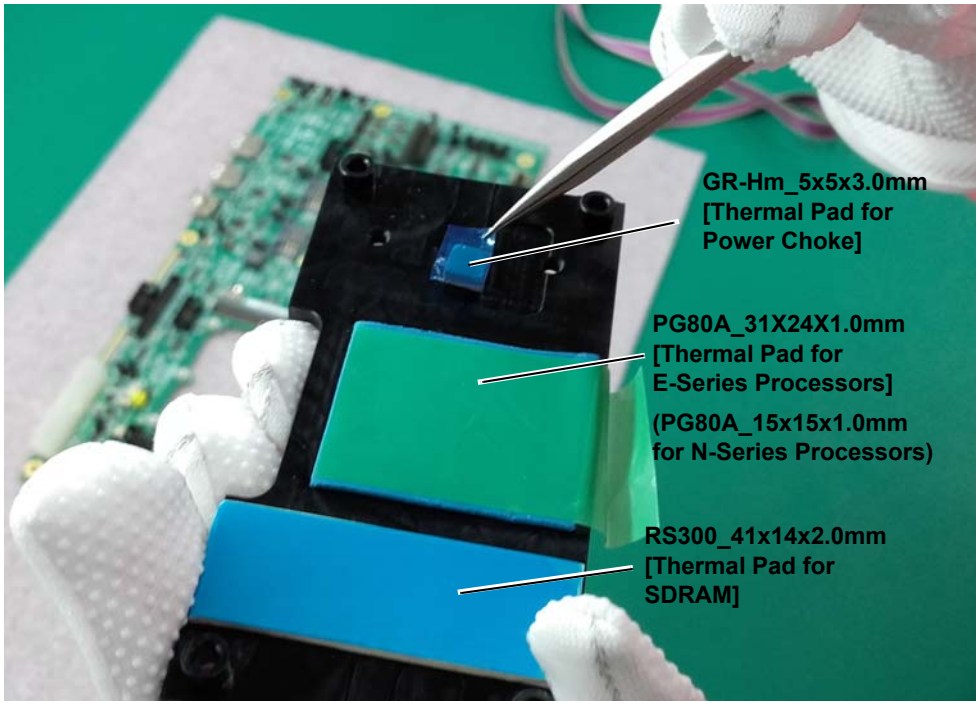
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1.6 Getting Started

This section provides the most efficient procedures to assemble and start up your system.

1.6.1 Mounting the Heat Spreader to the Module

Use the following two steps to mount the heat spreader to the LEC-AL.



Remove the protective membranes from the thermal pads on the heat spreader.

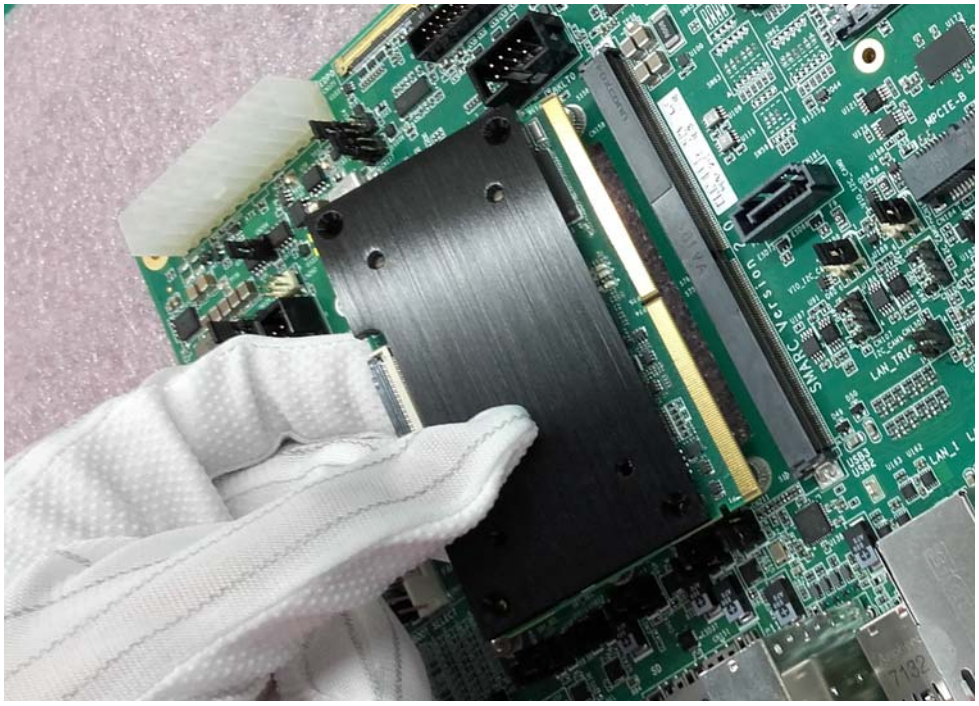


Lay the heat spreader on the top side of the module so that the thermal pads on the heat spreader cover their respective components on the module. See previous photo for locations and descriptions of thermal pads.

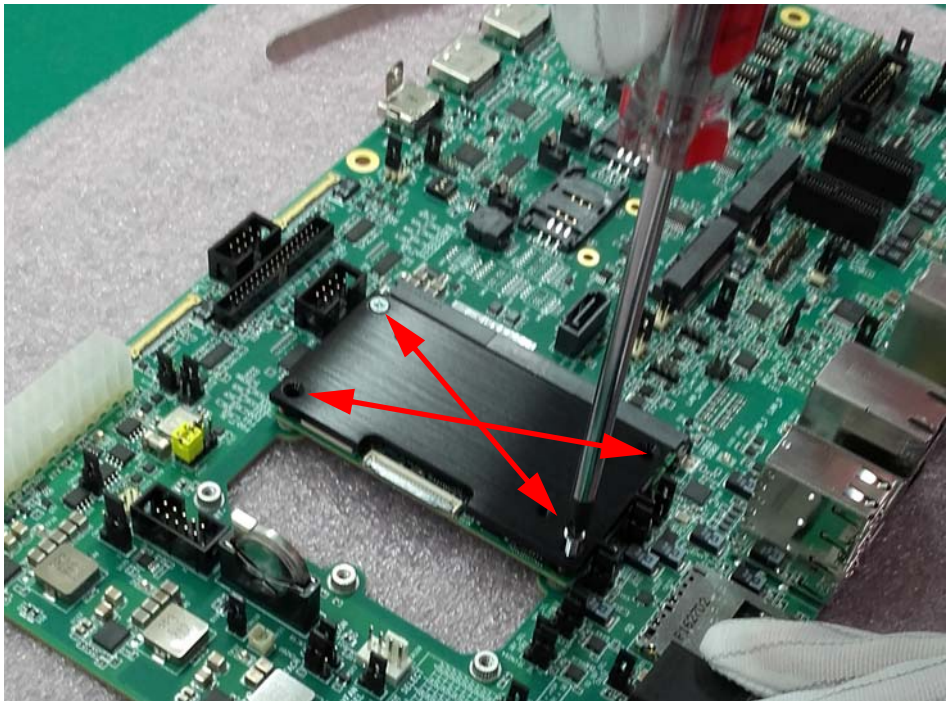
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1.6.2 Mounting the Module on the carrier

Mount the LEC-AL to the carrier as illustrated in the following two photos.



Insert the SMARC edge connector on the module into the SMARC socket on the carrier.



Install four M2.5x11 mounting screws using a diagonal installation sequence.

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1.6.3 Starting Up the System

Use the following section as a guideline to connect peripherals to the carrier board and to power up your system.



Be sure to observe the EMC security measures. Make sure you are always at the same potential as the module.



Never connect or disconnect peripherals like HDDs while the power supply is connected and switched on.

Use the cable set provided in the ADLINK Technology starter kit to connect the LEC-AL to a display. Connect a USB keyboard or mouse to the carrier. Use the SATA cable to connect the hard disk. Make sure that the pins match their counterparts correctly and are not twisted. If you plan to use additional peripherals, connect them to the appropriate headers or connectors on the carrier.

Connect a power supply to the power connector on the carrier and switch on the power.



Observe the minimum voltage values for the standard peripherals mentioned. For additional peripherals, make sure enough power is available. The system will not work if there is not enough supply current for all your devices.

The display shows the BIOS messages. If you want to change the standard BIOS settings, press the <DEL> key during the boot process to enter the BIOS setup menus. See Chapter 4 for setup details.

If you need to load the BIOS default values, they can be automatically loaded at boot time.

Depending on the installed operating system, the LEC-AL boots from eMMCs, USB sticks, hard disks, or µSD-Cards. Provided that any of these is connected and contains a valid operating system image, the display then shows the boot screen of your operating system.

The LEC-AL needs adequate cooling measures depending on the desired operating temperature range. Using the board without cooling could permanently damage the board.

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2 Hardware

This chapter describes the major integrated circuits (ICs) and interface connectors and headers on the module. The third section of this chapter further describes the major ICs and their roles on the LEC-AL.

2.1 Major Components (ICs)

This section illustrates and describes the major integrated circuits on the LEC-AL. Figure 2-1 and Figure 2-2 show the locations of the major ICs. Table 2-1 lists and specifies the ICs, including a brief description, manufacturer part and model numbers, and function of each IC.

Key:
U1 - CPU
U15 - BIOS 0
U16 - BIOS 1
SU1 - Temperature Sensor
MD1 - DDR3L SDRAM (Channel 2)
MD3 - DDR3L SDRAM (Channel 2)
MD6 - DDR3L SDRAM (Channel 2)
MD8 - DDR3L SDRAM (Channel 2)

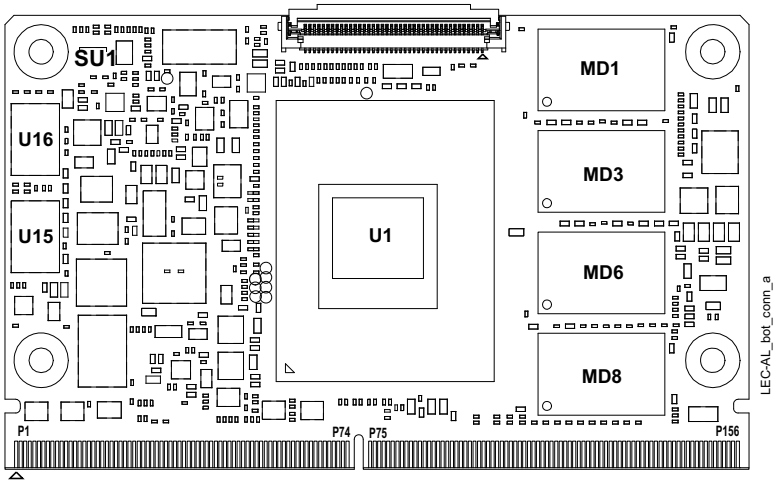


Figure 2-1: Component Locations (Top Side)

Key:
BU1 - BMC
GBU1 - eDP to LVDS Bridge
LU1 - GbE Controller
MD2 - DDR3L SDRAM (Channel 1)
MD4 - DDR3L SDRAM (Channel 1)
MD5 - DDR3L SDRAM (Channel 1)
MD7 - DDR3L SDRAM (Channel 1)
O2U1 - GPIO Expander
U204 - eMMC, NAND Flash

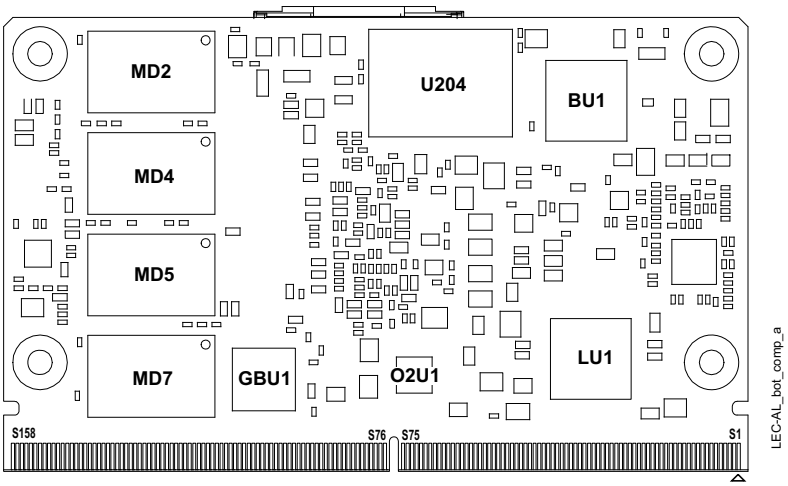


Figure 2-2: Component Locations (Bottom Side)

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Table 2-1: Major Integrated Circuit Descriptions and Functions

Chip Type	Mfg.	Model	Description	Function
CPU (U1)	Intel part numbers	• E3950 Atom (quad-core, 12W, 2.0GHz burst frequency) • E3940 Atom (quad-core, 9.5W, 1.80GHz burst frequency) • E3930 Atom (dual-core, 6.5W, 1.80GHz burst frequency) • N4200 Pentium (quad-core, 6W, 2.5GHz burst frequency) • N3350 Celeron (dual-core, 6W, 2.4GHz burst frequency)	E-Series and N-Series, 14nm SoC(s) (System on Chips) with Intel Architecture	Integrates Processor Core, Graphics / Memory Hub, and I/O Hub
Ethernet Controller (LU1 on bottom side; see Figure 2-2)	Intel	WGI210IT SLJXT (I211 version will be used on certain models)	Single-port Gigabit Ethernet controller	Integrates GbE MAC, PHY, and SGMII/SerDes to enable 10T/100TX/1000T Ethernet signals using the PCIe x1 bus
Embedded DisplayPort-to-LVDS Converter (GBU1)	NXP	PTN3460	Embedded DisplayPort (eDP) to LVDS bridge device that enables connectivity between an embedded DisplayPort (eDP) source and an LVDS display panel.	Processes the incoming embedded DisplayPort (eDP) stream, performs eDP to LVDS protocol conversion, and transmits processed stream in LVDS format.
BMC [Board Management Controller] (BU1)	Texas Instruments	TM4C123GH6ZRB	Micro controller for board functions including Watchdog Timer, LVDS control, system control, and failure protection	Controls dual BIOS and SEMA API through the SMBus
GPIO Expander (O2U1)	NXP/ Philips	PCA9535A	Module providing 16 bits of GPIO expansion for I2C/SMBus applications	Provides additional digital control lines
Temperature Sensor - CPU (SU1 on bottom side; see Figure 2-2)	Texas Instruments	LM73	Digital-output temperature sensor	Measures its own temperature and the temperature of the CPU thermal diode and provides temperature correction with fan speed control.
SPI Flash (U15 and U16)	Macronix	MX25L12835FM2I-10GTR	Serial Peripheral Interface Flash Memory chip (for firmware)	Stores BIOS 0 and BIOS 1 in Flash Memory

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Table 2-1: Major Integrated Circuit Descriptions and Functions (Continued)

Chip Type	Mfg.	Model	Description	Function
eMMC, NAND Flash (U204 on bottom side; see Figure 2-2)	Micron	• MTFC4GACAJCN-1M WT • MTFC4GACAJCN-4M IT	MultiMediaCard Controller and NAND Flash Memory up to 64GB	Provides communication and mass data storage capabilities
DDR3L SDRAM (MD1, MD2, MD3, MD4, MD5, MD6, MD7, MD8 [MD2, MD4, MD5, and MD7 on bottom side; see Figure 2-2])	Micron	NOTE: The following memory chips are aligned with their matching configurations in the column to the right: • MT41K126M16TW-107 (2GB model) • MT41K256M16TW-107 (4GB model) • MT41K512M16TW-107 (4GB model) • MT41K1G4I (8GB model) NOTE: The above DDR3L devices are subject to change per required memory configurations.	On-board DDR3L, 1.35V, non-ECC system memory • 4Gb, 4x 126Mx16 • 4Gb, 8x 256Mx16 • 8Gb, 4x 512Mx16 • 8Gb, 8x 1Mx16	Provides high-speed data transfer

2.2 Connectors, Switches, and LEDs

This section illustrates and describes the connectors, switches, and LEDs on the LEC-AL. Figure 2-1 and Figure 2-2 show the locations of these user interface components. Table 2-1 lists and specifies these components, including the PCB reference designator, board-side location, and description of each component.

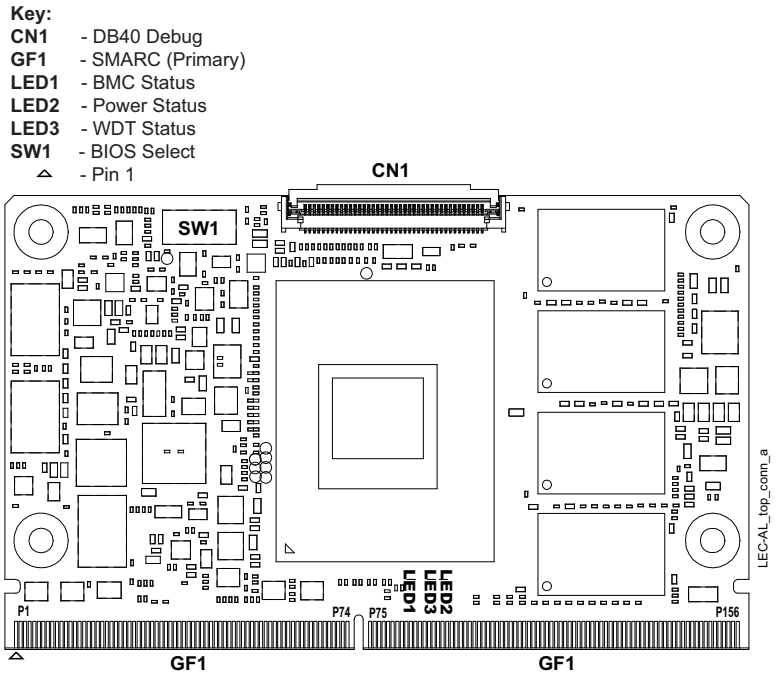


Figure 2-3: Connector Locations (Top Side)

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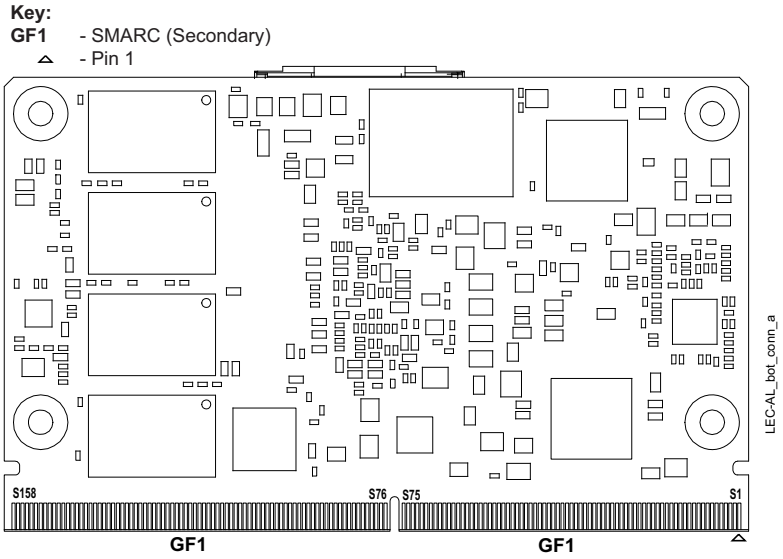
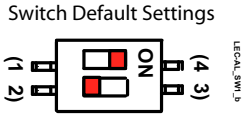


Figure 2-4: Connector Locations (Bottom Side)

Table 2-2: Module Connector Description

Connector#	Board Access	Description
CN1	Top	40-pin, DB40 Front-Flip connector for debug card (Molex, 502790-4091)
GF1 - SMARC Primary and Secondary (P and S)	Top/ Bottom	314-pin, MXM edge connector for Audio, Video, Camera, and I/O functions
LED1	Top	Blue LED indicating system status activities for HW Reset, SW Reset, Power Up, Power Down, Reset Button, and Power Button
LED2	Top	Green LED for Power On in S0 state, controlled by SLP_S3#
LED3	Top	Red LED for Watchdog time out, driven by SEMA and cleared by software or reset button
SW1	Top	4-pin dip switch for • Setting BIOS Boot (1=Boot from SPI1, 4=Boot from SPI0 [default]) • Selecting BIOS Mode (2=Failsafe BIOS [default], 3=Normal BIOS) 

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2.3 Component Features

This section further describes the supported features of the LEC-AL major, on-board hardware components.

2.3.1 CPU

The LEC-AL product family offers the following versions of the Intel Pentium and Celeron N-Series and Atom E-series, System-on-Chips (SoC): the N4200 Pentium (Quad Core with Gfx 800MHz), the N3350 Celeron (Dual Core with Gfx 640MHz), the E3950 Atom (Quad Core with Gfx 600MHz), and the E3940 Atom (Quad Core with Gfx 600MHz). The LEC-AL product family also includes a lower-cost alternative: the E3930 Atom with Gfx 320MHz. N-Series and E-series SoCs feature the Intel 64 Architecture and are manufactured based on Intel's 14-nanometer technology. Refer to the N-series and E-series SoC data sheets on the Intel web site. Other CPU SKUs are available on request.

2.3.2 SDRAM

The LEC-AL employs up to two channels of 64-bit DDR3L on-board memory. Up to eight SDRAM memory chips provide up to 32Gb of low-voltage non-ECC, unbuffered system memory. Two channels are used with an eight chip configuration. Only one channel is used with a four chip configuration. Refer to the MT41K SDRAM data sheet on the Micron web site.

Depending on the DRAM chips featured on the module, the following total DRAM capacities are supported:

- 4x 126M16 = 2 GB
- 8x 256M16 = 4 GB
- 4x 512M16 = 4 GB
- 8x 1M16 = 8 GB

2.3.3 I210 LAN Controller (I211 controller on some models)

The Intel I210 provides a single-port controller that supports GbE functionality using the high-speed PCIe standard, v2.1 (2.5GT/s). The I210 features a fully-integrated Media Access Control (MAC) and a Physical Layer (PHY), which enable 1000BASE-T implementations such as rack-mounted or pedestal servers in add-on NIC or LAN-on-Motherboard (LOM) designs. Other implementations include blade servers such as LOMs or mezzanine cards as well as embedded applications such as switch add-on cards and network appliances. Additionally, the I210 integrates an SGMII/SerDes port, which allows MAC-to-MAC blade server connections or MAC-to-external PHY connections. Refer to the Intel I210 Ethernet Controller data sheet on the Intel web site.

The Intel I211 provides a single-port controller that supports GbE functionality using the high-speed PCIe standard, v2.1 (2.5GT/s). The I211 features an integrated PHY, which enables 1000BASE-T implementations such as rack-mounted or pedestal servers in add-on NIC or LAN-on-Motherboard (LOM) designs. Other implementations include blade servers such as LOMs or mezzanine cards as well as embedded applications such as switch add-on cards and network appliances. Refer to the Intel I211 Ethernet Controller data sheet on the Intel web site.

2.3.4 BMC

The Board Management Controller (BMC) is a micro-controller chip that transmits and receives data to and from the SEMA, BIOS, and debug utilities—monitoring system performance, behavior, and diagnostics at transfer speeds up to 3.33Mbps at 400KHz. The BMC queries components on the board for data related to temperature, power-supply voltage and current, power sequencing, logistics and forensics, flat panel control, I2C bus control, user flash, Watchdog Timer, and fan control. Refer to the Texas Instruments web site for more information on the TM4C123GH6ZRB micro-controller.

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2.3.5 LM73 Temperature Sensor

The temperature sensor operates over a wide temperature range (-40°C to +150°C) with a 14-bit mode maximum resolution. Programmed to the BMC and controlled through the SEMA user interface, the temperature sensor monitors system temperatures and issues alerts, time outs, resets, and shutdowns, protecting the system as it approaches temperature limits. For more information on the LM73 Temperature Sensor, refer to the data sheet on the Texas Instruments website.

2.3.6 PTN3460I eDP-to-LVDS Converter

The PTN3460I supports single-bus or dual-bus LVDS signalling with color depths of 18 bits per pixel or 24 bits per pixel and pixel clock frequency up to 112MHz. LVDS data packing can be done either in VESA or JEIDA formats. Also, the DP AUX interface transports I2C-over-AUX commands and supports EDID-DDC communication with an LVDS panel. To support panels without EDID ROM, the PTN3460 can emulate EDID ROM behavior, avoiding specific changes in system video BIOS. Find more details on the NXP website.

2.3.7 PCA9535A GPIO Expander

The PCA9535A is a 24-pin device that provides 16 bits of General Purpose parallel Input/Output (GPIO) expansion for I2C-bus/SMBUS applications. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output register. The polarity of the read register can be inverted with the Polarity Inversion register. The operating power supply voltage range of the PCA535A is 1.65V to 5.5V. Find more details on the NXP website.

2.3.8 SMBus Slave Addresses

Table 2-3 lists the corresponding slave addresses of the devices on the SMBus.

Table 2-3: SMBus Slave Addresses

Address (HEX)	Function	Device
(40)	GPIO	PCA9535A
(50)	BIOS / SEMA	BMC
(A0)	DDR3L Channel A	DDR3L memory
(A4)	DDR3L Channel B	DDR3L memory
(92)	Temperature Sensor	LM73

2.3.9 eMMC NAND Flash

The Intel SoC supports one single, 8-bit eMMC interface, which can be used to support the onboard eMMC NAND flash device. Select the eMMC NAND flash as the boot device from the carrier board.

The module supports NAND chips with capacities from 4GB to 16GB. The default capacity is 8GB. Refer to the MTFC4GACAJCN data sheets on the Micron website.

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3 Interfaces

This section provides descriptions of the interfaces and signals within the SMARC P-S (Primary-Secondary) connector. Refer to the SMARC 2.0 specification at: http://www.sget.org for definitions of the SMARC interfaces. The SMARC P-S (Primary-Secondary) connector provides the following interfaces:

- Display
- Camera
- HD Audio
- PCI Express (PCIe)
- Gb Ethernet
- USB 2.0
- USB 3.0
- SATA
- I2C
- SPI /eSPI
- Serial UART
- I2S (Audio)
- SD/SDIO
- GPIO

NOTE: ADLINK Technology, Inc. only supports the features/ options tested and listed in this manual. The main chips used in the LEC-AL may provide more features or options than are listed for the LEC-AL, but some of these features or options are not supported on the module and will not function as specified in the chip documentation.

3.1 Display Interfaces

The LEC-AL supports three independent display interfaces, in parallel. This section describes all three interfaces including the standard and optional configurations for each.

3.1.1 18/24-Bit LVDS LCD (Primary Display)

The LVDS interface is connected to the eDP port of the SoC, and the translation is made by the eDP-to-LVDS converter. The standard LEC-AL configuration supports a single or dual channel LVDS interface (channel A = **S125-S138**; channel B = **S108-S121**) with a maximum resolution of 1920x1200 pixels at 60Hz. The interface supports color depths of 18-bit or 24-bit, which can be set through the Data Format and Color Depth settings of the BIOS setup's Advanced>Graphics Configuration menu. Refer to the NXP PTN3460I, eDP-to-LVDS converter datasheet. See the LEC-AL display interface diagram in Section 3.1.3.

NOTE: As a BOM option, the NXP eDP-to-LVDS converter can be removed, allowing the native eDP signal to be used with an appropriate carrier board and display.

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3.1.2 DisplayPort++/HDMI (Secondary Display)

The second digital display interface provides Dual-Mode DisplayPort (DisplayPort++) as the default operation on the SMARC HDMI pins (**P92-P106**). These signals originate from the DDI0 port of the SoC. The standard LEC-AL display configuration supports DP++. An optional version of the board provides HDMI (TMDS) as the secondary display, requiring separate order numbers for the module and the carrier. The secondary display interface provides the following features:

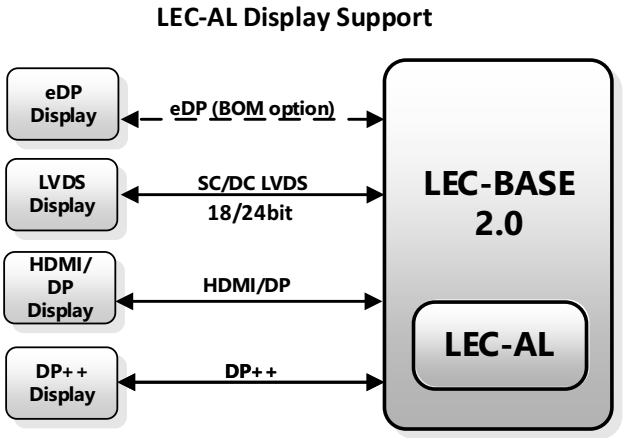
- 4 DisplayPort Data pairs
- 1 HDMI Clock pair (option)
- 3 HDMI Data pairs (option)
- DP and HDMI Service signals
- DP++ resolutions up to 4096x2160 @ 60Hz
- HDMI resolutions up to 3840x2160 @ 30Hz (option)
- Compliant with the HDMI 1.4b specification
- Compliant with the DP 1.2 specification

3.1.3 DisplayPort++ (Tertiary Display)

A third digital display interface supports DP++ (Dual-Mode DisplayPort) operation and originates from the DDI1 port of the SoC. This implementation uses the SMARC DP0 pins (**S93-S106**) and provides the following features:

- 4 DisplayPort data pairs
- DisplayPort Service signals
- DisplayPort resolutions up to 4096x2160 @ 60Hz
- Compliant with the DisplayPort 1.2a specification

The following diagram represents the standard and optional display interface configurations supported by the LEC-AL when mounted on the LEC-BASE 2.0 carrier.



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3.2 Camera MIPI-CSI

The LEC-AL brings out signals for two MIPI-CSI 2.0 (serial) camera interfaces, one with two data lanes (CSI0) and one with four data lanes (CSI1), supporting up to 1.5Gbp/s of actual pixels. The signal pairs for the **CSI0** interface are routed through SMARC pins **S8/S9**, **S11/S12**, and **S14/S15**. The signal pairs for the **CSI1** interface are routed through SMARC pins **P3/P4**, **P7/P8**, **P10/P11**, **P13/P14**, and **P16/P17**. The following bullets highlight the imaging capabilities of the Camera interface.

- Sensor interface for 2 sensors: x4, x2
- Up to 2 simultaneous sensors
- 24MP 2-D image capture
- Full HD 1080p60 video capture
- RAW 8, 10, 12, 14, RGB444, 565, 888, YUV420, 422, JPEG input formats
- YUV422, YUV420, RAW output formats
- Special features
  - Image and video stabilization
  - Low light noise reduction
  - Burst mode capture
  - Memory to memory processing
  - 3A (Auto Exposure [AE], Auto White Balance [AWB], and Auto Focus [AF])
  - High Dynamic Range (HDR)
  - Multi focus
  - Zero shutter lag



A camera driver is required for each OS.

3.2.1 Camera Add-On Card Support

The LEC-AL SoCs provide two Intel support models for camera add-on cards. The following two bullets identify the two support models.

- Pass-Through Mode with External IPU (supporting only Apollo Lake-I SoCs on Linux) – Intel provides the IPU driver. The user must provide the camera kernel driver for the selected camera module.
- MIPI Driver – The IOTG (Intel Internet of Things Group) is enabling one camera module vendor and three camera module types for longevity support (3+ years.)

ADLINK offers a MIPI-CSI camera add-on card (separate order number). This card is based on the MIPI driver model described above in the second bullet and supports the following Chicony camera modules for E39xx SoCs:

CIFGF18	CIFGF1820005190LH	2 lanes	21 pins 2MP
CJAG824	CJAG82420005190LH	4 lanes	31 pins 8MP
CYAGC27	CYAGC2720005190LH	4 lanes	31 pins 13MP

The ADLINK camera add-on card supports these three camera modules, which are connected through their defined 21-pin or 31-pin connectors.

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3.3 Audio (HDA)

The CPU provides an HDA controller, which communicates over the Intel HDA serial link with internal CODECs on the CPU or external CODECs on the baseboard. HDA signals are brought out through the I2S2/HDA pins on the SMARC connector (**S50-S53**) and are multiplexed with LPE_I2S audio signals. When HDA is active, LPE audio is disabled. Refer to the **Chipset > South Cluster Configuration > HD-Audio Configuration** menu in the BIOS Setup Utility section of Chapter 4. The following list highlights the features of the audio interface.

- Decode: MP3, AAC-LC, HE-ACC v1/2, WMA9, 10, PRO, Lossless, Voice, MPEG layer 2, Real Audio, OggVorbis, FLAC, DD/DD+
- Encode: MP3, ACC-LC, WMA, DD-2channel
- Supports MSI and legacy interrupt delivery
- Support for ACPI D3 and D0 Device States
- Supports up to:
  - 6 streams (three input, three output)
  - 16 channels per stream
  - 32 bits/sample
  - 192KHz sample rate
- 24 MHz HDA_CLK supports:
  - SDO double pumped at 48Mb/s
  - SDI single pumped at 24Mb/s
- Supports 3.3V mode
- Supports optional Immediate Command/Response mechanism

3.4 PCI Express (PCIe)

The CPU features five PCIe x1 ports, and the LEC-AL module uses four of them for the PCIe interface and one of them for the Gigabit Ethernet interface. The PCIe interface supports the PCIe Base Specification 2.0 with a maximum signal rate of 5 GT/s and can be configured to support PCIe edge cards or Express Cards.

3.5 Gigabit Ethernet

The on-board Intel I210IT Ethernet controller uses PCIe x1 (v2.1) bus signals from the CPU to enable 10T/100TX/1000T operation through integrated MAC, PHY, and MDI interfaces. The following bullets highlight the features of the I210IT GbE controller:

- IEEE 802.3az Energy Efficient Ethernet
- IEEE 1588/802.1AS precision time synchronization
- IEEE 802.3Qav traffic shaper
- Interrupt moderation, VLAN support, IP checksum offload
- PCIe OBFF (Optimized Buffer Flush/Fill) for improved system power management
- Four transmit and four receive queues
- RSS and MSI-X to lower CPU utilization in multi-core systems
- ECC - error correcting memory packet buffers
- Wake-On LAN
- NC-SI for increased bandwidth passthrough
- Preboot eXecution Environment (PXE) flash interface
- Jumbo frame support

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3.6 USB Ports

The USB interface originates from two host controllers on the CPU that provide six USB 2.0 host ports (5 standard and 1 client) and two USB 3.0 host ports.



The USB 2.0 OTG interface is brought out through the USB0 port (pins **P60-P64** on the SMARC interface connector). The USB 3.0 ports do not support USB OTG. Enable USB 2.0 OTG support from the Chipset > South Cluster Configuration > USB Configuration menu in the BIOS Setup Utility.

3.6.1 USB 2.0

The USB 2.0 ports use the USB 0-5 pins on the SMARC connector (**P60-P71** [including one ground pin] for USB 0-2; **S68-S69** for USB 3; **S35-S36** for USB 4; and **S59-S60** for USB 5.) Support signals for USB 2.0 include Over-Current Enable 0-3 (**P62**, **P67**, **P71**, **P74**), VBUS Detection (**P63**), and OTG ID (**P64**).

3.6.2 USB 3.0

The USB 3.0 ports use the USB 2-3 pins on the SMARC connector (**S71-S72** and **S74-S75** for USB 2_SSTX and USB 2_SSRX; **S62-S63** and **S65-S66** for USB 3_SSTX and USB 3_SSRX.)

3.7 SATA

The SATA interface provides one GEN3 port, using the SATA pins on the SMARC connector (**P48-P49** and **P51-P52** for SATA_TX and SATA_RX differential pairs.) The interface supports transfer rates up to 6Gb/s.

3.8 I2C Bus

The LEC-AL provides six interfaces through the I2C bus for general purpose signals with operating speeds up to 400kHz. The following table maps the I2C interfaces to their corresponding pins on the SMARC interface connector.

SMARC Pins	I2C Interfaces
P105/P106	HDMI Control
P121/P122	Power Management
S1/S2	Camera 1
S5/S7	Camera 0
S48/S49	General Purpose
S139/S140	LCD

3.9 SPI

The CPU implements two SPI controllers. One SPI controller connects to two SPI flash devices on the module and to the DB40 connecter. The second SPI controller supports SPI devices on the carrier through the SMARC (MXM3) connector pins (**P54-P58**).

3.10 Serial (UART)

The LEC-AL provides four serial interfaces: two high-speed, 4-wire ports with TX/RX and RTS#/CTS# signals and two 2-wire ports (with TX/RX only.)

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3.11 I2S

The SMARC connector provides five pins for an I2S audio interface, typically used for digital audio and other modest bandwidth functions. The I2S interface is brought out through the I2S pins on the SMARC connector (**S39-S42**). The voltage level of the I2S interface is 1.8V.

3.12 SD/SDIO Interface

Four parallel data lines comprise the SD/SDIO 3.0 (4bit) interface, supporting SD Card sockets.

3.13 GPIO

The LEC-AL provides 12 GPIO signals from the CMOS device on the module. The GPIO signals can be utilized for General Purpose IO interfaces as well as HDA Reset, Power Management Out, and Tachometer In functions. Table 3-1 provides the functions of the GPIO signals.

Table 3-1: GPIO Default Settings

SMARC Connector Pin	Function
P108	GPIO0
P109	GPIO1
P110	GPIO2
P111	GPIO3
P112	HDA_RST#
P113	BMC_PWM_OUT
P114	BMC_TACHIN
P115	GPIO7
P116	GPIO8
P117	GPIO9
P118	GPIO10
P119	GPIO11

NOTE: The # symbol indicates the signal is Active Low.

3.14 LPC Debug Interface

A 40-pin, front flip, DB40 connector allows access to the system to debug and update the BIOS, BMC, and OS code. (Refer to “Debug (DB40) Connector Signals” on page 51.)

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3.15 SMARC Interface Signals

Table 3-2 provides the supported pin signal definitions for the SMARC connector. Refer to the SMARC specification at http://www.sget.org/standards/smarc.html for further details of the SMARC signals.

Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
		S1	I2C_CAM1_CK **Description**: I2C clock support link for serial camera 1 **Direction**: Input / Output Open Drain **Type / Tolerance**: CMOS / 1.8V
P1	SMB_ALERT_1V8# **Description**: System Management Bus Alert (interrupt) **Direction**: Input **Type / Tolerance**: CMOS / 1.8V	S2	I2C_CAM1_DAT **Description**: I2C data support link for serial camera 1 **Direction**: Input / Output Open Drain **Type / Tolerance**: CMOS / 1.8V
P2	GND	S3	GND
P3	CSI1_CK+ **Description**: CSI1 differential clock **Direction**: Input **Type / Tolerance**: LVDS D-PHY	S4	Reserved
P4	CSI1_CK- **Description**: CSI1 differential clock **Direction**: Input **Type / Tolerance**: LVDS D-PHY	S5	I2C_CAM0_CK **Description**: I2C clock support link for serial camera 0 **Direction**: Input / Output Open Drain **Type / Tolerance**: CMOS / 1.8V
P5	Not connected	S6	I2C_CAM0_MCK **Description**: Master clock for CSI camera 0 support (may be used for CSI0 and / or CSI1 **Direction**: Output **Type / Tolerance**: CMOS / 1.8V

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P6	GBE0_SDP **Description**: IEEE 1588 Trigger signal. For hardware implementation of PTP [Precision Time Protocol]. This is typically implemented by the software-defined pins from the Ethernet controller. The SDP pins can be used for IEEE 1588 auxiliary device connections and for other miscellaneous hardware or software-control purposes **Direction**: Input / Output **Type / Tolerance**: CMOS / 3.3V	S7	I2C_CAM0_DAT **Description**: I2C data support link for serial camera 0 **Direction**: Input / Output Open Drain **Type / Tolerance**: CMOS / 1.8V
P7	CSI1_RX0+ **Description**: CSI1 differential data 0 **Direction**: Input **Type / Tolerance**: LVDS D-PHY	S8	CSI0_CK+ **Description**: CSI0 differential clock **Direction**: Input **Type / Tolerance**: LVDS D-PHY
P8	CSI1_RX0- **Description**: CSI1 differential data 0 **Direction**: Input **Type / Tolerance**: LVDS D-PHY	S9	CSI0_CK- **Description**: CSI0 differential clock **Direction**: Input **Type / Tolerance**: LVDS D-PHY
P9	GND	S10	GND
P10	CSI1_RX1+ **Description**: CSI1 differential data 1 **Direction**: Input **Type / Tolerance**: LVDS D-PHY	S11	CSI0_RX0+ **Description**: CSI0 differential data 0 **Direction**: Input **Type / Tolerance**: LVDS D-PHY
P11	CSI1_RX1- **Description**: CSI1 differential data 1 **Direction**: Input **Type / Tolerance**: LVDS D-PHY	S12	CSI0_RX0- **Description**: CSI0 differential data 0 **Direction**: Input **Type / Tolerance**: LVDS D-PHY
P12	GND	S13	GND
P13	CSI1_RX2+ **Description**: CSI1 differential data 2 **Direction**: Input **Type / Tolerance**: LVDS D-PHY)	S14	CSI0_RX1+ **Description**: CSI0 differential data 1 **Direction**: Input **Type / Tolerance**: LVDS D-PHY
P14	CSI1_RX2- **Description**: CSI1 differential data 2 **Direction**: Input **Type / Tolerance**: LVDS D-PHY	S15	CSI0_RX1- **Description**: CSI0 differential data 1 **Direction**: Input **Type / Tolerance**: LVDS D-PHY
P15	GND	S16	GND

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P16	CSI1_RX3+ **Description**: CSI1 differential data 3 **Direction**: Input **Type / Tolerance**: LVDS D-PHY	S17	Not Connected
P17	CSI1_RX3- **Description**: CSI1 differential data 3 **Direction**: Input **Type / Tolerance**: LVDS D-PHY	S18	Not Connected
P18	GND	S19	Not Connected
P19	GBE0_MDI3- **Description**: Transmit/receive pair 3 to magnetics **Direction**: Input / Output **Type / Tolerance**: MDI [Media Dependent Interface]	S20	Not Connected
P20	GBE0_MDI3+ **Description**: Transmit/receive pair 3 to magnetics **Direction**: Input / Output **Type / Tolerance**: MDI [Media Dependent Interface]	S21	Not Connected
P21	GBE0_LINK100# **Description**: Link Speed Indication LED for 100Mbps **Direction**: Output; able to sink 24mA or more carrier LED current **Type / Tolerance**: CMOS / 3.3V	S22	Not Connected
P22	GBE0_LINK1000# **Description**: Link Speed Indication LED for 1000Mbps **Direction**: Output; able to sink 24mA or more carrier LED current **Type / Tolerance**: CMOS / 3.3V	S23	Not Connected
P23	GBE0_MDI2- **Description**: Transmit/receive pair 2 to magnetics **Direction**: Input / Output **Type / Tolerance**: GBE MDI [Media Dependent Interface]	S24	Not Connected

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P24	GBE0_MDI2+ **Description**: Transmit/receive pair 2 to magnetics **Direction**: Input / Output **Type / Tolerance**: GBE MDI [Media Dependent Interface]	S25	GND
P25	GBE0_LINK_ACT# **Description**: Link / Activity Indication LED Driven low on Link [10, 100 or 1000 mbps] Blinks on Activity **Direction**: Output; able to sink 24mA or more Carrier LED current **Type / Tolerance**: CMOS / 3.3V	S26	Not Connected
P26	GBE0_MDI1- **Description**: Transmit/receive pair 1 to magnetics **Direction**: Input / Output **Type / Tolerance**: GBE MDI [Media Dependent Interface]	S27	Not Connected
P27	GBE0_MDI1+ **Description**: Transmit/receive pair 1 to magnetics **Direction**: Input / Output **Type / Tolerance**: GBE MDI [Media Dependent Interface]	S28	Not Connected
P28	GBE0_CTREF **Description**: Center-Tap reference voltage for GBE0 Carrier board Ethernet magnetic [if required by the Module GBE PHY] **Direction**: Output **Type / Tolerance**: Reference Voltage	S29	PCIE_D_TX+ **Description**: Differential PCIe Link D transmit data pair. Series coupling capacitors (0.1 uF 0402) are on the Module. **Direction**: Output **Type / Tolerance**: LVDS PCIe
P29	GBE0_MDI0- **Description**: Transmit/receive pair 0 to magnetics **Direction**: Input / Output **Type / Tolerance**: GBE MDI [Media Dependent Interface]	S30	PCIE_D_TX- **Description**: Differential PCIe Link D transmit data pair. Series coupling capacitors (0.1 uF 0402) are on the Module. **Direction**: Output **Type / Tolerance**: LVDS PCIe

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P30	GBE0_MDI0+ **Description**: Transmit/receive pair 0 to magnetics **Direction**: Input / Output **Type / Tolerance**: GBE MDI [Media Dependent Interface]	S31	Not connected
P31	Not connected	S32	PCIE_D_RX+ **Description**: Differential PCIe Link D receive data pair. No coupling caps on Module. **Direction**: Input **Type / Tolerance**: LVDS PCIe
P32	GND	S33	PCIE_D_RX- **Description**: Differential PCIe Link D receive data pair. No coupling caps on Module. **Direction**: Input **Type / Tolerance**: LVDS PCIe
P33	SDIO_WP **Description**: SDIO card Write Protect; 1K pull-up to 3.3V **Direction**: Input **Type / Tolerance**: CMOS / 3.3V	S34	GND
P34	SDIO_CMD **Description**: SDIO card Command line **Direction**: Input / Output **Type / Tolerance**: CMOS / 3.3V	S35	USB4+ **Description**: Differential USB 2.0 data pair **Direction**: Input / Output **Type / Tolerance**: USB
P35	SDIO_CD# **Description**: SDIO Card Detect; 1K pull-up to 3.3V **Direction**: Input **Type / Tolerance**: CMOS / 3.3V	S36	USB4- **Description**: Differential USB 2.0 data pair **Direction**: Input / Output **Type / Tolerance**: USB
P36	SDIO_CK **Description**: SDIO card Clock **Direction**: Output **Type / Tolerance**: CMOS / 3.3V	S37	Not Connected

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P37	SDIO_PWR_EN **Description**: SDIO card Power Enable **Direction**: Output **Type / Tolerance**: CMOS / 3.3V	S38	AUDIO_MCK **Description**: Master clock output to audio codecs **Direction**: Output **Type / Tolerance**: CMOS / 1.8V
P38	GND	S39	I2S0_LRCK **Description**: Left & Right audio synchronization clock **Direction**: Input / Output; **Type / Tolerance**: CMOS / 1.8V
P39	SDIO_D0 **Description**: SDIO card 4-bit data path **Direction**: Input / Output **Type / Tolerance**: CMOS / 3.3V	S40	I2S0_SDOUT **Description**: Digital audio output **Direction**: Output **Type /Tolerance**: CMOS / 1.8V
P40	SDIO_D1 **Description**: SDIO card 4-bit data path **Direction**: Input / Output **Type / Tolerance**: CMOS / 3.3V	S41	I2S0_SDIN **Description**: Digital audio input **Direction**: Input **Type /Tolerance**: CMOS / 1.8V
P41	SDIO_D2 **Description**: SDIO card 4-bit data path **Direction**: Input / Output **Type / Tolerance**: CMOS / 3.3V	S42	I2S0_CK **Description**: Digital audio clock **Direction**: Input / Output **Type / Tolerance**: CMOS / 1.8V
P42	SDIO_D3 **Description**: SDIO card 4-bit data path **Direction**: Input / Output **Type / Tolerance**: CMOS / 3.3V	S43	ESPI_ALERT0# **Description**: Enhanced SPI Slave request for service from Master **Direction**: Output Open Drain **Type / Tolerance**: CMOS / 1.8V
P43	SPI0_CS0# **Description**: SPI0 Master Chip Select 0; use to select carrier SPI boot device **Direction**: Output **Type / Tolerance**: CMOS / 1.8V	S44	ESPI_ALERT1# **Description**: Enhanced SPI Slave request for service from Master **Direction**: Output Open Drain **Type / Tolerance**: CMOS / 1.8V
P44	SPI0_CK **Description**: SPI0 Master Clock output **Direction**: Output **Type / Tolerance**: CMOS / 1.8V	S45	Not Connected

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P45	SPI0_DIN **Description**: SPI0 Master Data input [input to CPU, output from SPI device] **Direction**: Input **Type / Tolerance**: CMOS / 1.8V	S46	Not Connected
P46	SPI0_DO **Description**: SPI0 Master Data output [output from CPU, input to SPI device] **Direction**: Output **Type / Tolerance**: CMOS / 1.8V	S47	GND
P47	GND	S48	I2C_GP_CK **Description**: I2C General Purpose clock signal **Direction**: Input / Output Open Drain **Type / Tolerance**: CMOS / 1.8V
P48	SATA0_TX+ **Description**: Differential SATA 0 transmit data Pair; 10 nF 0402 capacitor on module **Direction**: Output **Type / Tolerance**: SATA	S49	I2C_GP_DAT I2C **Description**: I2C General Purpose data signal **Direction**: Input / Output Open Drain **Type / Tolerance**: CMOS / 1.8V
P49	SATA0_TX- **Description**: Differential SATA 0 transmit data Pair; 10 nF 0402 capacitor on module **Direction**: Output **Type / Tolerance**: SATA	S50	HDA_SYNC **Description**: Intel HD Audio Sync **Direction**: Input / Output **Type / Tolerance**: CMOS / 1.5V
P50	GND	S51	HDA_SDO **Description**: Intel HD Audio Data Out **Direction**: Output **Type / Tolerance**: CMOS / 1.5V
P51	SATA0_RX+ **Description**: Differential SATA 0 receive data Pair; 10 nF 0402 capacitor on module **Direction**: Input **Type / Tolerance**: SATA	S52	HDA_SDI **Description**: Intel HD Audio Data In **Direction**: Input **Type / Tolerance**: CMOS / 1.5V
P52	SATA0_RX- **Description**: Differential SATA 0 receive data Pair; 10 nF 0402 capacitor on module **Direction**: Input **Type / Tolerance**: SATA	S53	HDA_CK **Description**: Intel HD Audio Data Clock **Direction**: Input / Output **Type / Tolerance**: CMOS / 1.5V

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P53	GND	S54	SATA_ACT# **Description**: Active low SATA activity indicator, able to sink 24mA or more Carrier LED current **Direction**: Output **Type / Tolerance**: CMOS / 3.3V
P54	SPI1_CS0# **Description**: SPI1 Master Chip Select 0 **Direction**: Output **Type / Tolerance**: CMOS / 1.8V	S55	USB5_EN_OC# **Description**: Pulled low by Module OD driver to disable USB5 power. Pulled low by Carrier OD driver to indicate over- current situation. A pull-up is present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.10.3 of *SMARC Specification 2.0.* **Direction**: Input / Output Open Drain **Type / Tolerance**: CMOS / 3.3V
P55	SPI1_CS1# **Description**: SPI1 Master Chip Select 1 **Direction**: Output **Type / Tolerance**: CMOS / 1.8V	S56	Not Connected
P56	SPI1_CK **Description**: SPI1 Master Clock **Direction**: Output **Type / Tolerance**: CMOS / 1.8V	S57	Not Connected
P57	SPI1_IO_1 **Description**: SPI1 Master/Slave Data MISO **Direction**: Input / Output **Type / Tolerance**: CMOS / 1.8V	S58	ESPI_RESET# **Description**: Enhanced SPI interface master to slave reset **Direction**: Output **Type / Tolerance**: CMOS / 1.8V
P58	SPI1_IO_0 **Description**: SPI1 Master/Slave Data MOSI **Direction**: Input / Output **Type / Tolerance**: CMOS / 1.8V	S59	USB5+ **Description**: Differential USB 2.0 data pair 5 **Direction**: Input / Output **Type / Tolerance**: USB
P59	GND	S60	USB5- **Description**: Differential USB 2.0 data pair 5 **Direction**: Input / Output **Type / Tolerance**: USB

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P60	USB0+ **Description**: Differential USB 2.0 data pair 0 **Direction**: Input / Output **Type / Tolerance**: USB	S61	GND
P61	USB0- **Description**: Differential USB 2.0 data pair 0 **Direction**: Input / Output **Type / Tolerance**: USB	S62	USB3_SSTX+ **Description**: Transmit signal differential pair for Super Speed USB3 data; coupling caps are off module **Direction**: Output **Type / Tolerance**: USB SS
P62	USB0_EN_OC# **Description**: Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over- current situation. A pull-up is present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.10.3 of *SMARC Specification 2.0.* **Direction**: Input / Output Open Drain **Type / Tolerance**: CMOS / 3.3V	S63	USB3_SSTX- **Description**: Transmit signal differential pair for Super Speed USB3 data; coupling caps are off module **Direction**: Output **Type / Tolerance**: USB SS
P63	USB0_VBUS_DET **Description**: USB0 host power detection, when this port is used as a device; **Direction**: Input **Type / Tolerance**: USB VBUS 5V	S64	GND
P64	USB0_OTG_ID **Description**: USB0 On-The-Go ID, active high **Direction**: Input **Type / Tolerance**: CMOS 3.3V	S65	USB3_SSRX+ **Description**: Receive signal differential pair for Super Speed USB3 data; coupling caps are off module **Direction**: Input **Type / Tolerance**: USB SS
P65	USB1+ **Description**: Differential USB 2.0 data pair 1 **Direction**: Input / Output **Type / Tolerance**: USB	S66	USB3_SSRX- **Description**: Receive signal differential pair for Super Speed USB3 data; coupling caps are off module **Direction**: Input **Type / Tolerance**: USB SS

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P66	USB1- **Description**: Differential USB 2.0 data pair 1 **Direction**: Input / Output **Type / Tolerance**: USB	S67	GND
P67	USB1_EN_OC# **Description**: Pulled low by Module OD driver to disable USB1 power. Pulled low by Carrier OD driver to indicate over- current situation. A pull-up is present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.10.3 of *SMARC Specification 2.0.* **Direction**: Input / Output Open Drain **Type / Tolerance**: CMOS / 3.3V	S68	USB3+ **Description**: Differential USB 2.0 data pair 3 **Direction**: Input / Output **Type / Tolerance**: USB
P68	GND	S69	USB3- **Description**: Differential USB 2.0 data pair 3 **Direction**: Input / Output **Type / Tolerance**: USB
P69	USB2+ **Description**: Differential USB 2.0 data pair 2 **Direction**: Input / Output **Type / Tolerance**: USB	S70	GND
P70	USB2- **Description**: Differential USB 2.0 data pair 2 **Direction**: Input / Output **Type / Tolerance**: USB	S71	USB2_SSTX+ **Description**: Transmit signal differential pair for Super Speed USB2 data; coupling caps are off module **Direction**: Output **Type / Tolerance**: USB SS
P71	USB2_EN_OC# **Description**: Pulled low by Module OD driver to disable USB2 power. Pulled low by Carrier OD driver to indicate over- current situation. A pull-up ***shall*** be present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.10.3 of *SMARC Specification 2.0*. **Direction**: Input / Output Open Drain **Type / Tolerance**: CMOS / 3.3V	S72	USB2_SSTX- **Description**: Transmit signal differential pair for Super Speed USB2 data; coupling caps are off module **Direction**: Output **Type / Tolerance**: USB SS
P72	Not Connected	S73	GND

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P73	Not Connected	S74	USB2_SSRX+ **Description**: Receive signal differential pair for Super Speed USB2 data; coupling caps are off module **Direction**: Input **Type / Tolerance**: USB SS
P74	USB3_EN_OC# **Description**: Pulled low by Module OD driver to disable USB3 power. Pulled low by Carrier OD driver to indicate over- current situation. A pull-up ***shall*** be present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.10.3 of *SMARC Specification 2.0*. **Direction**: Input / Output Open Drain **Type / Tolerance**: CMOS / 3.3V	S75	USB2_SSRX- **Description**: Receive signal differential pair for Super Speed USB2 data; coupling caps are off module **Direction**: Input **Type / Tolerance**: USB SS
P75	PCIE_A_RST# **Description**: PCIe Port A reset output, active low **Direction**: Output **Type / Tolerance**: CMOS / 3.3V	S76	PCIE_B_RST# **Description**: PCIe Port B reset output, active low **Direction**: Output **Type / Tolerance**: CMOS / 3.3V
P76	USB4_EN_OC# **Description**: Pulled low by Module OD driver to disable USB4 power. Pulled low by Carrier OD driver to indicate over- current situation. A pull-up ***shall*** be present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.10.3 of *SMARC Specification 2.0*. **Direction**: Input / Output Open Drain **Type / Tolerance**: CMOS / 3.3V	S77	PCIE_C_RST# **Description**: PCIe Port C reset output, active low **Direction**: Output **Type / Tolerance**: CMOS / 3.3V
P77	Not Connected	S78	PCIE_C_RX+ **Description**: Differential PCIe Link C receive data pair. No coupling caps on Module. **Direction**: Input **Type / Tolerance**: LVDS PCIe

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P78	Not Connected	S79	PCIE_C_RX- **Description**: Differential PCIe Link C receive data pair. No coupling caps on Module. **Direction**: Input **Type / Tolerance**: LVDS PCIe
P79	GND	S80	GND
P80	PCIE_C_REFCK+ **Description**: Differential PCIe Link C reference clock. DC coupled **Direction**: Output **Type / Tolerance**: LVDS PCIe	S81	PCIE_C_TX+ **Description**: Differential PCIe Link C transmit data pair. Series coupling capacitors (0.1 uF 0402) are on the Module. **Direction**: Output **Type / Tolerance**: LVDS PCIe
P81	PCIE_C_REFCK- **Description**: Differential PCIe Link C reference clock. DC coupled. **Direction**: Output **Type / Tolerance**: LVDS PCIe	S82	PCIE_C_TX- **Description**: Differential PCIe Link C transmit data pair. Series coupling capacitors (0.1 uF 0402) are on the Module. **Direction**: Output **Type / Tolerance**: LVDS PCIe
P82	GND	S83	GND
P83	PCIE_A_REFCK+ **Description**: Differential PCIe Link A reference clock. DC coupled. **Direction**: Output **Type / Tolerance**: LVDS PCIe	S84	PCIE_B_REFCK+ **Description**: Differential PCIe Link B reference clock. DC coupled. **Direction**: Output **Type / Tolerance**: LVDS PCIe
P84	PCIE_A_REFCK- **Description**: Differential PCIe Link A reference clock. DC coupled. **Direction**: Output **Type / Tolerance**: LVDS PCIe	S85	PCIE_B_REFCK- **Description**: Differential PCIe Link B reference clock. DC coupled. **Direction**: Output **Type / Tolerance**: LVDS PCIe
P85	GND	S86	GND
P86	PCIE_A_RX+ **Description**: Differential PCIe Link A receive data pair. No coupling caps on Module. **Direction**: Input **Type / Tolerance**: LVDS PCIe	S87	PCIE_B_RX+ **Description**: Differential PCIe Link B receive data pair. No coupling caps on Module. **Direction**: Input **Type / Tolerance**: LVDS PCIe

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P87	PCIE_A_RX- **Description**: Differential PCIe Link A receive data pair. No coupling caps on Module. **Direction**: Input **Type / Tolerance**: LVDS PCIe	S88	PCIE_B_RX- **Description**: Differential PCIe Link B receive data pair. No coupling caps on Module. **Direction**: Input **Type / Tolerance**: LVDS PCIe
P88	GND	S89	GND
P89	PCIE_A_TX+ **Description**: Differential PCIe Link A transmit data pair. Series coupling capacitors (0.1 uF 0402) are on the Module. **Direction**: Output **Type / Tolerance**: LVDS PCIe	S90	PCIE_B_TX+ **Description**: Differential PCIe Link B transmit data pair. Series coupling capacitors (0.1 uF 0402) are on the Module. **Direction**: Output **Type / Tolerance**: LVDS PCIe
P90	PCIE_A_TX- **Description**: Differential PCIe Link A transmit data pair. Series coupling capacitors (0.1 uF 0402) are on the Module. **Direction**: Output **Type / Tolerance**: LVDS PCIe	S91	PCIE_B_TX- **Description**: Differential PCIe Link B transmit data pair. Series coupling capacitors (0.1 uF 0402) are on the Module. **Direction**: Output **Type / Tolerance**: LVDS PCIe
P91	GND	S92	GND
P92	HDMI_D2+ **Description**: TMDS / HDMI data 2 differential pair **Direction**: Output **Type / Tolerance**: TMDS DP1_LANE0+ [**default**] **Description**: DisplayPort++ 1 lane 0 differential pair **Direction**: Output **Coupling / Tolerance**: AC coupled off module	S93	DP0_LANE0+ **Description**: DisplayPort++ 0 lane 0 differential pair **Direction**: Output **Type / Tolerance**: LVDS PCIE

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P93	HDMI_D2- **Description**: TMDS / HDMI data 2 differential pair **Direction**: Output **Type / Tolerance**: TMDS DP1_LANE0- [**default**] **Description**: DisplayPort++ 1 lane 0 differential pair **Direction**: Output **Coupling / Tolerance**: AC coupled off module	S94	DP0_LANE0- **Description**: DisplayPort++ 0 lane 0 differential pair **Direction**: Output **Type / Tolerance**: LVDS PCIE
P94	GND	S95	DP0_AUX_SEL **Description**: Pulled to ground on carrier for DisplayPort++ 0 operation **Direction**: Input **Type / Tolerance**: CMOS / 1.8V
P95	HDMI_D1+ **Description**: TMDS / HDMI data 1 differential pair **Direction**: Output **Type / Tolerance**: TMDS DP1_LANE1+ [**default**] **Description**: DisplayPort++ 1 lane 1 differential pair **Direction**: Output **Coupling / Tolerance**: AC coupled off module	S96	DP0_LANE1+ **Description**: DisplayPort++ 0 lane 1 differential pair **Direction**: Output **Type / Tolerance**: LVDS PCIE
P96	HDMI_D1- **Description**: TMDS / HDMI data 1 differential pair **Direction**: Output **Type / Tolerance**: TMDS DP1_LANE1- [**default**] **Description**: DisplayPort++ 1 lane 1 differential pair **Direction**: Output **Coupling / Tolerance**: AC coupled off module	S97	DP0_LANE1- **Description**: DisplayPort++ 0 lane 1 differential pair **Direction**: Output **Type / Tolerance**: LVDS PCIE

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P97	GND	S98	DP0_HPD **Description**: DisplayPort++ 0 Hot Plug Detect **Direction**: Input **Type / Tolerance**: CMOS / 1.8V
P98	HDMI_D0+ **Description**: TMDS / HDMI data 0 differential pair **Direction**: Output **Type / Tolerance**: TMDS DP1_LANE2+ [**default**] **Description**: DisplayPort++ 1 lane 2 differential pair **Direction**: Output **Coupling / Tolerance**: AC coupled off module	S99	DP0_LANE2+ **Description**: DisplayPort++ 0 lane 2 differential pair **Direction**: Output **Type / Tolerance**: LVDS PCIE
P99	HDMI_D0- **Description**: TMDS / HDMI data 0 differential pair **Direction**: Output **Type / Tolerance**: TMDS DP1_LANE2- [**default**] **Description**: DisplayPort++ 1 lane 2 differential pair **Direction**: Output **Coupling / Tolerance**: AC coupled off module	S100	DP0_LANE2- **Description**: DisplayPort++ 0 lane 2 differential pair **Direction**: Output **Type / Tolerance**: LVDS PCIE
P100	GND	S101	GND
P101	HDMI_CK+ **Description**: HDMI clock differential pair **Direction**: Output **Type / Tolerance**: TMDS DP1_LANE3+ [**default**] **Description**: DisplayPort++ 1 lane 3 differential pair **Direction**: Output **Coupling / Tolerance**: AC coupled off module	S102	DP0_LANE3+ **Description**: DisplayPort++ 0 lane 3 differential pair **Direction**: Output **Type / Tolerance**: LVDS PCIE

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P102	HDMI_CK- **Description**: HDMI clock differential pair **Direction**: Output **Type / Tolerance**: TMDS DP1_LANE3- [**default**] **Description**: DisplayPort++ 1 lane 3 differential pair **Direction**: Output **Coupling / Tolerance**: AC coupled off module	S103	DP0_LANE3- **Description**: DisplayPort++ 0 lane 3 differential pair **Direction**: Output **Type / Tolerance**: LVDS PCIE
P103	GND	S104	Not Connected
P104	HDMI_HPD **Description**: HDMI Hot Plug Detect **Direction**: Input **Type / Tolerance**: CMOS / 1.8V DP1_HDP [**default**] **Description**: DisplayPort++ 1 Hot Plug Detect **Direction**: Input **Coupling / Tolerance**: DC coupled / CMOS 1.8V	S105	DP0_AUX+ **Description**: DisplayPort++ 0 Auxiliary Channel pair used for link management and device control **Direction**: Input / Output **Type / Tolerance**: LVDS PCIE
P105	HDMI_CTRL_CK **Description**: I2C clock line dedicated to HDMI **Direction**: Output Open Drain **Type / Tolerance**: CMOS / 1.8V DP1_AUX+ [**default**] **Description**: DisplayPort++ 1 Auxiliary Channel pair used for link management and device control **Direction**: Input / Output **Coupling / Tolerance**: AC coupled on module	S106	DP0_AUX- **Description**: DisplayPort++ 0 Auxiliary Channel pair used for link management and device control **Direction**: Input / Output **Type / Tolerance**: LVDS PCIE

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P106	HDMI_CTRL_DAT **Description**: I2C data line dedicated to HDMI **Direction**: Input / Output Open Drain **Type / Tolerance**: CMOS / 1.8V DP1_AUX- [**default**] **Description**: DisplayPort++ 1 Auxiliary Channel pair used for link management and device control **Direction**: Input / Output **Coupling / Tolerance**: AC coupled on module	S107	Not connected
P107	DP1_AUX_SEL **Description**: Pulled to ground on carrier for DisplayPort++ 1 operation **Direction**: Input **Coupling / Tolerance**: DC coupled / CMOS 1.8V	S108	LVDS1_CK+ [**option**] **Description**: LVDS1 channel B differential clock pair **Direction**: Output **Type** / **Tolerance**: LVDS LCD
P108	GPIO0 **Description**: General Purpose IO [Output recommended] **Direction**: Input / Output **Type / Tolerance**: CMOS 1.8V	S109	LVDS1_CK- [**option**] **Description**: LVDS1 channel B differential clock pair **Direction**: Output **Type** / **Tolerance**: LVDS LCD
P109	GPIO1 **Description**: General Purpose IO [Output recommended] **Direction**: Input / Output **Type / Tolerance**: CMOS 1.8V	S110	GND
P110	GPIO2 **Description**: General Purpose IO [Output recommended] **Direction**: Input / Output **Type / Tolerance**: CMOS 1.8V	S111	LVDS1_0+ [**option**] **Description**: LVDS1 control channel B differential data pair 0 **Direction**: Output **Type** / **Tolerance**: LVDS LCD
P111	GPIO3 **Description**: General Purpose IO [Output recommended] **Direction**: Input / Output **Type / Tolerance**: CMOS 1.8V	S112	LVDS1_0- [**option**] **Description**: LVDS1 control channel B differential data pair 0 **Direction**: Output **Type** / **Tolerance**: LVDS LCD

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P112	HDA_RST# **Description**: HDA Reset **Direction**: Output **Type / Tolerance**: CMOS 1.8V	S113	Not connected
P113	PWM_OUT **Description**: Power Management Out **Direction**: Output **Type / Tolerance**: CMOS 1.8V	S114	LVDS1_1+ [**option**] **Description**: LVDS1 control channel B differential data pair 1 **Direction**: Output **Type** / **Tolerance**: LVDS LCD
P114	TACHIN **Description**: Tachometer In **Direction**: Input **Type / Tolerance**: CMOS 1.8V	S115	LVDS1_1- [**option**] **Description**: LVDS1 control channel B differential data pair 1 **Direction**: Output **Type** / **Tolerance**: LVDS LCD
P115	GPIO7 **Description**: General Purpose IO [Input recommended] **Direction**: Input / Output **Type / Tolerance**: CMOS 1.8V	S116	Not connected
P116	GPIO8 **Description**: General Purpose IO [Input recommended] **Direction**: Input / Output **Type / Tolerance**: CMOS 1.8V	S117	LVDS1_2+ [**option**] **Description**: LVDS1 control channel B differential data pair 2 **Direction**: Output **Type** / **Tolerance**: LVDS LCD
P117	GPIO9 **Description**: General Purpose IO [Input recommended] **Direction**: Input / Output **Type / Tolerance**: CMOS 1.8V	S118	LVDS1_2- [**option**] **Description**: LVDS1 control channel B differential data pair 2 **Direction**: Output **Type** / **Tolerance**: LVDS LCD
P118	GPIO10 **Description**: General Purpose IO [Input recommended] **Direction**: Input / Output **Type / Tolerance**: CMOS 1.8V	S119	GND
P119	GPIO11 **Description**: General Purpose IO [Input recommended] **Direction**: Input / Output **Type / Tolerance**: CMOS 1.8V	S120	LVDS1_3+ [**option**] **Description**: LVDS1 control channel B differential data pair 3 **Direction**: Output **Type** / **Tolerance**: LVDS LCD

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P120	GND	S121	LVDS1_3- [**option**] **Description**: LVDS1 control channel B differential data pair 3 **Direction**: Output **Type** / **Tolerance**: LVDS LCD
P121	I2C_PM_CK **Description**: Power management I2C bus [SMBus] clock **Direction**: Input / Output Open Drain **Type / Tolerance**: CMOS 1.8V	S122	Not connected
P122	I2C_PM_DAT **Description**: Power management I2C bus [SMBus] data **Direction**: Input / Output Open Drain **Type / Tolerance**: CMOS 1.8V	S123	Not connected
P123	BOOT_SEL0# **Description**: Input straps determine the Module boot device. Pulled up on Module. Driven by OD part on Carrier **Direction**: Input **Type / Tolerance**: CMOS 1.8V	S124	GND
P124	BOOT_SEL1# **Description**: Input straps determine the Module boot device. Pulled up on Module. Driven by OD part on Carrier **Direction**: Input **Type / Tolerance**: CMOS 1.8V	S125	LVDS0_0+ **Description**: LVDS0 control channel A differential data pair 0 **Direction**: Output **Type** / **Tolerance**: LVDS LCD
P125	BOOT_SEL2# **Description**: Input straps determine the Module boot device. Pulled up on Module. Driven by OD part on Carrier **Direction**: Input **Type / Tolerance**: CMOS 1.8V	S126	LVDS0_0- **Description**: LVDS0 control channel A differential data pair 0 **Direction**: Output **Type** / **Tolerance**: LVDS LCD
P126	RESET_OUT# **Description**: General purpose reset output to Carrier board **Direction**: Output **Type / Tolerance**: CMOS 1.8V	S127	LCD0_BKLT_EN **Description**: Enables LVDS0 channel A panel backlight **Direction**: Output **Type / Tolerance**: CMOS / 1.8V

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P127	RESET_IN# **Description**: Reset input from Carrier board. Carrier drives low to force a Module reset; floats the line otherwise. Pulled up on Module. Driven by OD part on Carrier **Direction**: Input **Type / Tolerance**: CMOS / 1.8V	S128	LVDS0_1+ **Description**: LVDS0 control channel A differential data pair 1 **Direction**: Output **Type** / **Tolerance**: LVDS LCD
P128	POWER_BTN# **Description**: Power-button input from Carrier board. Carrier to float the line in inactive state. Active low, level sensitive. De-bounced on the Module. Pulled up on Module. Driven by OD part on Carrier **Direction**: Input **Type / Tolerance**: CMOS / 1.8V	S129	LVDS0_1- **Description**: LVDS0 control channel A differential data pair 1 **Direction**: Output **Type** / **Tolerance**: LVDS LCD
P129	SER0_TX **Description**: Asynchronous serial port 0 data Out **Direction**: Output **Type / Tolerance**: CMOS / 1.8V	S130	GND
P130	SER0_RX **Description**: Asynchronous serial port 0 data In **Direction**: Input **Type / Tolerance**: CMOS / 1.8V	S131	LVDS0_2+ **Description**: LVDS0 control channel A differential data pair 2 **Direction**: Output **Type** / **Tolerance**: LVDS LCD
P131	SER0_RTS# **Description**: Request to Send handshake line for SER0 **Direction**: Output **Type / Tolerance**: CMOS / 1.8V	S132	LVDS0_2- **Description**: LVDS0 control channel A differential data pair 2 **Direction**: Output **Type** / **Tolerance**: LVDS LCD
P132	SER0_CTS# **Description**: Clear to Send handshake line for SER0 **Direction**: Input **Type / Tolerance**: CMOS / 1.8V	S133	LCD0_VDD_EN **Description**: Enables LVDS0 channel A panel VDD **Direction**: Output **Type / Tolerance**: CMOS / 1.8V
P133	GND	S134	LVDS0_CK+ **Description**: LVDS0 channel A differential clock pair **Direction**: Output **Type** / **Tolerance**: LVDS LCD

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P134	SER1_TX **Description**: Asynchronous serial port 1 data Out **Direction**: Output **Type / Tolerance**: CMOS / 1.8V	S135	LVDS0_CK- **Description**: LVDS0 channel A differential clock pair **Direction**: Output **Type** / **Tolerance**: LVDS LCD
P135	SER1_RX **Description**: Asynchronous serial port 1 data In **Direction**: Input **Type / Tolerance**: CMOS / 1.8V	S136	GND
P136	SER2_TX **Description**: Asynchronous serial port 2 data Out **Direction**: Output **Type / Tolerance**: CMOS / 1.8V	S137	LVDS0_3+ **Description**: LVDS0 control channel A differential data pair 3 **Direction**: Output **Type** / **Tolerance**: LVDS LCD
P137	SER2_RX **Description**: Asynchronous serial port 2 data In **Direction**: Input **Type / Tolerance**: CMOS / 1.8V	S138	LVDS0_3- **Description**: LVDS0 control channel A differential data pair 3 **Direction**: Output **Type** / **Tolerance**: LVDS LCD
P138	SER2_RTS# **Description**: Request to Send handshake line for SER2 **Direction**: Output **Type / Tolerance**: CMOS / 1.8V	S139	I2C_LCD_CK **Description**: I2C clock – to read LVDS display EDID EEPROMs **Direction**: output **Type / Tolerance**: CMOS / 1.8V
P139	SER2_CTS# **Description**: Clear to Send handshake line for SER2 **Direction**: Input **Type / Tolerance**: CMOS / 1.8V	S140	I2C_LCD_DAT **Description**: I2C data – to read LVDS display EDID EEPROMs. Be aware of possible EDID PROM address conflicts if multiple displays are implemented. **Direction**: output **Type / Tolerance**: CMOS / 1.8V
P140	SER3_TX **Description**: Asynchronous serial port 3 data Out **Direction**: Output **Type / Tolerance**: CMOS / 1.8V	S141	LCD0_BKLT_PWM **Description**: LVDS channel A display backlight PWM control **Direction**: Output **Type / Tolerance**: CMOS / 1.8V

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P141	SER3_RX **Description**: Asynchronous serial port 3 data In **Direction**: Input **Type / Tolerance**: CMOS / 1.8V	S142	Not connected
P142	GND	S143	GND
P143	Not connected	S144	EDP0_HPD **Description**: eDP0 Hot Plug Detect **Direction**: Input **Type / Tolerance**: CMOS / 1.8V
P144	Not connected	S145	WDT_TIME_OUT# **Description**: Watchdog Timer Out **Direction**: Output **Type / Tolerance**: CMOS / 1.8V
P145	Not connected	S146	PCIE_WAKE **Description**: PCIe wake up interrupt to host – common to PCIe; links A, B, C – pulled up or terminated on Module **Direction**: Input **Type / Tolerance**: CMOS / 3.3V
P146	Not connected	S147	VDD_RTC **Description**: Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based Lithium cell or Super Cap. See ***Section 7.3 RTC Voltage Rail*** of the SMARC specification for an important safety note on the implementation of lithium backup batteries. **Direction**: Input **Type / Tolerance**: Power In (Power Out when charging a Super Cap)

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P147	VDD_IN **Description**: Module power input voltage - 3.0V min to 5.25V max **Direction**: Input **Type / Tolerance**: Power In	S148	LID# **Description**: Lid open/close indication to Module. Low indicates lid closure, which system ***may*** use to initiate a sleep state. Carrier to float the line in inactive state. Active low, level sensitive. De-bounced on the Module Pulled up on Module. Driven by OD part on Carrier. **Direction**: Input **Type / Tolerance**: CMOS / 1.8V
P148	VDD_IN **Description**: Module power input voltage - 3.0V min to 5.25V max **Direction**: Input **Type / Tolerance**: Power In	S149	SLEEP# **Description**: Sleep indicator from Carrier board; sourced from user Sleep button or Carrier logic. Carrier to float the line in inactive state. Active low, level sensitive; de-bounced on the Module. Pulled up on Module. Driven by OD part on Carrier. **Direction**: Input **Type / Tolerance**: CMOS / 1.8V
P149	VDD_IN **Description**: Module power input voltage - 3.0V min to 5.25V max **Direction**: Input **Type / Tolerance**: Power In	S150	VIN_PWR_BAD# **Description**: Power bad indication from Carrier board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) ***is not*** enabled while this signal is held low by the Carrier. Pulled up on Module. Driven by OD part on Carrier. **Direction**: Input **Type / Tolerance**: CMOS / VDD_IN
P150	VDD_IN **Description**: Module power input voltage - 3.0V min to 5.25V max **Direction**: Input **Type / Tolerance**: Power In	S151	CHARGING# **Description**: Held low by Carrier during battery charging. Carrier to float the line when charge is complete. Pulled up on Module. Driven by OD part on Carrier. **Direction**: Input **Type / Tolerance**: CMOS / 1.8V

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P151	VDD_IN **Description**: Module power input voltage - 3.0V min to 5.25V max **Direction**: Input **Type / Tolerance**: Power In	S152	CHARGER_PRSNT# **Description**: Held low by Carrier if DC input for battery charger is present. Pulled up on Module. Driven by OD part on Carrier. **Direction**: Input **Type / Tolerance**: CMOS / 1.8V
P152	VDD_IN **Description**: Module power input voltage - 3.0V min to 5.25V max **Direction**: Input **Type / Tolerance**: Power In	S153	CARRIER_STBY# **Description**: The Module drives this signal low when the system is in a standby power state **Direction**: Output **Type / Tolerance**: CMOS / 1.8V
P153	VDD_IN **Description**: Module power input voltage - 3.0V min to 5.25V max **Direction**: Input **Type / Tolerance**: Power In	S154	CARRIER_PWR_ON **Description**: Carrier board circuits [apart from power management and power path circuits] ***are*** powered up until the Module asserts the CARRIER_PWR_ON signal **Direction**: Output **Type / Tolerance**: CMOS / 1.8V
P154	VDD_IN **Description**: Module power input voltage - 3.0V min to 5.25V max **Direction**: Input **Type / Tolerance**: Power In	S155	FORCE_RECOV# **Description**: Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when the Force Recovery function is invoked. Pulled high on the Module. For SOCs that do not implement a USB based Force Recovery function, then a low on the Module FORCE_RECOV# pin ***may*** invoke the SOC native Force Recovery mode – such as over a Serial Port. Pulled up on Module. Driven by OD part on Carrier. **Direction**: Input **Type / Tolerance**: CMOS / 1.8V
P155	VDD_IN **Description**: Module power input voltage - 3.0V min to 5.25V max **Direction**: Input **Type / Tolerance**: Power In	S156	BATLOW# **Description**: Battery low indication to Module. Carrier to float the line in inactive state. Pulled up on Module. Driven by OD part on Carrier. **Direction**: Input **Type / Tolerance**: CMOS / 1.8V

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Signal (Primary - Top Side)	Pin #	Signal (Secondary - Bottom Side)
P156	VDD_IN **Description**: Module power input voltage - 3.0V min to 5.25V max **Direction**: Input **Type / Tolerance**: Power In	S157	TEST# **Description**: Held low by Carrier to invoke Module vendor specific test function(s). Pulled up on Module. Driven by OD part on Carrier. **Direction**: Input **Type / Tolerance**: CMOS / 1.8V
		S158	GND

NOTE: The # symbol indicates the signal is Active Low.

3.16 Debug (DB40) Connector Signals

Table 3-3 lists the pin signals of the CN1 connector, which provides 40 pins, 1 row, consecutive sequence with 0.02" (0.50mm) pitch.

Table 3-3: Debug Interface Signals (CN1)

Pin #	Interface	Signal
1	**Reserved**	RESVD
2	**SMC Debug**	SMC_STATUS
3		BIOS_MODE
4		SEL_BIOS
5		POSTWDT_DIS#
6	**Test Point**	SUS_S5#
7		SUS_S4#
8		SUS_S3#
9		CB_PWROK
10		CB_RESET#
11		SYS_RESET#
12		PWRBTN#
13	**SMC Program Interface**	SMC_OCD0B
14		SMC_OCD0A
15		SMC_CLK
16		SMC_DATA
17		SMC_RESET_IN#
18		SMC_FLMD0
19		SMC_RXD6
20		SMC_TXD6
21		GND3
22		3V3_DUAL
23		3V3_SMC1

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Table 3-3: Debug Interface Signals (CN1) (Continued)

Pin #	Interface	Signal
24	LPC Debug Card Interface	LPC_AD0
25		LPC_AD1
26		LPC_AD2
27		LPC_AD3
28		LPC_FRAME#
29		CLK33_LPC
30		RST#
31		BIOS_DIS0
32		GND2
33		LPC_3V3
34	SPI Program Interface	SPI_BIOS_CLK
35		SPI_BIOS_MOSI
36		SPI_BIOS_MISO
37		SPI_BIOS_CS1#
38		SPI_BIOS_CS0#
39		GND1
40		VCC_SPI_IN

NOTE: The gray table cells denote ground. The # symbol indicates the signal is Active Low.

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4 Utilities

This chapter provides information on how to use the BIOS Setup utility, the SEMA utility, the Watchdog Timer utility, and the board temperature sensors on the LEC-AL.

4.1 BIOS Setup

The LEC-AL features an AMI BIOS. The default settings provide a “ready to run” system, even without a BIOS setup backup battery.

The BIOS is located in flash memory and can be easily updated with software under DOS.

All setup changes of the BIOS are stored in the CMOS RAM.

The battery on the carrier will provide power to store that information for over two years without board activation.

This section presents the six primary menus of the BIOS Setup Utility. Use the following table as a quick reference for the contents of each primary menu in the BIOS Setup Utility. Each subsequent section provides an illustration of a primary menu followed by tables containing the setting options and submenus of the menu. The default setting options are presented in **bold**, and the function of each setting is described in the right hand column of the respective table.

Table 4-1: BIOS Setup Menu Structure

Main	Advanced	Chipset	Security	Boot	Save & Exit
• BIOS Information • System Information • Board Information► • System Date and Time • Access Level	• CPU Configuration► • Graphics Configuration► • Power Management► • System Management► • Thermal Management► • Watchdog Timer► • CSM Configuration► • Super IO Configuration► • Serial Console Redirection► • USB► • Network► • Miscellaneous► • Intel® I210 Gigabit Network Connection► • Driver Health► • AMI Graphic Output Protocol Policy► • SDIO Configuration►	• North Bridge► • South Bridge► • Uncore Configuration► • South Cluster Configuration►	• Setup Administrator Password • User Password • Secure Boot►	• Boot Configuration► • Setup Prompt Timeout • Bootup NumLock State • Quiet Boot • Fast Boot • New Boot Option Policy • Boot Mode Select • Boot Configuration • FIXED BOOT ORDER Priorities► • Boot Option #1 • Boot Option #2 • Boot Option #3 • Boot Option #4 • Boot Option #5 • Boot Option #6 • Boot Option #7 • Boot Option #8 • UEFI USB Key Drive BBS Priorities	• Save Change and Exit► • Discard Changes and Exit • Save Changes and Reset • Discard Changes and Reset • Save Options► • Boot Override►

Notes:
► indicates a submenu
Gray text indicates info only

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4.1.1 Starting the BIOS Setup Utility

Use the following bullets to initiate start-up activity for the BIOS Setup Utility.

- Press <DEL> during power up to start the BIOS setup utility.
- Press <F11> during power up to start the Boot menu.
- Press <END> during power up to return BIOS settings to default.

4.1.2 Main Menu

The Main Menu provides read-only information about your system and also allows you to set the System Date and Time. Refer to the tables below for details of the submenus and settings.

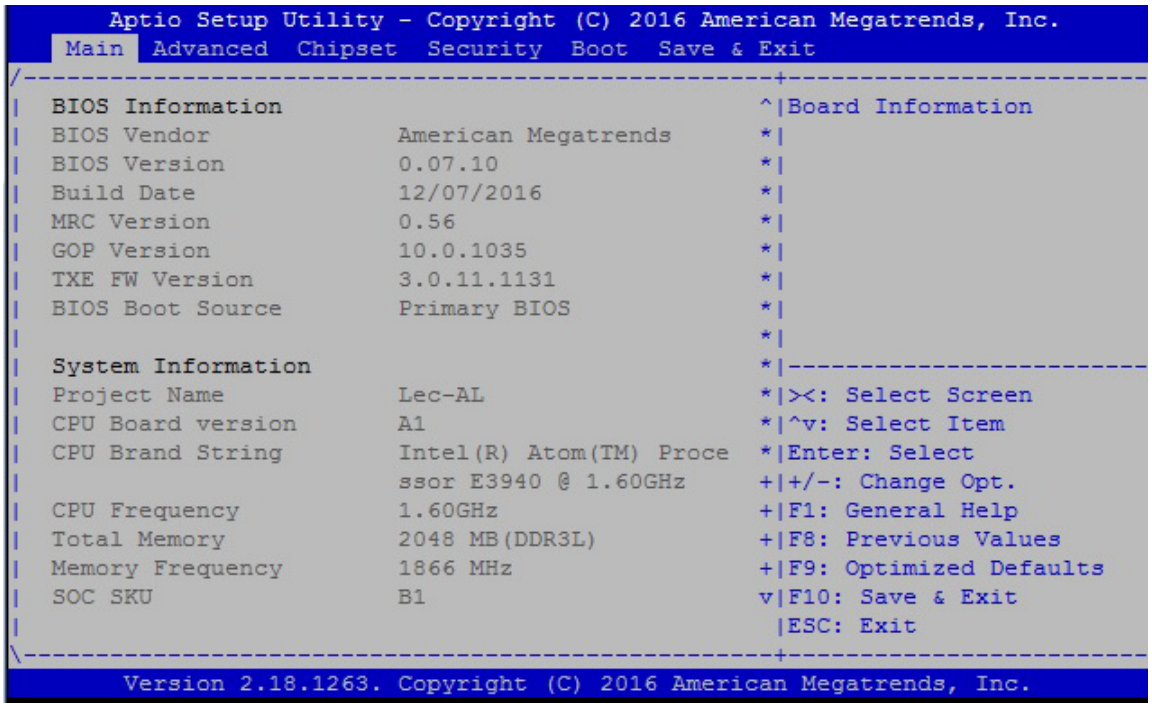


Figure 4-1: BIOS Setup Main Menu (Top)

Main > BIOS Information

Table 4-2: Main > BIOS Information

Feature	Options	Description
BIOS Vender	Info only	American Megatrends
BIOS Version	Info only	ADLINK BIOS version
Build Date	Info only	ADLINK BIOS Build Date
MRC Version	Info only	Display MRC Version
GOP Version	Info only	Display GOP Version
TXE FW Version	Info only	Display TXE FW Version
BIOS Boot Source	Info only	Display BIOS Boot Source

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Main > System Information

Table 4-3: Main > System Information

Feature	Options	Description
Project Name	Info only	Display Project Name
CPU Board version	Info only	Display CPU Board Version
CPU Board String	Info only	Display CPU Board String
CPU Frequency	Info only	Display CPU Frequency.
Total Memory	Info only	Display Installed Memory Size
Memory Frequency	Info only	Display Memory Frequency
SOC SKU	Info only	Display SOC SKU Version

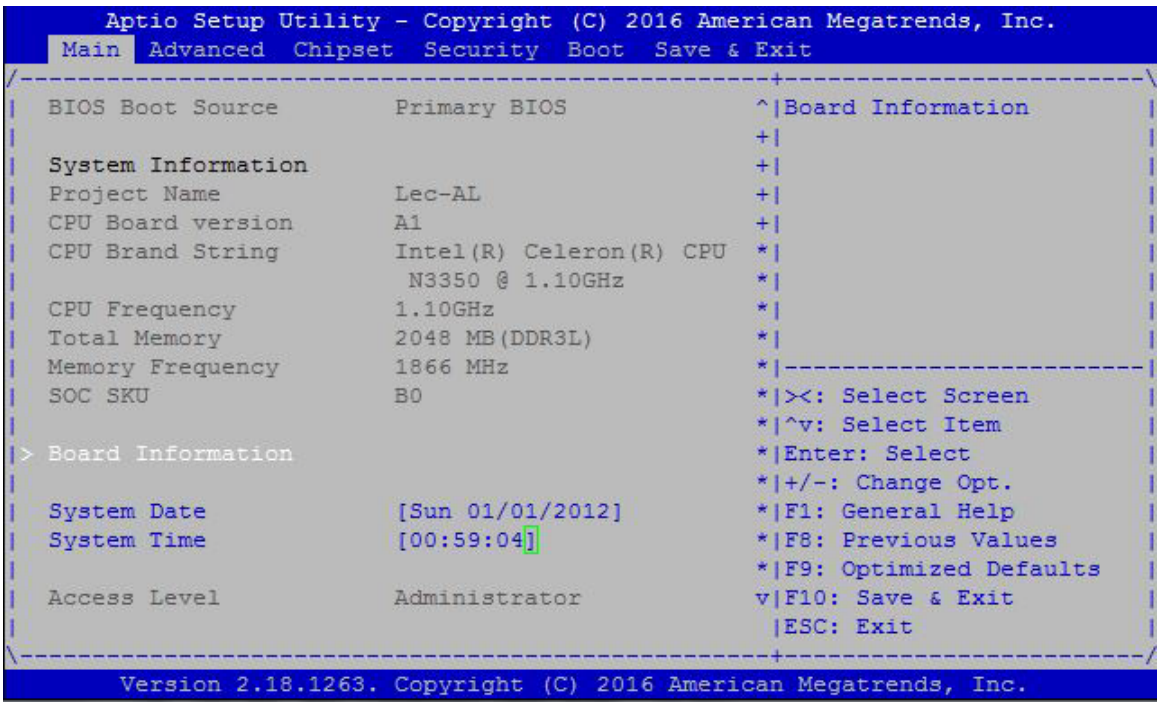


Figure 4-2: BIOS Setup Main Menu (Bottom)

Main > Board Information

Table 4-4: Main > Board Information

Feature	Options	Description
Board Information ▶	Submenu	
Board Information	Info only	
Serial Number	Info only	Display SEMA serial Number.
Manufacturing Date	Info only	Display SEMA manufacturing date.
Last Repair Date	Info only	Display SEMA last repair date.
MAC ID	Info only	Display SEMA MAC ID.
Runtime Statistics	Info only	

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Table 4-4: Main > Board Information (Continued)

Feature	Options	Description
Total Runtime	Info only	The returned value specifies the total time in minutes the system is running in S0 state.
Current Runtime	Info only	The returned value specifies the time in seconds the system is running in S0 state. This counter is cleared when the system is removed from the external power supply.
Power Cycles	Info only	The returned value specifies the number of times the external power supply has been shut down.
Boot Cycles	Info only	The Boot counter is increased after a HW- or SW-Reset or after a successful power-up.
Boot Reason	Info only	The boot reason is the event which causes the reboot of the system.

Main >System Date/Time

Table 4-5: Main > System Date and Time

Feature	Options	Description
System Date	Info only	
System Time	Info only	

Main >Access Level

Table 4-6: Main Menu > Access Level

Feature	Options	Description
Access Level	Info only	

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4.1.3 Advanced Menu

This menu contains the settings for most of the user interfaces in the system. The “Advanced” menu provides configuration settings for CPU, Graphics, Power Management, System Management, Thermal Management, Watchdog Timer, CSM, Super IO, Serial Console Redirection, USB, Miscellaneous, Gigabit Network Connection, Driver Health, AMI Graphic Output, and SDIO.



Inappropriate values for any of the following advanced settings below may cause system errors.

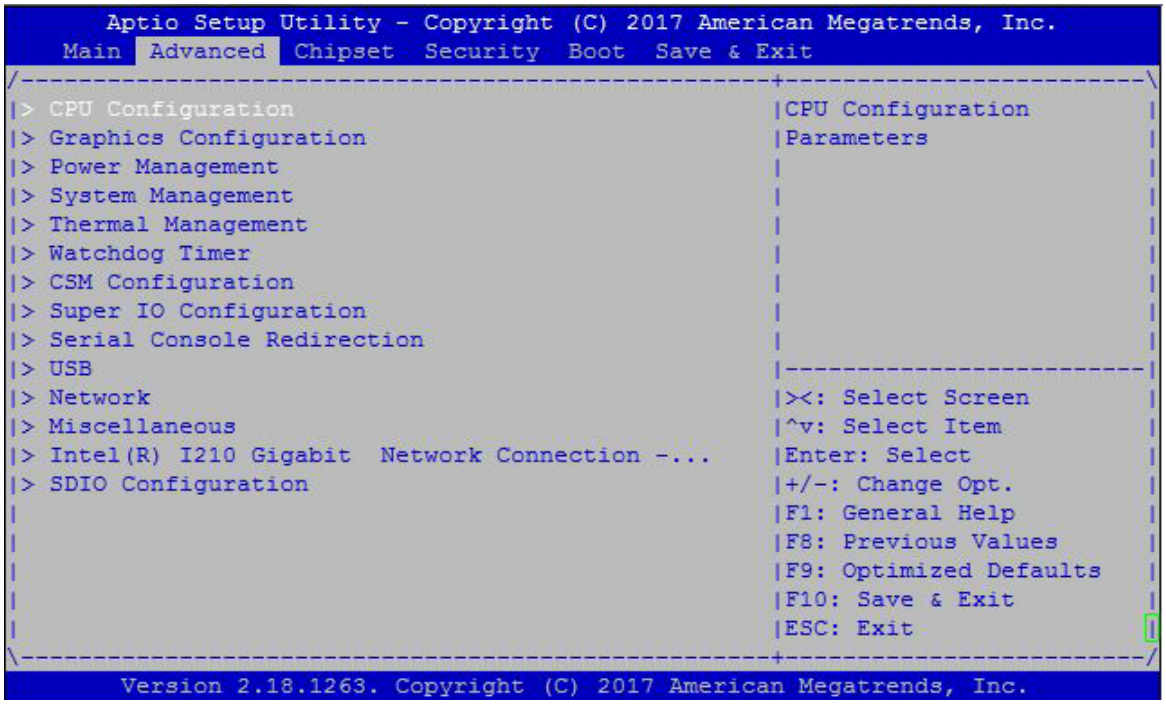


Figure 4-3: BIOS Setup Advanced Menu

Advanced > CPU Configuration

Table 4-7: Advanced > CPU Configuration

Feature	Options	Description
CPU Configuration	Info only	
Socket 0 CPU Information ▶	Submenu	Socket Specific CPU Information
Socket 0 CPU information	Info only	
CPU Signature	Info only	Display CPU Signature
Microcode Patch	Info only	Display Microcode Patch
Max CPU Speed	Info only	Display Max CPU speed
Min CPU speed	Info only	Display Min CPU speed
Processor Cores	Info only	Display Processor Cores
Intel HT Technology	Info only	Display Intel HT Technology support or not

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Table 4-7: Advanced > CPU Configuration (Continued)

Feature	Options	Description
Intel VT-x Technology	Info only	Display Intel VT-x Technology support or not
L1 Data Cache	Info only	Display cache info
L1 Code Cache	Info only	Display cache info
L2 Cache	Info only	Display cache info
L3 Cache	Info only	Display cache info
Speed	Info only	Display CPU Speed
64-bit	Info only	Display 64-bit Support
CPU Power Management ▶	Submenu	CPU Power Management options.
CPU Power Management Configuration	Info only	
EIST	Disabled **Enabled**	Enable / Disable Intel SpeedStep
Turbo Mode	Disabled **Enabled**	Enable / Disable turbo mode.
Boot performance mode	**Max Performance** Max Battery	Select the performance state that the BIOS will set before OS handoff.
C-States	Disabled **Enabled**	Enable / Disable C Sates.
Enhanced C-states	Disabled **Enabled**	Enable / Disable C1E. When enabled, CPU will switch to minimum speed when all core enter C-States.
Max Package C State	**PC2** PC1 C0	Controls the Max Package C State that the processor will support.
Max Core C State	**Core C6** Core C1	This option controls the Max Core C State that cores will Support.
C-State Auto Demotion	Disabled **C1**	Configure C-State Auto Demotion
C-State Un-demotion	Disabled **C1**	Configure C-State Auto Un-demotion
Power Limit 1 Enable	Disabled **Enabled**	Enable / Disable Power Limit 1
Power Limit 1	Info Only	Display Power Limit 1 Power Watts.
Power Limit 1 Clamp Mode	Disabled **Enabled**	Enable / Disable Power Limit 1 Clamp Mode.
Power Limit 1 Power	**Auto**, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25	Power Limit 1 in Watts. Auto will program Power Limit 1 based on silicon default support value.
Power Limit 1 Time Windows	**Auto**, 1, 2, 3, 4, 5, 6, 7, 8, 10, 12, 14, 16, 20, 24, 28, 32, 40, 48, 56, 64, 80, 96,112,128	Power Limit 1 Time Windows Value in Seconds. Auto will program Power Limit 1 Time Windows base on silicon default support value.
Active Processor Cores	**Disabled** Enabled	Number of cores to enable in each processor package.
Intel Virtualization Technology	Disabled **Enabled**	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

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Table 4-7: Advanced > CPU Configuration (Continued)

Feature	Options	Description
VT-d	Disabled **Enabled**	Enable / Disable CPU VT-d
Bi-directional PROCHOT	Disabled **Enabled**	When a processor thermal sensor trips (either core), the PROCHOT# will be driven. If bi-direction is enabled, external agents can drive PROCHOT# to throttle the processor.
Limit CPUID Maximum	**Disabled** Enabled	When **Enabled**, the processor will limit the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When **Disabled**, the processor will return the actual maximum CPUID input value
Execute Disable Bit	Disabled **Enabled**	Enable / Disable the Execute Disable Bit (XD) of the processor. With the XD bit set to enabled certain classes of malicious buffer overflow attacks can be prevented when combined with a supporting OS.
Thermal Monitor	Disabled **Enabled**	Enable / Disable Thermal Monitor.
Monitor Mwait	Disabled Enabled **Auto**	Enable / Disable Monitor Mwait.
P-STATE Coordination	**HW_ALL** SW_ALL SW_ANY	P-STATE Coordination type.
DTS	Disabled **Enabled**	Enable / Disable Digital Thermal Sensor.

Advanced > Graphics Configuration

Table 4-8: Advanced > Graphics Configuration

Feature	Options	Description
Graphics Configuration	Info only	
LVDS	Info only	
Data format and Color Depth	VESA 24 bpp JEIDA 24 bbp **JEIDA/vesa 18 bpp**	Data format and Color Depth select
LVDS Output Mode	Dual LVDS bus **Signal LVDS bus**	Signal / Dual mode select
DE Polarity	**Active High** Active Low	DE Polarity Select
Vsync Polarity	**Active High** Active Low	Vsync Polarity select
Hsync Polarity	**Active High** Active Low	Hsync Polarity select
LVDS Backlight Brightness	0 - **255**	LVDS Backlight Brightness adjust. A change takes effect immediately.

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Advanced > Power Management

Table 4-9: Advanced > Power Management

Feature	Options	Description
Power Management	Info only	
Enable ACPI Auto Configuration	**Disabled** Enabled	Enables or Disables BIOS ACPI Auto Configuration.
Enable Hibernation	Disabled **Enabled**	Enable or Disable System ability to Hibernate (OS/S4 Sleep State). This option maybe not effective with some OS.
ACPI Sleep State	Suspend Disable **S3 (Suspend to RAM)**	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
Emulation AT/ATX	Emulation AT **ATX**	Select Emulation AT or ATX function. If this option set to [Emulation AT], BIOS will report no suspend functions to ACPI OS. In windows XP, it will make OS show shutdown message during system shutdown.
Lock Legacy Resources	**Disabled** Enabled	Enables or Disables Lock of Legacy Resources.
LID Function	**Disabled** Enabled	Enable / Disable LID Function.
Power Consumption ▶	Submenu	Power Consumption.

Advanced > Power Management > Power Consumption

Table 4-10: Advanced > Power Management > Power Consumption

Feature	Options	Description
Power Consumption	Info Only	
Current Input Current	Info Only	Display Current Input Current
Current Input Power	Info Only	Display Current Input Power
VCORE	Info Only	Display VCORE Voltage
VGFX	Info Only	Display VGFX Voltage
VMEM	Info Only	Display VMEM Voltage
RTC	Info Only	Display RTC Voltage
3.3V	Info Only	Display 3.3V Voltage
3.3VSB	Info Only	Display 3.3VSB Voltage
VSMARC	Info Only	Display VSMARC Voltage

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Advanced > System Management

Table 4-11: Advanced > System Management

Feature	Options	Description
System Management	Info Only	
Version	Info Only	Display SEMA Module Version.
SEMA Firmware	Info Only	Display SEMA Firmware Version.
Build Date	Info Only	Display SEMA Firmware Build Date.
SEMA Bootloader	Info Only	Display SEMA Bootloader Version.
Build Date	Info Only	Display SEMA Bootloader Build Date.
SEMA Features ▶	Submenu	Display SEMA Supported Features
SEMA Supported Features	Info Only	Display SEMA Supported Features
Flags ▶	Submenu	Flag
Flags	Info Only	
BMC Flags	Info Only	
BIOS Select	Info Only	
ATX/AT-Mode	Info Only	
Exception Code	Info Only	

Advanced > Thermal Management

Table 4-12: Advanced > Thermal Management

Feature	Options	Description
Thermal Configuration Parameters	Info Only	
Thermal and Fan Speed ▶	Submenu	
Smart Fan ▶	Submenu	
Critical Trip Point	**Disabled** 80 C 90 C 95 C	The value is the temperature threshold of the Critical Trip Point.
Passive Cooling Trip Point	**Disabled** 70 C 80 C 90 C	The value is the temperature threshold of the Passive Cooling Trip Point.

Advanced > Thermal Management > Thermal and Fan Speed

Table 4-13: Advanced > Thermal Management > Thermal and Fan Speed

Feature	Options	Description
Temperatures and Fan Speed	Info Only	
CPU Temperature	Info Only	
Current	Info Only	Display Current CPU Temperature
Board Temperature	Info Only	
Current	Info Only	Display Current Board Temperature
Startup	Info Only	Display Startup Board Temperature
Min	Info Only	Display Min Board Temperature
Max	Info Only	Display Max Board Temperature
CPU Fan Speed	Info Only	Display CPU Fan Speed

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Advanced > Thermal Management > Smart Fan

Table 4-14: Advanced > Thermal Management > Smart Fan

Feature	Options	Description
Smart Fan	Info Only	
CPU Smart Fan Temperature Source	CPU Sensor **Board Sensor**	CPU Smart Fan Temperature Source
CPU Fan Mode	AUTO (Smart Fan) Fan Off **Fan On**	CPU Fan Mode
PWM Level	0 - **100**	Control PWM Level

Advanced > Watchdog Timer

Table 4-15: Advanced > Watchdog Timer

Feature	Options	Description
Watchdog Timer	Info Only	
Power-Up Watchdog	**Disabled** Enabled	The Power Up Watchdog resets the system after a certain amount of time after power up.

Advanced > CSM Configuration

Table 4-16: Advanced > CSM Configuration

Feature	Options	Description
Compatibility Support Module Configuration	Info Only	
CSM Support	**Disabled** Enabled	Enabled / Disabled CSM Support.

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Advanced > Serial Console Redirection

Table 4-17: Advanced > Serial Console Redirection

Feature	Options	Description
COM1	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings ▶	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. The item will be lunched before enable Console Redirection.
COM2	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings ▶	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. The item will be lunched before enable Console Redirection.
COM3	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings ▶	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. The item will be lunched before enable Console Redirection.
COM4	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings ▶	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. The item will be lunched before enable Console Redirection.
Legacy Console Redirection	Info only	
Legacy Console Redirection Settings ▶	Submenu	Legacy Console Redirection Settings

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Table 4-18: Advanced > Serial Console Redirection > Console Redirection Settings (If COM1 Enabled)

Feature	Options	Description
COM1	Info only	
Console Redirection Settings	Info only	
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7 **8**	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.They can be used as an additional data bit.
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
VT-UTF8 Combo Key Support	**Enabled** Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Resolution 100x31	Enabled **Disabled**	On Legacy OS, the Number of Rows and Columns supported redirection
Legacy OS Redirection Resolution	**80x24** 80x25	On Legacy OS, the Number of Rows and Columns supported redirection
Putty KeyPad	**VT100** Intel Linux XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.

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Table 4-18: Advanced > Serial Console Redirection > Console Redirection Settings (If COM1 Enabled) (Continued)

Feature	Options	Description
Redirection After BIOS POST	**Always Enable** BootLoader	When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always Enable.

Advanced > Serial Console Redirection > Console Redirection Settings (If COM2 Enable)

Table 4-19: Advanced > Serial Console Redirection > Console Redirection Settings (If COM2 Enabled)

Feature	Options	Description
COM2	Info only	
Console Redirection Settings	Info only	
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7 **8**	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.They can be used as an additional data bit.
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.

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Table 4-19: Advanced > Serial Console Redirection > Console Redirection Settings (If COM2 Enabled) (Continued)

Feature	Options	Description
VT-UTF8 Combo Key Support	**Enabled** Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Resolution 100x31	Enabled **Disabled**	On Legacy OS, the Number of Rows and Columns supported redirection
Legacy OS Redirection Resolution	**80x24** 80x25	On Legacy OS, the Number of Rows and Columns supported redirection
Putty KeyPad	**VT100** Intel Linux XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS POST	**Always Enable** BootLoader	When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always Enable.

Advanced > Serial Console Redirection > Console Redirection Settings (If COM3 Enable)

Table 4-20: Advanced > Serial Console Redirection > Console Redirection Settings (If COM3 Enabled)

Feature	Options	Description
COM3	Info only	
Console Redirection Settings	Info only	
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7 **8**	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.They can be used as an additional data bit.

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Table 4-20: Advanced > Serial Console Redirection > Console Redirection Settings (If COM3 Enabled) (Continued)

Feature	Options	Description
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
VT-UTF8 Combo Key Support	**Enabled** Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Resolution 100x31	Enabled **Disabled**	On Legacy OS, the Number of Rows and Columns supported redirection
Legacy OS Redirection Resolution	**80x24** 80x25	On Legacy OS, the Number of Rows and Columns supported redirection
Putty KeyPad	**VT100** Intel Linux XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS POST	**Always Enable** BootLoader	When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always Enable.

Advanced > Serial Console Redirection > Console Redirection Settings (If COM4 Enable)

Table 4-21: Advanced > Serial Console Redirection > Console Redirection Settings (If COM4 Enabled)

Feature	Options	Description
COM4	Info only	
Console Redirection Settings	Info only	
Terminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.

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Table 4-21: Advanced > Serial Console Redirection > Console Redirection Settings (If COM4 Enabled) (Continued)

Feature	Options	Description
Data Bits	7 **8**	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.They can be used as an additional data bit.
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
VT-UTF8 Combo Key Support	**Enabled** Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Resolution 100x31	Enabled **Disabled**	On Legacy OS, the Number of Rows and Columns supported redirection
Legacy OS Redirection Resolution	**80x24** 80x25	On Legacy OS, the Number of Rows and Columns supported redirection
Putty KeyPad	**VT100** Intel Linux XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS POST	**Always Enable** BootLoader	When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always Enable.

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Advanced > Serial Console Redirection > Legacy Console Redirection Settings

Table 4-22: Serial Console Redirection > Legacy Console Redirection Settings

Feature	Options	Description
Legacy Serial Redirection Port	**COM1** COM2 COM3 COM4	Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages

Advanced > USB

Table 4-23: Advanced > USB

Feature	Options	Description
USB	Info Only	
USB Module Version	Info Only	Display USB Module Version
USB Controllers	Info Only	Display USB Controllers are XHCI or EHCI.
USB Devices	Info Only	Display attachment USB devices.
Legacy USB Support	**Enabled** Disabled Auto	Enables Legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications.
XHCI Hand-off	**Enabled** Disabled	This is a workaround for Oses without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	Disabled **Enabled**	Enable / Disable USB Mass Storage Driver Support.
USB hardware delays and time-outs:	Info Only	
USB transfer rime-out	1 sec 5 sec 10 sec **20 sec**	The time-out value for Control, Bulk, and Interrupt transfers.
Device reset time-out	10 sec **20 sec** 30 sec 40 sec	USB mass storage device Start Unit command time-out.
Device power-up delay	**Auto** Manual	Maximum time the device will take before it properly reports itself to the Hot Controller. ‘Auto’ uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken form Hub descriptor.

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Advanced > Network

Table 4-24: Advanced > Network

Feature	Options	Description
Onboard LAN Controller	Disable **Enable**	Enable / Disable Onboard Intel I210LM Lan controller.
Network Stack	**Disable** Enable	Enable / Disable UEFI Network Stack.

Advanced > Miscellaneous

Table 4-25: Advanced > Miscellaneous

Feature	Options	Description
Miscellaneous	Info Only	Control the PCI Express Root Port.
Smart Battery Function	**Disable** Enable	Enable / Disable Battery Function

Advanced > Intel® I210 Gigabit Network Connection

Table 4-26: Advanced > Intel I210 Gigabit Network Connection

Feature	Options	Description
PORT CONFIGURATION MENU	Info Only	
NIC Configuration ▶	Submenu	Click to configure the network device port.
Blink LEDs	**0**	Identify the physical network port by blinking the associated LED
PORT CONFIGURATION INFORMATION	Info Only	
UEFI Driver	Info Only	
Adapter PBA	Info Only	
Chip Type	Info Only	
PCI Device ID	Info Only	
PCI Address	Info Only	
Link Status	Info Only	
MAC Address	Info only	
Virtual MAC Address	Info Only	

Advanced > Intel® I210 Gigabit Network Connection>NIC Configuration

Table 4-27: Advanced > Intel I210 Gigabit Network Connection > NIC

Feature	Options	Description
Link Speed	**Auto Negotiated** 10Mbps Half 10Mbps Full 100Mbps Half 100Mbps Full	Specifies the port speed used for the selected boot protocol.
Wake On LAN	Disable **Enable**	Enables the server to be powered on using an in-band magic packet.

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Advanced > SDIO Configuration

Table 4-28: Advanced > SDIO Configuration

Feature	Options	Description
SDIO Configuration	Info only	
SDIO Access Mode	**Auto** ADMA SDMA PIO	Auto Option: Access SD device in DMA mode if controller supports it, otherwise, in PIO mode.DMA Option: Access SD device in DMA mode. PIO Option: Access SD device in PIO mode.
Mass Storage Devices:	Info only	
Sdio Device 1 Details:	Info only	
Bus 0 Dev 1c Func 0	Info only	
MMC – xxxx(xx.xGB)	**Auto** Floppy Forced FDD Hard Disk	Mass storage device emulation type. 'AUTO' enumerates devices less than 530MB as floppies. Forced FDD option can be used to force HDD formatted drive to boot as FDD.

4.1.4 Chipset Menu

The Chipset menu allows you to set Northbridge and Southbridge system functions.

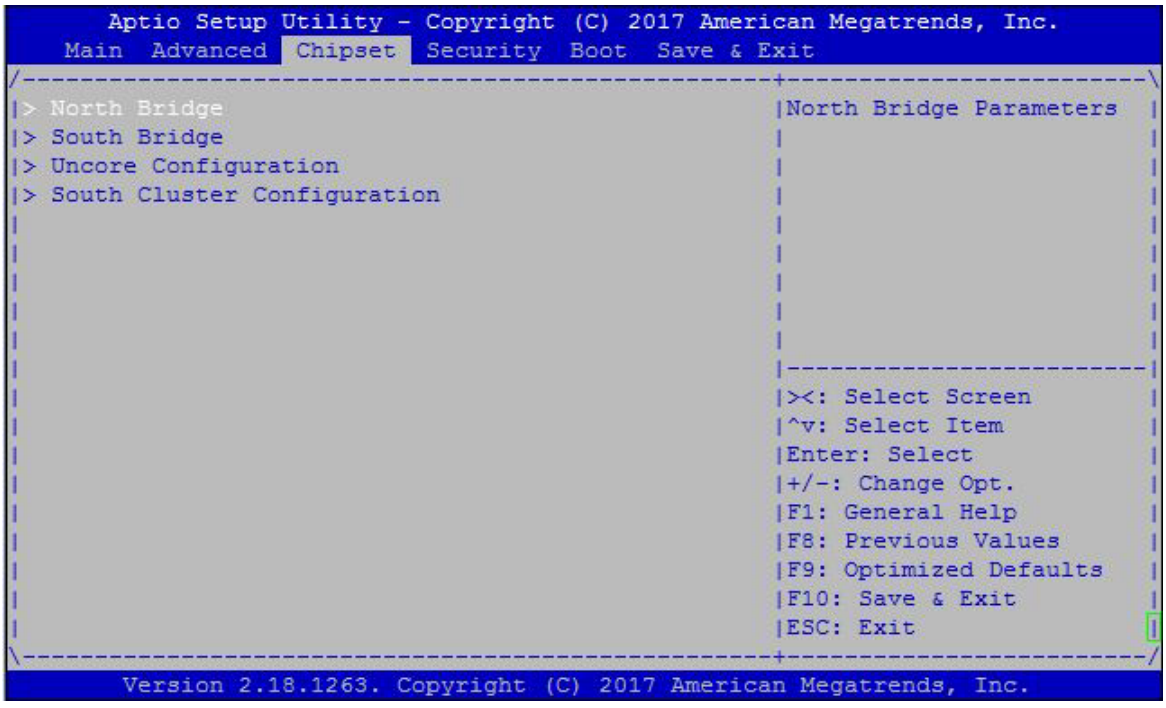


Figure 4-4: BIOS Setup Chipset Menu

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Chipset > North Bridge

Table 4-29: Chipset > North Bridge

Feature	Options	Description
Memory Information	Info only	
Total Memory	Info only	Display Total Memory Size.
Memory Voltage	Info only	Display Memory Voltige.
Memory Slot0	Info only	Display Installed Memory Slot0 Information.
Memory Slot1	Info only	Display Installed Memory Slot1 Information.
Max TOLUD	**2 GB** 2.25 GB 2.5 GB 2.75 GB 3 GB	Maximum Value of TOLUD.
PCIE VGA Workaround	**Disable** Enable	Enable it if your PCIe card cannot boot to DOS. This is for Test only.

Chipset > South Bridge

Table 4-30: Chipset > South Bridge

Feature	Options	Description
Serial IRQ Mode	Quiet **Continuous**	Configure Serial IRQ Mode.
SMBus Support	Disable **Enable**	Enable / Disable SMBus Support.
OS Selection	**Windows** Android Win7 Intel Linux	Select the target OS.
PCI CLOCK RUN	Disable **Enable**	Enables CLKRUN# logic to stop PCI clocks.
Real Time Option	**RT Disabled** RT Enabled, Agent IDI1 RT Enabled, Agent Disabled	Select Read-Time Enable and IDI Agent Real-Time Traffic Mask Bits

Chipset > Uncore Configuration

Table 4-31: Chipset > Uncore Configuration

Feature	Options	Description
GOP Configuration	Info only	
Active LFP Config	**No LFP** eDP/LVDS	Active Local Flat Panel Config.
LVDS Backlight Mode	GTT Mode **BMC Mode**	Select LVDS Backlight control function.
DDI port 1	No Device DisplayPort HDMI **DisplayPort with HDMI/ DVI Compatible**	DDI port 1 function choose to DisplayPort or HDMI.

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Table 4-31: Chipset > Uncore Configuration (Continued)

Feature	Options	Description
DDI port 2	No Device DisplayPort HDMI **DisplayPort with HDMI/ DVI Compatible**	DDI port 2 function choose to DisplayPort or HDMI.
LFP Panel Type	**Auto** 640x480 800x600 1024x768 1280x1024 1400x1050(RB) LVDS1 1400x1050 LVDS2 1600x1200 LVDS 1366x768 LVDS 1680x1050 1920x1200 1440x900 LVDS 1600x900 LVDS 1024x768 LVDS2 1280x800 1920x1080 LVDS 2048x1536 LVDS	Select LFP panel used by Internal Graphics Device by selecting the appropriate setup item.
GOP Brightness Level	20, 40, 60, 80, 100, 120, **140**, 160, 180, 200, 220, 240, 255	Set GOP Brightness Level.
IGD Configuration	Info only	
Integrated Graphics Devices	Disable **Enable**	Enable: Enable Integrated Graphics Device (IGD) when selected as the Primary Video Adaptor. Disable: Always disable IGD.
Primary Display	**IGD** PCIe HG	Select which of IGD / PCI Graphics device should be Primary Display.
Aperture Size	128MB **256MB** 512MB	Select the Aperture Size.
DVMT Pre-Allocated	**64M**, 96M, 128M, 160M, 192M, 224M, 256M, 288M, 320M, 352M, 384M, 416M, 448M, 480M, 512M	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device
DVMT Total Gfx Mem	128M **256M** MAX	Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device

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Chipset > South Cluster Configuration

Table 4-32: Chipset > South Cluster Configuration

Feature	Options	Description
HD-Audio Configuration ▶	Submenu	HD-Audio Configuration Setting.
PCI Express Configuration ▶	Submenu	PCI Express Configuration Setting.
SATA Drives ▶	Submenu	Press <Enter> to select the SATA Device Configuration Setup option.
SSC Configuration ▶	Submenu	SSC Configuration Settings.
USB Configuration ▶	Submenu	USB Configuration Settings.
Miscellaneous Configuration ▶	Submenu	Enable / Disable Misc. Feature.

Chipset > South Cluster Configuration > HD-Audio Configuration

Table 4-33: Chipset > South Cluster Configuration > HD-Audio Configuration

Feature	Options	Description
HD-Audio Configuration	Info only	
HD-Audio Support	Disable **Enable**	Select the target OS.
HD-Audio I/O Buffer Ownership Select	**I2S port owns all the I/O buffers** HD-Audio link owns all the I/O buffers	HD-Audio link owns 4 I/O buffers and I2S port owns 4 I/O buffers

Chipset > South Cluster Configuration > PCI Express Configuration

Table 4-34: Chipset > South Cluster Configuration > PCI Express Configuration

Feature	Options	Description
PCI Express Configuration	Info only	
PCIE Port assigned to LAN	Info only	Display PCIE Port assigned to LAN Information.
Compliance Mode	Disable **Enable**	Compliance Mode Enable / Disable.
PCIE Port 1-4 Configuration	**4x1 Port** 1x2 2x1 Port 2x2 Port 1x4 Port	To configure PCI-E Port 1-4 of PCH. [4X1]:Port 1-4 (x1) and Port 8 (x1) [1x2 2x1]:Port 1 (x2), Port 2 (disabled), Ports 3 and Port 4 (x1) [2x2]:Port 1-2 (x2) and Port 3-4 (x2) [1x4]:Port 1 (x4), Ports 2-4 (disabled)
PCI ExpressRoot Port 1 ▶	Submenu	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port Disable: Disable PCIe root port

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Table 4-34: Chipset > South Cluster Configuration > PCI Express Configuration (Continued)

Feature	Options	Description
PCI ExpressRoot Port 2 ▶	Submenu	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port Disable: Disable PCIe root port
PCI ExpressRoot Port 3 ▶	Submenu	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port Disable: Disable PCIe root port
PCI ExpressRoot Port 4 ▶	Submenu	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port Disable: Disable PCIe root port

Chipset > South Chuster Configuration > PCI Express Configuration > PCI Express Root Port 1

Table 4-35: Chipset > South Cluster Configuration > PCI Express Configuration > PCI Express Root Port 1

Feature	Options	Description
PCI Express Root Port 1	Disable **Enable** Auto	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port. Disable: Disable PCIe root port.
ASPM	Disable **Enable**	PCI Express Active State Power Management settings
L1 Substates	Disable L1.1 L1.2 **L1.1 & L1.2**	PCI Express L1 Substates settings.
ACS	Disable **Enable**	Enable/Disable Access Control Services Extended Capability
URR	**Disable** Enable	CI Express Unsupported Request Reporting Enable/Disable
FER	**Disable** Enable	PCI Express Device Fatal Error Reporting Enable/Disable
NFER	**Disable** Enable	PCI Express Device Non-Fatal Error Reporting Enable/Disable
CER	**Disable** Enable	PCI Express Device Correctable Error Reporting Enable/Disable
CTO	**Default Setting** 16-15 ms 65-210 ms 260-900 ms 1-3.5 s Disable	PCI Express Completion Timer TO Enable/Disable.

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Table 4-35: Chipset > South Cluster Configuration > PCI Express Configuration > PCI Express Root Port 1 (Continued)

Feature	Options	Description
SEFE	**Disable** Enable	Root PCI Express System Error on Fatal Error Enable/Disable
SENFE	**Disable** Enable	Root PCI Express System Error on Non-Fatal Error Enable/Disable
SECE	**Disable** Enable	Root PCI Express System Error on Correctable Error Enable/Disable
PME SCI	Disable **Enable**	PCI Express PME SCI Enable/Disable
Hot Plug	**Disable** Enable	PCI Express Hot Plug Enable/Disable
PCIe Speed	**Auto** Gen1 Gen2	Configure PCIe Speed
Transmitter Half Swing	**Disable** Enable	Transmitter Half Swing Enable/Disable.
Extra Bus Reserved	**0**	Extra Bus Reserved (0-7) for bridges behind this Root Bridge
Reserved Memory	**10**	Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge
Reserved I/O	**4**	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge
PCH PCIe LTR Configuration	Info only	
PCH PCIE LTR	Disable **Enable**	PCH PCIE Latency Reporting Enable/ Disable
Snoop Latency Override	Disabled Manual **Auto**	Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Non Snoop Latency Override	Disabled Manual **Auto**	Non Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow
PCIE LTR Lock	**Disable** Enable	PCIE LTR Configuration Lock
PCIe Selection De-emphasis	Disable **Enable**	When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. 1b -3.5 dB 0b -6 dB

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Chipset > South Chuster Configuration > PCI Express Configuration > PCI Express Root Port 2

Table 4-36: Chipset >South Cluster Configuration >PCI Express Configuration>PCI Express Root Port 2

Feature	Options	Description
PCI Express Root Port 2	Disable **Enable** Auto	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port. Disable: Disable PCIe root port.
ASPM	Disable **Enable**	PCI Express Active State Power Management settings
L1 Substates	Disable L1.1 L1.2 **L1.1 & L1.2**	PCI Express L1 Substates settings.
ACS	Disable **Enable**	Enable/Disable Access Control Services Extended Capability
URR	**Disable** Enable	CI Express Unsupported Request Reporting Enable/Disable
FER	**Disable** Enable	PCI Express Device Fatal Error Reporting Enable/Disable
NFER	**Disable** Enable	PCI Express Device Non-Fatal Error Reporting Enable/Disable
CER	**Disable** Enable	PCI Express Device Correctable Error Reporting Enable/Disable
CTO	**Default Setting** 16-15 ms 65-210 ms 260-900 ms 1-3.5 s Disable	PCI Express Completion Timer TO Enable/Disable.
SEFE	**Disable** Enable	Root PCI Express System Error on Fatal Error Enable/Disable
SENFE	**Disable** Enable	Root PCI Express System Error on Non-Fatal Error Enable/Disable
SECE	**Disable** Enable	Root PCI Express System Error on Correctable Error Enable/Disable
PME SCI	Disable **Enable**	PCI Express PME SCI Enable/Disable
Hot Plug	**Disable** Enable	PCI Express Hot Plug Enable/Disable
PCIe Speed	**Auto** Gen1 Gen2	Configure PCIe Speed
Transmitter Half Swing	**Disable** Enable	Transmitter Half Swing Enable/Disable.
Extra Bus Reserved	**0**	Extra Bus Reserved (0-7) for bridges behind this Root Bridge
Reserved Memory	**10**	Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge
Reserved I/O	**4**	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge

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Table 4-36: Chipset >South Cluster Configuration >PCI Express Configuration>PCI Express Root Port 2 (Continued)

Feature	Options	Description
PCH PCIe LTR Configuration	Info only	
PCH PCIE LTR	Disable **Enable**	PCH PCIE Latency Reporting Enable/ Disable
Snoop Latency Override	Disabled Manual **Auto**	Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Non Snoop Latency Override	Disabled Manual **Auto**	Non Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow
PCIE LTR Lock	**Disable** Enable	PCIE LTR Configuration Lock
PCIe Selection De0emphasis	Disable **Enable**	When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. 1b -3.5 dB 0b -6 dB

Chipset > South Chuster Configuration > PCI Express Configuration > PCI Express Root Port 3

Table 4-37: Chipset > South Cluster Configuration > PCI Express Configuration> PCI Express Root Port 3

Feature	Options	Description
PCI Express Root Port 3	Disable **Enable** Auto	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port. Disable: Disable PCIe root port.
ASPM	Disable **Enable**	PCI Express Active State Power Management settings
L1 Substates	Disable L1.1 L1.2 **L1.1 & L1.2**	PCI Express L1 Substates settings.
ACS	Disable **Enable**	Enable/Disable Access Control Services Extended Capability
URR	**Disable** Enable	CI Express Unsupported Request Reporting Enable/Disable
FER	**Disable** Enable	PCI Express Device Fatal Error Reporting Enable/Disable
NFER	**Disable** Enable	PCI Express Device Non-Fatal Error Reporting Enable/Disable
CER	**Disable** Enable	PCI Express Device Correctable Error Reporting Enable/Disable

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Table 4-37: Chipset > South Cluster Configuration > PCI Express Configuration> PCI Express Root Port 3 (Continued)

Feature	Options	Description
CTO	**Default Setting** 16-15 ms 65-210 ms 260-900 ms 1-3.5 s Disable	PCI Express Completion Timer TO Enable/Disable.
SEFE	**Disable** Enable	Root PCI Express System Error on Fatal Error Enable/Disable
SENFE	**Disable** Enable	Root PCI Express System Error on Non-Fatal Error Enable/Disable
SECE	**Disable** Enable	Root PCI Express System Error on Correctable Error Enable/Disable
PME SCI	Disable **Enable**	PCI Express PME SCI Enable/Disable
Hot Plug	**Disable** Enable	PCI Express Hot Plug Enable/Disable
PCIe Speed	**Auto** Gen1 Gen2	Configure PCIe Speed
Transmitter Half Swing	**Disable** Enable	Transmitter Half Swing Enable/Disable.
Extra Bus Reserved	**0**	Extra Bus Reserved (0-7) for bridges behind this Root Bridge
Reserved Memory	**10**	Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge
Reserved I/O	**4**	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge
PCH PCIe LTR Configuration	Info only	
PCH PCIE LTR	Disable **Enable**	PCH PCIE Latency Reporting Enable/ Disable
Snoop Latency Override	Disabled Manual **Auto**	Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Non Snoop Latency Override	Disabled Manual **Auto**	Non Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow
PCIE LTR Lock	**Disable** Enable	PCIE LTR Configuration Lock
PCIe Selection De0emphasis	Disable **Enable**	When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. 1b -3.5 dB 0b -6 dB

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Table 4-38: Chipset > South Cluster Configuration > PCI Express Configuration > PCI Express Root Port 4

Feature	Options	Description
PCI Express Root Port 4	Disable **Enable** Auto	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port. Disable: Disable PCIe root port.
ASPM	Disable **Enable**	PCI Express Active State Power Management settings
L1 Substates	Disable L1.1 L1.2 **L1.1 & L1.2**	PCI Express L1 Substates settings.
ACS	Disable **Enable**	Enable/Disable Access Control Services Extended Capability
URR	**Disable** Enable	CI Express Unsupported Request Reporting Enable/Disable
FER	**Disable** Enable	PCI Express Device Fatal Error Reporting Enable/Disable
NFER	**Disable** Enable	PCI Express Device Non-Fatal Error Reporting Enable/Disable
CER	**Disable** Enable	PCI Express Device Correctable Error Reporting Enable/Disable
CTO	**Default Setting** 16-15 ms 65-210 ms 260-900 ms 1-3.5 s Disable	PCI Express Completion Timer TO Enable/Disable.
SEFE	**Disable** Enable	Root PCI Express System Error on Fatal Error Enable/Disable
SENFE	**Disable** Enable	Root PCI Express System Error on Non-Fatal Error Enable/Disable
SECE	**Disable** Enable	Root PCI Express System Error on Correctable Error Enable/Disable
PME SCI	Disable **Enable**	PCI Express PME SCI Enable/Disable
Hot Plug	**Disable** Enable	PCI Express Hot Plug Enable/Disable
PCIe Speed	**Auto** Gen1 Gen2	Configure PCIe Speed
Transmitter Half Swing	**Disable** Enable	Transmitter Half Swing Enable/Disable.
Extra Bus Reserved	**0**	Extra Bus Reserved (0-7) for bridges behind this Root Bridge
Reserved Memory	**10**	Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge
Reserved I/O	**4**	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge

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Table 4-38: Chipset > South Cluster Configuration > PCI Express Configuration > PCI Express Root Port 4 (Continued)

Feature	Options	Description
PCH PCIe LTR Configuration	Info only	
PCH PCIE LTR	Disable **Enable**	PCH PCIE Latency Reporting Enable/ Disable
Snoop Latency Override	Disabled Manual **Auto**	Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Non Snoop Latency Override	Disabled Manual **Auto**	Non Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow
PCIE LTR Lock	**Disable** Enable	PCIE LTR Configuration Lock
PCIe Selection De0emphasis	Disable **Enable**	When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. 1b -3.5 dB 0b -6 dB

Chipset > South Cluster Configuration > SATA Drives

Table 4-39: Chipset > South Cluster Configuration > SATA Drives

Feature	Options	Description
SATA Drives	Info only	
Chipset- SATA Controller Configuration	Info only	
Chipset SATA	Disable **Enable**	Enables or Disables the Chipset SATA Controller. The Chipset SATA controller supports the 2 black internal SATA ports (up to 3Gb/s supported per port).
SATA Mode Selection	**AHCI**	Determines how SATA controller(s) operate.
SATA Interface Speed	Gen1 **Gen2** Gen3	Select SATA Interface Speed, CHV A1 always with Gen Speed.
SATA Test Mode	**Disabled** Enabled	Test Mode Enable / Disable.
Aggressive LPM Support	**Disabled** Enabled	Enable PCH to Aggressively enter link power state.
SATA0	Info only	
Software Preserve	Info only	
Port 0	Disabled **Enabled**	Enable / Disable SATA Port
SATA Port 0 Hot Plug Capability	**Disabled** Enabled	If enabled, SATA port will be reported as Hot Plug capable.
Configured as eSATA	Info only	Display Configured as eSATA support.

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Table 4-39: Chipset > South Cluster Configuration > SATA Drives (Continued)

Feature	Options	Description
Mechanical Presence Switch	Disabled **Enabled**	Controls reporting if this port has a Mechanical Presence Switch. Note. Request Hardware support.
Spin Up Device	Disabled **Enabled**	If enabled for any of ports, Staggered Spin Up will be performed, and only the drives which have this option enabled will spin up at boot. Otherwise, all drives spin up at boot.
SATA Device Type	**Hard Disk Drive** Solid State Drive	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.
SATA Port 0 DevSlp	**Disabled** Enabled	Enable/Disable SATA Port 0 DevSlp. Board rework for LP needed before enable.
DITO Configuration	**Disabled** Enabled	Enable/Disable DITO Configuration
DITO Value	**625**	DITO Value. Note. DITO Value can be accessed if DITO Configuration item must enable.
DM Value	**15**	DM Value. Note. DM Value can be accessed if DITO Configuration item must enable.
SATA1	Info only	
Software Preserve	Info only	
Port 1	Disabled **Enabled**	Enable / Disable SATA Port
SATA Port 1 Hot Plug Capability	**Disabled** Enabled	If enabled, SATA port will be reported as Hot Plug capable.
Configured as eSATA	Info only	Display Configured as eSATA support.
Mechanical Presence Switch	Disabled **Enabled**	Controls reporting if this port has a Mechanical Presence Switch. Note. Request Hardware support.
Spin Up Device	**Disabled** Enabled	If enabled for any of ports, Staggered Spin Up will be performed, and only the drives which have this option enabled will spin up at boot. Otherwise, all drives spin up at boot.
SATA Device Type	**Hard Disk Drive** Solid State Drive	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.
SATA Port 1 DevSlp	**Disabled** Enabled	Enable/Disable SATA Port 1 DevSlp. Board rework for LP needed before enable.
DITO Configuration	**Disabled** Enabled	Enable/Disable DITO Configuration
DITO Value	**625**	DITO Value. Note. DITO Value can be accessed if DITO Configuration item must enable.
DM Value	**15**	DM Value. Note. DM Value can be accessed if DITO Configuration item must enable.

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Chipset > South Cluster Configuration > SSC Configuration

Table 4-40: Chipset > South Cluster Configuration > SSC Configuration

Feature	Options	Description
SSC SD Card Support (D27:F0)	Disabled **Enabled**	Enable / Disable SCC SD Card Support.
SCC eMMC Support (D28:F0)	Disabled **Enabled**	Enable / Disable SCC eMMC Support.
eMMC Max Speed	**HS400** HS200 DDR50	Select the eMMC max Speed allowed.

Chipset > South Cluster Configuration > USB Configuration

Table 4-41: Chipset > South Cluster Configuration > USB Configuration

Feature	Options	Description
XHCI Pre-Boot Driver	**Disabled** Enabled	Enable / Disable XHCI Pre-Boot Driver support.
XHCI Mode	Disabled **Enabled**	Once disabled, XHCI controller would be function disabled, none of the USB devices are detectable and usable during boot and in OS. Do not disable it unless for debug purpose.
USB Port Disable Override	**Disabled** Enabled	Selectively Enable/Disable the corresponding USB port from reporting a Device Connection to the controller.
USB OTG Support	**Disabled** Enabled	Enable/Disable USB OTG

Chipset > South Cluster Configuration > Miscellaneous Configuration

Table 4-42: Chipset > South Cluster Configuration > Miscellaneous Configuration

Feature	Options	Description
Miscellaneous Configuration	Info only	
State After G3	**S0 State** S5 State Last State	Specify what state to go to when power is re-applied after a power failure (G3 state). S0 State: System will boot directly as soon as power applied. S5 State: System keeps in power-off state until power button is pressed.
Wake On Lan	**Disabled** Enabled	Enable or Disable the Wake on Lan.

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4.1.5 Security Menu

The Security menu allows you to set User and Administrator system passwords and to retrieve secure boot information.

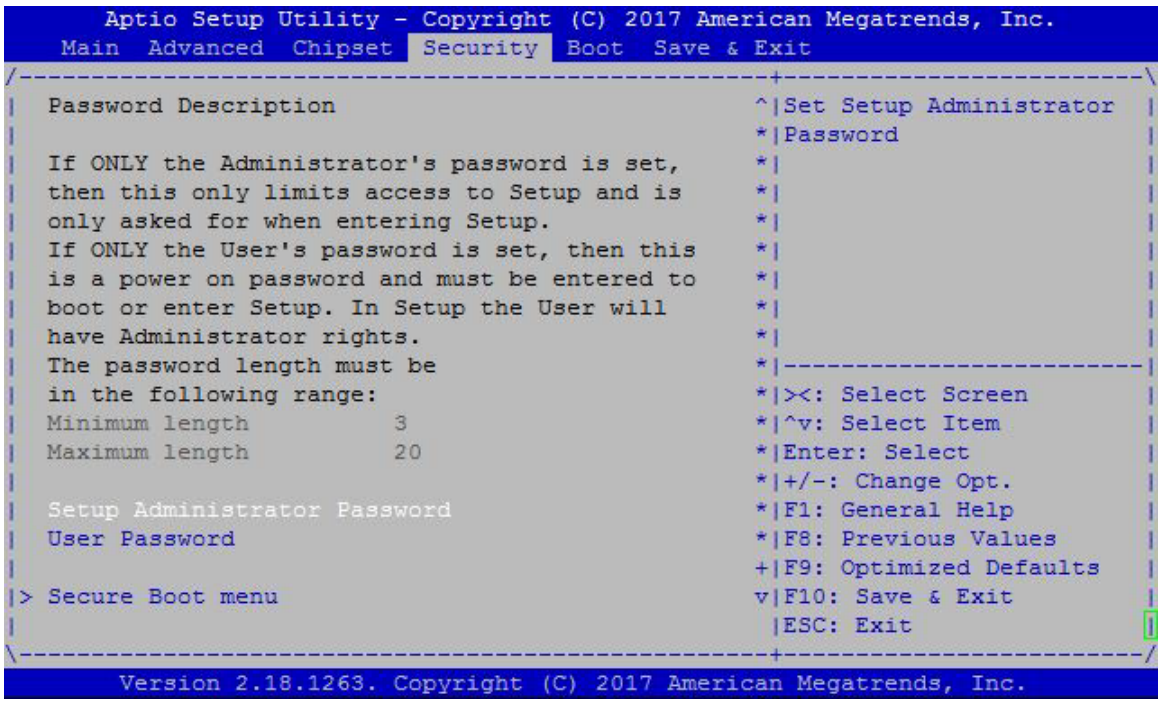


Figure 4-5: BIOS Setup Security Menu

Security > Password Description

Table 4-43: Security > Password Description

Feature	Options	Description
Password Description	Info only	
Setup Administrator Password	Enter Password	Set Setup Administrator Password
User Password	Enter Password	Set User Password
Secure Boot ▶	Submenu	Customizable Secure Boot settings
System Mode	Info only	
Secure Boot	Info only	
Secure Boot Control	**Disabled** Enabled	Secure Boot activated when Platform Key (PK) is enrolled, System mode is User / Deployed, and CSM function is disabled
HDD Security Configuration ▶	Submenu	HDD Security Configuration
HDD Password Description	Info Only	
HDD Password Configuration	Info Only	
Set User Password	Enter Password	Set User Password

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4.1.6 Boot Menu

The Boot menu allows you to configure how your system will boot and select the storage location from which the system boot up will occur.

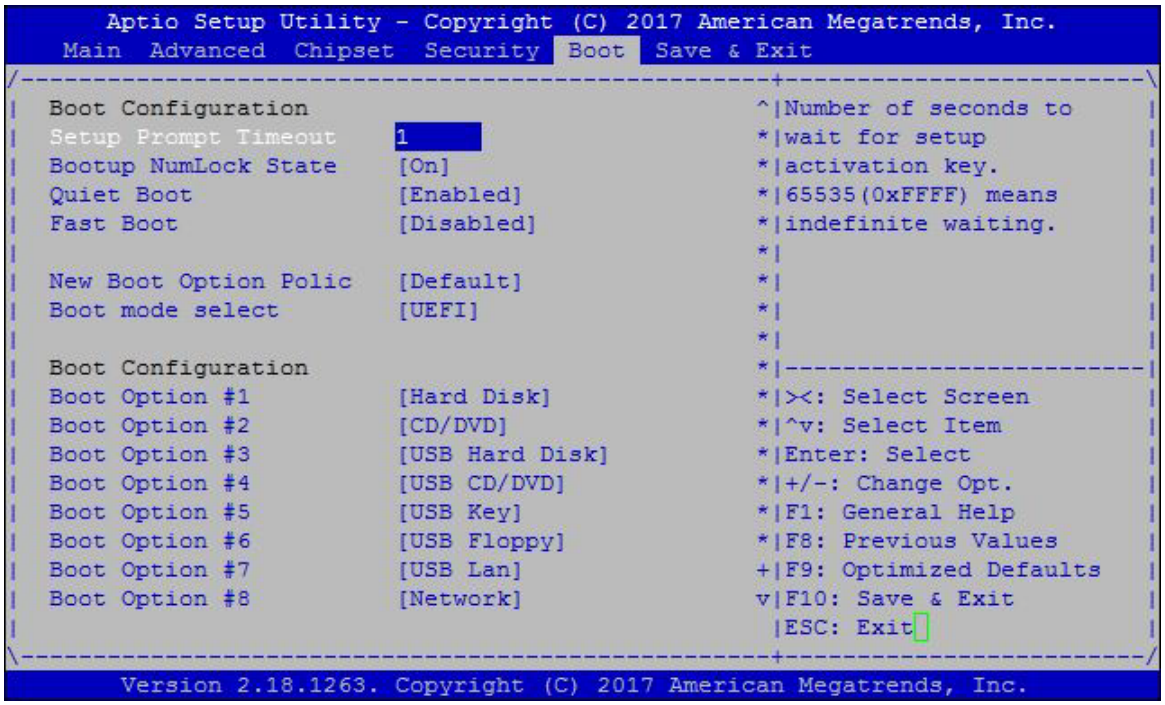


Figure 4-6: BIOS Setup Boot Menu

Boot > Boot Configuration

Table 4-44: Boot > Boot Configuration

Feature	Options	Description
Boot Configuration	Info only	
Setup Prompt Timeout	**1**	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
Bootup NumLock State	**On** Off	Select the keyboard Number state.
Ouiet Boot	Disabled **Enabled**	Select the keyboard NumLock state.
Fast Boot	**Disabled** Enabled	Enable or Disable FastBoot features. Most probes are skipped to reduce time cost during boot.
New Boot Option Policy	**Default** Place First Place Last	Controls the placement of newly detected UEFI boot option.
Boot Mode Select	**UEFI** LEGACY	Select boot mode LEGACY/UEFI
Boot Configuration	Info Only	

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Boot > FIXED BOOT ORDER Priorities

Table 4-45: Boot > FIXED BOOT ORDER Priorities

Feature	Options	Description
Boot Option #1	**Hardware**	Set the system boot order.
Boot Option #2	**CD/DVD**	Set the system boot order.
Boot Option #3	**USB Hard Disk**	Set the system boot order.
Boot Option #4	**USB CD/DVD**	Set the system boot order.
Boot Option #5	**USB Key**	Set the system boot order.
Boot Option #6	**USB Floppy**	Set the system boot order.
Boot Option #7	**USB Lan**	Set the system boot order.
Boot Option #8	**Network**	Set the system boot order.

4.1.7 Save & Exit Menu

Use the Save and Exit menu to save or discard BIOS setting changes, restore or save setting defaults, and retrieve certain override information.

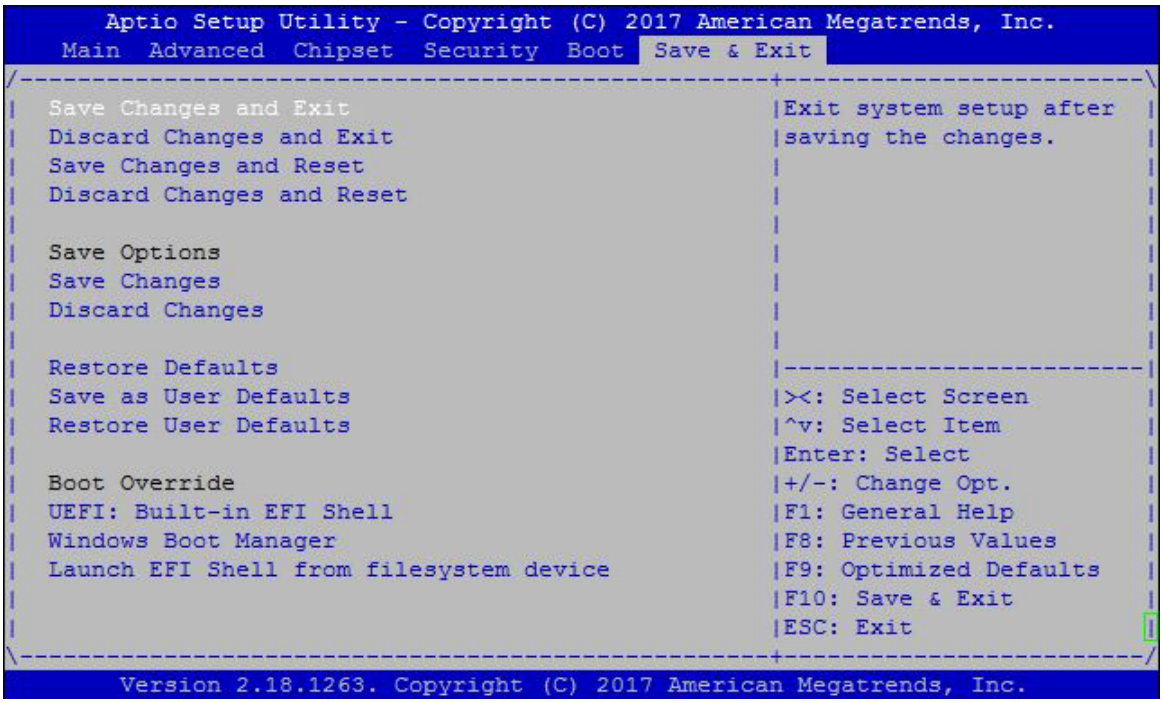


Figure 4-7: BIOS Setup Save and Exit Menu

Save and Exit

Table 4-46: Save and Exit

Feature	Options	Description
Save Changes and Exit		Exit system setup after saving the changes.
Discard Changes and Exit		Exit system setup without saving any changes.
Save Change and Reset		Reset the system after saving the changes.

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Table 4-46: Save and Exit (Continued)

Feature	Options	Description
Discard Changes and Reset		Reset system setup without saving any changes.
Save Options	Info only	
Save Changes		Save Changes done so far to any of the setup options.
Save as User Defaults		Save the changes done so far as User Defaults.
Restore User Defaults		Restore the User Defaults to all the setup options.
Boot Override	Info only	

4.2 SEMA functions

Under the management of the BMC chip (Board Management Controller), the SEMA utility (Smart Embedded Management Agent) provides system control and failure protection—counting, monitoring, and measuring hardware and software events, from which the SoC can trigger corrective commands. The optional SEMA Cloud utility not only controls local events on the module but system client events on the Internet of Things (IoT.) Refer to the following bullets for a list of SEMA functions.

- Total operating hours counter
  Counts the time the module has been run in minutes.
- On-time minutes counter
  Counts the seconds since last system start.
- Temperature monitoring of CPU and Board temperature
  Minimum and maximum temperature values of CPU and board are stored in flash.
- Power monitor
  Reads the current drawn by the board and reports the nominal operating voltage.
- Power cycles counter
- Boot counter
  Boot counter is increased after a HW- or SW-Reset or after a successful power-up.
- Watchdog Timer
  Set / Reset / Disable Watchdog Timer.
- System Restart Cause
  Power loss / Watchdog / External Reset.
- Flash area
  1kB Flash area for customer data
- Protected Flash area
  128 Bytes for Keys, ID's, etc. can be stored in a write- and clear-protectable region.
- Board Identify
  Vendor / Board / Serial number

The SEMA Tools are available for Windows and Linux. SEMA functionality can also be used in applications. Refer to the SEMA software manual and technical manual on the ADLINK web site for more information.

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4.2.1 Board Specific SEMA functions

Voltages

The BMC of the LEC-AL implements a Voltage Monitor and samples several Onboard Voltages. The Voltages can be read by calling the SEMA function, “Get Voltages”. The function returns a 16-bit value divided in Hi-Byte (MSB) and Lo-Byte (LSB).

Table 4-47: BMC Voltage Monitor Values

ADC Channel	Voltage Name	Voltage Formula [V]
0	VCORE	(MSB<<8 + LSB) * 3.3 / 1024
1	VGFX	(MSB<<8 + LSB) * 3.3 / 1024
3	VMEM	(MSB<<8 + LSB) * 3.3 / 1024
5	RTC	(MSB<<8 + LSB) * 3.3 / 1024
6	3.3V+	(MSB<<8 + LSB) * 1.100 * 3.3 / 1024
7	3.3VSB	(MSB<<8 + LSB) * 3.3 / 1024
15	VSMARC	(MSB<<8 + LSB) * 1.826 * 3.3 / 1024
16	(MAINCURRENT)	Use Main Current Function

Main Current

The BMC of the LEC-AL implements a Current Monitor. The current can be read by calling the SEMA function “Get Main Current”. The function returns four 16-bit values divided in Hi-Byte (MSB) and Lo-Byte (LSB). These four values represent the last four currents drawn by the board. The values are sampled every 250ms. The order of the four values is NOT in relationship to time. The access to the BMC may increase the drawn current of the whole system. In this case, you still have three samples without the influence of the read access.

Main Current = (MSB_n<<8 + LSB_n) * 8.06mA

TS#-Events

TS# is activated by a temperature sensor when a device reaches its critical temperature and released when the device is back in its normal temperature range. This counter gives the user information about temperature or cooling issues. This counter is cleared when the system is removed from power. The LEC-AL only monitors the board temperature and does not support TS#-Events.

Exception Blink Codes

In the case of an error, the BMC shows a blink code on the STATUS-LED (LED1). This error code is also reported by the BMC Flags register. The Exception Code is not stored in the Flash storage and is cleared when the power is removed. Therefore, the “Clear Exception Code”-Command is not supported.

Table 4-48: Blink Codes

Exception Blink Code	Error Message	Description
0	NOERROR	
2	NO_SUSCLK	No connection to SUSCLK
3	NO_SLP_S4_S5	No signal from PCH for SLP_S4-S5
4	NO_SLP_S3	No signal from PCH for SLP_S3

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Table 4-48: Blink Codes (Continued)

Exception Blink Code	Error Message	Description
5	BIOS_FAIL	BIOS failure
6	RESET_FAIL	Reset failure
7	RESETIN_FAIL	Reset In failure
8	NO_VIN_PWR_BAD	No VIN_PWR_BAD signal
9	CRITICAL TEMP	Critical temperature violation
10	POWER_FAIL	Power failure
11	VOLTAGE_FAIL	Voltage failure
12	NO_3V3_5V_A_PG	No 3V3_5V_A Power Good signal
13	NO_VNN_PG	No VNN Power Good signal
14	NO_1V24_A_PG	No 1V24 Power Good signal
15	NO_VDDQ_PG	No VDDQ Power Good signal
16	NO_V1P05S_PG	No V1P05S Power Good signal
17	NO_V3P3_S0_PG	No V3P3_S0 Power Good signal
18	NO_V12	No V12 input
19	MEMORY_ERROR	SDRAM error
20	NO_P3V3_A_READY	No P3V3_A_READY signal

BMC Flags

The BMC Flags register returns the last detected exception code since power up.

4.3 Watchdog Timer

The LEC-AL features three separate Watchdog Timers. One of them is integrated in the SoC and two are provided by the BMC (managed by the SEMA).

The SoC Watchdog can be configured in the BIOS or by programming the Watchdog registers. If this function is used by user application, the application has to provide all logging functionality if desired.

The BMC Watchdog activations are caused by under voltage protection. The Watchdog LED flashes after restart but only if the power supply reaches 4.2V.

4.4 Temperature Sensors

The LEC-AL supports two temperature sensor functions. One is offered from the SoC and one from a dedicated chip (Texas Instruments LM73) on the board.

The SoC temperature sensors can be configured by programming the appropriate SoC registers. Refer to the Thermal Management chapters in the N-series and E-series Intel processor data sheets for more information. The on-board LM73 temperature sensor is managed by the BMC and is configured through the SEMA utility.

4.5 Programming Examples

Programming examples can be provided based on a Linux operating system, upon request.

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Appendix A System Resources

Table A-1: Memory Map

Address Range	Description		
FF00_0000 – FFFF_FFFF	IFAW (BIOS)		
FED0_0000 – FEDF_33FF FEC0_0000 – FECF_FFFF	HPET IOAPIC		
0K –1MB	DOS DRAM		

Table A-2: I/O Map

I/O Address	IOSF Primary Target	IOSF SB Target
000h–01Fh	P2SB	Terminate
020h–021h	P2SB	ITSS (interrupt)
024h–025h	P2SB	ITSS (interrupt)
028h–029h	P2SB	ITSS (interrupt)
02Ch–02Dh	P2SB	ITSS (interrupt)
02Eh–02Fh	P2SB	LPC/eSPI
030h–031h	P2SB	ITSS (interrupt)
034h–035h	P2SB	ITSS (interrupt)
038h–039h	P2SB	ITSS (interrupt)
03Ch–03Dh	P2SB	ITSS (interrupt)
040h	P2SB	ITSS (Timer 0 Register)
041h	P2SB	Terminate
042h	P2SB	ITSS (Timer 2 Register)
043h	P2SB	ITSS (Timer Control Word Register)
04Eh–04Fh	LPC/eSPI	LPC/eSPI
050h	P2SB	ITSS (alias of 040h)
051h	P2SB	Terminate
052h	P2SB	ITSS (alias of 042h)
053h	P2SB	ITSS (alias of 043h)
060h	P2SB	LPC/eSPI
061h	P2SB	ITSS (CPU I/F)
062h	P2SB	LPC/eSPI
063h	P2SB	ITSS (CPU I/F)
064h	P2SB	LPC/eSPI
065h	P2SB	ITSS (CPU I/F)
066h	P2SB	LPC/eSPI
067h	P2SB	ITSS (CPU I/F)
070h	P2SB	ITSS (CPU I/F), RTC, PMC
071h	P2SB	RTC, PMC
072h–073h	P2SB	RTC, PMC

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Table A-2: I/O Map (Continued)

I/O Address	IOSF Primary Target	IOSF SB Target
073h	P2SB	RTC, PMC
074h	P2SB	RTC, PMC
075h	P2SB	RTC, PMC
076h–077h	P2SB	RTC, PMC
080h	P2SB	LPC/eSPI or PMC
081h–083h	P2SB	Terminate
084h–086h	P2SB	LPC/eSPI or PMC
087h	P2SB	Terminate
088h	P2SB	LPC/eSPI or PMC
089h–08Bh	P2SB	Terminate
08Ch–08Eh	P2SB	LPC/eSPI or PMC
08Fh	P2SB	Terminate
090h	P2SB	LPC/eSPI
091h	P2SB	Terminate
092h	P2SB	ITSS (CPU I/F)
093h	P2SB	Terminate
094h–096h	P2SB	LPC/eSPI or PMC
097h	P2SB	Terminate
098h	P2SB	LPC/eSPI or PMC
099h–09Bh	P2SB	Terminate
09Ch–09Eh	P2SB	LPC/eSPI or PMC
09Fh	P2SB	Terminate
0A0h–0A1h	P2SB	ITSS (interrupt)
0A4h–0A5h	P2SB	ITSS (interrupt)
0A8h–0A9h	P2SB	ITSS (interrupt)
0ACh–0ADh	P2SB	ITSS (interrupt)
0B0h–0B1h	P2SB	ITSS (interrupt)
0B2h–0B3h	P2SB	PMC
0B4h–0B5h	P2SB	ITSS (interrupt)
0B8h–0B9h	P2SB	ITSS (interrupt)
0BCh–0BDh	P2SB	ITSS (interrupt)
0C0h–0DFh	P2SB	Terminate
0F0h	P2SB	Terminate
170h–177h	P2SB	Terminate
376h	P2SB	Terminate
3F6h	P2SB	Terminate
4D0h–4D1h	P2SB	ITSS (interrupt)
CF9h	P2SB	ITSS (CPU I/F)

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Table A-3: Interrupt Request (IRQ) Lines

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
0	Counter 0	N/A	No
1	Keyboard controller	IRQ1 via SERIRQ	No
2	Cascade interrupt from slave PIC	N/A	No
3	Generic	IRQ3 via SERIRQ / PIRQ	Note (1)
4	Generic	IRQ4 via SERIRQ / PIRQ	Note (1)
5	Generic	IRQ5 via SERIRQ / PIRQ	Note (1)
6	Generic	IRQ6 via SERIRQ / PIRQ	No
7	Generic	IRQ7 via SERIRQ / PIRQ	Note (1)
8	Real-time clock	N/A	No
9	Generic	N/A	Note (1)
10	Generic	IRQ10 via SERIRQ / PIRQ	Note (1)
11	Generic	IRQ11 via SERIRQ / PIRQ	Note (1)
12	PS/2 Mouse	IRQ12 via SERIRQ / PIRQ	Note (1)
13	Math Processor	N/A	No
14	SATA Primary	IRQ14 via SERIRQ / PIRQ	Note (1)
15	SATA Secondary	IRQ15 via SERIRQ / PIRQ	Note (1)

Notes:

These IRQs can be used for PCI devices when onboard device is disabled.

Table A-4: IRQ Lines APIC Mode

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
0	Counter 0	N/A	No
1	Keyboard controller	IRQ1 via SERIRQ	No
2	Cascade interrupt from slave PIC	N/A	No
3	N/A	N/A	Note (1)
4	N/A	N/A	Note (1)
5	N/A	N/A	Note (1)
6	N/A	N/A	Note (1)
7	N/A	N/A	Note (1)
8	Real-time clock	N/A	No
9	N/A	IRQ9 via SERIRQ	Note (1)
10	N/A	N/A	Note (1)
11	N/A	IRQ11 via SERIRQN/A	Note (1)
12	PS/2 Mouse	IRQ12 via SERIRQ	Note (1)
13	FERR# logic	N/A	Note (1)
14	SATA Primary	IRQ14 via SERIRQ	Note (1)
15	SATA Secondary	IRQ15 via SERIRQ	Note (1)

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Table A-4: IRQ Lines APIC Mode (Continued)

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
16	N/A	P.E.G Root Port, Intel HDA, PCIE Port 0/1/2/3/4/5/6, EHCI Controller #2, I.G.D, XHCI Controller	Note (1)
17	N/A	PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port	Note (1)
18	N/A	PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port, SMBus Controller, EHCI Controller #2	Note (1)
19	N/A	PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port,	Note (1)
20	N/A	Gbe Controller	Note (1)
21	N/A		Note (1)
22	N/A	Intel HDA	Note (1)
23	N/A	EHCI Controller #1	Note (1)

Note: These IRQs can be used for PCI devices when onboard device is disabled.

Table A-5: PCI Configuration Space Map

Logical Function	Bus	Device	Function
Host Bridge	0	0	0
DPTF (Camarillo)	0	0	1
NPK	0	0	2
NPK (PSF ghost)	0	0	5
GMM	0	0	3
Gen	0	2	0
Iunit	0	3	0
Reserved (CSE)		7	0
P2SB	0	13	0
PMC	0	13	1
SPI	0	13	2
Shared SRAM	0	13	3
Audio	0	14	0
CSE-HECI1	0	15	0
CSE-HECI2	0	15	1
CSE-HECI3	0	15	2
CSE-fTPM (PSF ghost)	0	15	7
CSE-HOFFL	0	16	0
ISH	0	17	0
SATA	0	18	0
PCIe-A 0	0	19	0
PCIe-A 1	0	19	1
PCIe-A 2	0	19	2
PCIe-A 3	0	19	3
PCIe-B 0	0	20	0
PCIe-B 1	0	20	1
USB-Host (xHCI)	0	21	0

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Table A-5: PCI Configuration Space Map (Continued)

Logical Function	Bus	Device	Function
USB-Device (xDCI)	0	21	1
I2C 0	0	22	0
I2C 1	0	22	1
I2C 2	0	22	2
I2C 3	0	22	3
CSE I2C 6/7 access	0	22	6
CSE SSRAM access	0	22	7
I2C 4	0	23	0
I2C 5	0	23	1
I2C 6	0	23	2
I2C 7	0	23	3
UART 0	0	24	0
UART 1	0	24	1
UART 2	0	24	2
UART 3	0	24	3
SPI 0	0	25	0
SPI 1	0	25	1
SPI 2	0	25	2
PWM	0	26	0
SD Card	0	27	0
eMMC	0	28	0
UFS	0	29	0
SDIO	0	30	0
LPC	0	31	0
SMBUS	0	31	1

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Appendix B Technical Support

ADLINK Technology, Inc. provides a number of methods for contacting Technical Support listed in Table A-1 below. Requests for support through Ask an Expert are given the highest priorities, and usually will be addressed within one working day.

- ADLINK Ask an Expert – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the ADLINK web site at http://www.adlinktech.com/AAE/. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online if you wish to use the Ask a Question feature.

ADLINK strongly suggests that you register with the web site. By creating a profile on the ADLINK web site, you will have a portal page called “My ADLINK”, unique to you with access to exclusive services and account information.

- Personal Assistance – You may also request personal assistance by creating an Ask an Expert account and then going to the Ask a Question feature. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request, you must log in to go to the My Question area where you can check status, update your request, and access other features.
- Download Service – This service is also free and available 24 hours a day at http://www.adlinktech.com. For certain downloads such as technical documents and software, you must register online before you can log in to this service.

Table B-1: Technical Support Contact Information

Method	Contact Information
Ask an Expert	http://www.adlinktech.com/AAE/
Web Site	http://www.adlinktech.com
Standard Mail	**ADLINK Technology, Inc.** Address: 9F, No.166 Jian Yi Road, Zhonghe District New Taipei City 235, Taiwan 新北市中和區建一路 166 號 9 樓 Tel: +886-2-8226-5877 Fax: +886-2-8226-5717 Email: service@adlinktech.com **Ampro ADLINK Technology, Inc.** Address: 5215 Hellyer Avenue, #110 San Jose, CA 95138, USA Tel: +1-408-360-0200 Toll Free: +1-800-966-5200 (USA only) Fax: +1-408-360-0222 Email: info@adlinktech.com **ADLINK Technology (China) Co., Ltd.** Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203) 300 Fang Chun Rd., Zhangjiang Hi-Tech Park Pudong New Area, Shanghai, 201203 China Tel: +86-21-5132-8988 Fax: +86-21-5132-3588 Email: market@adlinktech.com

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Table B-1: Technical Support Contact Information (Continued)

	ADLINK Technology GmbH Address: Hans-Thoma-Strasse 11 D-68163 Mannheim, Germany Tel: +49-621-43214-0 Fax: +49-621 43214-30 Email: emea@adlinktech.com Please visit the contact page at www.adlinktech.com for information on how to contact the ADLINK regional office nearest you.

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