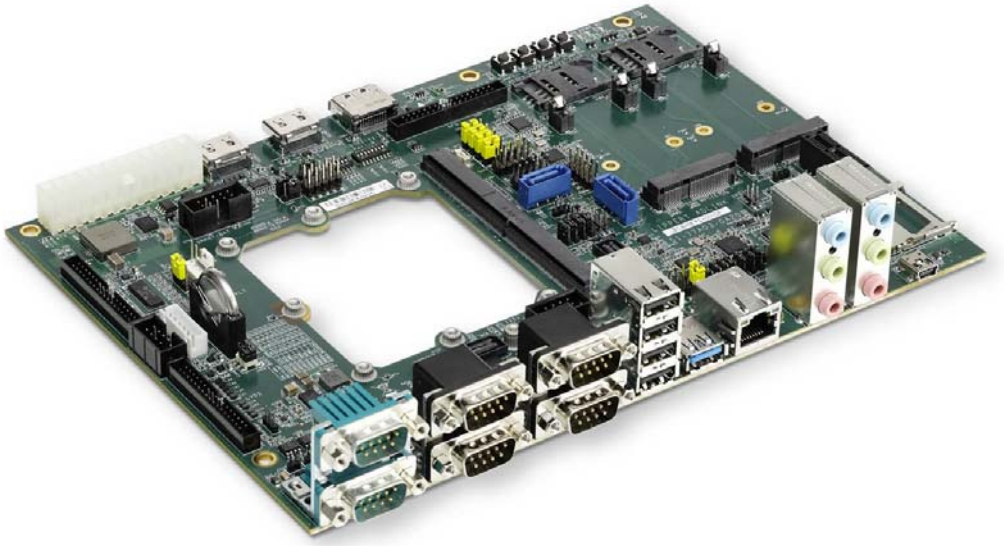
LEC-BASE MINI

(Low Energy Computer-On-Module Carrier)

Technical Reference
P/N 50-1Z213-1000
Rev 1.00



Advance Technologies. Automate the World.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Preface

Disclaimer

Information in this document is provided in connection with ADLINK products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in ADLINK´s Terms and Conditions of Sale for such products, ADLINK assumes no liability whatsoever, and ADLINK disclaims any express or implied warranty, relating to sale and/or use of ADLINK products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. If you intend to use ADLINK products in or as medical devices, you are solely responsible for all required regulatory compliance, including, without limitation, Title 21 of the CFR (US), Directive 2007/47/EC (EU), and ISO 13485 & 14971, if any. ADLINK may make changes to specifications and product descriptions at any time, without notice.

Trademarks

Product names mentioned herein are used for identification purposes only and may be trademarks and/or registered trademarks of their respective companies.

Revision History

Revision	Date	Description of Change(s)
1.00	06/27/2016	Initial Release

© Copyright 2016 ADLINK Technology, Incorporated

www.adlinktech.com

This document contains proprietary information protected by copyright. All rights are reserved. No part of this manual may be reproduced by any mechanical, electronic, or other means in any form without prior written permission of the manufacturer.

Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Environmental Responsibility

ADLINK is committed to fulfill its social responsibility to global environmental preservation through compliance with the European Union's Restriction of Hazardous Substances (RoHS) directive and Waste Electrical and Electronic Equipment (WEEE) directive. Environmental protection is a top priority for ADLINK. We have enforced measures to ensure that our products, manufacturing processes, components, and raw materials have as little impact on the environment as possible. When products are at their end of life, our customers are encouraged to dispose of them in accordance with the product disposal and/or recovery programs prescribed by their nation or company.

Important Safety Instructions

For user safety, please read and follow all **Instructions**, **WARNINGs**, **CAUTIONs,** and **NOTEs** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Conventions

The following conventions may be used throughout this manual, denoting special levels of information.



This information adds clarity or specifics to text and illustrations.



This information indicates the possibility of ***minor*** physical injury, component damage, data loss, and/or program corruption.



This information warns of possible ***serious*** physical injury, component damage, data loss, and/or program corruption.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Table of Contents

1 Product Overview 1
1.1 Carrier Description 1
1.2 Features 2
1.3 Ordering Information 3
1.4 Block Diagram 4
1.5 Specifications 5
1.5.1 Physical 5
1.5.2 Electrical 5
1.5.3 Environmental 5
1.5.4 Mechanical 6

2 Hardware 7
2.1 Interface Headers, Jumper Headers, Switches, LEDs, and Connectors 7
2.2 Standard Hardware References 13
2.2.1 Audio IO Jacks 13
2.2.2 PCIe Mini Card Slot 14
2.2.3 SDIO Slot 15
2.2.4 SIM Slot 16
2.2.5 Battery Socket 17

3 Interfaces 19
3.1 Standard USB Interfaces 19
3.2 ATX Power (CN2) 20
3.3 BattMan Enable (CN3) 20
3.4 ATX Power Supply Enable (CN4) 21
3.5 PCIe A x1 (CN14) 21
3.6 SDMMC Interface (CN20) 22
3.7 SPDIF I/O [CODEC] (CN22) 23
3.8 Display Interfaces 24
3.8.1 LCD RGB Backlight (CN16) 24
3.8.2 LCD RGB (CN17) 25
3.8.3 LVDS (CN25) 26
3.8.4 LVDS Voltage Select (CN26) 27
3.8.5 LVDS Backlight (CN27) 27
3.9 CAN 0-1 (Controller Area Network - CN28) 27
3.10 CAN0 Termination (CN29) 28
3.11 CAN1 Termination (CN30) 28
3.12 SPI0 (CN31) 28
3.13 SPI1 (CN32) 29
3.14 Serial Interfaces 29
3.14.1 COM0 and COM2 (CN33) 29
3.14.2 COM1 and COM3 (CN34) 30
3.15 GPIO 0-3 (CN35) 31
3.16 Alternate Function Block (CN37) 31
3.17 GPIO 4-7 (CN39) 33

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.18 GPIO 8-11 (CN41) 34
3.19 Miscellaneous (CN43) 34
3.20 I2S1 (CN44) 35
3.21 Smart Battery (BattMan) Interface (CN45) 35
3.22 Battery Enable (CN46) 36
3.23 Boot Select (CN48, CN49, CN50, CN51) 36
3.24 FAN Voltage Select (CN52) 36
3.25 FAN (CN53) 37
3.26 SPI Power Voltage Select (CN54) 37
3.27 SPDIF I/O [SMARC] (CN55) 37
3.28 MIC_BIAS to MIC Enable (CN57) 37
3.29 I2S0_SDIN Codec Select (CN58) 38
3.30 I2S0_SDOUT Codec Select (CN59) 38
3.31 I2S0_LRCK Codec Select (CN60) 38
3.32 I2S0_CK Codec Select (CN61) 38
3.33 LIN_L Codec Select (CN62) 39
3.34 LIN_R Codec Select (CN63) 39
3.35 LOUT_L Codec Select (CN64) 39
3.36 LOUT_R Codec Select (CN65) 39
3.37 MIC_BIAS Codec Select (CN66) 40
3.38 MIC Codec Select (CN67) 40
3.39 GND_ANALOG Codec Select (CN68) 40
3.40 I2C CAM (CN69) 40
3.41 I2C GP (CN70) 41
3.42 I2C LCD (CN71) 41
3.43 I2C PM (CN72) 41
3.44 Camera, PCAM / CSI (CN80) 41
3.45 VIN_PWR_BAD Source Select (CN81) 42
3.46 BatMan SMBus Voltage Select (CN82) 43
3.47 Display Mode Select (CN85) 43
3.48 Display Port Control Switch (SW6) 43
3.49 Display Port Control Switch (SW7) 43

Appendix A Technical Support 45

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

1 Product Overview

This chapter presents a general overview of the LEC-BASE MINI carrier. After reviewing this chapter you should understand the following features of the LEC-BASE MINI carrier board.

- Carrier Description
- I/O Features
- Functional Block Diagram
- Connector Locations and Descriptions
- Carrier Specifications

1.1 Carrier Description

The ADLINK LEC-BASE MINI is the host carrier board for ADLINK's SMARC modules and serves as reference design for SMARC modules. The SMARC module plugs directly into the LEC-BASE MINI where the carrier board becomes a design platform for testing and developing your applications. Figure 1-1 provides an overview photo of the LEC-BASE MINI with call outs of its interface hardware. The proceeding chapters and sections in this manual present these features in more detail.

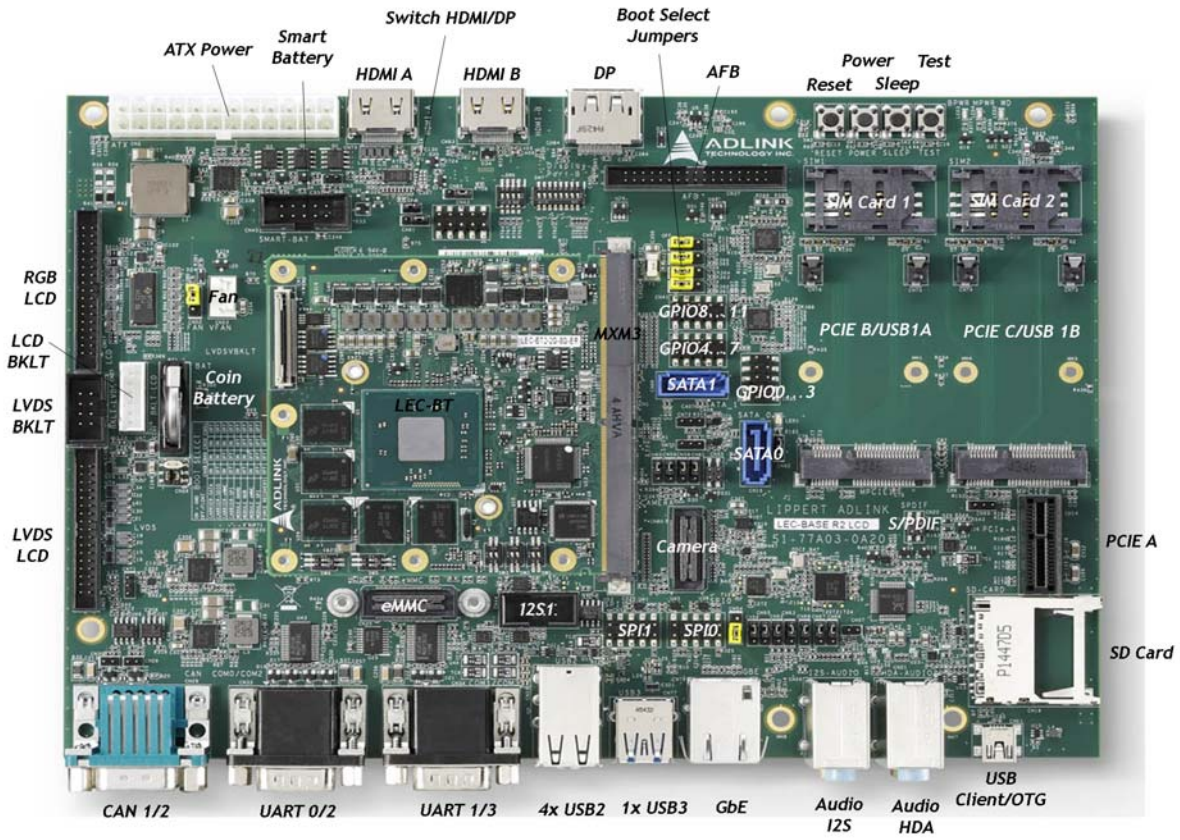


Figure 1-1: LEC-BASE MINI IO Overview

The ADLINK LEC-BASE MINI supports the features of SMARC Hardware Specification version 1.1 The following section presents the list of features for the LEC-BASE MINI.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

1.2 Features

- SMARC interface MXM3 connector
- PCI Express Bus
  - 3x PCIe x1 links
  - 1x PCIE x1 slot
  - 2x PCIE Mini slots
- Serial Port UART interfaces (4x UART)
  - Null Modem RS-232 on serial ports COM0 - COM3
  - 2-wire and 4-wire connectors
  - COM0 - COM3 interfaces on four 9-pin, DB9 connectors
- USB interfaces
  - One USB, 4-connector stack for ports 5 through 8 (USB 2.0)
  - One USB single connector for ports 0 and 1 (USB 3.0/2.0)
  - One mini-USB for USB 2.0 OTG or client
- Gigabit Ethernet interface
  - One standard RJ-45 connector
  - Activity/Link and Speed LED on Ethernet connector
- SDIO interface
  - One SDIO slot, 4-bit (for SD card)
- SDMMC interface
  - One SDMMC board-to-board connector, 8-bit (for eMMC)
- Audio interfaces
  - Supports HD Audio and AC'97
  - One 3-in-1 stack audio jack for I2S audio with Line In / Line Out / MIC In
  - One 3-in-1 stack audio jack for HD audio with Line In / Line Out / MIC In
  - One 4-pin, SPDIF Input / Output header
  - One I2S audio header
- Video interfaces
  - One HDMI connector for HDMI A interface
  - One Display Port connector
  - One HDMI or Display Port connector for HDMI B or Display Port interface
  - One single-channel LVDS header (dual channel optional)
  - One LCD RGB header (HDMI/DP/LVDS CH B optional)
  - One LVDS backlight header
  - One LCD RGB backlight header
- Power interface
  - One ATX-2.2 Power In connector (+12V and +5V)
  - Interface voltages are generated on the carrier (+3.3V, +2.8V, +1.8V, and +1.5V)
  - Optional: BattMan power supply

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

- Camera interface
  - One PCAM / MIPI CSI high-density connector
  - Two serial cameras
  - One parallel camera
  - Mixed mode (serial / parallel)
- Fan interfaces
  - One fan power selection (12V or 5V) jumper header
  - One fan function header
- SATA interfaces
  - Two standard SATA3 connectors (SATA0 and SATA1)
  - SATA1 can be optionally connected to the AFB port
- I^2C interface
  - One general purpose I^2C header
  - One I^2C camera
  - One I^2C LCD display I/D
- CAN interface
  - Two CAN DB9 connectors
- SPI interfaces
  - Two SPI headers
- Miscellaneous
  - Twelve GPIOs (interrupt capable)
  - Watchdog
  - Smart Battery
  - AFB (Alternate Function Block)
  - RTC
  - PWM Buttons
  - Boot Select

1.3 Ordering Information

Table 1-1: LEC-BASE MINI Models

Model Number	Description
LEC-BASE MINI Standard (91-77A03-000E or higher)	Second generation SMARC evaluation carrier with triple display (RGB LCD, SC LVDS and HDMI). This version is the standard configuration of the carrier, which is fully compliant with SMARC specification 1.1. This standard version supports one RGB LCD display, one single channel LVDS (18/24 bit) display, and one HDMI display.
LEC-BASE MINI Custom (91-77A03-010E or higher)	Second generation SMARC evaluation carrier with triple display (DC LVDS, HDMI, and HDMI/DP). This version is a custom option, if a third digital display is needed. This custom version supports one dual channel LVDS (18/24 bit) display, one HDMI display, and one HDMI/DP display.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

1.4 Block Diagram

Figure 1-2 presents a functional representation of the carrier.

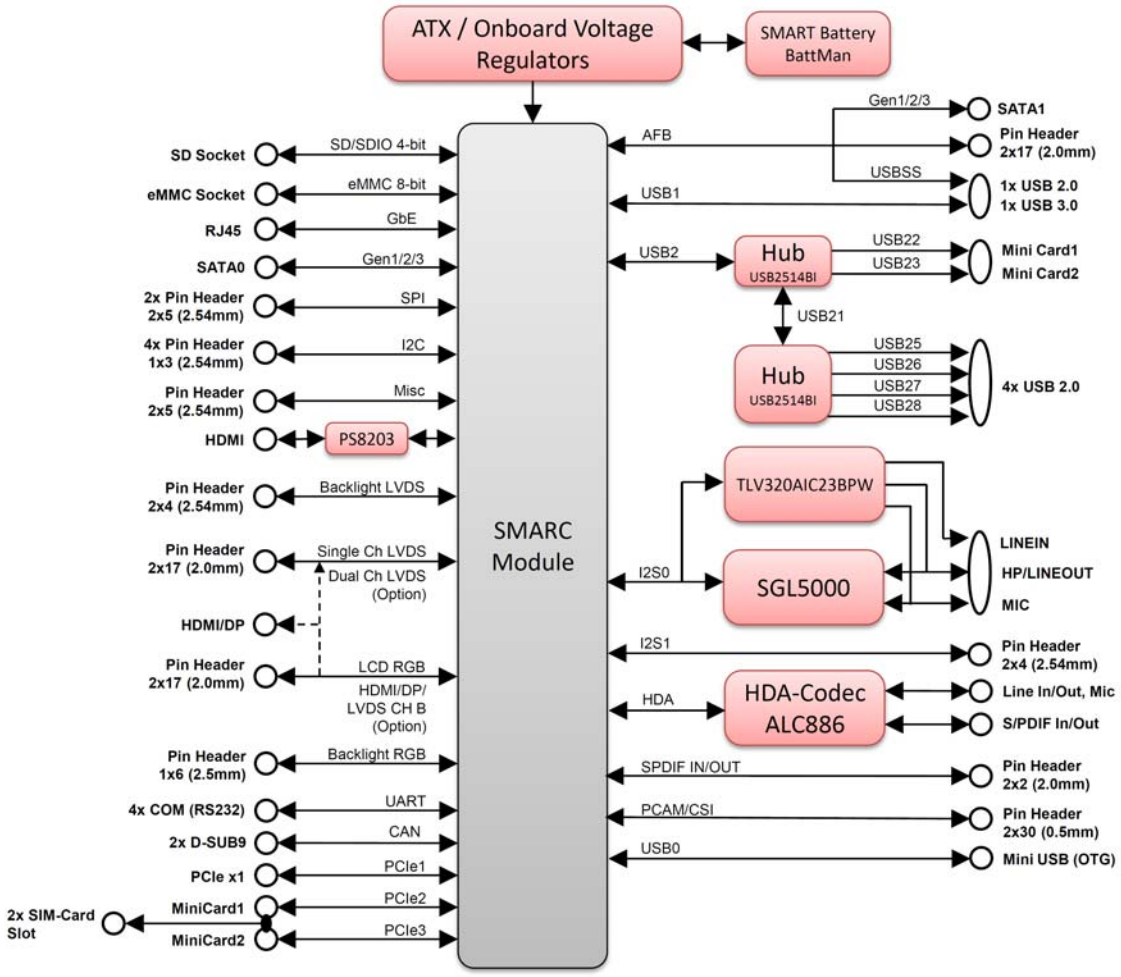


Figure 1-2: Functional Block Diagram

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

1.5 Specifications

1.5.1 Physical

Table 1-2 lists the physical dimensions of the carrier.

Table 1-2: Weight and Footprint Dimensions

Item	Dimension	
Weight	0.42 kg	Overall height is measured from the upper board surface to the top of the highest permanent component on the upper board surface. This measurement does not include the cooling solution, which can vary. The cooling solution will probably increase this dimension.
Height (overall)	33 mm	
Board thickness	2 mm	
Width	170 mm	
Length	237 mm	

1.5.2 Electrical

Table 1-3 specifies the voltage inputs of the carrier.

Table 1-3: Carrier Voltage Inputs

Parameter	Value
Standard	12V +/-5% and 5V +/-5% from ATX connector
RTC	3.0V, 2.0V to 3.3V (battery), +/-20mV ripple
BattMan Supply	12V +/-5% (3A max), 5.0V +/-5% (4A max), +/-50mV ripple

1.5.3 Environmental

Most components on the LEC-BASE MINI carrier are selected as extended temperature range parts (-40°C to +85°C). Some components are not available in this temperature range. In these cases, the component temperature ranges are narrower. The LEC-BASE MINI is validated in the -40°C to +85°C range.

The overall system performance depends on the combination of module and carrier subsystems. Some SMARC modules are available in the industrial temperature range. Others are commercial temperature range parts. Similar considerations apply to any of the add-on cards or peripherals that are used with the LEC-BASE MINI.

Table 1-4 defines the environmental conditions under which the carrier is qualified to operate and to be stored.

Table 1-4: Validated Temperature and Humidity Ranges

Parameter	Value
Temperature ▶ Operating ▶ Storage	 ▶ -40°C to +85°C ▶ -55°C to +85°C
Humidity ▶ Operating ▶ Non-operating	 ▶ 5% to 90% relative humidity, non-condensing ▶ 5% to 95% relative humidity, non-condensing

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

1.5.4 Mechanical

Figure 1-3 provides the mechanical dimensions and mounting hole sizes of the LEC-BASE MINI. The LEC-BASE MINI can be mounted to a chassis using M4, B-head screws. Mezzanine cards can be mounted to the carrier using female-female standoffs with M2.5 threads and M2.5, B-head screws.

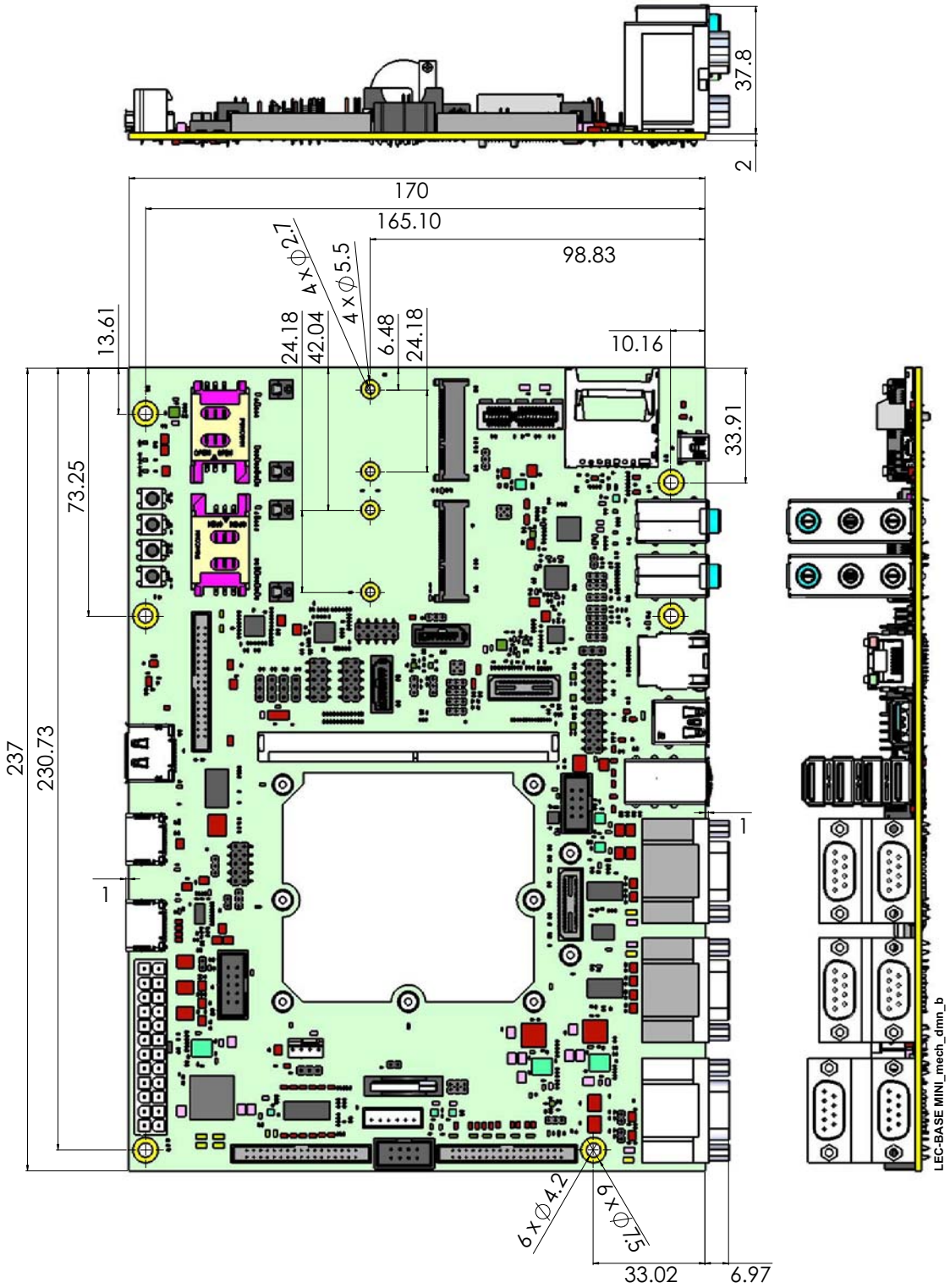


Figure 1-3: Mechanical Dimensions (Top Side)

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

2 Hardware

This chapter describes the physical specifications of the interface connectors, headers, LEDs, and switches on the LEC-BASE MINI. The third section of this chapter further describes the industry standard IO hardware on the carrier.

2.1 Interface Headers, Jumper Headers, Switches, LEDs, and Connectors

Table 2-1 describes the headers, switches, LEDs, and connectors for the LEC-BASE MINI baseboard shown in Figure 2-1, Figure 2-2, and Figure 2-3.

Table 2-1: Header, Switch, LED, and Connector Descriptions

Header / Connector#	Signal / Device	Description
BT1	Battery Socket	3-pin socket for CR2032 batteries that run at 3V [LOTES, AAA-BAT-038-K01. BK]
CN1	SMARC Interface	314-pin, MXM socket for receiving camera, graphics, and I/O signals from the SMARC module [FOXCONN, AS0B821-S55B-7H, BLACK]
CN2	ATX Power	24-pin standard ATX power input connector [ALEX, 9359-24, NATURAL]
CN3	ATX Standby	2-pin, 2.0mm jumper header for BattMan standby (Jumper needs to be installed on CN3 for BattMan operation) [JIH21N12050-02S10B-01G-4]
CN4	ATX Power Supply	2-pin, 2.0mm jumper header for shorting PSON# signal from ATX power supply to GND, enabling the power supply switched rails [JIH JVE, 27S1001-OPS35-01G-B, BLACK]
CN7	PCIe Mini1	52-pin, standard, right-angle slot for PCI Express Mini Card [Attend, 119A-LATCH-80]
CN8	SIM1	6-pin, standard slot, hinge connector for Subscriber Identity Module [REGO, 80440GFH-061-128L, BLACK]
CN9	PCIe Mini2	52-pin, standard, right-angle slot for PCI Express Mini Card [Attend, 119A-LATCH-80]
CN10	SIM2	6-pin, standard slot, hinge connector for Subscriber Identity Module [REGO, 80440GFH-061-128L, BLACK]
CN11	USB OTG	5-pin standard, Type B Mini-USB connector for USB 2.0 OTG [OCEAN, UNC1051-L1-50]
CN13	USB	16-pin standard, 4-stack right-angle, USB 2.0 connector [Kuon Yi, KS-004-ATB-10-L, BLACK]
CN14	PCIe A	36-pin, standard connector for PCI Express x1, Port A [FOXCONN, 2EG01817-D2D-DF, BLACK]
CN15	SATA0	7-pin, standard Serial ATA 0 connector [WIN WIN, WATM-07ABN4B3B8UW4, Blue]
CN16	LCD RGB Backlight	6-pin, 2.5mm header for LCD backlight control [NELTRON, 2317SJ-06, WHITE]
CN17	LCD RGB	34-pin, 2mm header for LCD display video [JIHVEI, 23N6850-34S10B-01G-G, BLACK]
CN18	SDIO	12-pin standard, 2.8mm slot connector for Secure Digital memory cards [TYCO, 1939115-1, BLACK]
CN20	SDMMC	60-pin, 0.5mm board-to-board connector for 8-bit eMMC interface [SAMTEC, QSH-030-01-L-D-A, BLACK]
CN21	HD Audio	13-pin standard audio jack for three HD audio signals: Line In (Blue), Line Out (Green), and MIC In (Pink) [FOXCONN, JA3331-HA1P-4F]

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Table 2-1: Header, Switch, LED, and Connector Descriptions (Continued)

CN22	SPDIF I/O (CODEC)	4-pin, 2mm header for SPDIF digital audio interface from the carrier CODEC [SAMTEC, TMM-102-01-T-D-SM]
CN25	LVDS	34-pin, 2mm header for LVDS output [JIHVEI, 23N6850-34S10B-01G-G, BLACK]
CN26	LVDS Voltage Select	6-pin, 2mm jumper header for selecting display and backlight LVDS voltages [JIHVEI, 27S1001-OPS35-01G-B, BLACK]
CN27	LVDS Backlight	8-pin, 2.54mm shrouded header for LVDS backlight control [JIHVEI, 23N6960-08S10B-01G-G, BLACK]
CN28	CAN	9-pin, standard dual DB9 connectors for transmitting and receiving Controller Area Network signals [FOXCONN, DM10151-H531-4F, TEAL]
CN29	CAN0 Termination	2-pin, 2mm jumper header to terminate CAN0 interface [JIH, 21N12050-02S10B-01G-4/2.8-G]
CN30	CAN1 Termination	2-pin, 2mm jumper header to terminate CAN1 interface [JIH, 21N12050-02S10B-01G-4/2.8-G]
CN31	SPI 0	10-pin, 2.54mm header for SPI0 (Serial Peripheral Interface) signals [JVE, 21N22564-10M00B-01G-6, BLACK]
CN32	SPI 1	10-pin, 2.54mm header for SPI1 (Serial Peripheral Interface) signals [JVE, 21N22564-10M00B-01G-6, BLACK]
CN33	COM0 [top] / COM2 [bottom]	9-pin standard, dual DB9 connectors for RS232 serial ports with 4-wire, RX/TX and RTS/CTS support [AMPHENOL, G17H1110131EU]
CN34	COM1 [top] / COM3 [bottom]	9-pin standard, dual DB9 connectors for RS232 serial ports with 2-wire, RX/TX support [AMPHENOL, G17H1110131EU]
CN35	GPIO 0-3	10-pin, 2.54mm header for GPIO 0-3 signals [JVE, 21N22564-10M00B-01G-6, BLACK]
CN37	AFB	34-pin, 2.54mm AFB (Alternate Function Block) for optionally connecting USB 3.0, SATA1, or general purpose AFB signals [JIHVEI, 23N6850-34S10B-01G-G, BLACK]
CN39	GPIO 4-7	10-pin, 2.54mm header for GPIO 4-7 signals [JVE, 21N22564-10M00B-01G-6, BLACK]
CN41	GPIO 8-11	10-pin, 2.54mm header for GPIO 8-11 signals [JVE, 21N22564-10M00B-01G-6, BLACK]
CN43	Miscellaneous	10-pin, 2.54mm header for miscellaneous power signals [JVE, 21N22564-10M00B-01G-6, BLACK]
CN44	I2S1	8-pin, 2.54mm shrouded header for I2S1 signals [JIHVEI, 23N6960-08S10B-01G-G, BLACK]
CN45	Smart Battery	10-pin, 2.54 box header for BattMan signals [JIHVEI, 23N6960-10S10B-01G-G, BLACK]
CN46	Battery Enable	2-pin, 2.0mm jumper header to enable RTC coin cell battery [JIH JVE, 27S1001-OPS35-01G-B, BLACK]
CN48	Boot Select 0	3-pin, 2.54mm jumper header for boot select signals [NELTRON,2317SJ-06, WHITE
CN49	Boot Select 1	3-pin, 2.54mm jumper header for boot select signals [NELTRON,2317SJ-06, WHITE
CN50	Boot Select 2	3-pin, 2.54mm jumper header for boot select signals [NELTRON,2317SJ-06, WHITE
CN51	Boot Select Force Recovery	3-pin, 2.54mm jumper header for boot select, force recovery signals [NELTRON,2317SJ-06, WHITE]

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Table 2-1: Header, Switch, LED, and Connector Descriptions (Continued)

CN52	Fan, Voltage Select	3-pin, 2.54mm jumper header to select FAN supply voltage [NELTRON,2317SJ-06, WHITE]
CN53	Fan	4-pin, 2.54mm header for CPU fan signals [JVE, 24W1163-04S10-01T-02]
CN54	SPI Power, Voltage Select	3-pin, 2.54mm jumper header for selecting voltages for SPI power [NELTRON,2317SJ-06, WHITE]
CN55	SPDIF I/O (SMARC)	4-pin, 2mm header for SPDIF digital audio interface from the SMARC connector [SAMTEC, TMM-102-01-T-D-SM]
CN56	I2S Stack	13-pin standard audio jack for three I2S audio signals: Line In (Blue), Line Out (Green), and MIC In (Pink) [FOXCONN, JA3331-HA1P-4F]
CN57	MIC_BIAS to MIC Enable	2-pin, 2.0mm jumper header for connecting MIC_BIAS to MIC [JIH JVE, 27S1001-OPS35-01G-B, BLACK]
CN58	I2S0 SD IN Codec Select C1/C2	3-pin, 2.0mm jumper header for selecting audio codecs on the carrier for I2S0 SD IN [JIH21N12050-03S10B-01G-4/2.8-G]
CN59	I2S0 SD OUT Codec Select C1/C2	3-pin, 2.0mm jumper header for selecting audio codecs on the carrier for I2S0 SD OUT [JIH21N12050-03S10B-01G-4/2.8-G]
CN60	I2S LRCK Codec Select C1/C2	3-pin, 2.0mm jumper header for selecting audio codecs on the carrier for I2S LRCK [JIH21N12050-03S10B-01G-4/2.8-G]
CN61	I2S0 CK Codec Select C1/C2	3-pin, 2.0mm jumper header for selecting audio codecs on the carrier for I2S0 CK [JIH21N12050-03S10B-01G-4/2.8-G]
CN62	I2S LIN_L Codec Select C1/C2	3-pin, 2.0mm jumper header for selecting audio codecs on the carrier for I2S LIN_L [JIH21N12050-03S10B-01G-4/2.8-G]
CN63	I2S LIN_R Codec Select C1/C2	3-pin, 2.0mm jumper header for selecting audio codecs on the carrier for I2S LIN_R [JIH21N12050-03S10B-01G-4/2.8-G]
CN64	I2S LOUT_L Codec Select C1/C2	3-pin, 2.0mm jumper header for selecting audio codecs on the carrier for I2S LOUT_L [JIH21N12050-03S10B-01G-4/2.8-G]
CN65	I2S LOUT_R Codec Select C1/C2	3-pin, 2.0mm jumper header for selecting audio codecs on the carrier for I2S LOUT_R [JIH21N12050-03S10B-01G-4/2.8-G]
CN66	I2S MIC BIAS Codec Select C1/C2	3-pin, 2.0mm jumper header for selecting audio codecs on the carrier for I2S MIC BIAS [JIH21N12050-03S10B-01G-4/2.8-G]
CN67	I2S MIC Codec Select C1/C2	3-pin, 2.0mm jumper header for selecting audio codecs on the carrier for I2S MIC [JIH21N12050-03S10B-01G-4/2.8-G]
CN68	I2S Analog GND Codec Select C1/C2	3-pin, 2.0mm jumper header for selecting audio codecs on the carrier for I2S analog ground [JIH21N12050-03S10B-01G-4/2.8-G]
CN69	I2C CAM	3-pin, 2.0mm header for I2C camera signals [JIH21N12050-03S10B-01G-4/2.8-G]
CN70	I2C GP	3-pin, 2.0mm header for I2C general purpose signals [JIH21N12050-03S10B-01G-4/2.8-G]
CN71	I2C LCD	3-pin, 2.0mm header for I2C LCD signals [JIH21N12050-03S10B-01G-4/2.8-G]
CN72	I2C PM	3-pin, 2.0mm header for I2C power management signals [JIH21N12050-03S10B-01G-4/2.8-G]

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

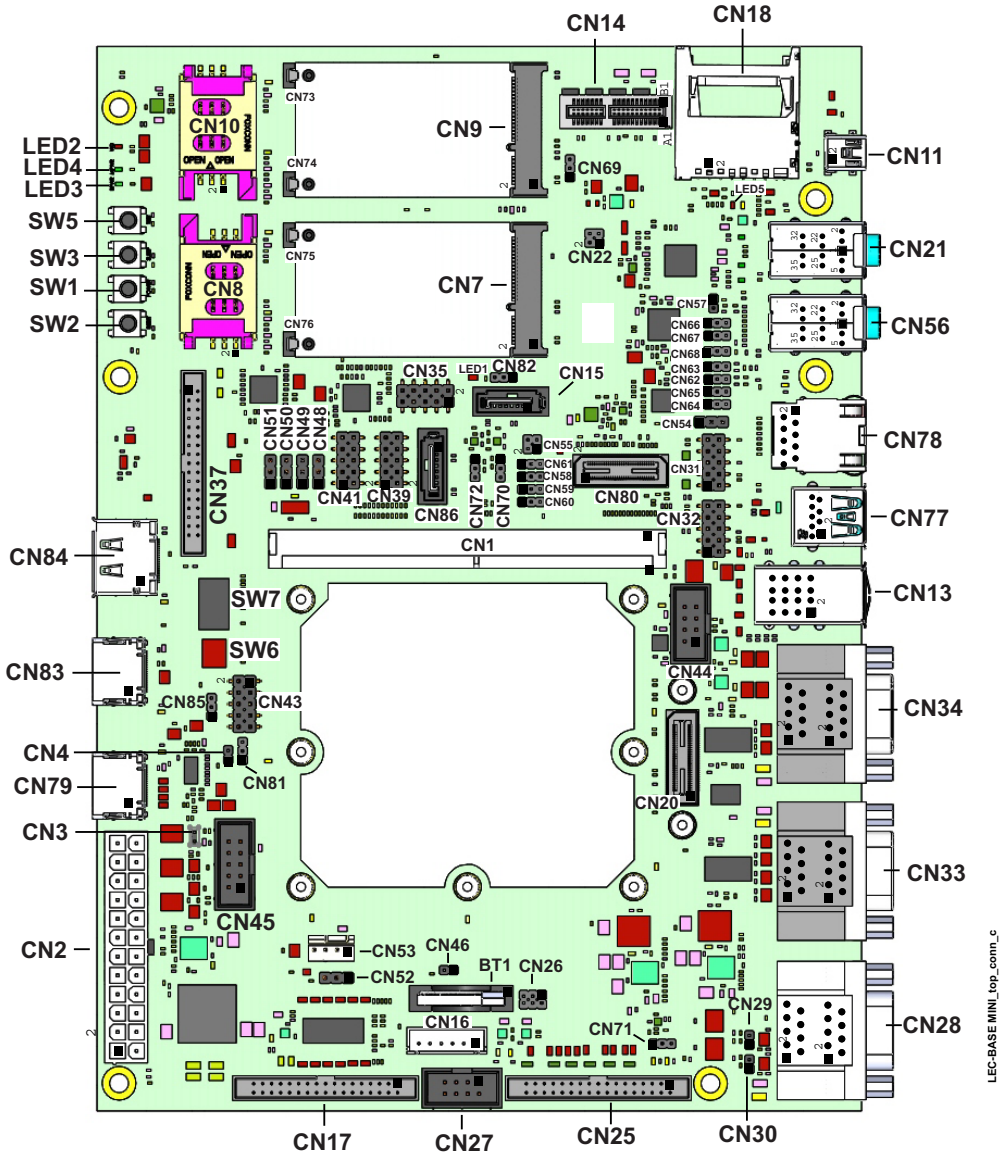
Table 2-1: Header, Switch, LED, and Connector Descriptions (Continued)

CN73	PCie2 Mini, Latch	Latch for fastening PCI Express Mini card [Attend, 119A-LATCH-80]
CN74	PCie2 Mini, Latch	Latch for fastening PCI Express Mini card [Attend, 119A-LATCH-80]
CN75	PCie2 Mini, Latch	Latch for fastening PCI Express Mini card [Attend, 119A-LATCH-80]
CN76	PCie2 Mini, Latch	Latch for fastening PCI Express Mini card [Attend, 119A-LATCH-80]
CN77	USB 2.0 / 3.0, Ports 1 / 0	9-pin standard, right-angle Type A, USB connector for USB 2.0 (port1) and USB 3.0 (port0) signals [FOXCONN, UEA11123-4HK3-4H]
CN78	GbE, Standard RJ45	16-pin standard, RJ45 connector with transformer and LED for Gigabit Ethernet [UDE, RT7-174AAM1A, BLACK]
CN79	HDMI A, Standard	19-pin standard, right-angle Type A, connector for HDMI A signals [TechBest, HDMI-KRPS00-A30N2A-L-R]
CN80	Camera, PCAM / CSI	60-pin, 0.5mm board-to-board connector for parallel and CSI camera signals [SAMTEC, QSH-030-01-L-D-A, BLACK]
CN81	PWR Bad Enable	3-pin, 2.0mm jumper header for selecting the source of VIN_PWR_BAD# [JIH21N12050-03S10B-01G-4/2.8-G]
CN82	Voltage Select for BattMan SMBus	3-pin, 2.0mm jumper header for selecting I2C_PM, BattMan SMBus voltages [JIH21N12050-03S10B-01G-4/2.8-G]
CN83	HDMI B, Standard	19-pin standard, right-angle Type A, connector for HDMI B signals [TechBest, HDMI-KRPS00-A30N2A-L-R]
CN84	Display Port, Standard	20-pin standard, right-angle connector for Display Port signals [FOXCONN, 3VD51203-D7JJ-7H, BLACK]
CN85	Display Mode Select, DP / HDMI	3-pin, 2.0mm jumper header for selecting between HDMI B and DP display mode [JIH21N12050-03S10B-01G-4/2.8-G]
CN86	SATA1, Standard	7-pin, standard Serial ATA 1 connector [WIN WIN, WATM-07ABN4B3B8UW4, Blue]
LED1	SATA Activity	Yellow LED indicating SATA activity
LED2	Watchdog Activity	Red LED indicating Watchdog activity
LED3	Carrier Power	Green LED indicating carrier power
LED4	Module Power	Green LED indicating module power
LED5	SD Power	Green LED indicating SD power
SW1	Power On	Push-button switch to Power On or shut down the module [CONTACT, TS-A02-2, BLACK]
SW2	Reset	Push-button switch to warm reset the module [CONTACT, TS-A02-2, BLACK]
SW3	Sleep	Push-button switch to induce module sleep mode [CONTACT, TS-A02-2, BLACK]
SW5	Start Debian Installer	Push-button switch for Automatically starting Linux installer on ARM CPU [CONTACT, TS-A02-2, BLACK]
SW6	DP Control	4-pole, 1.27mm dip switch for Display Port control [DIPTRONICS, DHNF-04-T-Q-T/R] Note: Refer to the PI3EQXDP1201, Display Port Redriver data sheet for more details.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Table 2-1: Header, Switch, LED, and Connector Descriptions (Continued)

SW7	DP Control	8-pole, 1.27mm dip switch for Display Port control [WINWIN, DHN-08-T-V, BLACK] Note: Refer to the PI3EQXDP1201, Display Port Redriver data sheet for more details.



KEY:

BT1 - Battery Holder
CN1 - SMARC Interface
CN2 - ATX Power
CN3 - ATX Standby Jumper
CN4 - ATX_PS_ON Enable Jumper
CN7 - PCIe Mini1
CN8 - SIM1 (PCIe Mini)
CN9 - PCIe Mini2
CN10 - SIM2 (PCIe Mini)
CN11 - USB OTG
CN13 - USB 2.0 Stack, Ports 5-8
CN14 - PCIeA x1
CN15 - SATA0
CN16 - LCD RGB Backlight
CN17 - LCD RGB
CN18 - SDIO
CN20 - SDMMC
CN21 - HD Audio Stack
CN22 - SPDIF I/O (CODEC)
CN25 - LVDS
CN26 - LVDS Voltage Select
CN27 - LVDS Backlight

CN28 - CAN
CN29 - CAN0 Termination
CN30 - CAN1 Termination
CN31 - SPI 0
CN32 - SPI 1
CN33 - UART COM0 / COM2
CN34 - UART COM1 / COM3
CN35 - GPIO 0-3
CN37 - AFB
CN39 - GPIO 4-7
CN41 - GPIO 8-11
CN43 - Miscellaneous
CN44 - I2S1
CN45 - Smart Battery
CN46 - Battery
CN48 - Boot Select 0
CN49 - Boot Select 1
CN50 - Boot Select 2
CN51 - Boot Select Force Recovery
CN52 - Fan, Voltage Select
CN53 - Fan

CN54 - SPI Power, Voltage Select
CN55 - SPDIF I/O (SMARC)
CN56 - I2S0 Stack
CN57 - MIC_BIAS to MIC Enable
CN58 - I2S0 SD IN Codec Select C1/C2
CN59 - I2S0 SD OUT Codec Select C1/C2
CN60 - I2S0 LRCK Codec Select C1/C2
CN61 - I2S0 CK Codec Select C1/C2
CN62 - I2S LIN_L Codec Select C1/C2
CN63 - I2S LIN_R Codec Select C1/C2
CN64 - I2S LOUT_L Codec Select C1/C2
CN65 - I2S LOUT_R Codec Select C1/C2
CN66 - I2S MIC BIAS Codec Select C1/C2
CN67 - I2S MIC Codec Select C1/C2
CN68 - I2S Analog GND Codec Select C1/C2
CN69 - I2C CAM
CN70 - I2C GP
CN71 - I2C LCD
CN72 - I2C PM
CN73 - PCIe2 Mini, Latch
CN74 - PCIe2 Mini, Latch
CN75 - PCIe1 Mini, Latch
CN76 - PCIe1 Mini, Latch

CN77 - USB 2.0 / 3.0, Ports 1 / 0
CN78 - GbE, Standard RJ45
CN79 - HDMI A, Standard
CN80 - Camera, PCAM / CSI
CN81 - PWR Bad Enable
CN82 - Voltage Select for BattMan SMBus
CN83 - HDMI B, Standard
CN84 - Display Port, Standard
CN85 - Display Mode Select, DP / HDMI
CN86 - SATA1, Standard

LED1 - SATA Activity, Yellow
LED2 - Watchdog Activity, Red
LED3 - Carrier Power, Green
LED4 - Module Power, Green
LED5 - SD Power, Green

SW1 - Button, Power On SMARC Module
SW2 - Button, Reset SMARC Module
SW3 - Button, Sleep Mode SMARC Module
SW5 - Button, Start Debian Installer ARM CPU
SW6 - Display Port Redriver Control
SW7 - Display Port Redriver Control

Figure 2-1: Header, Connector, Switch, and LED Locations (Top Side)

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Figure 2-2 illustrates the faces of the standard interface connectors mounted along one edge of the carrier. These connectors are for CAN, Serial Port, USB, Ethernet, and Audio industry-standard cable connectors.

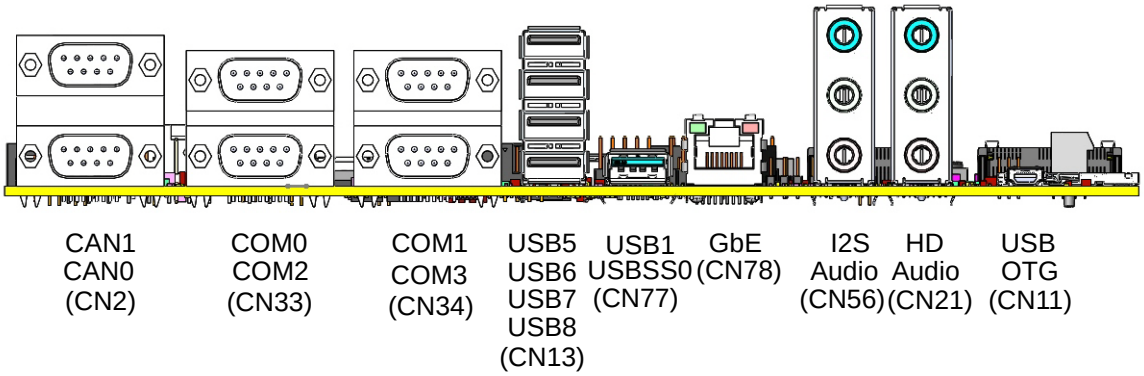


Figure 2-2: IO Panel Connector Locations

Figure 2-3 illustrates the faces of the standard interface connectors mounted along the opposite edge of the carrier shown in Figure 2-2. These connectors are for Display Port and HDMI industry-standard cable connectors.

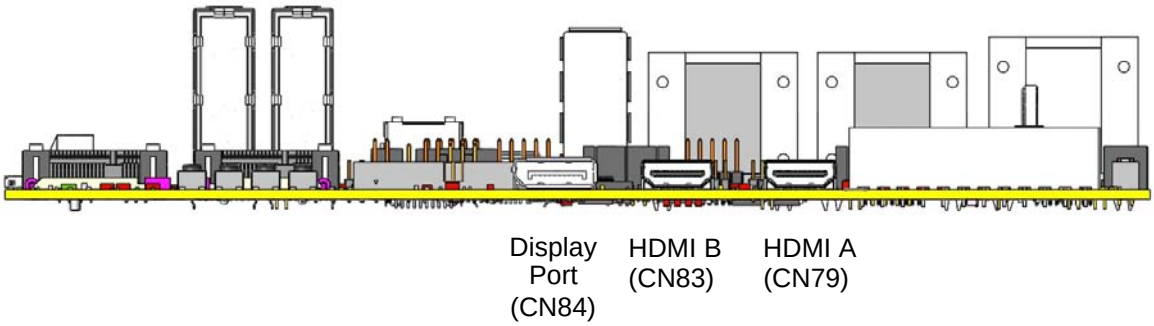


Figure 2-3: IO Panel Connector Locations (opposite side)

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

2.2 Standard Hardware References

This section further describes the supported features of the LEC-BASE MINI standard, on-board hardware.

2.2.1 Audio IO Jacks

The LEC-BASE MINI provides two standard audio jacks for HD (CN21) and I2S (CN56) audio. Two audio codecs support these two interfaces. Figure 2-4 depicts the three lines of the audio jacks: Line In (1 - Blue), Line Out (2 - Green), and MIC In (3 - Pink). Figure 2-5 presents the functional block diagram of I2S signals and hardware on the carrier.

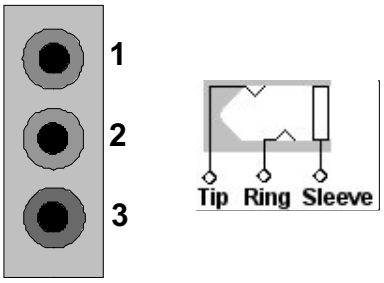


Figure 2-4: Stereo Jack Configuration

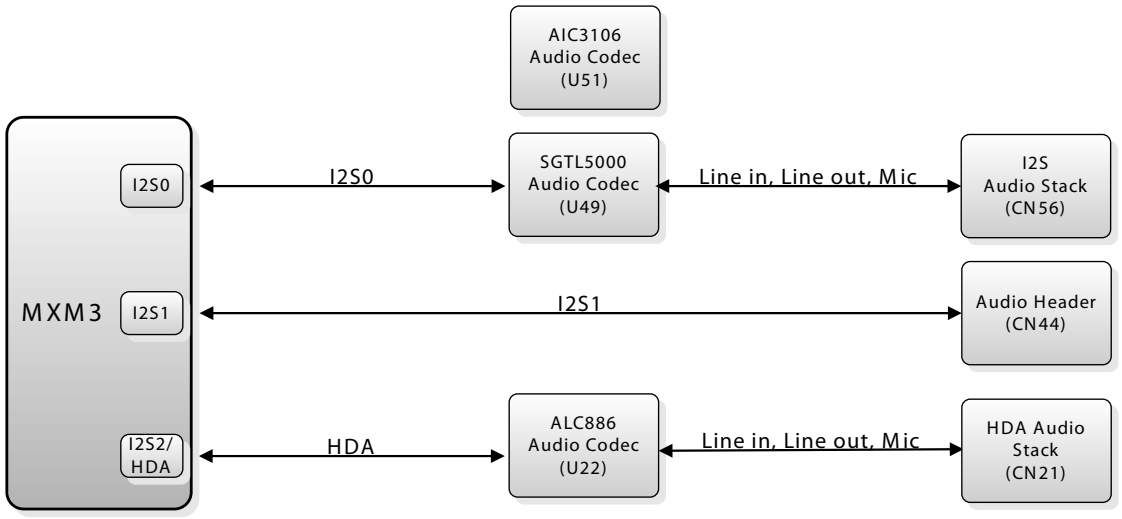


Figure 2-5: I2S/HDA Block Diagram

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

2.2.2 PCIe Mini Card Slot

The LEC-BASE MINI provides two standard PCI Express Mini Card slots. Figure 2-6 presents one mini card slot with one of the two fastening latches. Figure 2-7 illustrates the functional block diagram of the PCIe Mini Card signals and hardware on the carrier.

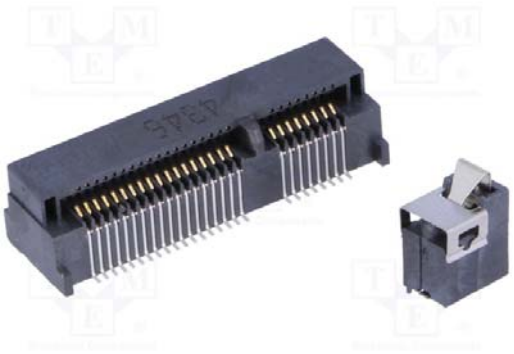


Figure 2-6: PCIe Mini Card Slot with Latch

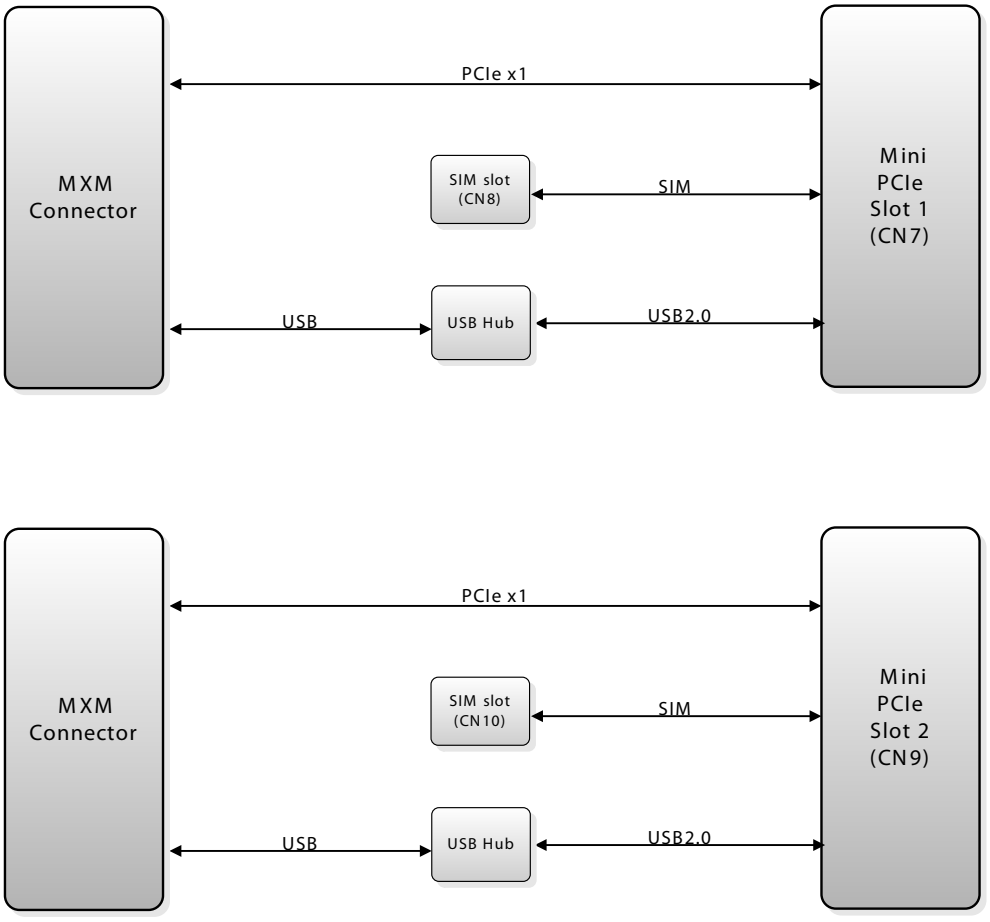


Figure 2-7: PCIe Mini Card Slot Block Diagram

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

2.2.3 SDIO Slot

The SDIO slot (CN18) provides the standard 4-bit, push-push interface for SD memory cards. LED5 provides indication of SD power.

NOTE: SD cards that operate with only 1.8V, are not supported.

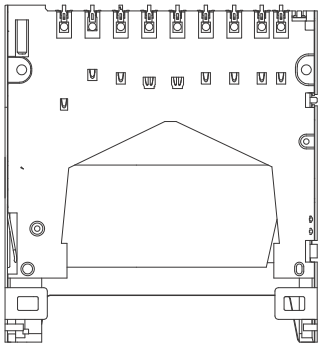


Figure 2-8: SDIO Slot

Table 2-2: SDIO Slot (CN18)

Pin #	Signal	Description
1	SDIO_D3	SDIO data bit3
2	SDIO_CMD	SDIO Command
3	GND	Ground
4	+VCC_SDIO	3.3V power supply
5	SDIO_CK	SDIO clock
6	GND	Ground
7	SDIO_D0	SDIO data bit0
8	SDIO_D1	SDIO data bit1
9	SDIO_D2	SDIO data bit2
10	SDIO_CD#	SDIO card detect
11	GND	Ground
12	SDIO_WP	SDIO write protect

Note: Shaded table cells denote power or ground.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

2.2.4 SIM Slot

Two SIM slots (CN8 / CN10) provide interface for two Subscriber Identity Modules, supporting both PCIe Mini Card slots: CN8 supports CN7 MINI Card slot and CN10 supports CN9 MINI Card slot. Figure 2-9 illustrates the slots' hinge-type connections. Table 2-3 and Table 2-4 provide the signals for both slots.

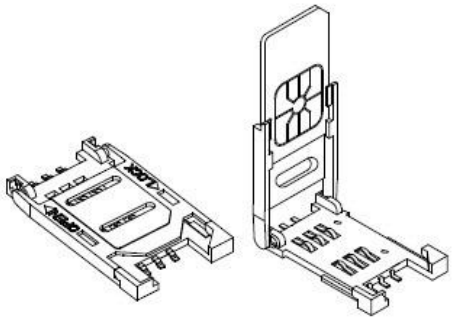


Figure 2-9: SIM Slot (CN8 / CN10)

Table 2-3: SIM Slot (CN8)

Pin #	Signal	Description
1	UM1_PWR	+5 VDC power supply input
2	UM1_RESET	Resets the card's communications
3	UM1_CLK	Clock signal for data communications timing
4	GND	Ground
5	UM1_VPP	Programming input voltage
6	UM1_DATA	I/O for serial data

Note: Shaded table cells denote power or ground.

Table 2-4: SIM Slot (CN10)

Pin #	Signal	Description
1	UM2_PWR	+5 VDC power supply input
2	UM2_RESET	Resets the card's communications
3	UM2_CLK	Clock signal for data communications timing
4	GND	Ground
5	UM2_VPP	Programming input voltage
6	UM2_DATA	I/O for serial data

Note: Shaded table cells denote power or ground.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

2.2.5 Battery Socket

One vertical, AAA battery socket provides power for an external RTC coin cell battery. Figure 2-10 illustrates the top and side views of the socket. Table 2-5 provides the signals for socket.

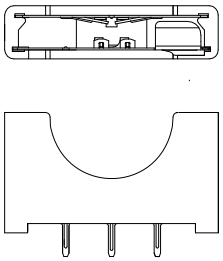


Figure 2-10: Battery Socket

Table 2-5: Battery Socket (BT1)

Pin #	Signal	Description
1	3V_BAT	+3 volts power for RTC
2	GND	Ground
3	3V_BAT	+3 volts power for RTC

Note: Shaded table cells denote power or ground. Jumper required on CN46 to enable the RTC.



A CR2032 battery may explode if incorrectly installed. Replace only with the same or equivalent type recommended by the socket manufacturer.

.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3 Interfaces

This section provides the pin signals for all the non-standard user interfaces on the LEC-BASE MINI. Unless pinouts for industry standard interfaces have been modified, those pin-out tables will not appear in this manual. Signal definitions for standard interfaces such as SATA, USB, and PCIe can be found in their respective specification datasheets.

NOTE:

The tables in this section define pin sequence using the method in the following example: A 10-pin header with two rows of pins, using odd/even numbering, where pin 2 is directly across from pin 1, is noted as **10 pins, 2 rows, odd/even pin sequence (1, 2)**. Consecutive numbering is noted, for example, as **24 pins, 2 rows, consecutive pin sequence (1, 13)**, where pin 13 is directly across from pin 1. Refer to Figure 2-1 for pin-1 locations.

3.1 Standard USB Interfaces

All USB interfaces on LEC-BASE MINI are supported through standard connectors, and their signal definitions can be found in their respective specification datasheets. Refer to the following block diagram for an illustration of the USB interface mapping on the carrier.

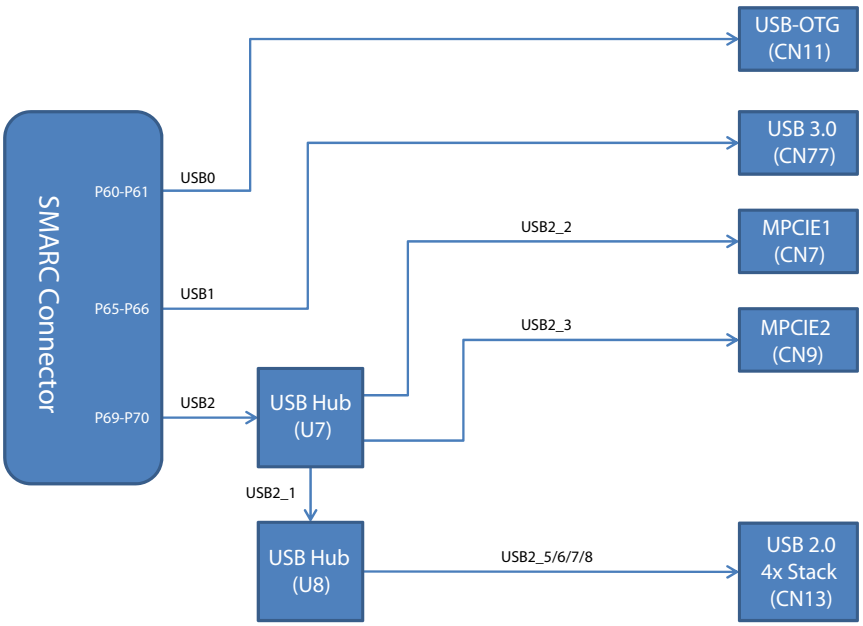


Figure 3-1: USB Mapping Block Diagram

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.2 ATX Power (CN2)

Table 3-1 lists the signals of the standard ATX Power connector, which provides 24 pins, 2 rows consecutive pin sequence (1, 13) with 4.20mm pitch. Use the SW1 button switch on the carrier to apply power to the module.

Table 3-1: ATX Power Signals (CN2)

Pin#	Signal	Description	Pin#	Signal	Description
1	+V3P3_ATX	Power Supply DC voltage	13	+V3P3_ATX	Power Supply DC voltage
2	+V3P3_ATX	Power Supply DC voltage	14	NC	Not Connected
3	GND	Ground	15	GND	Ground
4	+V5P0_ATX	Power Supply DC voltage	16	ATX_PS_ON#	Switch to turn on power supply, shorted to Ground
5	GND	Ground	17	GND	Ground
6	+V5P0_ATX	Power Supply DC voltage	18	GND	Ground
7	GND	Ground	19	GND	Ground
8	ATX_PWRGD_5V	Status from the power supply, notifying the computer that the DC operating voltages are within the required ranges	20	NC	Not Connected
9	+V5P0_SBY	Power Supply Standby DC voltage	21	+V5P0_ATX	Power Supply DC voltage
10	+V12P0_ATX	Power Supply DC voltage	22	+V5P0_ATX	Power Supply DC voltage
11	+V12P0_ATX	Power Supply DC voltage	23	+V5P0_ATX	Power Supply DC voltage
12	+V3P3_ATX	Power Supply DC voltage	24	GND	Ground

NOTE: Shaded table cells denote power or ground. The # symbol indicates the signal is Active Low. Shaded

3.3 BattMan Enable (CN3)

Table 3-2 lists the pin signals of the BattMan Enable jumper header, which provides 2 pins with 2.00mm pitch.

Table 3-2: ATX Standby (CN3)

Pin #	Signal	Jumper Position
1	GND	• Jumper Installed (1-2) - BattMan power supply enabled • Jumper Removed - ATX power supply enabled (**Default**)
2	+V5P0_SBY	

Note: Shaded table cell denotes ground.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.4 ATX Power Supply Enable (CN4)

Table 3-2 lists the pin signals of the ATX Power Supply jumper header, which provides 2 pins with 2.00mm pitch.

Table 3-3: ATX Power Supply (CN4)

Pin #	Signal	Jumper Position
1	GND	• Jumper Installed (1-2) - ATX switched rails / power supply enabled (**Default**) • Jumper Removed - ATX switched rails / power supply disabled
2	ATX_PS_ON#	

NOTE: Shaded table cell denotes ground. The # symbol indicates the signal is Active Low.



BattMan power supply also requires a jumper to be installed on this header (1-2).

3.5 PCIe A x1 (CN14)

Table 3-4 lists the signals for the PCIe A x1 connector, which provides 36 pins, two rows, consecutive pin sequence (1, 13) with 1.00mm pitch.

Table 3-4: PCIe A x1 (CN14)

Pin	Signal	Pin	Signal
B1	+V12P0_ATX	A1	PCIE_A_PRSNT1#
B2	+V12P0_ATX	A2	+V12P0_ATX
B3	+V12P0_ATX	A3	+V12P0_ATX
B4	GND	A4	GND
B5	I2C_CAM_CK_3V	A5	Not Connected
B6	I2C_CAM_DAT_3V	A6	Not Connected
B7	GND	A7	Not Connected
B8	+3VP3S	A8	Not Connected
B9	Not Connected	A9	+3VP3S
B10	+3VP3S	A10	+3VP3S
B11	PCIE_WAKE#	A11	PCIE_A_RST#
B12	Not Connected	A12	GND
B13	GND	A13	PCIE_A_CLK_P
B14	PCIE_A_TX_P	A14	PCIE_A_CLK_N
B15	PCIE_A_TX_N	A15	GND
B16	GND	A16	PCIE_A_RX_P
B17	PCIE_A_CKREQ#	A17	PCIE_A_RX_N
B18	GND	A18	GND

NOTE: Shaded table cells denote power or ground. The # symbol indicates the signal is Active Low.

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.6 SDMMC Interface (CN20)

Table 3-5 lists the pin signals of the SD Card ground plane socket, which provides 60-pins, 2 rows, odd/even pin sequence (1, 2) with 0.50mm pitch. These signals are connected to the SD/eMMC interface at pins S26 through S36 of the SMARC connector over a 3.3 volt level shifter.

Table 3-5: SD/eMMC Interface Signals (CN20)

Pin #	Signal	Description
1	GND	Ground
2	GND	Ground
3	MMC_D0	MMC data bit0
4	GND	Ground
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	MMC_D1	MMC data bit1
10	GND	Ground
11	GND	Ground
12	GND	Ground
13	GND	Ground
14	GND	Ground
15	MMC_D2	MMC data bit2
16	GND	Ground
17	GND	Ground
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	MMC_D3	MMC data bit3
22	VDD_3V3	3.3 Volt power supply
23	GND	Ground
24	GND	Ground
25	GND	Ground
26	GND	Ground
27	MMC_D4	MMC data bit4
28	VDD_3V3	
29	GND	Ground
30	GND	Ground
31	GND	Ground
32	GND	Ground
33	MMC_D5	MMC data bit5
34	GND	Ground
35	GND	Ground
36	GND	Ground
37	GND	Ground
38	GND	Ground
39	MMC_D6	MMC data bit6
40	GND	Ground

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Table 3-5: SD/eMMC Interface Signals (CN20) (Continued)

41	GND	Ground
42	GND	Ground
43	GND	Ground
44	GND	Ground
45	MMC_D7	MMC data bit7
46	GND	Ground
47	GND	Ground
48	GND	Ground
49	GND	Ground
50	GND	Ground
51	MMC_CK	MMC clock
52	GND	Ground
53	GND	Ground
54	GND	Ground
55	GND	Ground
56	GND	Ground
57	MMC_CMD	MMC command
58	GND	Ground
59	GND	Ground
60	GND	Ground

NOTE: The shaded table cells denote power or ground.

3.7 SPDIF I/O [CODEC] (CN22)

Table 3-6 lists the pin signals of the SPDIF I/O header, which provides 4 pins 2 rows, odd/even pin sequence (1, 2) with 2.00mm pitch.

Table 3-6: Digital Audio Signals (CN22)

Pin #	Signal	Description
1	CON_SPDIFI	Digital Audio In
2	GND	Ground
3	CON_SPDIFO	Digital Audio Out
4	GND	Ground

NOTE: Shaded table cells denote ground.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.8 Display Interfaces

This section describes the LCD RGB and LVDS display interfaces that the carrier supports through standard and non-standard headers and connectors. The DisplayPort and HDMI display interfaces are standard connectors and are described in Table 2-1 of Chapter 2. Figure 3-2 illustrates the carrier's two standard and custom display configurations available under separate model order numbers.

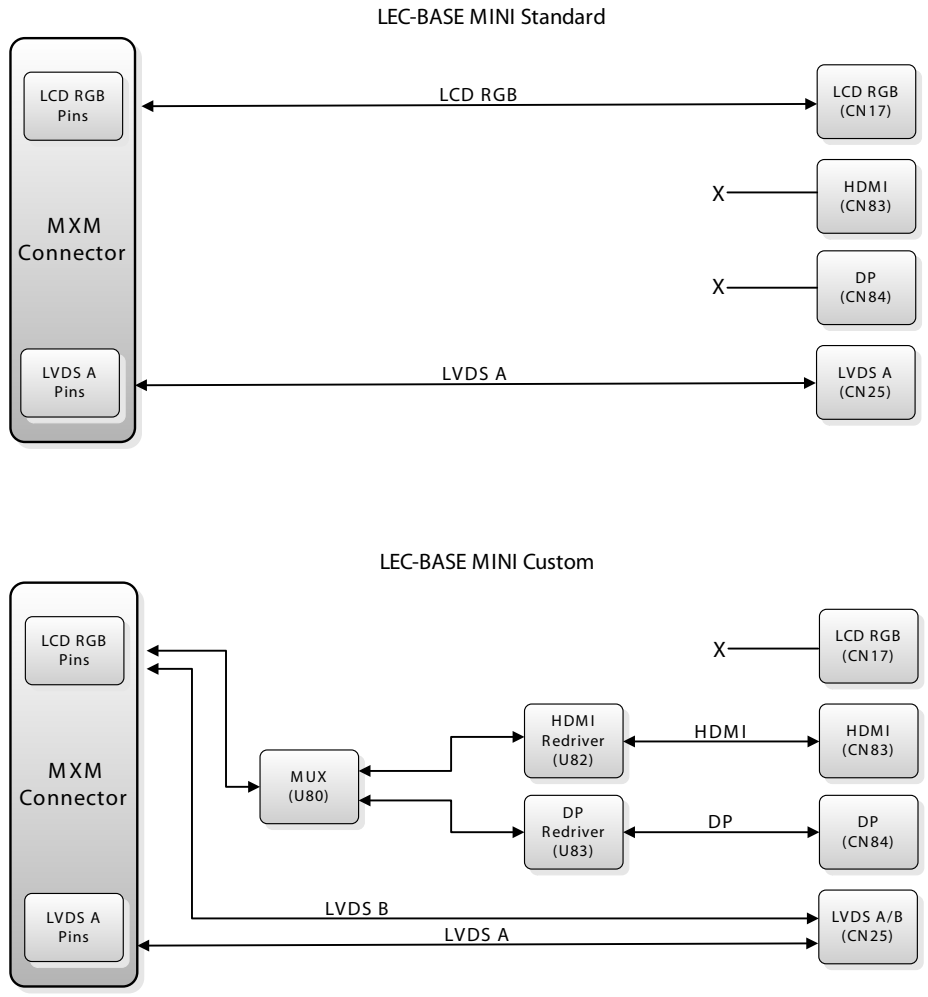


Figure 3-2: Display Configuration Block Diagram

3.8.1 LCD RGB Backlight (CN16)

Table 3-7 lists the signals of the LCD RGB Backlight header, which provides 6 pins in a single row with 2.50mm pitch.

Table 3-7: LCD RGB Backlight Signals (CN16)

Pin #	Signal
1	LCD_DE_33 (LCD data enable; connected over the 3.3 volt level shifter)
2	LCD_BKLT_PWM (LCD backlight PWM)
3	LCD_VDD_EN (LCD power enable)
4	Not Connected
5	GND (Ground)
6	+V3P3_LCD (Switched 3.3V power supply)

NOTE: Shaded table cells denote power or ground.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.8.2 LCD RGB (CN17)

Table 3-8 lists the pin signals of the LCD RGB header, which provides 34-pins, 2 rows, odd/even pin sequence (1, 2) with 2.00mm pitch. These pins are connected directly to the LCD interface at the SMARC connector.

Table 3-8: LCD RGB Video Signals (CN17)

Pin #	Signal	Description
1	LCD_CON_R_D0	Flat Panel bit0 – data output, Blue0 (24-bit)
2	LCD_CON_R_D16	Flat Panel bit16 – data output, Red0 (24-bit)
3	LCD_CON_R_D1	Flat Panel bit1 – data output, Blue1 (24-bit)
4	LCD_CON_R_D17	Flat Panel bit17 – data output, Red1 (24-bit)
5	LCD_CON_R_D2	Flat Panel bit2 – data output, Blue0 (18-bit); Blue2 (24-bit)
6	LCD_CON_R_D18	Flat Panel bit18 – data output, Red0 (18-bit), Red2 (24-bit)
7	LCD_CON_R_D3	Flat Panel bit3 – data output, Blue1 (18-bit); Blue3 (24-bit)
8	LCD_CON_R_D19	Flat Panel bit19 – data output, Red1 (18-bit), Red3 (24-bit)
9	LCD_CON_R_D4	Flat Panel bit4 – data output, Blue2 (18-bit); Blue4 (24-bit)
10	LCD_CON_R_D20	Flat Panel bit20 – data output, Red2 (18-bit), Red4 (24-bit)
11	LCD_CON_R_D5	Flat Panel bit5 – data output, Blue3 (18-bit); Blue5 (24-bit)
12	LCD_CON_R_D21	Flat Panel bit21 – data output, Red3 (18-bit), Red5 (24-bit)
13	LCD_CON_R_D6	Flat Panel bit6 – data output, Blue4 (18-bit); Blue6 (24-bit)
14	LCD_CON_R_D22	Flat Panel bit22 – data output, Red4 (18-bit), Red6 (24-bit)
15	LCD_CON_R_D7	Flat Panel bit7 – data output, Blue5 (18-bit); Blue7 (24-bit)
16	LCD_CON_R_D23	Flat Panel bit23 – data output, Red5 (18-bit), Red7 (24-bit)
17	LCD_CON_R_D8	Flat Panel bit8 – data output, Green0 (24-bit)
18	LCD_CON_R_VSYNC	Flat Panel Vertical Sync
19	LCD_CON_R_D9	Flat Panel bit9 – data output, Green1 (24-bit)
20	LCD_CON_R_HSYNC	Flat Panel Horizontal Sync
21	LCD_CON_R_D10	Flat Panel bit10 – data output, Green0 (18-bit), Green2 (24-bit)
22	LCD_CON_R_D_PCLK	Flat Panel Pixel Clock – This signal provides the clock for transferring digital pixel data
23	LCD_CON_R_D11	Flat Panel bit11 – data output, Green1 (18-bit), Green3 (24-bit)
24	VDD_5V	5 Volt Supply
25	LCD_CON_R_D12	Flat Panel bit12 – data output, Green2 (18-bit), Green4 (24-bit)
26	VDD_5V	5 Volt Supply
27	LCD_CON_R_D13	Flat Panel bit13 – data output, Green3 (18-bit), Green5 (24-bit)
28	VDD_5V	5 Volt Supply
29	LCD_CON_R_D14	Flat Panel bit14 – data output, Green4 (18-bit), Green6 (24-bit)
30	LCD_3V3	Switched 3.3 Volt Supply
31	LCD_CON_R_D15	Flat Panel bit15 – data output, Green5 (18-bit), Green7 (24-bit)
32	LCD_3V3	Switched 3.3 Volt Supply
33	GND	Ground
34	GND	Ground

NOTE: The shaded table cells denote power or ground.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.8.3 LVDS (CN25)

Table 3-9 lists the pin signals of the LVDS header which provides 34-pins, 2 rows, odd/even pin sequence (1, 2) with 2.00mm pitch. Channel A pins are connected directly to the LVDS interface at the SMARC connector. Channel B pins are connected to selected LCD pins on the SMARC connector

Table 3-9: LVDS Interface Pin Signals (CN25)

Pin #	Signal	Description	SMARC Signal
1	LVDS_DDC_DAT	System Management Data	I2C_LCD_DAT
2	LVDS_DDC_CLK	System Management Clock	I2C_LCD_DAT
3	+VCC_LVDS	Panel Power [CN26 jumper settings: (1-3) for 3.3V [default], (3-5) for 5V]	LCD_VDD_EN
4	+VCC_LVDS	Panel Power [CN26 jumper settings: (1-3) for 3.3V [default], (3-5) for 5V]	LCD_VDD_EN
5	GND	Ground	GND
6	LVDS_A0_L_N	Data Negative Output	LVDS0-
7	LVDS_A0_L_P	Data Positive Output	LVDS0+
8	NC	Not Connected	
9	LVDS_A1_L_N	Data Negative Output	LVDS1-
10	LVDS_A1_L_P	Data Positive Output	LVDS1+
11	NC	Not Connected	
12	LVDS_A2_L_P	Data Positive Output	LVDS2+
13	LVDS_A2_L_N	Data Negative Output	LVDS2-
14	NC	Not Connected	
15	LVDS_A_CK_L_N	Clock Negative	LVDS_CK-
16	LVDS_A_CK_L_P	Clock Positive	LVDS_CK+
17	+VCC_LVDS	Panel Power [CN26 jumper settings: (1-3) for 3.3V [default], (3-5) for 5V]	LCD_VDD_EN
18	LVDS_A3_L_P	Data Positive Output	LVDS3+
19	LVDS_A3_L_N	Data Negative Output	LVDS3-
20	GND	Ground	
21	LVDS_B0_L_N	Data Negative Output - Channel B	LCD_D17
22	LVDS_B0_L_P	Data Positive Output - Channel B	LCD_D16
23	GND	Ground	
24	LVDS_B1_L_N	Data Negative Output - Channel B	LCD_D20
25	LVDS_B1_L_P	Data Positive Output - Channel B	LCD_D19
26	GND	Ground	
27	LVDS_B2_L_N	Data Negative Output - Channel B	LCD_D23
28	LVDS_B2_L_P	Data Positive Output - Channel B	LCD_D22
29	GND	Ground	
30	LVDS_B_CK_L_P	Clock Positive - Channel B	LCD_DE
31	LVDS_B_CK_L_N	Clock Negative - Channel B	LCD_VS
32	Not Connected	Not Connected	
33	LVDS_B3_L_P	Clock Positive - Channel B	LCD_HS
34	LVDS_B3_L_N	Clock Negative - Channel B	LCD_PCK

NOTE: The shaded table cells denote power or ground.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.8.4 LVDS Voltage Select (CN26)

Table 3-10 lists the pin signals of the LVDS Voltage Select jumper header, which provides 6 pins in two rows with odd/even pin sequence (1,2) and 2.00mm pitch.

Table 3-10: LVDS Voltage Select Signals (CN26)

Pin #	Signal	Pin #	Signal	Description
1	+V3P3S	2	+V12P0_ATX	• Pins 1, 3, 5 for selecting LVDS voltage (See Table 3-9 on page 26, pins 3, 4, and 17) • Pins 2, 4, 6 for selecting LVDS backlight voltage (See Table 3-11, pins 2 and 8)
3	GND	4	BKLT_VCC_SEL	
5	+V5P0A	6	+V5P0A	

NOTE: Shaded table cells denote power or ground.

3.8.5 LVDS Backlight (CN27)

Table 3-11 lists the pin signals of the LVDS Backlight header, which provides 8 pins in two rows with odd/even pin sequence (1,2) and 2.54mm pitch.

Table 3-11: LVDS Backlight (CN27)

Pin #	Signal
1	GND
2	+VCC_LVDS [CN26 jumper settings: (1-3) for 3.3V [default], (3-5) for 5V]
3	LCD_BKLT_PWM
4	GND
5	LCD_BKLT_EN
6	GND
7	Not Connected
8	+VCC_BKLT [CN26 jumper settings: (2-4) for 12V [default], (4-6) for 5V]

NOTE: Shaded table cells denote power or ground.

3.9 CAN 0-1 (Controller Area Network - CN28)

Table 3-12 and Table 3-13 list the pin signals of the Controller Area Network interface (CAN0 and CAN1), which provides standard dual DB9 connectors.

Table 3-12: CAN0 Signals (CN28)

Pin #	Signal
1	Not Connected
2	CAN0_H
3	Not Connected
4	Not Connected
5	GND_CAN
6	Not Connected
7	CAN0_L
8	Not Connected
9	5 Volt

NOTE: These pins are connected over the CAN transceiver to the CAN0 SMARC connector interface (pins P143 and P144.) Shaded table cell denotes power.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Table 3-13: CAN1 Signals (CN28)

Pin #	Signal
1	Not Connected
2	CAN1_H
3	Not Connected
4	Not Connected
5	GND_CAN
6	Not Connected
7	CAN1_L
8	Not Connected
9	5 Volt

NOTE: These pins are connected over the CAN transceiver to the CAN1 SMARC connector interface (pins P145 and P146.) Shaded table cell denotes power.

3.10 CAN0 Termination (CN29)

Table 3-14 lists the pin signals of the CAN0 termination jumper header, which provides 2 pins with 2.00mm pitch.

Table 3-14: CAN0 Termination (CN29)

Pin #	Signal
1	CAN0_TERM
2	CAN0_H

Note: Default setting is empty pins.

3.11 CAN1 Termination (CN30)

Table 3-15 lists the pin signals of the CAN1 termination jumper header, which provides 2 pins with 2.00mm pitch.

Table 3-15: CAN1 Termination (CN30)

Pin #	Signal
1	CAN1_TERM
2	CAN1_H

Note: Default setting is empty pins.

3.12 SPI0 (CN31)

Table 3-16 lists the pin signals of the Serial Peripheral Interface 0 header, which provides 10 pins in two rows with odd/even pin sequence (1,2) and 2.54mm pitch. These pins are connected to the SMARC connector over a voltage level translator.

Table 3-16: SPI0 Signals (CN31)

Pin #	Signal
1	SPI0_HOLD#
2	SPI0_WP#
3	SPI0_CS0#_S
4	SPI0_CS1#_S
5	Ground

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Table 3-16: SPI0 Signals (CN31) (Continued)

6	+VCC_SPI
7	SPI0_CN_CLK
8	Not Connected
9	SPI0_CN_MOSI
10	SPI0_CN_MISO

NOTE: Shaded table cells denote power or ground. The # symbol indicates the signal is Active Low.

3.13 SPI1 (CN32)

Table 3-17 lists the pin signals of the Serial Peripheral Interface 1 header, which provides 10 pins in two rows with odd/even pin sequence (1,2) and 2.54mm pitch. These pins are connected to the SMARC connector over a voltage translator.

Table 3-17: SPI1 Signals (CN32)

Pin #	Signal
1	SPI1_HOLD#
2	SPI1_WP#
3	SPI1_CS0#_S
4	SPI1_CS1#_S
5	Ground
6	+VCC_SPI
7	SPI1_CN_CLK
8	Not Connected
9	SPI0_CN_MOSI
10	SPI0_CN_MISO

NOTE: Shaded table cell denote power or ground. The # symbol indicates the signal is Active Low.

3.14 Serial Interfaces

This section describes the signals of the two dual, standard DB9 serial port connectors for RS232 signals.

3.14.1 COM0 and COM2 (CN33)

Table 3-18 and Table 3-19 list the pin signals of the Serial A, 4-wire RS232 interface (COM0 and COM2), which provides standard dual DB9 connectors.

Table 3-18: COM0 Signals (CN33)

Pin #	Signal
1	Not Connected
2	COM0_RX
3	COM0_TX
4	Not Connected
5	GND
6	Not Connected
7	COM0_RTS#
8	COM0_CTS#
9	Not Connected

NOTE: Shaded table cell denotes ground. The # symbol indicates the signal is Active Low.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Table 3-19: COM2 Signals (CN33)

Pin #	Signal
1	Not Connected
2	COM2_RX
3	COM2_TX
4	Not Connected
5	GND
6	Not Connected
7	COM2_RTS#
8	COM2_CTS#
9	Not Connected

NOTE: Shaded table cell denotes ground. The # symbol indicates the signal is Active Low.

3.14.2 COM1 and COM3 (CN34)

Table 3-20 and Table 3-21 list the pin signals of the Serial B, 2-wire RS232 interface (COM1 and COM3), which provides standard dual DB9 connectors.

Table 3-20: COM1 Signals (CN34)

Pin #	Signal
1	Not Connected
2	COM1_RX
3	COM1_TX
4	Not Connected
5	GND
6	Not Connected
7	Not Connected
8	Not Connected
9	Not Connected

NOTE: Shaded table cell denotes ground.

Table 3-21: COM3 Signals (CN34)

Pin #	Signal
1	Not Connected
2	COM3_RX
3	COM3_TX
4	Not Connected
5	GND
6	Not Connected
7	Not Connected
8	Not Connected
9	Not Connected

NOTE: Shaded table cell denotes ground.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.15 GPIO 0-3 (CN35)

Table 3-22 lists the pin signals of the General Purpose IO 0-3 header, which provides 10 pins in 2 rows, odd/even pin sequence (1, 2), and 2.54mm pitch.

Table 3-22: General Purpose IO 0-3 (CN35)

Pin #	Signal
1	+V5P0A
2	CN_GPIO0 (connected to SMARC pin P108)
3	+V3P3S
4	CN_GPIO1 (connected to SMARC pin P109)
5	GND
6	CN_GPIO2 (connected to SMARC pin P110)
7	GND
8	CN_GPIO3 (connected to SMARC pin P111)
9	GND
10	GND

NOTE: These GPIOs are shared function pins. See SMARC Specification 1.1. Shaded table cells denote power or ground.

3.16 Alternate Function Block (CN37)

Table 3-23 lists the pin signals of the Alternate Function Block header which provides 34-pins, 2 rows, odd/even pin sequence (1, 2) with 2.54mm pitch. These pins are connected directly to the SMARC connector.

NOTE: Alternate functions on this connector include USB_Port0 and SATA-Port1 but can not be accessed through this connector without modification to the carrier. The default access to these functions is through the standard connectors on the carrier, CN77 for USB_Port0 and CN86 for SATA_Port1. See the following diagram for default and alternate configurations of the AFB interface.

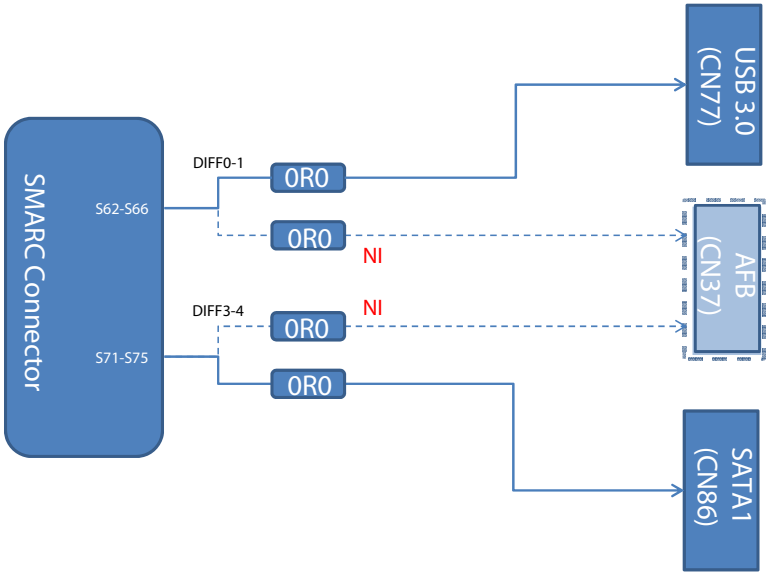


Figure 3-3: AFB Configuration Block Diagram

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Table 3-23: Alternate Function Block Interface Pin Signals (CN37)

Pin #	Signal	Alternate Function
1	+V5P0A	+V5P0A
2	+V5P0A	+V5P0A
3	AFB0_OUT (connected to SMARC pin S17)	PMU_SLP_S3# on Intel SOC for S3, Suspend to RAM
4	GND	GND
5	GND	GND
6	AFB_DIFF0+ (connected to SMARC pin S62)	USB3_TXP on Intel SOC for USB Super-Speed, positive signal of pair
7	AFB1_OUT (connected to SMARC pin S18)	PMU_SLP_S4# on Intel SOC for S4, Suspend to Disk
8	AFB_DIFF0- (connected to SMARC pin S63)	USB3_TXN on Intel SOC for USB Super-Speed, negative signal of pair
9	AFB2_OUT (connected to SMARC pin S19)	PMU_SUS_STAT# on SOC for Suspend Status
10	GND	GND
11	GND	GND
12	AFB_DIFF1+ (connected to SMARC pin S65)	USB3_RXP on Intel SOC for USB Super-Speed, positive signal of pair
13	AFB3_IN (connected to SMARC pin S20)	Reserved
14	AFB_DIFF1- (connected to SMARC pin S66)	USB3_RXN on Intel SOC for USB Super-Speed, negative signal of pair
15	GND	GND
16	GND	GND
17	AFB4_IN (connected to SMARC pin S21)	Reserved
18	AFB_DIFF2+ (connected to SMARC pin S68)	USB_DP0 on Intel SOC for USB 2.0, positive signal of pair
19	GND	GND
20	AFB_DIFF2- (connected to SMARC pin S69)	USB_DN0 on Intel SOC for USB 2.0, negative signal of pair
21	AFB5_IN (connected to SMARC pin S22)	Reserved
22	GND	GND
23	GND	GND
24	AFB_DIFF3+ (connected to SMARC pin S71)	SATA1_TXP on Intel SOC for SATA high-speed, positive signal of pair
25	AFB6_PTIO (connected to SMARC pin S23)	EN_OC# on AFB for USB super-speed, power enable and over current
26	AFB_DIFF3- (connected to SMARC pin S72)	SATA1_TXN on Intel SOC for SATA high-speed, negative signal of pair
27	AFB7_PTIO (connected to SMARC pin S24)	PCU_SMB_ALERT# on AFB for SM Bus Alert# (interrupt)

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Table 3-23: Alternate Function Block Interface Pin Signals (CN37) (Continued)

28	GND	GND
29	GND	GND
30	AFB_DIFF4+ (connected to SMARC pin S74)	SATA1_RXP on Intel SOC for SATA high-speed, positive signal of pair
31	AFB8_PTIO (connected to SMARC pin S55)	Reserved
32	AFB_DIFF4- (connected to SMARC pin S75)	SATA1_RXN on Intel SOC for SATA high-speed, negative signal of pair
33	AFB9_PTIO (connected to SMARC pin S56)	Reserved
34	GND	GND

NOTE: The shaded table cells denote power or ground.

3.17 GPIO 4-7 (CN39)

Table 3-24 lists the pin signals of the General Purpose IO 4-7 header, which provides 10 pins in 2 rows, odd/even pin sequence (1, 2), and 2.54mm pitch.

Table 3-24: General Purpose IO 4-7 (CN39)

Pin #	Signal
1	+V5P0A
2	CN_GPIO4 (connected to SMARC pin P112)
3	+V3P3S
4	CN_GPIO5 (connected to SMARC pin P113)
5	GND
6	CN_GPIO6 (connected to SMARC pin P114)
7	GND
8	CN_GPIO7 (connected to SMARC pin P115)
9	GND
10	GND

NOTE: These GPIOs are shared function pins. See SMARC Specification 1.1. Shaded table cells denote power or ground

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.18 GPIO 8-11 (CN41)

Table 3-25 lists the pin signals of the General Purpose IO 8-11 header, which provides 10 pins in 2 rows, odd/even pin sequence (1, 2), and 2.54mm pitch.

Table 3-25: General Purpose IO 8-11 (CN41)

Pin #	Signal
1	+V5P0A
2	CN_GPIO8 (connected to SMARC pin P116)
3	+V3P3S
4	CN_GPIO9 (connected to SMARC pin P117)
5	GND
6	CN_GPIO10 (connected to SMARC pin P118)
7	GND
8	CN_GPIO11 (connected to SMARC pin P119)
9	GND
10	GND

NOTE: These GPIOs are shared function pins. See SMARC Specification 1.1. Shaded table cells denote power or ground

3.19 Miscellaneous (CN43)

Table 3-26 lists the pin signals of the Miscellaneous header, which provides 10 pins in 2 rows, odd/even pin sequence (1, 2), and 2.54mm pitch.

Table 3-26: Miscellaneous (CN43)

Pin #	Signal
1	GND
2	BATLOW#
3	GND
4	BB_STBY#
5	GND
6	CHARGER_PRSNT#
7	GND
8	CHARGING#
9	GND
10	LID#

NOTE: Shaded table cells denote power or ground. The # symbol indicates the signal is Active Low.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.20 I2S1 (CN44)

Table 3-27 lists the pin signals of the I2S1 header, which provides 8 pins in a single row with 2.54mm pitch.

Table 3-27: I2S1 Signals (CN44)

Pin #	Signal
1	I2S1_LRCK (connected to SMARC pin S43)
2	+V3P3
3	I2S1_SDOUT (connected to SMARC pin S44)
4	+V1P8
5	I2S1_SDIN (connected to SMARC pin S45)
6	GND
7	I2S1_CK (connected to SMARC pin S46)
8	GND

NOTE: Shaded table cells denote power or ground.

3.21 Smart Battery (BattMan) Interface (CN45)

Table 3-28 lists the pin signals of the Smart Battery header, which provides 10 pins in 2 rows, odd/even pin sequence (1, 2), and 2.54mm pitch.



You must configure the jumper settings as described in Table 3-28, or system damage could occur when using a BattMan power supply to Power On the carrier.

Table 3-28: Smart Battery (BattMan) Interface (CN45)

Pin #	Signal	Jumper Settings
1	SMB_CLK (SMBus clock)	Make sure to set following jumper configurations before implementing a BattMan power supply to Power On the carrier: • Install a jumper on the 2-pin jumper header, **CN3** (Enable BattMan power rail) • Install a jumper on the 2-pin jumper header, **CN4** (Low active Enable for BattMan) • Installed a jumper on pins 1-2 of the **CN81** jumper header (VIN_PWR_BAD#, +5V_SBY) • Install a jumper on pins 2-3 of the **CN82** jumper header (BattMan SMBus, 5 volts)
2	SMB_DAT (SMBus data)	
3	Not Connected	
4	Not Connected	
5	ATX_PS_ON (ATX power supply)	
6	Not Connected	
7	+V12P0_ATX (12-volt power)	
8	+V5P0_SBY (5-volt standby power)	
9	SMB_ALERT# (SMBus alert)	
10	GND	

NOTE: The voltage level of this interface is determined by the CN82 jumper header (default 5V for BattMan supply.) Shaded table cells denote power or ground.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.22 Battery Enable (CN46)

Table 3-29 lists the pin signals of the coin cell battery enable jumper header, which provides 2 pins with 2.00mm pitch.

Table 3-29: Battery Enable (CN46)

Pin #	Signal	Jumper Position
1	3V_BAT	• Jumper Installed (1-2) - coin cell battery socket enabled (**Default**) • Empty - coin cell battery socket disabled
2	+VDD_RTC	

3.23 Boot Select (CN48, CN49, CN50, CN51)

Table 3-30 defines how to configure the Boot Select jumper headers for each device from which the system may boot. Each Boot Select jumper header provides 3 pins in a single row with 2.54mm pitch and the following signals: Pin 1 is not connected; pin 2 is BOOT_SEL#; pin 3 is ground

Table 3-30: Boot Select (CN48, CN49, CN50, CN51)

Boot Device	CN48 (SEL0#) ON=2-3 OFF=Float Jumper	CN49 (SEL1#) ON=2-3 OFF=Float Jumper	CN50 (SEL2#) ON=2-3 OFF=Float Jumper	CN51 (RECOV#) ON=2-3 OFF=Float Jumper
Carrier SATA	ON	ON	ON	OFF
Carrier SDIO	OFF	ON	ON	OFF
Carrier eMMC	ON	OFF	ON	OFF
Carrier SPI	OFF	OFF	ON	OFF
Module NAND	ON	ON	OFF	OFF
Module NOR	OFF	ON	OFF	OFF
Module eMMC	ON	OFF	OFF	OFF
Module SPI	OFF	OFF	OFF	OFF
Force Recovery	OFF	OFF	OFF	ON

NOTE: The # symbol indicates the signal is Active Low.

3.24 FAN Voltage Select (CN52)

Table 3-31 lists the pin signals of the Fan Voltage Select jumper header, which provides 3 pins in a single row with 2.54mm pitch.

Table 3-31: FAN Voltage Select (CN52)

Pin #	Signal
1	+V12P0_ATX
2	GND
3	+V5P0A

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.25 FAN (CN53)

Table 3-32 lists the pin signals of the CPU fan header, which provides 3 pins in a single row with 2.54mm pitch.

Table 3-32: FAN (CN53)

Pin #	Signal
1	GND
2	GND
3	FAN_TACH_IN
4	FAN_PWM_OUT

NOTE: Shaded table cells denote ground.

3.26 SPI Power Voltage Select (CN54)

Table 3-33 lists the pin signals of the SPI Voltage Select jumper header, which provides 3 pins in a single row with 2.54mm pitch.

Table 3-33: SPI Power Voltage Select (CN54)

Pin #	Signal
1	+V1P8S
2	+VCC_SPI
3	+V3P3S

3.27 SPDIF I/O [SMARC] (CN55)

Table 3-34 lists the pin signals of the SPDIF I/O header, which provides 4 pins 2 rows, odd/even pin sequence (1, 2) with 2.00mm pitch. These signals are connected directly to the SMARC connector.

Table 3-34: Digital Audio [SMARC] Signals (CN55)

Pin #	Signal	Description
1	CON_SPDIFI	Digital Audio In
2	GND	Ground
3	CON_SPDIFO	Digital Audio Out
4	GND	Ground

NOTE: Shaded table cells denote ground.

3.28 MIC_BIAS to MIC Enable (CN57)

Table 3-35 lists the pin signals of the MIC_BIAS to MIC jumper header, which provides 2 pins with 2.00mm pitch.

Table 3-35: MIC_BIAS to MIC (CN57)

Pin #	Signal	Jumper Position
1	MIC_FIL	• Jumper Installed (1-2) - MIC_BIAS to MIC enabled (**Default**) • Empty - MIC_BIAS to MIC disabled
2	MIC_BIAS_FIL	

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.29 I2S0_SDIN Codec Select (CN58)

Table 3-36 lists the pin signals of the I2S0_SDIN Codec Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-36: I2S0_SDIN Codec Select (CN58)

Pin #	Signal	Jumper Position
1	I2S0_SDIN_C1	• Jumper Installed 1-2 - CODEC SGTL5000 (**Default**) • Jumper Installed 2-3 - CODEC AIC3106
2	I2S0_SDIN	
3	I2S0_SDIN_C2	

3.30 I2S0_SDOUT Codec Select (CN59)

Table 3-37 lists the pin signals of the I2S0_SDOUT Codec Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-37: I2S0_SDOUT Codec Select (CN59)

Pin #	Signal	Jumper Position
1	I2S0_SDOUT_C1	• Jumper Installed 1-2 - CODEC SGTL5000 (**Default**) • Jumper Installed 2-3 - CODEC AIC3106
2	I2S0_SDOUT	
3	I2S0_SDOUT_C2	

3.31 I2S0_LRCK Codec Select (CN60)

Table 3-38 lists the pin signals of the I2S0_LRCK Codec Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-38: I2S0_LRCK Codec Select (CN60)

Pin #	Signal	Jumper Position
1	I2S0_LRCK_C1	• Jumper Installed 1-2 - CODEC SGTL5000 (**Default**) • Jumper Installed 2-3 - CODEC AIC3106
2	I2S0_LRCK	
3	I2S0_LRCK_C2	

3.32 I2S0_CK Codec Select (CN61)

Table 3-39 lists the pin signals of the I2S0_CK Codec Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-39: I2S0_CK Codec Select (CN61)

Pin #	Signal	Jumper Position
1	I2S0_CK_C1	• Jumper Installed 1-2 - CODEC SGTL5000 (**Default**) • Jumper Installed 2-3 - CODEC AIC3106
2	I2S0_CK	
3	I2S0_CK_C2	

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.33 LIN_L Codec Select (CN62)

Table 3-40 lists the pin signals of the LIN_L Codec Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-40: LIN_L Codec Select (CN62)

Pin #	Signal	Jumper Position
1	LIN_L_C1	• Jumper Installed 1-2 - CODEC SGTL5000 (**Default**) • Jumper Installed 2-3 - CODEC AIC3106
2	LIN_L_FIL	
3	LIN_L_C2	

3.34 LIN_R Codec Select (CN63)

Table 3-41 lists the pin signals of the LIN_R Codec Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-41: LIN_R Codec Select (CN63)

Pin #	Signal	Jumper Position
1	LIN_R_C1	• Jumper Installed 1-2 - CODEC SGTL5000 (**Default**) • Jumper Installed 2-3 - CODEC AIC3106
2	LIN_R_FIL	
3	LIN_R_C2	

3.35 LOUT_L Codec Select (CN64)

Table 3-42 lists the pin signals of the LOUT_L Codec Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-42: LOUT_L Codec Select (CN64)

Pin #	Signal	Jumper Position
1	LOUT_L_C1	• Jumper Installed 1-2 - CODEC SGTL5000 (**Default**) • Jumper Installed 2-3 - CODEC AIC3106
2	LOUT_L_FIL	
3	LOUT_L_C2	

3.36 LOUT_R Codec Select (CN65)

Table 3-43 lists the pin signals of the LOUT_R Codec Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-43: LOUT_R Codec Select (CN65)

Pin #	Signal	Jumper Position
1	LOUT_R_C1	• Jumper Installed 1-2 - CODEC SGTL5000 (**Default**) • Jumper Installed 2-3 - CODEC AIC3106
2	LOUT_R_FIL	
3	LOUT_R_C2	

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.37 MIC_BIAS Codec Select (CN66)

Table 3-44 lists the pin signals of the MIC_BIAS Codec Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-44: MIC_BIAS Codec Select (CN66)

Pin #	Signal	Jumper Position
1	MIC_BIAS_C1	• Jumper Installed 1-2 - CODEC SGTL5000 (**Default**) • Jumper Installed 2-3 - CODEC AIC3106
2	MIC_BIAS_FIL	
3	MIC_BIAS_C2	

3.38 MIC Codec Select (CN67)

Table 3-45 lists the pin signals of the MIC Codec Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-45: MIC Codec Select (CN67)

Pin #	Signal	Jumper Position
1	MIC_C1	• Jumper Installed 1-2 - CODEC SGTL5000 (**Default**) • Jumper Installed 2-3 - CODEC AIC3106
2	MIC_FIL	
3	MIC_C2	

3.39 GND_ANALOG Codec Select (CN68)

Table 3-46 lists the pin signals of the GND_ANALOG Codec Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-46: GND_ANALOG Codec Select (CN68)

Pin #	Signal	Jumper Position
1	AGND_C1	• Jumper Installed 1-2 - CODEC SGTL5000 (**Default**) • Jumper Installed 2-3 - CODEC AIC3106
2	GND_ANALOG	
3	AGND_C2	

3.40 I2C CAM (CN69)

Table 3-47 lists the pin signals of the I2C CAM header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-47: I2C CAM (CN69)

Pin #	Signal
1	I2C_CAM_CK_3V
2	I2C_CAM_DAT_3V
3	Ground

NOTE: Shaded table cell denotes ground.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.41 I2C GP (CN70)

Table 3-48 lists the pin signals of the I2C GP header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-48: I2C GP (CN70)

Pin #	Signal
1	I2C_GP_CK_3V
2	I2C_GP_DAT_3V
3	Ground

NOTE: Shaded table cell denotes ground.

3.42 I2C LCD (CN71)

Table 3-49 lists the pin signals of the I2C LCD header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-49: I2C LCD (CN71)

Pin #	Signal
1	I2C_LCD_CK_3V
2	I2C_LCD_DAT_3V
3	Ground

NOTE: Shaded table cell denotes ground.

3.43 I2C PM (CN72)

Table 3-50 lists the pin signals of the I2C PM header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-50: I2C PM (CN72)

Pin #	Signal
1	I2C_PM_CK_3V
2	I2C_PM_DAT_3V
3	Ground

NOTE: Shaded table cell denotes ground.

3.44 Camera, PCAM / CSI (CN80)

Table 3-51 lists the pin signals of the Camera, PCAM / CSI board-to-board connector, which provides 64-pins, 2 rows, odd/even pin sequence (1, 2) with 0.50mm pitch. These signals are connected directly to the MIPI CSI camera interface at the SMARC connector.

Table 3-51: Camera, PCAM / CSI Signals (CN80)

Pin#	Signal	Pin#	Signal
1	GND	2	GND
3	PCAMD9_CSI1D3N_R	4	CAM1_2V8
5	PCAMD8_CSI1D3P_R	6	CAM1_2V8
7	GND	8	CAM0_2V8
9	PCAMD7_CSI1D2N_R	10	CAM0_2V8
11	PCAMD6_CSI1D2P_R	12	GND
13	GND	14	PCAM_MCK_R

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Table 3-51: Camera, PCAM / CSI Signals (CN80) (Continued)

15	PCAMD5_CSI1D1N_R PCAMD4_CSI1D1P_R	16	Not Connected
17		18	Not Connected
19	GND	20	CAM_MCK_R
21	PCAMD3_CSI1D0N_R PCAMD2_CSI1D0P_R	22	GND
23		24	CAM1_1V8
25	GND	26	CAM1_1V8
27	PCAMD1_CSI1CKN_R PCAMD0_CSI1CKP_R	28	CAM0_1V8
29		30	CAM0_1V8
31	GND	32	GND
33	CSI0_D1_N_R CSI0_D1_P_R	34	CAM_VSYS
35		36	CAM_VSYS
37	GND	38	CAM_VSYS
39	CSI0_D0_N_R CSI0_D0_P_R	40	GND
41		42	+V1P5S
43	GND	44	I2C_CAM_CK_R
45	CSI0_CK_N_R CSI0_CK_P_R	46	I2C_CAM_DAT_R
47		48	GND
49	GND	50	CAM0_PWR#_R
51	CAM1_RST#_R CAM1_PWR#_R	52	PCAM_FLD_R
53		54	PCAM_DE_R
55	GND	56	GND
57	CAM0_RST#_R PCAM_PXL_CK0_R	58	PCAM_VSYNC_R
59		60	PCAM_HSYNC_R
61	GND	62	GND
63	GND	64	GND

NOTE: Shaded table cells denote power or ground.

3.45 VIN_PWR_BAD Source Select (CN81)

Table 3-52 lists the pin signals of the VIN_PWR_BAD Source Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-52: VIN_PWR_BAD Source Select (CN81)

Pin #	Signal	Jumper Position
1	+V5P0_SBY	• Jumper Installed 1-2 - 5-volt standby source • Jumper Installed 2-3 - 5-volt ATX source (**Default**)
2	VIN_PWR_BAD#	
3	ATX_PWRGD_5V	

NOTE: For BattMan operation, this header requires a jumper installed on pins 1-2. The # symbol indicates the signal is Active Low.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.46 BatMan SMBus Voltage Select (CN82)

Table 3-53 lists the pin signals of the BatMan SMBus voltage select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-53: BatMan SMBus Voltage Select (CN82)

Pin #	Signal	Jumper Position
1	+V3PS	• Jumper Installed 1-2 - 3.3-volt standby source • Jumper Installed 2-3 - 5-volt ATX source (**Default**)
2	I2C_PM_VSEL	
3	+V5P0A	

3.47 Display Mode Select (CN85)

Table 3-54 lists the pin signals of the Display Mode select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-54: Display Mode Select (CN85)

Pin #	Signal	Jumper Position
1	+V3PS	• Jumper Installed 1-2 - HDMI B mode • Jumper Installed 2-3 - Display Port mode (**Default**)
2	DP/HDMI_SEL2	
3	GND	

3.48 Display Port Control Switch (SW6)

Table 3-55 lists the pin signals of the Display Port Control dip switch, which provides 4 poles, 8 pin positions with 1.27mm pitch.

Table 3-55: Display Port Control Switch (SW6)

Pin #	Signal	Pin#	Signal
1 (off)	DP_CNTRL [**Default**]	8 (on)	+V3P3S
2 (off)	DP_CNTRL [**Default**]	7 (on)	GND
3 (off)	DP_EQ [**Default**]	6 (on)	+V3P3S
4 (off)	DP_EQ [**Default**]	5 (on)	GND

3.49 Display Port Control Switch (SW7)

Table 3-56 lists the pin signals of the Display Port Control dip switch, which provides 8 poles, 16 pin positions with 1.27mm pitch.

Table 3-56: Display Port Control Switch (SW7)

Pin #	Signal	Pin#	Signal
1 (off)	DP_ENABLE [**Default**]	16 (on)	GND
2 (off)	DP_AUTOEQ [**Default**]	15 (on)	GND
3 (off)	DP_OC_0 [**Default**]	14 (on)	GND
4 (off)	DP_OC_1 [**Default**]	13 (on)	GND
5 (off)	DP_OC_0 [**Default**]	12 (on)	GND
6 (off)	DP_OC_1 [**Default**]	11 (on)	GND
7 (off)	Not Connected [**Default**]	10 (on)	Not Connected
8 (off)	Not Connected [**Default**]	9 (on)	Not Connected

NOTE: Refer to the PI3EQXDP1201 Display Port Redriver datasheet for more details.

.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Appendix A Technical Support

ADLINK Technology, Inc. provides a number of methods for contacting Technical Support listed in Table A-1 below. Requests for support through Ask an Expert are given the highest priorities, and usually will be addressed within one working day.

- ADLINK Ask an Expert – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the ADLINK web site at http://www.adlinktech.com/AAE/. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online if you wish to use the Ask a Question feature.

ADLINK strongly suggests that you register with the web site. By creating a profile on the ADLINK web site, you will have a portal page called “My ADLINK”, unique to you with access to exclusive services and account information.

- Personal Assistance – You may also request personal assistance by creating an Ask an Expert account and then going to the Ask a Question feature. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request, you must log in to go to the My Question area where you can check status, update your request, and access other features.
- Download Service – This service is also free and available 24 hours a day at http://www.adlinktech.com. For certain downloads such as technical documents and software, you must register online before you can log in to this service.

Table A-1: Technical Support Contact Information

Method	Contact Information
Ask an Expert	http://www.adlinktech.com/AAE/
Web Site	http://www.adlinktech.com
Standard Mail	**ADLINK Technology, Inc.** Address: 9F, No.166 Jian Yi Road, Zhonghe District New Taipei City 235, Taiwan 新北市中和區建一路 166 號 9 樓 Tel: +886-2-8226-5877 Fax: +886-2-8226-5717 Email: service@adlinktech.com **Ampro ADLINK Technology, Inc.** Address: 5215 Hellyer Avenue, #110 San Jose, CA 95138, USA Tel: +1-408-360-0200 Toll Free: +1-800-966-5200 (USA only) Fax: +1-408-360-0222 Email: info@adlinktech.com **ADLINK Technology (China) Co., Ltd.** Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203) 300 Fang Chun Rd., Zhangjiang Hi-Tech Park Pudong New Area, Shanghai, 201203 China Tel: +86-21-5132-8988 Fax: +86-21-5132-3588 Email: market@adlinktech.com

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Table A-1: Technical Support Contact Information (Continued)

ADLINK Technology Beijing
Address: 北京市海淀区上地东路 1 号盈创动力大厦 E 座 801 室(100085)
Rm. 801, Power Creative E, No. 1 Shang Di East Rd.
Beijing, 100085 China
Tel: +86-10-5885-8666
Fax: +86-10-5885-8626
Email: market@adlinktech.com

ADLINK Technology Shenzhen
Address: 深圳市南山区科技园南区高新南七道 数字技术园
A1 栋 2 楼 C 区 (518057)
2F, C Block, Bldg. A1, Cyber-Tech Zone, Gao Xin Ave. Sec. 7
High-Tech Industrial Park S., Shenzhen, 518054 China
Tel: +86-755-2643-4858
Fax: +86-755-2664-6353
Email: market@adlinktech.com

LiPPERT ADLINK Technology GmbH
Address: Hans-Thoma-Strasse 11
D-68163 Mannheim, Germany
Tel: +49-621-43214-0
Fax: +49-621 43214-30
Email: emea@adlinktech.com

PENTA ADLINK Technology GmbH
Ulrichsbergerstrasse 17
94469 Deggendorf, Germany
Tel: +49 (0) 991 290 94 – 10
Fax: +49 (0) 991 290 94 - 29
Email: emea@adlinktech.com

ADLINK Technology, Inc. (French Liaison Office)
Address: 6 allée de Londres, Immeuble Ceylan
91940 Les Ulis, France
Tel: +33 (0) 1 60 12 35 66
Fax: +33 (0) 1 60 12 35 66
Email: france@adlinktech.com

ADLINK Technology Japan Corporation
Address: 〒101-0045 東京都千代田区神田鍛冶町 3-7-4
神田 374 ビル 4F
KANDA374 Bldg. 4F, 3-7-4 Kanda Kajicho,
Chiyoda-ku, Tokyo 101-0045, Japan
Tel: +81-3-4455-3722
Fax: +81-3-5209-6013
Email: japan@adlinktech.com

ADLINK Technology, Inc. (Korean Liaison Office)
Address: 경기도 성남시 분당구 수내로 46 번길 4 경동빌딩 2 층
(수내동 4-4 번지) (우) 463-825
2F, Kyungdong B/D, 4 Sunae-ro 46 beon-gil
Bundang-gu, Seongnam-si, Gyeonggi-do, Korea, 13595
Toll Free +82-80-800-0585
Tel +82-31-786-0585
Fax +82-31-786-0583
Email: korea@adlinktech.com

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Table A-1: Technical Support Contact Information (Continued)

	ADLINK Technology Singapore Pte. Ltd. Address: 84 Genting Lane #07-02A, Cityneon Design Centre Singapore 349584 Tel: +65-6844-2261 Fax: +65-6844-2263 Email: singapore@adlinktech.com **ADLINK Technology Singapore Pte. Ltd. (Indian Liaison Office)** Address: #50-56, First Floor, Spearhead Towers Margosa Main Road (between 16th/17th Cross) Malleswaram, Bangalore - 560 055, India Tel: +91-80-65605817, +91-80-42246107 Fax: +91-80-23464606 Email: india@adlinktech.com **ADLINK Technology, Inc. (Israeli Liaison Office)** Address: 27 Maskit St., Corex Building PO Box 12777 Herzliya 4673300, Israel Tel: +972-54-632-5251 Fax: +972-77-208-0230 Email: israel@adlinktech.com **ADLINK Technology, Inc. (UK Liaison Office)** Tel: +44 774 010 59 65 Email: UK@adlinktech.com

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000