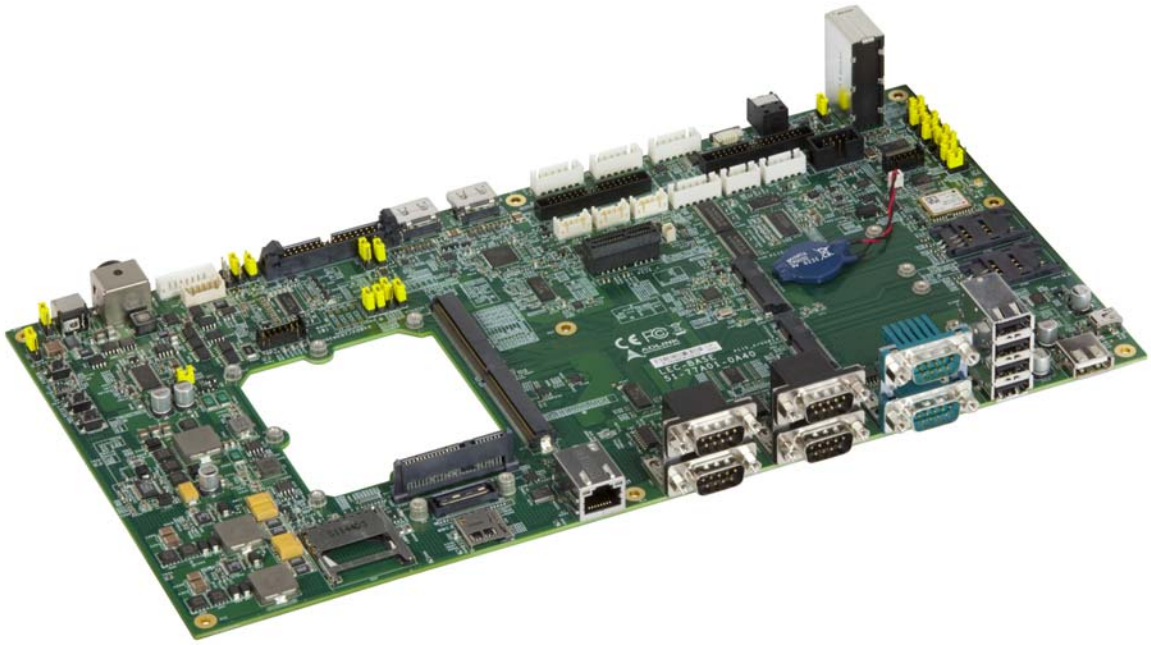
LEC-BASE

(SMARC Baseboard)

Technical Reference
P/N 50-1Z157-1010
Rev 1.01



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Revision History

Revision	Reason for Change	Date
1000	Initial Release	Dec/13
1.01	Revised board interface layout; updated interface pinout tables; changed this document's revision number from 1000 to 1.01	Apr/15

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Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

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For user safety, please read and follow all **Instructions**, **WARNINGs**, **CAUTIONs,** and **NOTEs** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,

If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

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1 Overview

This initial manual version presents a general overview of the LEC-BASE baseboard including the signal definitions of the non-standard user interfaces on the board. After reviewing this document you should understand the following features of the LEC-BASE.

- Functional Block Diagram
- Major Component (IC) Locations and Descriptions
- Connector Locations and Descriptions
- Specifications
- Non-Standard User Interface Signal Definitions (support is dependent on the specific SMARC module; refer to the specific SMARC module manual for details)

1.1 Block Diagram

Figure 1-1 presents a functional representation of the baseboard.

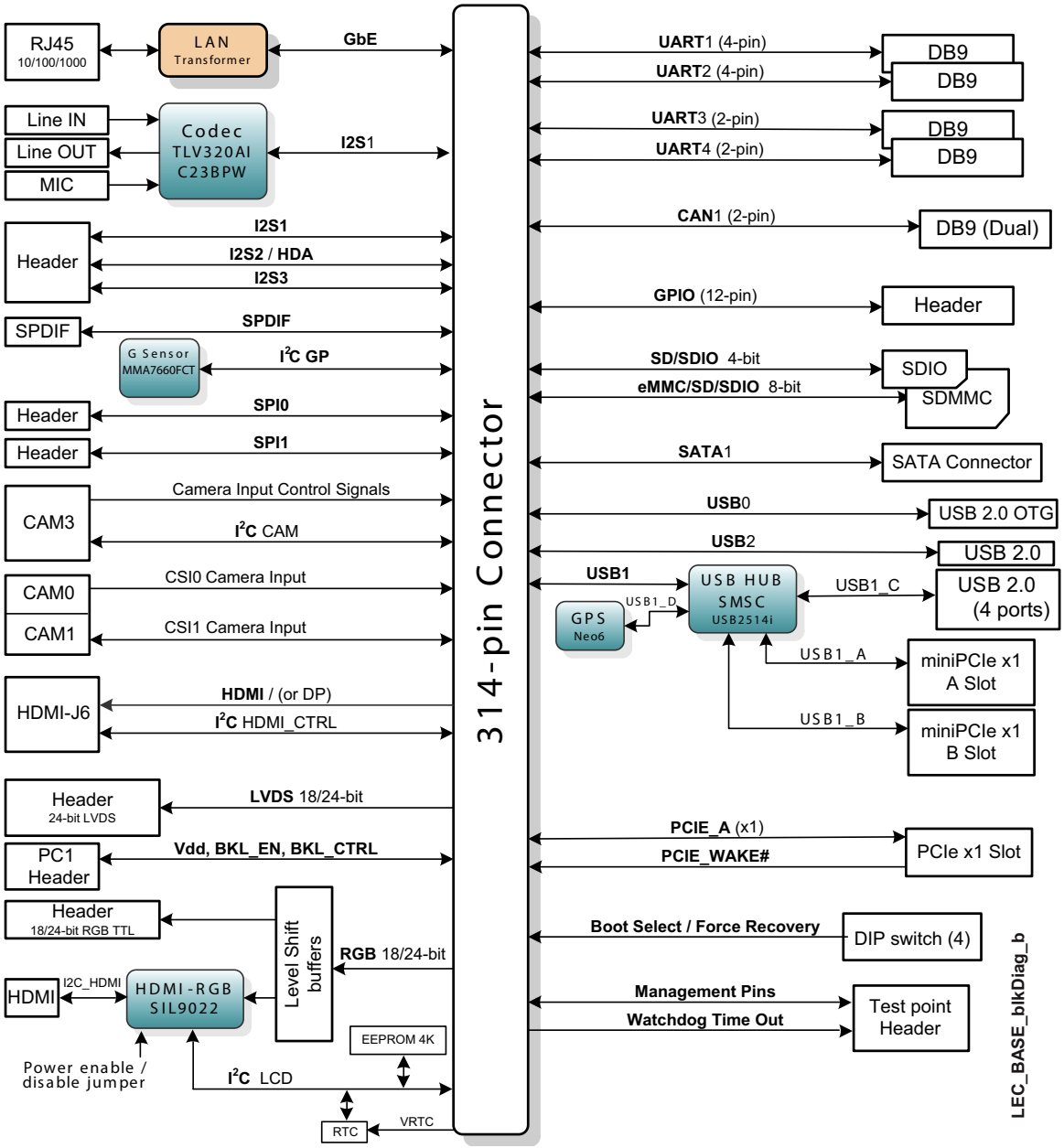


Figure 1-1: Functional Block Diagram

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1.2 Major Components (ICs)

Table 1-1 lists the major integrated circuits on the LEC-BASE, including a brief description of each IC. Figure 1-2 shows the locations of the major ICs.

Table 1-1: Major Integrated Circuit Descriptions and Functions

Chip Type	Mfg.	Model	Description	Function
G-Sensor (U4)	Freescale Semiconductor	MMA7660FC	3-axis Orientation/ Motion Detection Sensor, connected to the I2C GP interface at pins S48 and S49 of the SMARC connector. The I2C address is 0x4C/0x4D.	Senses data changes, product orientation, and gestures through an interrupt (INT) pin.
Touch Panel Controller (U18)	Texas Instruments	TSC2046	Low-Voltage Touch Controller, connected to the SPIO interface at pins P43, P44, P45, and P46 of the SMARC connector.	Senses 4-wire resistive touch screen.
I2C, 2-wire EEPROM (U19)	Atmel	AT24C08C	2-wire, 8Kb serial EEPROM, connected to the I2C LCD interface at pins S139 and S140 of the SMARC connector. The I2C address is 0xA8/0xA9.	Provides storage for baseboard parameters through the I^2C LCD pins, S139 and S140, on the SMARC module.
CAN Transceiver (U25, U26)	Texas Instruments	SN65HVDA540QDR	Transceiver for Controller Area Network, connected to the CAN0 and CAN1 interfaces at pins P143, P144, P145, and P146 of the SMARC connector.	Provides up to 1 Mbps of differential transmit and receive capabilities for the CAN controller in the CPU.
I2S Audio CODEC (U27)	Texas Instruments	TLV320AIC23B	I2S Stereo Audio CODEC, connected to the I2S0 interface at pins S39, S40, S41, S42 of the SMARC connector.	Supports data-transfer word lengths of 16, 20, 24, and 32 bits with sample rates from 8kHz to 96kHz.
Real Time Clock (U36)	Maxim	DS1337S	I2C Serial Real-Time Clock, connected to the I2C LCD interface at pins S139 and S140 of the SMARC connector. The I2C address is 0xD0/0xD1.	Provides low-power clock/ calendar with two programmable time-of-day alarms and a programmable square-wave output
GPS Module (U136)	u-blox	NEO-Q-0	GPS Receiver, connected over the USB hub to the SMARC connector at pins P65 and P66.	Provides 6-positioning engine for parallel time/frequency space searches

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Key:
U4 - G-Sensor
U18 - Touch Panel Controller
U19 - I2C EEPROM
U25, U26 - CAN Transceivers
U27 - Audio CODEC
U36 - Real Time Clock
U136 - GPS Module

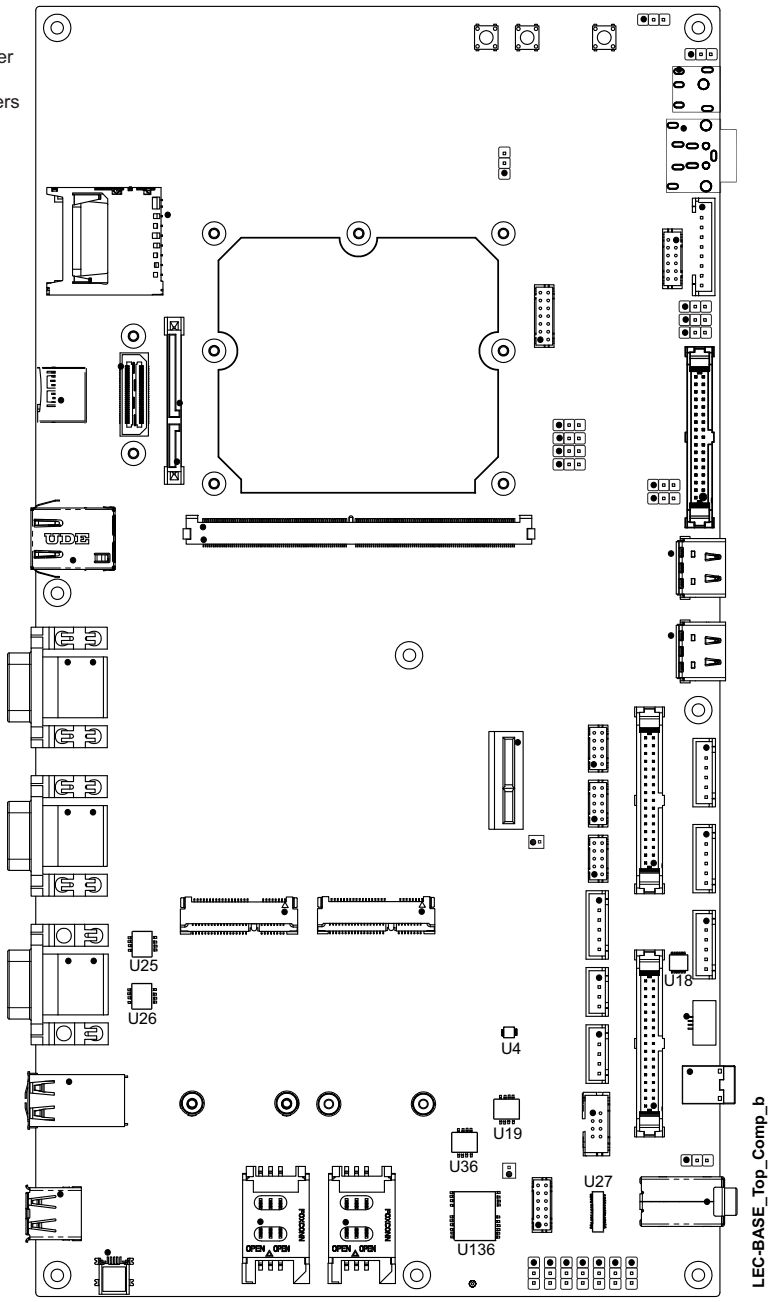


Figure 1-2: Component Locations (Top Side)

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1.3 Interface Headers, Jumper Headers, Switches, LEDs, and Connectors

Table 1-2 describes the headers, switches, LEDs, and connectors for the LEC-BASE baseboard shown in Figure 1-3.

Table 1-2: Header, Switch, LED, and Connector Descriptions

Header / Connector#	Signal / Device	Description
AFB2	SD/eMMC Card	60-pin terminal for eMMC card
AJ1	Audio Jack	32-pin standard audio jack for three audio interfaces: Line In (Blue), Line Out (Green), and MIC In (Pink)
ANT1	GPS Antenna	3-pin, radio frequency, 50 ohm antenna for receiving GPS signals
CAM0	Camera	10-pin header for MIPI CSI1 camera
CAM1	Camera	10-pin header for MIPI CSI0 camera
CAM3	Camera Control	10-pin header for I2C clock/data signals on MIPI CSI camera
CAN1 (two ports)	CAN Bus	Dual, 9-pin standard DB9 connectors for transmitting and receiving Controller Area Network signals
CN1	Touch Screen	4-pin, standard connector for 4-wire resistive touch controller (not for TTL USB-based touch screen controller in Starter Kit)
CN2	microSD	12-pin, standard socket for microSD memory cards
CN4	Cell Charger/Battery Supply	12-pin header for 2-cell, raw lithium ion battery interface to power the baseboard
CN5	MiniDin DC Jack	4-pin, female connector for additional power input for auxiliary circuitry
COM1 (two ports)	UART	Dual, 9-pin standard DB9 connectors for RS232 serial ports
COM2 (two ports)	UART	Dual, 9-pin standard DB9 connectors for RS232 serial ports
GPIO1	GPIO	12-pin header for General Purpose IO
H25	Battery2	9-pin header for smart battery connection
I2S1	I2S Devices	6-pin header for I2S devices such as audio CODECs, baseband modems, and touch controllers
I2S2	I2S Devices	6-pin header for I2S devices such as audio CODECs, baseband modems, and touch controllers
I2S3	I2S Devices	6-pin header for I2S devices such as audio CODECs, baseband modems, and touch controllers (designated also for HD Audio CODECs)
J1	SMARC Interface	314-pin, MXM socket for Memory, Video, and I/O functions
J3	TTL	34-pin header for VGA LCD flat panel output
J6	HDMI1	19-pin, standard HDMI micro connector
J8	LVDS	34-pin header for LVDS output
J9 (AFB1)	Auxiliary Devices	34-pin header for differential pair and data bit signals
J10	I2C	2-pin header for general purpose, level-shifted 3.3V, I2C clock and data signals for the module
J11	HDMI2	19-pin, standard HDMI micro connector
J12	Battery	2-pin header for RTC external battery
J14	LVDS Control	8-pin header for LVDS panel and backlight control
JACK1	DC Power	6-pin, standard, right-angle 19V center-pin, DC power jack
JP2	LCD Power Select	3-pin, jumper header for LCD 3.3V (1-2) or 5V (2-3) power selection
JP3	I2C Select	3-pin, jumper header to select I2C_LCD (clock/data pair) for HDMI controller (1-2 default)

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Table 1-2: Header, Switch, LED, and Connector Descriptions (Continued)

JP4	Battery Charger Enable	3-pin jumper header for enabling the smart battery/cell charger: ON (1-2) or OFF (2-3)
JP5	Cell Charger Present	3-pin jumper header to accept charging (1-2 if cell present; 2-3 if cell not present)
JP6	Cell Charger Voltage	3-pin jumper header for I2C voltage selection (pins 2-3 for 2.5V or pins 1-2 for 3.3V) between cell and charger
JP7	Cell Protection IC, I2C Signal Pair	3-pin header to allow Texas Instruments software to communicate with the cell protection IC: 1=Data, 2=Clock, and 3=GND
JP8	LCD/LVDS Select (High = 1-2; Low = 2-3)	3-pin jumper header to make selection between LCD and LVDS (JP9 Low and JP8 High = LVDS; JP9 High and JP8 Low = LCD; JP9 High and JP8 High = None)
JP9	LCD/LVDS Select (High = 1-2; Low = 2-3)	3-pin jumper header to make selection between LCD and LVDS (JP9 Low and JP8 High = LVDS; JP9 High and JP8 Low = LCD; JP9 High and JP8 High = None)
JP10	LVDS	3-pin jumper header for selecting strobe for LVDS converter: rising edge 1-2, falling edge 2-3
JP11	LVDS	3-pin jumper header for powering ON/OFF LVDS controller: ON 1-2, OFF 2-3
JP12	LVDS Backlight Control (for J14)	3-pin jumper header for backlight power management to select 3V (1-2) or 5V (2-3)
JP13	LVDS Panel Control (for J14)	3-pin jumper header for panel power to select 3V (1-2) or 5V (2-3)
JP14	LVDS Backlight Control (for J14)	3-pin jumper header for backlight power management to select 12V (1-2) or 5V (2-3)
JP15	I2C Select (related to JP3)	3-pin jumper header tor selecting I2C_HDMI for HDMI controller (2-3 Default)
JP16	Boot Select 0	3-pin jumper header for Boot Select Switch SW1 pins 1 and 8 (Pins 2-3 to ground boot_sel0; pins 1-2 to float boot_sel0)
JP17	Boot Select 1	3-pin jumper header for Boot Select Switch SW1 pins 1 and 8 (Pins 2-3 to ground boot_sel1; pins 1-2 to float boot_sel1)
JP18	Boot Select 2	3-pin jumper header for Boot Select Switch SW1 pins 1 and 8 (Pins 2-3 to ground boot_sel2; pins 1-2 to float boot_sel2)
JP19	Boot Select Force Recovery	3-pin jumper header for Boot Select Switch SW1 pins 4 and 5 (Pins 2-3 to ground force_recover; pins 1-2 to float force_recover)
JP20	VIO Select (IO Voltage)	3-pin jumper header for VIO 1.8V (1-2) [no other option is valid, as defined by the SMARC specification]
JP21	DC-OUT	3-pin jumper header to override (1-2) or not override (2-3) power button (PWRON1) for automatic Power On testing
LAN1	Ethernet	8-pin, standard RJ45 jack for Gigabit Ethernet port
LED1	USB	Green LED indicating USB is operational
LED2	Mini PCIE1	Green LED indicating WAN
LED3	Mini PCIE2	Green LED indicating WAN
LED4	nLID	Green LED indicating active low LID signal is asserted
LED5	nSLEEP	Green LED indicating active low SLEEP signal is asserted
LED6	nBATLOW	Green LED indicating active low BATLOW signal is asserted
LED7	SATA	Green LED indicating SATA activity
LED8	SD Card	Green LED indicating over current on SD card
LED9	USB	Green LED indicating USB is operational
LED11	Cell Protection IC	Green LED indicating battery pack conditions

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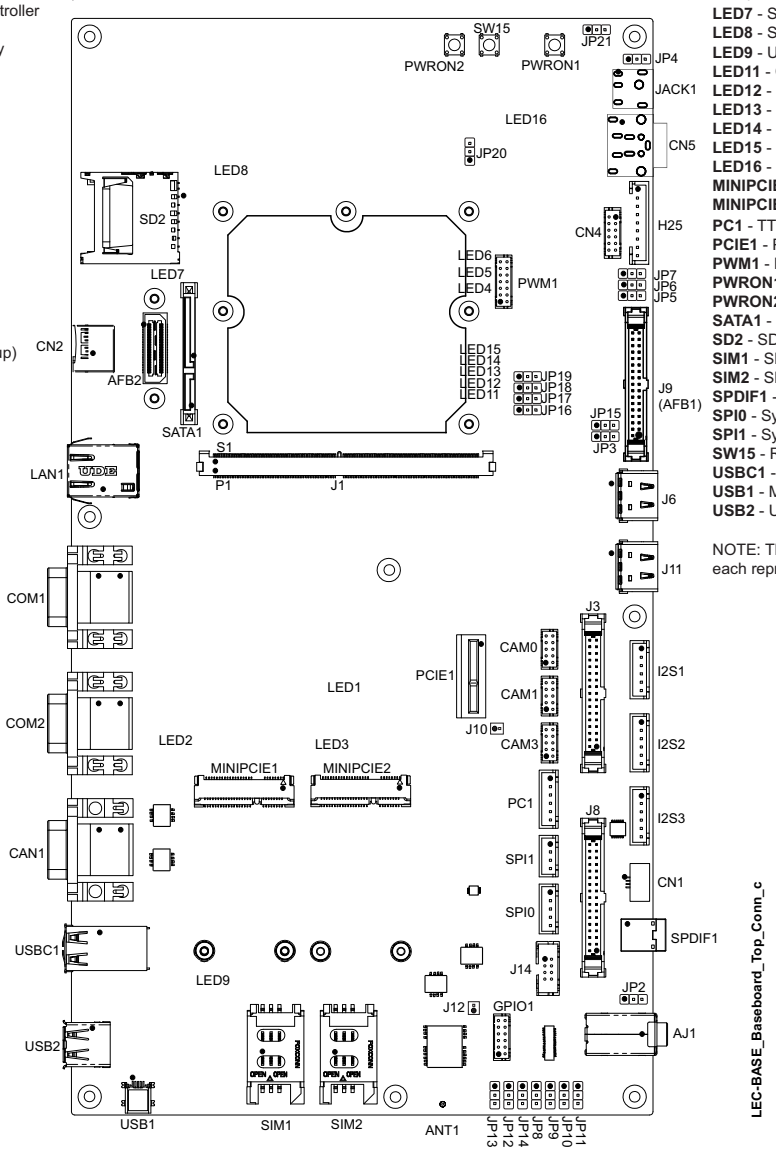
Table 1-2: Header, Switch, LED, and Connector Descriptions (Continued)

LED12	Cell Protection IC	Green LED indicating battery pack conditions
LED13	Cell Protection IC	Green LED indicating battery pack conditions
LED14	Cell Protection IC	Green LED indicating battery pack conditions
LED15	Cell Protection IC	Green LED indicating battery pack conditions
LED16	Power	Green LED indicating power asserted to baseboard
MINIPCIE1	PCIE Mini Card	52-pin, standard, right-angle socket for PCI Express Mini Card
MINIPCIE2	PCIE Mini Card	52-pin, standard, right-angle socket for PCI Express Mini Card
PC1	TTL Panel Control	6-pin header for control signals to flat panel display
PCIE1	PCI Express	36-pin, standard edge connector for x1 PCI Express interface
PWM1	Power Management	14-pin header for Power Management signals
PWRON1	Power On	4-pin, push-button switch to turn on 12V to baseboard
PWRON2	Power On	4-pin, push-button switch to assert POWER_nBTN signal for SMARC connector
SATA1	SATA	7-pin, standard Serial ATA connector with attached 15-pin power connection
SD2	SD Card Slot	Standard slot connector for Secure Digital memory card
SIM1	SIM Slot	Standard slot connector for Subscriber Identity Module
SIM2	SIM Slot	Standard slot connector for Subscriber Identity Module
SPDIF1	SPDIF-OUT Audio	Standard connector for SPDIF digital audio interface
SPI0	System Packet Interface	5-pin header for SPI interface
SPI1	System Packet Interface	4-pin header for SPI interface
SW15	Reset Switch	Push-button switch to warm reset the module
USBC1	USB	4-stack, standard USB 2.0 connector
USB1	Micro-USB	Standard connector for micro-USB interface, OTG
USB2	USB	Standard connector for single USB 2.0 interface

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Key:

AFB2 - Alternate Function Block 2
AJ1 - Audio Jack
ANT1 - GPS Antenna
CAM0 - Camera 0
CAM1 - Camera 1
CAM3 - Camera 3
CAN1 - Controller Area Network (Dual Ports)
CN1 - 4-wire Resistive Touch Controller
CN2 - microSD (8 bits)
CN4 - Cell Charger/Battery Supply
CN5 - MiniDin DC Jack
COM1 - UART (Dual Ports)
COM2 - UART (Dual Ports)
GPIO1 - General Purpose IO
H25 - Smart Battery
I2S1 - I2S 1
I2S2 - I2S 2
I2S3 - I2S 3
J1 - SMARC Interface
J3 - TTL LCD
J6 - HDMI1
J8 - LVDS LCD
J9 - Alternate Function Block 1
J10 - I2C
J11 - HDMI2
J12 - External Battery (RTC backup)
J14 - LVDS Control
JACK1 - DC Power In
JP2 - LCD Power Select
JP3 - Select I2C_LCD for J11
JP4 - Battery Charger Enable
JP5 - Cell Charger Present
JP6 - Cell Charger Voltage
JP7 - Cell Protection IC
JP8 - LCD/LVDS Select
JP9 - LCD/LVDS Select
JP10 - LVDS Strobe
JP11 - LVDS Controller
JP12 - LVDS Backlight Control
JP13 - LVDS Panel Control
JP14 - LVDS Backlight Control
JP15 - Select I2C_HDMI for J11
JP16 - Boot Select
JP17 - Boot Select
JP18 - Boot Select
JP19 - Boot Select Recovery
JP20 - VIO Select
JP21 - DC-OUT



LAN1 - Ehternet
LED1 - USB
LED2 - Mini PCIE1
LED3 - Mini PCIE2
LED4 - nLID
LED5 - nSLEEP
LED6 - nBATLOW
LED7 - SATA
LED8 - SD Card (4 bits)
LED9 - USB
LED11 - Cell Protection IC
LED12 - Cell Protection IC
LED13 - Cell Protection IC
LED14 - Cell Protection IC
LED15 - Cell Protection IC
LED16 - Power
MINIPCIE1 - PCIe Mini Card
MINIPCIE2 - PCIe Mini Card
PC1 - TTL Panel Control
PCIE1 - PCI Express
PWM1 - Power Management
PWRON1 - Power On
PWRON2 - Power On
SATA1 - SATA
SD2 - SD Card Slot
SIM1 - SIM Slot
SIM2 - SIM Slot
SPDIF1 - SPDIF OUT
SPI0 - System Packet Interface
SPI1 - System Packet Interface
SW15 - Reset Switch
USBC1 - USB
USB1 - Micro USB
USB2 - USB

NOTE: The larger black pins each represent pin 1

Figure 1-3: Connector Locations (Top Side)

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1.4 Specifications

1.4.1 Physical Specifications

Table 1-3 lists the physical dimensions of the baseboard.

Table 1-3: Weight and Footprint Dimensions

Item	Dimension	
Weight	0.42 kg (0.93 lb)	Overall height is measured from the upper board surface to the top of the highest permanent component on the upper board surface. This measurement does not include the cooling solution, which can vary. The cooling solution will probably increase this dimension.
Height (overall)	33.02 mm (1.30 inches)	
Board thickness	2.03 mm (0.08 inches)	
Width	175.00 mm (6.89 inches)	
Length	330.00 mm (12.99 inches)	

1.4.2 Mechanical Specifications

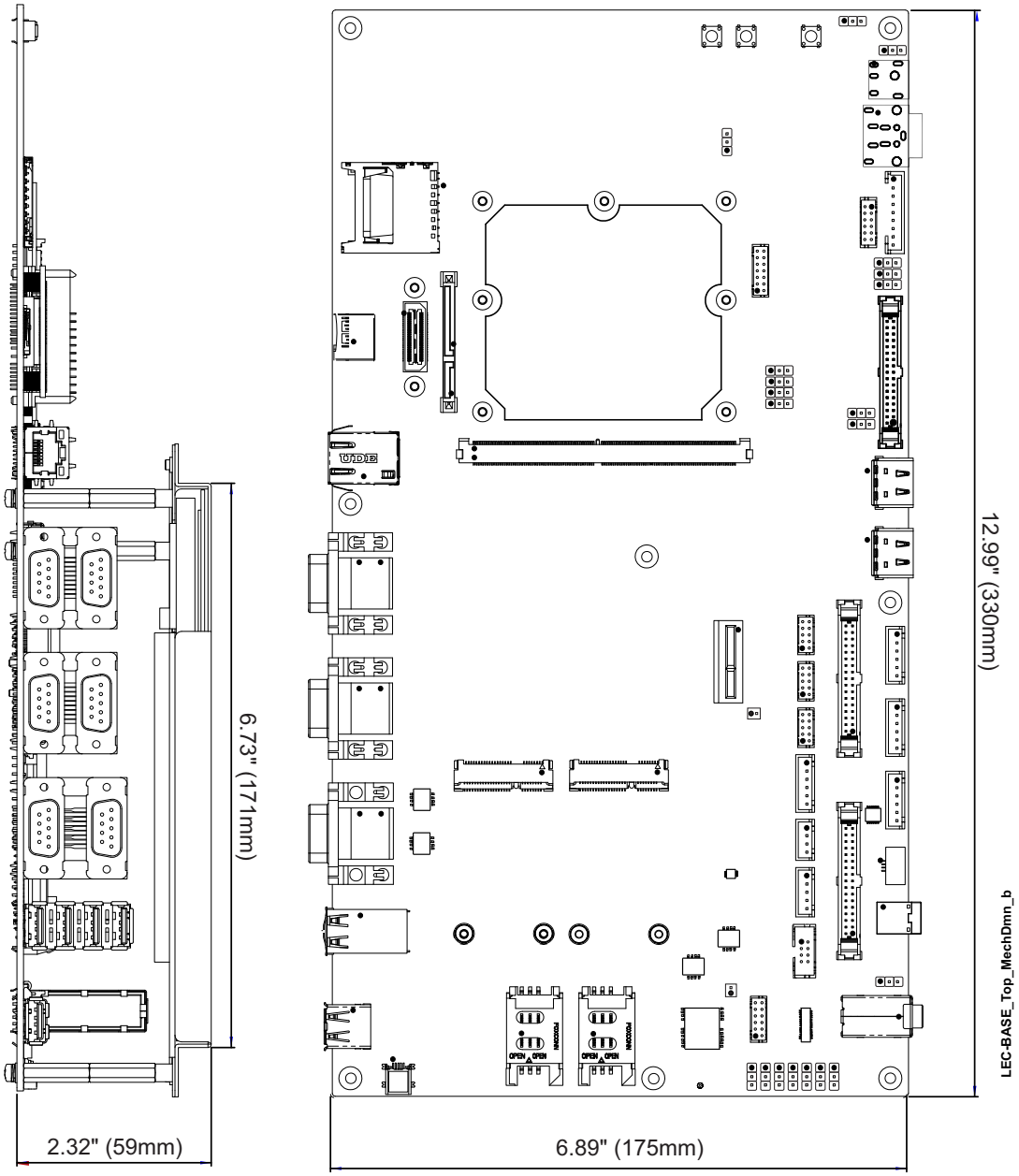


Figure 1-4: Mechanical Dimensions (Top Side)

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2 Interface Signals

This section provides the pin signals for all the non-standard user interfaces on the LEC-BASE. Signal definitions for standard interfaces such as SATA, USB, PCIe, and DB9 serial connectors can be found in their respective specification data sheets.

NOTE: The tables in this section define pin sequence using the method in the following example: A 10-pin header with two rows of pins, using odd/even numbering, where pin 2 is directly across from pin 1, is noted as **10 pins, 2 rows, odd/even pin sequence (1, 2)**.

2.1.1 SD/eMMC (AFB2) Interface

Table 2-4 lists the pin signals of the SD Card ground plane socket, which provides 60-pins, 2 rows, odd/even pin sequence (1, 2) with 0.02" (0.50mm) pitch. These signals are connected to the SD/eMMC interface at pins S26 through S36 of the SMARC connector over a 3.3 volt level shifter.

Table 2-4: SD/eMMC (AFB2) Interface Pin Signals

Pin #	Signal
1	GND
2	GND
3	MMC2_D0_3V
4	GND
5	GND
6	GND
7	GND
8	GND
9	MMC2_D1_3V
10	GND
11	GND
12	GND
13	GND
14	GND
15	MMC2_D2_3V
16	GND
17	GND
18	GND
19	GND
20	GND
21	MMC2_D3_3V
22	VDD_3V3
23	GND
24	GND
25	GND
26	GND
27	MMC2_D4_3V
28	VDD_3V3
29	GND
30	GND
31	GND
32	GND
33	MMC2_D5_3V
34	GND
35	GND

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Table 2-4: SD/eMMC (AFB2) Interface Pin Signals (Continued)

36	GND
37	GND
38	GND
39	MMC2_D6_3V
40	GND
41	GND
42	GND
43	GND
44	GND
45	MMC2_D7_3V
46	GND
47	GND
48	GND
49	GND
50	GND
51	MMC2_CK_3V
52	GND
53	GND
54	GND
55	GND
56	GND
57	MMC2_CMDD_3V
58	GND
59	GND
60	GND

NOTE: The shaded table cells denote power or ground.

2.1.2 Camera 0 (CAM0)

Table 2-5 lists the pin signals of the Camera0 header, which provides 10-pins, 2 rows, odd/even pin sequence (1, 2) with 0.079" (2.00mm) pitch. These signals are connected directly to the MIPI CSI camera interface at the SMARC connector.

Table 2-5:Camera 0 Pin Signals (CAM0)

Pin #	Signal
1	CSI1_CK+
2	CSI1_CK-
3	CSI1_D0+
4	CSI1_D0-
5	CSI1_D1+
6	CSI1_D1-
7	CSI1_D2+
8	CSI1_D2-
9	CSI1_D3+
10	CSI1_D3-

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2.1.3 Camera 1 (CAM1)

Table 2-6 lists the pin signals of the Camera1 header, which provides 10-pins, 2 rows, odd/even pin sequence (1, 2) with 0.079" (2.00mm) pitch. These signals are connected to the camera control signals at the SMARC connector.

Table 2-6: Camera 1 Pin Signals (CAM1)

Pin #	Signal
1	CSI0_CK+
2	CSI0_CK-
3	CSI0_D0+
4	CSI0_D0-
5	CSI0_D1+
6	Not Connected
7	CSI0_D1-
8	Not Connected
9	GND
10	GND

NOTE: The shaded table cells denote ground.

2.1.4 Camera 3 (CAM3)

Table 2-7 lists the pin signals of the Camera 3 header, which provides 10-pins, 2 rows, odd/even pin sequence (1, 2) with 0.079" (2.00mm) pitch. These signals are connected to the camera control signals at the SMARC connector.

Table 2-7: Camera 3 Pin Signals (CAM3)

Pin #	Signal
1	CAM0_nPWR
2	I2C_CAM_CLK_1.8V
3	Not Connected
4	I2C_CAM_DATA_1.8V
5	Not Connected
6	Not Connected
7	CAM0_nRST_3V over the 3.3V level shifter
8	Not Connected
9	5 Volt
10	Not Connected

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2.1.5 Controller Area Network (CAN1)

Table 2-8 and Table 2-9 list the pin signals of the Controller Area Network interface (CAN1A and CAN1B), which provides standard dual DB9 connectors.

Table 2-8: Controller Area Network Signals (CAN1A)

Pin #	Signal
1	Not Connected
2	CAN1_H
3	Not Connected
4	Not Connected
5	GND
6	Not Connected
7	CAN1_L
8	Not Connected
9	5 Volt

NOTE: These pins are connected over the CAN transceiver to the CAN0 SMARC connector interface (pins P143 and P144.)

Table 2-9: Controller Area Network Signals (CAN1B)

Pin #	Signal
1	Not Connected
2	CAN2_H
3	Not Connected
4	Not Connected
5	GND
6	Not Connected
7	CAN2_L
8	Not Connected
9	5 Volt

NOTE: These pins are connected over the CAN transceiver to the CAN1 SMARC connector interface (pins P145 and P146.)

2.1.6 Cell Charger/Battery Supply (CN4)

Table 2-10 lists the pin signals of the Cell Charger/Battery Supply header, which provides 12 pins in 2 rows, odd/even pin sequence (1, 2), and 0.079" (2.00mm) pitch.

Table 2-10: Cell Charger/Battery Supply (CN4)

Pin #	Signal
1	Therm1
2	+VE
3	Cell_4 (positive terminal of); connected to pins 2, 4, 6
4	+VE
5	Cell_3 (positive terminal of)
6	+VE
7	Cell_2 (positive terminal of)
8	-VE
9	Cell_1 (positive terminal of)
10	-VE
11	-VE (negative terminal of); connected to pins 8, 10, 12
12	-VE

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2.1.7 GPIO1

Table 2-11 lists the pin signals of the General Purpose IO header, which provides 12 pins in 2 rows, odd/even pin sequence (1, 2), and 0.079" (2.00mm) pitch. These pins are connected to the SMARC connector over the 3.3 volt level shifter.

Table 2-11: General Purpose IO (GPIO1)

Pin #	Signal
1	GPIO_28_3V (connected to SMARC pin P119)
2	CAM0_nPWREN_3V (connected to SMARC pin P108)
3	GPIO_29_3V (connected to SMARC pin P112)
4	CAM1_nPWREN_3V (connected to SMARC pin P109)
5	GPIO_177_3V (connected to SMARC pin P116)
6	CAM0_nRST_3V (connected to SMARC pin P110)
7	GPIO_54_3V (connected to SMARC pin P117)
8	CAM1_nRST_3V (connected to SMARC pin P111)
9	GPIO_55_3V (connected to SMARC pin P113)
10	CAM_FLD_3V (connected to SMARC pin P115)
11	GPIO_56_3V (connected to SMARC pin P114)
12	GPIO_27_3V (connected to SMARC pin P118)

NOTE: Signal names relative only to the LEC-3517 module.

2.1.8 Smart Battery (H25)

Table 2-12 lists the pin signals of the Smart Battery header, which provides 9 pins in a single row with 0.079" (2.00mm) pitch. These signals are connected to and controlled by the onboard LTC1760 smart battery charger controller.

Table 2-12: Smart Battery (H25)

Pin #	Signal
1	+VE (battery and charging voltage)
2	+VE (battery and charging voltage)
3	+VE (battery and charging voltage)
4	1760_SCL1 (I2C bus from LTC1760 charger controller)
5	1760_SDA1 (I2C bus from LTC1760 charger controller)
6	TH1 (Thermistor Force/Sense connection to LTC1760 charger controller)
7	GND
8	GND
9	GND

NOTE: Shaded table cells denote ground.

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2.1.9 I2S1

Table 2-13 lists the pin signals of the I2S1 header, which provides 6 pins in a single row with 0.098" (2.50mm) pitch. These pins are connected to the SMARC connector over the 3.3 volt level shifter.

Table 2-13: I2S1 Signals (I2S1)

Pin #	Signal
1	VDD_3V3
2	MCBSP1_FSX_3V (connected to SMARC pin S39)
3	MCBSP1_DX_3V (connected to SMARC pin S40)
4	MCBSP1_DR_3V (connected to SMARC pin S41)
5	MCBSP1_CLKX_3V (connected to SMARC pin S42)
6	GND

NOTE: Shaded table cells denote power or ground.

2.1.10 I2S2

Table 2-14 lists the pin signals of the I2S2 header, which provides 6 pins in a single row with 0.098" (2.50mm) pitch. These pins are connected to the SMARC connector over the 3.3 volt level shifter.

Table 2-14: I2S2 Signals (I2S2)

Pin #	Signal
1	VDD_3V3
2	MCBSP2_FSX_3V (connected to SMARC pin S43)
3	MCBSP2_DX_3V (connected to SMARC pin S44)
4	MCBSP2_DR_3V (connected to SMARC pin S45)
5	MCBSP2_CLKX_3V (connected to SMARC pin S46)
6	GND

NOTE: Shaded table cells denote power or ground.

2.1.11 I2S3

Table 2-15 lists the pin signals of the I2S3 header, which provides 6 pins in a single row with 0.098" (2.50mm) pitch. These pins are connected to the SMARC connector over the 3.3 volt level shifter.

Table 2-15: I2S3 Signals (I2S3)

Pin #	Signal
1	VDD_3V3
2	MCBSP3_FSX_3V (connected to SMARC pin S50)
3	MCBSP3_DX_3V (connected to SMARC pin S51)
4	MCBSP3_DR_3V (connected to SMARC pin S52)
5	MCBSP3_CLKX_3V (connected to SMARC pin S53)
6	GND

NOTE: Shaded table cells denote power or ground.

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2.1.12 Alternate Function Block 1 (J9)

Table 2-16 lists the pin signals of the Alternate Function Block 1 header which provides 34-pins, 2 rows, odd/even pin sequence (1, 2) with 0.079" (2.0mm) pitch. These pins are connected dirctly to the SMARC connector.

Table 2-16: Alternate Function Block 1 Interface Pin Signals (J9)

Pin #	Signal
1	VDD_5V
2	VDD_5V
3	AFB0_OUT (connected to SMARC pin S17)
4	GND
5	GND
6	AFB_DIFF0+ (connected to SMARC pin S62)
7	AFB1_OUT (connected to SMARC pin S18)
8	AFB_DIFF0- (connected to SMARC pin S63)
9	AFB2_OUT (connected to SMARC pin S19)
10	GND
11	GND
12	AFB_DIFF1+ (connected to SMARC pin S65)
13	AFB3_IN (connected to SMARC pin S20)
14	AFB_DIFF1- (connected to SMARC pin S66)
15	GND
16	GND
17	AFB4_IN (connected to SMARC pin S21)
18	AFB_DIFF2+ (connected to SMARC pin S68)
19	GND
20	AFB_DIFF2- (connected to SMARC pin S69)
21	AFB5_IN (connected to SMARC pin S22)
22	GND
23	GND
24	AFB_DIFF3+ (connected to SMARC pin S71)
25	AFB6_PTIO (connected to SMARC pin S23)
26	AFB_DIFF3- (connected to SMARC pin S72)
27	AFB7_PTIO (connected to SMARC pin S24)
28	GND
29	GND
30	AFB_DIFF4+ (connected to SMARC pin S74)
31	AFB8_PTIO (connected to SMARC pin S55)
32	AFB_DIFF4- (connected to SMARC pin S75)
33	AFB9_PTIO (connected to SMARC pin S56)
34	GND

NOTE: The shaded table cells denote ground or power.

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2.1.13 I2C (J10)

Table 2-17 lists the pin signals of the I2C header, which provides 2 pins with 0.049" (1.25mm) pitch. These pins are connected to the SMARC connector over the 3.3 volt level shifter.

Table 2-17: I2C Signals (J10)

Pin #	Signal
1	I2C_GP_DAT_3V (connected to SMARC pin S48)
2	I2C_GP_CK_3V (connected to SMARC pin S49)

2.1.14 Battery (J12)

Table 2-18 lists the pin signals of the battery header, which provides 2 pins with 0.049" (1.25mm) pitch.

Table 2-18: Battery Signals (J12)

Pin #	Signal
1	V_RTC
2	GND

NOTE: Shaded table cells denote power or ground.

2.1.15 LVDS Control (J14)

Table 2-19 lists the pin signals of the Smart Battery header, which provides 8 pins in two rows with odd/even pin sequence (1,2) and 0.01" (2.54mm) pitch.

Table 2-19: LVDS Control Signals (J14)

Pin #	Signal
1	GND
2	PNLPWR (display supply voltage, selectable with JP13)
3	LVDS_BKL_CTRL (backlight control, selectable with JP12)
4	GND
5	LCD_nEN (backlight enable)
6	GND
7	Not Connected
8	BLPWR (backlight supply voltage, selectable with JP14)

NOTE: Shaded table cells denote ground.

2.1.16 TTL Panel Control (PC1)

Table 2-20 lists the pin signals of the TTL Panel Control header, which provides 6 pins in a single row with 0.098" (2.50mm) pitch. These pins are connected directly to the display control pins at the SMARC connector.

Table 2-20: LVDS Control Signals (PC1)

Pin #	Signal
1	LCD_DE (connected over the 3.3 volt level shifter)
2	LCD_BKLT_PWM
3	LCD_VDD_EN
4	Not Connected
5	Not Connected
6	LCD_RESET (Active Low)

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2.1.17 Power Management (PW1)

Table 2-21 lists the pin signals of the Power Management header, which provides 14 pins in 2 rows, odd/even pin sequence (1, 2), and 0.079" (2.00mm) pitch. These pins are connected directly to the Power Management pins at the SMARC connector.

Table 2-21: Power Management Signals (PWM1)

Pin #	Signal
1	WDT_TIME
2	VIN_PWR_nBAD
3	nLID
4	nCHARGING
5	nSLEEP
6	CHARGE_nPRSNT
7	nBATLOW
8	CHARGE_nSTBY
9	nTEST
10	CARRIED_PWR_ON
11	Not Connected
12	Not Connected
13	GND
14	GND

NOTE: Shaded table cells denote ground.

2.1.18 SPI0

Table 2-22 lists the pin signals of the System Packet Interface 0 header, which provides 5 pins in a single row with 0.098" (2.50mm) pitch. These pins are connected to the SMARC connector over the 3.3 volt level shifter.

Table 2-22: System Packet Interface 0 Signals (SPI0)

Pin #	Signal
1	SPI2_CLK_3V (connected to SMARC pin P56)
2	SPI2_SOMI_3V (connected to SMARC pin P57)
3	SPI2_SIMO_3V (connected to SMARC pin P58)
4	SPI2_CS0_3V (connected to SMARC pin P54)
5	SPI2_CS1_3V (connected to SMARC pin P55)

NOTE: The signals for this header are defined by the module CPU as “SPI2”, but the header is labelled “SPI0” on the board.

2.1.19 SPI1

Table 2-23 lists the pin signals of the System Packet Interface 1 header, which provides 4 pins in a single row with 0.098" (2.50mm) pitch. These pins are connected to the SMARC connector over the 3.3 volt level shifter.

Table 2-23: System Packet Interface 1 Signals (SPI1)

Pin #	Signal
1	SPI1_CS0_3V (connected to SMARC pin P43)
2	SPI1_CLK_3V (connected to SMARC pin P44)
3	SPI1_SOMI_3V (connected to SMARC pin P45)
4	SPI1_SIMO_3V (connected to SMARC pin P46)

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2.1.20 LVDS

Table 2-24 lists the pin signals of the LVDS header which provides 34-pins, 2 rows, odd/even pin sequence (1, 2) with 0.079" (2.0mm) pitch. These pins are connected directly to the LVDS interface at the SMARC connector.

Table 2-24: LVDS Interface Pin Signals (J8)

Pin #	Signal	Description
1	I2C_LCD_DAT	System Management Data
2	I2C_LCD_CK	System Management Clock
3	PNL_PWR	Panel Power [JP2 (1-2) for 5V, (2-3) for 3.3V]
4	PNL_PWR	Panel Power [JP2 (1-2) for 5V, (2-3) for 3.3V]
5	GND	Ground
6	LVDS_A0N	Data Negative Output
7	LVDS_A0P	Data Positive Output
8	LCD_BLPWM_3V	Backlight PWM(3.3V)
9	LVDS_A1N	Data Negative Output
10	LVDS_A1P	Data Positive Output
11	LVDS_BL_EN	Backlight Enable, if supported
12	LVDS_A2P	Data Positive Output
13	LVDS_A2N	Data Negative Output
14	eDP_HPD	Display Port Control
15	LVDS_CKN	Clock Negative
16	LVDS_CKP	Clock Positive
17	PNL_PWR	Panel Power [JP2 (1-2) for 5V, (2-3) for 3.3V]
18	LVDS_A3P	Data Positive Output
19	LVDS_A3N	Data Negative Output
20	GND	Ground
21	LCD_DUAL_PCK	LCD Dual Display Pixel Clock
22	LCD_BKLTPWM_5V	LCD Backlight Power Management (5V)
23	GND	Ground
24	LCD_BKEN_5V	LCD Backlight Enable (5V)
25	SEL68	Connected over 4.7 KOhm to GND
26	GND	Ground
27	R/L	Connected over 4.7 KOhm to 3.3V
28	NC	Not Connected
29	GND	Ground
30	VDD_3V3	3.3V Supply
31	U/D	Connected over 4.7 KOhm to 3.3V
32	VDD_5V	5V Supply
33	REV	Connected over 4.7 KOhm to 3.3V
34	GND	Ground

NOTE: The shaded table cells denote power or ground.

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2.1.21 TTL

Table 2-25 lists the pin signals of the TTL header which provides 34-pins, 2 rows, odd/even pin sequence (1, 2) with 0.079" (2.0mm) pitch. These pins are connected directly to the LCD interface at the SMARC connector.

Table 2-25: TTL Video Interface Pin/Signal Descriptions (J3)

Pin #	Signal	Description
1	FP0	Flat Panel 0 – data output, Blue0 (24-bit)
2	FP16	Flat Panel 16 – data output, Red0 (24-bit)
3	FP1	Flat Panel 1 – data output, Blue1 (24-bit)
4	FP17	Flat Panel 17 – data output, Red1 (24-bit)
5	FP2	Flat Panel 2 – data output, Blue0 (18-bit); Blue2 (24-bit)
6	FP18	Flat Panel 18 – data output, Red0 (18-bit), Red2 (24-bit)
7	FP3	Flat Panel 3 – data output, Blue1 (18-bit); Blue3 (24-bit)
8	FP19	Flat Panel 19 – data output, Red1 (18-bit), Red3 (24-bit)
9	FP4	Flat Panel 4 – data output, Blue2 (18-bit); Blue4 (24-bit)
10	FP20	Flat Panel 20 – data output, Red2 (18-bit), Red4 (24-bit)
11	FP5	Flat Panel 5 – data output, Blue3 (18-bit); Blue5 (24-bit)
12	FP21	Flat Panel 21 – data output, Red3 (18-bit), Red5 (24-bit)
13	FP6	Flat Panel 6 – data output, Blue4 (18-bit); Blue6 (24-bit)
14	FP22	Flat Panel 22 – data output, Red4 (18-bit), Red6 (24-bit)
15	FP7	Flat Panel 7 – data output, Blue5 (18-bit); Blue7 (24-bit)
16	FP23	Flat Panel 23 – data output, Red5 (18-bit), Red7 (24-bit)
17	FP8	Flat Panel 8 – data output, Green0 (24-bit)
18	VSYNC	Vertical Sync
19	FP9	Flat Panel 9 – data output, Green1 (24-bit)
20	HSYNC	Horizontal Sync
21	FP10	Flat Panel 10 – data output, Green0 (18-bit), Green2 (24-bit)
22	LCD_PCLK	Pixel Clock – This signal provides the clock for transferring digital pixel data
23	FP11	Flat Panel 11 – data output, Green1 (18-bit), Green3 (24-bit)
24	VDD_5V	5 Volt Supply
25	FP12	Flat Panel 12 – data output, Green2 (18-bit), Green4 (24-bit)
26	VDD_5V	5 Volt Supply
27	FP13	Flat Panel 13 – data output, Green3 (18-bit), Green5 (24-bit)
28	VDD_5V	5 Volt Supply
29	FP14	Flat Panel 14 – data output, Green4 (18-bit), Green6 (24-bit)
30	LCD_3V3	3.3 Volt Supply
31	FP15	Flat Panel 15 – data output, Green5 (18-bit), Green7 (24-bit)
32	LCD_3V3	3.3 Volt Supply
33	GND	Ground
34	GND	Ground

NOTE: The shaded table cells denote power or ground.

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Appendix A Technical Support

ADLINK Technology, Inc. provides a number of methods for contacting Technical Support listed in Table A-1 below. Requests for support through Ask an Expert are given the highest priorities, and usually will be addressed within one working day.

- ADLINK Ask an Expert – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the ADLINK web site at http://www.adlinktech.com/AAE/. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online if you wish to use the Ask a Question feature.

ADLINK strongly suggests that you register with the web site. By creating a profile on the ADLINK web site, you will have a portal page called “My ADLINK”, unique to you with access to exclusive services and account information.

- Personal Assistance – You may also request personal assistance by creating an Ask an Expert account and then going to the Ask a Question feature. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request, you must log in to go to the My Question area where you can check status, update your request, and access other features.
- Download Service – This service is also free and available 24 hours a day at http://www.adlinktech.com. For certain downloads such as technical documents and software, you must register online before you can log in to this service.

Table A-1: Technical Support Contact Information

Method	Contact Information
Ask an Expert	http://www.adlinktech.com/AAE/
Web Site	http://www.adlinktech.com
Standard Mail	Contact us should you require any service or assistance. **ADLINK Technology, Inc.** Address: 9F, No.166 Jian Yi Road, Zhonghe District New Taipei City 235, Taiwan 新北市中和區建一路 166 號 9 樓 Tel: +886-2-8226-5877 Fax: +886-2-8226-5717 Email: service@adlinktech.com **Ampro ADLINK Technology, Inc.** Address: 5215 Hellyer Avenue, #110, San Jose, CA 95138, USA Tel: +1-408-360-0200 Toll Free: +1-800-966-5200 (USA only) Fax: +1-408-360-0222 Email: info@adlinktech.com **ADLINK Technology (China) Co., Ltd.** Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203) 300 Fang Chun Rd., Zhangjiang Hi-Tech Park, Pudong New Area, Shanghai, 201203 China Tel: +86-21-5132-8988 Fax: +86-21-5132-3588 Email: market@adlinktech.com

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