LEC-BTS

Technical Reference

Low Energy Computer On Module with
Intel® Atom™ E3800 Series and N2807 Celeron® Processors



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Leading **EDGE COMPUTING**

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Preface

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Revision History

Revision	Date	Description of Change(s)
1.00	Mar/16	Initial Release
2.00	Jul/16	Added Chapter 4, Utilities; updated SMARC signals, in Table 3-2 on page 14; added Electrical Specifications section to Chapter 1
2.1	May/18	Removed heatsink as an option from section 1.4.6

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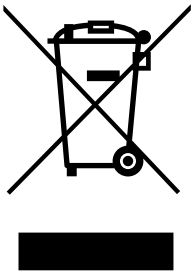
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Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

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Conventions

The following conventions may be used throughout this manual, denoting special levels of information.



This information adds clarity or specifics to text and illustrations.



This information indicates the possibility of ***minor*** physical injury, component damage, data loss, and/or program corruption.



This information warns of possible ***serious*** physical injury, component damage, data loss, and/or program corruption.

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Important Safety Instructions

For user safety, please read and follow all **Instructions**, **WARNINGs**, **CAUTIONs,** and **NOTEs** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

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1 Overview

This manual presents a general overview of the LEC-BTS. After reviewing this document you should understand the following perspectives of the LEC-BTS.

- Feature Overview
- Hardware Functions
- Interface Signal Definitions
- Utility Definitions
- Contact Information

NOTE: Refer to http://www.sget.org/standards/smarc.html for SMARC specifications. Please refer to BSP readme documents in the Quick Drive for BSP installation instructions.

1.1 Block Diagram

Figure 1-1 represents the component functions of the module.

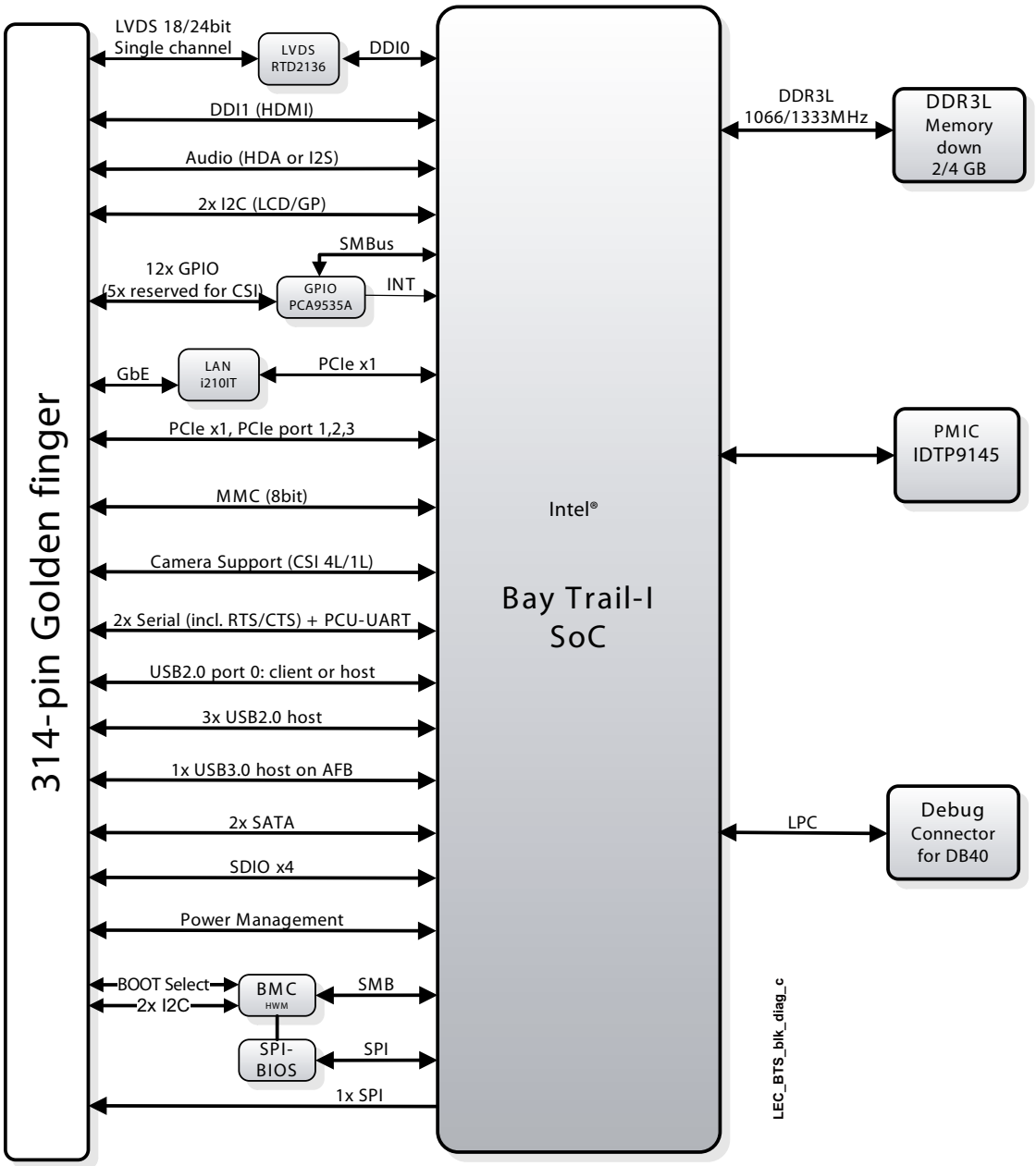


Figure 1-1: Functional Block Diagram

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1.2 Major Components (ICs)

Table 1-1 lists the major integrated circuits on the LEC-BTS, including a brief description of each IC. Figures 1-2 and 1-3 show the locations of the major ICs.

Table 1-1: Major Integrated Circuit Descriptions and Functions

Chip Type	Mfg.	Model	Description	Function
CPU (U1)	Intel	• E3805 (dual core, 3W, headless, 1.33GHz) • E3815 (single core, 5W, 1.46GHz) • E3826 (dual core, 7W, 1.46GHz) • E3845 (quad core, 10W, 1.91GHz) • N2807 (dual core, 4.3W, 1.58Ghz)	Atom, 22nm SoC (System on Chip) with Intel 64 Architecture Celeron, 22nm SoC (System on Chip) with Intel 64 Architecture	Integrates Processor Core, Graphics and Memory Controller Hub, and I/O Hub
Ethernet Controller (U9 [bottom])	Intel	WGI210IT SLIXT	Single-port Gigabit Ethernet controller	Integrates GbE MAC, PHY, and SGMII/SerDes to enable 10T/100TX/1000T Ethernet signals using the PCIe x1 bus
DDR3L SDRAM (U24 [bottom], U25, U26 [top], U27 [bottom])	Micron	MT41K256M16HA-125	On-board DDR3L, 1.35V, 4Gb, 32Mx16x8, non-ECC, un-buffered System Memory	Provides high-speed data transfer

Key:
U1 - CPU
U25 - DDR3L SDRAM
U26 - DDR3L SDRAM

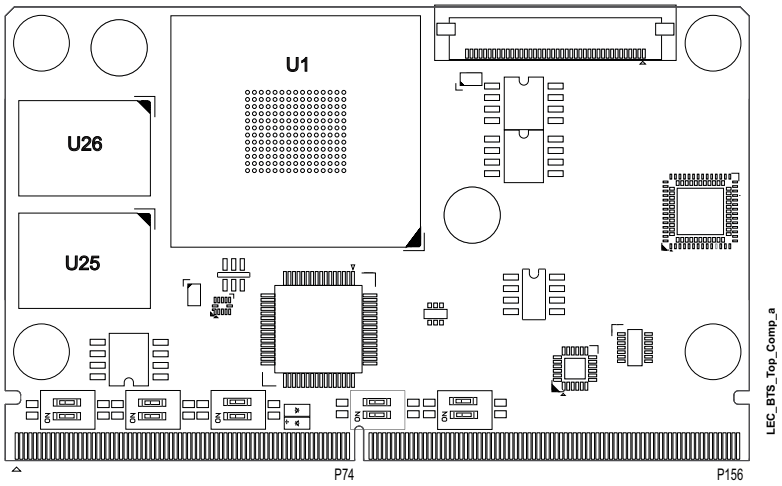


Figure 1-2: Component Locations (Top Side)

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Key:
U9 - GbE Controller
U24 - DDR3L SDRAM
U27 - DDR3L SDRAM

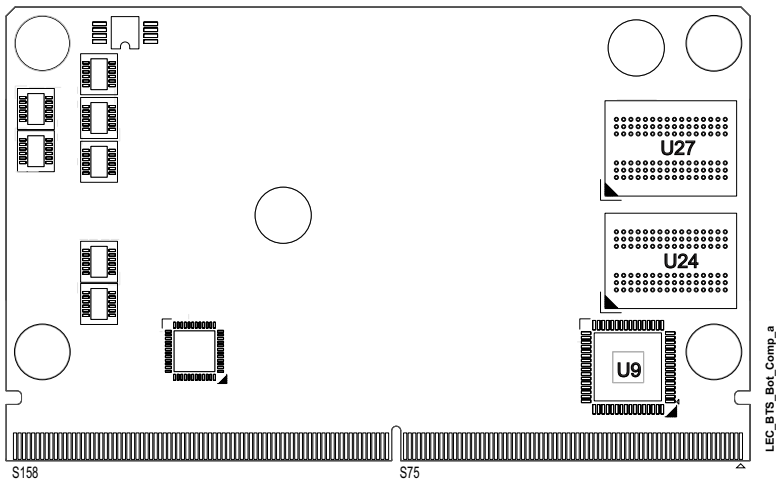
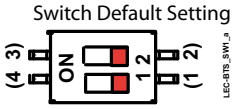
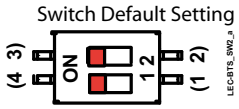
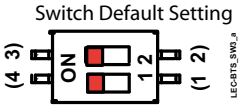


Figure 1-3: Component Locations (Bottom Side)

1.3 Connectors, Switches, and LEDs

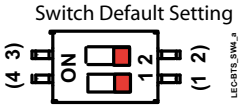
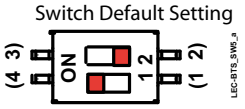
Table 1-2 describes the connectors, switches, and LEDs shown in Figure 1-4.

Table 1-2: Module Connector Description

Reference	Board Access	Description
GF1 – SMARC P-S	Top/Bottom	314-pin, MXM edge connector for routing camera, graphics, and I/O signals from the module to the baseboard.
CN1	Top	40-pin, DB40 connector for debug card
SW1	Top	4-pin dip switch for selecting CSI1 camera, 4L, Data1 configuration [default=off] 
SW2	Top	4-pin dip switch for selecting CSI1 camera, 4L, Data2 configuration [default=on] 
SW3	Top	4-pin dip switch for selecting CSI1 camera, 4L, Data3 configuration [default=on] 

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Table 1-2: Module Connector Description (Continued)

Reference	Board Access	Description
SW1, SW2, SW3 Configurations: • Camera with 1 MIPI-CSI lane = SW1-SW3 switches all set to ON • Camera with 2 MIPI-CSI lanes = SW1 (both OFF); SW2 (both ON); SW3 (both ON) • Camera with 3 MIPI-CSI lanes = SW1 (both OFF); SW2 (both OFF); SW3 (both ON) • Camera with 4 MIPI-CSI lanes = SW1-SW3 switches all set to OFF		
SW4	Top	4-pin dip switch for selecting LVDS color depth (18bit or 24bit) and loading BIOS setup defaults at Boot Up: 1 = LVDS 18bit [default] 4 = LVDS 24bit 2 = BIOS setup defaults off [default] 3 = BIOS setup defaults on 
SW5	Top	4-pin dip switch for BIOS_SELECT: 1 = BIOS 2 [blue LED blinks fast] 4 = BIOS 1 and WDT Disable [default] 2 = BMC switches to BIOS 2 when BIOS 1 not detected [default] 3 = Disables BIOS Detection Watchdog 
LED1	Top	Blue LED indicating system status activities for HW Reset, SW Reset, Power Up, Power Down, Reset Button, and Power Button
LED2	Top	Green LED for Power On
LED3	Top	Red LED for Watchdog Activity

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Key:
CN1 - DB40 Bebug
GF1 - SMARC
LED1 - System Status
LED2 - Power ON
SW1 - CSI 1 Camera
SW2 - CSI 2 Camera
SW3 - CSI 3 Camera
SW4 - BIOS Defaults
SW5 - BIOS1-2 Select

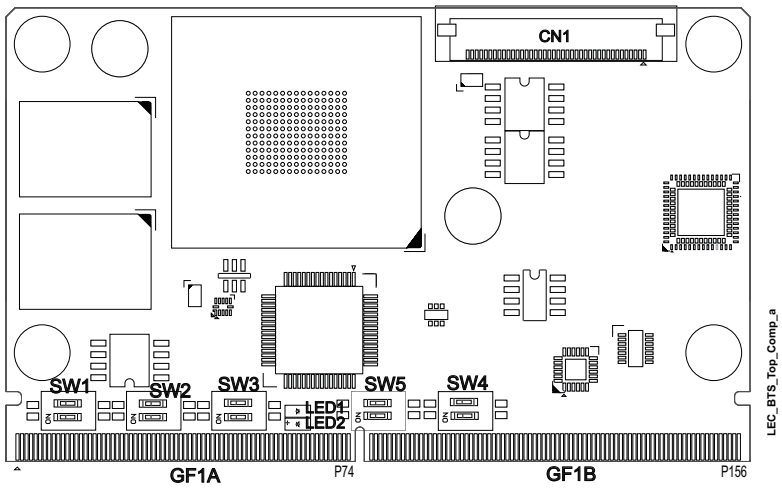


Figure 1-4: Connector Locations (Top Side)

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1.4 Specifications

1.4.1 Physical Specifications

Table 1-3 lists the physical dimensions of the module.

Table 1-3: Weight and Footprint Dimensions

Item	Dimension	
Weight	0.02 kg (0.05 lb)	Overall height is measured from the upper board surface to the top of the highest permanent component (CN1 connector) on the upper board surface. This measurement does not include the cooling solution, which can vary. The cooling solution will probably increase this dimension.
Height (overall)	2.50 mm (0.098 inches)	
Board thickness	1.27 mm (0.05 inches)	
Width	50.00 mm (1.97 inches)	
Length	82.00 mm (3.23 inches)	

1.4.2 Mechanical Specifications

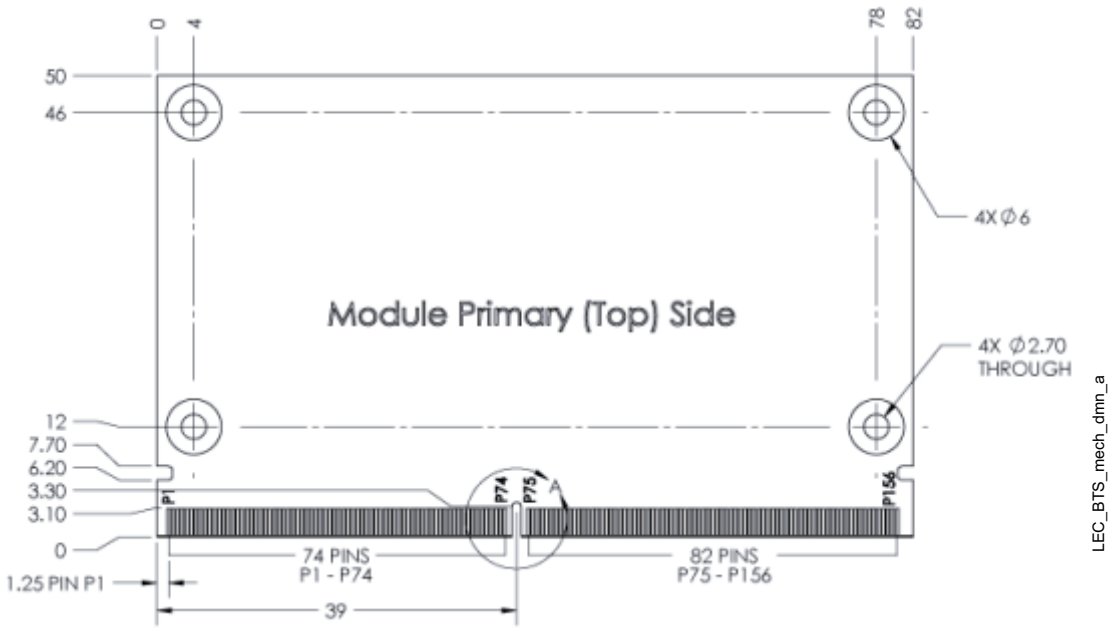


Figure 1-5: Mechanical Dimensions (Top Side)

NOTE: All dimensions are given in millimeters.

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1.4.3 Electrical Specifications

Table 1-4 specifies the electrical characteristics of the module.

Table 1-4: Electrical Specifications

Parameter	Value
Voltage Input	
Standard	▶ Fixed 5-Volt Supply (+4.75V DC min to +5.25V DC max)
RTC	▶ 3.0V, 2.0V to 3.3V (battery)
Power States	▶ C1-C6 processor power states ▶ S0 (active), S1 (sleep), S3 (save to RAM), S4 (suspend-to-disk), S5 (soft-off and wake-on-LAN), and S5 ECO (wake on USB S3/S4, WOL S3/S4/S5) system power states

1.4.4 Power Specifications

Table 1-5 provides the power requirements for this module.

Table 1-5: Power Supply Requirements

Parameter	E3815 (5W) Characteristics	E3826 (7W) Characteristics	E3845 (10W) Characteristics
Input Type	Regulated DC voltage	Regulated DC voltage	Regulated DC voltage
In-rush Voltage & Current	0.55A (2.75W) @ 5V	0.65A (3.25W) @ 5V	0.85A (4.25W) @ 5V
Typical Idle Voltage & Current	0.66A (3.30W) @ 5V	0.65A (3.25W) @ 5V	0.77A (3.85W) @ 5V
BIT* Voltage & Current	1.18A (5.90W) @ 5V	1.60A (8.00W) @ 5V	2.52A (12.60W) @ 5V

Operating configurations:

- ▶ In-rush operating configuration - Typical under Windows 8.1
- ▶ Idle operating configuration - Typical under Windows 8.1
- ▶ Intel TAT (Thermal Analysis Tool) operating configuration - Typical under Windows 8.1

1.4.5 Environmental Specifications

Table 1-6 provides the most efficient operating and storage condition ranges required for this module.

Table 1-6: Environmental Requirements

Parameter	Conditions
Temperature	
Standard	0° to +60° C (+32° to +140° F)
Extended	–40° to +85° C (–40° to +185° F)
Storage	–55° to +85° C (–67° to +185° F)
Humidity	
Operating	5% to 90% relative humidity, non-condensing
Non-operating	5% to 95% relative humidity, non-condensing

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1.4.6 Thermal/Cooling Requirements

The LEC-BTS is designed to operate at its maximum CPU speeds and requires a thermal solution to cool the SoC. ADLINK offers a heat spreader (separate order number) for cooling. This facilitates future module upgrades without the need to re-design the custom heatsink.



The optional heat spreader plate requires another form of cooling, such as a fan. A heat spreader plate is not a complete thermal solution for the LEC-BTS.

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2 Hardware

2.1 CPU

The LEC-BTS product family offers three versions of the Intel Atom E3800 Series CPU: the E3805 (dual core), the E3815 (Single Core), the E3826 (Dual Core), the E3845 (Quad Core), and the N2807 (Celeron Dual Core). E3800 CPUs feature the Intel 64 Architecture and are manufactured based on Intel's 22-nanometer technology. Refer to the CPU data sheet at the Intel web site.

2.2 Memory

The LEC-BTS employs one channel of 64-bit DDR3L on-board memory. Four SDRAM memory chips provide up to 16Gb of low voltage non-ECC, unbuffered system memory. Refer to the SDRAM data sheet at the Micron web site.

2.3 I210 LAN Controller

The Intel I210 provides a single-port controller that supports GbE functionality using the high-speed PCIe standard, v2.1 (2.5GT/s). The I210 features an integrated PHY, which enables 1000BASE-T implementations such as rack-mounted or pedestal servers in add-on NIC or LAN-on-Motherboard (LOM) designs. Other implementations include blade servers such as LOMs or mezzanine cards as well as embedded applications such as switch add-on cards and network appliances. Refer to the Intel I210 Ethernet Controller data sheet at the Intel web site.

2.4 SMBus Slave Addresses

Figure 2-1 lists the corresponding slave addresses of the devices on the SMBus

Table 2-1: SMBus Slave Addresses

Address (HEX)	Function	Device
(40)	GPIO	PCA9535A
(50)	BMC/SEMA	BMC
(6A)	DP to LVDS	RTD2136R
(A0)	DDR3L channel A	DDR3L memory
(92)	Thermal Sensor	LM73

2.5 Getting Started

Mount the LEC-BTS to the carrier as illustrated in Figure 2-1, which provides a profile view of the module mounted to the carrier with dimensions.

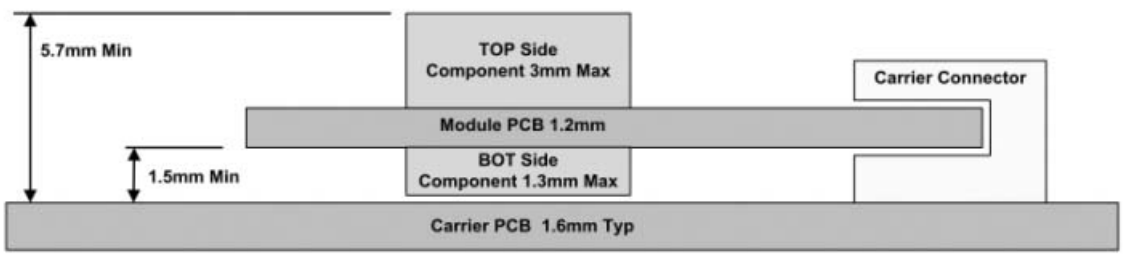


Figure 2-1: SMARC module mounting dimensions (profile)

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ADLINK strongly recommends plastic spacers instead of metal spacers for mounting the board. Metal spacers create the possibilities of short circuits with the components located around the mounting holes, which can ruin the board.



Be sure to observe the EMC security measures. Make sure you are always at the same potential as the module.



Never connect or disconnect peripherals like HDDs while the power supply is connected and switched on.

Connect a USB keyboard or mouse to the carrier. Use the SATA cable to connect a hard disk. Make sure that the pins match their counterparts correctly and are not twisted. If you plan to use additional peripherals, connect them to the appropriate headers or connectors on the carrier.

Connect a power supply to the power connector on the carrier and switch on the power.



Observe the minimum voltage values for the standard peripherals mentioned. For additional peripherals, make sure enough power is available. The system will not work if there is not enough supply current for all your devices.

The display shows the BIOS messages. If you want to change the standard BIOS settings, press the <DEL> key to enter the BIOS setup menus. See Chapter 4 for setup details.

If you need to load the BIOS default values, they can be automatically loaded at boot time.

The LEC-BTS boots from CD drives, USB sticks, hard disks, or µSD-Cards. Provided that any of these is connected and contains a valid operating system image, the display then shows the boot screen of your operating system.

The LEC-BTS needs adequate cooling measures depending on the desired operating temperature range. Using the board without cooling could permanently damage the board.

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3 Interfaces

This section provides descriptions of the interfaces and signals within the SMARC P-S (Primary-Secondary) connector. Refer to the SMARC specification at: http://www.sget.org/standards/smarc.html for definitions of the SMARC interfaces. The SMARC P-S (Primary-Secondary) connector provides the following interfaces:

- LVDS
- HDMI
- Camera CSIO
- Audio
- PCIe
- Gb Ethernet
- USB 2.0
- USB 3.0
- SATA
- I2C
- SPI
- Serial
- I2S
- SD/SDIO
- eMMC
- GPIO
- SMARC
- Debug



ADLINK Technology Inc. only supports the features/ options tested and listed in this manual. The main chips used in the LEC-BTS may provide more features or options than are listed for the LEC-BTS, but some of these features or options are not supported on the module and will not function as specified in the chip documentation.

3.1 18/24 Bit LVDS LCD

The LVDS interface is connected to the DDI0 interface of the SoC, while the translation is made by a DisplayPort™-to-LVDS converter. (Refer to the Realtek RTD2136R-CG, DisplayPort-to-LVDS converter datasheet.)



The LEC-BTS supports single-channel LVDS. Backlight Enable, Display Enable, and PWMOUT are controlled from the BIOS setup.

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3.2 HDMI (High-Definition Multimedia Interface)

The default setup defines the DDI1 port as HDMI and provides the following signals:

- 1 Clock pair
- 3 Data pairs
- Service signals

The HDMI interface is compliant with the HDMI 1.4 specification.

3.3 Camera CSI

The LEC-BTS brings out signals for two MIPI-CSI 2.0 (serial) camera interfaces, the first with clock and one data lane, the second with clock and up to four data lanes supporting up to 800 Mbit/s of actual pixels.

3.4 Audio (HDA)

The SoC provides an HDA controller, which communicates with internal or external CODECs over the Intel HDA serial link. HDA signals are brought out through the I2S2 pins on the SMARC connector and are multiplexed with LPE_I2S audio signals. When HDA is active, LPE audio is disabled.

3.5 PCI Express (PCIe)

The CPU features four PCIe x1 ports, and the LEC-BTS module uses three of them for the PCIe interface and one of them for the Gigabit Ethernet interface. The PCIe interface supports the PCIe Base Specification 2.0 with a maximum signal rate of 5 GT/s and can be configured to support PCIe edge cards or Express Cards.

3.6 Gigabit Ethernet

The on-board Intel I210IT Ethernet controller uses PCIe x1 (v2.1) bus signals from the CPU to enable 10T/100TX/1000T operation through integrated MAC, PHY, and SGMII/SerDes interfaces.

3.7 USB Ports

The USB interface originates from two host controllers on the SoC that provide four USB 2.0 ports and one USB 3.0 port.

3.7.1 USB2.0

Three of the four USB 2.0 ports use the USB 0-2 pins on the SMARC connector. The fourth USB 2.0 port is routed through the AFB-DIFF2 pins on the SMARC connector, which map to the USB_DP/N [0] pins on the SoC.

3.7.2 USB 3.0

The USB 3.0 port uses the AFB_DIFF 0-1 pins on the SMARC connector, which map to the USB3_TX/RX pins on the SoC. See Table 3-2.

3.8 SATA

The SATA interface provides one port through the SATA0 pins on the SMARC connector. The interface supports 1.5Gb/s and 3.0Gb/s. The LEC-BTS supports a second SATA port through the AFB Diff 3 and AFB Diff 4 signals on the SMARC connector (pins S71-S72 and S74-S75.)

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3.9 I2C Bus

The LEC-BTS provides four interfaces through the I2C bus for General Purpose, Power Management, Camera, and LCD video I2C signals with operating speeds up to 400kHz. All I2C interfaces have 1.8V pull ups with 2.2k resistors.

3.10 SPI

The CPU implements an SPI controller, which supports two SPI Flash devices on the module for BIOS storage.

3.11 Serial (UART)

The LEC-BTS provides two serial interfaces: One port is a high-speed, 4-wire port (with TX/RX and RTS#/CTS#), and one port is 2-wire (with TX/RX only.)

3.12 I2S

The SMARC connector provides three pins for an LPE_I2S audio interface. The LPE_I2S interface is brought out through the I2S0 pins on the SMARC connector.

3.13 SD/SDIO Interface

Four parallel data lines comprise the SD/SDIO interface, supporting SD Card sockets.

3.14 eMMC Interface

The LEC-BTS provides one 8-bit eMMC interface port, brought out from the CPU through the SDMMC pins on the SMARC connector.

3.15 GPIO

The LEC-BTS provides 12 GPIO signals from the CMOS device on the module. The GPIO signals can be utilized for General Purpose IOs as well as camera, HDA, PWM, TACH, and CAN interfaces.

Table 3-1: GPIO Default Settings

SMARC Connector Pin	Default Function
GPIO0	CAM0_PWR#
GPIO1	CAM1_PWR#
GPIO2	CAM0_RST#
GPIO3	CAM1_RST#
GPIO4	HDA_RST#
GPIO5	GPIO
GPIO6	GPIO
GPIO7	GPIO
GPIO8	GPIO
GPIO9	GPIO
GPIO10	GPIO
GPIO11	GPIO

3.16 LPC Debug

A 40-pin, front flip, DB40 connector allows access to debug and update the BIOS, BMC, and OS code on the module. (Refer to “Debug (DB40)” on page 22.)

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3.17 SMARC Interface Signals

Table 3-2 provides the pin signals for the SMARC P-S connector. Refer to the SMARC specification at http://www.sget.org/standards/smarc.html for definitions of the SMARC signals.

Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions

Pin #	Primary (Top Side)	Pin #	Secondary (Bottom Side)
		S1	Not connected
P1	Not connected	S2	Not connected
P2	GND	S3	GND
P3	CSI1_CK+ (CSI1 differential clock inputs.)	S4	Not connected
P4	CSI1_CK- (CSI1 differential clock inputs.)	S5	I2C_CAM_CK (Serial / Parallel camera support link - I2C clock)
P5	Not connected	S6	CAM_MCK
P6	Not connected	S7	I2C_CAM_DAT (Serial / Parallel camera support link - I2C data)
P7	CSI1_D0+ (CSI1 differential data inputs.)	S8	CSI0_CK+ (CSI0 differential clock inputs.)
P8	CSI1_D0- (CSI1 differential data inputs.)	S9	CSI0_CK- (CSI0 differential clock inputs.)
P9	GND	S10	GND
P10	CSI1_D1+ (CSI1 differential data inputs.)	S11	CSI0_D0+ (CSI0 differential data inputs.)
P11	CSI1_D1- (CSI1 differential data inputs.)	S12	CSI0_D0- (CSI0 differential data inputs.)
P12	GND	S13	GND
P13	CSI1_D2+ (CSI1 differential data inputs.)	S14	Not connected
P14	CSI1_D2- (CSI1 differential data inputs.)	S15	Not connected
P15	GND	S16	GND
P16	CSI1_D3+ (CSI1 differential data inputs.)	S17	AFB0_OUT (General purpose AFB output; maps to PMC_SLP_S3# on the SOC)
P17	CSI1_D3- (CSI1 differential data inputs.)	S18	AFB1_OUT (General purpose AFB output; maps to PMC_SLP_S4# on the SOC)
P18	GND	S19	AFB2_OUT (General purpose AFB output; maps to PMC_SUS_STAT# on the SOC)
P19	GBE_MDI3- (Bi-directional transmit/ receive pair 3 to magnetics [Media Dependent Interface])	S20	Not connected
P20	GBE_MDI3+(Bi-directional transmit/ receive pair 3 to magnetics [Media Dependent Interface])	S21	Not connected
P21	GBE_LINK100# (Link Speed Indication LED for 100Mbps; able to sink 24mA or more carrier LED current)	S22	Not connected
P22	GBE_LINK1000# (Link Speed Indication LED for 1000Mbps; able to sink 24mA or more carrier LED current)	S23	AFB6_PTIO (EN_OC# for USB SS)
P23	GBE_MDI2- (Bi-directional transmit/ receive pair 2 to magnetics [Media Dependent Interface])	S24	AFB7_PTIO (PCU_SMB_ALERT#)
P24	GBE_MDI2+ (Bi-directional transmit/ receive pair 2 to magnetics [Media Dependent Interface])	S25	GND

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Primary (Top Side)	Pin #	Secondary (Bottom Side)
P25	GBE_LINK_ACT# (Link / Activity Indication LED Driven low on Link [10, 100 or 1000 mbps] Blinks on Activity; able to sink 24mA or more Carrier LED current)	S26	SDMMC_D0 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P26	GBE_MDI1- (Bi-directional transmit/ receive pair 1 to magnetics [Media Dependent Interface])	S27	SDMMC_D1 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P27	GBE_MDI1+ (Bi-directional transmit/ receive pair 1 to magnetics [Media Dependent Interface])	S28	SDMMC_D2 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P28	GBE_CTREF(Center-Tap reference voltage for GBE0 Carrier board Ethernet magnetic [if required by the Module GBE PHY])	S29	SDMMC_D3 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P29	GBE0_MDI0- (Bi-directional transmit/ receive pair 0 to magnetics [Media Dependent Interface])	S30	SDMMC_D4 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P30	GBE0_MDI0+ (Bi-directional transmit/ receive pair 0 to magnetics [Media Dependent Interface])	S31	SDMMC_D5 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P31	Not connected	S32	SDMMC_D6 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P32	GND	S33	SDMMC_D7 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P33	SDIO_WP (SDIO card Write Protect; 10K pull-up to 3.3V)	S34	GND
P34	SDIO_CMD (SDIO card Command line)	S35	SDMMC_CK (clock)
P35	SDIO_CD# (SDIO Card Detect; 10K pull-up to 3.3V)	S36	SDMMC_CMD (command line)
P36	SDIO_CK (SDIO card Clock)	S37	SDMMC_RST# (Reset signal to eMMC device)
P37	SDIO_PWR_EN (SDIO card Power Enable)	S38	Not connected
P38	GND	S39	I2S0_LRCK (Left & Right audio synchronization clock)
P39	SDIO_D0 (SDIO card 4-bit data path)	S40	I2S0_SDOUT (Digital audio output)
P40	SDIO_D1 (SDIO card 4-bit data path)	S41	I2S0_SDIN (Digital audio input)
P41	SDIO_D2 (SDIO card 4-bit data path)	S42	I2S0_CK (Digital audio clock)
P42	SDIO_D3 (SDIO card 4-bit data path)	S43	Not connected
P43	Not connected	S44	Not connected
P44	Not connected	S45	Not connected
P45	Not connected	S46	Not connected
P46	Not connected	S47	GND
P47	GND	S48	I2C_GP_CK (I2C General Purpose clock signal)
P48	SATA0_TX+ (Differential SATA 0 transmit data Pair; 0.1 uF 0402 capacitor on module)	S49	I2C_GP_DAT I2C (General Purpose data signal)

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Primary (Top Side)	Pin #	Secondary (Bottom Side)
P49	SATA0_TX- (Differential SATA 0 transmit data Pair; 0.1 uF 0402 capacitor on module)	S50	I2S2_LRCK (Left & Right audio synchronization clock)
P50	GND	S51	I2S2_SDOUT (Digital audio output)
P51	SATA0_RX+ (Differential SATA 0 receive data Pair; 0.1 uF 0402 capacitor on module)	S52	I2S2_SDIN (Digital audio input)
P52	SATA0_RX- (Differential SATA 0 receive data Pair; 0.1 uF 0402 capacitor on module)	S53	I2S2_CK (Digital audio clock)
P53	GND	S54	SATA_ACT# (Active low SATA activity indicator If implemented, able to sink 24mA or more Carrier LED current)
P54	SPI1_CS0# (SPI1 Master Chip Select 0 output)	S55	Not connected
P55	Not connected	S56	Not connected
P56	SPI1_CK (SPI1 Master Clock output)	S57	Not connected
P57	SPI1_DIN (SPI1 Master Data input [input to CPU, output from SPI device])	S58	Not connected
P58	SPI1_DO (SPI1 Master Data output [output from CPU, input to SPI device])	S59	Not connected
P59	GND	S60	Not connected
P60	USB0+ (Differential USB0 data pair)	S61	GND
P61	USB0- (Differential USB0 data pair)	S62	AFB_DIFF0+ (maps to USB3_TX_P on the SOC)
P62	USB0_EN_OC# (Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up is present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.12.4 of *SMARC Specification.*)	S63	AFB_DIFF0- (maps to USB3_TX_N on the SOC)
P63	USB0_VBUS_DET (USB host power detection when this port is used as a device)	S64	GND
P64	USB0_OTG_ID (USB OTG ID input, active high)	S65	AFB_DIFF1+ (maps to USB3_RX_P on the SOC)
P65	USB1+ (Differential USB1 data pair)	S66	AFB_DIFF1- (maps to USB3_RX_N on the SOC)
P66	USB1- (Differential USB1 data pair)	S67	GND
P67	USB1_EN_OC# (Pulled low by Module OD driver to disable USB1 power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up is present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.12.4 of *SMARC Specification.*)	S68	AFB_DIFF2+ (maps to USB_D0_P on the SOC)
P68	GND	S69	AFB_DIFF2- (maps to USB_D0_N on the SOC)

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Primary (Top Side)	Pin #	Secondary (Bottom Side)
P69	USB2+ (Differential USB2 data pair)	S70	GND
P70	USB2- (Differential USB2 data pair)	S71	AFB_DIFF3+ (maps to SATA_TX1_P on the SOC)
P71	USB2_EN_OC# (Pulled low by Module OD driver to disable USB2 power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up ***shall*** be present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.12.4 of *SMARC Specification*.)	S72	AFB_DIFF3- (maps to SATA_TX1_N on the SOC)
P72	PCIE_C_PRSNT# (PCIe Port C present input. Pulled up or terminated on Module)	S73	GND
P73	PCIE_B_PRSNT# (PCIe Port B present input. Pulled up or terminated on Module)	S74	AFB_DIFF4+ (maps to SATA_RX1_P on the SOC)
P74	PCIE_A_PRSNT# (PCIe Port A present input. Pulled up or terminated on Module)	S75	AFB_DIFF4- (maps to SATA_RX1_N on the SOC)
	Key		Key
P75	PCIE_A_RST# (PCIe Port A reset output)	S76	PCIE_B_RST# (PCIe Port B reset output, active low)
P76	PCIE_C_CKREQ# (PCIe Port C clock request input. Pulled up or terminated on Module)	S77	PCIE_C_RST# (PCIe Port A reset output, active low)
P77	PCIE_B_CKREQ# (PCIe Port B clock request input. Pulled up or terminated on Module)	S78	PCIE_C_RX+ (Differential PCIe Link C receive data pair 0. No coupling caps on Module)
P78	PCIE_A_CKREQ# (PCIe Port A clock request input. Pulled up or terminated on Module)	S79	PCIE_C_RX- (Differential PCIe Link C receive data pair 0. No coupling caps on Module)
P79	GND	S80	GND
P80	PCIE_C_REFCK+ (Differential PCIe Link C reference clock output. DC coupled)	S81	PCIE_C_TX+ (Differential PCIe Link C transmit data pair 0. Series coupling caps are on the Module. Caps are 0402 package 0.1uF)
P81	PCIE_C_REFCK- (Differential PCIe Link C reference clock output. DC coupled)	S82	PCIE_C_TX- (Differential PCIe Link C transmit data pair 0. Series coupling caps are on the Module. Caps are 0402 package 0.1uF)
P82	GND	S83	GND
P83	PCIE_A_REFCK+ (Differential PCIe Link A reference clock output. DC coupled)	S84	PCIE_B_REFCK+ (Differential PCIe Link B reference clock output; DC coupled)
P84	PCIE_A_REFCK- (Differential PCIe Link A reference clock output. DC coupled)	S85	PCIE_B_REFCK- (Differential PCIe Link B reference clock output; DC coupled)
P85	GND	S86	GND
P86	PCIE_A_RX+ (Differential PCIe Link A receive data pair 0. No coupling caps on Module)	S87	PCIE_B_RX+ (Differential PCIe Link B receive data pair 0. No coupling caps on Module)
P87	PCIE_A_RX- (Differential PCIe Link A receive data pair 0. No coupling caps on Module)	S88	PCIE_B_RX- (Differential PCIe Link B receive data pair 0. No coupling caps on Module)
P88	GND	S89	GND

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Primary (Top Side)	Pin #	Secondary (Bottom Side)
P89	PCIE_A_TX+ (Differential PCIe Link A transmit data pair 0. Series coupling capacitors are on the Module. 0.1 uF 0402 capacitor are on module)	S90	PCIE_B_TX+ (Differential PCIe Link B transmit data pair 0. Series coupling caps are on the Module Caps are 0402 package 0.1uF)
P90	PCIE_A_TX- (Differential PCIe Link A transmit data pair 0. Series coupling capacitors are on the Module. 0.1 uF 0402 capacitor are on module)	P91	PCIE_B_TX- (Differential PCIe Link B transmit data pair 0. Series coupling caps are on the Module Caps are 0402 package 0.1uF)
P91	GND	S92	GND
P92	HDMI_D2+ (TMDS / HDMI data 2 differential pair)	S93	Not connected
P93	HDMI_D2- (TMDS / HDMI data 2 differential pair)	S94	Not connected
P94	GND	S95	Not connected
P95	HDMI_D1+ (TMDS / HDMI data 1 differential pair)	S96	Not connected
P96	HDMI_D1- (TMDS / HDMI data 1 differential pair)	S97	Not connected
P97	GND	S98	Not connected
P98	HDMI_D0+ (TMDS / HDMI data 0 differential pair)	S99	Not connected
P99	HDMI_D0- (TMDS / HDMI data 0 differential pair)	S100	Not connected
P100	GND	S101	GND
P101	HDMI_CK+ (TMDS / HDMI clock output differential pair)	S102	Not connected
P102	HDMI_CK- (TMDS / HDMI clock output differential pair)	S103	Not connected
P103	GND	S104	Not connected
P104	HDMI_HPD (HDMI Hot Plug Detect input)	S105	Not connected
P105	HDMI_CTRL_CK (I2C clock line dedicated to HDMI)	S106	Not connected
P106	HDMI_CTRL_DAT (I2C data line dedicated to HDMI)	S107	Not connected
P107	HDMI_CEC (HDMI Consumer Electronics Control, 1 – wire peripheral control interface)	S108	Not connected
P108	GPIO0 / CAM0_PWR# [default] (Camera 0 Power Enable, active low output)	S109	Not connected
P109	GPIO1 / CAM1_PWR# [default] (Camera 1 Power Enable, active low output)	S110	GND
P110	GPIO2 / CAM0_RST# [default] (Camera 0 Reset, active low output)	S111	Not connected
P111	GPIO3 / CAM1_RST# [default] (Camera 1 Reset, active low output)	S112	Not connected
P112	GPIO4 / HDA_RST# [default] (HD Audio Reset, active low output)	S113	Not connected
P113	GPIO5 (General Purpose IO)	S114	Not connected
P114	GPIO6 (General Purpose IO)	S115	Not connected
P115	GPIO7 (General Purpose IO)	S116	Not connected
P116	GPIO8 (General Purpose IO)	S117	Not connected

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Primary (Top Side)	Pin #	Secondary (Bottom Side)
P117	GPIO9 (General Purpose IO)	S118	Not connected
P118	GPIO10 (General Purpose IO)	S119	GND
P119	GPIO11 (General Purpose IO)	S120	Not connected
P120	GND	P121	Not connected
P121	I2C_PM_CK (Power management I2C bus clock)	S122	Not connected
P122	I2C_PM_DAT(Power management I2C bus data)	S123	Not connected
P123	BOOT_SEL0# (Input straps determine the Module boot device. Pulled up on Module. Driven by OD part on Carrier.)	S124	GND
P124	BOOT_SEL1# (Input straps determine the Module boot device. Pulled up on Module. Driven by OD part on Carrier.)	S125	LVDS0+ (LVDS LCD data channel differential pair)
P125	BOOT_SEL2# (Input straps determine the Module boot device. Pulled up on Module. Driven by OD part on Carrier.)	S126	LVDS0- (LVDS LCD data channel differential pair)
P126	RESET_OUT# (General purpose reset output to Carrier board.)	S127	LCD_BKLT_EN (High enables panel backlight)
P127	RESET_IN# (Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise. Pulled up on Module. Driven by OD part on Carrier.)	S128	LVDS1+ (LVDS LCD data channel differential pair)
P128	POWER_BTN# (Power-button input from Carrier board. Carrier to float the line in inactive state. Active low, level sensitive. De-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.)	S129	LVDS1- (LVDS LCD data channel differential pair)
P129	SER0_TX (Asynchronous serial port data out)	S130	GND
P130	SER0_RX (Asynchronous serial port data in)	S131	LVDS2+ (LVDS LCD data channel differential pair)
P131	SER0_RTS# (Request to Send handshake line for SER0)	S132	LVDS2- (LVDS LCD data channel differential pair)
P132	SER0_CTS# (Clear to Send handshake line for SER0)	S133	LCD_VDD_EN (High enables panel VDD)
P133	GND	S134	LVDS_CK+ (LVDS LCD differential clock pair)
P134	SER1_TX (Asynchronous serial port data out)	S135	LVDS_CK- (LVDS LCD differential clock pair)
P135	SER1_RX (Asynchronous serial port data in)	S136	GND
P136	SER2_TX (Asynchronous serial port data out)	S137	LVDS3+ (LVDS LCD data channel differential pair)
P137	SER2_RX (Asynchronous serial port data in)	S138	LVDS3- (LVDS LCD data channel differential pair)
P138	SER2_RTS# (Request to Send handshake line for SER2)	S139	I2C_LCD_CK (I2C clock – to read LCD display EDID EEPROMs)
P139	SER2_CTS# (Clear to Send handshake line for SER2)	S140	I2C_LCD_DAT (I2C data – to read LCD display EDID EEPROMs)

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Primary (Top Side)	Pin #	Secondary (Bottom Side)
P140	Not connected	S141	LCD_BKLT_PWM (Display backlight PWM control)
P141	Not connected	S142	Not connected
P142	GND	S143	GND
P143	Not connected	S144	RSVD / EDP_HPD (Reserved for future eDP Hot Plug Detect pin)
P144	Not connected	S145	WDT_TIME_OUT# (Watchdog Timer Output)
P145	Not connected	S146	PCIE_WAKE (PCIe wake up interrupt to host – common to PCIe; links A, B, C – pulled up or terminated on Module)
P146	Not connected	S147	VDD_RTC (Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based Lithium cell or Super Cap. See ***Section 7.3 RTC Voltage Rail*** of the SMARC specification for an important safety note on the implementation of lithium backup batteries.)
P147	VDD_IN (Module power input voltage - 5V)	S148	LID# (Lid open/close indication to Module. Low indicates lid closure, which system ***may*** use to initiate a sleep state. Carrier to float the line in inactive state. Active low, level sensitive. De-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.)
P148	VDD_IN (Module power input voltage - 5V)	S149	SLEEP# (Sleep indicator from Carrier board; sourced from user Sleep button or Carrier logic. Carrier to float the line in inactive state. Active low, level sensitive; de-bounced on the Module. Pulled up on Module. Driven by OD part on Carrier.)
P149	VDD_IN (Module power input voltage - 5V)	S150	VIN_PWR_BAD# (Power bad indication from Carrier board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) ***is not*** enabled while this signal is held low by the Carrier. Pulled up on Module. Driven by OD part on Carrier.)
P150	VDD_IN (Module power input voltage - 5V)	S151	CHARGING# (Held low by Carrier during battery charging. Carrier to float the line when charge is complete. Pulled up on Module. Driven by OD part on Carrier.)
P151	VDD_IN (Module power input voltage - 5V)	S152	CHARGER_PRSNT# (Held low by Carrier if DC input for battery charger is present. Pulled up on Module. Driven by OD part on Carrier.)
P152	VDD_IN (Module power input voltage - 5V)	S153	CARRIER_STBY# (The Module drives this signal low when the system is in a standby power state)

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Table 3-2: SMARC P-S Connector (GF1) Signal Descriptions (Continued)

Pin #	Primary (Top Side)	Pin #	Secondary (Bottom Side)
P153	VDD_IN (Module power input voltage - 5V)	S154	CARRIER_PWR_ON (Carrier board circuits [apart from power management and power path circuits] ***are*** powered up until the Module asserts the CARRIER_PWR_ON signal)
P154	VDD_IN (Module power input voltage - 5V)	S155	FORCE_RECOV# (Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when the Force Recovery function is invoked. Pulled high on the Module. For SOCs that do not implement a USB based Force Recovery function, then a low on the Module FORCE_RECOV# pin ***may*** invoke the SOC native Force Recovery mode – such as over a Serial Port. Pulled up on Module. Driven by OD part on Carrier.)
P155	VDD_IN (Module power input voltage - 5V)	S156	BATLOW# (Battery low indication to Module. Carrier to float the line in inactive state. Pulled up on Module. Driven by OD part on Carrier.)
P156	VDD_IN (Module power input voltage - 5V)	S157	TEST# (Held low by Carrier to invoke Module vendor specific test function(s). Pulled up on Module. Driven by OD part on Carrier.)
		S158	GND

Note: The # symbol indicates the signal is Active Low.

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3.18 Debug (DB40)

Table 3-3 lists the pin signals of the CN1 connector, which provides 40 pins, 1 row, consecutive sequence with 0.02" (0.50mm) pitch.

Table 3-3: Debug Interface Signals (CN1)

Pin #	Interface	Signal
1	**NC**	RESVD (0R0 PD to GND)
2	**SMC Debug**	SMC_STATUS (Connect LED)
3		BIOS_MODE (Not Used)
4		SEL_BIOS (Connect to jumper for debug)
5		POSTWDT_DIS# (Connect to jumper for debug)
6	**Test Point**	SUS_S5# (Bridge to pin 22 (3V#_DUAL)
7		SUS_S4#
8		SUS_S3#
9		CB_PWROK (Connected to V3P3S)
10		CB_RESET# (Connected to pin 30)
11		SYS_RESET#
12		PWRBTN#
13	**SMC Program Interface**	SMC_OCD0B (Use jumper to connect 0CD0B via 1K0 pull-down to GND)
14		SMC_OCD0A (Use jumper to connect 0CD0A via 1K0 pull-up to 3.3V_SMC)
15		SMC_CLK
16		SMC_DATA
17		SMC_RESET_IN#
18		SMC_FLMD0
19		SMC_RXD6
20		SMC_TXD6
21		GND3
22		3V3_DUAL (Connected to V3P3A)
23		3V3_SMC1 (Connected to VBMC)
24	**LPC Debug Card Interface**	LPC_AD0
25		LPC_AD1 (3.3V provided from module)
26		LPC_AD2
27		LPC_AD3
28		LPC_FRAME#
29		CLK33_LPC
30		RST#
31		BIOS_DIS0
32		GND2
33		LPC_3V3 (Connected to V3P3S)
34	**SPI Program Interface**	SPI_BIOS_CLK
35		SPI_BIOS_MOSI
36		SPI_BIOS_MISO
37		SPI_BIOS_CS1#
38		SPI_BIOS_CS0#
39		GND1
40		VCC_SPI_IN (SPI power input from flash tool to module)

NOTE: The gray table cells denote ground. The # symbol indicates the signal is Active Low.

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4 Utilities

This chapter provides information on how to read information from and configure the BIOS Setup utility, the SEMA utility, the Watchdog Timer utility, and the board temperature sensors on the LEC-BTS.

4.1 BIOS

The LEC-BTS features an AMI BIOS. The default settings provide a “ready to run” system, even without a BIOS setup backup battery.

The BIOS is located in flash memory and can be easily updated with software under DOS.

All setup changes of the BIOS are stored in the CMOS RAM.

The battery on the baseboard will provide power to store that information for over two years without board activation.

This section presents screen shots the five primary menus of the BIOS Setup Utility. Use the following table as a quick reference for the contents of the BIOS Setup Utility. The submenus are presented as tables and describe the submenus and setting options for each menu item. The default setting options are presented in **bold**, and the function of each setting is described in the right hand column of the respective table.

Table 4-1: BIOS Setup Menu Structure

Main	Advanced	Security	Boot	Save & Exit
• BIOS Information • CPU Configuration • Memory Information • GOP Information • TXE Information • System Management ► • System Date • System Time	• CPU ► • Graphics ► • SATA► • USB ► • SDIO ► • Network ► • Audio ► • PCI/PCIe ► • Baytrail Features Configuration ► • ACPI ► • Serial Port Console ► • Thermal ► • Security ► • Miscellaneous ►	• Password Description ► • Administrator Password • Secure Boot Menu ►	• Boot Configuration ► • CSM Parameters ► • Boot Option Priorities • Add New Boot Option ► • Delete Boot Option ►	• Reset Options • Save Options • Boot Override • Launch EFI Shell from filesystem device • Reset System with ME disabled ModeMEUD000►

Notes:
► indicates a submenu

4.1.1 Starting the BIOS Setup Utility

Use the following bullets to initiate start-up activity for the BIOS Setup Utility.

- ► Press <DEL> during power up to start the BIOS setup utility.
- ► Press <F11> during power up to start the Boot menu.
- ► Press <END> during power up to return BIOS settings to default.

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4.1.2 Main Menu

The Main Menu provides read-only information about your system and also allows you to change System Management settings and set the System Date and Time. Refer to the tables below for details of the submenus and settings.

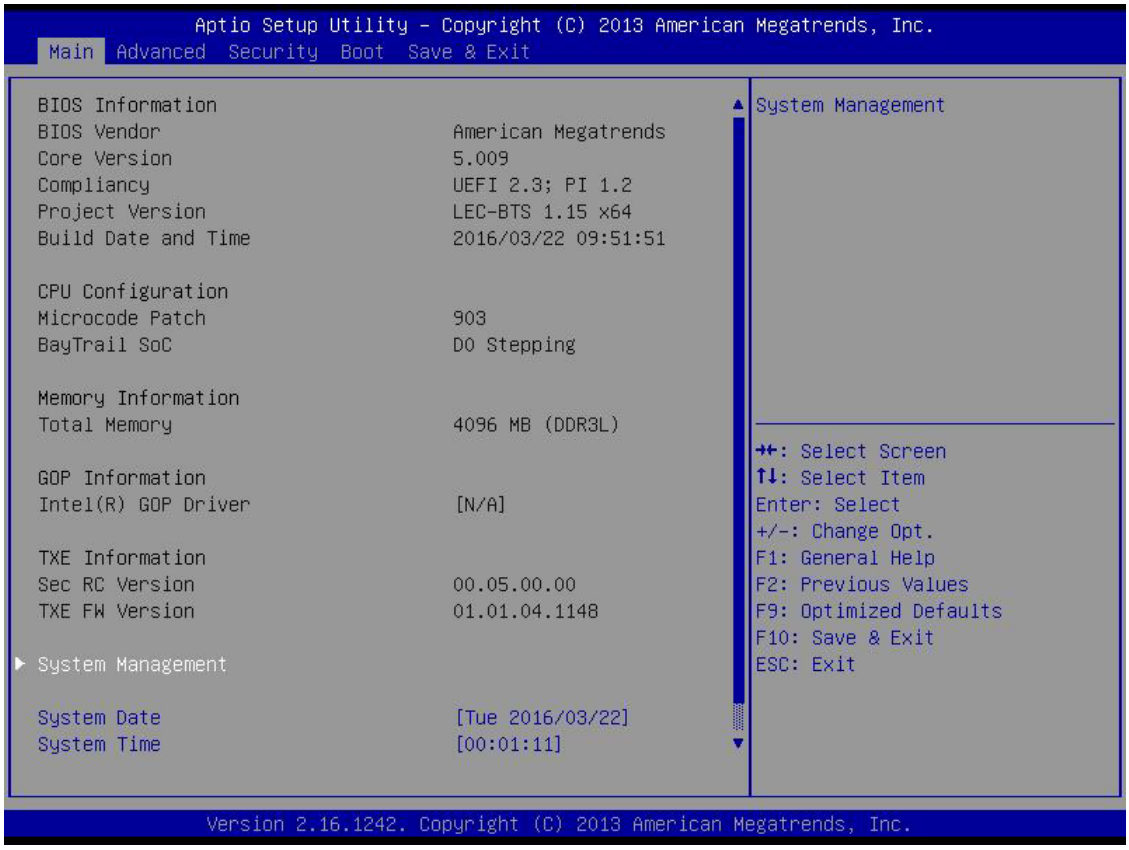


Figure 4-1: BIOS Setup Main Menu

BIOS Information

Table 4-2: Main Menu BIOS Information

Feature	Options	Description
BIOS Version	Info only	ADLINK BIOS version
Build Date and Time	Info only	Date the BIOS was built

Processor Information

Table 4-3: Main Menu Processor Information

Feature	Options	Description
CPU Microcode	Info only	Display CPU Microcode Patch
Bay Trail SOC	Info only	Display SOC stepping

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Memory Information

Table 4-4: Main Menu Memory Information

Feature	Options	Description
Total Memory	Info only	Display total memory information

GOP Information

Table 4-5: Main Menu GOP Information

Feature	Options	Description
Intel(R) GOP Driver	I[N/A]	

TXE Information

Table 4-6: Main Menu TXE Information

Feature	Options	Description
Sec RC Version	Info Only	Display RC Version
TXE FW Version	Info Only	display version of TXE

Main Menu > System Management

The System Management submenu provides read-only information about your system and also allows you to change some System Management settings. Refer to the tables below for details of the submenus and settings

Main Menu > System Management > Board Information

Table 4-7: Main Menu > System Management > Board Information

Board Information	Options	Description
SEMA Firmware	Read only	Display SMC firmware
Build Date	Read only	Display SMC firmware build date
SEMA Boot loader	Read only	Display SMC boot loader
Build Date	Read only	Display SMC boot loader build date
Hardware Version	Read only	Display SMC hardware version
Serial Number	Read only	Display SMC serial number
Manufacturing Date	Read only	Display SMC manufacturing date
Last Repair Date	Read only	Display SMC last repair date
MAC ID	Read only	Display SMC MAC ID
SEMA Features:	Read only	Display SEMA features

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Main Menu > System Management > Temperatures

Table 4-8: Main Menu > System Management > Temperature

Feature	Options	Description
Temperatures	Info only	
Board Temperatures	Info only	
▷ Current	Read only	Display current board temperature
▷ Startup	Read only	Display board startup temperature
▷ Min	Read only	Display board min. temperature
▷ Max	Read only	Display board max. temperature

Main Menu > System Management > Power Consumption

Table 4-9: Main Menu > System Management > Power Consumption

Feature	Options	Description
Power Consumption	Info only	
Current Input Current	Read only	Display input current
Current Input Power	Read only	Display input power
GPU_Vcore	Read only	Display actual GPU-Vcore voltage
GFX-Vcore	Read only	Display actual GFX-Vcore voltage
V1.00	Read only	Display actual V1.00 voltage
VMEM	Read only	Display actual VMEM voltage
V1.80	Read only	Display actual V1.80 voltage
V3.30	Read only	Display actual V3.30 voltage
V3.30	Read only	Display actual V3.30 voltage
VIN	Read only	Display actual VIN voltage

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Main Menu > System Management > Runtime Statistics

Table 4-10: Main Menu > System Management > Runtime Statistics

Feature	Options	Description
Runtime Statistics	Info only	
Total Runtime	Read only	The returned value specifies the total time in minutes the system is running in S0 state.
Current Runtime	Read only	• The returned value specifies the time in seconds the system is running in S0 state. • This counter is cleared when the system is removed from the external power supply.
Power Cycles	Read only	The returned value specifies the number of times the external power supply has been shut down
Boot Cycles	Read only	The Bootcounter is increased after a HW- or SW-Reset or after a successful power-up.
Boot Reason	Read only	The boot reason is the event which causes the reboot of the system.

Main Menu > System Management > Flags

Table 4-11: Main Menu > System Management > Flags

Feature	Options	Description
Flags	Info only	
BMC Flags	Read only	
BIOS Select	Read only	Display the selection of current BIOS ROM
ATX/AT-Mode	Read only	Display ATX/AT-Mode
Exception Code	Read only	System exception reason

Main Menu > System Management > Power Up

Table 4-12: Main Menu >System Management > Power Up

Feature	Options	Description
Power Up	Info only	
Power Up watchdog Note: F12 disables the Power Up Watchdog.	• Enabled • **Disabled**	The Power-Up Watchdog resets the system after a certain amount of time after power-up.
Power-up Mode Attention: The Power-Up Mode only has affect, if the module is in ATX-Mode.	• **Turn on** • Remain off • Last State	• Turn On: The machine starts automatically when the power supply is turned on. • Remain Off: To start the machine the power button has to be pressed. • Last State: When powered on during a power failure the system will automatically power on when power is restored.

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Main Menu > System Management > LVDS Backlight

Table 4-13: Main Menu > System Management > LVDS Backlight

Feature	Options	Description
LVDS Backlight	Info only	
LVDS Backlight Bright	255	The value range starts at 0 and ends at 255.

Main Menu > System Date and Time

Table 4-14: Main Menu > System Date and Time

Feature	Options	Description
System Date	Day of Week, MM/DD/YYYY	Requires the alpha-numeric entry of the day of the week, day of the month, calendar month, and all 4 digits of the year, indicating the century and year (Fri XX/XX/20XX)
System Time	HH/MM/SS	Presented as a 24-hour clock setting in hours, minutes, and seconds

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4.1.3 Advanced Menu

This menu contains the settings for most of the user interfaces in the system. The “Advanced” menu provides configuration settings for CPU, Memory, Graphics, SATA, USB, SDIO, Network, Audio, PCIe Configuration, ACPI, Serial Console, Thermal, Security, and Miscellaneous.



Inappropriate values for any of the following advanced settings may cause system errors.

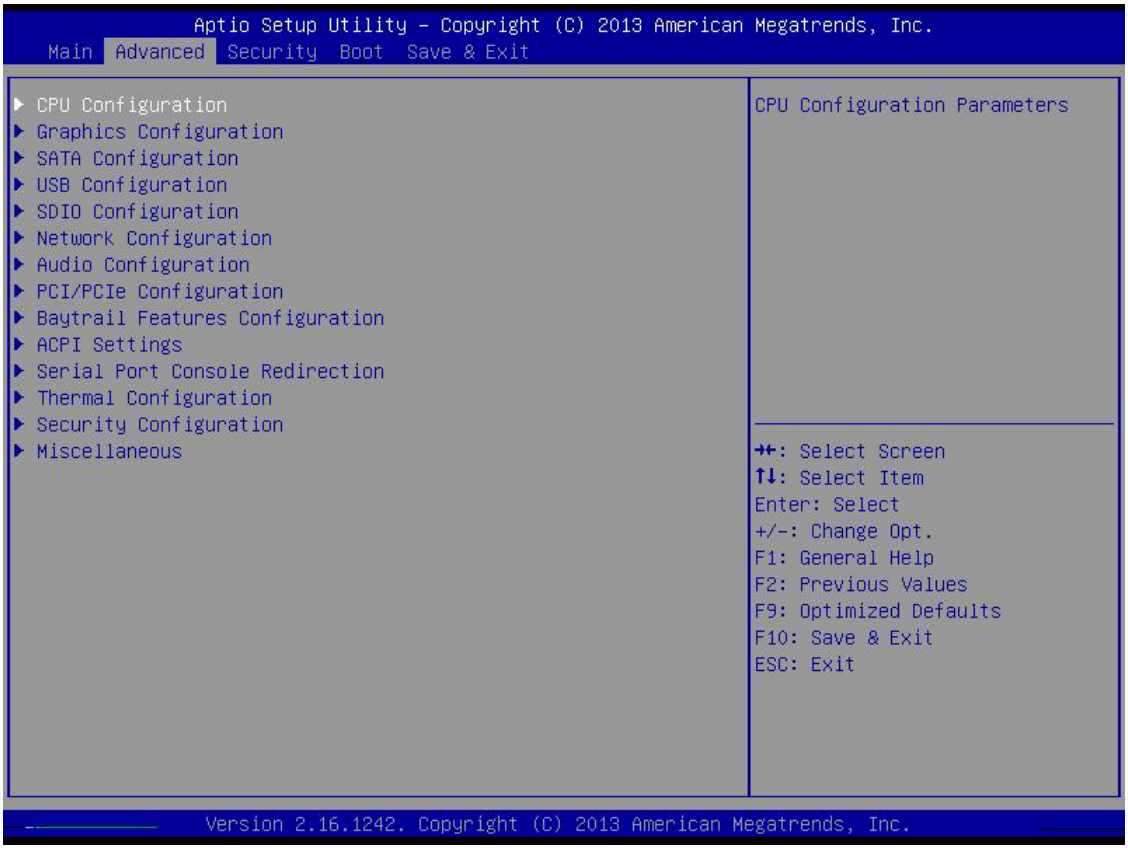


Figure 4-2: BIOS Setup Advanced Menu

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Advanced Menu > CPU Configuration



Figure 4-3: BIOS Setup Advanced Menu > CPU Configuration

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Advanced > CPU Configuration > Socket 0 CPU Information

Table 4-15: Advanced > CPU Configuration > Socket 0 Information

Feature	Options	Description
CPU Brand Name	Info only	Display CPU brand name
CPU Signature	Info only	Display CPU signature
Microcode Patch	Info only	Display microcode patch
Max CPU speed	Info only	Display max. CPU speed
Min CPU speed	Info only	Display min. CPU speed
Processor Cores	Info only	Display number of processor cores
Intel HT Technology	Info only	Display Intel HT Technology support
Intel VT-x Technology	Info only	Display Intel VT-x Technology support
64-bit	Info only	Display 64-bit support
L1 Data Cache	Info only	Display cache info
L1 Code Cache	Info only	Display cache info
L2 Cache	Info only	Display cache info
L3 Cache	Info only	Display cache info

Advanced > CPU Configuration > CPU Thermal Configuration

Table 4-16: Advanced > CPU Configuration > CPU Thermal Configuration

Feature	Options	Description
DTS	• Disabled • **Enabled**	Enable/Disable digital thermal sensor

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Advanced > CPU Configuration > PPM Configuration

Table 4-17: Advanced > CPU Configuration > CPU Thermal Configuration

Feature	Options	Description
CPU C state report	• Disabled • **Enabled**	Enable/Disable CPU C state report to OS
Max CPU C state	• **C7** • C6 • C1	This option controls Max C state that the processor will support
CPU speed	Info only	
64-bit	Info only	
Limit CPUID Maximum	• **Disabled** • Enabled	Disabled for windows XP
Execute Disabled Bit	• Disabled • **Enabled**	XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, Red Hat enterprise 3 Update3.)
Intel Virtualization Technology	• Disabled • **Enabled**	When enabled, a VWM can utilize the additional hardware capabilities provided by Vanderpool Technology
Power Technology	• Disabled • **Energy Efficient** • Custom	Enable the power management features

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Advanced Menu > Graphics

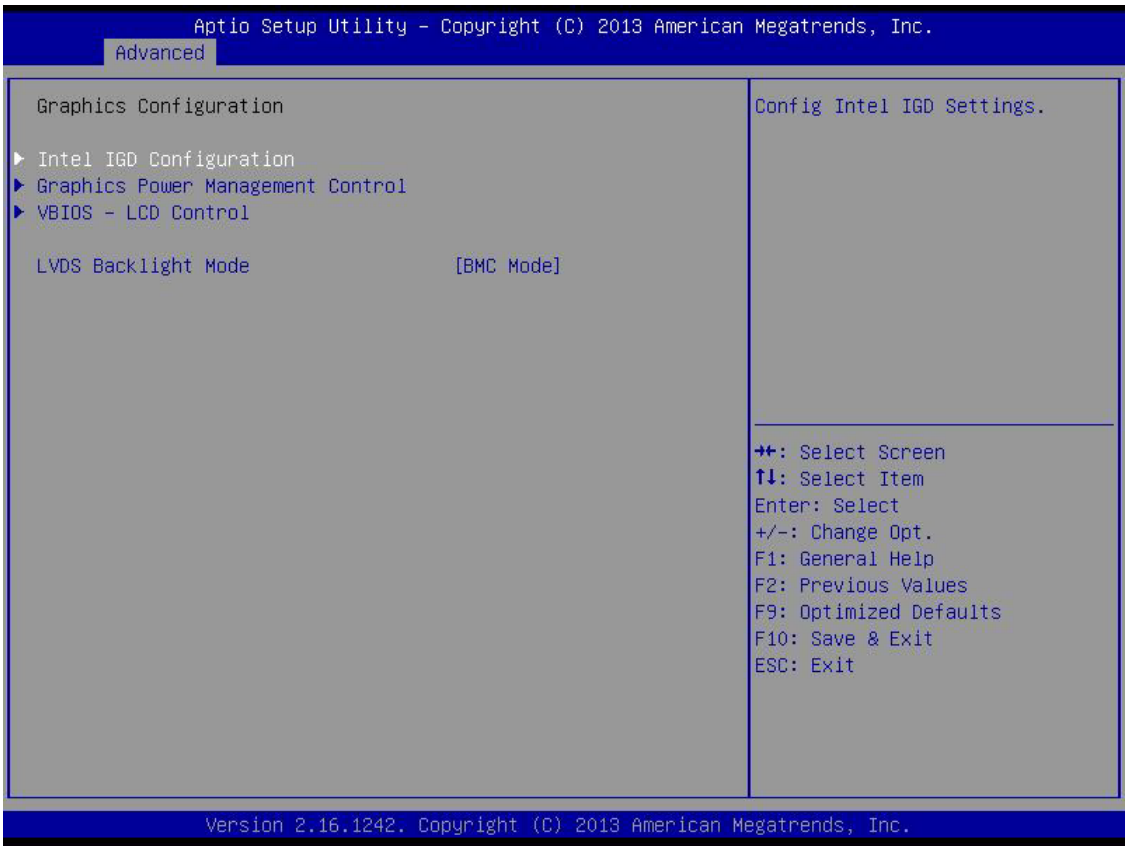


Figure 4-4: BIOS Setup Advanced Menu > Graphics Configuration

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Advanced > Graphics > Intel IGD Configuration

Table 4-18: Advanced > Graphics Configuration

Feature	Options	Description
Integrated Graphics Device	• **Enabled** • Disabled	Enabled: Enable Integrated Graphics Device (IGD) when selected as the primary display; Disabled: Always disable IGD
IGD Turbo Enable	• **Enabled** • Disabled	Enable: Enable IGD Turbo Enable; Disable: IGD Turbo Disable
Primary Display	• **Auto** • IGD • PCIE	Select which graphics device (IGD/PCI) should be primary display
GFX Boost	• Enabled • **Disabled**	Enable/Disable GFX Boost
PAVC	• Disabled • **LITE Mode** • SERPENT Mode	Enable/Disable Protected Audio Video Control
DVMT Pre-Allocated	**64M**	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.
DVMT Total Gfx Mem	**256MB**	Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device.
Aperture Size	**256MB**	Select the aperture size
DOP CG	• **Enabled** • Disabled	Enable/Disable DOP Clock Gating
GTT Size	**2MB**	Select the GTT size
IGD Thermal	• Enabled • **Disabled**	Enable/Disable IGD Thermal
Spread Spectrum clock	• Enabled • **Disabled**	Enable/Disable Spread Spectrum clock
ISP Enable/Disable	• **Enabled** • Disabled	Enable/Disable ISP PCI Device Selection
ISP PCI Device Selection	• **Disabled** • ISP PCI Device as B0D2F0 • ISP PCI Device as B0D3F0	Default ISP is PCI B0D2F0 for Window Boot. Linux Boot to Select B0D3F0
Vcc_Vnn for Power State2	• Enabled • **Disabled**	Enable or Disable Vcc Vnn Config for Power State2

Advanced > Graphics > Graphics Power Management Control

Table 4-19: Advanced > CPU Configuration > CPU Thermal Configuration

Feature	Options	Description
RC6 (Render Standby)	• **Enabled** • Disabled	Enable/Disable render standby support

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Advanced > Graphics > VBIOS - LCD Control

Table 4-20: Advanced > Graphics > VBIOS > LCD control

Feature	Options	Description
Primary IGFX Boot Display	• **VBIOS Default** • HDMI • LVDS	Select the Video Device that will be activated during POST. This has no effect if external graphics are present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display.
LCD Panel Type	**VBIOS Default**	Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.
Panel Scaling	• **Auto** • Off • Force Scaling	Select the LCD panel scaling option used by the Internal Graphics Device.

Advanced > Graphics > LVDS Backlight Mode

Table 4-21: Advanced >Graphics > LVDS Backlight Mode

Feature	Options	Description
LVDS Backlight Mode	• **BMC Mode** • GTT Mode	Select LVDS backlight control function.

Advanced Menu > SATA

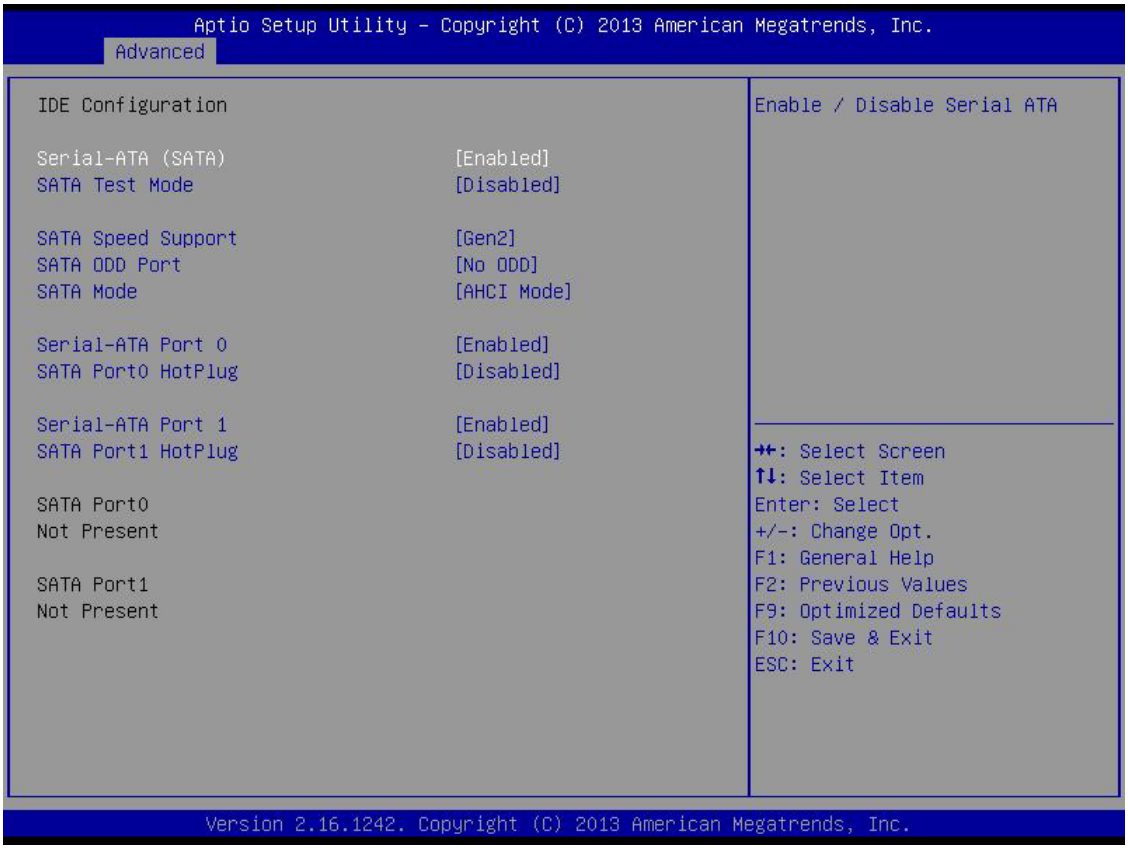


Figure 4-5: BIOS Setup Advanced Menu > SATA

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Table 4-22: Advanced > SATA

Feature	Options	Description
Serial-ATA Controller	• **Enabled** • Disabled	Enable/Disable Serial ATA.
SATA Test Mode	• Enabled • **Disabled**	Test Mode enable/disable
SATA Speed Support	• Gen1 • **Gen2**	SATA speed support Gen1 or Gen2.
SATA ODD Port	• Port0 ODD • **No ODD**	SATA ODD is Port0 or Port1
SATA Mode	• IDE Mode • **AHCI Mode**	Select IDE/AHCI
Serial-ATA Port X	• **Enabled** • Disabled	Enable/Disable SATA port X.
SATA PortX HotPlug	• Enabled • **Disabled**	Enable/Disable SATA port X hotplug.

Advanced Menu > USB

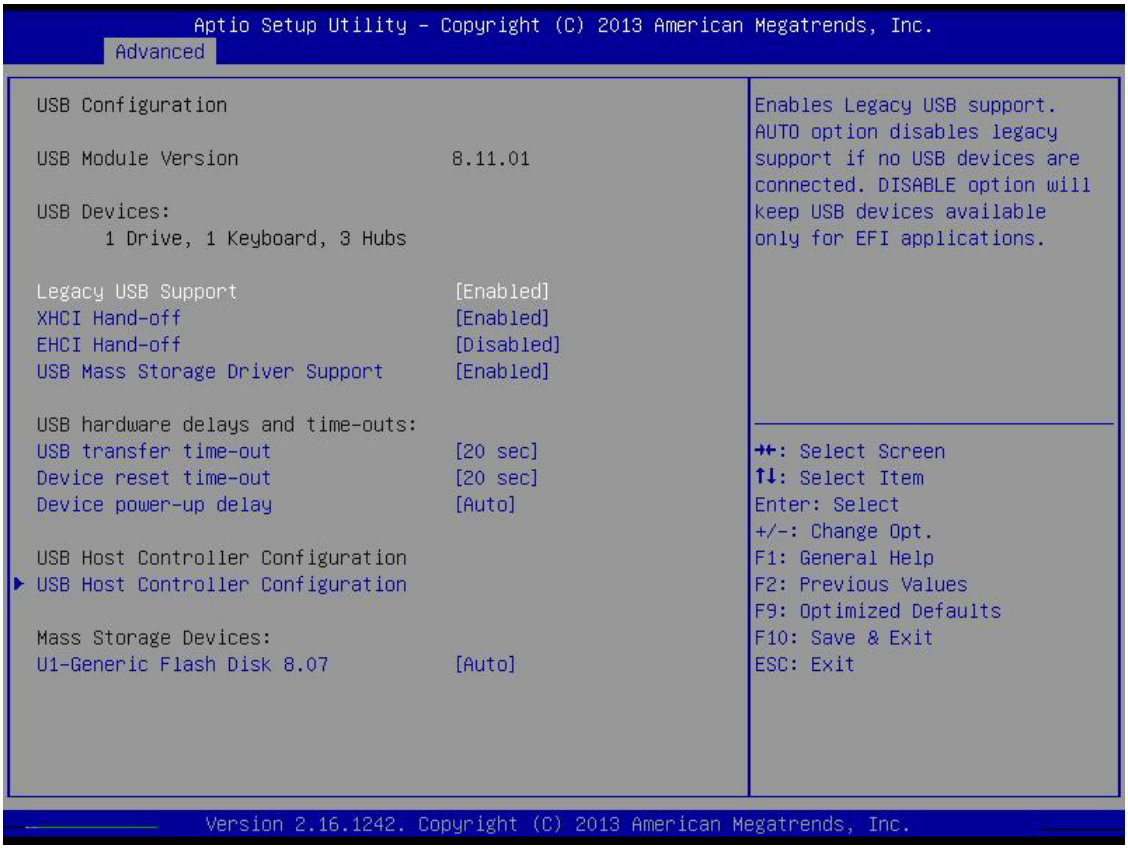


Figure 4-6: BIOS Setup Advanced Menu > USB

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Table 4-23: Advanced Menu > USB

Feature	Options	Description
USB	Info only	
USB Module Version	Info only	
USB Devices	Info only	Drives, keyboards, mouse, hubs
Legacy USB Support	• **Enabled** • Disabled • Auto	• Enables legacy USB support. • Auto option disables legacy support if no USB devices are connected. • Disable option will keep USB devices available only for EFI applications and setup.
XHCI Hand-off	• **Enabled** • Disabled	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by the XHCI OS driver.
EHCI Hand-off	• Enabled • **Disabled**	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by the EHCI OS driver.
USB Mass Storage Driver Support	• **Enabled** • Disabled	Enable/Disable USB mass storage driver support.
USB transfer time-out	• 1 sec • 5 sec • 10 sec • **20 sec**	The time-out value for control, bulk, and interrupt transfers
Device reset time-out	• 10 sec • **20 sec** • 30 sec • 40 sec	USB mass storage device Start Unit command time-out.
Device power-up delay	• **Auto** • Manual	Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.
Mass Storage Devices	Info only	List current USB mass storage devices.

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Advanced > USB > USB Host Controller Configuration

Table 4-24: Advanced Chipset USB Configuration

Feature	Options	Description
USB Client Support	• PCI mode • **Disabled**	Enable/Disable USB OTG Support
XHCI Mode	• Enabled • **Disabled** • Auto • Smart Auto	Mode of operation of xHCI controller.
USB 2.0 (EHCI) Support	• **Enabled** • Disabled	Control the USB EHCI (USB 2.0) functions. One EHCI controller must always be enabled.
USB EHCI debug	• Enabled • **Disabled**	Enable/Disable PCH EHCI debug capability
USB Per Port Control	• **Enabled** • Disabled	Control each of the USB ports (0~2). Enable: Enable USB per port; Disable: Use USB port x settings.
USB Port #0~2	• **Enabled** • Disabled	Enable/Disable USB port 0-2.

Advanced Menu > SDIO

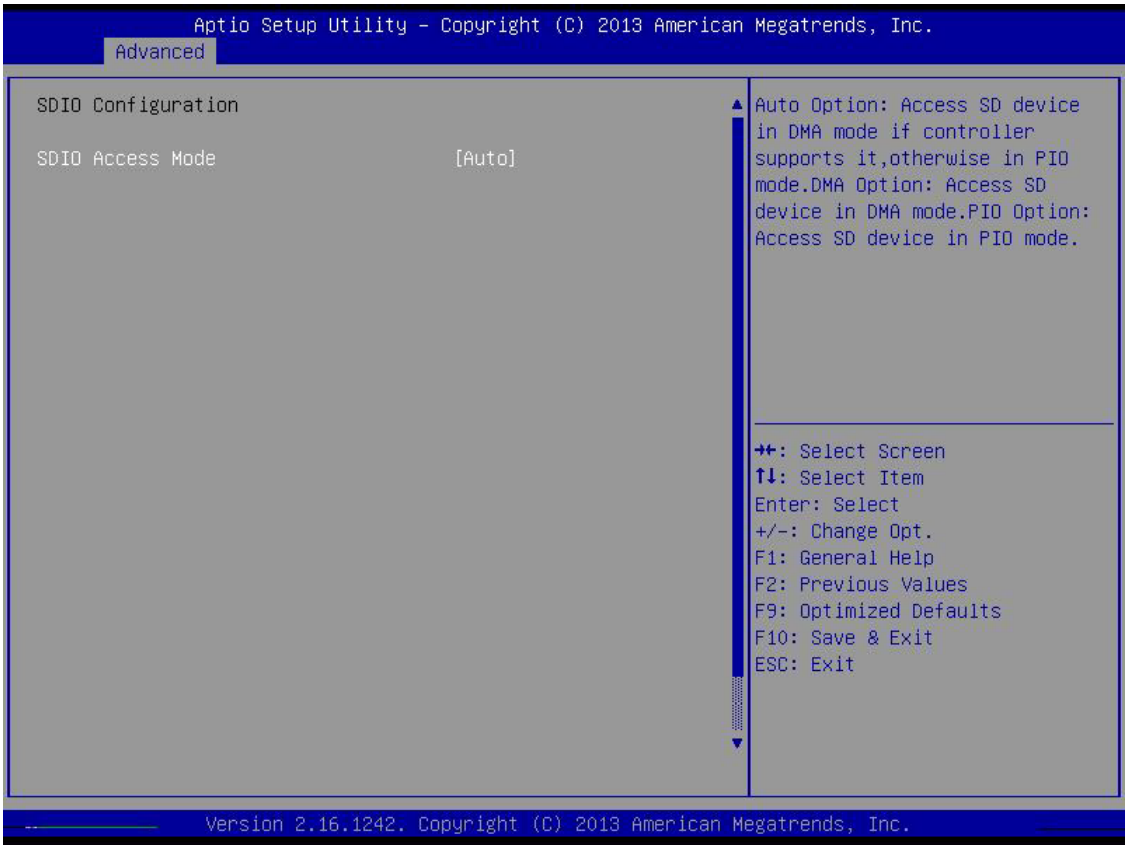


Figure 4-7: BIOS Setup Advanced Menu > SDIO

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Table 4-25: Advanced Menu > SDIO

Feature	Options	Description
SDIO Access Mode	• **Auto** • DMA • PIO	Auto Option: Access SD device in DMA mode if controller supports it, other wise in PIO mode. DMA Option: Access SD device in DMA mode. PIO Option: Access SD device in PIO mode.

Advanced Menu > Network

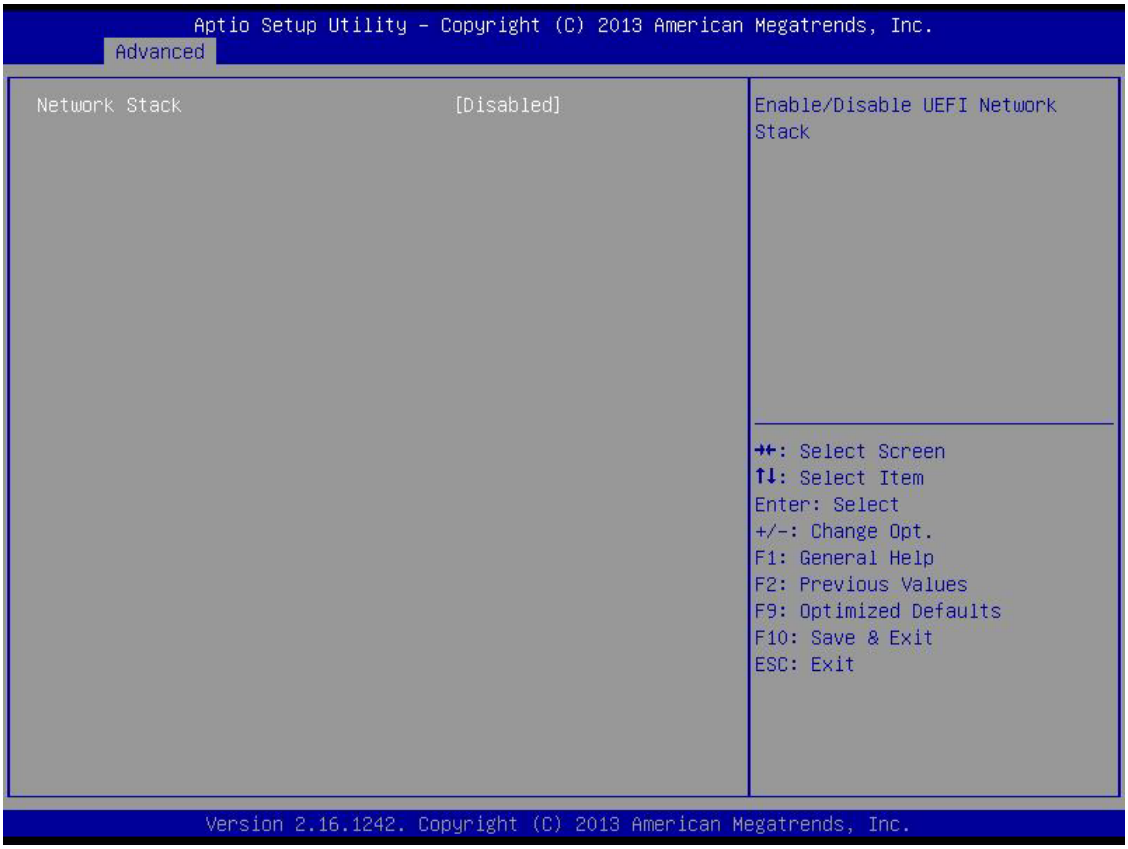


Figure 4-8: BIOS Setup Advanced Menu > Network

Table 4-26: Advanced Network

Feature	Options	Description
Network Stack	• Enabled • **Disabled**	Enable/Disable UEFI network stack.

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Advanced Menu > Audio Configuration

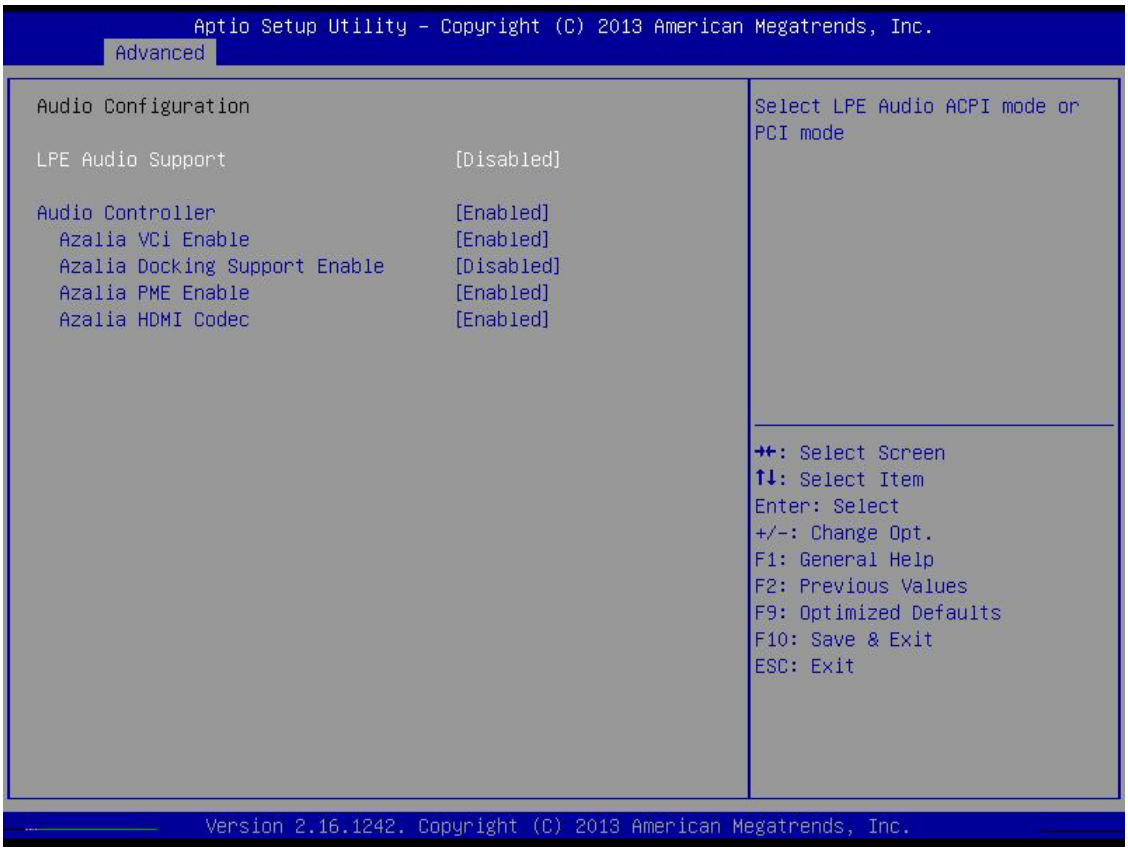


Figure 4-9: BIOS Setup Advanced Menu > Audio Configuration

Table 4-27: Advanced Menu > Audio Configuration

Feature	Options	Description
LPE Audio Support	• Enabled • **Disabled**	Select LPE Audio ACPI mode or PCI mode
Audio Controller	• **Enabled** • Disabled	Control Detection of the Azalia device. Disabled = Azalia will be unconditionally disabled. Enabled = Azalia will be unconditionally Enabled
Azalia VCi Enable	• **Enabled** • Disabled	Enable/Disable Virtual Channel 1 of Audio Controller
Azalia Docking Support Enable	• Enabled • **Disabled**	Enable/Disable Azalia Docking Support of Audio Controller
Azalia PME Enable	• **Enabled** • Disabled	Enable/Disable Power Management capability of Audio Controller
Azalia HDMI Codec	• **Enabled** • Disabled	Enable/Disable internal HDMI codec for Azalia

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Advanced Menu > PCI_PCIe Configuration

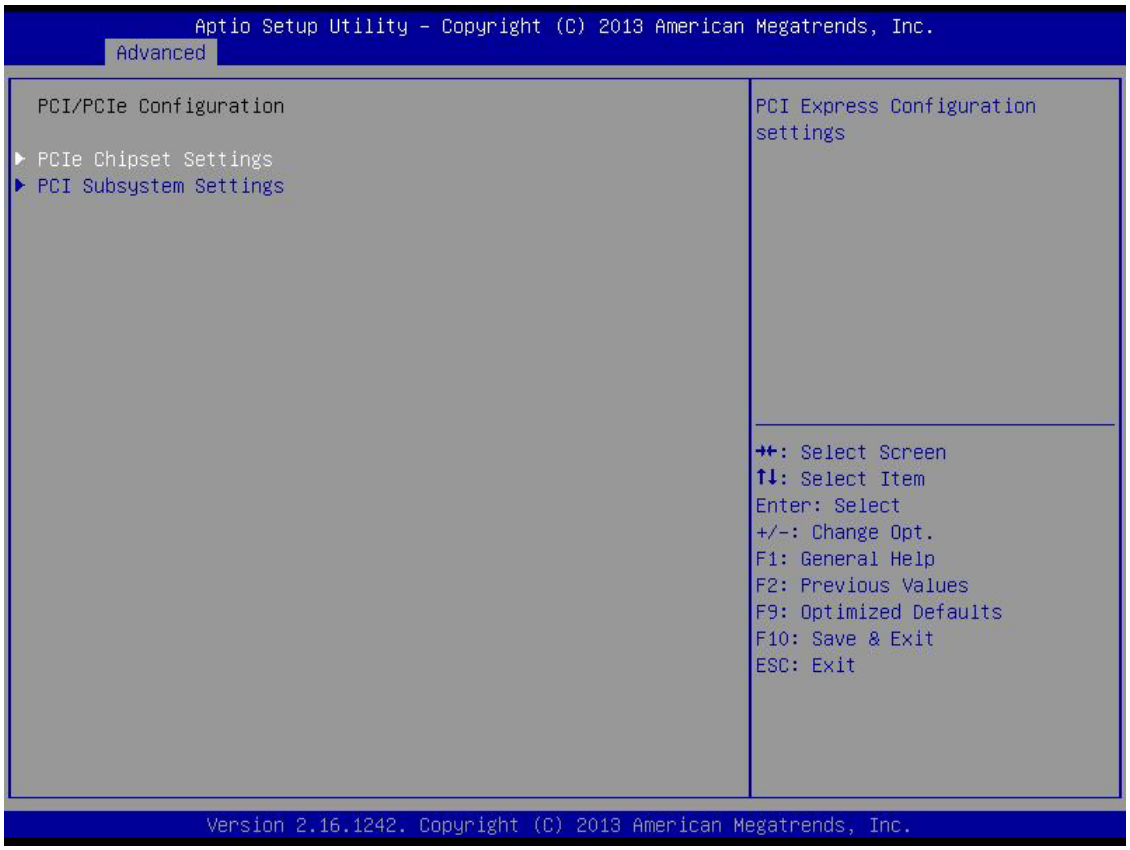


Figure 4-10: BIOS Setup Advanced Menu > PCI_PCIe Configuration

Advanced Menu > PCIe Configuration > PCIe Chipset Settings

Table 4-28: Advanced Menu > PCIe Configuration > PCIe Chipset Settings

Feature	Options	Description
PCI Express Port x	• **Enabled** • Disabled	Enable or disable the PCI Express Port x in the chipset.
Hot Plug	• **Enabled** • Disabled	Enable or disable PCI Express hotplug.
Speed	• **Auto** • Gen 2 • Gen 1	Configure PCIe port speed.

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Advanced Menu > PCIe Configuration > PCI Subsystem Settings

Table 4-29: Advanced Menu > PCIe Configuration > PCI Subsystem Settings

Feature	Options	Description
PCI Latency Timer	**32 PCI Bus Clocks**	Value to be programmed into PCI latency timer register
PCI-X Latency Timer	**64 PCI Bus Clocks**	Value to be programmed into PCI-X latency timer register
VGA Palette Snoop	• Enabled • **Disabled**	Enables or Disables VGA palette registers snooping
PERR# Generation	• Enabled • **Disabled**	Enables or Disables PCI Device to Generate PERR#
SERR# Generation	• Enabled • **Disabled**	Enables or Disables PCI Device to generate SERR#
Above 4G Decoding	• Enabled • **Disabled**	Enables or Disables 64bit capable Devices to be Decoded in Above 4G Address Space (Only if System Supports 64 bit PCI Decoding)
SR-IOV Support	• Enabled • **Disabled**	If system has SR-IOV capable PCIe Devices, this option Enables or Disables Single Root IO Virtualization Support

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Advanced Menu > PCIe Configuration > PCI Subsystem Settings > PCI Express Settings

Table 4-30: Advanced Menu > PCIe Configuration > PCI Subsystem Settings > PCIe Settings

Feature	Options	Description
Relaxed Ordering	• Enabled • **Disabled**	Enables or Disables PCI Express device relaxed ordering.
Extended Tag	• Enabled • **Disabled**	If Enabled, allows device to use 8-bit tag field as a requester.
No Snoop	• **Enabled** • Disabled	Enables or Disables PCI Express device No Snoop option.
Maximum Payload	**Auto**	Set maximum payload of PCI Express device or allow system BIOS to select the value.
Maximum Read Request	**Auto**	Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value
PCI Express Link Register Settings	Info only	
ASPM Support	• **Disabled** • Auto • Force L0s	• Set the ASPM Level: • DISABLE - Disables ASPM • AUTO - BIOS auto configure • Force L0s - Force all links to L0s State
Extended Synch	• Enabled • **Disabled**	If ENABLED allows generation of Extended Synchronization patterns
Link Training Retry	• Disabled • 2 • 3 • **5**	Defines number of Retry Attempts software will take to retrain the link if previous training attempt was unsuccessful
Link Training Timeout (uS)	**1000**	Defines number of Microseconds software will wait before polling 'Link Training' bit in Link Status register. Value range from 10 to 10000 uS
Unpopulated Links	• **Keep Link ON** • Disabled	In order to save power, software will disable unpopulated PCI Express links, if this option set to 'Disable Link'
Restore PCIE Registers	• Enabled • **Disabled**	On non-PCI Express aware OS's (Pre Windows Vista) some devices may not be correctly reinitialized after S3. Enabling this restores PCI Express device configurations on S3 resume. Warning: Enabling this may cause issues with other hardware after S3 resume

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Advanced Menu > PCIe Configuration > PCI Subsystem Settings > PCI Express GEN 2 Settings

Table 4-31: Advanced Menu > PCIe Configuration > PCI Subsystem Settings > PCIe GEN 2 Settings

Feature	Options	Description
Completion Timeout	• **Default** • Shorter • Longer • Disabled	In device Functions that support Completion Timeout programmability, allows system software to modify the Completion Timeout value. 'Default' 50us to 50ms. If 'Shorter' is selected, software will use shorter timeout ranges supported by hardware. If 'Longer' is selected, software will use longer timeout ranges
ARI Forwarding	• Enabled • **Disabled**	If supported by hardware and set to 'Enabled', the Downstream Port disables its traditional Device Number field being 0 enforcement when turning a Type1 Configuration Request into a Type0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port
AtomicOp Requester Enable	• Enabled • **Disabled**	If supported by hardware and set to 'Enabled', this function initiates AtomicOp Requests only if Bus Master Enable bit is in the Command Register Set
AtomicOp Egress Blocking	• Enabled • **Disabled**	If supported by hardware and set to 'Enabled', outbound AtomicOp Requests via Egress Ports will be blocked
IDO Request Enable	• Enabled • **Disabled**	If supported by hardware and set to 'Enabled', this permits setting the number of ID-Based Ordering (IDO) bit (Attribute[2]) requests to be initiated
IDO Completion Enable	• Enabled • **Disabled**	If supported by hardware and set to 'Enabled', this permits setting the number of ID-Based Ordering (IDO) bit (Attribute[2]) requests to be initiated
LTR Mechanism Enable	• Enabled • **Disabled**	If supported by hardware and set to 'Enabled', this enables the Latency Tolerance Reporting (LTR) Mechanism
End-End TLP Prefix Blocking	• Enabled • **Disabled**	If supported by hardware and set to 'Enabled', this function will block forwarding of TLPs containing End-End TLP Prefixes
PCI Express GEN2 Link Register Settings	Info only	

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Table 4-31: Advanced Menu > PCIe Configuration > PCI Subsystem Settings > PCIe GEN 2 Settings (Continued)

Feature	Options	Description
Target Link Speed	• **Auto** • Force to 2.5 GT/s • Force to 5.0 GT/s	If supported by hardware and set to 'Force to 2.5 GT/s' for Downstream Ports, this sets an upper limit on Link operational speed by restricting the values advertised by the Upstream component in its training sequences. When 'Auto' is selected HW initialized data will be used
Clock Power Management	• Enabled • **Disabled**	If supported by hardware and set to 'Enabled', the device is permitted to use CLKREQ# signal for power management of Link clock in accordance to protocol defined in appropriate form factor specification
Compliance SOS	• Enabled • **Disabled**	If supported by hardware and set to 'Enabled', this will force LTSSM to send SKP Ordered Sets between sequences when sending Compliance Pattern or Modified Compliance Pattern
Hardware Autonomous Width	• Enabled • **Disabled**	If supported by hardware and set to 'Disabled', this will disable the hardware's ability to change link width except width size reduction for the purpose of correcting unstable link operation
Hardware Autonomous Speed	• Enabled • **Disabled**	If supported by hardware and set to 'Disabled', this will disable the hardware's ability to change link speed except speed rate reduction for the purpose of correcting unstable link operation

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Advanced Menu > Baytrail Features

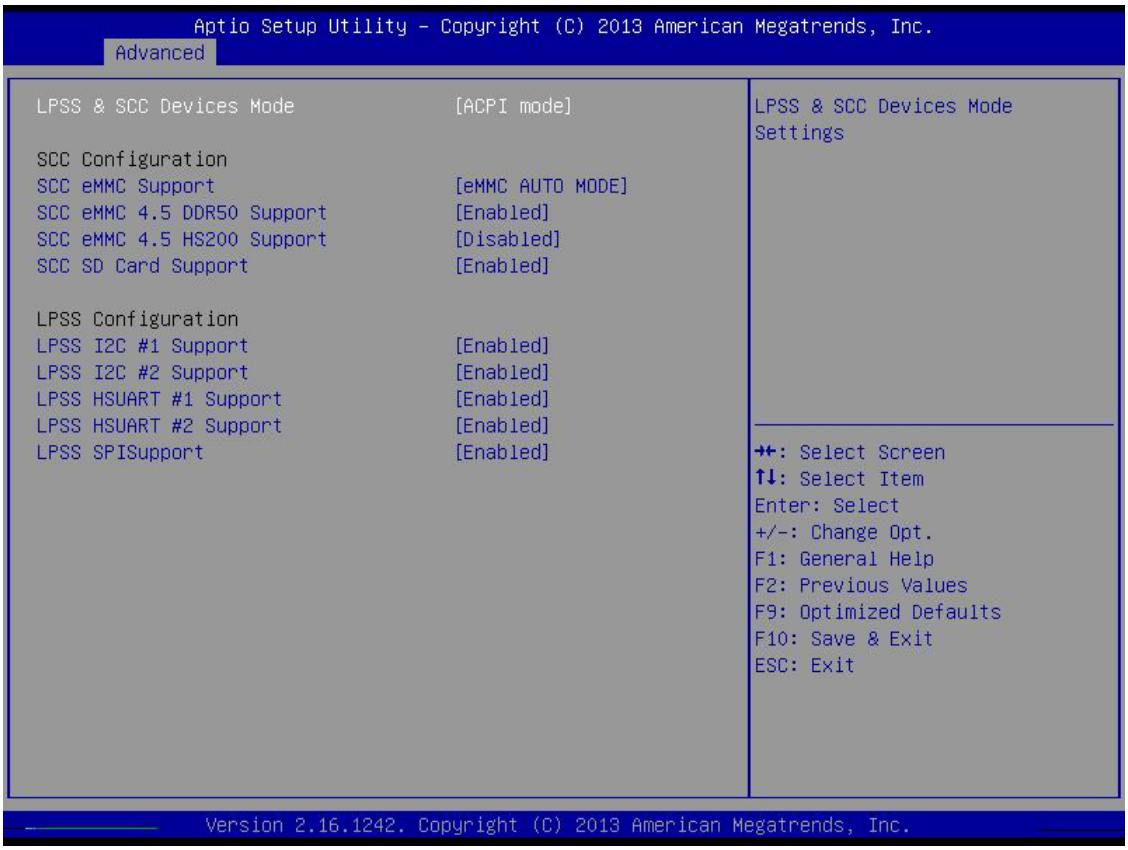


Figure 4-11: BIOS Setup Advanced Menu > Baytrail Features

Table 4-32: Advanced > Baytrail Features

Feature	Options	Description
LPSS & SCC Devices Mode	• **ACPI mode** • PCI mode	LPSS & SCC Devices Mode Settings
SCC Configuration	Info only	
SCC eMMC Support	• Enable eMMC 4.5 Support • Enable eMMC 4.41 Support • **eMMC AUTO MODE** • Disabled	SCC eMMC Support Enable\Disable
SCC eMMC 4.5 DDR50 Support	• **Enabled** • Disabled	SCC eMMC 4.5 DDR50 Support Enable\Disable
SCC eMMC 4.5 HS200 Support	• Enabled • **Disabled**	SCC eMMC 4.5 HS200 Support Enable\Disable
SCC SD Card Support	• **Enabled** • Disabled	SCC SD Card Support Enable\Disable
LPSS Configuration	• Info only	
LPSS I2C #1 Support	• **Enabled** • Disabled	LPSS I2C #1 Support Enable\Disable
LPSS I2C #2 Support	• **Enabled** • Disabled	LPSS I2C #2 Support Enable\Disable

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Table 4-32: Advanced > Baytrail Features (Continued)

Feature	Options	Description
LPSS HSUART #1 Support	• **Enabled** • Disabled	LPSS HSUART #1 Support Enable\Disable
LPSS HSUART #2 Support	• **Enabled** • Disabled	LPSS HSUART #2 Support Enable\Disable
LPSS SPISupport	• **Enabled** • Disabled	LPSS SPISupport Enable\Disable

Advanced Menu > ACPI

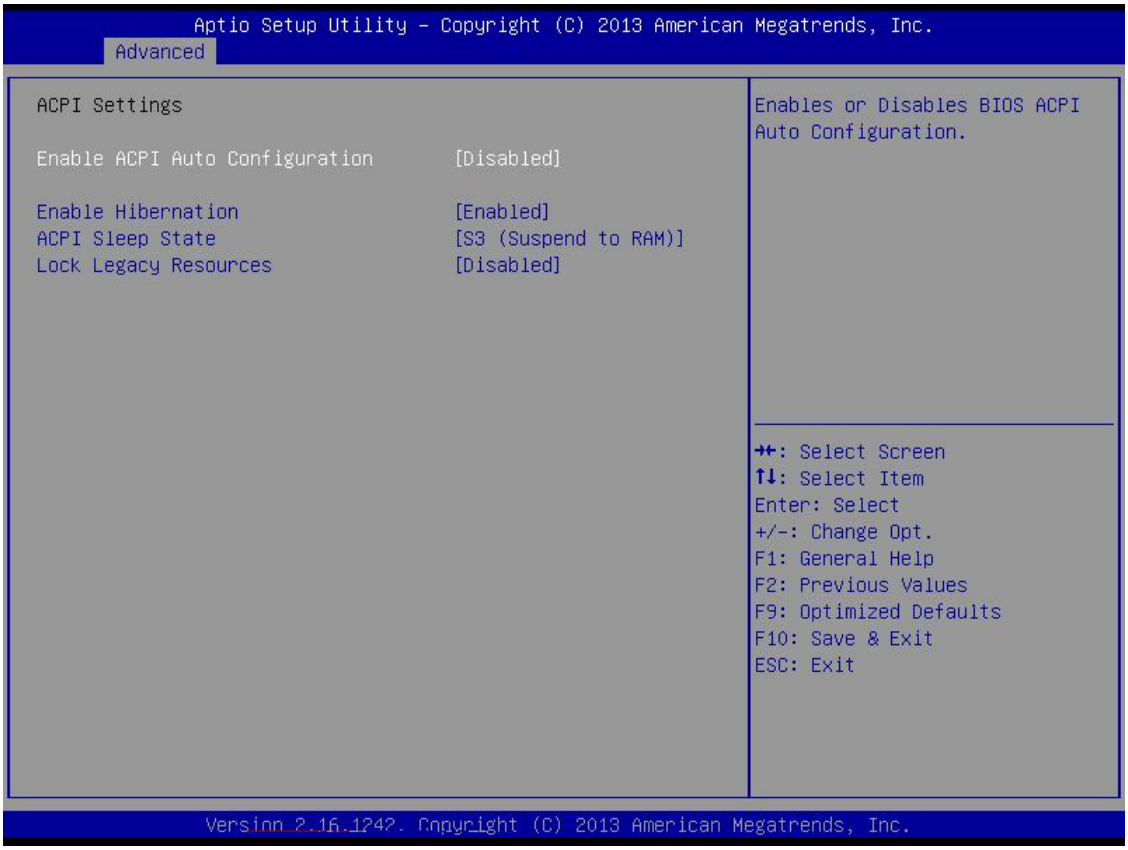


Figure 4-12: BIOS Setup Advanced Menu > ACPI

Table 4-33: Advanced > ACPI

Feature	Options	Description
ACPI	Info only	
Enable ACPI Auto Configuration	• Enabled • **Disabled**	Enables or disables BIOS ACPI Auto Configuration.
Enable Hibernation	• **Enabled** • Disabled	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	• Suspend Disabled • **S3 (Suspend to RAM)**	Select the highest ACPI sleep state the system will enter when the Suspend button is pressed.

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Table 4-33: Advanced > ACPI

Feature	Options	Description
Lock Legacy Resources	• Enabled • **Disabled**	Enables or Disables Lock of Legacy Resources

Advanced Menu > Serial Port Console Redirection

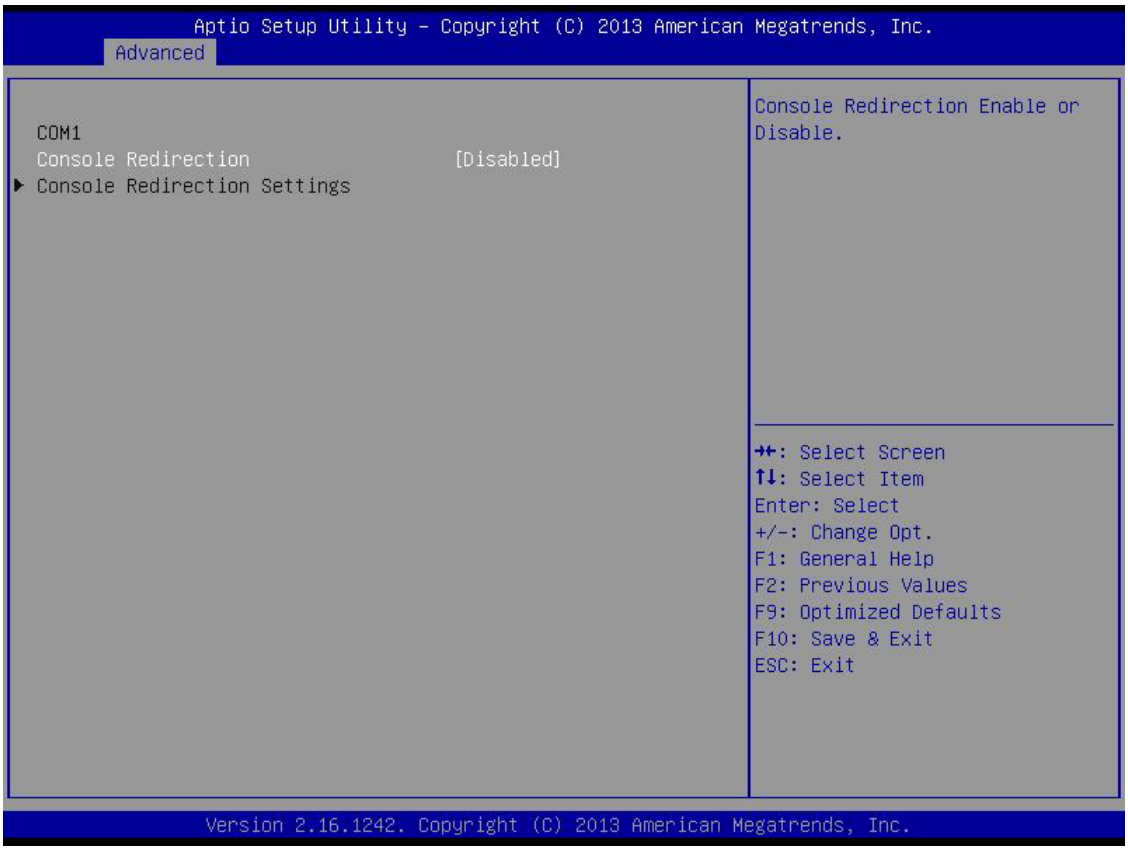


Figure 4-13: BIOS Setup Advanced Menu > Serial Port Console Redirection

Table 4-34: Advanced Menu > Serial Port Console Redirection

Feature	Options	Description
Console Redirection	• **Disabled** • Enabled	Console Redirection enable or disable.
Console Redirection Settings ►	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

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Advanced Menu > Serial Port Console Redirection > Console Redirection Settings

Table 4-35: Advanced Menu > Serial Port Console Redirection > Console Redirection Settings

Feature	Options	Description
• COM0/COM1 • Console Redirection Settings	Info only	
Terminal Type	• VT100 • VT100+ • VT-UTF8 • **ANSI**	VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes. ANSI: Extended ASCII char set.
Bits per second	• 9600 • 19200 • 38400 • 57600 • **115200**	Selects serial port transmission speed. The speed must be matched on the remote computer. Long or noisy lines may require lower speeds.
Data Bits	• 7 • **8**	Select data bits.
Parity	• **None** • Even • Odd • Mark • Space	Select parity.
Stop Bits	• **1** • 2	Select number of stop bits.
Flow Control	• **None** • Hardware RTS/CTS	Select flow control.
VT-UTF8 Combo Key Support	• Disabled • **Enable**	Enable VT-UTF8 combination key support for ANSI/VT100 terminals.
Recorder Mode	• **Disabled** • Enable	With this mode enabled only text will be sent. This is to capture terminal data.
Resolution 100x31	• **Disabled** • Enable	Enables or disables extended terminal resolution
Legacy OS Redirection	• **80x24** • 80x25	On legacy OSes, the number of rows and columns supported by redirection
Putty KeyPad	• **VT100** • LINUX • XTERMR6 • SCO • ESCN • VT400	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS Post	• **Always Enabled** • BootLoader	The Settings specify if BootLoader is selected, then legacy console redirection is disabled before booting to legacy OS. Default value is Always Enable which means legacy console redirection is enabled for legacy OS.

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Advanced Menu > Thermal

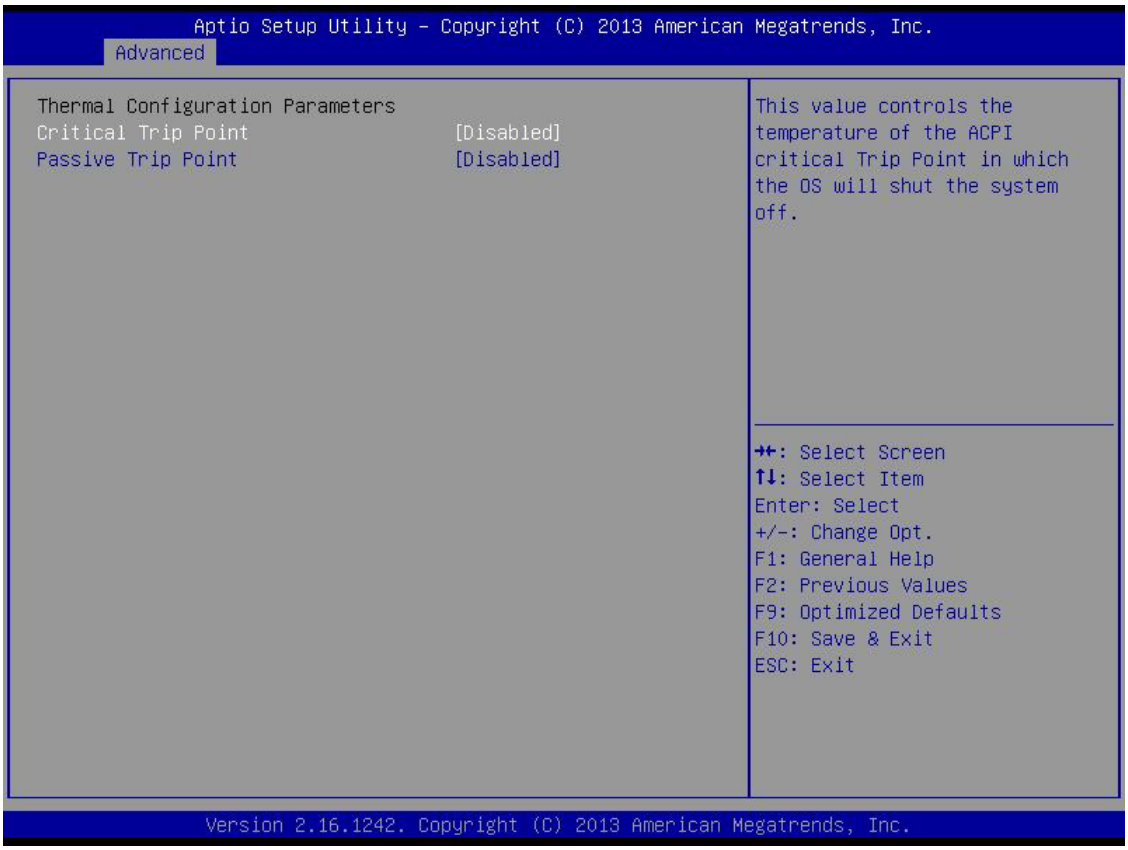


Figure 4-14: BIOS Setup Advanced Menu > Thermal

Table 4-36: Advanced Menu > Thermal

Feature	Options	Description
Critical Trip Point	• **Disabled** • 85 C • 95 C	This value controls the temperature of the ACPI critical Trip Point - the point at which the OS will shut the system down.
Passive Trip Point	• **Disabled** • 90 C • 80 C	This value controls the temperature of the ACPI passive Trip Point - the point at which the OS will begin throttling the processor.

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Advanced Menu > Security

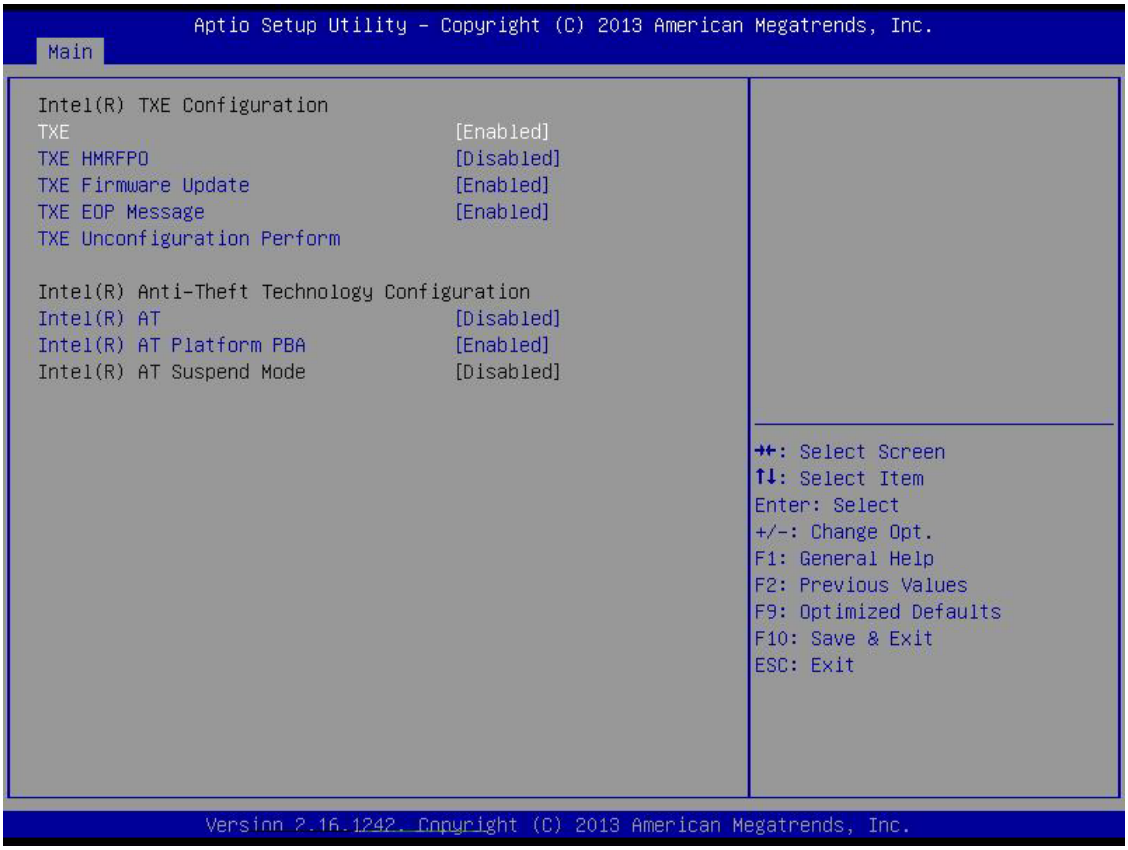


Figure 4-15: BIOS Setup Advanced Menu > Security

Table 4-37: Advanced Menu > Security

Feature	Options	Description
TXE	• **Enabled** • Disabled	
TXE HMRFPO	• Enabled • **Disabled**	
TXE Firmware Update	• **Enabled** • Disabled	
TXE EOP Message	• **Enabled** • Disabled	Send EOP Message Before Enter OS
TXE Unconfiguration Perform		Revert TXE settings to factory defaults
Intel(R) Anti-Theft Technology Configuration	Info only	
Intel(R) AT	• Enabled • **Disabled**	Enable/Disable BIOS AT Code from Runing
Intel(R) AT Platform PBA	• **Enabled** • Disabled	Enable/Disable BIOS AT Code from Runing
Intel(R) AT Suspend Mode	• **Disabled** • Enabled	Request that platform enter AT Suspend Mode - Only Available when AT Enrolled

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Advanced Menu > Miscellaneous

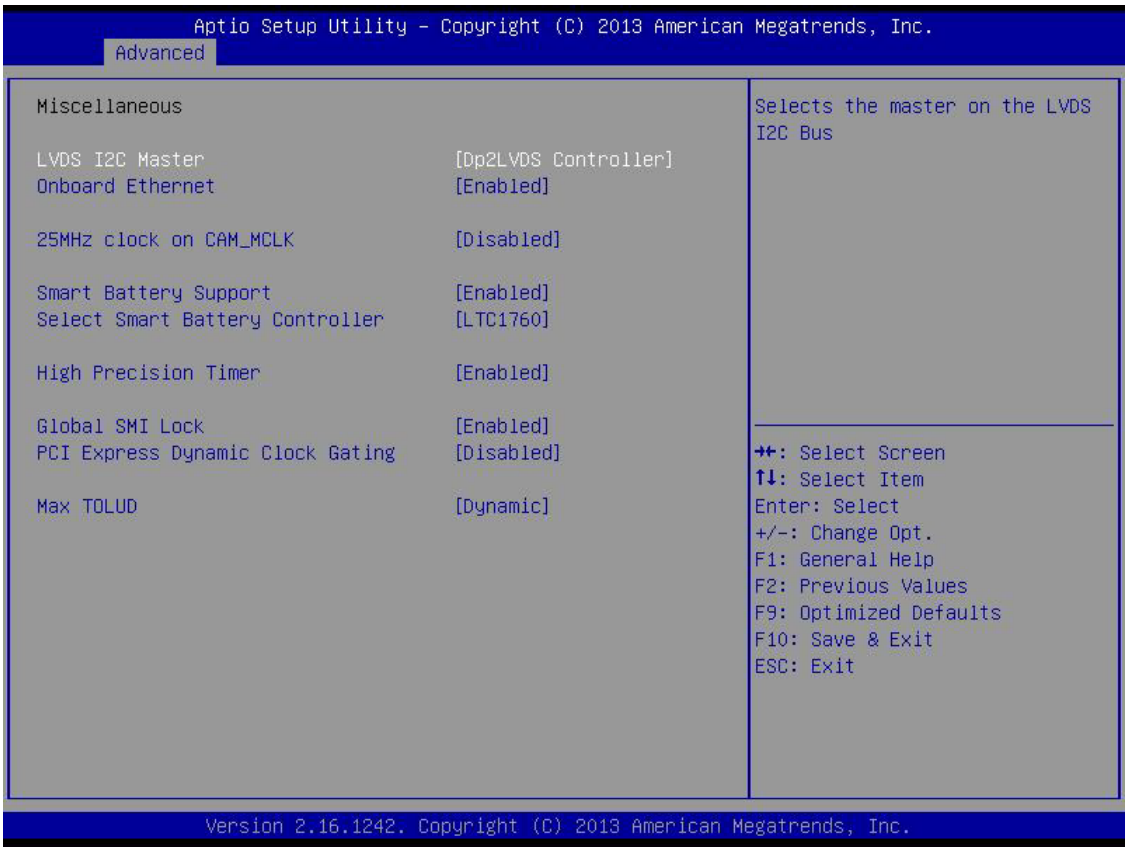


Figure 4-16: BIOS Setup Advanced Menu > Miscellaneous

Table 4-38: Advanced > Miscellaneous

Feature	Options	Description
LVDS I2C Master	• BMC Controller • **Dp2LVDS Controller**	Selects the master on the LVDS I2C Bus
Onboard Ethernet	• **Enabled** • Disabled	If Disabled: The onboard Ethernet controller is not available
25MHz clock on CAM_MCLK	• Enabled • **Disabled**	Enables a 25MHz clock output on SMARC CAM_MCLK
Smart Battery Support	• **Enabled** • Disabled	Enabled Smart Battery Support
Select Smart Battery Controller	• **LTC1760** • LTC4100	Select Smart Battery Controller
High Precision Timer	• **Enabled** • Disabled	Enable or disable the High Precision Event Timer
Global SMI Lock	• **Enabled** • Disabled	Enable or Disable SMI lock
PCI Express Dynamic Clock Gating	• Enabled • **Disabled**	Enable/Disable PCI Express Dynamic Clock Gating

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Table 4-38: Advanced > Miscellaneous (Continued)

Feature	Options	Description
Max TOLUD	• **Dynamic** • 2 GB • 2.25 GB • 2.5 GB • 2.75 GB • 3 GB	Maximum Value of TOLUD

4.1.4 Security Menu

The Security menu allows you to set User and Administrator system passwords and to retrieve secure boot information.

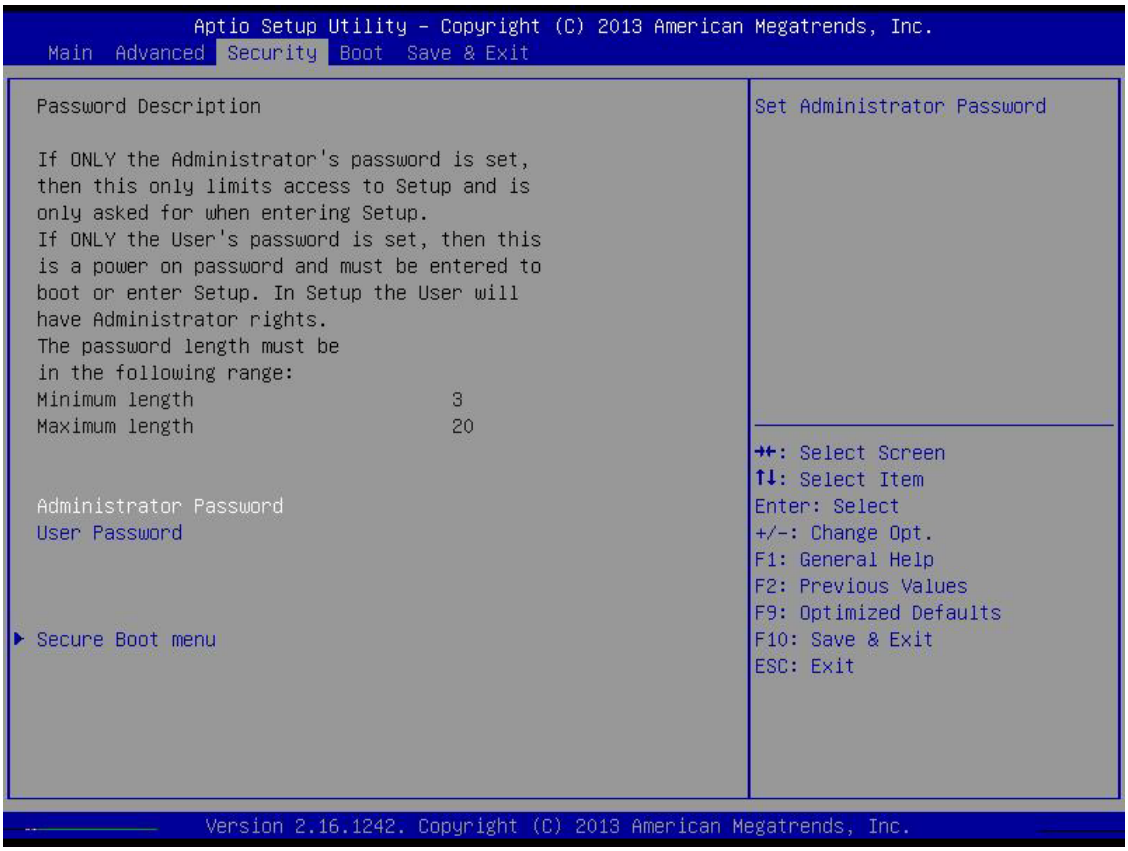


Figure 4-17: BIOS Setup Security Menu

Password Description

Table 4-39: Security Password

Feature	Options	Description
Administrator Password	Enter password	See description in Figure 4-17
User Password	Enter password	See description in Figure 4-17
Secure Boot menu ►	Submenu	Customizable Secure Boot settings.

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Security Menu > Secure Boot

Table 4-40: Security Menu > Secure Boot

Feature	Options	Description
System Mode	Setup	
Secure Boot	Info only	
Secure Boot	• **Enabled** • Disabled	Secure Boot can be enabled if: 1. System running in User mode with enrolled Platform Key (PK) 2. CSM function is disabled.
Secure Boot Mode	• **Standard** • Custom	Secure Boot mode selector. 'Custom' Mode enables users to change Image Execution policy and manage Secure Boot keys.

4.1.5 Boot

The Boot menu allows you to configure how your system will boot and select the storage location from which the system boot up will occur.

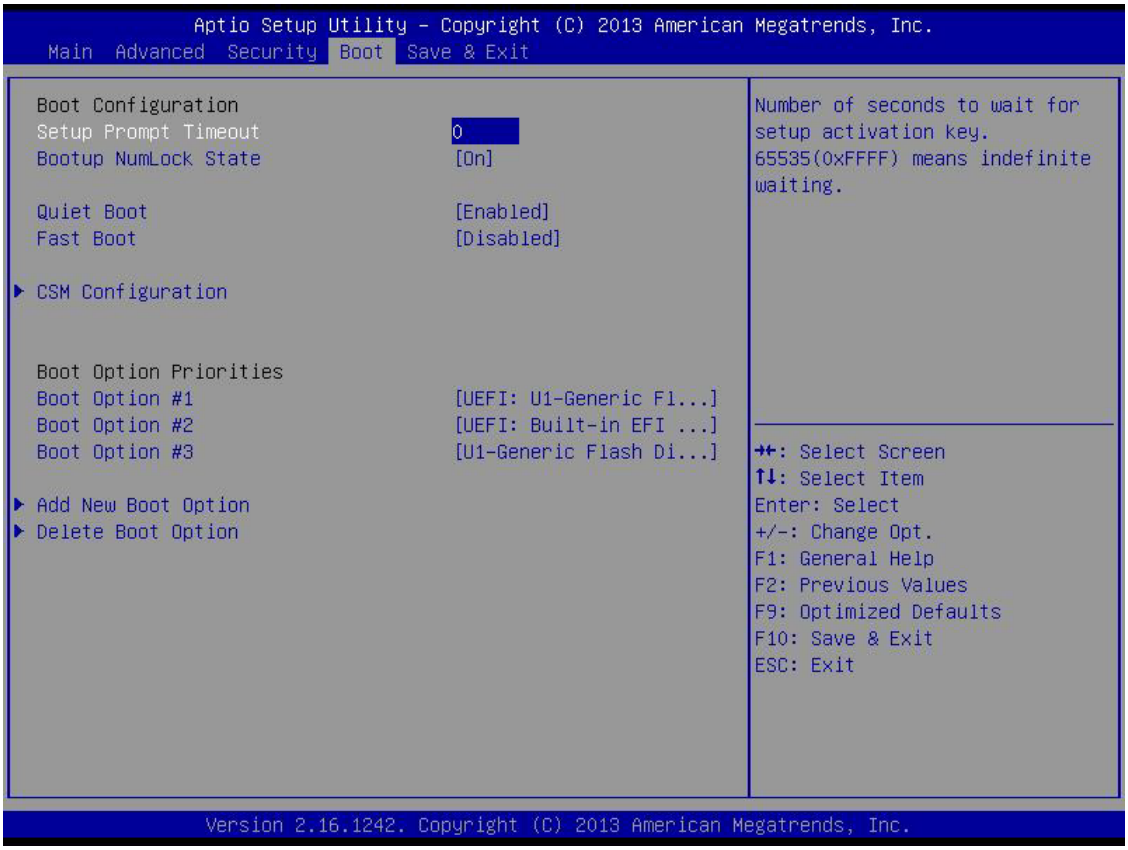


Figure 4-18: BIOS Setup Boot Menu

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Boot Configuration

If more than one drive is attached to the LEC-BTS, you can select from the “Boot Configuration” screen the boot order in which the drives are scanned for a bootable OS image.

Table 4-41: Boot Configuration

Feature	Options	Description
Setup Prompt Timeout	**0**	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
Bootup NumLock State	• **On** • Off	Select the keyboard NumLock state.
Quiet Boot	• **Enabled** • Disabled	Enable or disables logo Quiet Boot option for OEM Logo function.
Fast Boot	• **Disabled** • Enabled	Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect on BBS boot options.
CSM Configuration ►	Submenu	CSM configuration: Enable/Disable, Option ROM execution settings, etc.
Boot Option Priorities	Info only	
Hard Drive BBS Priorities	Info only	

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Boot Configuration > CSM Parameters

Table 4-42: Boot Configuration > CSM Parameters

Feature	Options	Description
Compatibility Support Module Configuration	Info	
CSM Support	• **Enabled** • Disable	CSM Support
CSM16 Module Version	Info only	
GataA20 Active	• **Upon Request** • Always	• Upon Request – GA20 can be disabled using BIOS services. • Always – do not allow disabling of GA20; this option is useful when any RT code is executed above 1MB.
Option ROM Messages	• Force BIOS • Keep Current	Set display mode for Option ROM.
INT19 Trap Response	• **Immediate** • Postponed	• BIOS reaction on INT19 trapping by Option ROM: • Immediate - execute the trap right away; Postponed – execute the trap during legacy boot.
Boot option filter	• **UEFI and Legacy** • Legacy only • UEFI only	This option controls legacy/UEFI ROM priority.
Option ROM execution	Info only	
Network	• **Do not launch** • UEFI only • Legacy only	Controls the execution of UEFI and legacy PXE OpROM.
Storage	• Do not launch • **UEFI only** • Legacy only	Controls the execution of UEFI and legacy storage OpROM.
Video	• UEFI only • **Legacy only**	Controls the execution of UEFI and legacy video OpROM.
Other PCI devices	• **UEFI only** • Legacy only	Determines OpROM execution policy for devices other than network, storage or video.

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4.1.6 Save & Exit

Use the Save and Exit menu to save or discard BIOS setting changes, restore or save setting defaults, and retrieve certain override information.

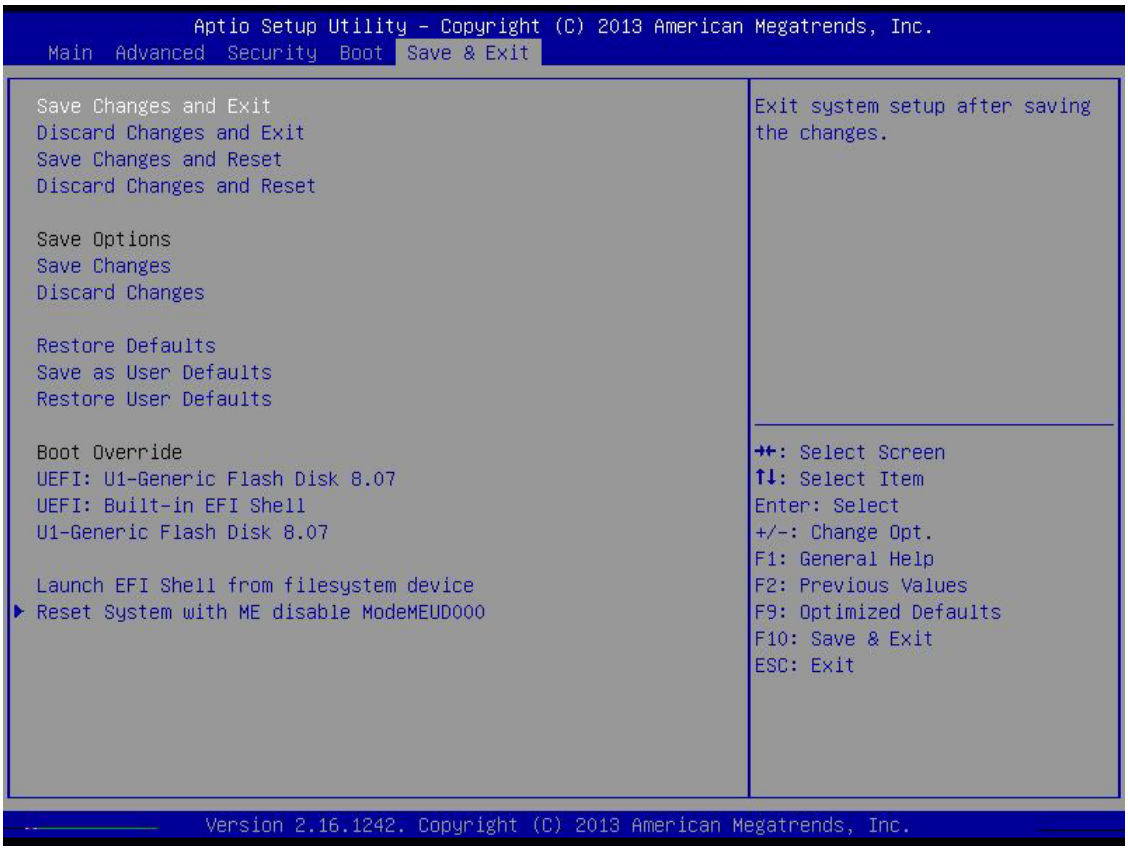


Figure 4-19: BIOS Setup Save and Exit Menu

Table 4-43: Save and Exit

Feature	Options	Description
Save Changes and Exit	Yes No	Exit system setup after saving the changes.
Discard Changes and Exit	Yes No	Exit system setup without saving any changes.
Save Changes and Reset	Yes No	Reset the system after saving the changes.
Discard Changes and Reset	Yes No	Reset system setup without saving any changes.
Save Options	Info only	
Save Changes	Yes No	Save Changes done so far to any of the setup options.
Discard Changes	Yes No	Discard Changes done so far to any of the setup options.
Restore Defaults	Yes No	Restore/Load Default values for all the setup options.
Save as User Defaults	Yes No	Save the changes done so far as User Defaults.
Restore User Defaults	Yes No	Restore the User Defaults to all the setup options.
Boot Override	Info only	

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4.2 SEMA functions

Under the management of the BMC chip (Board Management Controller), the SEMA utility (Smart Embedded Management Agent) provides system control and failure protection—counting, monitoring, and measuring hardware and software events, from which the SoC can trigger corrective commands. The optional SEMA Cloud utility not only controls local events on the module but system client events on the Internet of Things (IoT.) Refer to the following bullets for a list of SEMA functions.

- Total operating hours counter
  Counts the time the module has been run in minutes.
- On-time minutes counter
  Counts the seconds since last system start.
- Temperature monitoring of CPU and Board temperature
  Minimum and maximum temperature values of CPU and board are stored in flash.
- Power monitor
  Reads the current drawn by the board and reports the nominal operating voltage.
- Power cycles counter
- Boot counter
  Boot counter is increased after a HW- or SW-Reset or after a successful power-up.
- Watchdog Timer
  Set / Reset / Disable Watchdog Timer.
- System Restart Cause
  Power loss / Watchdog / External Reset.
- Flash area
  1kB Flash area for customer data
- Protected Flash area
  128 Bytes for Keys, ID's, etc. can be stored in a write- and clear-protectable region.
- Board Identify
  Vendor / Board / Serial number

The SEMA Tools are available for Windows and Linux. SEMA functionality can also be used in applications. Refer to the SEMA software manual and technical manual on the ADLINK web site for more information.

4.2.1 Board Specific SEMA functions

Voltages

The BMC of the LEC-BTS implements a Voltage Monitor and samples several Onboard Voltages. The Voltages can be read by calling the SEMA function, “Get Voltages”. The function returns a 16-bit value divided in Hi-Byte (MSB) and Lo-Byte (LSB).

Table 4-44: BMC Voltage Monitor Values

ADC Channel	Voltage Name	Voltage Formula [V]
0	---	---
1	+V1.0S	(MSB<<8 + LSB) * 3.3 / 1024
2	+V1.2S	(MSB<<8 + LSB) * 3.3 / 1024
3	+V1.8S	(MSB<<8 + LSB) * 3.3 / 1024
4	+V3.3S	(MSB<<8 + LSB) * 1.100 * 3.3 / 1024
5	+V1.5S	(MSB<<8 + LSB) * 3.3 / 1024
6	+V5.0A	(MSB<<8 + LSB) * 1.833 * 3.3 / 1024
7	(MAINCURRENT)	Use Main Current Function

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Main Current

The BMC of the LEC-BTS implements a Current Monitor. The current can be read by calling the SEMA function “Get Main Current”. The function returns four 16-bit values divided in Hi-Byte (MSB) and Lo-Byte (LSB). These four values represent the last four currents drawn by the board. The values are sampled every 250ms. The order of the four values is NOT in relationship to time. The access to the BMC may increase the drawn current of the whole system. In this case, you still have three samples without the influence of the read access.

Main Current = (MSB_n<<8 + LSB_n) * 8.06mA

TS#-Events

TS# is activated by a temperature sensor when a device reaches its critical temperature and released when the device is back in its normal temperature range. This counter gives the user information about temperature or cooling issues. This counter is cleared when the system is removed from power. The LEC-BTS only monitors the board temperature and does not support TS#-Events.

Exception Blink Codes

In the case of an error, the BMC shows a blink code on the STATUS-LED (LED1). This error code is also reported by the BMC Flags register. The Exception Code is not stored in the Flash storage and is cleared when the power is removed. Therefore, the “Clear Exception Code”-Command is not supported.

Table 4-45: Blink Codes

Exception Blink Code	Error Message
0	NOERROR
2	NO_SUSCLK
3	NO_SLP_S5
4	NO_SLP_S3
5	RESET_FAIL
6	
7	POWER_FAIL
8	LOW_VIN
9	NO_PWRGD_ATX
10	NO_PWRGD_1V0S
11	NO_PWRGD_1V2S
13	NO_PWRGD_1V8S
14	NO_PWRGD_3V3S
15	NO_PWRGD_1V5S

BMC Flags

The BMC Flags register returns the last detected exception code since power up.

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4.3 Watchdog Timer

The LEC-BTS features three separate Watchdog Timers. One of them is integrated in the SoC and two are provided by the BMC (managed by the SEMA).

The SoC Watchdog can be configured in the BIOS or by programming the Watchdog registers. If this function is used by user application, the application has to provide all logging functionality if desired.

The BMC Watchdog activations are caused by under voltage protection. The Watchdog LED flashes after restart but only if the power supply reaches 4.2V.

4.4 Temperature Sensors

The LEC-BTS supports two temperature sensor functions. One is offered from the SoC and one from a dedicated chip (Texas Instruments LM73) on the board.

The SoC temperature sensors can be configured by programming the appropriate SoC registers. Refer to the Thermal Management chapter in the Atom E3800 Intel processor data sheet for more information. The on-board LM73 temperature sensor is managed by the BMC and is configured through the SEMA utility.

4.5 Programming Examples

Programming examples can be provided based on a Linux operating system, upon request.

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Appendix A Technical Support

ADLINK Technology, Inc. provides a number of methods for contacting Technical Support listed in Table A-1 below. Requests for support through Ask an Expert are given the highest priorities, and usually will be addressed within one working day.

- ADLINK Ask an Expert – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the ADLINK web site at **http://askanexpert.adlinktech.com**. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online if you wish to use the Ask a Question feature.

ADLINK strongly suggests that you register with the web site. By creating a profile on the ADLINK web site, you will have a portal page called “My ADLINK”, unique to you with access to exclusive services and account information.

- Personal Assistance – You may also request personal assistance by creating an Ask an Expert account and then going to the Ask a Question feature. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request, you must log in to go to the My Question area where you can check status, update your request, and access other features.
- Download Service – This service is also free and available 24 hours a day using the web site link shown in Table A-1. For certain downloads such as technical documents and software, you must register online before you can log in to this service.

Table A-1: Technical Support Contact Information

Method	Contact Information
Ask an Expert	**http://askanexpert.adlinktech.com**
Web Site	**https://emb.adlinktech.com**
Standard Mail	**ADLINK Technology, Inc.** Address: 9F, No.166 Jian Yi Road, Zhonghe District New Taipei City 235, Taiwan 新北市中和區建一路 166 號 9 樓 Tel: +886-2-8226-5877 Fax: +886-2-8226-5717 Email: service@adlinktech.com **Ampro ADLINK Technology, Inc.** Address: 5215 Hellyer Avenue, #110 San Jose, CA 95138, USA Tel: +1-408-360-0200 Toll Free: +1-800-966-5200 (USA only) Fax: +1-408-360-0222 Email: info@adlinktech.com **ADLINK Technology (China) Co., Ltd.** Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203) 300 Fang Chun Rd., Zhangjiang Hi-Tech Park Pudong New Area, Shanghai, 201203 China Tel: +86-21-5132-8988 Fax: +86-21-5132-3588 Email: market@adlinktech.com

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Table A-1: Technical Support Contact Information (Continued)

Method	Contact Information
	ADLINK Technology GmbH Address: Hans-Thoma-Strasse 11 D-68163 Mannheim, Germany Tel: +49-621-43214-0 Fax: +49-621 43214-30 Email: emea@adlinktech.com Please visit the contact page using the web site link shown above or information on how to contact the ADLINK regional office nearest you.

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