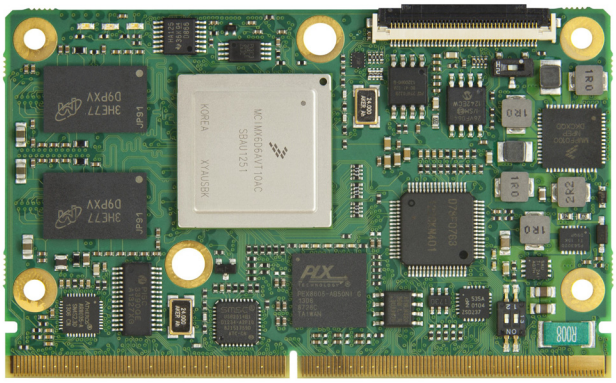
LEC-iMX6

(Low Energy Computer on Module)

Technical Reference

P/N 50-1Z167-1010

Rev 2.00



STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

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Preface

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Revision History

Revision	Reason for Change	Date
1.0	Initial Release	Jan/16
2.00	Revised camera signals in Table 4-1 on page 17; revised block diagram; other minor revisions	Jan/16

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Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

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Environmental Responsibility

ADLINK is committed to fulfill its social responsibility to global environmental preservation through compliance with the European Union's Restriction of Hazardous Substances (RoHS) directive and Waste Electrical and Electronic Equipment (WEEE) directive. Environmental protection is a top priority for ADLINK. We have enforced measures to ensure that our products, manufacturing processes, components, and raw materials have as little impact on the environment as possible. When products are at their end of life, our customers are encouraged to dispose of them in accordance with the product disposal and/or recovery programs prescribed by their nation or company.

Important Safety Instructions

For user safety, please read and follow all **Instructions**, **WARNINGs**, **CAUTIONs,** and **NOTEs** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,

If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

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1 Overview

This initial manual version presents a general overview of the LEC-iMX6. After reviewing this document you should understand the following features of the LEC-iMX6.

- Functional Block Diagram
- Major Components (ICs) and Connectors (Locations and Descriptions)
- Specifications
- Boot Up Configuration
- Interface Signal and Power Management Definitions

NOTE: Please refer to BSP readme documents in the Quick Drive for BSP installation instructions.

1.1 Block Diagram

Figure 1-1 represents the component functions of the module.

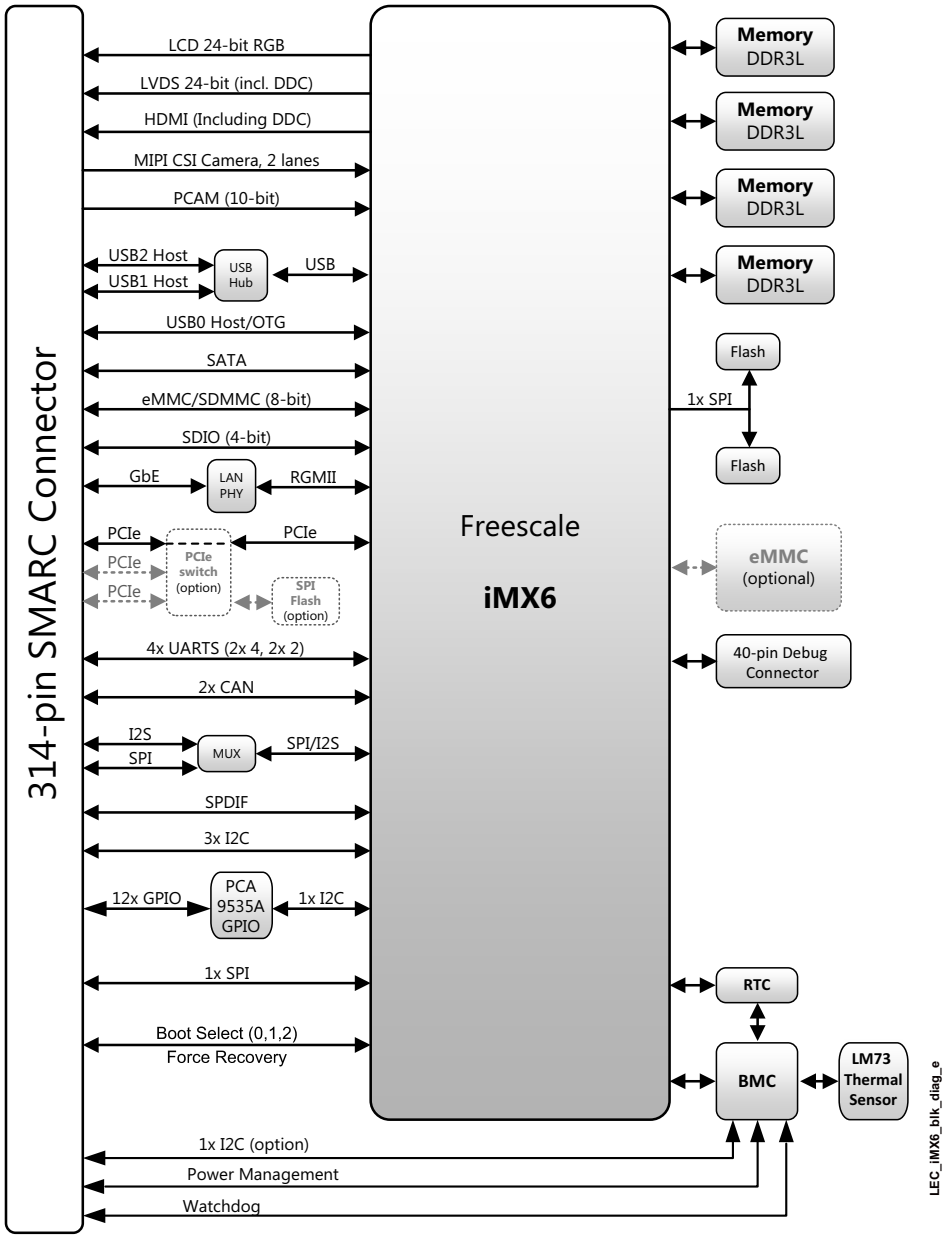


Figure 1-1: Functional Block Diagram

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1.2 Major Components (ICs)

Table 1-1 lists the major integrated circuits on the LEC-iMX6, including a brief description of each IC. Figure 1-2 and Figure 1-3 show the locations of the major ICs.

Table 1-1: Major Integrated Circuit Descriptions and Functions

Chip Type	Mfg.	Model	Description	Function
CPU (U1)	Freescale Semiconductor	• i.MX 6Solo (one core, no SATA) • i.MX 6Dual (two cores, SATA) • i.MX 6DualLite (two cores, no SATA) • i.MX 6Quad (four cores, SATA)	800 MHz, ARM Cortex-A9, 40nm SoC (System on Chip)	Integrates Processor Core, Graphics and Memory Controller Hub, and I/O Hub
DDR3L SDRAM (U7, U8, U9, U10 [U8 and U10 on bottom side])	Micron	MT41K256M16HA	On-board DDR3L, 1.35V, 4Gb, 32Mx16x8 System Memory	Provides high-speed data transfer
Ethernet PHY Transceiver (U11)	Atheros	AR8035-AL1B-R	Integrated 10/100/ 1000 Mbps single-port, tri-speed Ethernet PHY Transceiver	Provides a standard IEEE 802.3 Ethernet interface for Ethernet transfer rates up to 400Mbps
eMMC, NAND Flash (U16 - on bottom side)	Micron	MTFC8GLDEA-4M-IT	MultiMediaCard Controller and NAND Flash Memory up to 64GB	Provides communication and mass data storage capabilities

Key:
U1 - CPU
U7 - DDR3L SDRAM
U9 - DDR3L SDRAM
U11 - Ethernet Controller
▲ - Pin 1

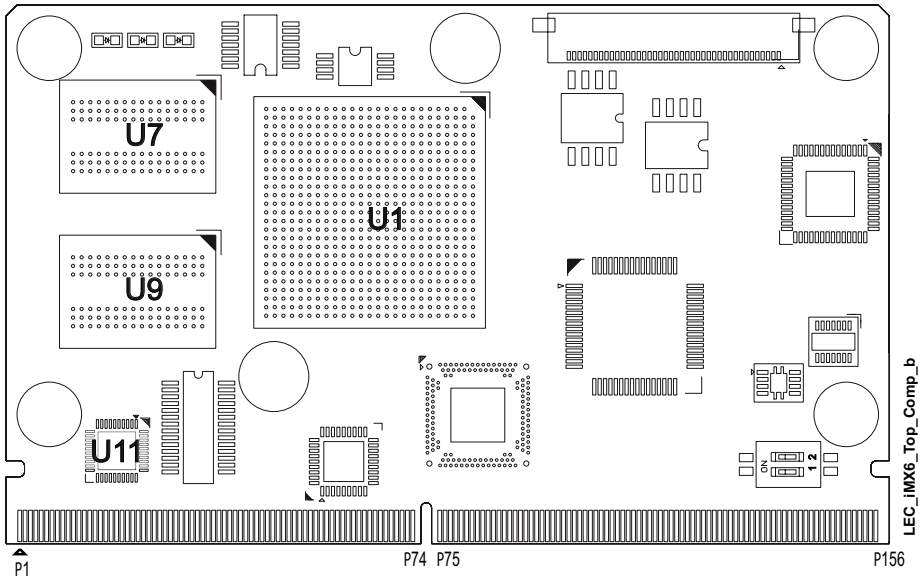


Figure 1-2: Component Locations (Top Side)

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Key:
U8 - DDR3L SDRAM
U10 - DDR3L SDRAM
U16 - eMMC, NAND Flash
▲ - Pin 1

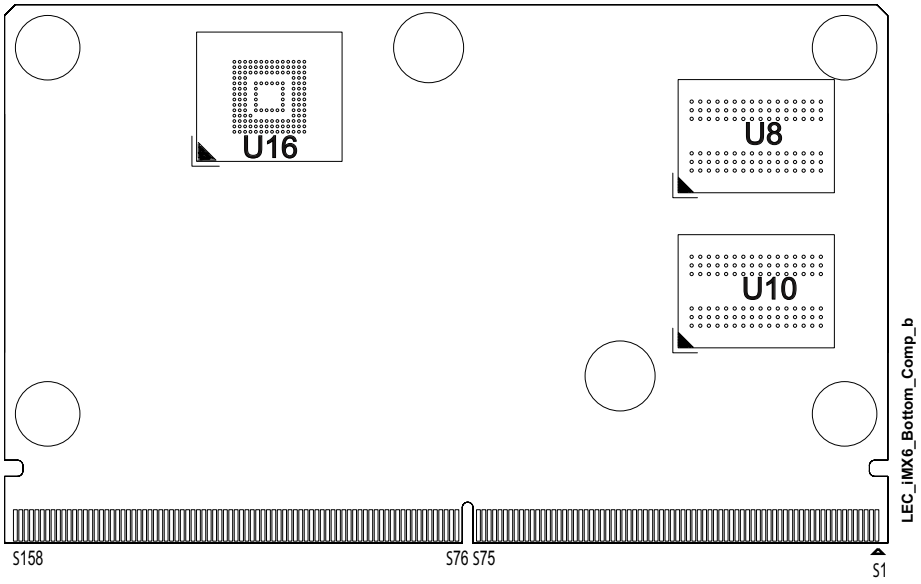
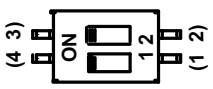


Figure 1-3: Component Locations (Bottom Side)

1.3 Connectors, LEDs, and Switches

Table 1-2 describes the connectors, LEDs, and switches shown in Figure 1-4.

Table 1-2: Module Connector, LED, and Switch Descriptions

Connector, LED, Switch #	Board Access	Description
J1 – SMARC P-S	Top/ Bottom	314-pin, MXM edge connector for Camera, Display, and I/O functions.
CN2	Top	40-pin connector for debug card
LED1	Top	Blue LED indicating system status activities for HW Reset, SW Reset, Power Up, Power Down, Reset Button, Power Button, and U-Boot_Select
LED2	Top	Green LED for Power On
LED3	Top	Red LED for Watchdog Activity
SW1	Top	4-pin dip switch for: • U-BOOT_SELECT: 1=off, 4=on [default] 1 = 4MB SPI Flash with U-BOOT+Debian installer 4 = 8MB SPI Flash with U-BOOT [default] • WDT Disable: 2=off, 3=on [default] 

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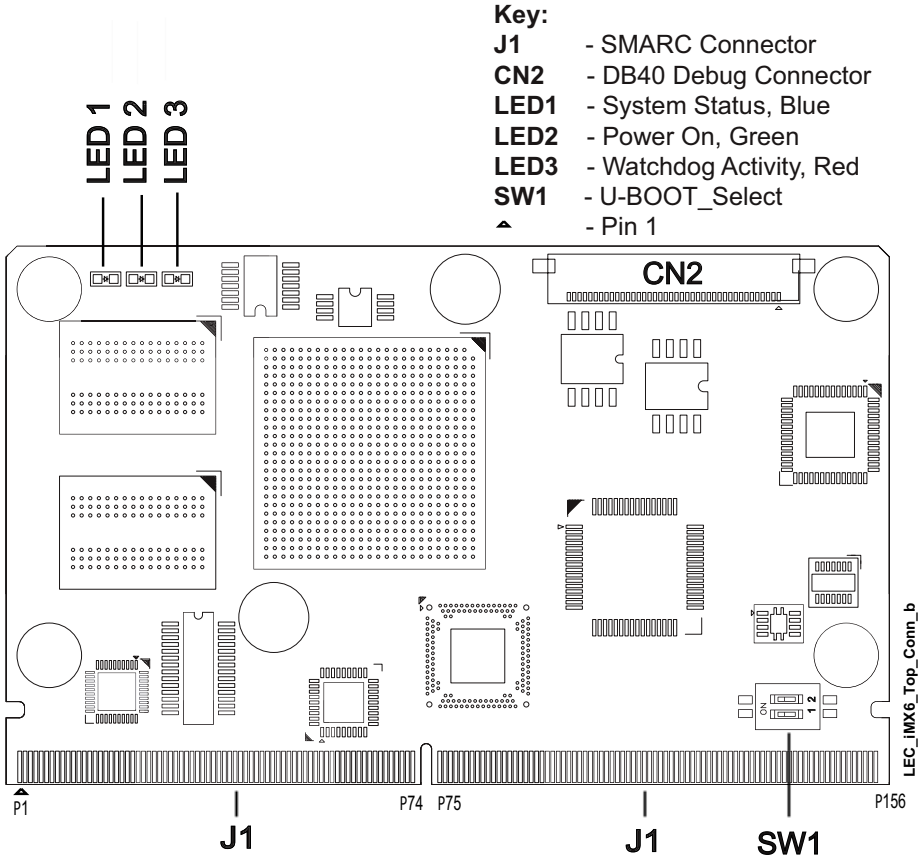


Figure 1-4: Connector, LED, and Switch Locations (Top Side)

1.4 Specifications

1.4.1 Physical Specifications

Table 1-3 lists the physical dimensions of the module.

Table 1-3: Weight and Footprint Dimensions

Item	Dimension	
Weight	0.02 kg (0.05 lb)	Overall height is measured from the upper board surface to the top of the highest permanent component (CN2 connector) on the upper board surface. This measurement does not include the cooling solution, which can vary. The cooling solution will probably increase this dimension.
Height (overall)	3.05 mm (0.12 inches)	
Board thickness	1.27 mm (0.05 inches)	
Width	50.00 mm (1.97 inches)	
Length	82.00 mm (3.23 inches)	

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1.4.2 Mechanical Specifications

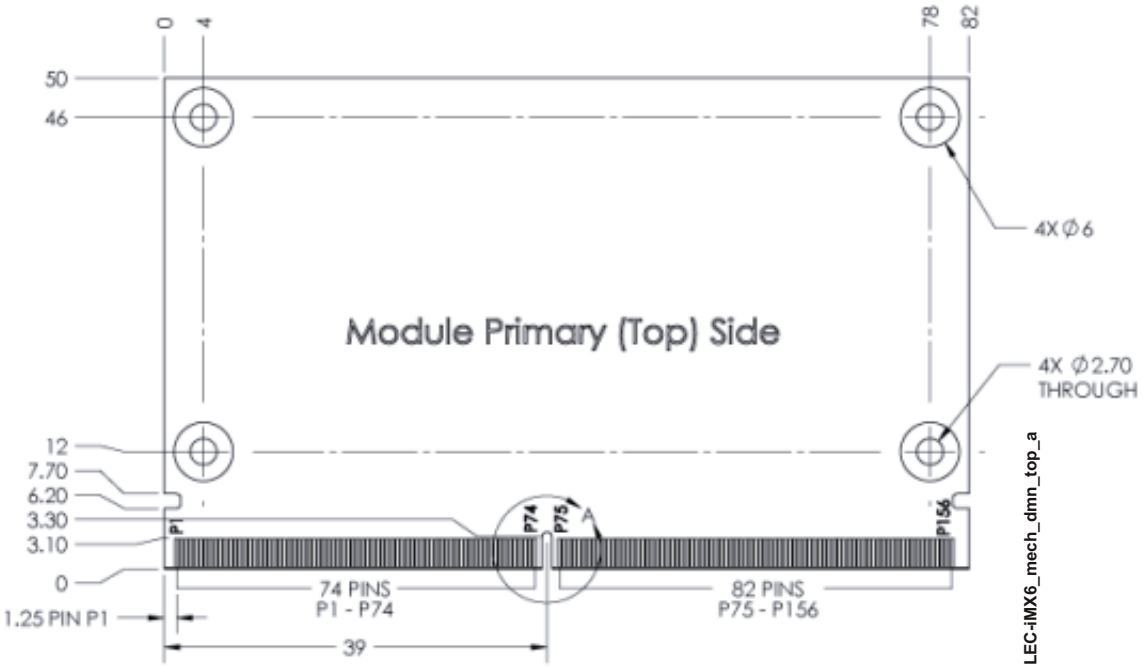


Figure 1-5: Mechanical Dimensions (Top Side)

NOTE: All dimensions are given in millimeters.

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1.4.3 Power Specifications

Table 1-4 provides the power requirements for this module.

Table 1-4: Power Supply Requirements

Parameter	800MHz Characteristics
Input Type	+3V to +5.25V Regulated DC voltage
In-rush Current	@5V: • Solo: 443mA • Dual Lite: 456mA • Dual: 794mA • Quad: 813mA
Typical Idle Current	@ 5V: • Dual: 337mA • Quad: 362mA
BIT (Burn-In Test) Current	@5V: Solo: 509mA Dual Lite: 524mA Dual: 902mA Quad: 907mA

Operating configurations:

- In-rush operating configuration - Typical
- Idle operating configuration - Typical
- BIT operating configuration - Typical

1.4.4 Environmental Specifications

Table 1-5 provides the most efficient operating and storage condition ranges required for this module.

Table 1-5: Environmental Requirements

Parameter	Conditions
Temperature	
Extended	–40° to +85° C (–40° to +185° F)
Storage	–55° to +85° C (–67° to +185° F)
Humidity	
Operating	5% to 90% relative humidity, non-condensing
Non-operating	5% to 95% relative humidity, non-condensing

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1.4.5 Thermal/Cooling Requirements

The LEC-iMX6 is designed to operate at its maximum CPU speed and requires a thermal solution. ADLINK offers one cooling option described in Table 1-6.

> CAUTION: The optional heat spreader plate requires another form of cooling, such as a fan. A heat spreader plate is not a complete thermal solution for the LEC-iMX6.

> CAUTION: The overall system design must keep the ICs within their operating temperature specifications.

Table 1-6: ADLINK Optional Cooling Option

Option	Description
Heat Spreader	Provides a simple thermal platform on which to build a cooling solution. The heat spreader is available as an optional order item.

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1.5 Getting Started

This section describes how to configure the boot select jumpers on the LEC-BASE baseboard and how to configure U-Boot to run a Linux image.

1.5.1 Configure boot select jumpers

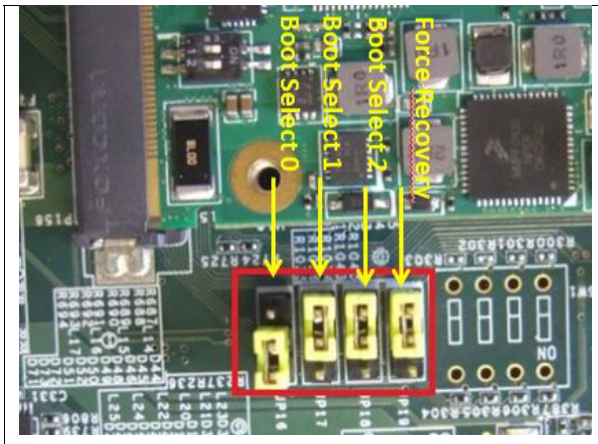
Before starting up the LEC-iMX6, the boot select jumpers on the LEC-BASE baseboard must be configured to correspond with the storage location of the U-Boot boot loader. This section also discusses boot requirements for the Operating System.

Before you boot your system, consider the storage locations of the following software:

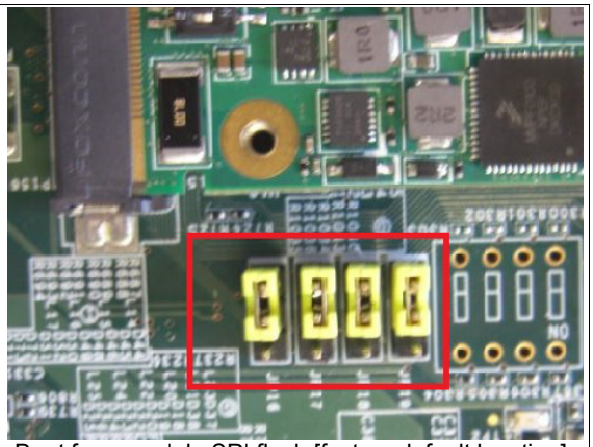
- U-Boot boot loader (the factory default location is the onboard SPI flash)
- Linux Operating System

The storage locations (devices) of these two software packages can be the same or distinct.

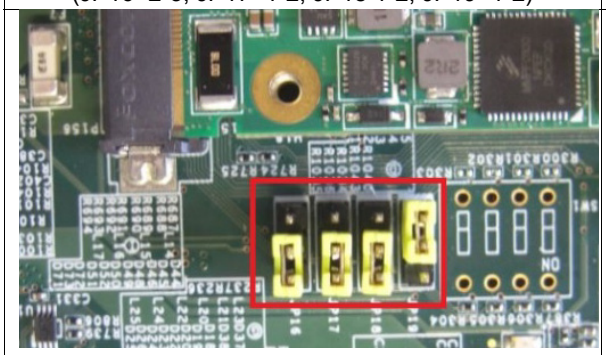
1. To boot the system from a specific boot device (location of the U-Boot boot loader), the LEC-BASE boot select jumpers must be set as shown in the following photos.



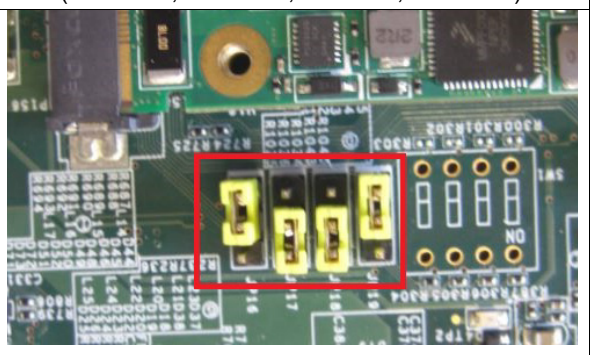
Boot from module eMMC
(JP16=2-3; JP17=1-2; JP18 1-2; JP19=1-2)



Boot from module SPI flash [factory default location]
(JP16=1-2; JP17=1-2; JP18 1-2; JP19=1-2)



Boot from carrier SATA disk
(JP16=2-3; JP17=2-3; JP18 2-3; JP19=1-2)



Boot from carrier SD card
(JP16=1-2; JP17=2-3; JP18 2-3; JP19=1-2)

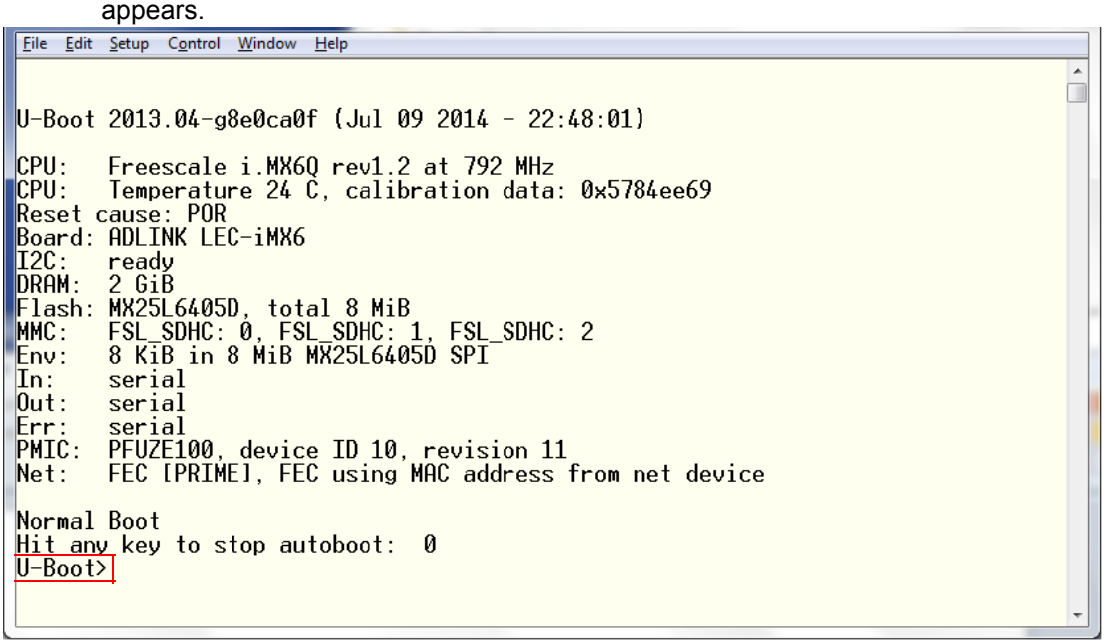
2. The storage location of the **Operating System** can be set during boot up through a U-Boot command entry. Otherwise, the default setting will be used.

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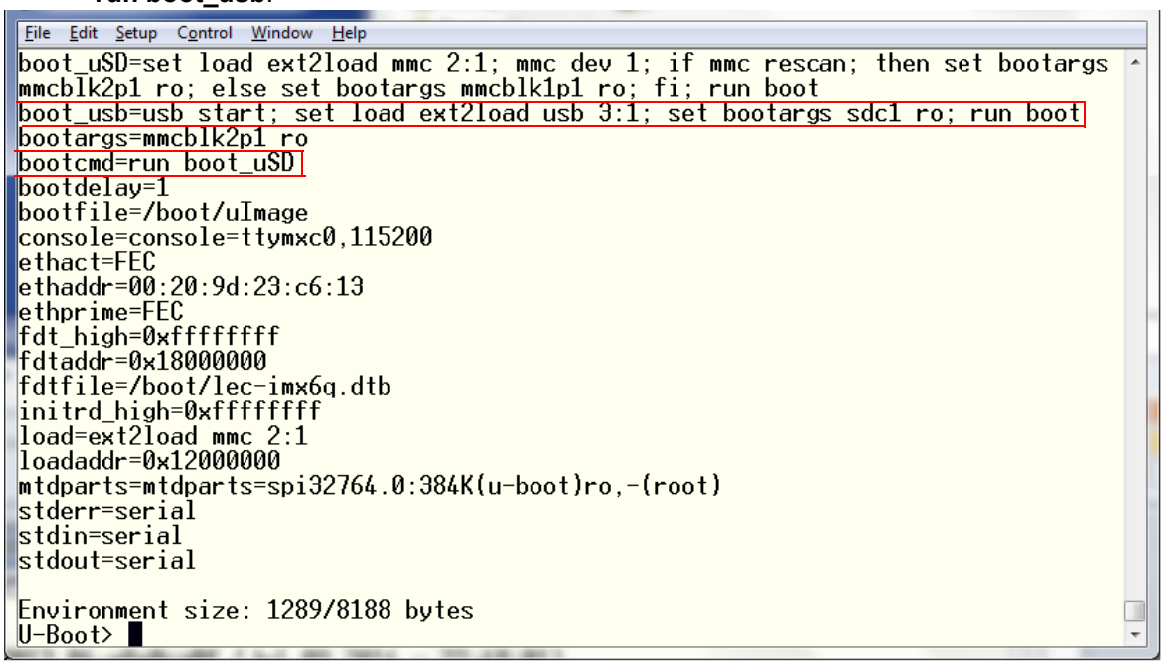
1.5.2 Verify U-Boot Configuration

To ensure U-Boot will run a Linux image from the corresponding boot device, perform the following steps.

1. Make a serial connection between the COM1 port of the LEC-iMX6 target and a host computer.
2. Open a terminal program with settings 115200 Baud, 8N1. The following screen appears.



3. Press any key to interrupt and open the U-Boot command shell.
4. Enter **pri** at the **U-Boot>** command line to list all environmental variables set inside U-Boot.
5. Find the appropriate variable and run the corresponding start command. For example: **run boot_usb**.



6. To run Linux from USB by default, edit **bootcmd** using:

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- **edit bootcmd**
- **run boot_usb**
- **save**

Note: You need to enter "**save**" after making a change, or the new setting will be lost after the next boot.

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2 Hardware

2.1 CPU

The LEC-iMX6 product family offers four standard models of the Freescale™ i.MX6 CPU: the i.MX 6Solo (1 core, 2 displays, no SATA), the i.MX 6Dual (2 cores, 3 displays, SATA), the i.MX 6DualLite (2 cores, 2 displays, no SATA), and the i.MX 6Quad (4 cores, 3 displays, SATA). LEC-iMX6 CPUs feature 32-bit ARM Cortex-A9 processor cores built on 40-nanometer process technology. The CPUs are designed for one-chip platforms, all using the same package, and are pin compatible. Refer to the CPU data sheet and reference manual at:
http://www.freescale.com/webapp/sps/site/taxonomy.jsp?code=IMX6X_SERIES.

2.2 Memory

The LEC-iMX6 employs one channel of 64-bit DDR3L on-board memory. Four SDRAM memory chips provide up to 32Gb of non-ECC, unbuffered, low voltage system memory. Refer to the SDRAM datasheet at:
http://www.micron.com/parts/dram/ddr3-sdram/mt41k256m16ha-125-it

2.3 eMMC NAND Flash

The module supports an optional on-board eMMC (Multi-Media Card) NAND chip with capacity up to 64GB and can be used as the Boot device.The data signals are routed from the NAND chip through the SDMMC pins on the SMARC connector. If the optional eMMC NAND chip is present on the module, the eMMC interface will not be available for the baseboard on the SMARC connector. Refer to the NAND Flash datasheet at:
http://www.micron.com/parts/nand-flash/managed-nand/mtfc8gldea-4m-it

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3 Interfaces

This section provides descriptions of the interfaces and signals within the SMARC P-S (Primary-Secondary) connector. The SMARC P-S connector provides the following features:

- Parallel LCD
- LVDS
- HDMI
- Camera PCAM
- Camera MIPI-CSI
- PCIe
- Gb Ethernet
- USB 2.0 (Host and OTG)
- SATA
- I2C
- SPI
- Serial
- SPDIF
- I2S
- CAN
- SD/SDIO
- eMMC
- GPIO
- AFB (Alternate Function Block)
- Debug

NOTE: ADLINK Technology Inc. only supports the features/options tested and listed in this manual. The main chips used in the LEC-iMX6 may provide more features or options than are listed for the LEC-iMX6, but some of these features or options are not supported on the module and will not function as specified in the chip documentation.

3.1 Parallel LCD Video

The Parallel LCD interface on the LEC-iMX6 can be used in 18-Bit or 24-Bit modes at up to 225 Mpixels/sec.

The voltage level of the LCD interface is 1.8V.

The Parallel LCD interface uses the I2C interface from the i.MX 6. At the SMARC connector the signal names are I2C_LCD_CK and I2C_LCD_DAT. The I2C interface is also shared onboard with I2C_GP_CK and I2C_GP_DAT at the SMARC connector and with the PMIC I2C interface.

3.2 18/24 Bit LVDS LCD

The module routes single-channel LVDS output from the CPU through the following SMARC interface pins:

- 1 Clock pair (S134/S135)
- 4 Data pairs (S125/S126; S128/S129; S131/S132; S137/S138)

The LVDS port can support up to 165 Mpixels/sec and voltage levels of the LVDS specification.

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3.3 HDMI (High-Definition Multimedia Interface)

The HDMI port utilizes the following HDMI pins on the SMARC interface:

- 1 Clock pair (P101/P102)
- 3 Data pairs (P92/P93; P95/P96; P98/P99)
- Service signals (P104-P107)

The HDMI interface is compliant with HDMI 1.4, HDMI CTS 1.4a, DVI 1.0 (with DVI-to-HDMI adapter), and HDCP 1.4. The module supports Monitor Detection for plug and unplug detection.

The voltage level of the HDMI interface is 1.8V.

3.4 Camera PCAM

The Parallel Camera interface supports 10-Bit video with up to 240 MHz clock speed.

The voltage level of the PCAM interface is 1.8V.

3.5 Camera MIPI-CSI

The LEC-iMX6 brings out signals for an MIPI CSI-2 serial camera interface. This serial camera port supports up to 1000 Mbps/lane in 1/2-lane mode.

The voltage level of the MIPI CSI-2 interface complies with the MIPI CSI specification.

3.6 PCIe

The module supports a PCIe port x1 lane, Gen 2.0 from the CPU, providing up to 5 Gb/s bandwidth in each direction. An optional PCIe switch IC allows for three lanes of PCIe expansion and an optional SPI Flash. The i.MX 6 PCIe includes 3 Cores: Dual Mode core, Root Complex core, and Endpoint core.

The LEC-iMX6 PCIe configurations include the following options:

- 1x PCIe 1x Gen 2.0
- 3x PCIe 1x Gen 2.0 using the optional PCIe switch
- Service signals per lane:

PCIE_X_CKREQ#	PCIE_X_RST#	PCIE_X_PRSNT#

- One PCIe wake-up input signal:

PCIE_WAKE#	Input

3.7 Gigabit Ethernet

The LEC-iMX6 uses an Ethernet PHY, which is connected to the CPU Ethernet controller with an RGMII interface. The PHY circuitry provides a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-Te applications. The following bullets highlight the Ethernet interface:

- Operates on TCP/IP, UDP/IP, and ICMP/IP protocol data or on IP header only
- Supports IPv4 and IPv6

NOTE: The Ethernet throughput is limited to 400 Mbit/s by the Freescale SoC.

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3.8 USB 2.0 Ports

The LEC-iMX6 provides two host USB ports and one OTG port. The two host ports are provided from a 4-port USB HUB. All Ports are fully compliant with the *USB 2.0 Specification*.

3.9 SATA

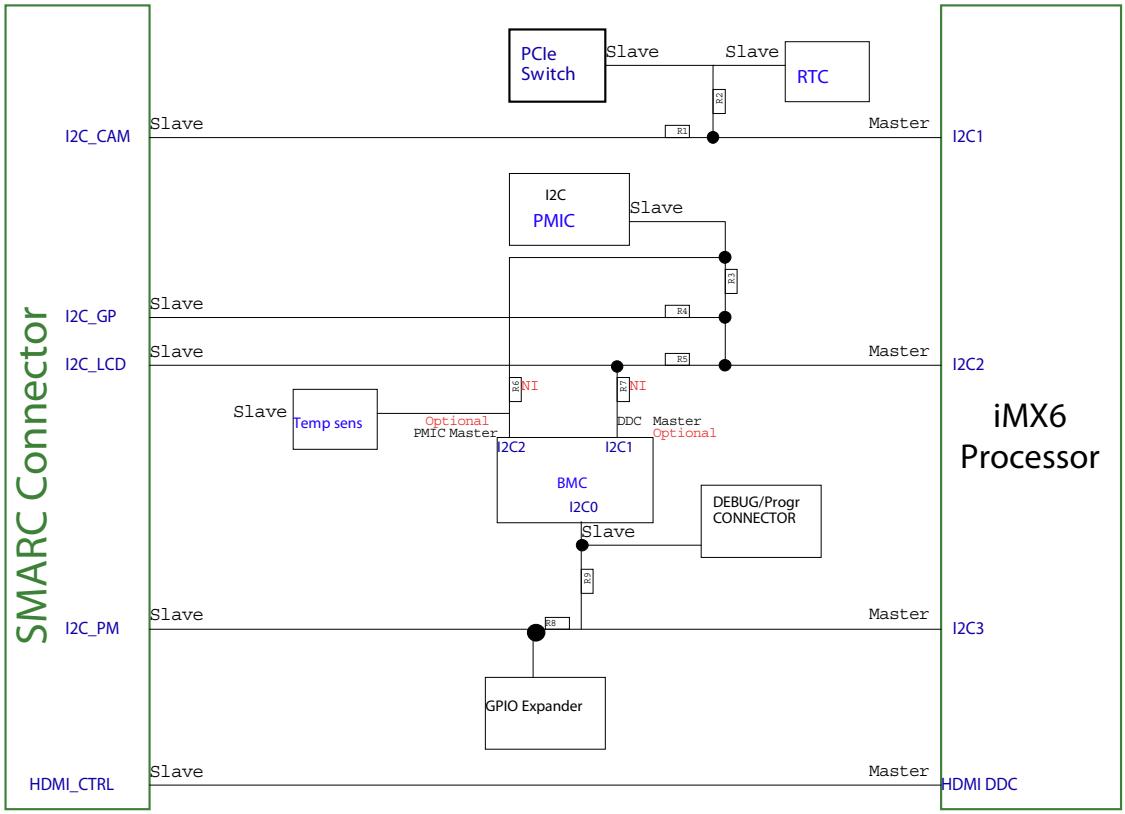
Only the Dual and Quad variants of the LEC-iMX6 module provide a SATA interface. The SATA interfaces on the Dual and Quad models comply with the following specifications.

- Serial ATA 3.0
- AHCI Revision 1.3
- AMBA 2.0 from ARM

The interface supports 1.5Gb/s and 3.0Gb/s.

3.10 I2C

The CPU provides three I2C master ports, and the SMARC connector provides five I2C slave ports for Camera, General Purpose, LCD, Power Management, and HDMI Control (private) interfaces. Refer to the following block diagram. The I2C interfaces operate at data rates up to 400 kbps. All I2C interfaces have 1.8V pull ups with 1k resistors.



3.11 SPI

The LEC-iMX6 provides three SPI interfaces. SPI0 is multiplexed with I2S and connected to the SMARC connector. SPI1 connects directly to the SMARC connector. The internal SPI interface connects to the U-Boot flash memory devices.

The voltage levels of the SPI interfaces are 1.8V.

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3.12 Serial (UART)

The LEC-iMX6 provides four serial interfaces: Two ports are high-speed, 4-wire ports (with TX/RX and RTS#/CTS#), and two ports are 2-wire (with TX/RX only.) Refer to the following table.

The voltage levels of the UART interfaces are 1.8V.

i.MX6	SMARC connector	Bus width
UART1	SER0	4 wire bus
UART2	SER1	2 wire bus
UART5	SER2	4 wire bus
UART4	SER3	2 wire bus

3.13 SPDIF

The Sony/Philips Digital Interconnect Format (SPDIF) audio block is a stereo transceiver that allows the processor to receive and transmit digital audio. Since the SPDIF internal data width is 24-bit, the eight most-significant bits of all registers return zeros. The SPDIF uses 2 wires, one data output, and one input.

The voltage level of the SPDIF interface is 1.8V

3.14 I2S

The LEC-iMX6 provides one I2S audio interface, and the signals are brought out through the I2S0 pins on the SMARC connector. The signals are shared with the SPI0 interface on the SMARC connector. The signal that allows switching between SPI and I2S is GPIO1_IO3. The default state is SPI (GPIO1_IO3 = low). When GPIO1_IO3 = high, I2S is switched through the SMARC connector.

The voltage level of the I2S interface is 1.8V

3.15 CAN

The LEC-iMX6 provides two CAN (FLEXCAN) interfaces that comply with the CAN 2.0B protocol specification. Two CAN bus transceivers reside on the CPU and are not required on the module. Refer to the following table for signal designators.

i.MX6	SMARC connector
FLEXCAN1	CAN0
FLEXCAN2	CAN1

The voltage level of the CAN interface is 1.8V

3.16 SD/SDIO Interface

Four parallel data lines comprise the SD/SDIO interface, supporting SD Card sockets. The LEC-iMX6 provides a 4-bit transfer mode at the SMARC connector using the SDIO pins and the SD2 interface of the i.MX 6 CPU. The following modes can be selected for data transfer:

- SD/SDIO full speed mode (up to 25 MHz)
- SD/SDIO high speed mode (up to 50 MHz)
- SD/SDIO UHS-I mode (up to 208 MHz in SDR mode, up to 50 Mhz in DDR mode)

The SDIO interface can be selected as the Boot Device. The voltage level of the SD/SDIO interface is 3.3V

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3.17 eMMC Interface

The LEC-iMX6 provides one onboard eMMC NAND Flash memory chip with a standard 8GB storage capacity (other optional storage capacities are available.) The eMMC interface has an 8-bit width and complies with the MMC system specification. The LEC-iMX6 supports a second 8-bit wide eMMC interface at the SMARC connector (pins S26-S33.)

3.18 GPIO

The LEC-iMX6 provides 12 GPIO signals. Seven signals (GPIO 4, 5, 6, 8, 9, 10, 11) are generated by the 9535A GPIO expander, and the remaining five signals (0, 1, 2, 3, and 7) originate from the iMX6 CPU and are designated for CAM0 and CAM1 (PWR and RST). The GPIO signals can be utilized for General Purpose IOs as well as camera enable pins and camera field input, as defined in the SMARC specification.

3.19 AFB Alternate Function Block

The AFB is used for an MLB (Media Local Bus) interface. The MLB is only supported in automotive and consumer parts.

3.20 LPC Debug

A 40-pin, front flip, DB40 connector allows access to debug and update the U-Boot boot loader, BMC, and OS code on the module. (Refer to “Debug (DB40)” on page 25.)

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4 Interface Signals

4.1 SMARC Interface

Table 4-1 provides the pin signals for the SMARC P-S connector. Refer to the SMARC specification at http://www.sget.org/standards/smarc.html for definitions of the SMARC signals.

Table 4-1: SMARC P-S Connector (J1) Signal Descriptions

Pin #	Primary (Top Side)	Pin #	Secondary (Bottom Side)
		S1	CSI0_VSYNC (Serial camera Vertical Sync input
P1	Not Connected	S2	CSI0_HSYNC (Parallel camera Horizontal Sync input)
P2	GND	S3	GND
P3	CSI1_CK+ (CSI1 differential clock input.)	S4	CSI0_PXL_CK0 (Serial camera primary pixel clock input)
P4	CSI1_CK- (CSI1 differential clock input.)	S5	I2C_CAM_CK (Serial / Parallel camera support link - I2C clock)
P5	PCAM_DE (Parallel camera Data Enable input)	S6	CAM_MCK (Master clock output for CSI camera support (may be used for CSI0 and / or CSI1)
P6	PCAM_MCK (Parallel camera Master Clock output)	S7	I2C_CAM_DAT (Serial / Parallel camera support link - I2C data)
P7	CSI1_D0+ (CSI1 differential data input.)	S8	CSI0_CK+(CSI0 differential clock input)
P8	CSI1_D0- (CSI1 differential data input.)	S9	CSI0_CK-(CSI0 differential clock input)
P9	GND	S10	GND
P10	CSI1_D1+ (CSI1 differential data input.)	S11	CSI0_D0+(CSI0 differential data input)
P11	CSI1_D1- (CSI1 differential data input.)	S12	CSI0_D0-(CSI0 differential data input)
P12	GND	S13	GND
P13	CSI1_D2+ (CSI1 differential data input.)	S14	CSI0_D1+(CSI0 differential data input)
P14	CSI1_D2- (CSI1 differential data input.)	S15	CSI0_D1-(CSI0 differential data input)
P15	GND	S16	GND
P16	CSI1_D3+ (CSI1 differential data input.)	S17	Not connected
P17	CSI1_D3- (CSI1 differential data input.)	S18	Not connected
P18	GND	S19	Not connected
P19	GBE_MDI3- (Bi-directional transmit/ receive pair 3 to magnetics [Media Dependent Interface])	S20	Not connected
P20	GBE_MDI3+ (Bi-directional transmit/ receive pair 3 to magnetics [Media Dependent Interface])	S21	Not connected
P21	GBE_LINK100# (Link Speed Indication LED for 100Mbps; able to sink 24mA or more carrier LED current)	S22	Not connected
P22	GBE_LINK1000# (Link Speed Indication LED for 1000Mbps; able to sink 24mA or more carrier LED current)	S23	Not connected
P23	GBE_MDI2- (Bi-directional transmit/ receive pair 2 to magnetics [Media Dependent Interface])	S24	Not connected

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Table 4-1: SMARC P-S Connector (J1) Signal Descriptions (Continued)

P24	GBE_MDI2+ (Bi-directional transmit/ receive pair 2 to magnetics [Media Dependent Interface])	S25	GND
P25	GBE_LINK_ACT# (Link / Activity Indication LED Driven low on Link [10, 100 or 1000 mbps] Blinks on Activity; able to sink 24mA or more Carrier LED current)	S26	SDMMC_D0 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P26	GBE_MDI1- (Bi-directional transmit/ receive pair 1 to magnetics [Media Dependent Interface])	S27	SDMMC_D1 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P27	GBE_MDI1+ (Bi-directional transmit/ receive pair 1 to magnetics [Media Dependent Interface])	S28	SDMMC_D2 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P28	GBE_CTREF (Center-Tap reference voltage for GBE0 Carrier board Ethernet magnetic [if required by the Module GBE PHY])	S29	SDMMC_D3 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P29	GBE0_MDI0- (Bi-directional transmit/ receive pair 0 to magnetics [Media Dependent Interface])	S30	SDMMC_D4 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P30	GBE0_MDI0+ (Bi-directional transmit/ receive pair 0 to magnetics [Media Dependent Interface])	S31	SDMMC_D5 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P31	SPI0_CS1# (SPI0 Master Chip Select 1 output)	S32	SDMMC_D6 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P32	GND	S33	SDMMC_D7 (bidirectional, 8-bit data path; ***may*** be used for 4- and 1-bit wide eMMC devices as well)
P33	SDIO_WP (SDIO card Write Protect; 10K pull-up to 3.3V)	S34	GND
P34	SDIO_CMD (SDIO card Command line)	S35	SDMMC_CK (clock)
P35	SDIO_CD# (SDIO Card Detect; 10K pull-up to 3.3V)	S36	SDMMC_CMD (command line)
P36	SDIO_CK (SDIO card Clock)	S37	SDMMC_RST# (Reset signal to eMMC device)
P37	SDIO_PWR_EN (SDIO card Power Enable)	S38	AUDIO_MCK (Master clock output to Audio codecs)
P38	GND	S39	I2S0_LRCK (Left& Right audio synchronization clock)
P39	SDIO_D0 (SDIO card 4-bit data path)	S40	I2S0_SDOUT (Digital audio Output)
P40	SDIO_D1 (SDIO card 4-bit data path)	S41	I2S0_SDIN (Digital audio Input)
P41	SDIO_D2 (SDIO card 4-bit data path)	S42	I2S0_CK (Digital audio clock)
P42	SDIO_D3 (SDIO card 4-bit data path)	S43	Not connected
P43	SPI0_CS0# (SPI0 Master Chip Select 0 output; use to select carrier SPI boot device)	S44	Not connected
P44	SPI0_CK (SPI0 Master Clock output)	S45	Not connected
P45	SPI0_DIN (SPI0 Master Data input [input to CPU, output from SPI device])	S46	Not connected
P46	SPI0_DO (SPI0 Master Data output [output from CPU, input to SPI device])	S47	GND

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Table 4-1: SMARC P-S Connector (J1) Signal Descriptions (Continued)

P47	GND	S48	I2C_GP_CK (I2C General Purpose clock signal)
P48	SATA0_TX+ (Differential SATA 0 transmit data Pair; 0.1 uF 0402 capacitor on module)	S49	I2C_GP_DAT (I2C General Purpose data signal)
P49	SATA0_TX- (Differential SATA 0 transmit data Pair; 0.1 uF 0402 capacitor on module)	S50	Not connected
P50	GND	S51	Not connected
P51	SATA_RX+ (Differential SATA 0 receive data Pair; 0.1 uF 0402 capacitor on module)	S52	Not connected
P52	SATA_RX- (Differential SATA 0 receive data Pair; 0.1 uF 0402 capacitor on module)	S53	Not connected
P53	GND	S54	Not connected
P54	SPI1_CS0# (SPI1 Master Chip Select 0 output)	S55	Not connected
P55	SPI1_CS1# (SPI1 Master Chip Select 1 output)	S56	Not connected
P56	SPI1_CK (SPI1 Master Clock output)	S57	Not connected
P57	SPI1_DIN (SPI1 Master Data input [input to CPU, output from SPI device])	S58	GND
P58	SPI1_DO (SPI1 Master Data output [output from CPU, input to SPI device])	S59	SPDIF_OUT (Digital Audio Output)
P59	GND	S60	SPDIF_IN (Digital Audio Input)
P60	USB0+ (Differential USB0 data pair)	S61	GND
P61	USB0- (Differential USB0 data pair)	S62	Not connected
P62	USB0_EN_OC# (Pulled low by Module OD driver to disable USB0power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up is present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.12.4 of *SMARC Specification.*)	S63	Not connected
P63	USB0_VBUS_DET (USB host power detection, when this port is used as a device.)	S64	GND
P64	USB0_OTG_ID (USB OTG ID input, active high)	S65	AFB_DIFF1+ (maps to MLB_CP [Media Local Bus_Clock Positive] on the SOC)
P65	USB1+ (Differential USB1 data pair)	S66	AFB_DIFF1- (maps to MLB_CN [Media Local Bus_Clock Negative] on the SOC)
P66	USB1- (Differential USB1 data pair)	S67	GND
P67	USB1_EN_OC# (Pulled low by Module OD driver to disable USB1 power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up is present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.12.4 of *SMARC Specification.*)	S68	AFB_DIFF2+ (maps to MLB_SP [Media Local Bus_Signal Positive] on the SOC)

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Table 4-1: SMARC P-S Connector (J1) Signal Descriptions (Continued)

P68	GND	S69	AFB_DIFF2- (maps to MLB_SN [Media Local Bus_Signal Negative] on the SOC)
P69	USB2+ (Differential USB2 data pair)	S70	GND
P70	USB2- (Differential USB2 data pair)	S71	AFB_DIFF3+ (maps to MLB_DP [Media Local Bus_Data Positive] on the SOC)
P71	USB2_EN_OC# (Pulled low by Module OD driver to disable USB2 power. Pulled low by Carrier OD driver to indicate over-current situation. A pull-up ***shall*** be present on the Module to a 3.3V rail. The pull-up rail ***may*** be switched off to conserve power if the USB port is not in use. Further details may be found in Section 4.12.4 of *SMARC Specification*.)	S72	AFB_DIFF3- (maps to MLB_DN [Media Local Bus_Data Negative] on the SOC)
P72	PCIE_C_PRSNT# (PCIe Port C present input. Pulled up or terminated on Module)	S73	GND
P73	PCIE_B_PRSNT# (PCIe Port B present input. Pulled up or terminated on Module)	S74	Not Connected
P74	PCIE_A_PRSNT# (PCIe Port A present input. Pulled up or terminated on Module)	S75	Not Connected
	Key		Key
P75	PCIE_A_RST# (PCIe Port A reset output)	S76	PCIE_B_RST# (PCIe Port B reset output, active low)
P76	PCIE_C_CKREQ# (PCIe Port C clock request input. Pulled up or terminated on Module)	S77	PCIE_C_RST# (PCIe Port A reset output, active low)
P77	PCIE_B_CKREQ# (PCIe Port B clock request input. Pulled up or terminated on Module)	S78	PCIE_C_RX+ (Differential PCIe Link C receive data pair 0. No coupling caps on Module)
P78	PCIE_A_CKREQ# (PCIe Port A clock request input. Pulled up or terminated on Module)	S79	PCIE_C_RX- (Differential PCIe Link C receive data pair 0. No coupling caps on Module)
P79	GND	S80	GND
P80	PCIE_C_REFCK+ (Differential PCIe Link C reference clock output. DC coupled)	S81	PCIE_C_TX+ (Differential PCIe Link C transmit data pair 0. Series coupling caps are on the Module. Caps are 0402 package 0.1uF)
P81	PCIE_C_REFCK- (Differential PCIe Link C reference clock output. DC coupled)	S82	PCIE_C_TX- (Differential PCIe Link C transmit data pair 0. Series coupling caps are on the Module. Caps are 0402 package 0.1uF)
P82	GND	S83	GND
P83	PCIE_A_REFCK+ (Differential PCIe Link A reference clock output. DC coupled)	S84	PCIE_B_REFCK+ (Differential PCIe Link B reference clock output; DC coupled)
P84	PCIE_A_REFCK- (Differential PCIe Link A reference clock output. DC coupled)	S85	PCIE_B_REFCK- (Differential PCIe Link B reference clock output; DC coupled)
P85	GND	S86	GND
P86	PCIE_A_RX+ (Differential PCIe Link A receive data pair 0. No coupling caps on Module)	S87	PCIE_B_RX+ (Differential PCIe Link B receive data pair 0. No coupling caps on Module)
P87	PCIE_A_RX- (Differential PCIe Link A receive data pair 0. No coupling caps on Module)	S88	PCIE_B_RX- (Differential PCIe Link B receive data pair 0. No coupling caps on Module)

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Table 4-1: SMARC P-S Connector (J1) Signal Descriptions (Continued)

P88	GND	S89	GND
P89	PCIE_A_TX+ (Differential PCIe Link A transmit data pair 0. Series coupling capacitors are on the Module. 0.1 uF 0402 capacitor are on module)	S90	PCIE_B_TX+ (Differential PCIe Link B transmit data pair 0. Series coupling caps are on the Module Caps are 0402 package 0.1uF)
P90	PCIE_A_TX- (Differential PCIe Link A transmit data pair 0. Series coupling capacitors are on the Module. 0.1 uF 0402 capacitor are on module)	P91	PCIE_B_TX- (Differential PCIe Link B transmit data pair 0. Series coupling caps are on the Module Caps are 0402 package 0.1uF)
P91	GND	S92	GND
P92	HDMI_D2+ (TMDS / HDMI data 2 differential pair)	S93	LCD_D0 (8-bit BLU color data - 18-bit display implementations leave the two LS bits (D0, D1) bit not connected)
P93	HDMI_D2- HDMI_D2- (TMDS / HDMI data 2 differential pair)	S94	LCD_D1 (8-bit BLU color data - 18-bit display implementations leave the two LS bits (D0, D1) bit not connected)
P94	GND	S95	LCD_D2 (8-bit BLU color data - 18-bit display implementations leave the two LS bits (D0, D1) bit not connected)
P95	HDMI_D1+ (TMDS / HDMI data 1 differential pair)	S96	LCD_D3 (8-bit BLU color data - 18-bit display implementations leave the two LS bits (D0, D1) bit not connected)
P96	HDMI_D1- (TMDS / HDMI data 1 differential pair)	S97	LCD_D4 (8-bit BLU color data - 18-bit display implementations leave the two LS bits (D0, D1) bit not connected)
P97	GND	S98	LCD_D5 (8-bit BLU color data - 18-bit display implementations leave the two LS bits (D0, D1) bit not connected)
P98	HDMI_D0+ (TMDS / HDMI data 0 differential pair)	S99	LCD_D6 (8-bit BLU color data - 18-bit display implementations leave the two LS bits (D0, D1) bit not connected)
P99	HDMI_D0- (TMDS / HDMI data 0 differential pair)	S100	LCD_D7 (8-bit BLU color data - 18-bit display implementations leave the two LS bits (D0, D1) bit not connected)
P100	GND	S101	GND
P101	HDMI_CK+ (TMDS / HDMI clock output differential pair)	S102	LCD_D8 (8-bit GRN color data - 18-bit display implementations leave the two LS bits (D8, D9) not connected)
P102	HDMI_CK- (TMDS / HDMI clock output differential pair)	S103	LCD_D9 (8-bit GRN color data - 18-bit display implementations leave the two LS bits (D8, D9) not connected)
P103	GND	S104	LCD_D10 (8-bit GRN color data - 18-bit display implementations leave the two LS bits (D8, D9) not connected)
P104	HDMI_HPD (HDMI Hot Plug Detect input)	S105	LCD_D11 (8-bit GRN color data - 18-bit display implementations leave the two LS bits (D8, D9) not connected)
P105	HDMI_CTRL_CK (I2C clock line dedicated to HDMI)	S106	LCD_D12 (8-bit GRN color data - 18-bit display implementations leave the two LS bits (D8, D9) not connected)
P106	HDMI_CTRL_DAT (I2C data line dedicated to HDMI)	S107	LCD_D13 (8-bit GRN color data - 18-bit display implementations leave the two LS bits (D8, D9) not connected)

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Table 4-1: SMARC P-S Connector (J1) Signal Descriptions (Continued)

P107	HDMI_CEC (Not Supported)	S108	LCD_D14 (8-bit GRN color data - 18-bit display implementations leave the two LS bits (D8, D9) not connected)
P108	CAM0_PWR# (Camera 0 Power Enable, active low output)	S109	LCD_D15 (8-bit GRN color data - 18-bit display implementations leave the two LS bits (D8, D9) not connected)
P109	CAM1_PWR# (Camera 1 Power Enable, active low output)	S110	GND
P110	CAM0_RST# (Camera 0 Reset, active low output)	S111	LCD_D16 (8-bit RED color data - 18-bit display implementations leave the two LS bits (D16, D17) not connected)
P111	CAM1_RST# (Camera 1 Reset, active low output)	S112	LCD_D17 (8-bit RED color data - 18-bit display implementations leave the two LS bits (D16, D17) not connected)
P112	GPIO4 (General Purpose IO)	S113	LCD_D18 (8-bit RED color data - 18-bit display implementations leave the two LS bits (D16, D17) not connected)
P113	GPIO5 (General Purpose IO)	S114	LCD_D19 (8-bit RED color data - 18-bit display implementations leave the two LS bits (D16, D17) not connected)
P114	GPIO6 (General Purpose IO)	S115	LCD_D20 (8-bit RED color data - 18-bit display implementations leave the two LS bits (D16, D17) not connected)
P115	PCAM_FLD (PCAM_FLD (Field) signal input)	S116	LCD_D21 (8-bit RED color data - 18-bit display implementations leave the two LS bits (D16, D17) not connected)
P116	GPIO8 (General Purpose IO)	S117	LCD_D22 (8-bit RED color data - 18-bit display implementations leave the two LS bits (D16, D17) not connected)
P117	GPIO9 (General Purpose IO)	S118	LCD_D23 (8-bit RED color data - 18-bit display implementations leave the two LS bits (D16, D17) not connected)
P118	GPIO10 (General Purpose IO)	S119	GND
P119	GPIO11 (General Purpose IO)	S120	LCD_DE (Display Enable - signal is high during the active display line; low otherwise)
P120	GND	P121	LCD_VS (Vertical Sync - high pulse indicates the start of a new display frame)
P121	I2C_PM_CK (Power management I2C bus clock)	S122	LCD_HS (Horizontal Sync - high pulse indicates the start of a new horizontal display line)
P122	I2C_PM_DAT (Power management I2C bus data)	S123	LCD_PCK (Pixel Clock - display data transitions on the positive clock edge)
P123	BOOT_SEL0# (Input straps determine the Module boot device. Pulled up on Module. Driven by OD part on Carrier.)	S124	GND
P124	BOOT_SEL1# (Input straps determine the Module boot device. Pulled up on Module. Driven by OD part on Carrier.)	S125	LVDS0+ (LVDS LCD data channel differential pair)
P125	BOOT_SEL2# (Input straps determine the Module boot device. Pulled up on Module. Driven by OD part on Carrier.)	S126	LVDS0- (High enables panel backlight)
P126	RESET_OUT# (General purpose reset output to Carrier board.)	S127	LCD_BKLT_EN (High enables panel backlight)

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Table 4-1: SMARC P-S Connector (J1) Signal Descriptions (Continued)

P127	RESET_IN# (Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise. Pulled up on Module. Driven by OD part on Carrier.)	S128	LVDS1+ (LVDS LCD data channel differential pair)
P128	POWER_BTN# (Power-button input from Carrier board. Carrier to float the line in inactive state. Active low, level sensitive. De-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.)	S129	LVDS1- (LVDS LCD data channel differential pair)
P129	SER0_TX (Asynchronous serial port data out)	S130	GND
P130	SER0_RX (Asynchronous serial port data in)	S131	LVDS2+ (LVDS LCD data channel differential pair)
P131	SER0_RTS# (Request to Send handshake line for SER0)	S132	LVDS2- (LVDS LCD data channel differential pair)
P132	SER0_CTS# (Clear to Send handshake line for SER0)	S133	LCD_VDD_EN (High enables panel VDD)
P133	GND	S134	LVDS_CK+ (LVDS LCD differential clock pair)
P134	SER1_TX (Asynchronous serial port data out)	S135	LVDS_CK- (LVDS LCD differential clock pair)
P135	SER1_RX (Asynchronous serial port data in)	S136	GND
P136	SER2_TX (Asynchronous serial port data out)	S137	LVDS3+ (LVDS LCD data channel differential pair)
P137	SER2_RX (Asynchronous serial port data in)	S138	LVDS3- (LVDS LCD data channel differential pair)
P138	SER2_RTS# (Request to Send handshake line for SER2)	S139	I2C_LCD_CK (I2C clock – to read LCD display EDID EEPROMs)
P139	SER2_CTS# (Clear to Send handshake line for SER2)	S140	I2C_LCD_DAT (I2C data – to read LCD display EDID EEPROMs)
P140	SER3_TX (Asynchronous serial port data out)	S141	LCD_BKLT_PWM (Display backlight PWM control)
P141	SER3_RX (Asynchronous serial port data in)	S142	Not connected
P142	GND	S143	GND
P143	CAN0_TX (CAN0 Transmit output)	S144	Not connected
P144	CAN0_RX (CAN0 Receive input)	S145	WDT_TIME_OUT# (Watchdog Timer Output)
P145	CAN1_TX (CAN1 Transmit output)	S146	PCIE_WAKE (PCIe wake up interrupt to host – common to PCIe; links A, B, C – pulled up or terminated on Module)
P146	CAN1_RX (CAN1 Receive input)	S147	VDD_RTC (Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based Lithium cell or Super Cap. See ***Section 7.3 RTC Voltage Rail*** of the SMARC specification for an important safety note on the implementation of lithium backup batteries.)

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Table 4-1: SMARC P-S Connector (J1) Signal Descriptions (Continued)

P147	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S148	LID# (Lid open/close indication to Module. Low indicates lid closure, which system ***may*** use to initiate a sleep state. Carrier to float the line in inactive state. Active low, level sensitive. De-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.)
P148	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S149	SLEEP# (Sleep indicator from Carrier board; sourced from user Sleep button or Carrier logic. Carrier to float the line in inactive state. Active low, level sensitive; de-bounced on the Module. Pulled up on Module. Driven by OD part on Carrier.)
P149	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S150	VIN_PWR_BAD# (Power bad indication from Carrier board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) ***is not*** enabled while this signal is held low by the Carrier. Pulled up on Module. Driven by OD part on Carrier.)
P150	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S151	CHARGING# (Held low by Carrier during battery charging. Carrier to float the line when charge is complete. Pulled up on Module. Driven by OD part on Carrier.)
P151	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S152	CHARGER_PRSNT# (Held low by Carrier if DC input for battery charger is present. Pulled up on Module. Driven by OD part on Carrier.)
P152	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S153	CHARGER_STBY# (The Module drives this signal low when the system is in a standby power state)
P153	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S154	CARRIER_PWR_ON (Carrier board circuits [apart from power management and power path circuits] ***are*** powered up until the Module asserts the CARRIER_PWR_ON signal)
P154	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S155	FORCE_RECOV# (Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when the Force Recovery function is invoked. Pulled high on the Module. For SOCs that do not implement a USB based Force Recovery function, then a low on the Module FORCE_RECOV# pin ***may*** invoke the SOC native Force Recovery mode – such as over a Serial Port. Pulled up on Module. Driven by OD part on Carrier.)
P155	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S156	BATLOW# (Battery low indication to Module. Carrier to float the line in inactive state. Pulled up on Module. Driven by OD part on Carrier.)

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Table 4-1: SMARC P-S Connector (J1) Signal Descriptions (Continued)

P156	VDD_IN (Module power input voltage - 3.0V min to 5.25V max)	S157	TEST# (Held low by Carrier to invoke Module vendor specific test function(s). Pulled up on Module. Driven by OD part on Carrier.)
		S158	GND

4.2 Debug (DB40)

Table 4-2 lists the pin signals of the CN2 connector, which provides 40 pins, 1 row, consecutive sequence with 0.02" (0.50mm) pitch.

Table 4-2: Debug Interface Signals (CN2)

Pin #	Signal	Interface
1	RESVD	
2	SMC_STATUS	SMC Debug
3	Not Connected	SMC Debug
4	SEL_U-BOOT	SMC Debug
5	POSTWDT_DIS#	SMC Debug
6	SUS_S5#	Test Point
7	SUS_S4#	Test Point
8	SUS_S3#	Test Point
9	CB_PWROK	Test Point
10	CB_RESET#	Test Point
11	SYS_RESET#	Test Point
12	PWRBTN#	Test Point
13	SMC_OCD0B	SMC Program
14	SMC_OCD0A	SMC Program
15	SMC_CLK	SMC Program
16	SMC_DATA	SMC Program
17	SMC_RESET_IN#	SMC Program
18	SMC_FLMD0	SMC Program
19	SMC_RXD6	SMC Program
20	SMC_TXD6	SMC Program
21	GND	
22	3V3_DUAL	SMC Program
23	3V3_SMC1	SMC Program
24	Not Connected	
25	Not Connected	
26	LPC_AD2	LPC Debug Card
27	LPC_AD3	LPC Debug Card
28	LPC_FRAME#	LPC Debug Card
29	CLK33_LPC	LPC Debug Card
30	RST#	LPC Debug Card
31	Not Connected	
32	Not Connected	
33	LPC_3V3	LPC Debug Card
34	SPI_U-BOOT_CLK	SPI Program
35	SPI_U-BOOT_MOSI	SPI Program
36	SPI_U-BOOT_MISO	SPI Program

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Table 4-2: Debug Interface Signals (CN2) (Continued)

37	SPI_U-BOOT_CS1#	SPI Program
38	SPI_U-BOOT_CS0#	SPI Program
39	GND	
40	VCC_SPI_IN	SPI Program

NOTE: The gray table cells denote ground.

5 Power and System Management

5.1 SEMA Utility

Under the management of the BMC chip (Board Management Controller), the SEMA utility (Smart Embedded Management Agent) provides system control and failure protection—counting, monitoring, and measuring hardware and software events, from which the SOC can trigger corrective commands. The optional SEMA Cloud utility not only controls local events on the module but system client events on the IoT.

5.2 On-Board Power Supply

The on-board power supply generates all necessary voltages from the single supply voltage range of 3V to 5.25V DC.

Externally, +5V Standby can be used instead of the on-board generated +5V Standby voltage.

5.3 System States

The following system states are supported: Suspend to RAM, Freeze, and Standby.

5.4 External Power Button

The board provides support for a power button to initiate transition from Off to On and On to Off (hold for 4 seconds to power off.)

5.5 Reset-In Signal

The board provides support for a reset button to restart the system.

5.6 External Battery

The module supports an external RTC that is powered by a battery on the baseboard.

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Appendix A Technical Support

ADLINK Technology, Inc. provides a number of methods for contacting Technical Support listed in Table A-1 below. Requests for support through Ask an Expert are given the highest priorities, and usually will be addressed within one working day.

- ADLINK Ask an Expert – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the ADLINK web site at http://www.adlinktech.com/AAE/. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online if you wish to use the Ask a Question feature.

ADLINK strongly suggests that you register with the web site. By creating a profile on the ADLINK web site, you will have a portal page called “My ADLINK”, unique to you with access to exclusive services and account information.

- Personal Assistance – You may also request personal assistance by creating an Ask an Expert account and then going to the Ask a Question feature. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request, you must log in to go to the My Question area where you can check status, update your request, and access other features.
- Download Service – This service is also free and available 24 hours a day at http://www.adlinktech.com. For certain downloads such as technical documents and software, you must register online before you can log in to this service.

Table A-1: Technical Support Contact Information

Method	Contact Information
Ask an Expert	http://www.adlinktech.com/AAE/
Web Site	http://www.adlinktech.com
Standard Mail	**ADLINK Technology, Inc.** Address: 9F, No.166 Jian Yi Road, Zhonghe District New Taipei City 235, Taiwan 新北市中和區建一路 166 號 9 樓 Tel: +886-2-8226-5877 Fax: +886-2-8226-5717 Email: service@adlinktech.com **Ampro ADLINK Technology, Inc.** Address: 5215 Hellyer Avenue, #110 San Jose, CA 95138, USA Tel: +1-408-360-0200 Toll Free: +1-800-966-5200 (USA only) Fax: +1-408-360-0222 Email: info@adlinktech.com **ADLINK Technology (China) Co., Ltd.** Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203) 300 Fang Chun Rd., Zhangjiang Hi-Tech Park Pudong New Area, Shanghai, 201203 China Tel: +86-21-5132-8988 Fax: +86-21-5132-3588 Email: market@adlinktech.com

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Table A-1: Technical Support Contact Information (Continued)

ADLINK Technology Beijing
Address: 北京市海淀区上地东路 1 号盈创动力大厦 E 座 801 室(100085)
Rm. 801, Power Creative E, No. 1 Shang Di East Rd.
Beijing, 100085 China
Tel: +86-10-5885-8666
Fax: +86-10-5885-8626
Email: market@adlinktech.com

ADLINK Technology Shenzhen
Address: 深圳市南山区科技园南区高新南七道 数字技术园
A1 栋 2 楼 C 区 (518057)
2F, C Block, Bldg. A1, Cyber-Tech Zone, Gao Xin Ave. Sec. 7
High-Tech Industrial Park S., Shenzhen, 518054 China
Tel: +86-755-2643-4858
Fax: +86-755-2664-6353
Email: market@adlinktech.com

LiPPERT ADLINK Technology GmbH
Address: Hans-Thoma-Strasse 11
D-68163 Mannheim, Germany
Tel: +49-621-43214-0
Fax: +49-621 43214-30
Email: emea@adlinktech.com

PENTA ADLINK Technology GmbH
Ulrichsbergerstrasse 17
94469 Deggendorf, Germany
Tel: +49 (0) 991 290 94 – 10
Fax: +49 (0) 991 290 94 - 29
Email: emea@adlinktech.com

ADLINK Technology, Inc. (French Liaison Office)
Address: 6 allée de Londres, Immeuble Ceylan
91940 Les Ulis, France
Tel: +33 (0) 1 60 12 35 66
Fax: +33 (0) 1 60 12 35 66
Email: france@adlinktech.com

ADLINK Technology Japan Corporation
Address: 〒101-0045 東京都千代田区神田鍛冶町 3-7-4
神田 374 ビル 4F
KANDA374 Bldg. 4F, 3-7-4 Kanda Kajicho,
Chiyoda-ku, Tokyo 101-0045, Japan
Tel: +81-3-4455-3722
Fax: +81-3-5209-6013
Email: japan@adlinktech.com

ADLINK Technology, Inc. (Korean Liaison Office)
Address: 137-881 서울시 서초구 서초대로 326, 802 (서초동, 모인터빌딩)
802, Mointer B/D, 326 Seocho-daero, Seocho-Gu,
Seoul 137-881, Korea
Tel: +82-2-2057-0565
Fax: +82-2-2057-0563
Email: korea@adlinktech.com

ADLINK Technology Singapore Pte. Ltd.
Address: 84 Genting Lane #07-02A, Cityneon Design Centre
Singapore 349584
Tel: +65-6844-2261
Fax: +65-6844-2263
Email: singapore@adlinktech.com

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Table A-1: Technical Support Contact Information (Continued)

	ADLINK Technology Singapore Pte. Ltd. (Indian Liaison Office) Address: #50-56, First Floor, Spearhead Towers Margosa Main Road (between 16th/17th Cross) Malleswaram, Bangalore - 560 055, India Tel: +91-80-65605817, +91-80-42246107 Fax: +91-80-23464606 Email: india@adlinktech.com **ADLINK Technology, Inc. (Israeli Liaison Office)** Address: 27 Maskit St., Corex Building PO Box 12777 Herzliya 4673300, Israel Tel: +972-54-632-5251 Fax: +972-77-208-0230 Email: israel@adlinktech.com **ADLINK Technology, Inc. (UK Liaison Office)** Tel: +44 774 010 59 65 Email: UK@adlinktech.com

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