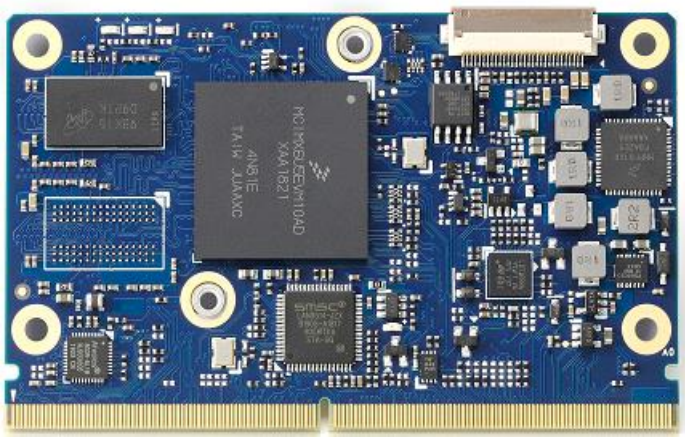
LEC-IMX6R2

User's Guide

02/12/2021



SMARC module

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Preface

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Safety Instructions

For user safety, please read and follow all Instructions, **WARNING**s, **CAUTION**s, and **NOTE**s marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

Conventions

The following conventions may be used throughout this manual, denoting special levels of information



Note: This information adds clarity or specifics to text and illustrations.



Caution: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.



Warning: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

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Revision History

Revision	Description	Date dd/mm/yyyy	Author
1.0	Initial public release	10/03/2021	Henri Parmentier

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Introduction

1.1 The SMARC Formfactor

The SMARC ("Smart Mobility ARChitecture") is a versatile small form factor computer on Module definition targeting applications that require low power, low costs, and high performance. The Modules will typically use ARM SOCs similar or the same as those used in many familiar devices such as tablet computers and smart phones. Alternative low power SOCs and CPUs, such as tablet oriented X86 devices and other RISC CPUs may be used as well. The Module power envelope is typically under 6W.

Two Module sizes are defined: 82 mm x 50 mm and 82 mm x 80 mm.

The Module PCBs have 314 edge fingers that mate with a low profile 314 pin 0.5 mm pitch right angle connector (the connector is sometimes identified as a 321 pin connector, but 7 pins are lost to the key).

The Modules are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE and a single channel LVDS display transmitter are concentrated on the Module. The Modules are used with application specific Carrier Boards that implement other features such as audio CODECs, touch controllers, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

SGeT STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

SMARC module and carrier specifications are available online at: https://www.sget.org/standards/smarc.html

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2. Specifications

2.1 Core System

SoC

NXP i.MX 6 Series

- i.MX6 Solo / Duallite: Single/Dual core ARM® Cortex™-A9 SOC
- i.MX6 Dual / Quad: Dual/Quad core ARM® Cortex™-A9 SOC
- i.MX6 DualPlus / QuadPlus: Dual/Quad core ARM® Cortex™-A9 SOC

available either as industrial (-40°C to +85°C) or commercial (0°C to +70°C) type"

L2 Cache

- 32 KB I-cache 32 KB D-cache

Memory

- 512MB/ 1/2/4GB DDR3L memory down

IoT security

CryptoAuthentication™ Device, Microchip ATECC608A

- Cryptographic co-processor with secure hardware-based key storage
- Protected storage for up to 16 Keys, certificates or data
- ECDH: FIPS SP800-56A Elliptic Curve Diffie-Hellman
- NIST standard P256 elliptic curve support
- SHA-256 & HMAC hash including off-chip context save/restore
- AES-128: encrypt/decrypt, galois field multiply for GCM

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2.2 Video

LEC-iMX6R2 standard display support is consisting of full HD capable HDMI 1.4, MIPI DSI and single/dual channel 24-bit LVDS.

GPU Core:

- Vivante GC880 / GX2000 / GC2000+
  GPU cores are varying between SKU's check datasheet for more info

GPU/VPU Feature Support

- Video, 2D and 3D Graphics Units integrated in i.MX6 Processor
- OpenGL® ES 1.1/2.0/Halti, OpenVG™ 1.1, OpenCL™ 1.1 EP
- Multi-Format Hardware Video Encoder/Decoder

HDMI

- HDMI V1.4 up to WUXGA (1920x1080)
- FHD 1080p @ 30fps

LVDS

- Dual-channel 18/24-bit max 1920 x 1080 x 30fps
- Single-channel 18/24-bit max 1366 x 768 x 30fps

MIPI DSI

- 1080p @ 60fps display output
- Compatible with MIPI specification v1.0
- 2 data lanes**,** 1.0 Gbps max data rate per lane
- support HS and LP mode

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Camera support

- Single MIPI CSI camera supported on CSI1
- Four lanes : QuadPlus, Quad, DualPlus, Dual
- Two lanes : DualLite and Solo

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2.3 Audio

- Supports i2S audio codec interface, audio ADC and DAC (located on carrier)

2.4 Dual Ethernet

Primary LAN

- MAC 10/100/1000 Ethernet Controller in SOC
- PHY on module through RGMII
- Operates on TCP/IP, UDP/IP, and ICMP/IP protocol data or on IP header only

NOTE: The Ethernet throughput is limited to 400 Mbit/s by the Freescale SoC.

Optional Secondary LAN

- MAC/PHY 10/100 Ethernet Controller in LAN9514 on USB 2.0
- Supports 10/100-Mbps data transfer rates, both full-duplex and half-duplex
- Supports IEEE 802.1Q VLAN tag detection for reception frames
- Support detection of LAN wake-up frames and AMD Magic Packet frames

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2.5 Extension busses

PCIe

One PCI Express GEN2 x1 interfaces

- Only available on QuadPlus, Quad, DualPlus, Dual

SATA

Single port SATA 2 support

- Only available on QuadPlus, Quad, DualPlus, Dual

USB

4x USB 2.0 and 1x USB2.0 OTG

UART

Four UART interface SER0 and SER2 (TX/X/CTS/RTS)

- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 5 MHz • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE

CAN bus

2x CAN2.0B only or mixed CAN2.0B and CAN FB mode, data bit rate up to 8 Mbps via SPI to CAN controller

SPI

2 x SPI

I2S

2x I2S interfaces with audio resolution from 16-bits to 32-bits and sample rate up to 192KHz (see Audio Codec support)

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I2C

Three I2C interfaces

- Support 7bits and 10bits address mode
- Data transfer rates of 100 kbit/s, 400 kbit/s and 1 Mbit/s
  - General Purpose I2C_GP for usage on carrier
  - Power Management I2C_PM , connected to PMIC
  - LCD I2C to detect and manage connected displays
  - Camera I2C

GPIO

12x GPIO with interrupt

2.6 System Storage

SDIO

1x SDIO (4-bit) compatible up to version 3.0.

eMMC

soldered on module 16, 32 or 64 GB (build option) either standard or -40+85C temp range

Compatible with eMMC specification 4.41, 4.51 and 5.0

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2.7 SEMA® Board Management Controller

Voltage/current monitoring, boot configuration, logistics and forensic

information, flat panel control, watchdog timer

2.8 Debug Header

30-pin multipurpose flat cable connector for use with optional DB-30 debug module Provides JTAG, BMC access; UART, power test points; diagnostic LEDs, Power, Reset, Boot configuration

2.9 Boot Modes

eMMC and SD-Card boot modes are supported

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2.10 Power

Supply Voltage

4.75 V – 5.25 V

2.11 Mechanical and Environmental

Form Factor

SGET SMARC Specifications v2.1

Dimension

SMARC small size module, 82mm x 50mm

Operating Temperature

Standard: 0°C to +60°C

Rugged: -40°C to +85°C (optional)

Humidity

5-90% RH operating, non-condensing

5-95% RH storage (and operating with conformal coating)

Shock and Vibration

IEC 60068-2-64 and IEC-60068-2-27, MIL-STD-202 F, Method 213B, Table 213-I,

Condition A and Method 214A, Table 214-I, Condition D

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3. Block Diagram

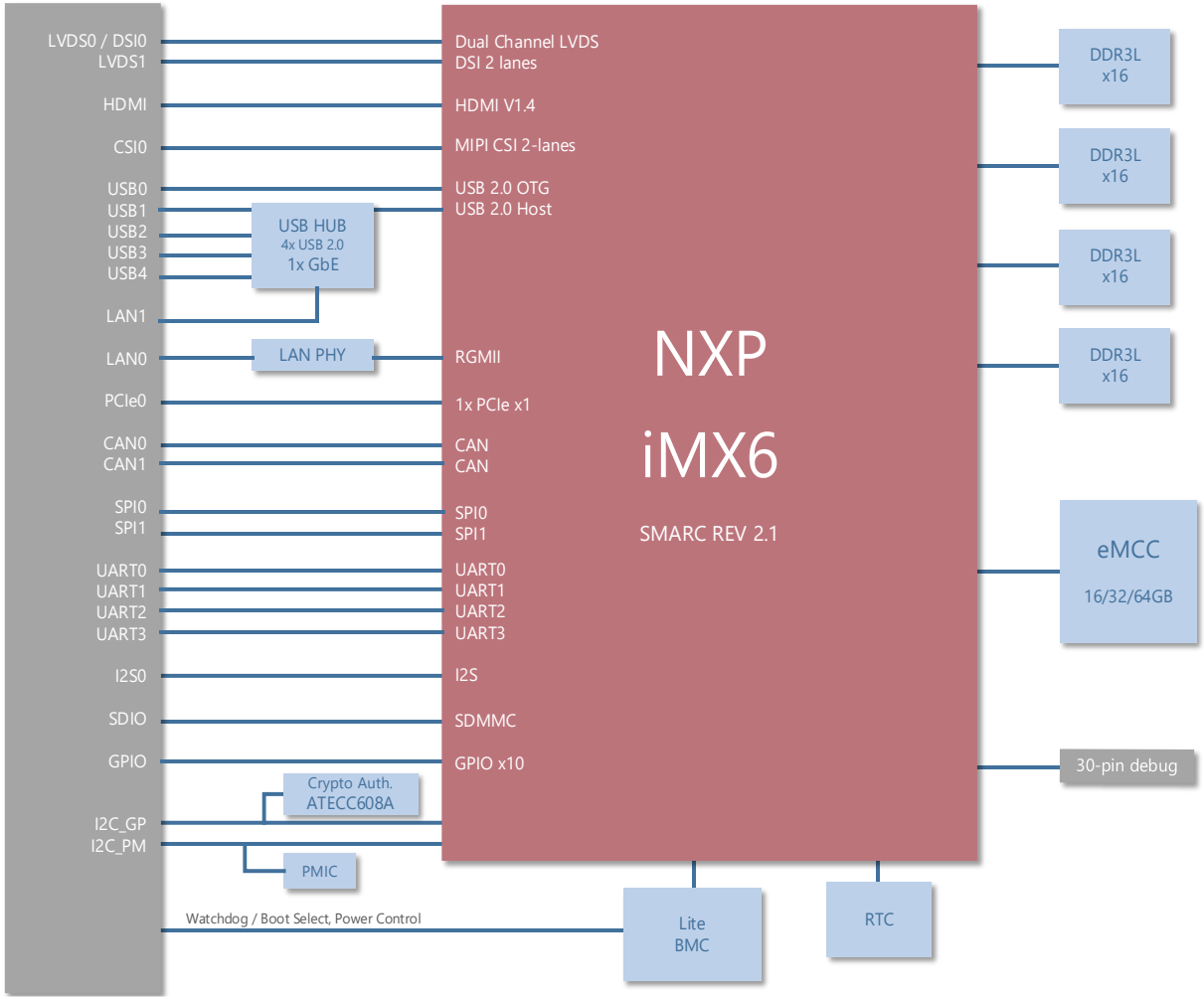


Figure 1 – Module function diagram

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4. Pinout and Signal Descriptions

4.1 Pin Summary

The below table is a comprehensible list of all signal pins on the MXM 3 connector in the standard specification SMARC 2.1.

Those signals not supported on LEC-iMX6R2 are strikethrough ~~STRIKETHROUGH~~

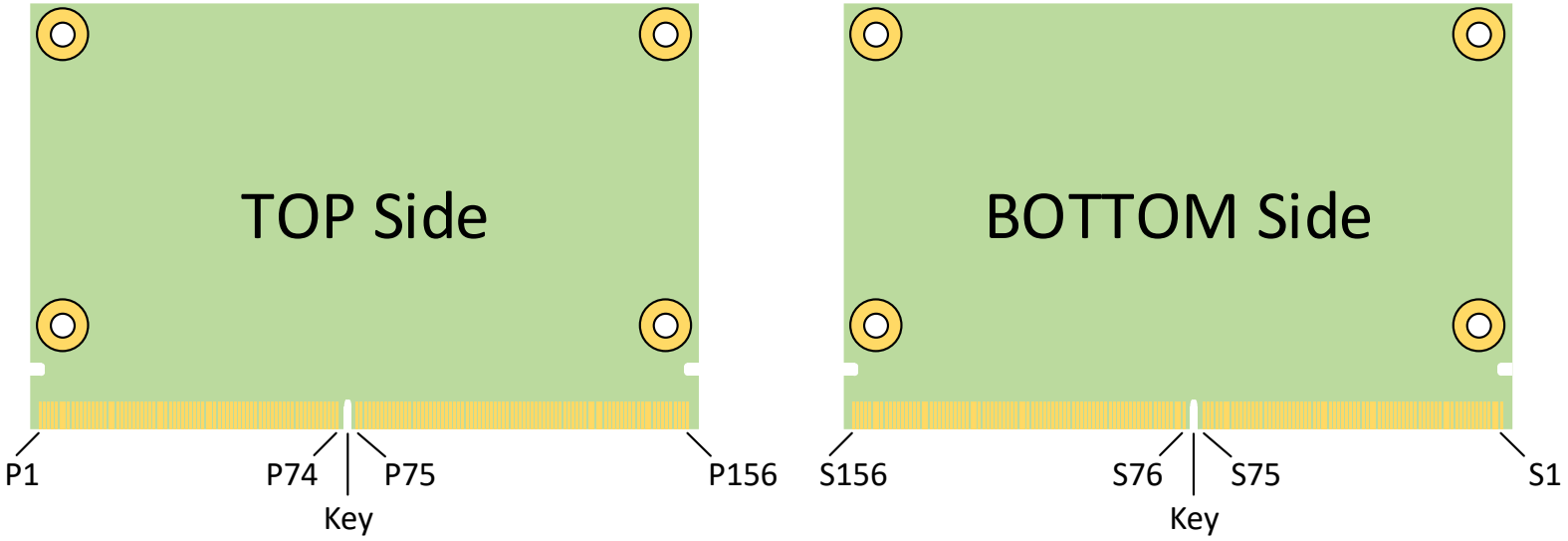


Figure 2 – Module top/botom side pin numbering

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P-Pin	Primary (Top) Side
P1	~~SMB_ALERT_1V8#~~
P2	GND
P3	CSI1_CK+
P4	CSI1_CK-
P5	~~GBE1_SDP~~
P6	~~GBE0_SDP~~
P7	CSI1_RX0+
P8	CSI1_RX0-
P9	GND
P10	CSI1_RX1+
P11	CSI1_RX1-
P12	GND
P13	CSI1_RX2+
P14	CSI1_RX2-
P15	GND
P16	CSI1_RX3+
P17	CSI1_RX3-
P18	GND
P19	GBE0_MDI3-
P20	GBE0_MDI3+
P21	GBE0_LINK100#
P22	GBE0_LINK1000#
P23	GBE0_MDI2-
P24	GBE0_MDI2+
P25	GBE0_LINK_ACT#
P26	GBE0_MDI1-
P27	GBE0_MDI1+
P28	~~GBE0_CTREF~~
P29	GBE0_MDI0-
P30	GBE0_MDI0+
P31	SPI0_CS1# note 2
P32	GND
P33	SDIO_WP
P34	SDIO_CMD
P35	SDIO_CD#

S-Pin	Secondary (Bottom) Side
S1	~~CSI1_TX+~~ / I2C_CAM1_CK
S2	~~CSI1_TX-~~ / I2C_CAM1_DAT
S3	GND
S4	~~RSVD~~
S5	~~CSI0_TX- / I2C_CAM0_CK~~
S6	CAM_MCK
S7	~~CSI0_TX+ / I2C_CAM0_DAT~~
S8	~~CSI0_CK+~~
S9	~~CSI0_CK-~~
S10	GND
S11	~~CSI0_RX0+~~
S12	~~CSI0_RX0-~~
S13	GND
S14	~~CSI0_RX1+~~
S15	~~CSI0_RX1-~~
S16	GND
S17	GBE1_MDI0+
S18	GBE1_MDI0-
S19	GBE1_LINK100#
S20	GBE1_MDI1+
S21	GBE1_MDI1-
S22	~~GBE1_LINK1000#~~
S23	~~GBE1_MDI2+~~
S24	~~GBE1_MDI2-~~
S25	GND
S26	~~GBE1_MDI3+~~
S27	~~GBE1_MDI3-~~
S28	~~GBE1_CTREF~~
S29	~~PCIE_D_TX+ / SERDES_1_TX+~~
S30	~~PCIE_D_TX- / SERDES_1_TX-~~
S31	GBE1_LINK_ACT#
S32	~~PCIE_D_RX+ / SERDES_1_RX+~~
S33	~~PCIE_D_RX- / SERDES_1_RX-~~
S34	GND
S35	USB4+
S36	USB4-

P-Pin	Primary (Top) Side
P36	SDIO_CK
P37	~~SDIO_PWR_EN~~
P38	GND
P39	SDIO_D0
P40	SDIO_D1
P41	SDIO_D2
P42	SDIO_D3
P43	SPI0_CS0# note 2
P44	SPI0_CK note 2
P45	SPI0_DIN note 2
P46	SPI0_DO note 2
P47	GND
P48	SATA_TX+
P49	SATA_TX-
P50	GND
P51	SATA_RX+
P52	SATA_RX-
P53	GND
P54	~~ESPI_CS0#~~ / SPI1_CS0#
P55	~~ESPI_CS1#~~ / SPI1_CS1#
P56	~~ESPI_CK~~ / SPI1_CK
P57	~~ESPI_IO_1~~ / SPI1_DIN
P58	~~ESPI_IO_0~~ / SPI1_DO
P59	GND
P60	USB0+
P61	USB0-
P62	USB0_EN_OC#
P63	USB0_VBUS_DET
P64	USB0_OTG_ID
P65	USB1+
P66	USB1-
P67	USB1_EN_OC#
P68	GND
P69	USB2+
P70	USB2-
P71	USB2_EN_OC#

S-Pin	Secondary (Bottom) Side
S37	~~USB3_VBUS_DET~~
S38	AUDIO_MCK
S39	I2S0_LRCK
S40	I2S0_SDOUT
S41	I2S0_SDIN
S42	I2S0_CK
S43	~~ESPI_ALERT0#~~
S44	~~ESPI_ALERT1#~~
S45	~~MDIO_CLK~~
S46	~~MDIO_DAT~~
S47	GND
S48	I2C_GP_CK
S49	I2C_GP_DAT
S50	~~HDA_SYNC / I2S2_LRCK~~
S51	~~HDA_SDO / I2S2_SDOUT~~
S52	~~HDA_SDI / I2S2_SDIN~~
S53	~~HDA_CK / I2S2_CK~~
S54	SATA_ACT#
S55	~~USB5_EN_OC#~~
S56	~~ESPI_IO_2~~
S57	~~ESPI_IO_3~~
S58	ESPI_RESET#
S59	~~USB5+~~
S60	~~USB5-~~
S61	GND
S62	~~USB3_SSTX+~~
S63	~~USB3_SSTX-~~
S64	GND
S65	~~USB3_SSRX+~~
S66	~~USB3_SSRX-~~
S67	GND
S68	USB3+
S69	USB3-
S70	GND
S71	~~USB2_SSTX+~~
S72	~~USB2_SSTX-~~

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P-Pin	Primary (Top) Side
P72	~~RSVD~~
P73	~~RSVD~~
P74	USB3_EN_OC#
	Key
P75	PCIE_A_RST#
P76	USB4_EN_OC#
P77	~~PCIE_B_CKREQ#~~
P78	~~PCIE_A_CKREQ#~~
P79	GND
P80	~~PCIE_C_REFCK+~~
P81	~~PCIE_C_REFCK-~~
P82	GND
P83	PCIE_A_REFCK+
P84	PCIE_A_REFCK-
P85	GND
P86	PCIE_A_RX+
P87	PCIE_A_RX-
P88	GND
P89	PCIE_A_TX+
P90	PCIE_A_TX-
P91	GND
P92	HDMI_D2+ / ~~DP1_LANE0+~~
P93	HDMI_D2- / ~~DP1_LANE0-~~
P94	GND
P95	HDMI_D1+ / ~~DP1_LANE1+~~
P96	HDMI_D1- / ~~DP1_LANE1-~~
P97	GND
P98	HDMI_D0+ / ~~DP1_LANE2+~~
P99	HDMI_D0- / ~~DP1_LANE2-~~
P100	GND
P101	HDMI_CK+ / ~~DP1_LANE3+~~
P102	HDMI_CK- / ~~DP1_LANE3-~~
P103	GND

S-Pin	Secondary (Bottom) Side
S73	GND
S74	~~USB2_SSRX+~~
S75	~~USB2_SSRX-~~
	Key
S76	~~PCIE_B_RST#~~
S77	~~PCIE_C_RST#~~
S78	~~PCIE_C_RX+ / SERDES_2_RX+~~
S79	~~PCIE_C_RX- / SERDES_2_RX-~~
S80	GND
S81	~~PCIE_C_TX+ / SERDES_2_TX+~~
S82	~~PCIE_C_TX- / SERDES_2_TX-~~
S83	GND
S84	~~PCIE_B_REFCK+~~
S85	~~PCIE_B_REFCK-~~
S86	GND
S87	~~PCIE_B_RX+~~
S88	~~PCIE_B_RX-~~
S89	GND
S90	~~PCIE_B_TX+~~
S91	~~PCIE_B_TX-~~
S92	GND
S93	~~DP0_LANE0+~~
S94	~~DP0_LANE0-~~
S95	~~DP0_AUX_SEL~~
S96	~~DP0_LANE1+~~
S97	~~DP0_LANE1-~~
S98	~~DP0_HPD~~
S99	~~DP0_LANE2+~~
S100	~~DP0_LANE2-~~
S101	GND
S102	~~DP0_LANE3+~~
S103	~~DP0_LANE3-~~
S104	~~USB3_OTG_ID~~

P-Pin	Primary (Top) Side
P104	HDMI_HPD / ~~DP1_HPD~~
P105	HDMI_CTRL_CK / ~~DP1_AUX+~~
P106	HDMI_CTRL_DAT / ~~DP1_AUX-~~
P107	~~DP1_AUX_SEL~~
P108	GPIO0 / CAM0_PWR#
P109	GPIO1 / CAM1_PWR#
P110	GPIO2 / CAM0_RST#
P111	GPIO3 / CAM1_RST#
P112	GPIO4 / ~~HDA_RST#~~
P113	GPIO5 / ~~PWM_OUT~~
P114	GPIO6 / ~~TACHIN~~
P115	GPIO7
P116	GPIO8
P117	GPIO9
P118	GPIO10
P119	GPIO11
P120	GND
P121	I2C_PM_CK
P122	I2C_PM_DAT
P123	BOOT_SEL0#
P124	BOOT_SEL1#
P125	BOOT_SEL2#
P126	RESET_OUT#
P127	RESET_IN#
P128	POWER_BTN#
P129	SER0_TX
P130	SER0_RX
P131	SER0_RTS#
P132	SER0_CTS#
P133	GND
P134	SER1_TX
P135	SER1_RX
P136	SER2_TX
P137	SER2_RX
P138	SER2_RTS#

S-Pin	Secondary (Bottom) Side
S105	~~DP0_AUX+~~
S106	~~DP0_AUX-~~
S107	~~LCD1_BKLT_EN~~
S108	LVDS1_CK+/~~eDP1_AUX+~~/ ~~DSI1_CLK+~~
S109	LVDS1_CK- / ~~eDP1_AUX-~~ / ~~DSI1_CLK-~~
S110	GND
S111	LVDS1_0+ / ~~eDP1_TX0+~~ / ~~DSI1_D0+~~
S112	LVDS1_0- / ~~eDP1_TX0-~~ / ~~DSI1_D0-~~
S113	~~eDP1_HPD / DSI1_TE~~
S114	LVDS1_1+ / ~~eDP1_TX1+~~ / ~~DSI1_D1+~~
S115	LVDS1_1- / ~~eDP1_TX1-~~ / ~~DSI1_D1-~~
S116	~~LCD1_VDD_EN~~
S117	LVDS1_2+ / ~~eDP1_TX2+~~ / ~~DSI1_D2+~~
S118	LVDS1_2- / ~~eDP1_TX2-~~ / ~~DSI1_D2-~~
S119	GND
S120	LVDS1_3+ / ~~eDP1_TX3+~~ / ~~DSI1_D3+~~
S121	LVDS1_3- / ~~eDP1_TX3-~~ / ~~DSI1_D3-~~
S122	~~LCD1_BKLT_PWM~~
S123	~~GPIO13~~
S124	GND
S125	LVDS0_0+ / ~~eDP0_TX0+~~ / DSI0_D0+
S126	LVDS0_0- / ~~eDP0_TX0-~~ / DSI0_D0-
S127	LCD0_BKLT_EN
S128	LVDS0_1+ / ~~eDP0_TX1+~~ / DSI0_D1+
S129	LVDS0_1- / ~~eDP0_TX1-~~ / DSI0_D1-
S130	GND
S131	LVDS0_2+/~~eDP0_TX2+~~/ ~~DSI0_D2+~~
S132	LVDS0_2- /~~eDP0_TX2-~~ / ~~DSI0_D2-~~
S133	LCD0_VDD_EN
S134	LVDS0_CK+/~~eDP0_AUX~~/ DSI0_CLK+
S135	LVDS0_CK-/~~eDP0_AUX-~~ / DSI0_CLK-
S136	GND
S137	LVDS0_3+ / ~~eDP0_TX3+~~ / ~~DSI0_D3+~~
S138	LVDS0_3- / ~~eDP0_TX3-~~ / ~~DSI0_D3-~~
S139	I2C_LCD_CK

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P-Pin	Primary (Top) Side
P139	SER2_CTS#
P140	SER3_TX
P141	SER3_RX
P142	GND
P143	CAN0_TX
P144	CAN0_RX
P145	CAN1_TX
P146	CAN1_RX
P147	VDD_IN
P148	VDD_IN

S-Pin	Secondary (Bottom) Side
S140	I2C_LCD_DAT
S141	LCD0_BKLT_PWM
S142	GPIO12
S143	GND
~~S144~~	~~eDP0_HPD / DSI0_TE~~
S145	WDT_TIME_OUT#
S146	PCIE_WAKE#
S147	VDD_RTC
S148	LID#
S149	SLEEP#

P-Pin	Primary (Top) Side
P149	VDD_IN
P150	VDD_IN
P151	VDD_IN
P152	VDD_IN
P153	VDD_IN
P154	VDD_IN
P155	VDD_IN
P156	VDD_IN

S-Pin	Secondary (Bottom) Side
S150	VIN_PWR_BAD#
S151	CHARGING#
S152	CHARGER_PRSNT#
S153	CARRIER_STBY#
S154	CARRIER_PWR_ON
S155	FORCE_RECOV#
S156	BATLOW#
S157	TEST#
S158	GND

Note 1: Secondary LAN connected to the USB hub

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4.2 Signal Terminology Descriptions

Meaning of the terms used for signal description tables

Term	Description
I	Input to the module
O	Output from the module
O OD	Open drain output from the module
I OD	Open drain input to the module, with mandatory PU (pull up) on module
OD	Open drain
I/O	Bi-directional Input/Output
PU	PU (pull-up) resistor on module
PD	PD (pull-down) resistor on module
VDD_IN	Main power source from carrier to module
CMOS	Logic input or output
GBE MDI	Differential analog signaling for Gigabit Media Dependent Interface
LVDS DP	Low Voltage Differential Signal for DisplayPort interface
LVDS D-PHY	Low Voltage Differential Signal for MIPI CSI-2 cameras and DSI displays
LVDS M-PHY	Low Voltage Differential Signal for MIPI CSI-3 cameras
LVDS LCD	Low Voltage Differential Signal for LCD displays
LVDS PCIE	Low Voltage Differential Signal for PCIe
LVDS SATA	Low Voltage Differential Signal for SATA
TMDS HDMI	Transition Minimized Differential Signal for HDMI displays
USB	DC coupled differential signaling for traditional (non-Superspeed) USB signals
USB SS	Differential signal for SuperSpeed USB signals
USB VBUS 5V	5V tolerant input for USB VBUS detection
3.3V	3.3V Power Domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
1.8V	1.8V Power Domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
3.3Vsb	3.3V Power Domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)
1.8Vsb	1.8V Power Domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)

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4.3 Signal Description by function

4.3.1 The First Display Interface

The first display interface is a group of 30-pins that is split into a channel 0 and channel 1. The SMARC specification allows to support either dual channel LVDS ports, 2 separate single channel LVDS ports, 2 MIPI DSI ports of 4 lanes each or 2 eDP ports 4 lanes each. A mix of different display type such as DSI and eDP is also permitted. Below tables show which display ports are supported on this particular module

Pin #	LVDS Name	MIPI DSI Name	eDP Name
S125	LVDS0_0+	DSI0_D0+	~~eDP0_TX0+~~
S126	LVDS0_0-	DSI0_D0-	~~eDP0_TX0-~~
S128	LVDS0_1+	DSI0_D1+	~~eDP0_TX1+~~
S129	LVDS0_1 -	DSI0_D1-	~~eDP0_TX1-~~
S131	LVDS0_2+	~~DSI0_D2+~~	~~eDP0_TX2+~~
S132	LVDS0_2-	~~DSI0_D2-~~	~~eDP0_TX2-~~
S137	LVDS0_3+	~~DSI0_D3+~~	~~eDP0_TX3+~~
S138	LVDS0_3-	~~DSI0_D3-~~	~~eDP0_TX3-~~
S134	LVDS0_CK+	DSI0_CLK+	~~eDP0_AUX+~~
S135	LVDS0_CK-	DSI0_CLK-	~~eDP0_AUX-~~
S133	LCD0_VDD_EN	LCD0_VDD_EN	~~LCD0_VDD_EN~~
S127	LCD0_BKLT_EN	LCD0_BKLT_EN	~~LCD0_BKLT_EN~~
S141	LCD0_BKLT_PWM	LCD0_BKLT_PWM	~~LCD0_BKLT_PWM~~
S144		DSI0_TE	~~eDP0_HPD~~
S139	I2C_LCD_CK	I2C_LCD_CK	~~I2C_LCD_CK~~
S140	I2C_LCD_DAT	I2C_LCD_DAT	~~I2C_LCD_DAT~~

Pin #	LVDS Name	MIPI DSI Name	eDP Name
S111	LVDS1_0+	~~DSI1_D0+~~	~~eDP1_TX0+~~
S112	LVDS1_0-	~~DSI1_D0-~~	~~eDP1_TX0-~~
S114	LVDS1_1+	~~DSI1_D1+~~	~~eDP1_TX1+~~
S115	LVDS1_1 -	~~DSI1_D1-~~	~~eDP1_TX1-~~
S117	LVDS1_2+	~~DSI1_D2+~~	~~eDP1_TX2+~~
S118	LVDS1_2-	~~DSI1_D2-~~	~~eDP1_TX2-~~
S120	LVDS1_3+	~~DSI1_D3+~~	~~eDP1_TX3+~~
S121	LVDS1_3-	~~DSI1_D3-~~	~~eDP1_TX3-~~
S108	LVDS1_CK+	~~DSI1_CLK+~~	~~eDP1_AUX+~~
S109	LVDS1_CK-	~~DSI1_CLK-~~	~~eDP1_AUX-~~
S116	~~LCD1_VDD_EN~~	~~LCD1_VDD_EN~~	~~LCD1_VDD_EN~~
S107	~~LCD1_BKLT_EN~~	~~LCD1_BKLT_EN~~	~~LCD1_BKLT_EN~~
S122	~~LCD1_BKLT_PWM~~	~~LCD1_BKLT_PWM~~	~~LCD1_BKLT_PWM~~
S113		~~DSI1_TE~~	~~eDP1_HPD~~

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4.3.1.1 LVDS0/LVDS1 mode

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
LVDS0_0+ LVDS0_0- LVDS0_1+ LVDS0_1 - LVDS0_2+ LVDS0_2- LVDS0_3+ LVDS0_3-	S125 S126 S128 S129 S131 S132 S137 S138	Primary LVDS channel differential pair data lines	O LVDS LCD		Runtime		
LVDS0_CK+ LVDS0_CK-	S134 S135	Primary LVDS channel differential pair clock lines	O LVDS LCD		Runtime		
LCD0_VDD_EN	S133	Primary LVDS channel power enable, active high	O CMOS	1.8V	Runtime		
LCD0_BKLT_EN	S127	Primary LVDS channel backlight enable, active high	O CMOS	1.8V	Runtime		
LCD0_BKLT_PWM	S141	Primary LVDS channel brightness control through pulse width modulation (PWM)	O CMOS	1.8V	Runtime		
LVDS1_0+ LVDS1_0- LVDS1_1+ LVDS1_1 - LVDS1_2+ LVDS1_2- LVDS1_3+ LVDS1_3-	S111 S112 S114 S115 S117 S118 S120 S121	Secondary LVDS channel differential pair data lines	O LVDS LCD		Runtime		
LVDS1_CK+ LVDS1_CK-	S108 S109	Secondary LVDS channel differential pair clock lines.	O LVDS LCD		Runtime		
LCD1_VDD_EN	S116	Secondary panel power enable, active high	O CMOS	1.8V	Runtime		
LCD1_BKLT_EN	S107	Secondary panel backlight enable, active high	O CMOS	1.8V	Runtime		
LCD1_BKLT_PWM	S122	Secondary panel brightness control through pulse width modulation (PWM)	O CMOS	1.8V	Runtime		

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Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
I2C_LCD_DAT	S140	DDC data line used for flat panel detection and control	I/O OD CMOS	1.8V	Runtime	PU 2k2	
I2C_LCD_CK	S139	DDC clock line used for flat panel detection and control	O OD CMOS	1.8V	Runtime	PU 2k2	

4.3.1.2 DSI mode

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
DSI0_D0+ DSI0_D0- DSI0_D1+ DSI0_D1- ~~DSI0_D2+~~ ~~DSI0_D2-~~ ~~DSI0_D3+~~ ~~DSI0_D3-~~	S125 S126 S128 S129 S131 S132 S137 S138	Primary DSI panel differential pair data lines	O LVDS D-PHY		Runtime		Build option
DSI0_CLK+ DSI0_CLK-	S134 S135	Primary DSI panel differential pair clock lines.	O LVDS D-PHY		Runtime		Build option
LCD0_VDD_EN	S133	Primary panel power enable, active high	O CMOS	1.8V	Runtime		
LCD0_BKLT_EN	S127	Primary panel backlight enable, active high	O CMOS	1.8V	Runtime		
LCD0_BKLT_PWM	S141	Primary panel brightness control through pulse width modulation (PWM)	O CMOS	1.8V	Runtime		
DSI0_TE	S144	Primary DSI panel tearing effect signal	I CMOS	1.8V	Runtime		

I2C_LCD_DAT	S140	DDC data line used for flat panel detection and control	I/O OD CMOS	1.8V	Runtime	PU 2k2	
I2C_LCD_CK	S139	DDC clock line used for flat panel detection and control	O OD CMOS	1.8V	Runtime	PU 2k2	

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4.3.2 Second & Third Display Interface

Pin #	HDMI signal names	DP++ signal names
P92	HDMI_D2+	~~DP1_LANE0+~~
P93	HDMI_D2-	~~DP1_LANE0-~~
P95	HDMI_D1+	~~DP1_LANE1+~~
P96	HDMI_D1-	~~DP1_LANE1-~~
P98	HDMI_D0+	~~DP1_LANE2+~~
P99	HDMI_D0-	~~DP1_LANE2-~~
P101	HDMI_CK+	~~DP1_LANE3+~~
P102	HDMI_CK-	~~DP1_LANE3-~~
S105	HDMI_CTRL_CK	~~DP1_AUX+~~
S106	HDMI_CTRL_DAT	~~DP1_AUX-~~
P104	HDMI_HPD	~~DP1_HPD~~
P107	-	~~DP1_AUX_SEL~~

Pin #	DP++ signal names
P92	~~DP0_LANE0+~~
P93	~~DP0_LANE0-~~
P95	~~DP0_LANE1+~~
P96	~~DP0_LANE1-~~
P98	~~DP0_LANE2+~~
P99	~~DP0_LANE2-~~
P101	~~DP0_LANE3+~~
P102	~~DP0_LANE3-~~
S105	~~DP0_AUX+~~
S106	~~DP0_AUX-~~
P104	~~DP0_HPD~~
P107	~~DP0_AUX_SEL~~

Note: DisplayPort is not supported

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4.3.2.1 HDMI

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
HDMI_D2+ HDMI_D2- HDMI_D1+ HDMI_D1- HDMI_D0+ HDMI_D0-	P92 P93 P95 P96 P98 P99	HDMI port, differential pair data lines	O TMDS HDMI		Runtime		AC coupled off module
HDMI_CK+ HDMI_CK-	P101 P102	HDMI port, differential pair clock lines	O TMDS HDMI		Runtime		AC coupled off module
HDMI_CTRL_CK	P105	I2C_CLK line dedicated to HDMI	O OD COMS	1.8V	Runtime	PU 2.2	Level shifter FET and 5V PU resistor shall be placed between the module and the HDMI connector.
HDMI_CTRL_DAT	P106	I2C_DAT line dedicated to HDMI	I/O OD COMS	1.8V	Runtime	PU 2.2K	Level shifter FET and 5V PU resistor shall be placed between the module and the HDMI connector.
HDMI_HPD	P104	HDMI Hot plug active high detection signal that serves as an interrupt request	I CMOS	1.8V	Standby		Module must tolerate high level in stand-by mode

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4.3.3 MIPI Camera support

4.3.3.1 MIPI CSI0

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
~~CSI0_RX0+~~ ~~CSI0_RX0-~~ ~~CSI0_RX1+~~ ~~CSI0_RX1-~~	~~S11~~ ~~S12~~ ~~S14~~ ~~S15~~	~~CSI0 differential input (point to point)~~	~~I LVDS D-PHY / I LVDS M-PHY~~	-	~~Runtime~~	-	-
~~CSI0_CK+~~ ~~CSI0_CK-~~	~~S8~~ ~~S9~~	~~CSI0 differential clock intput (point to point)~~	~~I LVDS D-PHY~~	-	~~Runtime~~	-	-
~~I2C_CAM0_DAT / CSI0_TX-~~	~~S7~~	~~I2C data for serial camera data support link or differential data lane~~	~~I/O OD CMOS / O LVDS M-PHY~~	~~1.8V~~	~~Runtime~~	~~PU 2.2K~~	~~MIPI-CSI 2.0 uses I2C_CAM0_DAT~~ ~~MIPI-CSI 3.0 uses CSI0_TX-~~
~~I2C_CAM0_CK / CSI0_TX+~~	~~S5~~	~~I2C clock for serial camera data support link or differential data lane~~	~~O OD CMOS / O LVDS M-PHY~~	~~1.8V~~	~~Runtime~~	~~PU 2.2K~~	~~MIPI-CSI 2.0 uses I2C_CAM0_CK~~ ~~MIPI-CSI 3.0 uses CSI0_TX+~~
~~CAM0_PWR# / GPIO0~~	~~P108~~	~~Camera 0 Power Enable, active low output.~~	~~O CMOS~~	~~1.8V~~	~~Runtime~~	-	-
~~CAM0_RST# / GPIO2~~	~~P110~~	~~Camera 0 reset, active low output~~	~~O CMOS~~	~~1.8V~~	~~Runtime~~	-	-
CAM_MCK	S6	Master clock output	O CMOS	1.8V	Runtime		This signal is used by both CSI0 and CSI1

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4.3.3.2 MIPI CSI1 (Camera)

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CSI1_RX0+ CSI1_RX0- CSI1_RX1+ CSI1_RX1- CSI1_RX2+ CSI1_RX2- CSI1_RX3+ CSI1_RX3-	P7 P8 P10 P11 P13 P14 P16 P17	CSI1 differential input (point to point)	I LVDS D-PHY / I LVDS M-PHY		Runtime		Solo / Duallite limited to 2 data lines
CSI1_CK+ CSI1_CK-	P3 P4	CSI1 differential clock input (point to point)	I LVDS D-PHY		Runtime		
I2C_CAM1_DAT / ~~CSI1_TX-~~	S2	I2C data for serial camera data support link or differential data lane	I/O OD CMOS / O LVDS M-PHY	1.8V	Runtime	PU 2.2K	MIPI-CSI 2.0 mode uses I2C_CAM1_DAT MIPI-CSI 3.0 mode uses CSI1_TX-
I2C_CAM1_CK / ~~CSI1_TX+~~	S1	I2C clock for serial camera data support link or differential data lane	O OD CMOS / O LVDS M-PHY	1.8V	Runtime	PU 2.2K	MIPI-CSI 2.0 mode uses I2C_CAM1_CK MIPI-CSI 3.0 mode uses CSI1_TX+
CAM1_PWR# / GPIO1	P109	Camera 0 Power Enable, active low output.	O CMOS	1.8V	Runtime		CAM1_PWR# is default, GPIO1 can be enabled through DVT
CAM1_RST# / GPIO3	P111	Camera 0 reset, active low output	O CMOS	1.8V	Runtime		CAM1_PWR# is default, GPIO3 can be enabled through DVT
CAM_MCK	S6	Master clock output	O CMOS	1.8V	Runtime		This signal is used by both CSI0 and CSI1

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4.3.4 I2S (audio)

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
I2S0_LRCK	S39	I2S0 Left & Right synchronization clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
I2S0_SDOUT	S40	I2S0 Digital audio Output	O CMOS	1.8V	Runtime		
I2S0_SDIN	S41	I2S0 Digital audio Input	I CMOS	1.8V	Runtime		
I2S0_CK	S42	I2S0 Digital audio clock	I/O CMOS	1.8V	Runtime		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
~~I2S2_LRCK~~	~~S50~~	~~I2S2 Left & Right synchronization clock~~	~~I/O CMOS~~	~~1.8V~~	~~Runtime~~		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
~~I2S2_SDOUT~~	~~S51~~	~~I2S2 Digital audio Output~~	~~O CMOS~~	~~1.8V~~	~~Runtime~~		
~~I2S2_SDIN~~	~~S52~~	~~I2S2 Digital audio Input~~	~~I CMOS~~	~~1.8V~~	~~Runtime~~		
~~I2S2_CK~~	~~S53~~	~~I2S2 Digital audio clock~~	~~I/O CMOS~~	~~1.8V~~	~~Runtime~~		Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
AUDIO_MCK	S38	Master clock output to I2S codec(s)	O CMOS	1.8V	Runtime		

Note: support for I2S1 signalling pins has been removed during update to SMARC 2.0 specification

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4.3.5 USB ports

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Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
USB0+ USB0-	P60 P61	USB differential data pairs for port 0	I/O USB	USB	Runtime		From SOC
USB0_EN_OC#	P62	USB over-current sense for port 0	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB0_VBUS_DET	P63	USB port 0 host power detection, when this port is used as a device.	I USB VBUS 5V	USB VBUS 5V	Runtime		Can be connected to a USB client port VBUS pin
USB0_OTG_ID	P64	Input pin to announce OTG device insertion on USB 2.0 port	I CMOS	3.3Vsb / 3.3V	Runtime		
USB1+ USB1-	P65 P66	USB differential data pairs for port 1	I/O USB	USB	Runtime		From USB HUB
USB1_EN_OC#	P67	USB over-current sense for port 1	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB2+ USB2-	P69 P70	USB differential data pairs for port 2	I/O USB	USB	Runtime		From USB HUB
~~USB2_SSRX+ USB2_SSRX-~~	~~S74 S75~~	~~Receive signal differential pairs for SuperSpeed on port 2~~	~~I USB SS~~	~~USB SS~~	~~Runtime~~	-	
~~USB2_SSTX+ USB2_SSTX-~~	~~S71 S72~~	~~Transmit signal differential pairs for SuperSpeed on port 2~~	~~O USB SS~~	~~USB SS~~	~~Runtime~~	-	
USB2_EN_OC#	P71	USB over-current sense for port 2	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
USB3+ USB3-	S68 S69	USB differential data pairs for port 3	I/O USB	USB	Runtime		From USB HUB
~~USB3_SSRX+ USB3_SSRX-~~	~~S65 S66~~	~~Receive signal differential pairs for SuperSpeed on port 3~~	~~I USB SS~~	~~USB SS~~	~~Runtime~~	-	

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~~USB3_SSTX+ USB3_SSTX-~~	~~S62 S63~~	~~Transmit signal differential pairs for SuperSpeed on port 3~~	~~O USB SS~~	~~USB SS~~	~~Runtime~~	-	
USB3_EN_OC#	P74	USB over-current sense for port 3	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
~~USB3_VBUS_DET~~	~~S37~~	~~USB port 3 host power detection, when this port is used as a device.~~	~~I USB VBUS 5V~~	~~USB VBUS 5V~~	~~Runtime~~	-	-
~~USB3_OTG_ID~~	~~S104~~	~~Input pin to announce OTG device insertion on USB 3.0 port~~	~~I CMOS~~	~~3.3Vsb / 3.3V~~	~~Runtime~~	-	-

USB4+ USB4-	S35 S36	USB differential data pairs for port 4	I/O USB	USB	Runtime		
USB4_EN_OC#	P76	USB over-current sense for port 4	I/O OD CMOS	3.3Vsb / 3.3V	Runtime	PU 10k	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.

~~USB5+ USB5-~~	~~S59 S60~~	~~USB differential data pairs for port 5~~	~~I/O USB~~	~~USB~~	~~Standby~~	-	
~~USB5_EN_OC#~~	~~S55~~	~~USB over-current sense for port 5~~	~~I/O OD CMOS~~	~~3.3Vsb / 3.3V~~	~~Standby~~	~~PU 10k~~	~~Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.~~

Note: USB0 is directly connected to the SOC, USB1/2/3/4 have shared bandwidth through a HUB, USB5 is not supported

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4.3.6 PCIe Ports

The module supports two PCIe Gen 2.1 ports (PCIE_A and PCIE_B).

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
PCIE_A_TX+ PCIE_A_TX-	P89 P90	Differential PCIe link A transmit data pair	O LVDS PCIE		Runtime		Series AC coupled on module
PCIE_A_RX+ PCIE_A_RX-	P86 P87	Differential PCIe link A receive data pair	I LVDS PCIE		Runtime		Series AC coupled off module
PCIE_A_REFCK+ PCIE_A_REFCK-	P83 P84	Differential PCIe Link A reference clock output	O LVDS PCIE		Runtime		
PCIE_A_RST#	P75	PCIe Port A reset output	O CMOS	3.3V	Runtime		
~~PCIE_A_CKREQ#~~	~~P78~~	~~PCIe Port A clock request~~	~~I OD CMOS~~	~~3.3V~~	~~Runtime~~	-	No need for this signal because module provides onboard PCIe clock
~~PCIE_B_TX+ PCIE_B_TX-~~	~~S90 S91~~	~~Differential PCIe link B transmit data pair~~	~~O LVDS PCIE~~	-	~~Runtime~~	-	~~Series AC coupled on module~~
~~PCIE_B_RX+ PCIE_B_RX-~~	~~S87 S88~~	~~Differential PCIe link B receive data pair~~	~~I LVDS PCIE~~	-	~~Runtime~~	-	~~Series AC coupled off module~~
~~PCIE_B_REFCK+ PCIE_B_REFCK-~~	~~S84 S85~~	~~Differential PCIe Link B reference clock output~~	~~O LVDS PCIE~~	-	~~Runtime~~	-	-
~~PCIE_B_RST#~~	~~S76~~	~~PCIe Port B reset output~~	~~O CMOS~~	~~3.3V~~	~~Runtime~~	-	-
~~PCIE_B_CKREQ#~~	~~P77~~	~~PCIe Port B clock request~~	~~I OD CMOS~~	~~3.3V~~	~~Runtime~~		No need for this signal because module provides onboard PCIe clock
~~PCIE_C_TX+ PCIE_C_TX-~~	~~S81 S82~~	~~Differential PCIe link C transmit data pair~~	~~O LVDS PCIE~~	-	~~Runtime~~	-	~~Series AC coupled on module~~
~~PCIE_C_RX+ PCIE_C_RX-~~	~~S78 S79~~	~~Differential PCIe link C receive data pair~~	~~I LVDS PCIE~~	-	~~Runtime~~	-	~~Series AC coupled off module~~
~~PCIE_C_REFCK+ PCIE_C_REFCK-~~	~~P80 P81~~	~~Differential PCIe Link C reference clock output~~	~~O LVDS PCIE~~	-	~~Runtime~~	-	-
~~PCIE_C_RST#~~	~~S77~~	~~PCIe Port C reset output~~	~~O CMOS~~	~~3.3V~~	~~Runtime~~	-	-

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Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
~~PCIE_D_TX+~~ ~~PCIE_D_TX-~~	~~S29~~ ~~S30~~	~~Differential PCIe link D transmit data pair~~	~~O LVDS PCIE~~	-	~~Runtime~~	-	~~Series AC coupled on module~~
~~PCIE_D_RX+~~ ~~PCIE_D_RX-~~	~~S32~~ ~~S33~~	~~Differential PCIe link D receive data pair~~	~~I LVDS PCIE~~	-	~~Runtime~~	-	~~Series AC coupled off module~~
PCIE_WAKE#	S146	PCIe wake up interrupt to host – common to PCIe links A, B, C, D	I OD CMOS	3.3V	Runtime	PU 10k	

Note: Module provides PCIe clock generators for PCIE_A so no external clock source on the carrier is needed

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4.3.7 SATA Ports

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SATA0_TX+ SATA0_TX-	P48 P49	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Runtime		Series AC coupled on Module 10 nF
SATA0_RX+ SATA0_RX-	P51 P52	Serial ATA channel 0, Receive Input differential pair.	I SATA		Runtime		Series AC coupled on Module 10 nF
SATA_ACT#	S54	SATA activity indicator	O OD CMOS	3.3V	Runtime		Shall be able to sink 24mA or more Carrier LED current

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4.3.8 LAN ports

4.3.8.1 First LAN port

The first LAN port is derived from the SOCs RGMII interface

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	P30 P29 P27 P26 P24 P23 P20 P19	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: 1000 / 100 / 10 MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	GBE MDI		Runtime		Twisted pair signals for external transformer.
GBE0_LINK100#	P21	Link Speed Indication LED for GBE 0 100Mbps	O OD CMOS	3.3V	Runtime		Shall be able to sink 24mA or more Carrier LED current
GBE0_LINK1000#	P22	Link Speed Indication LED for GBE 0 1000Mbps	O OD CMOS	3.3V	Runtime		Shall be able to sink 24mA or more Carrier LED current
GBE0_LINK_ACT#	P25	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity	O OD CMOS	3.3V	Runtime		Shall be able to sink 24mA or more Carrier LED current
~~GBE0_CTREF~~	~~P28~~	~~Center-Tap reference voltage for Carrier board Ethernet magnetic (if required by the Module GBE PHY)~~	~~Analog~~	~~0 to 3.3V max~~	Runtime	-	-
~~GBE0_SDP~~	~~P6~~	~~IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol)~~	~~IO CMOS~~	~~3.3V~~	Runtime		

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4.3.8.2 Second LAN port

Second LAN port is derived from USB hub

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GBE1_MDI0+ GBE1_MDI0- GBE1_MDI1+ GBE1_MDI1- ~~GBE1_MDI2+~~ ~~GBE1_MDI2-~~ ~~GBE1_MDI3+~~ ~~GBE1_MDI3-~~	S17 S18 S20 S21 ~~S23~~ ~~S24~~ ~~S26~~ ~~S27~~	Gigabit Ethernet Controller 1: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: 1000 100 10 MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	GBE MDI		Runtime		Twisted pair signals for external transformer.
GBE1_LINK100#	S19	Link Speed Indication LED for GBE 1 100Mbps	O OD CMOS	3.3V	Runtime		Shall be able to sink 24mA or more Carrier LED current
~~GBE1_LINK1000#~~	~~S22~~	~~Link Speed Indication LED for GBE 1 1000Mbps~~	~~O OD CMOS~~	~~3.3V~~	~~Runtime~~	-	~~Shall be able to sink 24mA or more Carrier LED current~~
~~GBE1_LINK_ACT#~~	~~S31~~	~~Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity~~	~~O OD CMOS~~	~~3.3V~~	~~Runtime~~	-	~~Shall be able to sink 24mA or more Carrier LED current~~
~~GBE1_CTREF~~	~~S28~~	~~Center-Tap reference voltage for Carrier board Ethernet magnetic `(if required by the Module GBE PHY)`~~	~~Analog~~	~~0 to 3.3V max~~	~~Runtime~~		
~~GBE1_SDP~~	~~P5~~	~~IEEE 1588 Trigger Signal. For hardware implementation of PTP (precision time protocol)~~	~~IO CMOS~~	~~3.3V~~	~~Runtime~~		

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4.3.9 SDIO

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SDIO_D0 SDIO_D1 SDIO_D2 SDIO_D3	P39 P40 P41 P42	SDIO Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V	Runtime		SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly
SDIO_WP	P33	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I OD CMOS	3.3V	Runtime	PU 10k	Pulled up on module
SDIO_CMD	P34	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O CMOS	1.8V or 3.3V	Runtime		SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly
SDIO_CD#	P35	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	I OD CMOS	3.3V	Runtime	PU 10k	Pulled up on module
SDIO_CK	P36	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.	O CMOS	1.8V or 3.3V	Runtime		
~~SDIO_PWR_EN~~	~~P37~~	~~SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.~~	~~O CMOS~~	~~3.3V~~	~~Runtime~~	-	~~should be driven low in STB Mode by the module~~

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4.3.10 SPI & ESPI

4.3.11 SPI0

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SPI0_CS0#	P43	SPI0 Master Chip Select 0	O CMOS	1.8V	Standby		This signal can be used to select carrier SPI as boot device
SPI0_CS1#	P31	SPI0 Master Chip Select 1	O CMOS	1.8V	Standby		
SPI0_CK	P44	SPI0 Clock	O CMOS	1.8V	Standby		-
SPI0_DIN	P45	SPI0 Master input / Slave output	I CMOS	1.8V	Standby		also referred to as MISO
SPI0_DO	P46	SPI0 Master output / Slave input	O CMOS	1.8V	Standby		also referred to as MOSI

~~SPI1_CS0#~~	~~P54~~	~~SPI1 Master Chip Select 0~~	~~O CMOS~~	~~1.8V~~	~~Standby~~	-	See ESPI
~~SPI1_CS1#~~	~~P55~~	~~SPI1 Master Chip Select 1~~	~~O CMOS~~	~~1.8V~~	~~Standby~~	-	See ESPI
~~SPI1_CK~~	~~P56~~	~~SPI1 Clock~~	~~O CMOS~~	~~1.8V~~	~~Standby~~	-	See ESPI
~~SPI1_DIN~~	~~P57~~	~~SPI1 Master input / Slave output~~	~~I CMOS~~	~~1.8V~~	~~Standby~~	-	See ESPI
~~SPI1_DO~~	~~P58~~	~~SPI1 Master output / Slave input~~	~~O CMOS~~	~~1.8V~~	~~Standby~~	-	See ESPI

Note: SPI0 is free to use on the carrier but support only one device through CS0

SPI1 supports a CAN bus controller on the module through CS0, that leaves CS1 free for a device on the carrier

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4.3.12 ESPI

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
ESPI_CS0#	P54	ESPI1 Master Chip Select 0	O CMOS	1.8V	Standby		
ESPI_CS1#	P55	ESPI1 Master Chip Select 1	O CMOS	1.8V	Standby		
ESPI_CK	P56	ESPI Master Clock output	O CMOS	1.8V	Standby		
ESPI_RESET#	S58	ESPI Reset	O CMOS	1.8V	Standby		Reset the eSPI interface for both master and slaves. eSPI Reset# is typically driven from eSPI master to eSPI slaves
~~ESPI_ALERT0#~~ ~~ESPI_ALERT1#~~	~~S43~~ ~~S44~~	~~ESPI ALERT~~	~~I OD CMOS~~	~~1.8V~~	~~Standby~~		This pin is used by eSPI slave to request service from eSPI.master.Alert# is an open-drain output from the slave. This pin is optional for Single Master-Single Slave configuration where I/O[1] can be used to signal the Alert event.
~~ESPI_IO_0~~ ~~ESPI_IO_1~~ ~~ESPI_IO_2~~ ~~ESPI_IO_3~~	~~P58~~ ~~P57~~ ~~S56~~ ~~S57~~	~~ESPI Master Data Input / Output.~~	~~I/O CMOS~~	~~1.8V~~	~~Standby~~		ESPI_IO_0 can also be used as SPI1_DO (MOSI) ESPI_IO_1 can also be used as SPI1_DIN (MISO) In Single I/O mode, ESPI_IO_0 is the eSPI master output / eSPI slave input (MOSI) whereas ESPI_IO_1 is the SPI master input / eSPI slave output (MISO).

Note: On NXP i.MX8M parts ECSPI is used (Enhanced Configurable Serial Peripheral Interface)

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4.4 General Purpose I2C

The SMARC specification supports a total of 6 different I2C busses on its pinout. Most of these busses are designated for specific functions such as I2C for camera management, I2C for EDID on HDMI, LVDS panels or I2C for PMIC. Just one I2C bus is marked as General purpose

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
I2C_GP_DAT	S49	General purpose I2C data signal	I/O OD CMOS	1.8V	Runtime	PU 2k2	
I2C_GP_CK	S48	General purpose I2C clock signal	O OD CMOS	1.8V	Runtime	PU 2k2	

Most of the other I2C busses are described in their designated function tables rather than in a single big list.

Below is an overview of all I2C busses and where to find them.

Name	Pin #	Description	Where to find
I2C_LCD_DAT	S140	DDC data line used for flat panel detection and control	LVDS / DSI / eDP tables
I2C_LCD_CK	S139	DDC clock line used for flat panel detection and control	LVDS / DSI / eDP tables
HDMI_CTRL_CK	P105	I2C_CLK line dedicated to HDMI	HDMI table
HDMI_CTRL_DAT	P106	I2C_DAT line dedicated to HDMI	HDMI table
I2C_CAM0_DAT	S7	I2C data for serial camera data support link	MIPI CSI table
I2C_CAM0_CK	S5	I2C clock for serial camera data support link	MIPI CSI table
I2C_CAM1_DAT	S2	I2C data for serial camera data support link	MIPI CSI table
I2C_CAM1_CK	S1	I2C clock for serial camera data support link	MIPI CSI table
I2C_PM_DAT	P122	Power management I2C bus DATA (SMBus for x86)	Power and System Management
I2C_PM_CK	P121	Power management I2C bus CLK (SMBus for x86)	Power and System Management

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4.4.1 GPIO

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
GPIO0 / CAM0_PWR#	P108	General purpose I/O pin 0.	I/O CMOS	1.8V	Runtime	PU 470K on the Module.	Default use is GPIO0, alternative use is Camera 0 Power Enable - active low, through DTS
GPIO1 / CAM1_PWR#	P109	General purpose I/O pin 1.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	Default use is is GPIO1 alternative use is Camera 1 Power Enable - active low, through DTS
GPIO2 / CAM0_RST#	P110	General purpose I/O pin 2.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	Default use is GPIO2, alternative use is Camera 0 Reset - active low, through DTS
GPIO3 / CAM1_RST#	P111	General purpose I/O pin 3.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	Default use is GPIO3, alternative use is Camera 1 Reset - active low, through DTS
GPIO4 / ~~HDA_RST#~~	P112	General purpose I/O pin 4.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO5 / ~~PWM_OUT~~	P113	General purpose I/O pin 5.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO6	P114	General purpose I/O pin 6.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO7	P115	General purpose I/O pin 7.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO8	P116	General purpose I/O pin 8.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO9	P117	General purpose I/O pin 9.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO10	P118	General purpose I/O pin 10.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO11	P119	General purpose I/O pin 11.	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO12	S142	General purpose I/O pin 12	I/O CMOS	1.8V	Runtime	PU 470K on the Module	
GPIO13	S123	General purpose I/O pin 13	I/O CMOS	1.8V	Runtime	PU 470K on the Module	

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4.4.2 UART

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
SER0_TX	P129	Asynchronous serial data output port 0	O CMOS	1.8V	Runtime		
SER0_RX	P130	Asynchronous serial data input port 0	I CMOS	1.8V	Runtime		
SER0_RTS#	P131	"Request to Send" handshake line for port 0	O CMOS	1.8V	Runtime		
SER0_CTS#	P132	"Clear to Send" handshake line for port 0	I CMOS	1.8V	Runtime		
SER1_TX	P134	Asynchronous serial data output port 1	O CMOS	1.8V	Runtime		
SER1_RX	P135	Asynchronous serial data input port 1	I CMOS	1.8V	Runtime		
SER2_TX	P136	Asynchronous serial data output port 2	O CMOS	1.8V	Runtime	-	-
SER2_RX	P137	Asynchronous serial data input port 2	I CMOS	1.8V	Runtime	-	-
SER2_RTS#	P138	"Request to Send" handshake line for port 2	O CMOS	1.8V	Runtime	-	-
SER2_CTS#	P139	"Clear to Send" handshake line for port 2	I CMOS	1.8V	Runtime	-	-
SER3_TX	P140	Asynchronous serial data output port 3	O CMOS	1.8V	Runtime		
SER3_RX	P141	Asynchronous serial data input port 3	I CMOS	1.8V	Runtime		

Four asynchronous serial ports are supported. The ports are designated SER0 – SER3. Ports SER0 and SER2 are 4 wire ports, (2 data - and 2 handshake lines). Ports SER1 and SER3 are 2 wire ports (data only).

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4.4.3 CAN bus

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
CAN0_TX	P143	CAN port 0 Transmit output	O CMOS	1.8V	Runtime		
CAN0_RX	P144	CAN port 0 Receive input	I CMOS	1.8V	Runtime		
CAN1_TX	P145	CAN port 1 Transmit output	O CMOS	1.8V	Runtime		
CAN1_RX	P146	CAN port1 Receive input	I CMOS	1.8V	Runtime		

4.4.4 Miscellaneous

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
TEST#	S157	Held low by Carrier to invoke Module vendor specific test function(s).	I CMOS	1.8V	Runtime	PU 47	Module must implement PU but actual value is depended on particular module design. Carrier Board should leave this pin floating for normal operation
WDT_TIME_OUT#	S145	Watch-Dog-Timer Output, low active.	O CMOS	1.8V	Runtime		Driven only during runtime

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4.4.5 Power and System Management

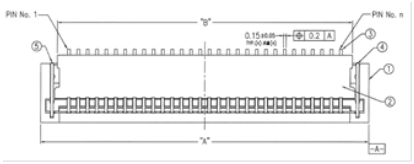
Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
BATLOW#	S156	Battery low indication to Module. Carrier to float the line in inactive state.	I OD CMOS	1.8 to 5V	Standby/Sleep	PU 10k	Driven by OD on Carrier
CARRIER_PWR_ON	S154	Carrier Board circuits (apart from power management and power path circuits) ***Should Not*** be powered up until the Module asserts the CARRIER_PWR_ON signal.	O CMOS	1.8Vsb / 1.8V	Standby		On x86 designs this pin should utilize a standby related power signal i.e. RSM_RST# or SLP_A# signal.
CARRIER_STBY#	S153	The Module ***Shall*** drive this signal low when the system is in a standby power state.	O CMOS	1.8V	Standby		On x86 designs this pin should utilize the SUS_S3# signal.
CHARGER_PRSNT#	S152	Held low by Carrier if DC input for battery charger is present.	I OD CMOS	1.8 to 5V	Standby/Sleep	PU 10k	Driven by OD on Carrier.
CHARGING#	S151	Held low by Carrier during battery charging. Carrier to float the line when charge is complete.	I OD CMOS	1.8 to 5V	Standby/Sleep	PU 10k	Driven by OD on Carrier.
VIN_PWR_BAD#	S150	Power bad indication from Carrier Board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) ***Shall Not*** be enabled while this signal is held low by the Carrier.	I OD CMOS	VDD_IN		PU 10k	Module must implement PU but actual value is depended on particular Module design. Driven by OD on Carrier
SLEEP#	S149	Sleep indicator from Carrier Board. ***May*** be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. ***Should*** be de-bounced on the Module.	I OD CMOS	1.8 to 5V	Standby	PU 10k	Driven by OD on Carrier.
LID#	S148	Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. ***Should*** be de-bounced on the Module.	I OD CMOS	1.8 to 5V	Standby	PU 10k	Driven by OD on Carrier.
POWER_BTN#	P128	Power-button input from Carrier board. Carrier to float the line in in-active state. Active low, level sensitive. ***Should*** be debounced on the Module.	I OD CMOS	1.8 to 5V	Sleep	PU 10k	Driven by OD on Carrier.

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Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
RESET_OUT#	P126	General purpose reset output to Carrier board.	O CMOS	1.8V	Runtime		
RESET_IN#	P127	Reset input from Carrier Board. Carrier drives low to force a Module reset, floats the line otherwise. This signal ***Shall*** be level triggered during bootup to allow to stop booting of the module. After bootup it ***May*** act as an edge triggered signal.	I OD CMOS	1.8 to 5V	Standby	PU 10k	Driven by OD on Carrier.
I2C_PM_DAT	P122	Power management I2C bus DATA	I/O OD CMOS	1.8V	Runtime	PU 2k2	On x86 systems these serve as SMB DATA. Pulled up on module.
I2C_PM_CK	P121	Power management I2C bus CLK	O OD CMOS	1.8V	Runtime	PU 2k2	On x86 systems these serve as SMB CLK. Pulled up on module.
~~SMB_ALERT_1V8#~~	P1	~~SMBus Alert# (interrupt) signal~~	~~I OD CMOS~~	~~1.8V~~	~~Runtime~~	~~PU 2k2~~	~~only used on x86 design~~

4.4.6 DB30 Multipurpose Connector

- **FPC Connector type :** HIROSE,FH12-30S-0.5SH(55)



DB30 connector brings out the following type of signals

SPI0 bus

JTAG to SOC

Boot Select strap pins

BMC programming interface

Serial port

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4.4.7 Boot Select

Name	Pin #	Description	I/O Type	I/O Level	Power Domain	PU / PD	Comments
BOOT_SEL0# BOOT_SEL1# BOOT_SEL2#	P123 P124 P125	Input straps determine the Module boot	I OD CMOS	1.8Vsb	Standby	PU 4.7K	Driven by OD on Carrier. Pulled up on module. Only booting from EMMc and SDcard is supported
~~FORCE_RECOV#~~	S155		~~I OD CMOS~~	~~1.8Vsb~~	~~Standby~~	~~PU 10K~~ -	~~Driven by OD on Carrier.~~ ~~Pulled up on module.~~ ~~Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked. Pulled high on the Module. For SOCs that do not implement a USB based Force Recovery functions, then a low on the Module FORCE_RECOV# pin may invoke the SOC native Force Recovery mode – such as over a Serial Port. For x86 systems this signal may be used to load BIOS defaults. Pulled up on Module. Driven by OD part on Carrier.~~

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4.4.8 Power

Name	Pin #	Description	I/O Type	Power Rail / Tolerance	PU / PD	Comments
VDD_IN	P147, P148, P149, P150, P151, P152, P153, P154, P155, P156	Module power input voltage 4.75 min to 5.25V max		3 to 5.25V / 5V		
GND	P2, P9, P12, P15, P18, P32, P38, P47, P50, P53, P59, P68, P79, P82, P85, P88, P91, P94, P97, P100, P103, P120, P133, P142, S3, S10, S16, S25, S34, S47, S61, S64, S67, S70, S73, S80, S83, S86, S89, S92, S101, S110, S119, S124, S130, S136, S143, S158	Module signal and power return, and GND reference		Ground		
VDD_RTC	S147	Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based Lithium cell or Super Cap.		[2 to 3.25] / 3.25V		

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4.5 SMARC pin to controller mapping

Pin	SMARC Signal Name	Module Direction	Module Termination	Type/Tolerance	Controller	Controller Pin Name	I/O Mux default	Power Rail
P1	SMB_ALERT_1V8#	-	-					
P2	GND	-	-					
P3	CSI1_CK+	In	-	LVDS D-PHY	i.MX6 QP/Q/DP/D/DL/S	CSI_CLK0P	-	NVCC_MIPI
P4	CSI1_CK-	In	-	LVDS D-PHY	i.MX6 QP/Q/DP/D/DL/S	CSI_CLK0M	-	NVCC_MIPI
P5	GBE1_SDP	-	-					
P6	GBE0_SDP	-	-					
P7	CSI1_RX0+	In	-	LVDS D-PHY	i.MX6 QP/Q/DP/D/DL/S	CSI_D0P	-	NVCC_MIPI
P8	CSI1_RX0-	In	-	LVDS D-PHY	i.MX6 QP/Q/DP/D/DL/S	CSI_D0M	-	NVCC_MIPI
P9	GND	-	-					
P10	CSI1_RX1+	In	-	LVDS D-PHY	i.MX6 QP/Q/DP/D/DL/S	CSI_D1P	-	NVCC_MIPI
P11	CSI1_RX1-	In	-	LVDS D-PHY	i.MX6 QP/Q/DP/D/DL/S	CSI_D1M	-	NVCC_MIPI
P12	GND	-	-					
P13	CSI1_RX2+	In	-	LVDS D-PHY	i.MX6 QP/Q/DP/D	CSI_D2P	-	NVCC_MIPI
P14	CSI1_RX2-	In	-	LVDS D-PHY	i.MX6 QP/Q/DP/D	CSI_D2M	-	NVCC_MIPI
P15	GND	-	-					
P16	CSI1_RX3+	In	-	LVDS D-PHY	i.MX6 QP/Q/DP/D	CSI_D3P	-	NVCC_MIPI
P17	CSI1_RX3-	In	-	LVDS D-PHY	i.MX6 QP/Q/DP/D	CSI_D3M	-	NVCC_MIPI
P18	GND	-	-					
P19	GBE0_MDI3-	Bi-Dir	-	GBE MDI	AR8035-AL1B	TRXN3	-	NVCC_RGMII
P20	GBE0_MDI3+	Bi-Dir	-	GBE MDI	AR8035-AL1B	TRXP3	-	NVCC_RGMII
P21	GBE0_LINK100#	Out/OD	-	CMOS/3.3V	AR8035-AL1B	LED_10_100	-	NVCC_RGMII
P22	GBE0_LINK1000#	Out/OD	-	CMOS/3.3V	AR8035-AL1B	LED_1000	-	NVCC_RGMII
P23	GBE0_MDI2-	Bi-Dir	-	GBE MDI	AR8035-AL1B	TRXN2	-	NVCC_RGMII
P24	GBE0_MDI2+	Bi-Dir	-	GBE MDI	AR8035-AL1B	TRXP2	-	NVCC_RGMII
P25	GBE0_LINK_ACT#	Out/OD	-	CMOS/3.3V	AR8035-AL1B	LED_ACT	-	NVCC_RGMII
P26	GBE0_MDI1-	Bi-Dir	-	GBE MDI	AR8035-AL1B	TRXN1	-	NVCC_RGMII
P27	GBE0_MDI1+	Bi-Dir	-	GBE MDI	AR8035-AL1B	TRXP1	-	NVCC_RGMII
P28	GBE0_CTREF	-	-					

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P29	GBE0_MDI0-	Bi-Dir	-	GBE MDI	AR8035-AL1B	TRXN0	-	NVCC_RGMII
P30	GBE0_MDI0+	Bi-Dir	-	GBE MDI	AR8035-AL1B	TRXP0	-	NVCC_RGMII
P31	SPI0_CS1#	Out	-	CMOS/1.8V	i.MX6	DISP0_DAT4	Alt2	NVCC_LCD
P32	GND	-	-					
P33	SDIO_WP	In	-	CMOS/3.3V	i.MX6 QP/Q/DP/D/DL/S	GPIO_2	Alt6	NVCC_GPIO
P34	SDIO_CMD	Bi-Dir	-	CMOS/3.3V	i.MX6 QP/Q/DP/D/DL/S	SD2_CMD	Alt0	NVCC_SD2
P35	SDIO_CD#	In	-	CMOS/3.3V	i.MX6 QP/Q/DP/D/DL/S	GPIO_4	Alt6	NVCC_SD2
P36	SDIO_CK	Out	-	CMOS/3.3V	i.MX6 QP/Q/DP/D/DL/S	SD2_CLK	Alt0	NVCC_SD2
P37	SDIO_PWR_EN	Out	-	CMOS/3.3V	i.MX6 QP/Q/DP/D/DL/S	KEY_COL2	Alt5	NVCC_GPIO
P38	GND	-	-	CMOS/3.3V				
P39	SDIO_D0	Bi-Dir	-	CMOS/3.3V	i.MX6 QP/Q/DP/D/DL/S	SD2_DAT0	Alt0	NVCC_SD2
P40	SDIO_D1	Bi-Dir	-	CMOS/3.3V	i.MX6 QP/Q/DP/D/DL/S	SD2_DAT1	Alt0	NVCC_SD2
P41	SDIO_D2	Bi-Dir	-	CMOS/3.3V	i.MX6 QP/Q/DP/D/DL/S	SD2_DAT2	Alt0	NVCC_SD2
P42	SDIO_D3	Bi-Dir	-	CMOS/3.3V	i.MX6 QP/Q/DP/D/DL/S	SD2_DAT3	Alt0	NVCC_SD2
P43	SPI0_CS0#	Out	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	DISP0_DAT3	Alt2	NVCC_LCD
P44	SPI0_CK	Out	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	DISP0_DAT0	Alt2	NVCC_LCD
P45	SPI0_DIN	In	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	DISP0_DAT2	Alt2	NVCC_LCD
P46	SPI0_DO	Out	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	DISP0_DAT1	Alt2	NVCC_LCD
P47	GND	-	-					
P48	SATA_TX+	Out	serial-0.1u	SATA	i.MX6 QP/Q/DP/D	SATA_TXP	-	SATA_VPH
P49	SATA_TX-	Out	serial-0.1u	SATA	i.MX6 QP/Q/DP/D	SATA_TXM	-	SATA_VPH
P50	GND	-	-					
P51	SATA_RX+	In	serial-0.1u	SATA	i.MX6 QP/Q/DP/D	SATA_RXP	-	SATA_VPH
P52	SATA_RX-	In	serial-0.1u	SATA	i.MX6 QP/Q/DP/D	SATA_RXM	-	SATA_VPH
P53	GND	-	-					
P54	ESPI_CS0# / SPI1_CS0#	Out	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	EIM_RW	Alt2	NVCC_EIM1
P55	ESPI_CS1# / SPI1_CS1#	Out	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	EIM_LBA	Alt2	NVCC_EIM1
P56	ESPI_CK / SPI1_CK	Out	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	EIM_CS0	Alt2	NVCC_EIM1
P57	ESPI_IO_1 / SPI1_DIN	In	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	EIM_OE	Alt2	NVCC_EIM1
P58	ESPI_IO_0 / SPI1_DO	Out	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	EIM_CS1	Alt2	NVCC_EIM1
P59	GND	-	-					
P60	USB0+	Bi-Dir	-	USB	i.MX6 QP/Q/DP/D/DL/S	USB_OTG_DP	-	VDD_USB_CAP
P61	USB0-	Bi-Dir	-	USB	i.MX6 QP/Q/DP/D/DL/S	USB_OTG_DN	-	VDD_USB_CAP

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P62	USB0_EN_OC#	In	PU-10K	CMOS/3.3V	i.MX6 QP/Q/DP/D/DL/S	ENET_RXD0	Alt5	NVCC_ENET
P63	USB0_VBUS_DET	PWR	-	USB VBUS/5V	i.MX6 ??	USB_OTG_VBUS	-	-
P64	USB0_OTG_ID	In	-	CMOS/3.3V	i.MX6 QP/Q/DP/D/DL/S	ENET_RX_ER	Alt0	NVCC_ENET
P65	USB1+	Bi-Dir	-	USB	LAN9514-JZX	USBDP2	-	-
P66	USB1-	Bi-Dir	-	USB	LAN9514-JZX	USBDM2	-	-
P67	USB1_EN_OC#	In	PU-10K	CMOS/3.3V	LAN9514-JZX	PRTCTL2	-	-
P68	GND	-	-					
P69	USB2+	Bi-Dir	-	USB	LAN9514-JZX	USBDP3	-	-
P70	USB2-	Bi-Dir	-	USB	LAN9514-JZX	USBDM3	-	-
P71	USB2_EN_OC#	In	PU-10K	CMOS/3.3V	LAN9514-JZX	PRTCTL3	-	-
P72	RSVD	-	-					
P73	RSVD	-	-					
P74	USB3_EN_OC#	In	PU-10K	CMOS/3.3V	LAN9514-JZX	PRTCTL4	-	-
P75	PCIE_A_RST#	Out	-	CMOS/3.3V	i.MX6 QP/Q/DP/D/DL/S	GPIO_17	Alt5	NVCC_GPIO
P76	USB4_EN_OC#	In	PU-10K	CMOS/3.3V	LAN9514-JZX	PRTCTL5	-	-
P77	PCIE_B_CKREQ#	-	-					
P78	PCIE_A_CKREQ#	-	-					
P79	GND	-	-					
P80	PCIE_C_REFCK+	-	-					
P81	PCIE_C_REFCK-	-	-					
P82	GND	-	-					
P83	PCIE_A_REFCK+	Out	serial-0.1u, PD-49.9	PCIe	i.MX6 QP/Q/DP/D/DL/S	CLK1_P	-	VDD_HIGH_CAP
P84	PCIE_A_REFCK-	Out	serial-0.1u, PD-49.9	PCIe	i.MX6 QP/Q/DP/D/DL/S	CLK1_N	-	VDD_HIGH_CAP
P85	GND	-	-					
P86	PCIE_A_RX+	In	serial-0R	PCIe	i.MX6 QP/Q/DP/D/DL/S	PCIE_RXP	-	PCIE_VPH
P87	PCIE_A_RX-	In	serial-0R	PCIe	i.MX6 QP/Q/DP/D/DL/S	PCIE_RXM	-	PCIE_VPH
P88	GND	-	-					
P89	PCIE_A_TX+	Out	serial-0.1u	PCIe	i.MX6 QP/Q/DP/D/DL/S	PCIE_TXP	-	PCIE_VPH
P90	PCIE_A_TX-	Out	serial-0.1u	PCIe	i.MX6 QP/Q/DP/D/DL/S	PCIE_TXM	-	PCIE_VPH
P91	GND	-	-					
P92	HDMI_D2+ / DP1_LANE0+	Out	-	HDMI	i.MX6 QP/Q/DP/D/DL/S	HDMI_D2P	-	HDMI_VPH

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P93	HDMI_D2- / DP1_LANE0-	Out	-	HDMI	i.MX6 QP/Q/DP/D/DL/S	HDMI_D2M	-	HDMI_VPH
P94	GND	-	-					
P95	HDMI_D1+ / DP1_LANE1+	Out	-	HDMI	i.MX6 QP/Q/DP/D/DL/S	HDMI_D1P	-	HDMI_VPH
P96	HDMI_D1- / DP1_LANE1-	Out	-	HDMI	i.MX6 QP/Q/DP/D/DL/S	HDMI_D1M	-	HDMI_VPH
P97	GND	-	-					
P98	HDMI_D0+ / DP1_LANE2+	Out	-	HDMI	i.MX6 QP/Q/DP/D/DL/S	HDMI_D0P	-	HDMI_VPH
P99	HDMI_D0- / DP1_LANE2-	Out	-	HDMI	i.MX6 QP/Q/DP/D/DL/S	HDMI_D0M	-	HDMI_VPH
P100	GND	-	-					
P101	HDMI_CK+ / DP1_LANE3+	Out	-	HDMI	i.MX6 QP/Q/DP/D/DL/S	HDMI_CLKP	-	HDMI_VPH
P102	HDMI_CK- / DP1_LANE3-	Out	-	HDMI	i.MX6 QP/Q/DP/D/DL/S	HDMI_CLKM	-	HDMI_VPH
P103	GND	-	-					
P104	HDMI_HPD / DP1_HPD	In	-	HDMI	i.MX6 QP/Q/DP/D/DL/S	HDMI_HPD	-	HDMI_VPH
P105	HDMI_CTRL_CK / DP1_AUX+	Out	PU-1.5K	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	KEY_COL3	Alt2	NVCC_GPIO
P106	HDMI_CTRL_DAT / DP1_AUX-	Bi-Dir	PU-1.5K	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	KEY_ROW3	Alt2	NVCC_GPIO
P107	DP1_AUX_SEL	-	-					
P108	GPIO0 / CAM0_PWR#	Out	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	EIM_A25	Alt5	NVCC_EIM0
P109	GPIO1 / CAM1_PWR#	Out	PU-470K	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	DISP0_DAT13	Alt5	NVCC_LCD
P110	GPIO2 / CAM0_RST#	Out	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	DISP0_DAT12	Alt5	NVCC_LCD
P111	GPIO3 / CAM1_RST#	Out	PU-470K	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	DISP0_DAT14	Alt5	NVCC_LCD
P112	GPIO4 / HDA_RST#	Bi-Dir	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	DISP0_DAT15	Alt5	NVCC_LCD
P113	GPIO5 / PWM_OUT	Out	PU-470K	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	SD1_DAT1	Alt2	NVCC_SD1
P114	GPIO6 / TACHIN	Bi-Dir	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	SD1_DAT0	Alt5	NVCC_SD1
P115	GPIO7	Bi-Dir	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	DISP0_DAT17	Alt5	NVCC_LCD
P116	GPIO8	Bi-Dir	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	DISP0_DAT18	Alt5	NVCC_LCD
P117	GPIO9	Bi-Dir	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	DISP0_DAT19	Alt5	NVCC_LCD
P118	GPIO10	Bi-Dir	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	DISP0_DAT20	Alt5	NVCC_LCD
P119	GPIO11	Bi-Dir	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	DISP0_DAT21	Alt5	NVCC_LCD
P120	GND	-	-					
P121	I2C_PM_CK	Out	PU-1K	I2C2	i.MX6 QP/Q/DP/D/DL/S	EIM_EB2	Alt6	NVCC_EIM0
P122	I2C_PM_DAT	Bi-Dir	PU-1K	I2C2	i.MX6 QP/Q/DP/D/DL/S	EIM_D16	Alt6	NVCC_EIM0
P123	BOOT_SEL0#	In	PU-4.7K	CMOS/1.8V	BMC	PB3	-	-
P124	BOOT_SEL1#	In	PU-4.7K	CMOS/1.8V	BMC	PB5	-	-
P125	BOOT_SEL2#	In	PU-4.7K	CMOS/1.8V	BMC	PA2	-	-

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P126	RESET_OUT#	Out	-	CMOS/1.8V	BMC	PC4	-	-
P127	RESET_IN#	In	PU-10K	CMOS/1.8V	BMC	PC12	-	-
P128	POWER_BTN#	In	-	CMOS/1.8V	BMC	PA11	-	-
P129	SER0_TX	Out	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	SD3_DAT7	Alt1	NVCC_SD3
P130	SER0_RX	In	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	SD3_DAT6	Alt1	NVCC_SD3
P131	SER0_RTS#	In	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	EIM_D20	Alt4	NVCC_EIM0
P132	SER0_CTS#	Out	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	EIM_D19	Alt4	NVCC_EIM0
P133	GND	-	-					
P134	SER1_TX	Out	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	EIM_D26	Alt4	NVCC_EIM0
P135	SER1_RX	In	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	EIM_D27	Alt4	NVCC_EIM0
P136	SER2_TX	In	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	KEY_COL1	Alt4	NVCC_GPIO
P137	SER2_RX	Out	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	KEY_ROW1	Alt4	NVCC_GPIO
P138	SER2_RTS#	In	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	KEY_COL4	Alt4	NVCC_GPIO
P139	SER2_CTS#	Out	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	KEY_ROW4	Alt4	NVCC_GPIO
P140	SER3_TX	Out	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	KEY_COL0	Alt4	NVCC_GPIO
P141	SER3_RX	In	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	KEY_ROW0	Alt4	NVCC_GPIO
P142	GND	-	-					
P143	CAN0_TX	Out	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	SD3_CMD	Alt2	NVCC_SD3
P144	CAN0_RX	In	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	SD3_CLK	Alt2	NVCC_SD3
P145	CAN1_TX	Out	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	SD3_DAT0	Alt2	NVCC_SD3
P146	CAN1_RX	In	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	SD3_DAT1	Alt2	NVCC_SD3
P147	VDD_IN	PWR						
P148	VDD_IN	PWR						
P149	VDD_IN	PWR						
P150	VDD_IN	PWR						
P151	VDD_IN	PWR						
P152	VDD_IN	PWR						
P153	VDD_IN	PWR						
P154	VDD_IN	PWR						
P155	VDD_IN	PWR						
P156	VDD_IN	PWR						
S1	CSI1_TX+ / I2C_CAM1_CK	In	PU-2.2K	I2C1	i.MX6 QP/Q/DP/D/DL/S	CSI0_DAT9	Alt4	NVCC_CSI

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S2	CSI1_TX- / I2C_CAM1_DAT	In	PU-2.2K	I2C1	i.MX6 QP/Q/DP/D/DL/S	CSI0_DAT8	Alt4	NVCC_CSI
S3	GND	-	-					
S4	RSVD	-	-					
S5	CSI0_TX- / I2C_CAM0_CK	-	-					
S6	CAM_MCK	Out	serial-0R	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	GPIO_0	Alt0	NVCC_GPIO
S7	CSI0_TX+ / I2C_CAM0_DAT	-	-					
S8	CSI0_CK+	-	-					
S9	CSI0_CK-	-	-					
S10	GND	-	-					
S11	CSI0_RX0+	-	-					
S12	CSI0_RX0-	-	-					
S13	GND	-	-					
S14	CSI0_RX1+	-	-					
S15	CSI0_RX1-	-	-					
S16	GND	-	-					
S17	GBE1_MDI0+	Bi-Dir	PU-49.9R	RGMII	LAN9514-JZX	TXP	-	-
S18	GBE1_MDI0-	Bi-Dir	PU-49.9R	RGMII	LAN9514-JZX	TXN	-	-
S19	GBE1_LINK100#	Out	serial-0R	RGMII	LAN9514-JZX	nSPD_LED/GPIO2	-	-
S20	GBE1_MDI1+	Bi-Dir	PU-49.9R	RGMII	LAN9514-JZX	RXP	-	-
S21	GBE1_MDI1-	Bi-Dir	PU-49.9R	RGMII	LAN9514-JZX	RXN	-	-
S22	GBE1_LINK1000#	-	-				-	-
S23	GBE1_MDI2+	-	-					
S24	GBE1_MDI2-	-	-					
S25	GND	-	-					
S26	GBE1_MDI3+	-	-					
S27	GBE1_MDI3-	-	-					
S28	GBE1_CTREF	-	-					
S29	PCIE_D_TX+ / SERDES_1_TX+	-	-					
S30	PCIE_D_TX- / SERDES_1_TX-	-	-					
S31	GBE1_LINK_ACT#	Out	serial-0	RGMII	LAN9514-JZX	nLNKA_LED/GPIO1	-	-
S32	PCIE_D_RX+ / SERDES_1_RX+	-	-				-	-
S33	PCIE_D_RX- / SERDES_1_RX-	-	-				-	-
S34	GND	-	-					

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S35	USB4+	Bi-Dir	-	USB	LAN9514-JZX	USBDP5	-	-
S36	USB4-	Bi-Dir	-	USB	LAN9514-JZX	USBDM5	-	-
S37	USB3_VBUS_DET	-	-				-	-
S38	AUDIO_MCK	Out	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	GPIO_3	Alt4	NVCC_GPIO
S39	I2S0_LRCK	Bi-Dir	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	CSI0_DAT6	Alt4	NVCC_CSI
S40	I2S0_SDOUT	Out	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	CSI0_DAT5	Alt4	NVCC_CSI
S41	I2S0_SDIN	In	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	CSI0_DAT7	Alt4	NVCC_CSI
S42	I2S0_CK	Bi-Dir	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	CSI0_DAT4	Alt4	NVCC_CSI
S43	ESPI_ALERT0#	-	-					
S44	ESPI_ALERT1#	-	-					
S45	MDIO_CLK	-	-					
S46	MDIO_DAT	-	-					
S47	GND	-	-					
S48	I2C_GP_CK	Out	PU-2.2K	I2C3	i.MX6 QP/Q/DP/D/DL/S	EIM_D17	Alt6	NVCC_EIM0
S49	I2C_GP_DAT	Bi-Dir	PU-2.2K	I2C3	i.MX6 QP/Q/DP/D/DL/S	EIM_D16	Alt6	NVCC_EIM0
S50	HDA_SYNC / I2S2_LRCK	-	-					
S51	HDA_SDO / I2S2_SDOUT	-	-					
S52	HDA_SDI / I2S2_SDIN	-	-					
S53	HDA_CK / I2S2_CK	-	-					
S54	SATA_ACT#	Out	-	CMOS/3.3V	i.MX6 QP/Q/DP/D/DL/S	DISP0_DAT23	Alt5	NVCC_LCD
S55	USB5_EN_OC#	-	-					
S56	ESPI_IO_2	-	-					
S57	ESPI_IO_3	-	-					
S58	ESPI_RESET#	Out	-	CMOS/1.8V	BMC	PC4	-	-
S59	USB5+	-	-					
S60	USB5-	-	-					
S61	GND	-	-					
S62	USB3_SSTX+	-	-					
S63	USB3_SSTX-	-	-					
S64	GND	-	-					
S65	USB3_SSRX+	-	-					
S66	USB3_SSRX-	-	-					

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S67	GND	-	-					
S68	USB3+	Bi-Dir	-	USB	LAN9514-JZX	USBDP4	-	-
S69	USB3-	Bi-Dir	-	USB	LAN9514-JZX	USBDM4	-	-
S70	GND	-	-					
S71	USB2_SSTX+	-	-					
S72	USB2_SSTX-	-	-					
S73	GND	-	-					
S74	USB2_SSRX+	-	-					
S75	USB2_SSRX-	-	-					
S76	PCIE_B_RST#	-	-					
S77	PCIE_C_RST#	-	-					
S78	PCIE_C_RX+ / SERDES_2_RX+	-	-					
S79	PCIE_C_RX- / SERDES_2_RX-	-	-					
S80	GND	-	-					
S81	PCIE_C_TX+ / SERDES_2_TX+	-	-					
S82	PCIE_C_TX- / SERDES_2_TX-	-	-					
S83	GND	-	-					
S84	PCIE_B_REFCK+	-	-					
S85	PCIE_B_REFCK-	-	-					
S86	GND	-	-					
S87	PCIE_B_RX+	-	-					
S88	PCIE_B_RX-	-	-					
S89	GND	-	-					
S90	PCIE_B_TX+	-	-					
S91	PCIE_B_TX-	-	-					
S92	GND	-	-					
S93	DP0_LANE0+	-	-					
S94	DP0_LANE0-	-	-					
S95	DP0_AUX_SEL	-	-					
S96	DP0_LANE1+	-	-					
S97	DP0_LANE1-	-	-					
S98	DP0_HPD	-	-					
S99	DP0_LANE2+	-	-					

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S100	DP0_LANE2-	-	-					
S101	GND	-	-					
S102	DP0_LANE3+	-	-					
S103	DP0_LANE3-	-	-					
S104	USB3_OTG_ID	-	-					
S105	DP0_AUX+	-	-					
S106	DP0_AUX-	-	-					
S107	LCD1_BKLT_EN	-	-					
S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	Out	-	LVDS	i.MX6 QP/Q/DP/D/DL/S	LVDS1_CLK_P	-	NVCC_LVDS_2P5
S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	Out	-	LVDS	i.MX6 QP/Q/DP/D/DL/S	LVDS1_CLK_N	-	NVCC_LVDS_2P5
S110	GND	-	-					
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	Out	-	LVDS	i.MX6 QP/Q/DP/D/DL/S	LVDS1_TX0_P	-	NVCC_LVDS_2P5
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	Out	-	LVDS	i.MX6 QP/Q/DP/D/DL/S	LVDS1_TX0_N	-	NVCC_LVDS_2P5
S113	eDP1_HPD / DSI1_TE	-	-					
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	Out	-	LVDS	i.MX6 QP/Q/DP/D/DL/S	LVDS1_TX1_P	-	NVCC_LVDS_2P5
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	Out	-	LVDS	i.MX6 QP/Q/DP/D/DL/S	LVDS1_TX1_N	-	NVCC_LVDS_2P5
S116	LCD1_VDD_EN	-	-					
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	Out	-	LVDS	i.MX6 QP/Q/DP/D/DL/S	LVDS1_TX2_P	-	NVCC_LVDS_2P5
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	Out	-	LVDS	i.MX6 QP/Q/DP/D/DL/S	LVDS1_TX2_N	-	NVCC_LVDS_2P5
S119	GND	-	-					
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	Out	-	LVDS	i.MX6 QP/Q/DP/D/DL/S	LVDS1_TX3_P	-	NVCC_LVDS_2P5
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	Out	-	LVDS	i.MX6 QP/Q/DP/D/DL/S	LVDS1_TX3_N	-	NVCC_LVDS_2P5
S122	LCD1_BKLT_PWM	-	-					
S123	GPIO13	-	-					
S124	GND	-	-					

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S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	Out	serial-0R	LVDS	i.MX6 QP/Q/DP/D/DL/S	LVDS0_TX0_P	-	NVCC_LVDS_2P5
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	Out	serial-0R	LVDS	i.MX6 QP/Q/DP/D/DL/S	LVDS0_TX0_N	-	NVCC_LVDS_2P5
S127	LCD0_BKLT_EN	Out	serial-0R	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	EIM_D31	Alt5	NVCC_EIM0
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	Out	serial-0R	LVDS	i.MX6 QP/Q/DP/D/DL/S	LVDS0_TX1_P	-	NVCC_LVDS_2P5
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	Out	serial-0R	LVDS	i.MX6 QP/Q/DP/D/DL/S	LVDS0_TX1_N	-	NVCC_LVDS_2P5
S130	GND	-	-					
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	Out	-	LVDS	i.MX6 QP/Q/DP/D/DL/S	LVDS0_TX2_P	-	NVCC_LVDS_2P5
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	Out	-	LVDS	i.MX6 QP/Q/DP/D/DL/S	LVDS0_TX2_N	-	NVCC_LVDS_2P5
S133	LCD0_VDD_EN	Out	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	ENET_TXD0	Alt5	NVCC_ENET
S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	Out	serial-0R	LVDS	i.MX6 QP/Q/DP/D/DL/S	LVDS0_CLK_P	-	NVCC_LVDS_2P5
S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	Out	serial-0R	LVDS	i.MX6 QP/Q/DP/D/DL/S	LVDS0_CLK_N	-	NVCC_LVDS_2P5
S136	GND	-	-					
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	Out	-	LVDS	i.MX6 QP/Q/DP/D/DL/S	LVDS0_TX3_P	-	NVCC_LVDS_2P5
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	Out	-	LVDS	i.MX6 QP/Q/DP/D/DL/S	LVDS0_TX3_N	-	NVCC_LVDS_2P5
S139	I2C_LCD_CK	Out	PU-1K	I2C2	i.MX6 QP/Q/DP/D/DL/S	EIM_EB2	Alt6	NVCC_EIM0
S140	I2C_LCD_DAT	Bi-Dir	PU-1K	I2C2	i.MX6 QP/Q/DP/D/DL/S	EIM_D16	Alt6	NVCC_EIM0
S141	LCD0_BKLT_PWM	Out	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	GPIO_9	Alt4	NVCC_GPIO
S142	GPIO12	In	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	DISP0_DAT11	Alt5	NVCC_LCD
S143	GND	-	-					
S144	eDP0_HPD / DSI0_TE	-	-					
S145	WDT_TIME_OUT#	Out	PD-100K	CMOS/1.8V	BMC	PC7	-	-
S146	PCIE_WAKE#	In	-	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	CSI0_DATA_EN	Alt5	NVCC_CSI
S147	VDD_RTC	PWR					-	-
S148	LID#	In	PU-4.7K	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	GPIO_7	Alt5	NVCC_GPIO
S149	SLEEP#	In	PU-4.7K	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	NANDF_D7	Alt5	NVCC_NANDF
S150	VIN_PWR_BAD#	In	PU-10K	CMOS/1.8V	BMC	PB7	-	-

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S151	CHARGING#	Out	PU-68K	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	EIM_D23	Alt5	NVCC_EIM0
S152	CHARGER_PRSNT#	Out	PU-100K	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	NANDF_D6	Alt5	NVCC_NANDF
S153	CARRIER_STBY#	Out	-	CMOS/1.8V	BMC	PB1	-	-
S154	CARRIER_PWR_ON_B (BMC)	Out	-	CMOS/1.8V	BMC	PB6	-	-
S155	FORCE_RECOV_B	In	PU-4.7K	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	BOOT_MODE0/1	Alt0	VDD_SNVS_IN
S156	BATLOW_B	Out	PU-68K	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	NANDF_RB0	Alt5	NVCC_NANDF
S157	TEST_B	In	PU-4.7K	CMOS/1.8V	i.MX6 QP/Q/DP/D/DL/S	GPIO_8	Alt5	NVCC_GPIO
S158	GND	-	-					

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5. Software Support

5.1.1 Uboot / Yocto

Goto : https://github.com/adlink

Yocto source-code and compiling instructions are available

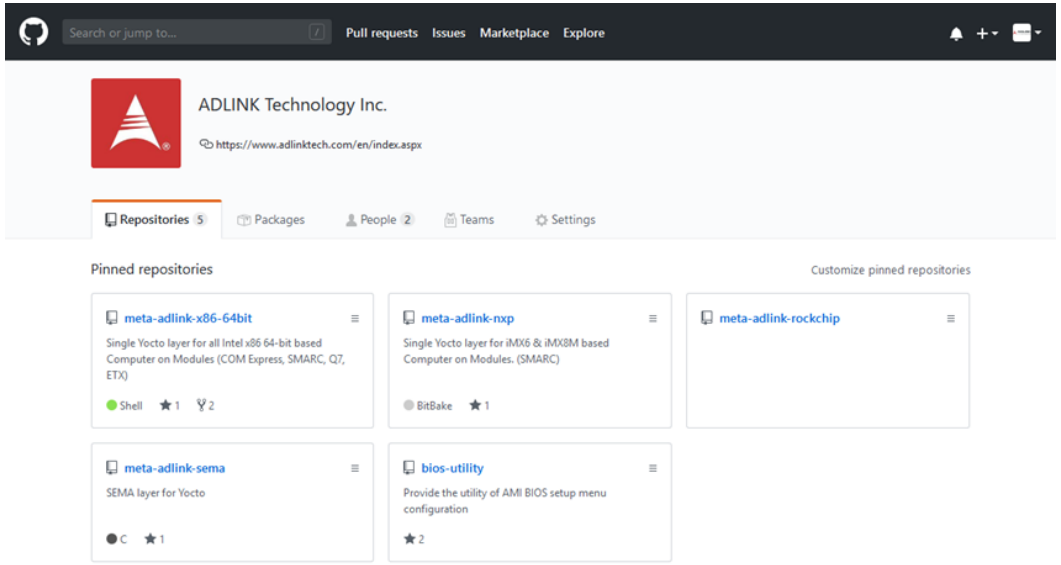
5.1.2 Ubuntu

Build instruction from source, are available on Github

5.1.3 Android

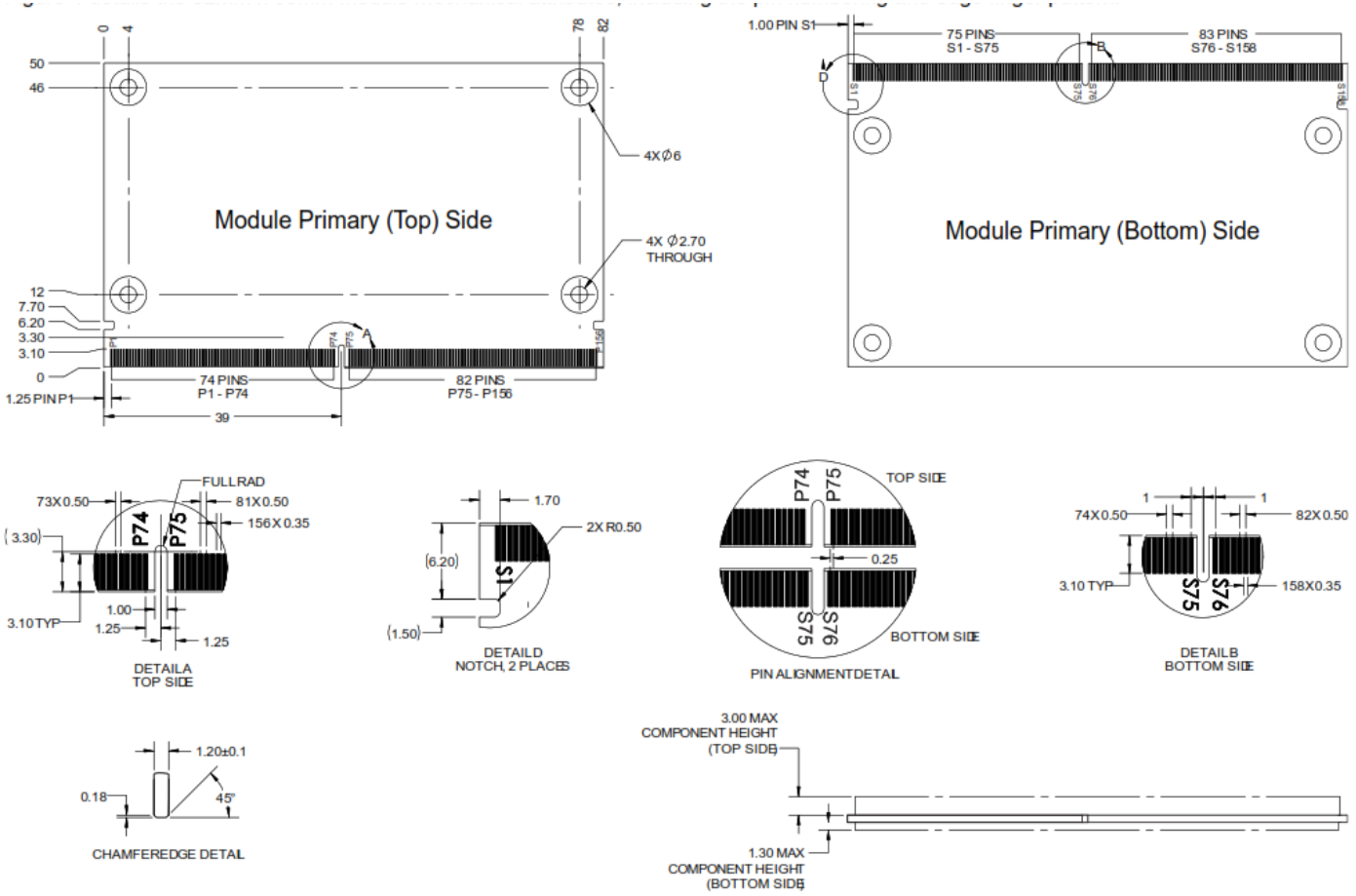
Goto : https://github.com/adlink

Android source-code and compiling instructions are available



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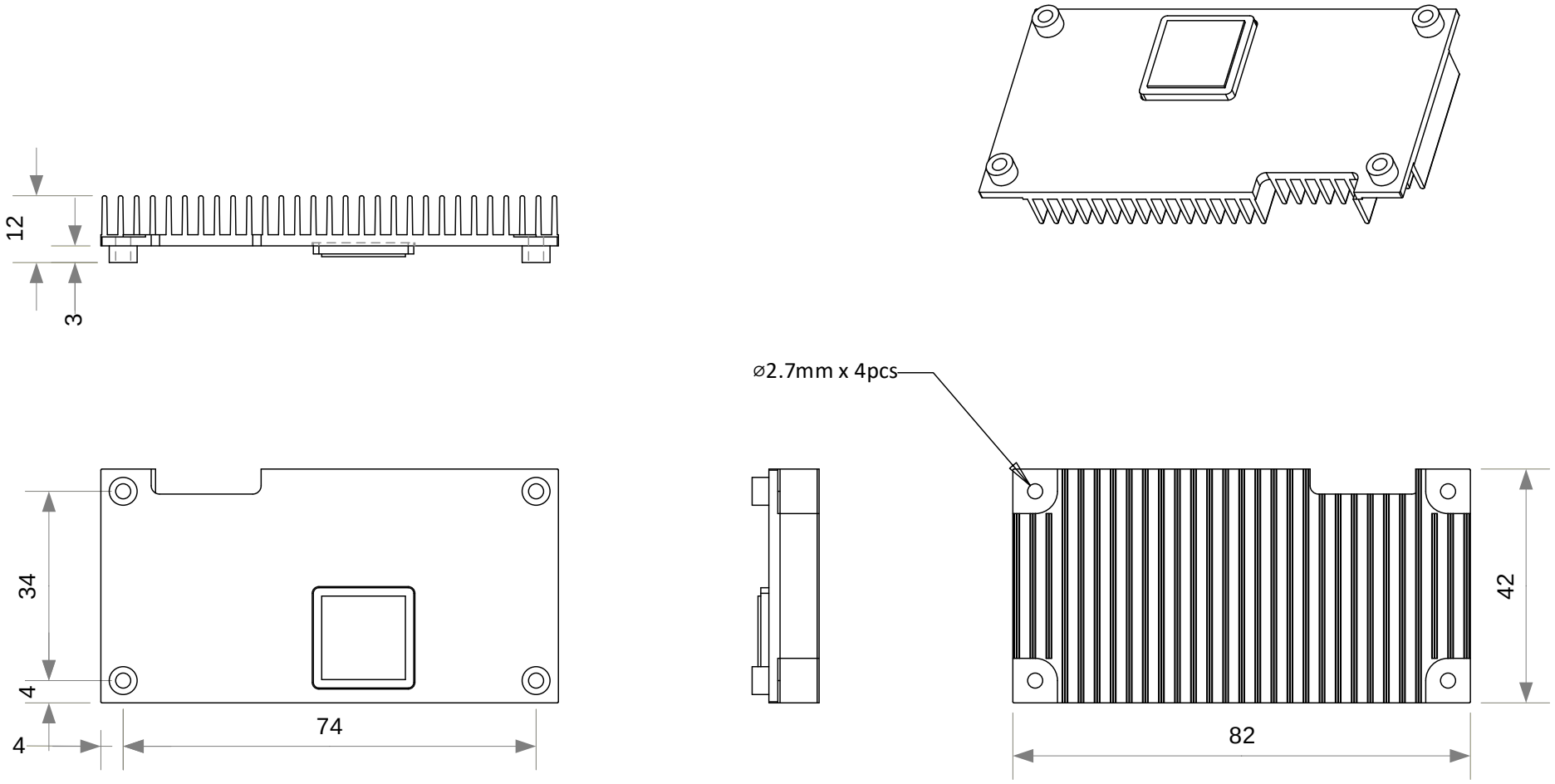
6. Mechanical



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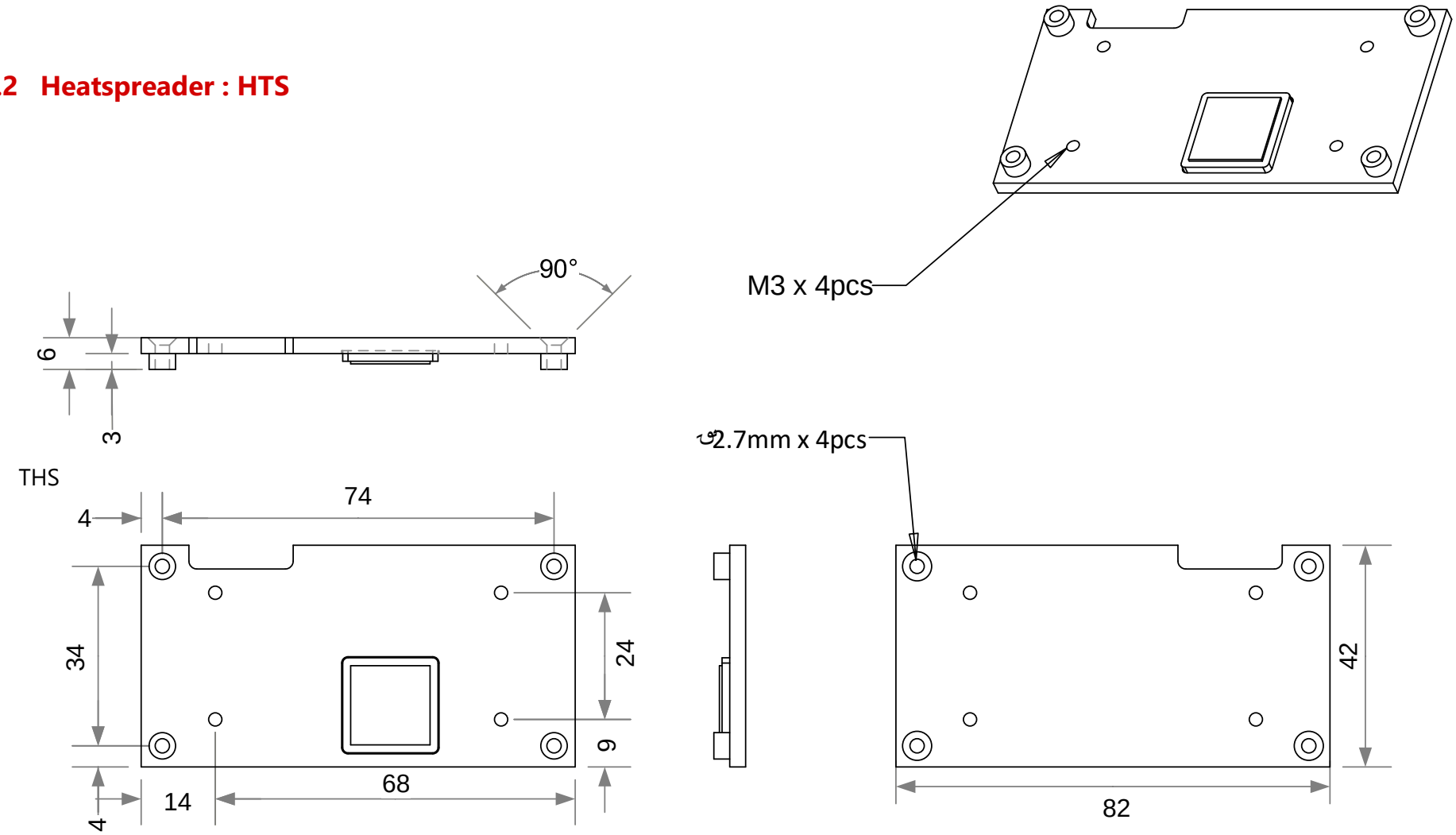
7. Thermal Solutions

7.1.1 Heatsink : THS



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7.1.2 Heatspreader : HTS



HTS-sIMX6R2-SDL	Heatspreader for LEC-iMXR2 solo/Duallite	THS-sIMX6R2-SDL	Low profile heatsink for LEC-iMX6R2 Solo/DualLite
HTS-sIMX6R2-DQP	Heatspreader for LEC-iMX8R2 Dual/Quad	THS-sIMX6R2-DQP	Low profile heatsink for LEC-iMX6R2 with Dual/Quad

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