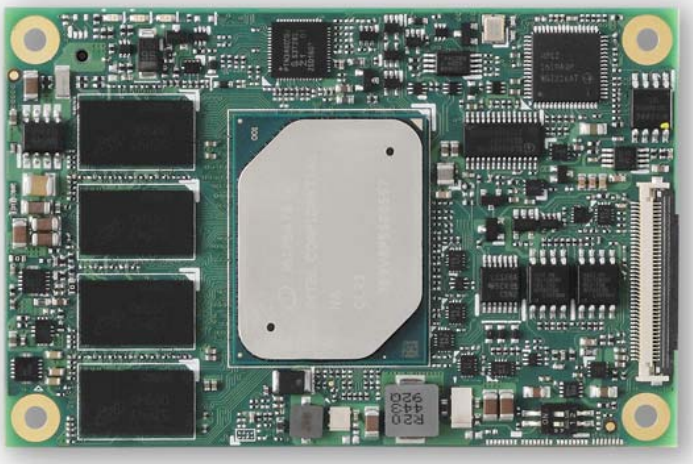
nanoX-AL

User's Manual

COM Express Mini Size Type 10 Module with
Intel Atom®, Pentium®, Celeron® SoC



COM Express®

Manual Rev.:	1.3
Revision Date:	July 16, 2020
Part Number:	50-1J088-1030

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Preface

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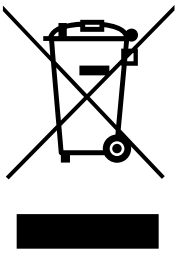
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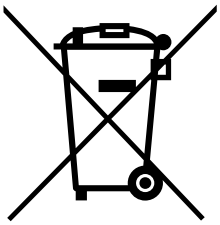
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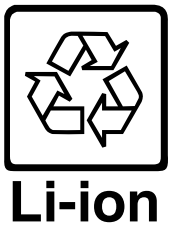
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Revision History

Revision	Description	Date	By
1.0	Initial release	2018-04-02	JC
1.1	Correct LVDS specification	2019-11-18	JC
1.2	Update dual BIOS to “build option”; update Ethernet controller temperature support	2019-12-06	JC
1.3	Correct GBE0_MDI0- pin number	2020-07-16	JC

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1. Introduction

The nanoX-AL is a COM Express® COM.0 R3.0 Type 10 module supporting Intel Atom® processor E3900 series system-on-chip (SoC). The nanoX-AL is specifically designed for customers who need optmized processing and graphics performance with low power consumption in a long product life solution.

The nanoX-AL features the dual/quad core Intel Atom® processor E3900 series supporting non-ECC type DDR3L single-channel or dual-channel memory at 1600/1867 MHz to provide excellent overall performance. Integrated Intel® Gen9 LP Graphics includes features such as OpenGL 4.3, DirectX 12, OpenCL 2.0 and support for H.265/HEVC, H.264, MPEG2, VC1, VP9, MVC, JPEG/MJPEG hardware decode. Graphics outputs include DDI ports supporting HDMI/DVI/DisplayPort and single-channel 18/24-bit LVDS (eDP by build option). The nanoX-AL is specifically designed for customers with balanced performance and power consumption requirements who want to outsource the custom core logic of their systems for reduced development time.

The nanoX-AL has 2GB of soldered type non-ECC DDR3L memory (4GB and 8GB optional). In addition, onboard eMMC memory (8GB/16GB/32GB) and SD signals are available as build options.

The nanoX-AL features a single onboard Gigabit Ethernet port, multiple PCIe lanes, USB 3.0 ports and USB 2.0 ports, and SATA 6 Gb/s ports. Support is provided for SMBus and I^2C. The module is equipped with SPI AMI EFI BIOS (dual BIOS by build option), supporting embedded features such as remote console, CMOS backup, hardware monitor, and watchdog timer.

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2. Specifications

2.1. Core System

CPU	**Dual or quad-core Intel Atom® processor E3900 SoC** • Intel Atom® E3950 1.6/2.0GHz (Burst), 400-650MHz (Graphics) 12W (4C/1866) • Intel Atom® E3940 1.6/1.8GHz (Burst), 400-600MHz (Graphics) 9W (4C/1866) • Intel Atom® E3930 1.3/1.8GHz (Burst), 400-550MHz (Graphics) 6W (2C/1866) • Pentium® N4200 1.1/2.5GHz (Turbo), 200-750MHz (graphics), 6W (4C/1866) • Celeron® N3350 1.1/2.4GHz (Turbo), 200-650MHz (graphics), 6W (2C/1866) Supports dual or quad Out-of-Order Execution (OOE) processor cores, Intel® VT-x, Intel® VT-d, Intel® SSE4.1 and SSE4.2, Intel® 64 architecture, Intel® Turbo Boost Technology 2.0, Intel AES-NI, Intel® TXT, PCLMULQDQ instruction DRNG **Notes:** Availability of features may vary between processor SKUs and operating systems; N4200/M3350 by project basis.
L3 Cache	2MB for all SKUs
Memory	Single channel or dual channel non-ECC 1600/1866 MHz soldered DDR3L memory up to 8GB (4GB and 8GB supported by build option) **Notes:** 2GB and 4GB are 1866MHz and 8GB is 1600MHz (or 1866MHz, by project basis). Availability of features may vary between processor SKUs. 2GB is single channel and 4GB/8GB are dual channel.
BIOS	AMI EFI with CMOS backup in 16MB SPI BIOS

2.2. Expansion Busses

PCI Express	Multiple PCI Express x1 Gen2 (AB): Lanes 0/1/2/4, configurable to 3 x1 (default); 2 x1+1 x2 or 1 x4 (by request) Recommend up to three devices only.
Other	• LPC bus • SMBus (system) • I^2C (user)

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2.3. Video

Integrated on SoC	Intel® Generation 9 Low Power Graphics core architecture with up to 18 execution units supporting two independent displays
GPU Feature Support	• 3D graphics hardware acceleration • Support for DirectX12/11.3/10/9.3, OCL 2.0, OGL ES 3.0, OGL 4.3 • Video decode hardware acceleration including support for H.265 (HEVC), H.264, MVC, MPEG-2, VC-1, WMV9, VP8/VP9, JPEG/MJPEG formats • Video encode hardware acceleration including support for H.265 (HEVC), H.264, VP8/VP9, JPEG/MJPEG formats • Supports content protection using PAVP 2.0 and HDCP 1.4/2.0 **Note:** Availability of features may vary between operating systems.
Display Types	• **Single channel 18/24-bit LVDS:** supports DE mode and H/V-Sync mode display, resolution up to 1920x1200 with single channel LVDS. • **eDP x4 lanes** (eDP 1.3, by build option in place of LVDS) • **DDI0:** Supports DisplayPort, HDMI, DVI

2.4. Audio

Integrated	Intel® HD Audio integrated on SoC
Codec	Located on carrier miniBASE-10R (ALC262 standard support)

2.5. LAN

Intel MAC/PHY	Intel® Ethernet Controller I210 (Extreme Rugged operating temperature range) Intel® Ethernet Controller I211 (standard operating temperature range) Supports GbE0_SDP, IEEE 1588 for real-time applications
Interface	10/100/1000 Mbit/s connection

2.6. Multi I/O and Storage

I/O Hub	Integrated on SoC
USB	2x USB. 3.0/2.0/1.1 (USB 0/1) 6x USB. 2.0/1.1 (USB 2/3/4/5/6/7) **Note:** USB port 7 supports USB 2.0 OTG on Yocto Linux OS, detection pin is B96. Does not comply with PICMG R3.0 USB OTG support order (port 0, then port 7) due to design prior to finalization of specification.
SATA	2x ports SATA 6Gb/s (SATA0, SATA1)
eMMC 5.0 (build option)	8/16/32 GB (boot device support may vary between operating systems)*
SD (build option)	SD 3.0 signal is muxed with GPIO, switching through BOM option (boot device support may vary between operating systems) **Note:** Supports 3.30V SD cards only.
GPIO	4 GPO and 4 GPI **Note:** GPI with interruput supported on Linux.

***Note:** See table below for detailed boot device support information.

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Boot Device Support

		Windows 10 Enterprise	Linux (Yocto)
Storage only	**eMMC 5.0**	Yes	Yes
	SD	Yes	Yes
OS Installation	**eMMC 5.0**	Yes	Yes
	SD	No	No

Note: eMMC and SD functionality as an OS installation device may change dependent on Intel updates. Please contact your local sales representative for more information.

2.7. Serial I/O on Module

- **Ports:** 2x UART ports COM 1/2, baud rate up to 115.2k bps
- **Console Redirection:** selectable in BIOS, supported during BIOS POST

COM Port	Description	IRQ	Address	Console Redirection Support
COM 1	Supported by module (SER0, A98/A99), via NCT5104D	10	0x240	Yes
COM 2	Supported by module (SER1, A101/A102), via NCT5104D	11	0x248	Yes
COM 3	Supported by Super I/O (W83627DHG) on carrier board	4	0x3F8	Yes
COM 4	Supported by Super I/O (W83627DHG) on carrier board	3	0x2F8	Yes

2.8. Trusted Platform Module (TPM)

- **Chipset:** Infineon
- **Type:** TPM 2.0

Note: TPM supported by build option.

2.9. SEMA Board Controller

- **Type:** ADLINK Smart Embedded Management Agent (SEMA)
- **Functions:**
  - Voltage/Current monitoring
  - Power sequence debug support
  - AT/ATX mode control
  - Logistics and forensic information
  - Flat panel control
  - General purpose I2C
  - Failsafe BIOS (dual BIOS by build option)
  - Watchdog timer and fan control

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2.10. Debug

- 40-pin flat cable connector to be used with DB-40 debug module
  Supports: BIOS POST code LED, BMC access, SPI BIOS flashing, power testpoints, debug LEDs
- MIPI60 60-pin header for debug of SoC (build option)

2.11. Power Specifications

Power Modes	AT and ATX mode (AT mode startup controlled by SEMA Board Controller)
Standard Voltage Input	ATX: 12V ±5% / 5Vsb ±5% or AT = 12V ±5%
Wide Voltage Input	ATX: 4.75-20V, 5Vsb ±5%; AT: 4.75-20V
Power Management	ACPI 5.0 compliant, Smart Battery support
Power States	Supports C0, C1, C1E, C6L, C6, S0, S3, S4, S5, S5 ECO mode (Wake-on-USB S3/S4, WoL S3/S4/S5)
ECO Mode	Supports deep S5 for 5Vsb power saving

2.12. Power Consumption

Please contact your ADLINK representative for the document “COM Express Module Power Consumption”.

2.13. Operating Temperatures

Standard Operating Temperature	0°C to +60°C (wide voltage input) Storage: -20°C to +70°C
Extreme Rugged Operating Temperature (optional)	-40°C to +85°C (standard voltage input only, build option, Intel Atom® SKUs only) Storage: -40°C to +85°C

2.14. Environmental

Humidity	Operating: 5-90% RH, non-condensing Storage: 5-95% RH (and operating with conformal coating)
Shock and Vibration	IEC 60068-2-64 and IEC-60068-2-27 MIL-STD-202F, Method 213B, Table 213-I, Condition A and Method 214A, Table 214-I, Condition D
HALT	Thermal Stress, Vibration Stress, Thermal Shock and Combined Test

2.15. Specification Compliance

- PICMG COM.0: Rev 3.0 Type 10, Mini size 84 x 55 mm

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2.16. Operating Systems

Standard Support	• Windows 10 (64-bit) • Linux (64-bit) • VxWorks (64-bit)
Extended Support (BSP)	• Linux (64-bit) • VxWorks (64-bit)

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2.17. Functional Diagram

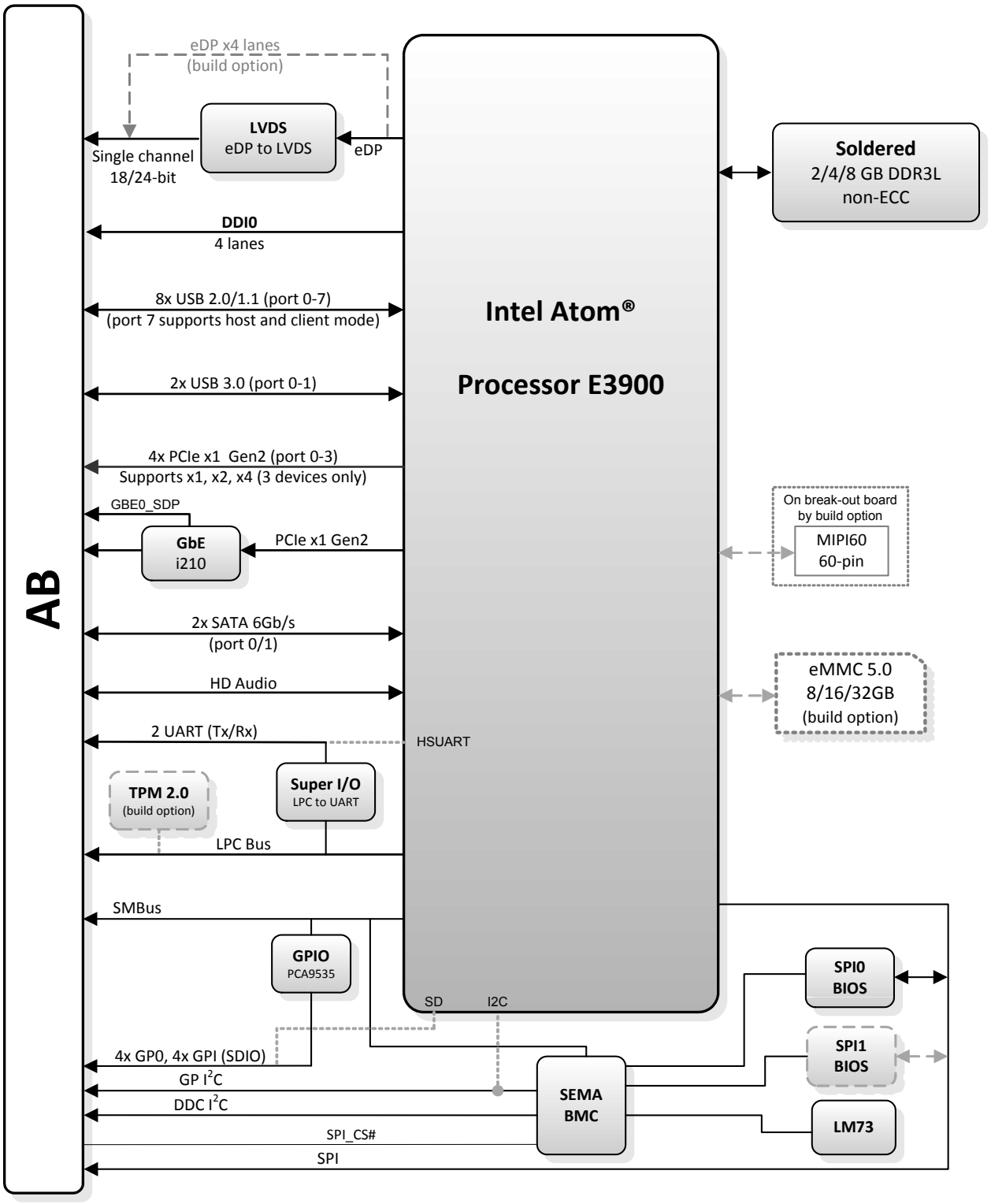
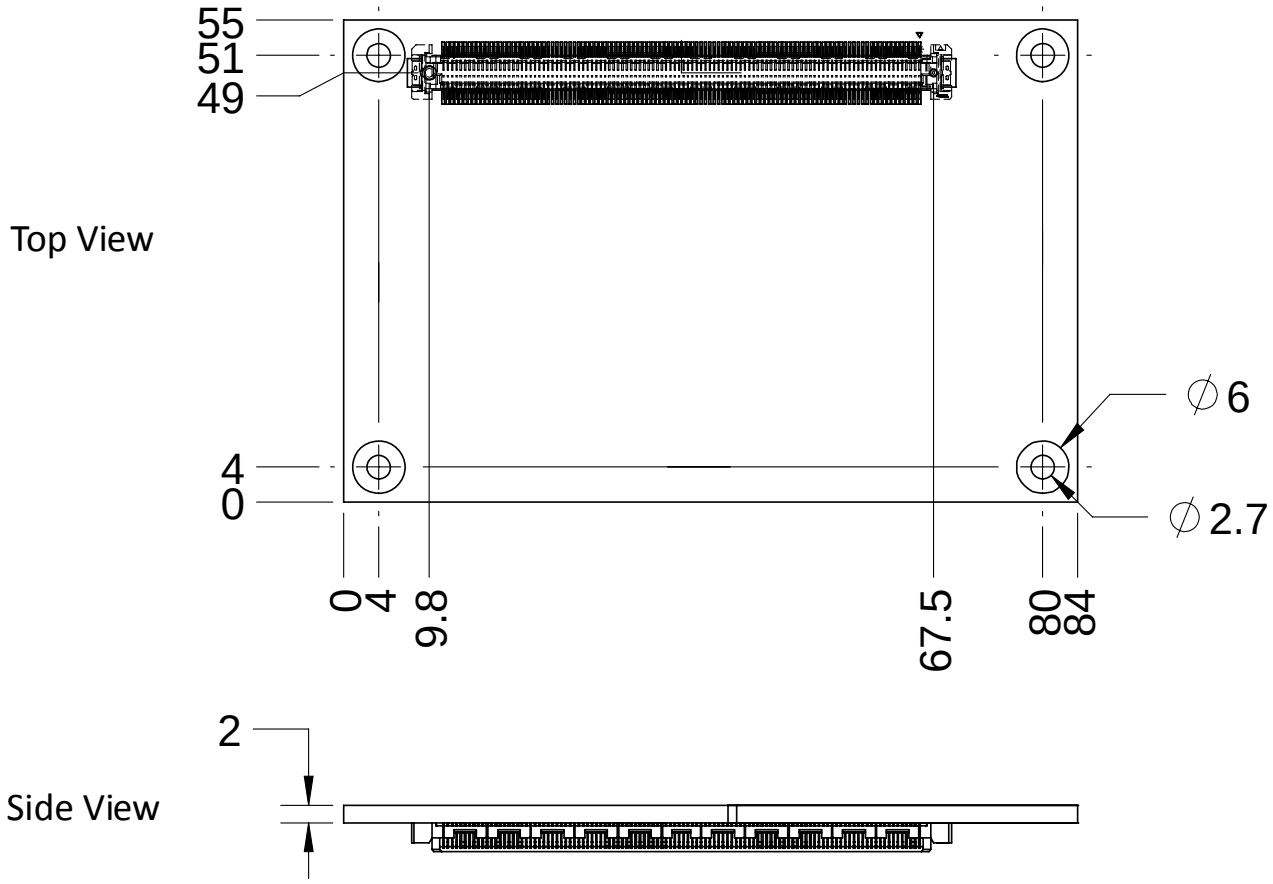


Figure 1: nanoX-AL Functional Block Diagram

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2.18. Mechanical Drawing



All are dimensions shown in millimeters.

Tolerances should be ± 0.25mm, unless otherwise noted. The tolerances of the module connector locating peg holes (dimensions [9.8, 49]) should be ±0.10mm.

Figure 2: nanoX-AL Mechanical Drawing

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3. Pinouts and Signal Descriptions

3.1. AB/CD Pin Definitions

The nanoX-AL is a Type 10 module supporting USB 3.0 and DDI channel on the AB connector. All standard pins of the COM Express specification are described in the table below, including those not supported on the nanoX-AL.

Note: Signals not supported on the nanoX-AL module are ~~crossed out~~.

Table 1: nanoX-AL Type 10 COM.0 Rev. 3.0 Pin Definitions

	Row A		Row B
Pin	**Name**	**Pin**	**Name**
1	GND(FIXED)	1	GND(FIXED)
2	GBE0_MDI3-	2	GBE0_ACT#
3	GBE0_MDI3+	3	LPC_FRAME# ~~/ ESPI_CS0#~~
4	GBE0_LINK100#	4	LPC_AD0 ~~/ ESPI_IO_0~~
5	GBE0_LINK1000#	5	LPC_AD1 ~~/ ESPI_IO_1~~
6	GBE0_MDI2-	6	LPC_AD2 ~~/ ESPI_IO_2~~
7	GBE0_MDI2+	7	LPC_AD3 ~~/ ESPI_IO_3~~
8	GBE0_LINK#	8	LPC_DRQ0# ~~/ ESPI_ALERT0#~~
9	GBE0_MDI1-	9	LPC_DRQ1# ~~/ ESPI_ALERT_1#~~
10	GBE0_MDI1+	10	LPC_CLK ~~/ ESPI_CK~~
11	GND(FIXED)	11	GND(FIXED)
12	GBE0_MDI0-	12	PWRBTN#
13	GBE0_MDI0+	13	SMB_CK
14	GBE0_CTREF	14	SMB_DAT
15	SUS_S3#	15	SMB_ALERT#
16	SATA0_TX+	16	SATA1_TX+
17	SATA0_TX-	17	SATA1_TX-
18	SUS_S4#	18	SUS_STAT# ~~/ ESPI_RESET#~~
19	SATA0_RX+	19	SATA1_RX+
20	SATA0_RX-	20	SATA1_RX-
21	GND(FIXED)	21	GND(FIXED)
22	USB_SSRX0-	22	USB_SSTX0-
23	USB_SSRX0+	23	USB_SSTX0+
24	SUS_S5#	24	PWR_OK
25	USB_SSRX1-	25	USB_SSTX1-
26	USB_SSRX1+	26	USB_SSTX1+
27	BATLOW#	27	WDT
28	(S)ATA_ACT#	28	~~HDA_SDIN2~~
29	HDA_SYNC	29	~~HDA_SDIN1~~
30	HDA_RST#	30	HDA_SDIN0
31	GND(FIXED)	31	GND(FIXED)
32	HDA_BITCLK	32	SPKR
33	HDA_SDOUT	33	I2C_CK
34	BIOS_DIS0# ~~/ ESPI_SAFS~~	34	I2C_DAT
35	THRMTRIP#	35	THRM#

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Row A		Row B	
Pin	Name	Pin	Name
36	USB6-	36	USB7-
37	USB6+	37	USB7+
38	USB_6_7_OC#	38	USB_4_5_OC#
39	USB4-	39	USB5-
40	USB4+	40	USB5+
41	GND(FIXED)	41	GND(FIXED)
42	USB2-	42	USB3-
43	USB2+	43	USB3+
44	USB_2_3_OC#	44	USB_0_1_OC#
45	USB0-	45	USB1-
46	USB0+	46	USB1+
47	VCC_RTC	47	~~ESPI_EN~~
48	RSVD	48	~~USB0_HOST_PRSNT~~
49	GBE0_SDP	49	SYS_RESET#
50	LPC_SERIRQ ~~/ ESPI_CS1#~~	50	CB_RESET#
51	GND(FIXED)	51	GND(FIXED)
52	RSVD	52	RSVD
53	RSVD	53	RSVD
54	GPI0	54	GPO1
55	RSVD	55	RSVD
56	RSVD	56	RSVD
57	GND	57	GPO2
58	PCIE_TX3+	58	PCIE_RX3+
59	PCIE_TX3-	59	PCIE_RX3-
60	GND(FIXED)	60	GND(FIXED)
61	PCIE_TX2+	61	PCIE_RX2+
62	PCIE_TX2-	62	PCIE_RX2-
63	GPI1	63	GPO3
64	PCIE_TX1+	64	PCIE_RX1+
65	PCIE_TX1-	65	PCIE_RX1-
66	GND	66	WAKE0#
67	GPI2	67	WAKE1#
68	PCIE_TX0+	68	PCIE_RX0+
69	PCIE_TX0-	69	PCIE_RX0-
70	GND(FIXED)	70	GND(FIXED)
71	LVDS_A0+ / eDP_TX2+	71	DDI0_PAIR0+
72	LVDS_A0- / eDP_TX2-	72	DDI0_PAIR0-
73	LVDS_A1+ / eDP_TX1+	73	DDI0_PAIR1+
74	LVDS_A1- / eDP_TX1-	74	DDI0_PAIR1-
75	LVDS_A2+ / eDP_TX0+	75	DDI0_PAIR2+
76	LVDS_A2- / eDP_TX0-	76	DDI0_PAIR2-
77	LVDS_/eDP_VDD_EN	77	~~DDI0_PAIR4+~~
78	LVDS_A3+	78	~~DDI0_PAIR4-~~
79	LVDS_A3-	79	LVDS_/eDP_BKLT_EN
80	GND(FIXED)	80	GND(FIXED)

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Row A		Row B	
Pin	**Name**	**Pin**	**Name**
81	LVDS_A_CK+ / eDP_TX3+	81	DDI0_PAIR3+
82	LVDS_A_CK- / eDP_TX3-	82	DDI0_PAIR3-
83	LVDS_I2C_CK / eDP_AUX+	83	LVDS_BKLT_CTRL / eDP_BKLT_CTRL
84	LVDS_I2C_DAT / eDP_AUX-	84	VCC_5V_SBY
85	GPI3	85	VCC_5V_SBY
86	RSVD	86	VCC_5V_SBY
87	eDP_HPD	87	VCC_5V_SBY
88	PCIE_CLK_REF+	88	BIOS_DIS1#
89	PCIE_CLK_REF-	89	DDI0_HPD
90	GND(FIXED)	90	GND(FIXED)
91	SPI_POWER	91	~~DDI0_PAIR5+~~
92	SPI_MISO	92	~~DDI0_PAIR5-~~
93	GPO0	93	~~DDI0_PAIR6+~~
94	SPI_CLK	94	~~DDI0_PAIR6-~~
95	SPI_MOSI	95	DDI0_DDC_AUX_SEL
96	TPM_PP	96	USB7_HOST_PRSNT
97	TYPE10#	97	SPI_CS#
98	SER0_TX	98	DDI0_CTRLCLK_AUX+
99	SER0_RX	99	DDI0_CTRLDATA_AUX-
100	GND(FIXED)	100	GND(FIXED)
101	SER1_TX	101	FAN_PWMOUT
102	SER1_RX	102	FAN_TACHIN
103	LID#	103	SLEEP#
104	VCC_12V	104	VCC_12V
105	VCC_12V	105	VCC_12V
106	VCC_12V	106	VCC_12V
107	VCC_12V	107	VCC_12V
108	VCC_12V	108	VCC_12V
109	VCC_12V	109	VCC_12V
110	GND(FIXED)	110	GND(FIXED)

Notes:

- LID# and SLEEP# signals are not natively supported on the SOC, they instead connect to GPIO pins simulating their behaviour.
- eDP x4 lanes supported by build option.
- SD signals are muxed with GPIO (supported by build option).
- No EXCD0_PERST#, EXCD0_CPPE#, EXCD1_PERST#, EXCD1_CPPE# support.

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3.2. Signal Description Terminology

The following terms are used in the COM Express AB/CD Signal Descriptions below.

I	Input to the Module
O	Output from the Module
I/O	Bi-directional input/output signal
OD	Open drain output
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I/O 3.3Vsb	Input 3.3V tolerant active in standby state
P	Power Input/Output
REF	Reference voltage output that may be sourced from a module power plane.
PDS	Pull-down strap. This is an output pin on the module that is either tied to GND or not connected. The signal is used to indicate the PICMG module type to the Carrier Board.
PU	ADLINK implemented pull-up resistor on module
PD	ADLINK implemented pull-down resistor on module

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3.3. AB Signal Descriptions

3.3.1. Audio Signals

Signal	Pin	Description	I/O	PU/PD	Comment
HDA_RST#	A30	Reset output to CODEC, active low.	O 3.3VSB	PU 10k 3.3VSB	
HDA_SYNC	A29	Sample-synchronization signal to the CODEC(s).	O 3.3V		
HDA_BITCLK	A32	Serial data clock generated by the external CODEC(s).	I/O 3.3V		
HDA_SDOUT	A33	Serial TDM data output to the CODEC.	O 3.3V		
HDA_SDIN[2:0]	B28- B30	Serial TDM data inputs from up to 3 CODECs.	I/O 3.3V		AC_SDIN0: supported AC_SDIN1: not supported AC_SDIN2: not supported

3.3.2. LVDS/eDP

Signal	Pin	Description	I/O	PU/PD	Comment
LVDS_A0+ / eDP_TX2+ LVDS_A0- / eDP_TX2- LVDS_A1+ / eDP_TX1+ LVDS_A1- / eDP_TX1- LVDS_A2+ / eDP_TX0+ LVDS_A2- / eDP_TX0+ LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		eDP by build option
LVDS_A_CK+ / eDP_TX3+ LVDS_A_CK- / eDP_TX3-	A81 A82	LVDS Channel A differential clock	O LVDS		
LVDS_VDD_EN / eDP_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 10k	
LVDS_BKLT_EN / eDP_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V	PD 10k	
LVDS_BKLT_CTRL / eDP_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V	PD 100k	eDP to LVDS requirement
LVDS_I2C_CK / eDP_AUX+	A83	DDC lines used for flat panel detection and control.	O 3.3V	PU 2k2 3.3V	
LVDS_I2C_DAT / eDP_AUX-	A84	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 2k2 3.3V	
RSVD / eDP_HPD	A87	Digital Display Interface Hot-Plug Detect	I 3.3V	PD 100k	

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3.3.3. DDI0 Channel

Signal	Pin	Description	I/O	PU/PD	Comment
DDI0_PAIR0+ DDI0_PAIR0- DDI0_PAIR1+ DDI0_PAIR1- DDI0_PAIR2+ DDI0_PAIR2- DDI0_PAIR3+ DDI0_PAIR3- DDI0_PAIR4+ DDI0_PAIR4- DDI0_PAIR5+ DDI0_PAIR5- DDI0_PAIR6+ DDI0_PAIR6-	B71 B72 B73 B74 B75 B76 B81 B82 B77 B78 B91 B92 B93 B94	Digital Display Interface differential pairs	O PCIE		Pair 4 to Pair 6 are not supported
DDI0_HPD	B89	Digital Display Interface Hot-Plug Detect	I 3.3V	PD 100k	
DDI0_CTRLCLK_AUX+	B98	IF DDI0_DDC_AUX_SEL is floating	I/O PCIe	PD 100k	DP1_AUX+ AC coupled on Module
		IF DDI0_DDC_AUX_SEL pulled high	I/O OD 3.3V		HDMI1_CTRLCLK PU 10k 3.3V
DDI0_CTRLDATA_AUX-	B99	IF DDI0_DDC_AUX_SEL is floating	I/O PCIe	PU 100K 3.3V	DP1_AUX- AC coupled on Module
		IF DDI0_DDC_AUX_SEL pulled high	I/O OD 3.3V		HDMI1_CTRLDATA PU 10k 3.3V
DDI0_DDC_AUX_SEL	B95	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.	I/O OD 3.3V	PD 1M	

3.3.4. Gigabit Ethernet

Gigabit Ethernet	Pin	Description	I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: **1000 100 10** MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	I/O Analog		Twisted pair signals for external transforme r.
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.	OD 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.	OD 3.3VSB		
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active	OD		

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Gigabit Ethernet	Pin	Description	I/O	PU/PD	Comment
		low.	3.3VSB		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	OD 3.3VSB		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 1 and 2 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be 250 mA or less.	GND min 3.3V max		Not supported (NC pin)
GBE0_SDP	A49	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE 1588 support such as 1pps signal.	I/O 3.3VSB		

3.3.5. SATA

Signal	Pin	Description	I/O	PU/PD	Comment
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		AC coupled on Module
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		AC coupled on Module
(S)ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	O 3.3V	PU 10k 3.3V	

3.3.6. PCI Express

Signal	Pin	Description	I/O	PU/PD	Comment
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		AC coupled on module
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		AC coupled off module
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		AC coupled on module
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		AC coupled off module
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		AC coupled on module
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		AC coupled off module
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		AC coupled on module
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		AC coupled off module
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		

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3.3.7. Express Card (Not supported)

Signal	Pin	Description	I/O	PU/PD	Comment
EXCD0_CPPE# EXCD1_CPPE#	A49 B48	PCI ExpressCard: PCI Express capable card request	I 3.3V	PU 10k 3.3V	Not supported
EXCD0_PERST# EXCD1_PERST#	A48 B47	PCI ExpressCard: reset	O 3.3V		Not supported

3.3.8. LPC Bus

Signal	Pin	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V		
LPC_DRQ0# LPC_DRQ1#	B8 B9	LPC serial DMA request	I 3.3V		NC. No support on Apollo Lake platform
LPC_SERIRQ	A50	LPC serial interrupt	I/O OD 3.3V	PU 8k2 3.3V	
LPC_CLK	B10	LPC clock output - 33MHz nominal	O 3.3V		The LPC_CLK frequency is 25M

3.3.9. USB 1.1/2.0

Signal	Pin	Description	I/O	PU/PD	Comment
USB0+ USB0-	A46 A45	USB differential data pairs for Port 0	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB1+ USB1-	B46 B45	USB differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB2+ USB2-	A43 A42	USB differential data pairs for Port 2	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB3+ USB3-	B43 B42	USB differential data pairs for Port 3	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB4+ USB4-	A40 A39	USB differential data pairs for Port 4	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB5+ USB5-	B40 B39	USB differential data pairs for Port 5	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB6+ USB6-	A37 A36	USB differential data pairs for Port 6	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB7+ USB7-	B37 B37	USB differential data pairs for Port 7	I/O 3.3VSB		USB 1.1/ 2.0 compliant
USB_HOST_PRSNT	B96	Module USB client may detect the presence of a USB host. A high value indicates that a host is present.	I 3.3VSB		
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the	I 3.3VSB	PU 10k 3.3VSB	Do not pull high on carrier

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Signal	Pin	Description	I/O	PU/PD	Comment
		module. An open drain driver from a USB current monitor on the carrier board may drive this line low.			
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3VSB	PU 10k 3.3VSB	Do not pull high on carrier
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull high on carrier
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull high on carrier
USB0_HOST_PRSNT	B48	Module USB client may detect the presence of a USB host on USB0. A high value indicates that a host is present	I 3.3VSB		Not supported
USB7_HOST_PRSNT	B96	Module USB client may detect the presence of a USB host on USB7. A high value indicates that a host is present	I 3.3VSB	PU 10k 3.3VSB	

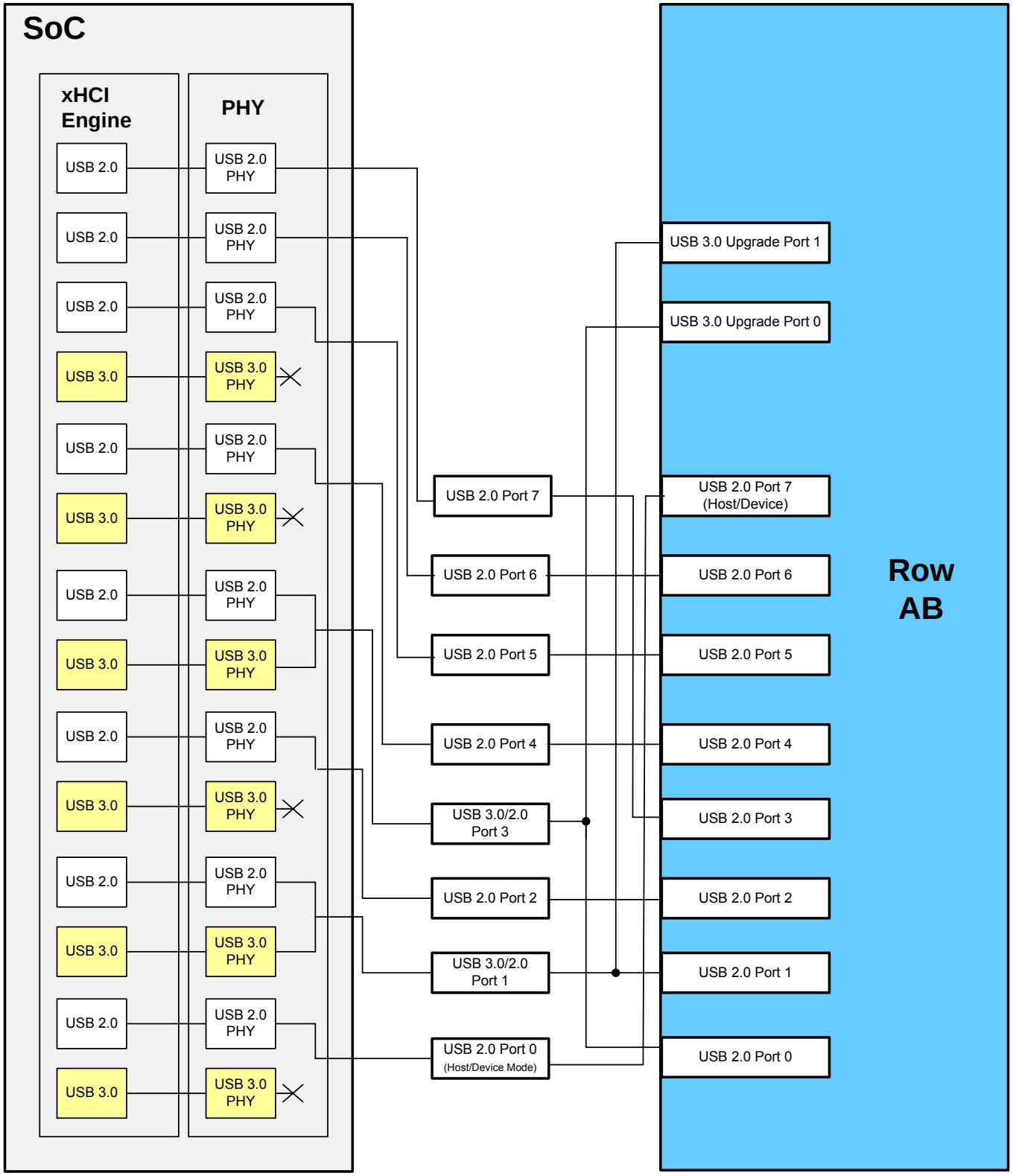
Note: USB port 7 can support USB Client (may vary between operating systems).

3.3.10. USB 3.0 Extension

Signal	Pin	Description	I/O	PU/PD	Comment
USB_SSRX0- USB_SSRX0+	A22 A23	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB0	I PCIE		
USB_SSTX0- USB_SSTX0+	B22 B23	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB0	O PCIE		AC coupled on module
USB_SSRX1- USB_SSRX1+	A25 A26	Additional Receive signal differential pairs for the SuperSpeed USB data path on USB1	I PCIE		
USB_SSTX1- USB_SSTX1+	B25 B26	Additional Transmit signal differential pairs for the SuperSpeed USB data path on USB1	O PCIE		AC coupled on module

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3.3.11. USB Root Segmentation



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3.3.12. SPI (BIOS only)

Signal	Pin	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash.	O 3.3VSB	PU 10k 3.3VSB	
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash.	I 3.3VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB		
SPI_POWER	A91	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier	O P 3.3VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I	PU 10k 3.3VSB	Carrier shall pull to GND or leave not connected
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device.	I	PU 10k 3.3VSB	Carrier shall pull to GND or leave not connected

3.3.13. Miscellaneous

Signal	Pin	Description	I/O	PU/PD	Comment
SPKR	B32	Output for audio enunciator, the “speaker” in PC-AT systems	O 3.3V	PU 10k 3.3V	
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V		
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3V		
THERMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3V		
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan’s RPM.	O OD 3.3V	PU 2.2k 3.3V	There shall be PD on carrier board
FAN_TACHIN11	B102	Fan tachometer input for a fan with a two pulse output.	I OD 3.3V	PU 10k 3.3V	
TPM_PP11	A96	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V	PD 100k	PD only when TPM on module (TBD)

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3.3.14. SMBus

Signal	Pin	Description	I/O	PU/PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line. Power sourced through 5V standby rail and main power rails.	I/O OD 3.3VSB	PU 8k2 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line. Power sourced through 5V standby rail and main power rails.	I/O OD 3.3VSB	PU 8k2 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 5V standby rail and main power rails.	I 3.3VSB	PU 10k 3.3VSB	

3.3.15. I2C Bus

Signal	Pin	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output/input	I/O OD 3.3VSB	PU 2k2 3.3VSB	Source SEMA BMC or Apollo Lake SoC as alternative. (BMC by default)
I2C_DAT	B34	General purpose I²C port data I/O line	I/O OD 3.3VSB	PU 2k2 3.3VSB	Source SEMA BMC or Apollo Lake SoC as alternative. (BMC by default)

3.3.16. General Purpose I/O (GPIO)

Signal	Pin	Description	I/O	PU/PD	Comment
GPO[0]	A93	General purpose output pins.	O 3.3V	PD 10k	After hardware RESET output low
GPO[1]	B54	General purpose output pins.	O 3.3V	PD 10k	After hardware RESET output low
GPO[2]	B57	General purpose output pins.	O 3.3V	PD 10k	After hardware RESET output low
GPO[3]	B63	General purpose output pins.	O 3.3V	PD 10k	After hardware RESET output low
GPI[0]	A54	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10k 3.3V	
GPI[1]	A63	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10k 3.3V	
GPI[2]	A67	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10k 3.3V	
GPI[3]	A85	General purpose input pins. Pulled high internally on the module.	I 3.3V	PU 10k 3.3V	

Notes: GPO[0:3], PU 10k 3.3V is by build option for programming these pins to be GPI.

GPI[0:3], PD 10k is by build option for programming these pins to be GPO.

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3.3.17. Serial Interface Signals

Signal	Pin	Description	I/O	PU/PD	Comment
SER0_TX	A98	General purpose serial port transmitter (TTL level output)	O CMOS	PU 4k7 5V	Power rail tolerance 5V/12V There shall be PD on carrier board
SER0_RX	A99	General purpose serial port receiver (TTL level input)	I CMOS	PU 4k7 5V	Power rail tolerance 5V/12V
SER1_TX	A101	General purpose serial port transmitter (TTL level output)	O CMOS	PU 4k7 5V	Power rail tolerance 5V/12V There shall be PD on carrier board
SER1_RX	A102	General purpose serial port receiver (TTL level input)	I CMOS	PU 4k7 5V	Power rail tolerance 5V/12V

3.3.18. Power And System Management

Signal	Pin	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge.	I 3.3VSB	PU 10k 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low request for module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.	I 3.3VSB	PU 10k 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3VSB		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow carrier based FPGAs or other configurable devices time to be programmed.	I 3.3V	PU 100k 3.3VSB	
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as “PS_ON”) may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB		
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB		Not supported, connect to SUS_S4#
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 10k 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 10k 3.3VSB	Not supported, connected to WAKE0#

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Signal	Pin	Description	I/O	PU/PD	Comment
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I 3.3VSB	PU 10k 3.3VSB	
LID#	A103	LID button. Low active signal used by the ACPI operating system for a LID switch.	I OD 3.3VSB	PU 10k 3.3VSB	Emulate GPIO (BIOS)
SLEEP#	B103	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I OD 3.3VSB	PU 10K 3.3VSB	Emulated GPIO (BIOS)

3.3.19. Power and Ground

Signal	Pin	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109	Primary power input: +12V nominal See section 7 “Electrical Specifications“ for allowable input range. All available VCC_12V pins on the connector(s) shall be used.	P		4.75-20 V
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. See section 7 “Electrical Specifications“ for allowable input range. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		5Vsb ±5%
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A66, A80, A90, A96, A100, A110, B1, B11, B21 ,B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path.	P		

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4. Module Interfaces

This chapter describes connectors and pinouts, LEDs and switches that are used on the module but are not included in the PICMG standard specification

4.1. Connector, Switch and LED Locations

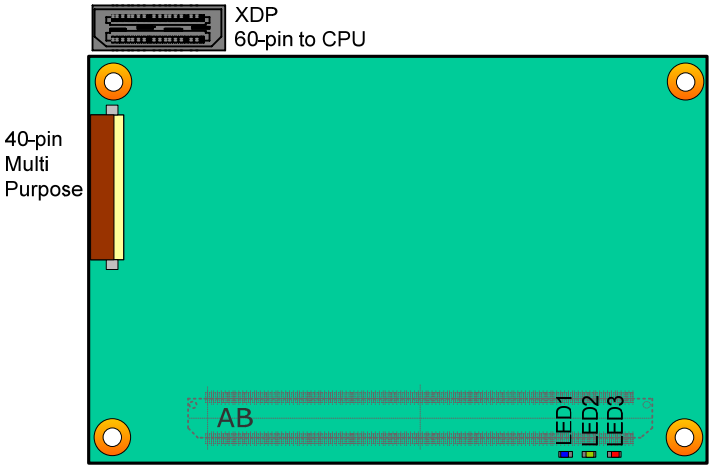


Figure 3: nanoX-AL Connector, Switch and LED Locations

Note: The optional MIPI60 Debug Header is located on the breakout PCB.

nanoX-AL and the DB40 Debug Module

(the diagram below is for illustration purpose only)

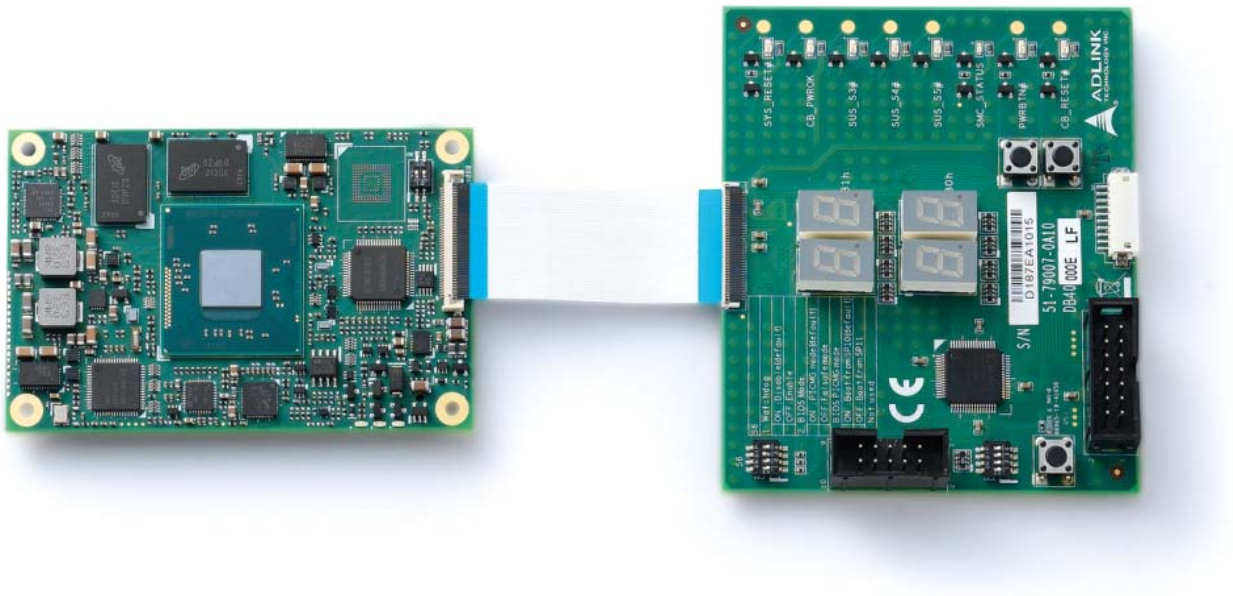


Figure 4: nanoX-AL and the DB40 Debug Module

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4.2. 40-pin Debug Connector

FPC Connector Type: FCI 59GF Flex 10042867

Pin Orientation



1 40

40-pin Debug Connector Pin Definition on the COM Express Module

Pin #	Interface	Siganls	Remark
1	NC	RSVD	
2	For SMC Debug	SMC_STATUS	Connect to LED
3		BIOS_MODE	Connect to Jumper for Debug
4		SEL_BIOS	Connect to Jumper for Debug
5		POSTWDT_DIS#	Connect to Jumper for Debug
6	Test Point	SUS_S5#	
7		SUS_S4#	
8		SUS_S3#	
9		CB_PWROK	
10		CB_RESET#	
11		SYS_RESET#	
12		PWRBTN#	
13	SMC Program interface	SMC_OCD0B	Include a jumper to connect OCD0B via 1Kohm pull-down to GND
14		SMC_OCD0A	Include a jumper to connect OCD0A via 1Kohm pull-up to 3.3V_SMC
15		SMC_CLK	
16		SMC_DATA	
17		SMC_RESET_IN#	
18		SMC_FLMD0	
19		SMC_RXD6	
20		SMC_TXD6	
21		GND3	
22		3V3_A	3.3VSB provided from COM module
23		3V3_SMC1	3.3VSB provided from COM module

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Pin #	Interface	Siganls	Remark
24	LPC Debug card Interface	LPC_AD0	
25		LPC_AD1	
26		LPC_AD2	
27		LPC_AD3	
28		LPC_FRAME#	
29		CLK33_LPC	
30		RST#	
31		BIOS_DIS0	
32		GND2	
33		3V3_LPC	System power 3.3V provided from COM module
34	SPI Program Interface	SPI_BIOS_CLK	
35		SPI_BIOS_MOSI	
36		SPI_BIOS_MISO	
37		SPI_BIOS_CS1#	
38		SPI_BIOS_CS0#	
39		GND1	
40		VCC_SPI_IN	SPI Power Input from flash tool to module. HW needs to add MOS FET to switch SPI power for SPI ROM

Table 2: 40-pin Debug Connector Pin Definition

Note: The pin definition on the debug module is the inverse of that on the COM Express module.

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4.3. Status LEDs

To facilitate easier maintenance, status LED's are mounted on the board.



LED1 LED2 LED3

LED Descriptions

Name	Color	Connection	Function
LED1	Blue	BMC output	Power Sequence Status Code (BMC) Power Changes, RESET (see 5.1.4 Exception Codes below)
LED2	Green	Power Source 3Vcc	S0 LED ON S3/S4/S5 LED OFF ECO mode LED OFF
LED3	Red	BMC output and same signal as WDT (B27) on BtB connector	Module power up WD LED = LED OFF Watchdog counting WD LED = Keep Last State Watchdog timed out WD LED = LED ON Watchdog RESET WD LED = LED ON Rebooted after WD RESET WD LED = LED ON Rebooted after PWRBTN WD LED = LED OFF Rebooted after RESET BTN WD LED = LED OFF Note: only a RESET not initiated by the BMC can clear the WD LED (user action)

Table 3: nanoX-AL LED Descriptions

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4.4. MIPI60 Debug Header (build option)

Not all pins of the Intel® MIPI60 connector are connected to the CombiProbe Intel x86/x64 MIPI60-C.



Pin	Signal	Pin	XDP Signal
1	VREF_DEBUG	2	TMS
3	TCK0	4	TDO
5	TDI	6	Open Drain Reset Out
7	Reset In	8	No Connect
9	TRST_N	10	PREQ_N
11	PRDY_N	12	VREF_TRACE
13	PTI_0_CLK	14	PTI_1_CLK
15	GND	16	GND
17	No Connect	18	PTI_1_DATA[0]
19	PTI_0_DATA[0]	20	PTI_1_DATA[1]
21	PTI_0_DATA[1]	22	PTI_1_DATA[2]
23	PTI_0_DATA[2]	24	PTI_1_DATA[3]
25	PTI_0_DATA[3]	26	No Connect
27	PTI_0_DATA[4]	28	No Connect
29	PTI_0_DATA[5]	30	No Connect
31	PTI_0_DATA[6]	32	No Connect
33	PTI_0_DATA[7]	34	Reset Out
35	No Connect	36	Boot Stall
37	No Connect	38	CPU Boot Stall
39	No Connect	40	Power Button
41	No Connect	42	PWRGOOD
43	No Connect	44	No Connect
45	No Connect	46	No Connect
47	No Connect	48	I2C_SCL
49	No Connect	50	I2C_SDA
51	No Connect	52	No Connect
53	No Connect	54	DBG_UART_TX
55	No Connect	56	DBG_UART_RX
57	GND	58	GND
59	No Connect	60	No Connect

Table 4: MIPI60 Debug Header Pin Definition

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4.5. Switch Settings

Switch Locations

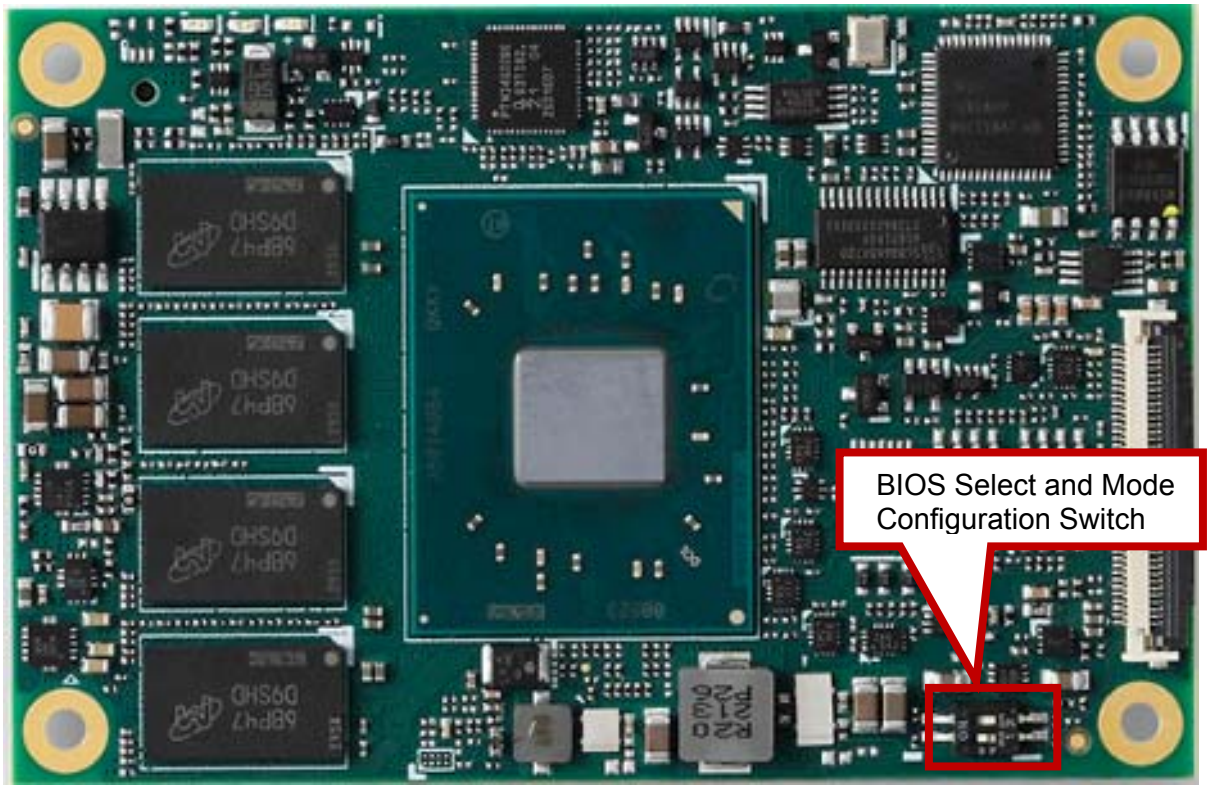


Figure 5: cExpress Switch Locations

BIOS Select and Mode Configuration Switch

Module has two BIOS chips and BIOS operation can be configured to "PICMG" and "Failsafe" modes using BSW1, Pin 2. (name of this swtich on circuit is BSW1)

Setting the module to PICMG mode will configure the BIOS chips on the module as SPI0 and SPI1. In PICMG mode, a BIOS chip CANNOT be placed in SPI0 on the carrier.

In dual-BIOS Failsafe mode, both BIOS chips on the module are configured as SPI1. Only one of the two is connected to the SPI bus at any given time. In case of BIOS failure of the primary SPI1 BIOS, the system will reboot and switch to the secondary SPI1 BIOS on the module. In Failsafe mode, it is allowed to also have an SPI0 BIOS on the carrier.

In both modes, strapping can select whether to boot from SPI0 or SPI1 (BSW1 Pin 1).

Mode	Pin 1	Pin 2
Boot from SPI0 (Default)	On	—
Boot from SPI1	Off	—
Set BIOS to PICMG mode	—	On
Set BIOS to Failsafe BIOS mode (Default)	—	Off

Table 5: BIOS Select and Mode Configuration Switch Settings

Note: The switch can be removed and 0 ohm used to support all configurations above by project basis.

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5. Smart Embedded Management Agent (SEMA)

The onboard microcontroller (BMC) implements power sequencing and Smart Embedded Management Agent (SEMA) functionality. The microcontroller communicates via the System Management Bus with the CPU/chipset. The following functions are implemented:

- Total operating hours counter. Counts the number of hours the module has been run in minutes.
- On-time minutes counter. Counts the seconds since last system start.
- Temperature monitoring of CPU and board temperature. Minimum and maximum temperature values of CPU and board are stored in flash.
- Power cycles counter
- Boot counter. Counts the number of boot attempts.
- Watchdog Timer. Set/Reset/Disable Watchdog Timer. Features auto-reload at power-up.
- System Restart Cause. Power loss/BIOS Fail/Watchdog/Internal Reset/External Reset
- Fail-safe BIOS support. In case of a boot failure, hardware signals tells external logic to boot from fail-safe BIOS.
- Flash area. 1kB Flash area for customer data
- 2K Bytes Protected Flash area. Keys, IDs, etc. can be stored in a write- and clear-protectable region.
- Board Identify. Vendor/Board/Serial number/Production Date
- Main-current & voltage. Monitors drawn current and main voltages

For a detailed description of SEMA features and functionality, please refer to **SEMA Technical Manual** and **SEMA Software Manual**, downloadable at: **http://www.adlinktech.com/sema/**.

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5.1. Board Specific SEMA Functions

5.1.1. Voltages

The BMC of the nanoX-AL implements a voltage monitor and samples several onboard voltages. The voltages can be read by calling the SEMA function “Get Voltages”. The function returns a 16-bit value divided into high-byte (MSB) and low-byte (LSB).

ADC Channel	Voltage Name	Voltage Formula [V]
0	VCORE	(MSB<<8 + LSB) x 3.3 / 1024
1	VGFX	(MSB<<8 + LSB) x 3.3 / 1024
2	VMEM	(MSB<<8 + LSB) x 3.3 / 1024
3	5VSB	(MSB<<8 + LSB) x 1.826 x 3.3 / 1024
4	VIN	(MSB<<8 + LSB) x 6.000 x 3.3 / 1024
5	5V	(MSB<<8 + LSB) x 1.826 x 3.3 / 1024
6	3.3V	(MSB<<8 + LSB) x 1.100 x 3.3 / 1024
7	3.3VSB	(MSB<<8 + LSB) x 1.100 x 3.3 / 1024
8	(MAIN CURRENT)	Use Main Current Function

Table 6: SEMA Onboard Voltage Monitor

5.1.2. Main Current

The BMC of the nanoX-AL implements a current monitor. The current can be read by calling the SEMA function “Get Main Current”. The function returns four 16-bit values divided in high-byte (MSB) and low-byte (LSB). These 4 values represent the last 4 currents drawn by the board. The values are sampled every 250ms. The order of the 4 values is NOT in chronological order. Access by the BMC may increase the drawn current of the whole system. In this case, there are still 3 samples not influenced by the read access.

$$\text{Main Current} = (\text{MSB_n}<<8 + \text{LSB_n}) \times 8.06\text{mA}$$

5.1.3. BMC Status

This register shows the status of BMC controlled signals on the nanoX-AL.

Status Bit	Signal
0	WDT_OUT
1	LVDS_VDDEN
2	LVDS_BKLTEN
3	BIOS_MODE
4	POSTWDT_DISn
5	SEL_BIOS
6	BIOS_DIS0n
7	BIOS_DIS1n

Table 7: SEMA BMC Status

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5.1.4. Exception Codes

In case of an error, the BMC drives a blinking code on the blue Status LED (LED1). The same error code is also reported by the BMC Flags register. The Exception Code is not stored in the Flash Storage and is cleared when the power is removed. Therefore, a “Clear Exception Code” command is not needed or supported.

Exception Code	Error Message
0	NOERROR
2	NO_SUSCLK
3	NO_SLP_S5
4	NO_SLP_S4
5	NO_SLP_S3
6	NO_CB_PWRGD
7	BIOS_FAIL
8	RESET_FAIL
9	RESETIN_FAIL
10	CRITICAL_TEMP
11	POWER_FAIL
12	VOLTAGE_FAIL
13	NO_SYS_GD
14	NO_3V3_A_PGD
15	NO_VDDQ_PG
16	NO_P_5V_3V3_S0_PG
17	NO_1V0_A_PG
18	NO_VCORE_PG

Table 8: SEMA Exception Codes

5.1.5. BMC Flags

The BMC Flags register returns the last detected Exception Code since power-up and shows the BIOS in use and the power mode.

Bit	Description
[0 ~ 4]	Exception Code
[6]	0 = AT mode 1 = ATX mode
[7]	0 = Standard BIOS 1 = Fail-safe BIOS.

Table 9: SEMA BMC Flags

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6. System Resources

6.1. System Memory Map

Address Range (hex)	Description
FF00_0000 – FFFF_FFFF	IFAW (BIOS)
FED0_0000 – FEDF_33FF	HPET
FEC0_0000 – FECF_FFFF	IOAPIC
0K –1MB	DOS DRAM

6.2. I/O Map

I/O Address	IOSF Primary Target	IOSF SB Target
000h–01Fh	P2SB	Terminate
020h–021h	P2SB	ITSS (interrupt)
024h–025h	P2SB	ITSS (interrupt)
028h–029h	P2SB	ITSS (interrupt)
02Ch–02Dh	P2SB	ITSS (interrupt)
02Eh–02Fh	P2SB	LPC/eSPI
030h–031h	P2SB	ITSS (interrupt)
034h–035h	P2SB	ITSS (interrupt)
038h–039h	P2SB	ITSS (interrupt)
03Ch–03Dh	P2SB	ITSS (interrupt)
040h	P2SB	ITSS (Timer 0 Register)
041h	P2SB	Terminate
042h	P2SB	ITSS (Timer 2 Register)
043h	P2SB	ITSS (Timer Control Word Register)
04Eh–04Fh	LPC/eSPI	LPC/eSPI
050h	P2SB	ITSS (alias of 040h)
051h	P2SB	Terminate
052h	P2SB	ITSS (alias of 042h)
053h	P2SB	ITSS (alias of 043h)
060h	P2SB	LPC/eSPI
061h	P2SB	ITSS (CPU I/F)
062h	P2SB	LPC/eSPI
063h	P2SB	ITSS (CPU I/F)
064h	P2SB	LPC/eSPI
065h	P2SB	ITSS (CPU I/F)

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I/O Address	IOSF Primary Target	IOSF SB Target
066h	P2SB	LPC/eSPI
067h	P2SB	ITSS (CPU I/F)
070h	P2SB	ITSS (CPU I/F), RTC, PMC
071h	P2SB	RTC, PMC
072h–073h	P2SB	RTC, PMC
073h	P2SB	RTC, PMC
074h	P2SB	RTC, PMC
075h	P2SB	RTC, PMC
076h–077h	P2SB	RTC, PMC
080h	P2SB	LPC/eSPI or PMC
081h–083h	P2SB	Terminate
084h–086h	P2SB	LPC/eSPI or PMC
087h	P2SB	Terminate
088h	P2SB	LPC/eSPI or PMC
089h–08Bh	P2SB	Terminate
08Ch–08Eh	P2SB	LPC/eSPI or PMC
08Fh	P2SB	Terminate
090h	P2SB	LPC/eSPI
091h	P2SB	Terminate
092h	P2SB	ITSS (CPU I/F)
093h	P2SB	Terminate
094h–096h	P2SB	LPC/eSPI or PMC
097h	P2SB	Terminate
098h	P2SB	LPC/eSPI or PMC
099h–09Bh	P2SB	Terminate
09Ch–09Eh	P2SB	LPC/eSPI or PMC
09Fh	P2SB	Terminate
0A0h–0A1h	P2SB	ITSS (interrupt)
0A4h–0A5h	P2SB	ITSS (interrupt)
0A8h–0A9h	P2SB	ITSS (interrupt)
0ACh–0ADh	P2SB	ITSS (interrupt)
0B0h–0B1h	P2SB	ITSS (interrupt)
0B2h–0B3h	P2SB	PMC
0B4h–0B5h	P2SB	ITSS (interrupt)
0B8h–0B9h	P2SB	ITSS (interrupt)
0BCh–0BDh	P2SB	ITSS (interrupt)
0C0h–0DFh	P2SB	Terminate
0F0h	P2SB	Terminate

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I/O Address	IOSF Primary Target	IOSF SB Target
170h–177h	P2SB	Terminate
2F8h–2FFh	P2SB	Serial Port
240h–24Fh	P2SB	Serial Port
2F8h–2FFh	P2SB	Serial Port
376h	P2SB	Terminate
3F6h	P2SB	Terminate
3F8h–3FFh	P2SB	Serial Port
4D0h–4D1h	P2SB	ITSS (interrupt)
CF9h	P2SB	ITSS (CPU I/F)

6.3. Interrupt Request (IRQ) Lines

APIC Interrupt Map

The following table describes the APIC interrupt mapping. The Apollo Lake platform supports 120 IRQs in total.

IO APIC Pin	Routing
0	8259
1	PS2 Keyboard
2	8254 Counter 0, HPET #0 (legacy mode)
3	Serial Port 3
4	Serial Port 4
5	NA
6	NA
7	NA
8	RTC, HPET #1 (legacy mode)
9	Option for configurable sources including internal ACPI/PCI devices, SCI and TCO
10	Serial Port 1
11	Serial Port 2
12	PS2 Mouse
13	xDCI
14	Option for configurable sources including GPIO, internal ACPI/PCI devices

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IO APIC Pin	Routing
15	Option for configurable sources including internal ACPI/PCI devices
16	Option for configurable sources including internal PIRQA, internal ACPI/PCI devices
17	PIRQB (xHCI)
18	Option for configurable sources including internal PIRQC, internal ACPI/PCI devices
19	Option for configurable sources including internal PIRQD, internal ACPI/PCI devices
20	Option for configurable sources including internal PIRQE, SCI, TCO, internal ACPI/PCI devices and HPET
21	Option for configurable sources including internal PIRQF, SCI, TCO, internal ACPI/PCI devices and HPET
22	Option for configurable sources including internal PIRQG, SCI, TCO, internal ACPI/PCI devices and HPET
23	Option for configurable sources including internal PIRQH, SCI, TCO, internal ACPI/PCI devices and HPET
24	Punit (DPTF)
25	Audio
26	ISH
27	I2C 0
28	I2C 1
29	I2C 2
30	I2C 3
31	I2C 4
32	I2C 5
33	I2C 6
34	I2C 7
35	SPI 0
36	SPI 1
37	SPI 2
38	UFS
39	EMMC
40	PMC IPC
41	PMC PMIC
42	SDIO
43	reserved
44	reserved
45	reserved

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IO APIC Pin	Routing
46	reserved
47	reserved
48	reserved
49	reserved
50 - 119	GPIO (Not for end user)

Note: These IRQs can be used for PCI devices when onboard device is disabled.

APIC Mode

IRQ#	Typical Intterupt Resource	Connected to Pin	Available
0	Counter 0	N/A	No
1	Keyboard controller	IRQ1 via SERIRQ	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 4 (COM3)	IRQ3 via SERIRQ	Note (1)
4	Serial Port 3 (COM4)	IRQ4 via SERIRQ	Note (1)
5	N/A	N/A	Note (1)
6	N/A	N/A	Note (1)
7	N/A	N/A	Note (1)
8	Real-time clock	N/A	No
9	N/A	IRQ9 via SERIRQ	Note (1)
10	Serial Port 1 (COM1)	IRQ10 via SERIRQ	Note (1)
11	Serial Port 2 (COM2)	IRQ11 via SERIRQ	Note (1)
12	PS/2 Mouse	IRQ12 via SERIRQ	Note (1)
13	FERR# logic	N/A	Note (1)
14	SATA Primary	IRQ14 via SERIRQ	Note (1)
15	SATA Secondary	IRQ15 via SERIRQ	Note (1)
16	N/A	P.E.G Root Port, Intel HDA, PCIE Port 0/1/2/3/4/5/6, EHCI Conterller #2, I.G.D, XHCI Controller	Note (1)
17	N/A	PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port,	Note (1)
18	N/A	PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port, SMBus Controller, EHCI Controller #2	Note (1)
19	N/A	PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port,	Note (1)
20	N/A	GbEController	Note (1)
21	N/A		Note (1)
22	N/A	Intel HDA	Note (1)
23	N/A	EHCI Controller #1	Note (1)

Note: These IRQs can be used for PCI devices when onboard device is disabled.

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6.4. PCI Configuration Space Map

Logical Function	Bus	Device	Function
Host Bridge	0	0	0
DPTF (Camarillo)	0	0	1
NPK	0	0	2
NPK (PSF ghost)	0	0	5
GMM	0	0	3
Gen	0	2	0
Iunit	0	3	0
Reserved (CSE)		7	0
P2SB	0	13	0
PMC	0	13	1
SPI	0	13	2
Shared SRAM	0	13	3
Audio	0	14	0
CSE-HECI1	0	15	0
CSE-HECI2	0	15	1
CSE-HECI3	0	15	2
CSE-fTPM (PSF ghost)	0	15	7
CSE-HOFFL	0	16	0
ISH	0	17	0
SATA	0	18	0
PCIe-A 1	0	19	0
PCIe-A 2	0	19	1
PCIe-A 3	0	19	2
PCIe-B 1 (multpixted with USB3.0 port)	0	19	3
PCIe-B 2 (connect to onboard LAN)	0	20	0
PCIe-A 1	0	20	1
USB-Host (xHCI)	0	21	0
USB-Device (xDCI)	0	21	1
I2C 0	0	22	0
I2C 1	0	22	1
I2C 2	0	22	2
I2C 3	0	22	3
CSE I2C 6/7 access	0	22	6
CSE SSRAM access	0	22	7
I2C 4	0	23	0

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Logical Function	Bus	Device	Function
I2C 5	0	23	1
I2C 6	0	23	2
I2C 7	0	23	3
UART 0	0	24	0
UART 1	0	24	1
UART 2	0	24	2
UART 3	0	24	3
SPI 0	0	25	0
SPI 1	0	25	1
SPI 2	0	25	2
PWM	0	26	0
SD Card	0	27	0
eMMC	0	28	0
UFS	0	29	0
SDIO	0	30	0
LPC	0	31	0
SMBUS	0	31	1

6.5. PCI Interrupt Routing Map

INT Line	PCIE port1	PCIE port 2	PCIE port 3	PCIE Onboard LAN i210	Mobile IGFX	PUNIT Device	SMBus Controller
Int0	INTA:22	INTB:23	INTC:22	INTB:21	NTD:19		
Int1	INTB:23	INTC:20	INTD:23	INTC:22		INTF:24	INTE:20
Int2	INTC:20	INTD:21	INTA:20	INTD:23			
Int3	INTD:21	INTA:22	INTB:21	INTA:20			

INT Line	NPK Device	IUNT	PMC	HD Audio	CES	ISH	SATA Controller	XHCI	XDCI
Int0	INTA:16	INTF:21	INTA:40	INTA:25	INTE:20	INTE:26	INTA:19	INTB:17	
Int1									INTC:13
Int2									
Int3									

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INT Line	I2C0	I2C1	I2C2	I2C3	I2C4	I2C5	I2C6	I2C7
Int0	INTA:27				INTF:31			
Int1		INTB:28				INTB:32		
Int2			INTC:29				INTC:33	
Int3				INTD:30				INTD:34

INT Line	SPI1	SPI3	SPI3	SD Host #0	SD Host #1	SD Host #2	SD Host #3
Int0	INTA:35			INTC:15	INTD:39	INTH:38	INTB:37
Int1		INTB:36					
Int2			INTC:37				
Int3							

6.6. SMBus Address Table

Device	Address
DIMMA	A0h
DIMMB	A4h
BMC	50h
Extend GPIO	40h
I210	49h
USB2514BI	58h
LM73	92h
PEX8605	B7h,C1h
NXP(eDP to LVDS transmitter)	C0h

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7. BIOS Setup

7.1. Menu Structure

This section presents the six primary menus of the BIOS Setup Utility. Use the following table as a quick reference for the contents of the BIOS Setup Utility. The subsections in this section describe the submenus and setting options for each menu item. The default setting options are presented in **bold**, and the function of each setting is described in the right hand column of the respective table.

Main	Advanced	Chipset	Security	Boot	Save & Exit
BIOS Information System Information Board Information ► System Date and Time Access Level	CPU Configuration ► Graphics Configuration ► Power Management ► System Management ► Thermal Management ► Watchdog Timer ► CSM Configuration ► Super IO Configuration ► Serial Console Redirection ► USB ► Network ► Miscellaneous ► Driver Health ► Trusted Computing ► SDIO Configuration ►	North Bridge ► South Bridge ► Uncore Configuration ► South Cluster ► Configuration ►	Setup Administrator Password User Password Secure Boot ►	Boot Configuration FIXED BOOT ORDER Priorities UEFI USB Key Drive BBS Priorities	Save Change and Exit Discard Changes and Exit Save Changes and Reset Discard Changes and Reset Save Options Boot Override

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7.2. Main

The Main Menu provides read-only information about your system and also allows you to set the System Date and Time. Refer to the tables below the screen shot of this menu for details of the submenus and settings.

7.2.1. Main > BIOS Information

Feature	Options	Description
BIOS Vendor	Info only	American Megatrends
BIOS Version	Info only	ADLINK BIOS version
Build Date	Info only	ADLINK BIOS Build Date
MRC Version	Info only	Display MRC Version
GOP Version	Info only	Display GOP Version
TXE FW Version	Info only	Display TXE FW Version
BIOS Boot Source	Info only	Display BIOS Boot Source

7.2.2. Main > System Information

Feature	Options	Description
Project Name	Info only	Display Project Name.
CPU Board version	Info only	Display CPU Board Version.
CPU Board String	Info only	Display CPU Board String.
CPU Frequency	Info only	Display CPU Frequency.
Total Memory	Info only	Display Installed Memory Size.
Memory Frequency	Info only	Display Memory Frequency.
SOC SKU	Info only	Display SOC SKU Version

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7.2.3. Main > Board Information

Feature	Options	Description
Board Information	Submenu	
Board Information	Info only	
Serial Number	Info only	Display SEMA serial Number.
Manufacturing Date	Info only	Display SEMA manufacturing date.
Last Repair Date	Info only	Display SEMA last repair date.
MAC ID	Info only	Display SEMA MAC ID.
Runtime Statistics	Info only	
Total Runtime	Info only	The returned value specifies the total time in minutes the system is running in S0 state.
Current Runtime	Info only	The returned value specifies the time in seconds the system is running in S0 state. This counter is cleared when the system is removed from the external power supply.
Power Cycles	Info only	The returned value specifies the number of times the external power supply has been shut down
Boot Cycles	Info only	The Boot counter is increased after a HW- or SW-Reset or after a successful power-up.
Boot Reason	Info only	The boot reason is the event which causes the reboot of the system.

7.2.4. Main >System Date/Time

Feature	Options	Description
System Date	Info only	
System Time	Info only	

7.2.5. Main >Access Level

Feature	Options	Description
Access Level	Info only	

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7.3. Advanced

This menu contains the settings for most of the user interfaces in the system.

7.3.1. Advanced > CPU Configuration

Feature	Options	Description
CPU Configuration	Info only	
Socket 0 CPU Information	Submenu	Socket Specific CPU Information.
Stocket 0 CPU information	Info only	
CPU Signature	Info only	Display CPU Signature.
Microcode Patch	Info only	Display Microcode Patch.
Max CPU Speed	Info only	Display Max CPU speed.
Min CPU speed	Info only	Display Min CPU speed.
Processor Cores	Info only	Display Processor Cores.
Intel HT Technology	Info only	Display Intel HT Technology support or not.
Intel VT-x Technology	Info only	Display Intel VT-x Technology support or not.
L1 Data Cache	Info only	Display cache info.
L1 Code Cache	Info only	Display cache info.
L2 Cache	Info only	Display cache info.
L3 Cache	Inf o only	Display cache info.
Speed	Info only	Display CPU Speed.
64-bit	Info only	Display 64-bit Support.
CPU Power Management	Submenu	CPU Power Management options.
CPU Power Management Configuration	Info only	
EIST	Disabled **Enabled**	Enable / Disable Intel SpeedStep
Turbo Mode	Disabled **Enabled**	Enable / Disable turbo mode.
Boot performance mode	**Max Performance** Max Battery	Select the performance state that the BIOS will set before OS handoff.
C-States	Disabled **Enabled**	Enable / Disable C Sates.
Enhanced C-states	Disabled **Enabled**	Enable / Disable C1E. When enabled, CPU will switch to minimum speed when all core enter C-States.
Max Package C State	**PC2** PC1 C0	Controls the Max Package C State that the processor will support.
Max Core C State	**Core C6** Core C1	This option controls the Max Core C State that cores will Support.

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Feature	Options	Description
C-State Auto Demotion	Disabled **C1**	Configure C-State Auto Demotion
C-State Un-demotion	Disabled **C1**	Configure C-State Auto Un-demotion
Power Limit 1 Enable	Disabled **Enabled**	Enable / Disable Power Limit 1
Power Limit 1	Info Only	Display Power Limit 1 Power Watts.
Power Limit 1 Clamp Mode	Disabled **Enabled**	Enable / Disable Power Limit 1 Clamp Mode.
Power Limit 1 Power	**Auto** 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25	Power Limit 1 in Watts. Auto will program Power Limit 1 based on silicon default support value.
Power Limit 1 Time Windows	**Auto** 1 2 3 4 5 6 7 8 10 12 14 16 20 24 28 32 40 48 56 64 80 96 112 128	Power Limit 1 Time Windows Value in Seconds. Auto will program Power Limit 1 Time Windows base on silicon default support value.
Active Processor Cores	**Disabled** Enabled	Number of cores to enable in each processor package.
Intel Virtualization Technology	Disabled **Enabled**	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

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Feature	Options	Description
VT-d	Disabled **Enabled**	Enable / Disable CPU VT-d
Bi-directional PROCHOT	Disabled **Enabled**	When a processor thermal sensor trips (either core), the PROCHOT# will be driven. If bi-direction is enabled, external agents can drive PROCHOT# to throttle the processor.
Limit CPUID Maximum	**Disabled** Enabled	When **Enabled**, the processor will limit the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value. When **Disabled**, the processor will return the actual maximum CPUID input value
Execute Disable Bit	Disabled **Enabled**	Enable / Disable the Execute Disable Bit (XD) of the processor. With the XD bit set to enabled certain classes of malicious buffer overflow attacks can be prevented when combined with a supporting OS.
Thermal Monitor	Disabled **Enabled**	Enable / Disable Thermal Monitor.
Monitor Mwait	Disabled Enabled **Auto**	Enable / Disable Monitor Mwait.
Change P-STATE Coordination	**HW_ALL** SW_ALL SW_ANY	Change P-STATE Coordination type.
DTS	Disabled **Enabled**	Enable / Disable Digital Thermal Sensor.

7.3.2. Advanced > Graphics Configuration

Feature	Options	Description
Graphics Configuration	Info only	
LVDS	Info only	
Data format and Color Depth	VESA 24 bpp JEIDA 24 bbp **JEIDA/vesa 18 bpp**	Data format and Color Depth select
LVDS Output Mode	Dual LVDS bus **Signal LVDS bus**	Signal / Dual mode select
DE Polaarity	**Active High** Active Low	DE Polaarity Select
Vsync Polarity	**Active High** Active Low	Vsync Polarity select
Hsync Polarity	**Active High** Active Low	Hsync Polarity select
LVDS Backlight Brightness	0 - **255**	LVDS Backlight Brightness adjust. A change takes effect immediately.

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7.3.3. Advanced > Power Management

Feature	Options	Description
Power Management	Info only	
Enable ACPI Auto Configuration	**Disabled** Enabled	Enables or Disables BIOS ACPI Auto Configuration.
Enable Hibernation	Disabled **Enabled**	Enable or Disable System ability to Hibernate (OS/S4 Sleep State). This option maybe not effective with some OS.
ACPI Sleep State	Suspend Disable **S3 (Suspend to RAM)**	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
Emulation AT/ATX	Emulation AT **ATX**	Select Emulation AT or ATX function. If this option set to [Emulation AT], BIOS will report no suspend functions to ACPI OS. In windows XP, it will make OS show shutdown message during system shutdown.
Lock Legacy Resources	**Disabled** Enabled	Enables or Disables Lock of Legacy Resources.
LID Function	**Disabled** Enabled	Enable / Disable LID Function.
ECO Mode	**Disabled** Enabled	Reduces the power consumption of the system, but after a shutdown, you have to wait at least 5 seconds before you can restart the system.
Power Consumption	Submenu	Power Consumption.

7.3.3.1. Advanced > Power Management > Power Consumption

Feature	Options	Description
Power Consumption	Info Only	
Current Input Current	Info Only	Display Current Input Current
Current Input Power	Info Only	Display Current Input Power
VCORE	Info Only	Display VCORE Voltage
VGFX	Info Only	Display VGFX Voltage
VMEM	Info Only	Display VMEM Voltage
5VSB	Info Only	Display 5VSB Voltage
VIN	Info Only	Display VIN Voltage
3.3V	Info Only	Display 3.3V Voltage
3.3VSB	Info Only	Display 3.3VSB Voltage
RTC	Info Only	Display RTC Voltage

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7.3.4. Advanced > System Management

Feature	Options	Description
System Management	Info Only	
Version	Info Only	Display SEMA Module Version.
SEMA Firmware	Info Only	Display SEMA Firmware Version.
Build Date	Info Only	Display SEMA Firmware Build Date.
SEMA Bootloader	Info Only	Display SEMA Bootloader Version.
Build Date	Info Only	Display SEMA Bootloader Build Date.
SEMA Features	Submenu	Display SEMA Supported Features
SEMA Supported Features	Info only	Display SEMA Supported Features
Flags	Submenu	Flag
Flags	Info only	
BMC Flags	Info Only	
BIOS Select	Info Only	
ATX/AT-Mode	Info Only	
Exception Code	Info Only	

7.3.5. Advanced > Thermal Management

Feature	Options	Description
Thermal Configuration Parameters	Info Only	
Thermal and Fan Speed	Submenu	
Smart Fan	Submenu	
Critical Trip Point	**Disabled** 80 C 90 C 95 C	The value is the temperature threshold of the Critical Trip Point.
Passive Cooling Trip Point	**Disabled** 70 C 80 C 90 C	The value is the temperature threshold of the Passive Cooling Trip Point.

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7.3.5.1. Advanced > Thermal Management > Thermal and Fan Speed

Feature	Options	Description
Temperatures and Fan Speed	Info Only	
CPU Temperature	Info Only	
Current	Info Only	Display Current CPU Temperature
Board Temperature	Info Only	
Current	Info Only	Display Current Board Temperature
Startup	Info Only	Display Startup Board Temperature
Min	Info Only	Display Min Board Temperature
Max	Info Only	Display Max Board Temperature
CPU Fan Speed	Info Only	Display CPU Fan Speed

7.3.5.2. Advanced > Thermal Management > Smart Fan

Feature	Options	Description
Smart Fan	Info Only	
CPU Smart Fan Temperature Source	CPU Sensor **Board Sensor**	CPU Smart Fan Temperature Source
CPU Fan Mode	AUTO (Smart Fan) **Fan Off** Fan On	CPU Fan Mode
PWM Level	0 - **100**	Control PWM Level

7.3.6. Advanced > Watchdog Timer

Feature	Options	Description
Watchdog Timer	Info only	
Power-Up Watchdog	**Disabled** Enabled	The Power Up Watchdog resets the system after a certain amount of time after power up.

7.3.7. Advanced > CSM Configuration

Feature	Options	Description
Compatibility Support Module Configuration	Info only	
CSM Support	**Disableed** Enabled	Enabled / Disabled CSM Support.

7.3.8. Advanced > Super IO Configuration

Feature	Options	Description
NCT5104D	Info only	
Serial Port 1 Configuration	Submenu	Set Parameters of Serial Port 1 (COMA).
Serial Port 2 Configuration	Submenu	Set Parameters of Serial Port 2 (COMB).

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Feature	Options	Description
W83627DHG	Info Only	
Serial Port 1 Configuration	Submenu	Set Parameters of Serial Port 1 (COMA).
Serial Port 2 Configuration	Submenu	Set Parameters of Serial Port 2 (COMB).

7.3.8.1. Advanced > Super IO Configuration > Serial Port 1 Configuration (NCT5104D)

Feature	Options	Description
NCT5104D	Info only	
Serial Port 1 Configuration	Submenu	Set Parameters of Serial Port 1 (COMA).
Serial Port 1 Configuration	Info only	
Serial Port	Disableed **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	Info Only	Display IO / IRQ information of COM Port.
Change Settings	**Auto** IO=240h; IRQ=10; IO=240h; IRQ=3,4,5,6,7,10,11,12 IO=248h; IRQ=3,4,5,6,7,10,11,12 IO=250h; IRQ=3,4,5,6,7,10,11,12 IO=258h; IRQ=3,4,5,6,7,10,11,12	Select an optimal setting for Super IO Device.

7.3.8.2. Advanced > Super IO Configuration > Serial Port 2 Configuration (NCT5104D)

Feature	Options	Description
Serial Port 2 Configuration	Submenu	Set Parameters of Serial Port 2 (COMB).
Serial Port 2 Configuration	Info only	
Serial Port	Disableed **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	Info Only	Display IO / IRQ information of COM Port.
Change Settings	**Auto** IO=248h; IRQ=11; IO=240h; IRQ=3,4,5,6,7,10,11,12 IO=248h; IRQ=3,4,5,6,7,10,11,12 IO=250h; IRQ=3,4,5,6,7,10,11,12 IO=258h; IRQ=3,4,5,6,7,10,11,12	Select an optimal setting for Super IO Device.

7.3.8.3. Advanced > Super IO Configuration > Serial Port 1 Configuration (W83627DHG)

Feature	Options	Description
Serial Port 1 Configuration	Submenu	Set Parameters of Serial Port 1 (COMA).
Serial Port 1 Configuration	Info only	
Serial Port	Disableed **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	Info Only	Display IO / IRQ information of COM Port.
Change Settings	**Auto** IO=3F8h; IRQ=4; IO=3F8h; IRQ=3,4,5,6,7,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,10,11,12	Select an optimal setting for Super IO Device.

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7.3.8.4. Advanced > Super IO Configuration > Serial Port 2 Configuration (W83627DHG)

Feature	Options	Description
Serial Port 2 Configuration	Submenu	Set Parameters of Serial Port 2 (COMB).
Serial Port 2 Configuration	Info only	
Serial Port	Disableed **Enabled**	Enable or Disable Serial Port (COM).
Device Settings	Info Only	Display IO / IRQ information of COM Port.
Change Settings	**Auto** IO=2F8h; IRQ=3; IO=3F8h; IRQ=3,4,5,6,7,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,10,11,12	Select an optimal setting for Super IO Device.

7.3.9. Advanced > Serial Console Redirection

Feature	Options	Description
COM1	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. The item will be lunched before enable Console Redirection.
COM2	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. The item will be lunched before enable Console Redirection.
COM3	Info only	
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. The item will be lunched before enable Console Redirection.
COM4	Info only	

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Feature	Options	Description
Console Redirection	Enabled **Disabled**	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. The item will be lunched before enable Console Redirection.
Legacy Console Redirection	Info only	
Legacy Console Redirection Settings	Submenu	Legacy Console Redirection Settings

7.3.9.1. Advanced > Serial Console Redirection > Console Redirection Settings

Feature	Options	Description
COM1~4 (dependent on which is enabled)	Info only	
Console Redirection Settings	Info only	
Teriminal Type	VT100 VT100+ VT-UTF8 **ANSI**	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7 **8**	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.They can be used as an additional data bit.
Stop Bits	**1** 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.

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Feature	Options	Description
VT-UTF8 Combo Key Support	**Enabled** Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Resolution 100x31	Enabled **Disabled**	On Legacy OS, the Number of Rows and Columns supported redirection
Legacy OS Redirection Resolution	**80x24** 80x25	On Legacy OS, the Number of Rows and Columns supported redirection
Putty KeyPad	**VT100** Intel Linux XTERMR6 SCO ESCN VT400	Select FunctionKey and KeyPad on Putty.
Redirection After BIOS POST	**Always Enable** BootLoader	When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always Enable.

7.3.9.2. Advanced > Serial Console Redirection > Legacy Console Redirection Settings

Feature	Options	Description
Legacy Serial Redirection Port	**COM1** COM2 COM3 COM4	Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages

7.3.10. Advanced > USB

Feature	Options	Description
USB	Info Only	
USB Module Version	Info Only	Display USB Module Version
USB Controllers:	Info Only	Display USB Controllers is XHCI or EHCI.
USB Devices:	Info Only	Display attatcment USB deviecs.
Legacy USB Support	**Enabled** Disabled Auto	Enables Legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices availiable only for EFI applications.
XHCI Hand-off	**Enabled** Disabled	This is a workaround for Oses without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	Disableed **Enabled**	Enable / Disable USB Mass Storge Driver Support.
USB hardware delays and time-outs:	Info Only	
USB transfer rime-out	1 sec 5sec 10sec **20 sec**	The time-out value for Control, Bulk, and Interrupt transfers.

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Feature	Options	Description
Device reset time-out	10 sec **20 sec** 30 sec 40 sec	USB mass storage device Start Unit command time-out.
Device power-up delay	**Auto** Manual	Maximum time the device will take before it properly reports itself to the Hot Controller. 'Auto' uses default value: for a Root po\rt it is 100 ms, for a Hub port the delay is taken form Hub descriptor.

7.3.11. Advanced > Network

Feature	Options	Description
Onboard LAN Controller	Disable **Enable**	Enable / Disable Onboard Intel I210LM Lan controller.
Network Stack	**Disable** Enable	Enable / Disable UEFI Network Stack.

7.3.12. Advanced > Miscellaneous

Feature	Options	Description
Miscellanous	Info Only	Control the PCI Express Root Port.
Smart Battery Function	**Disable** Enable	Enable / Disable Battery Function

7.3.13. Advanced > Driver Health

Feature	Options	Description
Driver Name	Info only	Provides Health Status for the Drivers / Controllers.

7.3.14. Advanced > Trusted Computing

Feature	Options	Description
TPM20 Device Found	Info Only	
Security Device Support	Disable **Enable**	Enables or Disable BIOS support for security device. OS will not show Security Device. TCG EFI protocol and available.
Active PCR banks	Info Only	
Available PCR banks	Info Only	
Pending operation	**None** TPM Clear	Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.
Platform hierarchy	Disable **Enable**	Enable or Disable Platform Hierarchy
Storage Hierarchy	Disable **Enable**	Enable or Disable Storage Hierarchy
Endorsement Hierarchy	Disable **Enable**	Enable or Disable Endorsement Hierarchy

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Feature	Options	Description
TPM2.0 UEFI Spec Version	TCG_1_2 **TCG_2**	Select the TCG2 Spec Version Support, TCG_1_2: the Compatible mode for Win8/Win10, TCG_2: Support new TCG2 protocol and event format for Win10 or later
Physical Presence Spec Version	**1.2** 1.3	Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.
TPM 20 Interface Type	Info only	
Device Select	TPM 1.2 **TPM 2.0** Auto	PM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated.

7.3.15. Advanced > Trusted Computing

Feature	Options	Description
SDIO Configuration	Info only	
SDIO Access Mode	**Auto** ADMA SDMA PIO	Auto Option: Access SD device in DMA mode if controller supports it,otherwise in PIO mode. DMA Option: Access SD device in DMA mode. PIO Option: Access SD device in PIO mode.

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7.4. Chipset

7.4.1. Chipset > North Bridge

Feature	Options	Description
Memory Information	Info only	
Total Memory	Info only	Display Total Memory Size.
Memory Vlotage	Info only	Display Memory Vlotage.
Memory Slot0	Info only	Display Installed Memory Slot0 Information.
Memory Slot1	Info only	Display Installed Memory Slot1 Information.
Max TOLUD	**2 GB** 2.25 GB 2.5 GB 2.75 GB 3 GB	Maximum Value of TOLUD.
Above 4GB MMIO BIOS assignment	Enabled **Disabled**	Enable/Disable above 4GB MemoryMappedIO BIOS assignemt. This is disabled automatically when Aperture Size is set to 2048MB.
PCIE VGA Workaround	Disable **Enable**	Enable it if your PCIe card cannot boot to DOS. This is for Test only.

7.4.2. Chipset > South Bridge

Feature	Options	Description
Serial IRQ Mode	Quiet **Continuous**	Configure Serial IRQ Mode.
SMBus Support	Disable **Enable**	Enable / Disable SMBus Support.
OS Selection	**Windows** Android Win7 Intel Linux	Select the target OS.
PCI CLOCK RUN	Disable **Enable**	Enables CLKRUN# logic to stop PCI clocks.
Real Time Option	RT Disabled RT Enabled, Agent IDI1 RT Enabled, Agent Disabled	Select Real-Time Enable and IDI Agenet Real-Time Traffic Mask Bits.

7.4.3. Chipset > Uncore Configuration

Feature	Options	Description
GOP Configuration	Info only	
Active LFP Config	**No LFP** eDP	Active Local Flat Panel Config.
LVDS Backlight Mode	GTT Mode **BMC Mode**	Select LVDS Backlight control function.

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Feature	Options	Description
DDI port 1	No Device Display Port HDMI **DisplayPort with HDMI/DVI Compatible**	DDI port 1 function choose to Display Port or HDMI.
LFP Panel Type	**Auto** 640x480 800x600 1024x768 1280x1024 1400x1050(RB) LVDS1 1400x1050 LVDS2 1600x1200 LVDS 1366x768 LVDS 1680x1050 1920x1200 1440x900 LVDS 1600x900 LVDS 1024x768 LVDS2 1280x800 1920x1080 LVDS 2048x1536 LVDS	Select LFP panel used by Internal Graphics Device by selecting the appropriate setup item.
GOP Brightness Level	20 40 60 80 100 120 **140** 160 180 200 220 240 255	Set GOP Brightness Level.
IGD Configuration	Info only	
Integerated Graphics Devices	Disable **Enable**	Enable: Enable Integrated Graphics Device (IGD) when selected as the Primary Video Adaptor. Disable: Always disable IGD.
Primary Display	**IGD** PCIe HG	Select which of IGD / PCI Graphics device should be Primary Display.
Aperture Size	128MB **256MB** 512MB	Select the Aperture Size.
DVMT Pre-Allocated	**64M** 96M 128M 160M 192M 224M 256M 288M 320M 352M 384M 416M 448M 480M 512M	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device

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Feature	Options	Description
DVMT Total Gfx Mem	128M **256M** MAX	Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device

7.4.4. Chipset > South Cluster Configuration

Feature	Options	Description
HD-Audio Configuration	Submenu	HD-Audio Configuration Setting.
PCI Express Configuration	Submenu	PCI Express Configuration Setting.
SATA Drives	Submenu	Press <Enter> to select the SATA Device Configuration Setup option.
SSC Configuration	Submenu	SSC Configuration Settings.
USB Configuration	Submenu	USB Configuration Settings.
Miscellaneous Configuration	Submenu	Enable / Disable Misc. Feature.

7.4.4.1. Chipset > South Cluster Configuration > HD-Audio Configuration

Feature	Options	Description
HD-Audio Configuration	Info only	
HD-Audio Support	Disable **Enable**	Select the target OS.

7.4.4.2. Chipset > South Cluster Configuration > PCI Express Configuration

Feature	Options	Description
PCI Express Configuration	Info only	
PCIE Port assigned to LAN	Info only	Display PCIE Port assigned to LAN Information.
Complicace Mode	**Disable** Enable	Complicace Mode Enable / Disable.
PCIE Port 1-4 Configuration >>Note: Default configuration for the lanes is 3x1.Other configurations (1x2,2x1 / 2x2 / 4x1) require a customized BIOS.<<	**3x1 Port**	To configure PCI-E Port 1-4 of PCH. [4X1]:Port 1-4 (x1) and Port 8 (x1) [1x2 2x1]:Port 1 (x2), Port 2 (disabled), Ports 3 and Port 4 (x1) [2x2]:Port 1-2 (x2) and Port 3-4 (x2) [1x4]:Port 1 (x4), Ports 2-4 (disabled)
PCI ExpressRoot Port 1	Submenu	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port Disable: Disable PCIe root port
PCI ExpressRoot Port 2	Submenu	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port Disable: Disable PCIe root port

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Feature	Options	Description
PCI ExpressRoot Port 3	Submenu	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port Disable: Disable PCIe root port

Chipset > South Cluster Configuration > PCI Express Configuration > PCI Express Root Port 1

Feature	Options	Description
PCI Express Root Port 1	Disable **Enable** Auto	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port. Disable: Disable PCIe root port.
ASPM	Disable **Enable**	PCI Express Active State Power Management settings
L1 Substates	Disable L1.1 L1.2 **L1.1 & L1.2**	PCI Express L1 Substates settings.
ACS	Disable **Enable**	Enable/Disable Access Control Services Extended Capability
URR	**Disable** Enable	CI Express Unsupported Request Reporting Enable/Disable
FER	**Disable** Enable	PCI Express Device Fatal Error Reporting Enable/Disable
NFER	**Disable** Enable	PCI Express Device Non-Fatal Error Reporting Enable/Disable
CER	**Disable** Enable	PCI Express Device Correctable Error Reporting Enable/Disable
CTO	**Default Setting** 16-15 ms 65-210 ms 260-900 ms 1-3.5 s Disable	PCI Express Completion Timer TO Enable/Disable.
SEFE	**Disable** Enable	Root PCI Express System Error on Fatal Error Enable/Disable
SENFE	**Disable** Enable	Root PCI Express System Error on Non-Fatal Error Enable/Disable
SECE	**Disable** Enable	Root PCI Express System Error on Correctable Error Enable/Disable
PME SCI	Disable **Enable**	PCI Express PME SCI Enable/Disable
Hot Plug	**Disable** Enable	PCI Express Hot Plug Enable/Disable
PCIe Speed	**Auto** Gen1 Gen2	Configure PCIe Speed
Transmitter Half Swing	**Disable** Enable	Transmitter Half Swing Enable/Disable.

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Feature	Options	Description
Extra Bus Reserved	**0**	Extra Bus Reserved (0-7) for bridges behind this Root Bridge
Reserved Memory	**10**	Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge
Reserved I/O	**4**	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge
PCH PCIe LTR Configuration	Info only	
PCH PCIE LTR	Disable **Enable**	PCH PCIE Latency Reporting Enable/Disable
Snoop Latency Override	Disabled Manual **Auto**	Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Non Snoop Latency Override	Disabled Manual **Auto**	Non Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow
PCIE LTR Lock	**Disable** Enable	PCIE LTR Configuration Lock
PCIe Selection De0emphasis	Disable **Enable**	When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. 1b -3.5 dB 0b -6 dB

Chipset > South Cluster Configuration > PCI Express Configuration > PCI Express Root Port 2

Feature	Options	Description
PCI Express Root Port 2	Disable **Enable** Auto	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port. Disable: Disable PCIe root port.
ASPM	Disable **Enable**	PCI Express Active State Power Management settings
L1 Substates	Disable L1.1 L1.2 **L1.1 & L1.2**	PCI Express L1 Substates settings.
ACS	Disable **Enable**	Enable/Disable Access Control Services Extended Capability
URR	**Disable** Enable	CI Express Unsupported Request Reporting Enable/Disable
FER	**Disable** Enable	PCI Express Device Fatal Error Reporting Enable/Disable
NFER	**Disable** Enable	PCI Express Device Non-Fatal Error Reporting Enable/Disable
CER	**Disable** Enable	PCI Express Device Correctable Error Reporting Enable/Disable

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Feature	Options	Description
CTO	**Default Setting** 16-15 ms 65-210 ms 260-900 ms 1-3.5 s Disable	PCI Express Completion Timer TO Enable/Disable.
SEFE	**Disable** Enable	Root PCI Express System Error on Fatal Error Enable/Disable
SENFE	**Disable** Enable	Root PCI Express System Error on Non-Fatal Error Enable/Disable
SECE	**Disable** Enable	Root PCI Express System Error on Correctable Error Enable/Disable
PME SCI	Disable **Enable**	PCI Express PME SCI Enable/Disable
Hot Plug	**Disable** Enable	PCI Express Hot Plug Enable/Disable
PCIe Speed	**Auto** Gen1 Gen2	Configure PCIe Speed
Transmitter Half Swing	**Disable** Enable	Transmitter Half Swing Enable/Disable.
Extra Bus Reserved	**0**	Extra Bus Reserved (0-7) for bridges behind this Root Bridge
Reserved Memory	**10**	Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge
Reserved I/O	**4**	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge
PCH PCIe LTR Configuration	Info only	
PCH PCIE LTR	Disable **Enable**	PCH PCIE Latency Reporting Enable/Disable
Snoop Latency Override	Disabled Manual **Auto**	Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Non Snoop Latency Override	Disabled Manual **Auto**	Non Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow
PCIE LTR Lock	**Disable** Enable	PCIE LTR Configuration Lock
PCIe Selection De0emphasis	Disable **Enable**	When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. 1b -3.5 dB 0b -6 dB

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Chipset > South Cluster Configuration > PCI Express Configuration > PCI Express Root Port 3

Feature	Options	Description
PCI Express Root Port 3	Disable **Enable** Auto	Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port. Disable: Disable PCIe root port.
ASPM	Disable **Enable**	PCI Express Active State Power Management settings
L1 Substates	Disable L1.1 L1.2 **L1.1 & L1.2**	PCI Express L1 Substates settings.
ACS	Disable **Enable**	Enable/Disable Access Control Services Extended Capability
URR	**Disable** Enable	CI Express Unsupported Request Reporting Enable/Disable
FER	**Disable** Enable	PCI Express Device Fatal Error Reporting Enable/Disable
NFER	**Disable** Enable	PCI Express Device Non-Fatal Error Reporting Enable/Disable
CER	**Disable** Enable	PCI Express Device Correctable Error Reporting Enable/Disable
CTO	**Default Setting** 16-15 ms 65-210 ms 260-900 ms 1-3.5 s Disable	PCI Express Completion Timer TO Enable/Disable.
SEFE	**Disable** Enable	Root PCI Express System Error on Fatal Error Enable/Disable
SENFE	**Disable** Enable	Root PCI Express System Error on Non-Fatal Error Enable/Disable
SECE	**Disable** Enable	Root PCI Express System Error on Correctable Error Enable/Disable
PME SCI	Disable **Enable**	PCI Express PME SCI Enable/Disable
Hot Plug	**Disable** Enable	PCI Express Hot Plug Enable/Disable
PCIe Speed	**Auto** Gen1 Gen2	Configure PCIe Speed
Transmitter Half Swing	**Disable** Enable	Transmitter Half Swing Enable/Disable.
Extra Bus Reserved	**0**	Extra Bus Reserved (0-7) for bridges behind this Root Bridge
Reserved Memory	**10**	Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge
Reserved I/O	**4**	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge

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Feature	Options	Description
PCH PCIe LTR Configuration	Info only	
PCH PCIE LTR	Disable **Enable**	PCH PCIE Latency Reporting Enable/Disable
Snoop Latency Override	Disabled Manual **Auto**	Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Non Snoop Latency Override	Disabled Manual **Auto**	Non Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow
PCIE LTR Lock	**Disable** Enable	PCIE LTR Configuration Lock
PCIe Selection De0emphasis	Disable **Enable**	When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. 1b -3.5 dB 0b -6 dB

7.4.4.3. Chipset > South Cluster Configuration > SATA Drives

Feature	Options	Description
SATA Drives	Info only	
Chipset- SATA Controller Configuration	Info only	
Chipset SATA	Disable **Enable**	Enables or Disables the Chipset SATA Controller. The Chipset SATA controller supports the 2 black internal SATA ports (up to 3Gb/s supported per port).
SATA Mode Selection	**AHCI**	Determines how SATA controller(s) operate.
SATA Interface Speed	Gen1 **Gen2** Gen3	Select SATA Interface Speed, CHV A1 always with Gen Speed.
SATA Test Mode	**Disabled** Enabled	Test Mode Enable / Disable.
Aggressive LPM Support	**Disabled** Enabled	Enable PCH to Aggressively enter link power state.
SATA0	Info only	
Software Preserve	Info only	
Port 0	Disabled **Enabled**	Enable / Disable SATA Port
SATA Port 0 Hot Plug Capability	**Disabled** Enabled	If enabled, SATA port will be reported as Hot Plug capable.
Configured as eSATA	Info only	Display Configured as eSATA support.
Mechanical Presence Switch	Disabled **Enabled**	Controls reporting if this port has a Mechanical Presence Switch. Note. Request Hardware support.

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Feature	Options	Description
Spin Up Device	**Disabled** Enabled	If enabled for any of ports Staggerred Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
SATA Device Type	**Hard Disk Drive** Solid State Drive	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.
SATA Port 0 DevSlp	**Disabled** Enabled	Enable/Disable SATA Port 0 DevSlp. Board rework for LP needed before enable.
DITO Configuration	**Disabled** Enabled	Enable/Disable DITO Configuration
DITO Value	**625**	DITO Value. Note. DITO Value can be accessed if DITO Configuration item must enable.
DM Value	**15**	DM Value. Note. DM Value can be accessed if DITO Configuration item must enable.
SATA1	Info only	
Software Preserve	Info only	
Port 1	Disabled **Enabled**	Enable / Disable SATA Port
SATA Port 1 Hot Plug Capability	**Disabled** Enabled	If enabled, SATA port will be reported as Hot Plug capable.
Configured as eSATA	Info only	Display Configured as eSATA support.
Mechanical Presence Switch	Disabled **Enabled**	Controls reporting if this port has a Mechanical Presence Switch. Note. Request Hardware support.
Spin Up Device	**Disabled** Enabled	If enabled for any of ports Staggerred Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
SATA Device Type	**Hard Disk Drive** Solid State Drive	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.
SATA Port 1 DevSlp	**Disabled** Enabled	Enable/Disable SATA Port 1 DevSlp. Board rework for LP needed before enable.
DITO Configuration	**Disabled** Enabled	Enable/Disable DITO Configuration
DITO Value	**625**	DITO Value. Note. DITO Value can be accessed if DITO Configuration item must enable.
DM Value	**15**	DM Value. Note. DM Value can be accessed if DITO Configuration item must enable.

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7.4.4.4. Chipset > South Cluster Configuration > SSC Configuration

Feature	Options	Description
SSC SD Card Support (D27:F0)	Disabled **Enabled**	Enable / Disable SCC SD Card Support.
SCC eMMC Support (D28:F0)	Disabled **Enabled**	Enable / Disable SCC eMMC Support.
eMMC Max Speed	**HS400** HS200 DDR50	Select the eMMC max Speed allowed.
SCC UFS Support (D29:F0)	**Disabled** Enabled	Enable / Disable UFS SDIO Support.
SCC SDIO Support (D30:F0)	**Disabled** Enabled	Enable / Disable SCC SDIO Support.
~~SDIO/GPIO~~	~~**GPIO MODE**~~ ~~SDIO MODE~~	~~Select SDIO or GPIO function.~~

7.4.4.5. Chipset > South Cluster Configuration > USB Configuration

Feature	Options	Description
XHCI Pre-Boot Driver	**Disabled** Enabled	Enable / Disable XHCI Pre-Boot Driver support.
XHCI Mode	Disabled **Enabled**	Once disabled, XHCI controller would be function disabled, none of the USB devices are detectable and usable during boot and in OS. Do not disable it unless for debug purpose.
USB Port Disable Override	**Disabled** Enabled	Selectively Enable/Disable the corresponding USB port from reporting a Device Connection to the controller.
XDCI Support	**Disabled** PCI Mode	Enable/Disable XDCI
XHCI Disable Compliance Mode	**FALSE** TRUE	Option to disable XHCI Link Compliance Mode. Default is FALSE to not disable Compliance Mode. Set TRUE to disable Complicance Mode.
USB HW MODE AFE Comparators	**Disabled** Enabled	Enable/Disable USB HW MODE AFE Comparators
USB OTG Support	**Disabled** Enabled	Enable/Disable USB OTG Support

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7.4.4.6. Chipset > South Cluster Configuration > Miscellaneous Configuration

Feature	Options	Description
Miscellaneous Configuration	Info only	
State After G3	**S0 State** S5 State Last State	Specify what state to go to when power is re-applied after a power failure (G3 state). S0 State: System will boot directly as soon as power applied. S5 State: System keeps in power-off state until power button is pressed.
Wake On Lan	**Disabled** Enabled	Enable or Disable the Wake on Lan.

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7.5. Security

7.5.1. Security > Password Description

Feature	Options	Description
Password Description	Info only	
Setup Administrator Password	Enter Password	Set Setup Administrator Password
User Password	Enter Password	Set User Password
Secure Boot	Submenu	Customizable Secure Boot settings.
System Mode	Info only	
Secure Boot	Info only	
Attempt Secure Control	Disabled **Enabled**	Secure Boot activated when Platform Key(PK) is enrolled, System mode is User / Deployed, and CSM function is disabled

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7.6. Boot

7.6.1. Boot > Boot Configuration

Feature	Options	Description
Boot Configuration	Info only	
Setup Prompt Timeout	**1**	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
Bootup NumLock State	**On** Off	Select the keyboard Number state.
Ouiet Boot	Disabled **Enabled**	Select the keyboard NumLock state.
Fast Boot	**Disabled** Enabled	Enable or Disable FastBoot features. Most probes are skipped to reduce time cost during boot.
New Boot Option Policy	**Default** Place First Place Last	Controls the placement of newly detected UEFI boot option.
Boot mode select	Legacy **UEFI**	Select boot mode LEGACY/UEFI

7.6.2. Boot > FIXED BOOT ORDER Priorities

Feature	Options	Description
Boot Option #1	Hardware	Set the system boot order.
Boot Option #2	CD/DVD	Set the system boot order.
Boot Option #3	USB Hard Disk	Set the system boot order.
Boot Option #4	USB CD/DVD	Set the system boot order.
Boot Option #5	USB Key	Set the system boot order.
Boot Option #6	USB Floppy	Set the system boot order.
Boot Option #7	USB Lan	Set the system boot order.
Boot Option #8	Network	Set the system boot order.

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7.7. Save & Exit

Feature	Options	Description
Save Changes and Exit		Exit system setup after saving the changes.
Discard Changes and Exit		Exit system setup without saving any changes.
Save Change and Reset		Reset the system after saving the changes.
Discard Changes and Reset		Reset system setup without saving any changes.
Save Options	Info only	
Save Changes		Save Changes done so far to any of the setup options.
Discard Change		Discard Changes fone so far to any of the setup options.
Restore Defaults		Restore/Load Default values for all the setup options.
Save as User Defaults		Save the changes done so far as User Defaults.
Restore User Defaults		Restore the User Defaults to all the setup options.
Boot Override	Info only	

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8. BIOS Checkpoints, Beep Codes

This section of this document lists checkpoints and beep codes generated by AMI Aptio BIOS. The checkpoints defined in this document are inherent to the AMIBIOS generic core, and do not include any chipset or board specific checkpoint definitions.

Checkpoints and Beep Codes Definition

A checkpoint is either a byte or word value output to I/O port 80h. The BIOS outputs checkpoints throughout bootblock and Power-On Self Test (POST) to indicate the task the system is currently executing. Checkpoints are very useful for debugging problems that occur during the preboot process.

Beep codes are used by the BIOS to indicate a serious or fatal error. They are used when an error occurs before the system video has been initialized, and generated by the system board speaker.

Aptio Boot Flow

While performing the functions of the traditional BIOS, Aptio 5.x core follows the firmware model described by the Intel Platform Innovation Framework for EFI (“the Framework”). The Framework refers the following “boot phases”, which may apply to various status code & checkpoint descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization[1]
- Driver Execution Environment (DXE) – main hardware initialization[2]
- Boot Device Selection (BDS) – system setup, pre-OS user interface & selecting a bootable device (CD/DVD, HDD, USB, Network, Shell, …)

Viewing BIOS Checkpoints

Viewing all checkpoints generated by the BIOS requires a checkpoint card, also referred to as a □OST Card or POST Diagnostic Card. These are PCI add-in cards that show the value of I/O port 80h on a LED display.

Some computers display checkpoints in the bottom right corner of the screen during POST. This display method is limited, since it only displays checkpoints that occur after the video card has been activated.

Keep in mind that not all computers using AMI Aptio BIOS enable this feature. In most cases, a checkpoint card is the best tool for viewing AMI Aptio BIOS checkpoints.

[1]Analogous to “bootblock” functionality of legacy BIOS
[2]Analogous to “POST” functionality in legacy BIOS

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8.1. Status Code Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

8.2. Standard Status Codes

8.2.1. SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization

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SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

8.2.2. SEC Beep Codes

None

8.2.3. PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization

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Status Code	Description
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes

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Status Code	Description
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

8.2.4. PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

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8.2.5. DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration

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Status Code	Description
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)

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Status Code	Description
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

8.2.6. DXE Beep Codes

# of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

‘’

8.2.7. ACPI/ASL Checkpoint

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state

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Status Code	Description
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

8.3. OEM-Reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

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9. Mechanical Information

9.1. Board-to-Board Connectors

To allow for different stacking heights, the receptacles for COM Express carrier boards are available in two heights: 5 mm and 8 mm. When 5 mm receptacles are chosen, the carrier board should be free of components.

Tyco 3-1827253-6

Foxconn QT002206-2131-3H

- 220-pin board-to-board connector with 0.5mm for a stacking height of 5 mm.
- This connector can be used with 5 mm through-hole standoffs (SMT type).



Tyco 3-6318491-6

Foxconn QT002206-4141-3H

- 220-pin board-to-board connector with 0.5mm for a stacking height of 8 mm.
- This connector can be used with 8 mm through-hole standoffs (SMT type).



Common Specifications

- Current capacity: 0.5A per pin
- Rated voltage: 50 VAC
- Insulation resistance: 100M or greater @ 500 VDC
- Temperature rating: -40°C ~ 85°C
- UL certification (ECBT2.E28476)
- Copper alloy (contacts)
- Housing: thermo-plastic molded compound (L.C.P.)

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9.2. Thermal Solution

9.2.1. Heat Spreaders

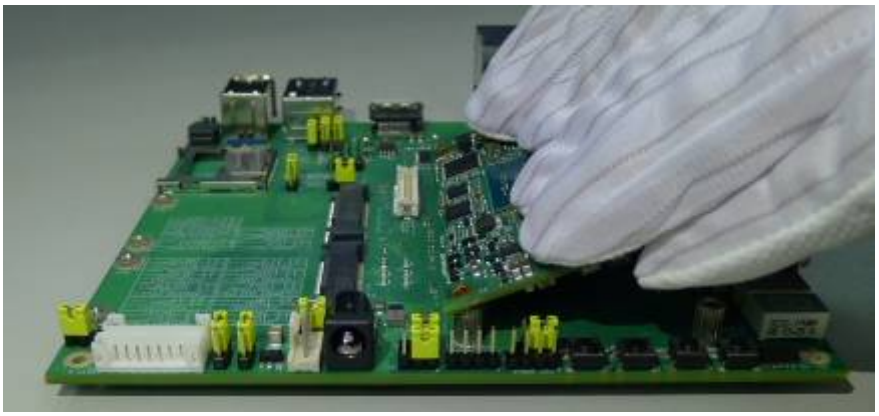
The function of the heat spreader is to ensure an identical mechanical profile for all COM Express modules. By using a heat spreader, the thermal solution that is built on top of the module is compatible with all COM Express modules.

9.2.2. Heat Sinks

A heat sink can be used as a thermal solution for a specific COM Express module and can have a fan or be fanless, depending on the thermal requirements.

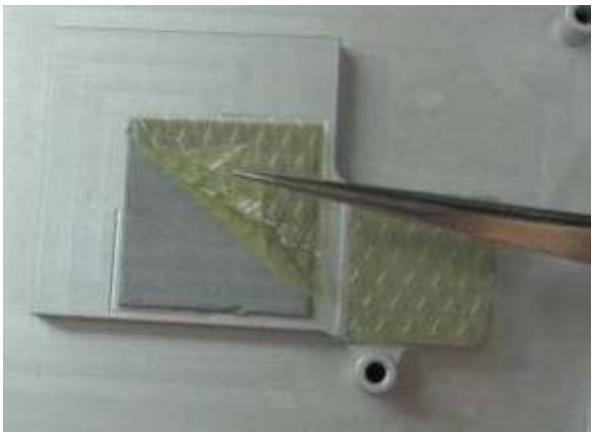
9.2.3. Installation

Step 1: Place the COM Express module onto the connectors on the carrier board as shown.



Then press down on the module until it is firmly seated on the carrier board.

Step 2: Remove the protective membranes from the thermal pads.

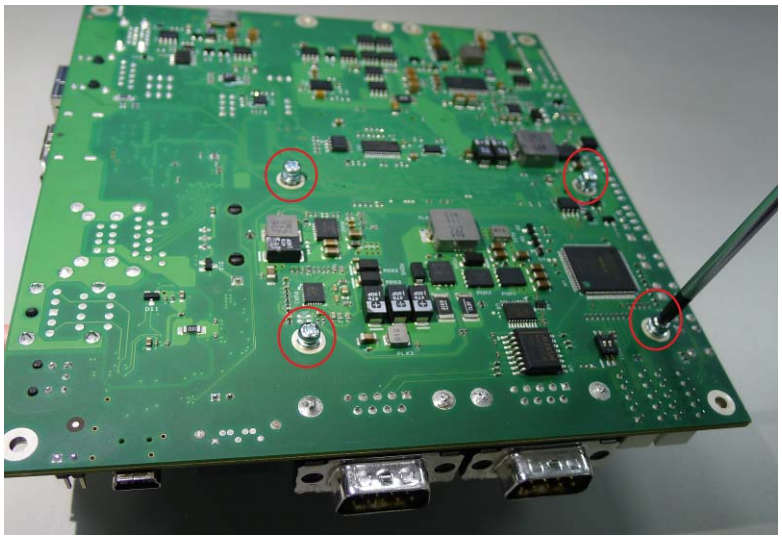


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Step 3: Put heatsink on the COM Express module and assemble the heatsink onto the COM Express module.



Use the four M2.5, L=6mm screws provided to fasten the heatsink to the module.



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9.3. Mounting Methods

There are several standard ways to mount the COM Express module with a thermal solution onto a carrier board. In addition to the choice of 5 mm or 8mm board-to-board connectors, there is the choice of Top and Bottom mounting. In Top mounting, the threaded standoffs are on the carrier board and the thermal solution is equipped with through-hole standoffs. In Bottom mounting, the threaded standoffs are on the thermal solution and the carrier board has through-hole standoffs.

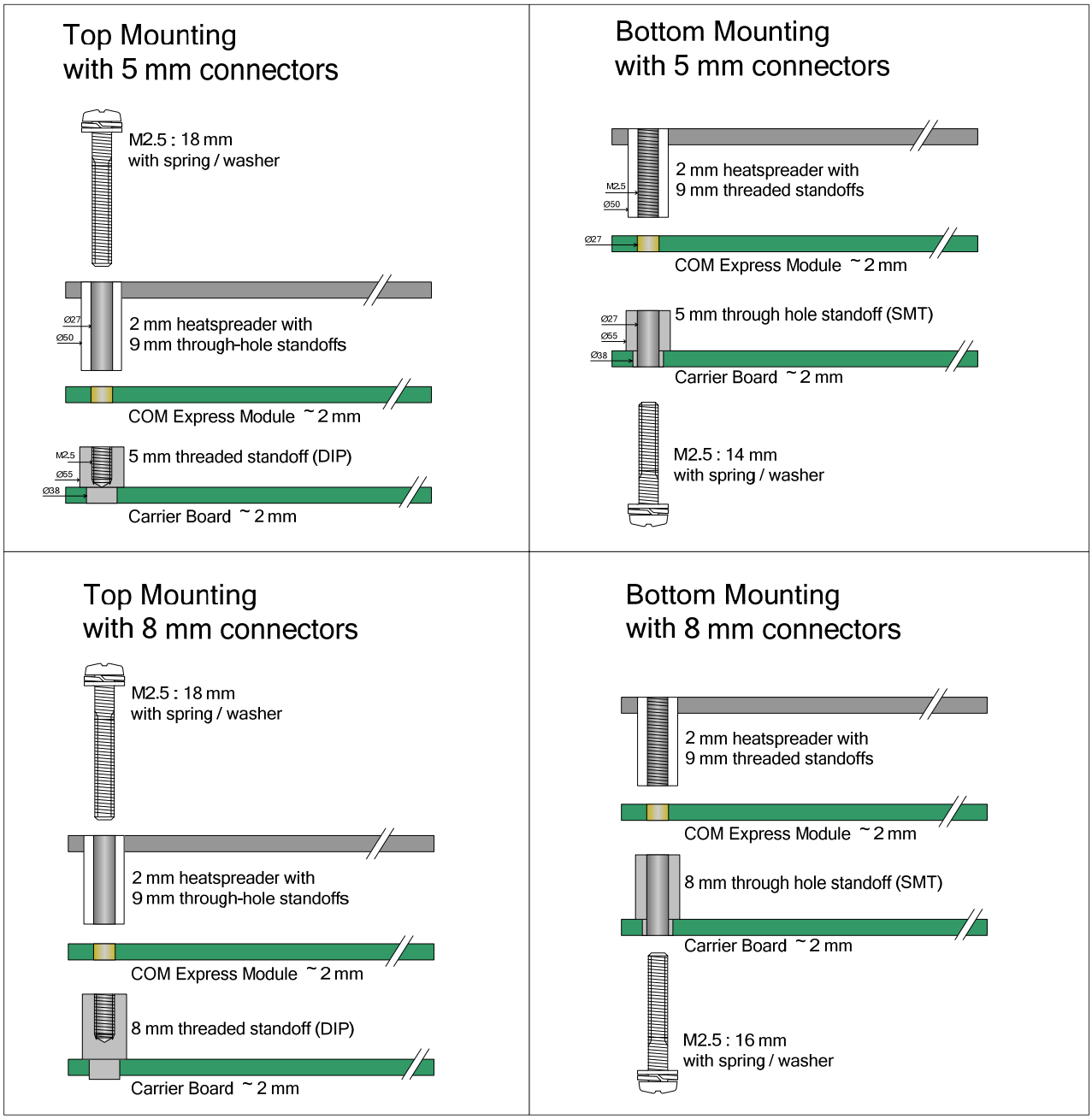


Figure 6: COM Express Mounting Methods

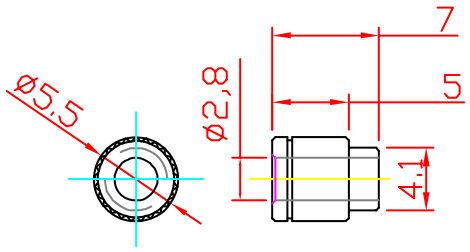
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9.4. Standoff Types

The standoffs available for Top and Bottom mounting methods are shown below. Note that threaded standoffs are DIP type and through-hole standoffs are SMT type. Other types not listed are available upon request.

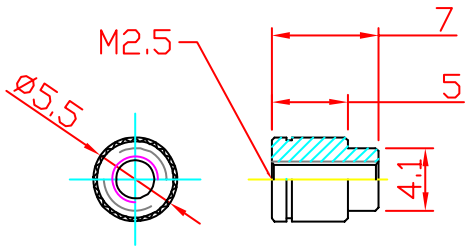
5mm through-hole standoff (SMT type)

P/N: 33-72000-0050



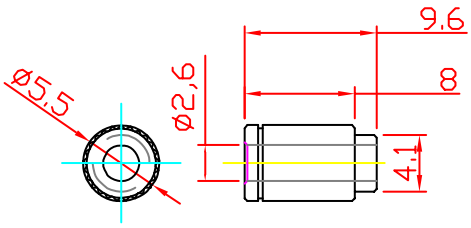
5mm threaded standoff (DIP type)

P/N: 33-72016-0050



8mm through-hole standoff (SMT type)

P/N: 33-72000-0080



8mm threaded standoff (DIP type)

P/N: 33-72015-0050

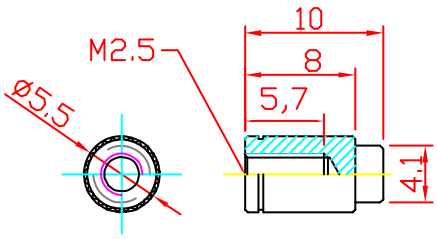


Figure 7: COM Express Standoff Types

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Safety Instructions

Read and follow all instructions marked on the product and in the documentation before you operate your system. Retain all safety and operating instructions for future use.

- Please read these safety instructions carefully.
- Please keep this User‘s Manual for later reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment, turn off the power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources.
  - Keep equipment away from high heat or high humidity.
  - Keep equipment properly ventilated (do not block or cover ventilation openings).
  - Make sure to use recommended voltage and power source settings.
  - Always install and operate equipment near an easily accessible electrical socket-outlet.
  - Secure the power cord (do not place any object on/over the power cord).
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings.
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.
- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

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Getting Service

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