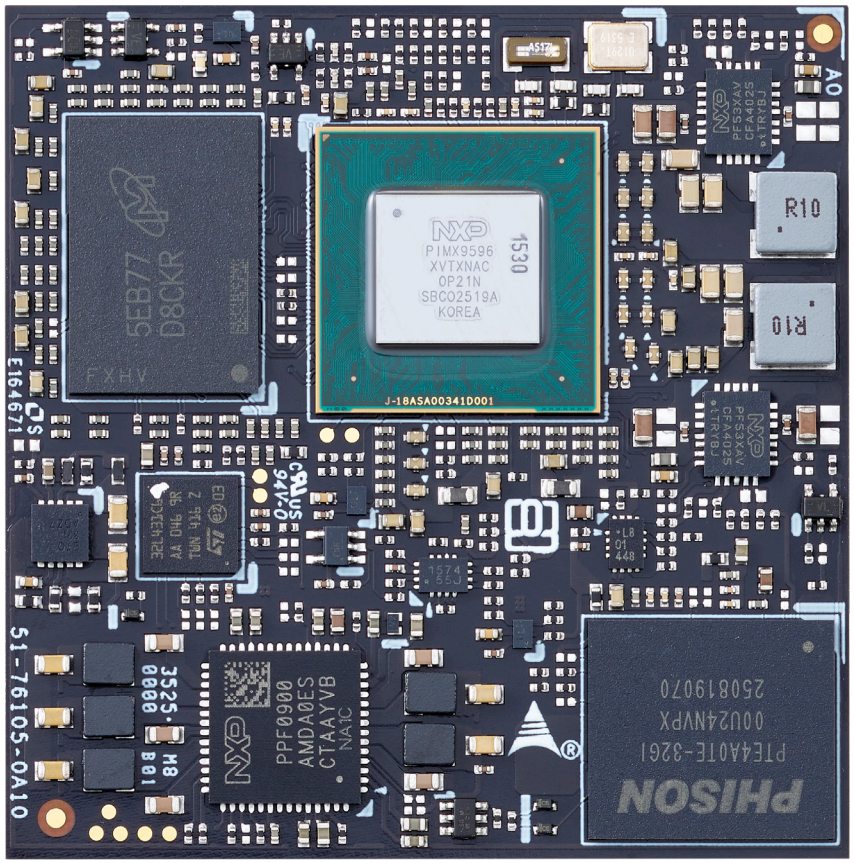
OSM-IMX95

User's Guide



OPEN STANDARD MODULE™

Revision:	1.1
Date:	2026-02-12
Part Number:	50M-76105-1010

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Revision History

Revision	Description	Date	Author
1.0	Initial release	2026-01-05	AL
1.1	Module feature list and specifications updated	2026-02-12	AL

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Preface

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Safety Instructions

For user safety, please read and follow all Instructions, **WARNING**s, **CAUTION**s, and **NOTE**s marked in this manual and on the associated equipment before handling/operating the equipment.

Read these safety instructions carefully.

- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

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Conventions

The following conventions may be used throughout this manual, denoting special levels of information.



Note: This information adds clarity or specifics to text and illustrations.



Caution: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.



Warning: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

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1. Introduction

1.1. The OSM Form Factor

The OSM ("Open Standard Module")™ specification enables the development, production, and distribution of embedded modules for the most popular MCU32, ARM, and x86 architectures. For a growing number of IoT applications, this standard helps combine the advantages of modular embedded computing with increasing requirements regarding cost, space, and interfaces.

The modules are used as building blocks for portable and stationary embedded systems. They integrate the core CPU and supporting circuits, including DRAM, boot flash, power-sequencing logic, and CPU power supplies. The modules are paired with application-specific carrier boards that implement additional features such as audio CODECs, touch controllers, wireless devices, PHYs, etc. This modular approach allows scalability, fast time-to-market, and upgradability while maintaining low cost, low power consumption, and a small physical footprint.

Note: This module is compliant with the SGET OSM 1.2 specification.

SGET STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

OSM module and carrier specifications are available online at: https://sget.org/standards/osm/

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1.2. Module Feature List

Memory: LPDDR4 2 to 8 GB

eMMC: BGA 32 to 256 GB

LAN: Dual Gbe with built-in MAC and Precision Time Protocol (PTP)

Graphics: Mali-G310 rendering engine

USB: 1x USB 2.0 OTG, 1x USB 3.0 (all from SoC)

AUDIO: I^2S to carrier

CAN: dual CAN-FD

PCIe: single lane Gen 3

Industrial interfaces: SPI/I^2C/I^2S/UART/GPIO

SECURITY: NXP ARM TrustZone with safety island (Cortex M33)

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2. Specifications

2.1. Core System

CPU
4 cores or 6 cores ARM Cortex-A55
eIQ Neutron NPU

The ARM Cortex-A55 processors deliver high performance while being optimized for low power consumption.

Memory
LPDDR4, solder-down, single-chip, up to 8 GB
32-bit DRAM interface

Cache
Per core: >32 KB I-cache, 32 KB D-cache, 64 KB L2 cache
Unified: >512 KB L3 cache

Security
Arm® TrustZone
Cryptography engine
Tamper detection
Secure clock
Secure boot
eFuse key storage
Random number generator

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2.2. Video

2.2.1 GPU

GPU Core
Mali G310

Graphics Feature Support
3D GPU supporting 50 GFLOPs
OpenGL®ES 3.2
Vulkan ®1.2
OpenCL 3.0

VPU Feature Support
•4Kp30 H.265 and H.264 encode and decode
•1× JPEG encoder
•1× JPEG decoder

2.2.2 Display Interface Support

MIPI DSI
1x MIPI DSI 4 lane compliant to MIPI-DSI standard v1.2
Maximum resolution 4Kp30

LVDS
Dual-channel LVDS, maximum resolution 1080p60

2.3. Camera

One 4-lane MIPI CSI2 camera input

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2.4. Audio

I^2S to carrier

2.5. Dual Wired Ethernet

Primary LAN
MAC 10/100/1000 TSN Ethernet controller on SoC
Supports 10/100/1000 Mbps data transfer rates, both full-duplex and half-duplex

Secondary LAN
MAC 10/100/1000 TSN Ethernet controller on SoC
Supports 10/100/1000 Mbps data transfer rates, both full-duplex and half-duplex

2.6. Expansion Buses

PCIe
1× single-lane, Rev 3.0

USB
1× USB 2.0, 1× USB 3.0 (OTG on USB 2.0 interface)

UART
4 UART interfaces

CANbus
CAN0, CAN1
Supports CAN 2.0B only, or mixed CAN 2.0B and CAN FD mode
Data bit rate up to 8 Mbps

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SPI

3× SPI interfaces

I2S

2× I2S interface with audio resolution from 16 to 32 bits and sample rate up to 192 kHz (see Audio Codec support)

I2C

2 I2C interfaces
Supports 7-bit addressing mode
Software-programmable clock frequency: 100 kbit/s in Standard-mode, 400 kbit/s in Fast-mode, or 1 Mbit/s in Fast-mode Plus

GPIO

14x GPIO with interrupt

2.7. System Storage

SDIO

2x SDIO (4-bit) compatible with SD3.0

eMMC

32 GB to 256 GB (build option)

Compatible with eMMC specifications 4.41, 4.51, 5.0, and 5.1

2.8. Power

Power Modes: ON / OFF / SUSPEND

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Power on / off behavior same as x86	ATX (hold off boot until PWRBTN) / AT (always boot)
Voltage Input:	5.0V +/- 5%

Operating Temperatures (vs power input)

Standard Operating Temperature:	0 to 60°C -commercial grade BOM (memory, eMMC, USB hub, SOC)
Extreme Rugged Operating Temperature:	-40 to 85°C-industrial grade BOM (memory, eMMC, USB hub, SOC)

2.9. Mechanical and Environmental

Environmental Humidity

5-90% RH operating, non-condensing

5-95% RH storage (and operating with conformal coating)

EMI

EN55022 Class B inside an enclosure

Shock and Vibration

HALT Testing, including test report confirming the extended operating temperature range during and after vibration. A separate shock test report in accordance with MIL-STD-202F, Method 213B, Table 213-I, Condition A.

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IN ADDITION: When installed on a baseboard, the device shall operate under 18 sawtooth mechanical shocks
(3 shocks in each direction) with a peak acceleration of 40g for a duration of 18 ms each, and 75g for a duration of 6 ms each.

Capable of supporting random vibration: MIL-STD-202F, Method 214A, Table 214-I, Condition D. If HALT testing shows equal or better performance, a separate vibration test report is not necessary.

MTBF

300,000 hrs. (at 40 C), 100,000 hrs. (at 85°C)

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3. Block Diagram

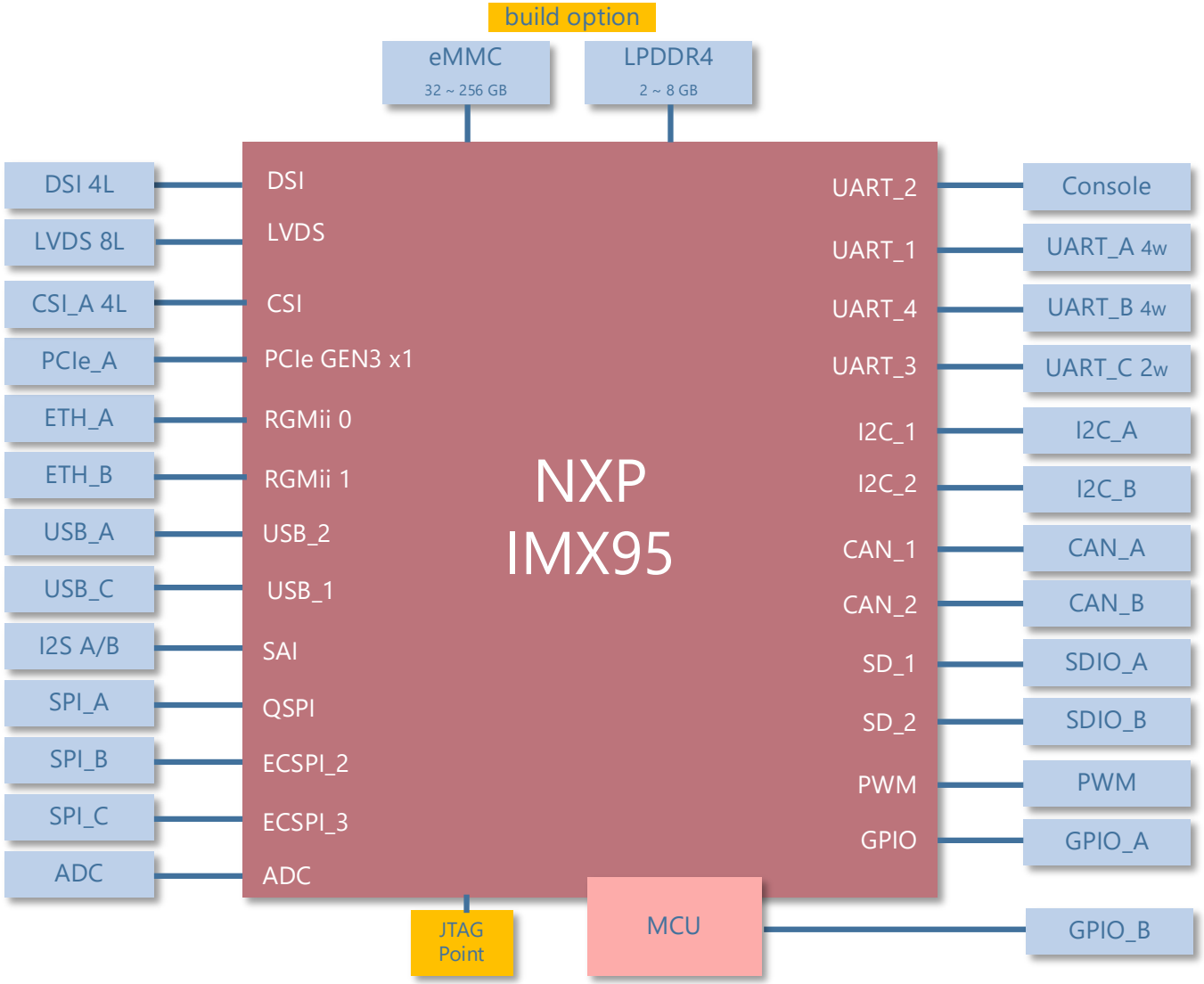


Figure 1 – Module function diagram

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4. Pinout and Signal Descriptions

4.1. Pin Summary

- Size-0 – "Zero": 30 mm x 15 mm
- Size-S – "Small": 30 mm x 30 mm
- Size-M – "Medium": 30 mm x 45 mm
- Size-L – "Large": 45 mm x 45 mm

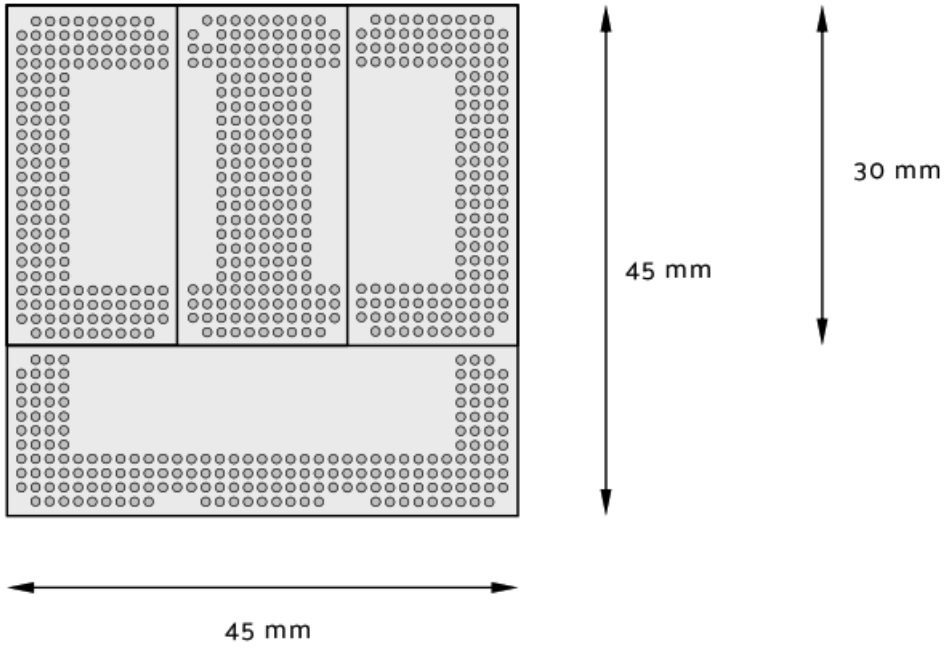


Figure 2 – Module size grid

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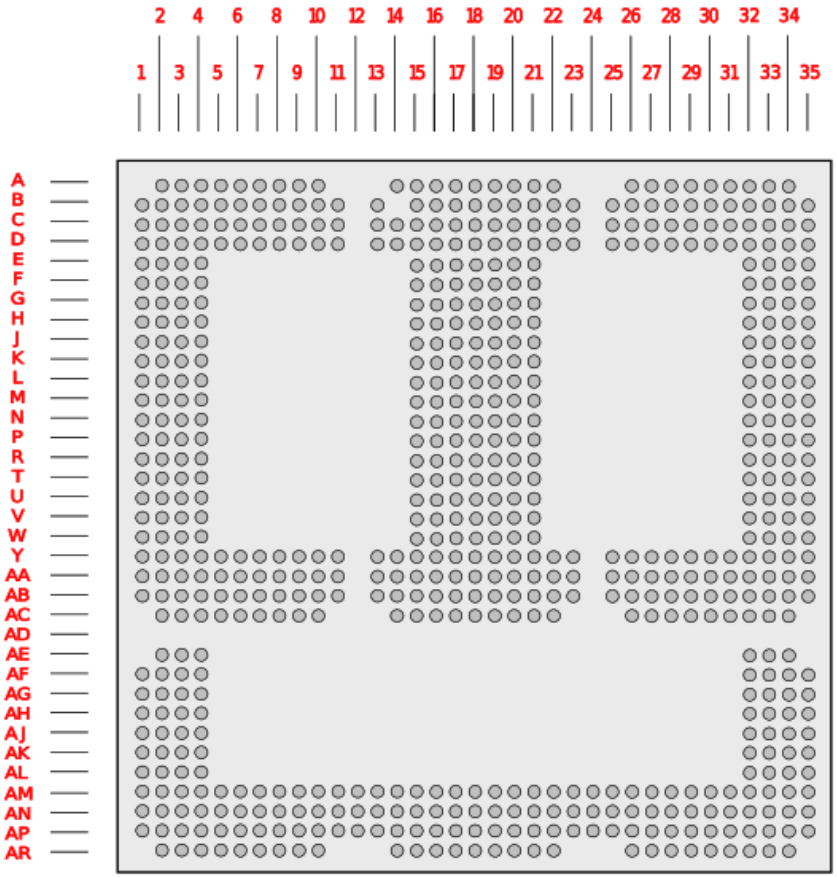


Figure 3 – Module pinout grid

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4.2. Signal Terminology Descriptions

The following information provides descriptions of the terms used in the signal description table:

Term	Description
I	Input to the Module
O	Output from the Module
I/O	Bi-directional input/output
OD	Open drain
PU	PU (pull-up) resistor
PD	PD (pull-down) resistor
CMOS	Logic input or output
GBE MDI	Differential analogue signaling for gigabit media dependent interface
DP	Low voltage differential signal for DisplayPort interface
D-PHY	Low voltage differential signal for MIPI CSI-2 cameras and DSI displays
M-PHY	Low voltage differential signal for MIPI CSI-3 cameras
LVDS	Low voltage differential signal for LCD displays
PCIE	Low voltage differential signal for PCIe
SATA	Low voltage differential signal for SATA
TMDS HDMI	Transition minimized differential signal for HDMI displays
USB	DC coupled differential signaling for traditional (non-Superspeed) USB signals
USB SS	Differential signal for SuperSpeed USB signals
USB VBUS 5V	5V tolerant input for USB VBUS detection
VDD_IN	Main power source from Carrier to Module
3.3V	3.3V power domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
1.8V	1.8V power domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
3.3Vsb	3.3V standby power domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)
1.8Vsb	1.8V standby power domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)
Sleep	Module is in its lowest power state
Runtime	Module is full on. CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
Standby	Module is in standby state or higher

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4.3. Signal Description by Function

4.3.1 LVDS Display Interface

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name
LVDS_BL_EN	AN23	O CMOS	1.8V		LVDS0_BKLT_EN_1V8	MCU(STM32L431RCI6)	F7
LVDS_A_CLK_P	AN13	O LVDS LCD			LVDS0_CLK_P	i.MX95	LVDS0_CLK_P
LVDS_A_CLK_N	AN12	O LVDS LCD			LVDS0_CLK_N	i.MX95	LVDS0_CLK_N
LVDS_A_LANE0_P	AP18	O LVDS LCD			LVDS0_D0_P	i.MX95	LVDS0_D0_P
LVDS_A_LANE0_N	AP17	O LVDS LCD			LVDS0_D0_N	i.MX95	LVDS0_D0_N
LVDS_A_LANE1_P	AR16	O LVDS LCD			LVDS0_D1_P	i.MX95	LVDS0_D1_P
LVDS_A_LANE1_N	AR15	O LVDS LCD			LVDS0_D1_N	i.MX95	LVDS0_D1_N
LVDS_A_LANE2_P	AP15	O LVDS LCD			LVDS0_D2_P	i.MX95	LVDS0_D2_P
LVDS_A_LANE2_N	AP14	O LVDS LCD			LVDS0_D2_N	i.MX95	LVDS0_D2_N
LVDS_A_LANE3_P	AP12	O LVDS LCD			LVDS0_D3_P	i.MX95	LVDS0_D3_P
LVDS_A_LANE3_N	AP11	O LVDS LCD			LVDS0_D3_N	i.MX95	LVDS0_D3_N
LVDS_B_CLK_P	AN17	O LVDS LCD			LVDS1_CLK_P	i.MX95	LVDS1_CLK_P
LVDS_B_CLK_N	AN16	O LVDS LCD			LVDS1_CLK_N	i.MX95	LVDS1_CLK_N
LVDS_B_LANE0_P	AM21	O LVDS LCD			LVDS1_D0_P	i.MX95	LVDS1_D0_P
LVDS_B_LANE0_N	AM20	O LVDS LCD			LVDS1_D0_N	i.MX95	LVDS1_D0_N
LVDS_B_LANE1_P	AN20	O LVDS LCD			LVDS1_D1_P	i.MX95	LVDS1_D1_P
LVDS_B_LANE1_N	AN19	O LVDS LCD			LVDS1_D1_N	i.MX95	LVDS1_D1_N
LVDS_B_LANE2_P	AM18	O LVDS LCD			LVDS1_D2_P	i.MX95	LVDS1_D2_P
LVDS_B_LANE2_N	AM17	O LVDS LCD			LVDS1_D2_N	i.MX95	LVDS1_D2_N
LVDS_B_LANE3_P	AM15	O LVDS LCD			LVDS1_D3_P	i.MX95	LVDS1_D3_P
LVDS_B_LANE3_N	AM14	O LVDS LCD			LVDS1_D3_N	i.MX95	LVDS1_D3_N

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4.3.1.1. DSI0 Mode

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name
DSI_DATA0_N	AB11	O LVDS D-PHY			DSI_D0_N	i.MX95	MIPI_DSICSI1_D0_N
DSI_DATA0_P	AB10	O LVDS D-PHY			DSI_D0_P	i.MX95	MIPI_DSICSI1_D0_P
DSI_DATA1_N	AC9	O LVDS D-PHY			DSI_D1_N	i.MX95	MIPI_DSICSI1_D1_N
DSI_DATA1_P	AC8	O LVDS D-PHY			DSI_D1_P	i.MX95	MIPI_DSICSI1_D1_P
DSI_DATA2_N	AC6	O LVDS D-PHY			DSI_D2_N	i.MX95	MIPI_DSICSI1_D2_N
DSI_DATA2_P	AC5	O LVDS D-PHY			DSI_D2_P	i.MX95	MIPI_DSICSI1_D2_P
DSI_DATA3_N	AB5	O LVDS D-PHY			DSI_D3_N	i.MX95	MIPI_DSICSI1_D3_N
DSI_DATA3_P	AB4	O LVDS D-PHY			DSI_D3_P	i.MX95	MIPI_DSICSI1_D3_P
DSI_CLOCK_N	AB8	O LVDS D-PHY			DSI_CLK_N	i.MX95	MIPI_DSICSI1_CLK_N
DSI_CLOCK_P	AB7	O LVDS D-PHY			DSI_CLK_P	i.MX95	MIPI_DSICSI1_CLK_P
DSI_TE	AA3	I CMOS	1.8V		DSI_TE	i.MX95	GPIO_IO13

4.3.1.2. eDP Mode

Not supported.

4.4. Secondary Display Interface

4.4.1 HDMI Mode

Derived from the DSI signals on the carrier; see EB4 schematics for implementation.

4.4.2 DP++ Mode

Not supported.

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4.4.3 MIPI Camera Support

4.4.3.1. CSI (4 Lanes)

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name
CSI_A_DATA0_N	C1	I LVDS D-PHY / I LVDS M-PHY			CSI1_DN0	i.MX95	MIPI_CSI1_D0_N
CSI_A_DATA0_P	B1				CSI1_DP0	i.MX95	MIPI_CSI1_D0_P
CSI_A_DATA1_N	A2				CSI1_DN1	i.MX95	MIPI_CSI1_D1_N
CSI_A_DATA1_P	A3				CSI1_DP1	i.MX95	MIPI_CSI1_D1_P
CSI_A_DATA2_N	A5				CSI1_DN2	i.MX95	MIPI_CSI1_D2_N
CSI_A_DATA2_P	A6				CSI1_DP2	i.MX95	MIPI_CSI1_D2_P
CSI_A_DATA3_N	B6				CSI1_DN3	i.MX95	MIPI_CSI1_D3_N
CSI_A_DATA3_P	B7				CSI1_DP3	i.MX95	MIPI_CSI1_D3_P
CSI_A_CLOCK_N	B3	I LVDS D-PHY			CSI1_CKN	i.MX95	MIPI_CSI1_CLK_N
CSI_A_CLOCK_P	B4	I LVDS D-PHY			CSI1_CKP	i.MX95	MIPI_CSI1_CLK_P
CAM_MCK	C2	O CMOS	1.8V		CSI1_MCLK_1V8	i.MX95	CCM_CLKO1
CAM_A_SDA / CSI_A_TX_N	C3	I/O OD CMOS / O LVDS M-PHY	1.8V	PU 2k2	I2C2_SDA_1V8	i.MX95	I2C2_SDA
CAM_A_SCL / CSI_A_TX_P	C4	I/O OD CMOS / O LVDS M-PHY	1.8V	PU 2k2	I2C2_SCL_1V8	i.MX95	I2C2_SCL
CAM_A_PWR / GPIO_C_6	G3	O CMOS	1.8V		CSI1_PWR_1V8	i.MX95	PB12
CAM_A_RST# / GPIO_C_7	G4	O CMOS	1.8V		CSI1_RST_1V8	i.MX95	PB13

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4.4.4 Audio Interfaces

4.4.4.1. I²S0

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name
I2S_A_DATA_IN	V21	I/O CMOS	1.8V		SAI3_RXD_1V8	i.MX95	GPIO_IO20
I2S_A_DATA_OUT	W21				SAI3_TXD_1V8	i.MX95	GPIO_IO21
I2S_B_DATA_IN	V19				SAI1_RXD_1V8	i.MX95	SAI1_RXD0
I2S_B_DATA_OUT	W19				SAI1_TXD_1V8	i.MX95	SAI1_TXD0
I2S_MCLK	V18				SAI3_MCLK_1V8	i.MX95	GPIO_IO17
I2S_A_LRCLK	W18				SAI3_TXFS_1V8	i.MX95	GPIO_IO26
I2S_A_BITCLK	W20				SAI3_TXC_1V8	i.MX95	GPIO_IO16
I2S_B_LRCLK	T18				(not connect)		
I2S_B_BITCLK	T19				(not connect)		

4.4.5 USB Ports

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name
USB_A_D_N	AB13	I/O USB	USB		USB2_DN_CPU	i.MX95	USB2_D_N
USB_A_D_P	AC14	I/O USB	USB		USB2_DP_CPU	i.MX95	USB2_D_P
USB_A_ID	AB14	I OD CMOS	1.8V	PU 10k	USB2_ID_1V8	i.MX95	USB2_ID
USB_A_OC#	AC15	I OD CMOS	1.8V	PU 10k	USB2_OC#_1V8	i.MX95	ENET2_MDIO
USB_A_VBUS	AB16	I USB VBUS 5V	5V		(not connect)		
USB_A_EN	AC16	O CMOS	1.8V		USB_A_EN_1V8	MCU(STM32L431RCI6)	PB6
USB_C_D_N	D11	I/O USB	USB		USB1_DN_CPU	i.MX95	USB1_D_N
USB_C_D_P	D10	I/O USB	USB		USB1_DP_CPU	i.MX95	USB1_D_P
USB_C_OC#	C8	I OD CMOS	1.8V	PU 10K	USB1_OC#_1V8	i.MX95	ENET2_MDC
USB_C_EN	C10	O CMOS	1.8V		USB1_EN_1V8	i.MX95	GPIO_IO12
USB_C_SSTX_N	A9	O USB SS	USB SS		USB1_TX0_N	i.MX95	USB1_TX0_N

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USB_C_SSTX_P	A8	O USB SS	USB SS		USB1_TX0_P	i.MX95	USB1_TX0_P
USB_C_SSRX_N	B11	I USB SS	USB SS		USB1_RX0_N	i.MX95	USB1_RX0_N
USB_C_SSRX_P	B10	I USB SS	USB SS		USB1_RX0_P	i.MX95	USB1_RX0_P

Note 1: USB A supports OTG and Host.

Note: **2**: USB C carries SS signals.

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4.4.6 PCIe

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name
PCIe_A_HSI0_P	AB1	I LVDS PCIE			PCIEA_RX0_P	i.MX95	PCIE1_RX0_P
PCIe_A_HSI0_N	AB2	I LVDS PCIE			PCIEA_RX0_N	i.MX95	PCIE1_RX0_N
PCIe_A_HSO0_P	AC2	O LVDS PCIE			PCIEA_TX0_P	i.MX95	PCIE1_TX0_P
PCIe_A_HSO0_N	AC3	O LVDS PCIE			PCIEA_TX0_N	i.MX95	PCIE1_TX0_N
PCIe_CLKREQ#	W2	I OD CMOS	1.8V	PU 10k	PCIEA_CLKREQ#_1V8	i.MX95	GPIO_IO32
PCIe_A_PERST#	V2	O CMOS	1.8V		PCIEA_RST#_1V8	MCU(STM32L431RCI6)	PB5
PCIe_REFCLK_P	W1	O LVDS PCIE			PCIEA_CLKOUT_P	i.MX95	PCIE_REF_OUT_CLK_P
PCIe_REFCLK_N	Y1	O LVDS PCIE			PCIEA_CLKOUT_N	i.MX95	PCIE_REF_OUT_CLK_N
PCIe_WAKE#	T2	I OD CMOS	1.8V	PU 10k	PCIE_WAKE#_1V8	PCAL6408AHKX	P4
PCIe_SMDAT	U1	I/O OD CMOS	1.8V	PU 2k2	I2C2_SDA_1V8	i.MX95	I2C2_SDA
PCIe_SMCLK	T1	O OD CMOS	1.8V	PU 2k2	I2C2_SCL_1V8	i.MX95	I2C2_SCL
PCIe_SM_ALERT#	R2	I OD CMOS	1.8V	PU 2k2	I2C2_INT#_1V8	i.MX95	GPIO_IO27

4.4.7 LAN Port

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name
ETH_A_(R)(G)MII_CRS	E16	I CMOS	1.8V		(not connect)		
ETH_A_(R)(G)MII_COL	F15	I CMOS			(not connect)		
ETH_A_(S)(R)(G)MII_TXD0	H15	O CMOS			ENET1_TD0	i.MX95	ENET1_TD0
ETH_A_(S)(R)(G)MII_TXD1	G15	O CMOS			ENET1_TD1	i.MX95	ENET1_TD1
ETH_A_(S)(R)(G)MII_TXD2	H16	O CMOS			ENET1_TD2	i.MX95	ENET1_TD2
ETH_A_(S)(R)(G)MII_TXD3	G16	O CMOS			ENET1_TD3	i.MX95	ENET1_TD3
ETH_A_(R)(G)MII_TX_EN(_ER)	K16	O CMOS			ENET1_TX_CTL	i.MX95	ENET1_TX_CTL
ETH_A_(R)(G)MII_TX_CLK	J15	I/O CMOS			ENET1_TXC	i.MX95	ENET1_TXC

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ETH_A_(S)(R)(G)MII_RXD0	K15	I CMOS			ENET1_RD0	i.MX95	ENET1_RD0
ETH_A_(S)(R)(G)MII_RXD1	L15	I CMOS			ENET1_RD1	i.MX95	ENET1_RD1
ETH_A_(R)(G)MII_RXD3	P15	I CMOS			ENET1_RD3	i.MX95	ENET1_RD3
ETH_A_(R)(G)MII_RX_ER	L16	I CMOS			(not connect)		
ETH_A_(R)(G)MII_RX_DV(_ER)	M15	I CMOS			ENET1_RX_CTL	i.MX95	ENET1_RX_CTL
ETH_A_(R)(G)MII_RX_CLK	R15	I/O CMOS			ENET1_RXC	i.MX95	ENET1_RXC
ETH_A_SDP	N16	O CMOS			(not connect)		
ETH_MDIO	T15	I/O CMOS			ENET1_MDIO_1V8	i.MX95	ENET1_MDIO
ETH_MDC	T16	O CMOS			ENET1_MDC_1V8	i.MX95	ENET1_MDC
ETH_IOPWR	M17	PO			VDD_1V8_S	PMIC	
ETH_B_(R)(G)MII_CRS	D2	I CMOS			(not connect)		
ETH_B_(R)(G)MII_COL	E1	I CMOS			(not connect)		
ETH_B_(S)(R)(G)MII_TXD0	G1	O CMOS			ENET2_TD0	i.MX95	ENET2_TD0
ETH_B_(S)(R)(G)MII_TXD1	F1	O CMOS			ENET2_TD1	i.MX95	ENET2_TD1
ETH_B_(S)(R)(G)MII_TXD2	G2	O CMOS			ENET2_TD2	i.MX95	ENET2_TD2
ETH_B_(S)(R)(G)MII_TXD3	F2	O CMOS			ENET2_TD3	i.MX95	ENET2_TD3
ETH_B_(R)(G)MII_TX_EN(_ER)	J2	O CMOS			ENET2_TX_CTL	i.MX95	ENET2_TX_CTL
ETH_B_(R)(G)MII_TX_CLK	H1	I/O CMOS			ENET2_TXC	i.MX95	ENET2_TXC
ETH_B_(S)(R)(G)MII_RXD0	J1	I CMOS			ENET2_RD0	i.MX95	ENET2_RD0
ETH_B_(S)(R)(G)MII_RXD1	K1	I CMOS			ENET2_RD1	i.MX95	ENET2_RD1
ETH_B_(R)(G)MII_RXD2	M1	I CMOS			ENET2_RD2	i.MX95	ENET2_RD2
ETH_B_(R)(G)MII_RXD3	N1	I CMOS			ENET2_RD3	i.MX95	ENET2_RD3
ETH_B_(R)(G)MII_RX_ER	K2	I CMOS			(not connect)		
ETH_B_(R)(G)MII_RX_DV(_ER)	L1	I CMOS			ENET2_RX_CTL	i.MX95	ENET2_RX_CTL
ETH_B_(R)(G)MII_RX_CLK	P1	I/O CMOS			ENET2_RXC	i.MX95	ENET2_RXC
ETH_B_SDP	M2	O CMOS			(not connect)		
ETH_B_MDIO	C7	I/O CMOS			ENET1_MDIO_1V8		ENET1_MDIO
ETH_B_MDC	C6	O CMOS			ENET1_MDC_1V8		ENET1_MDC

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4.4.8 SDIO Card (4-Bit)

The carrier SDIO card ***may*** be selected as the boot device.

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller
SDIO_A_CMD	E20	I/O CMOS			SD2_CMD	i.MX95
SDIO_A_CLK	F21	O CMOS			SD2_CLK	i.MX95
SDIO_A_D0	G20	I/O CMOS			SD2_DATA0	i.MX95
SDIO_A_D1	G21	I/O CMOS			SD2_DATA1	i.MX95
SDIO_A_D2	H20	I/O CMOS			SD2_DATA2	i.MX95
SDIO_A_D3	H21	I/O CMOS			SD2_DATA3	i.MX95
SDIO_A_CD#	J21	I OD CMOS		PU 10K	SD2_CD_B_1V8A3V	i.MX95
SDIO_A_WP	D20	I OD CMOS		PU 10K	SD2_WP_1V8	i.MX95
SDIO_A_PWR_EN	D21	O CMOS			SD2_RST_B_1V8A3V	i.MX95
SDIO_A_IOPWR	C20	PO			VDD_SDIO2_S	PMIC
SDIO_B_CLK	K20	O CMOS			SD3_CLK	i.MX95
SDIO_B_CMD	K21	I/O CMOS			SD3_CMD	i.MX95
SDIO_B_D0	L20	I/O CMOS			SD3_DATA0	i.MX95
SDIO_B_D1	L21	I/O CMOS			SD3_DATA1	i.MX95
SDIO_B_D2	M21	I/O CMOS			SD3_DATA2	i.MX95
SDIO_B_D3	N20	I/O CMOS			SD3_DATA3	i.MX95
SDIO_B_D4	N21	I/O CMOS			(not connect)	
SDIO_B_D5	P20	I/O CMOS			(not connect)	
SDIO_B_D6	P21	I/O CMOS			(not connect)	
SDIO_B_D7	R21	I/O CMOS			(not connect)	
SDIO_B_CD#	T21	I OD CMOS		PU 10K	(not connect)	
SDIO_B_WP	U20	I OD CMOS		PU 10K	(not connect)	
SDIO_B_PWR_EN	U21	O CMOS			(not connect)	
SDIO_B_IOPWR	T20	PO			VDD_1V8_S	PMIC

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4.4.9 SPI Interfaces

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name
SPI_A_SDI_(IO1)	U15	I/O CMOS			QSPIA_DATA1	i.MX95	XSPI1_DATA1
SPI_A_SDO_(IO0)	V15	I/O CMOS			QSPIA_DATA0	i.MX95	XSPI1_DATA0
SPI_A_/WP_(IO2)	W16	I/O CMOS			QSPIA_DATA2	i.MX95	XSPI1_DATA2
SPI_A_/HOLD_(IO3)	W15	I/O CMOS			QSPIA_DATA3	i.MX95	XSPI1_DATA3
SPI_A_CS0#	Y15	O CMOS		100K PU	QSPIA_nSS0	i.MX95	XSPI1_SS0_B
SPI_A_CS1# / GPIO_A_6	K17	O CMOS		100K PU	QSPIA_nSS1	i.MX95	XSPI1_SS1_B
SPI_A_SCK	U16	O CMOS			QSPIA_SCLK	i.MX95	XSPI1_SCLK
SPI_B_SDI	Y22	I CMOS			SPI6_MISO_1V8	i.MX95	GPIO_IO01
SPI_B_SDO	Y23	O CMOS			SPI6_MOSI_1V8	i.MX95	GPIO_IO02
SPI_B_CS0#	AA23	O CMOS		100K PU	SPI6_SS0_1V8	i.MX95	GPIO_IO00
SPI_B_CS1# / GPIO_A_7	L17	O CMOS		100K PU	SPI6_SS1_1V8	i.MX95	GPIO_IO24
SPI_B_SCK	Y21	O CMOS			SPI6_SCLK_1V8	i.MX95	GPIO_IO03
SPI_C_SDI	C29	I CMOS	1.8V		SPI7_MISO_1V8	i.MX95	GPIO_IO05
SPI_C_SDO	D30	O CMOS	1.8V		SPI7_MOSI_1V8	i.MX95	GPIO_IO06
SPI_C_CS0#	C30	O CMOS	1.8V		SPI7_SS0_1V8	i.MX95	GPIO_IO04
SPI_C_CS1# / GPIO_D_7	Y33	O CMOS	1.8V		SPI7_SS1_1V8	i.MX95	GPIO_IO25
SPI_C_SCK	D29	O CMOS	1.8V		SPI7_SCLK_1V8	i.MX95	GPIO_IO07

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4.4.10 GPIO

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name
GPIO_A_0	D17	I/O CMOS			GPIO_A0_1V8	i.MX95	GPIO_IO18
GPIO_A_1	E17				GPIO_A1_1V8	i.MX95	GPIO_IO19
GPIO_A_2	F17				GPIO_A2_1V8	i.MX95	GPIO_IO33
GPIO_A_3	G17				GPIO_A3_1V8	i.MX95	GPIO_IO34
GPIO_A_4	H17				GPIO_A4_1V8	i.MX95	XSPI1_DATA4
GPIO_A_5	J17				GPIO_A5_1V8	i.MX95	XSPI1_DATA5
GPIO_B_0	D19				GPIO_B0_1V8	i.MX95	XSPI1_DATA6
GPIO_B_1	E19				GPIO_B1_1V8	i.MX95	XSPI1_DATA7
GPIO_B_2	F19				GPIO_B2_1V8	MCU(STM32L431RCI6)	PA2
GPIO_B_3	G19				GPIO_B3_1V8	MCU(STM32L431RCI6)	PA3
GPIO_B_4	H19				GPIO_B4_1V8	MCU(STM32L431RCI6)	PA4
GPIO_B_5	J19				GPIO_B5_1V8	MCU(STM32L431RCI6)	PA7
GPIO_B_6	K19				GPIO_B6_1V8	MCU(STM32L431RCI6)	PA8
GPIO_B_7	L19				GPIO_B7_1V8	MCU(STM32L431RCI6)	PA9

Note: Fast GPIOs are directly from the i.MX95.

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4.4.11 Power + Boot Select

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name
VCC_2_TEST	M19	PO	0.61V ~ 0.955V		VDD_SOC	PMIC	
VCC_3_TEST	Y16	PO	0.8V		VDD_DDR	PMIC	
VCC_4_TEST	Y20	PO	0.5V		VDDQ_CPU_DDR_S	PMIC	
VCC_IN_5V	Y17	P	5V		VSYS_5V	From carrier	
VCC_IN_3V3	Y19	P	3.3V		(not connect)		
V_BAT	AA18, AB18	P			(not connect)		
GND	D18, E15, E21, F16, F20, J16, J20, L18, M16, M20, P18, R16, R20, V16, V20, Y18, AA14, AA17, AA19, AA22, AB15, AB21	P			GND		
RESET_OUT#	Y14	O CMOS	1.8V		1P8_RESET_OUT-L	Logic IC	
RESET_IN#	U17	I OD CMOS	1.8V	PU 10K	RST_IN#_1V8	Logic IC	
CARRIER_PWR_EN	V17	O CMOS	1.8V		CARRIER_PWR_EN	Logic IC	
CARRIER_STBY	Y13	O CMOS	1.8V		1P8_CARRIER_STBY-L	Logic IC	
VCC_OUT_IO	U18	P	1.8V		VDD_1V8_S	PMIC	
RTC_PWR	W17	P			(not connect)		
BOOT_SEL0#	U19	I OD CMOS	1.8V	PU 10K	BOOT_SEL0#_1V8	MCU(STM32L431RCI6)	PC6

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BOOT_SEL1#	R18	I OD CMOS	1.8V	PU 10K	BOOT_SEL1#_1V8	MCU(STM32L431RCI6)	PC7
FORCE_RECOVERY#	T17	I OD CMOS	1.8V	PU 10K	FORCE_RECOVERY#_1V8	MCU(STM32L431RCI6)	PC9
VCC_5_TEST	Y3	PO			VDD2_CPU_DDR_S	PMIC	
VCC_6_TEST	C5	PO			VDD_ARM	PMIC	
VCC_IN_5V	Y8, Y9, Y10, Y11	P			VSYS_5V	From carrier	
GND	A4, A7, A10, B2, B5, B8, B9, C11, D1, D5, D8, E2, H2, H4, L2, L4, P2, P4, R1, U2, U4, V1, W3, Y2, AA1, AA4, AA7, AA8, AA10, AA11, AB3, AB6, AB9, AC4, AC7, AC10	P			GND		
PWR_BTN#	AA9	I OD CMOS		PU 10K	ONOFF_1V8	i.MX95	ONOFF
VCC_7_TEST	AA33	P	3.3V		VDD_3V3_S	PMIC	
VCC_8_TEST	B29	P	1.8V		VDD_1V8_S	PMIC	
VCC_IN_5V	Y25, Y26, Y27, Y28	P	5V		VSYS_5V	From carrier	

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GND	A26, A29, A32, B27, B28, B30, B33, C25, C32, C35, D28, D34, F33, F35, G34, H32, J33, J35, K34, M35, N34, T34, W34, AA25, AA26, AA27, AA28, AA32, AB28, AB31, AB34, AC27, AC30, AC33	P			GND		
VCC_IN_5V	AE4, AF4, AG4, AH3, AH4, AJ3, AJ4, AK4	P	5V		VSYS_5V	From carrier	
GND	AE2, AE34, AF35, AG3, AH2, AH34, AJ35, AK3, AL2, AL34, AM13, AM16, AM19, AM22, AM35, AN3, AN6, AN9, AN11, AN15, AN18, AN21, AN33, AP2, AP5, AP8, AP13, AP16, AP19, AP22, AP25, AP28, AP31, AP34, AR14, AR17, AR20, AR26, AR29, AR32	P			GND		

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5. Software Support

5.1. Standard Support

The standard OS is Yocto

5.2. Yocto

All features are supported on the Yocto 64-bit BSP, based on the latest kernel supported by NXP.

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6. Mechanical

6.1. Module Dimensions

Module OSM L Size 45x 45mm

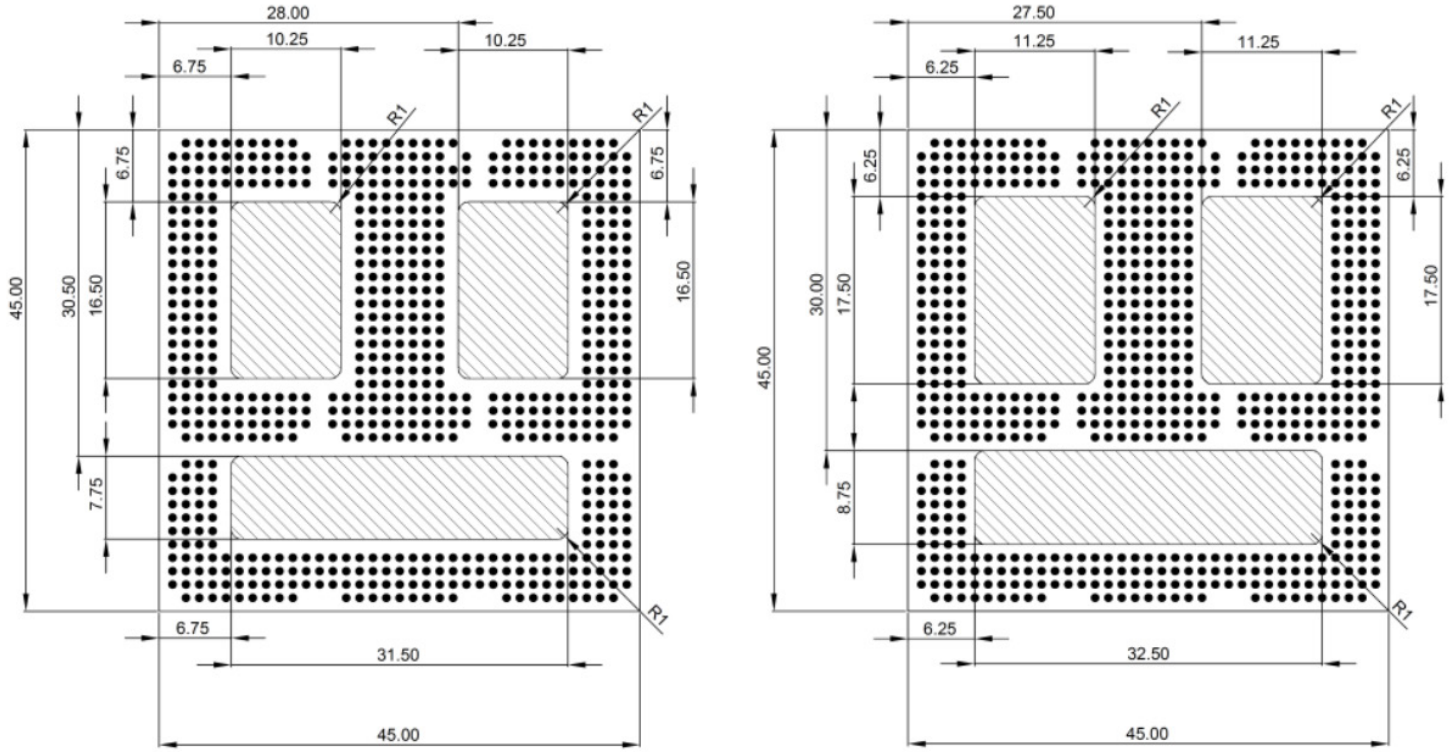


Figure 16: Placement Area (left) and Cut-Out Area (right) - Size L (view from bottom)

Figure 4 – Placement and cut-out area – Size (L)

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7. Thermal Solutions

7.1. Heatspreader: HTS

To be defined on the carrier.

7.2. Heatsink: THS

To be defined on the carrier.

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