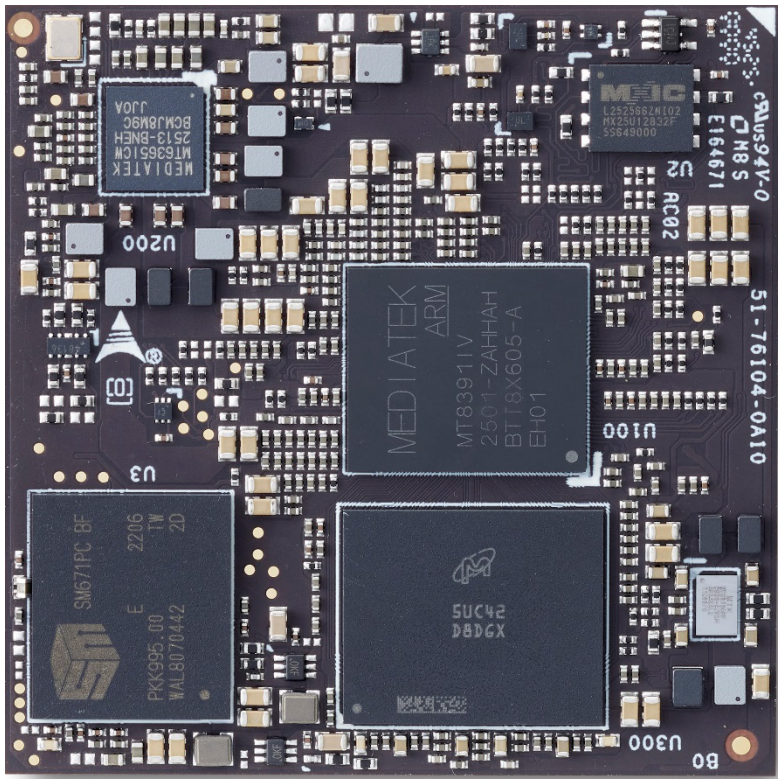
OSM-MTK520

User's Guide

Powered by MediaTek



OPEN STANDARD MODULE ™

Revision:	Rev. 1.0
Date:	2026-04-02
Part Number:	50M-76104-1000

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Revision History

Revision	Description	Date	Author
1.0	Initial release	2026-04-02	AL

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Preface

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Safety Instructions

For user safety, please read and follow all Instructions, **WARNING**s, **CAUTION**s, and **NOTE**s marked in this manual and on the associated equipment before handling/operating the equipment.

Read these safety instructions carefully.

- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

Conventions

The following conventions may be used throughout this manual, denoting special levels of information

Note: This information adds clarity or specifics to text and illustrations.

Caution: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.

Warning: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

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1. Introduction

1.1 The OSM Form Factor

The OSM ("Open Standard Module") Open Standard Module™ specification facilitates the development, production, and distribution of embedded modules tailored for renowned MCU32, ARM, and x86 architectures. This standard is increasingly relevant for IoT applications, as it merges the benefits of modular embedded computing with the growing demands for cost efficiency, compactness, and versatile interfaces.

The modules serve as building blocks for portable and stationary embedded systems. They integrate the core CPU and support circuits, including DRAM, boot flash, power sequencing, and CPU power supplies. The modules are used with application-specific carrier boards to implement features such as audio CODECs, touch controllers, wireless devices, PHY, and more. The modular design not only promotes scalability and fast time to market but also ensures upgradability, all while maintaining low costs, low power consumption, and a compact physical size.

1.2 Brief

The OSM-MTK520 is an OSM (Open Standard Module) size-L form factor designed for small-sized, low-cost embedded computer modules, fully compliant with the SGET (Standardization Group for Embedded Technologies) OSM Specification Version 1.2.

OSM modules combine the advantages of modular embedded computing with increasing requirements for cost, space, and interfaces. The core of the OSM-MTK520 is the MT8371 CPU, which integrates an ARM processor core, graphics, an LPDDR5 memory controller, and I/O interfaces into a single system-on-chip solution. The OSM-MTK520 also includes high-bandwidth interfaces such as PCI Express, USB 3.0/2.0, Gigabit Ethernet, CSI, I2S, DP, eDP, DSI, and SDIO/UFS.

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1.3 Module Feature List

Memory: LPDDR5 2 to 16GB
UFS: BGA 64 to 512 GB
LAN: GbE built in MAC with TSN support
Graphics: Mali-G57 MC2 GPU
USB: 1x USB 3.1, 2x USB 2.0, 1x USB 2.0 OTG
AUDIO: I²S to carrier
PCIe: Single Lane Gen 2
Industrial interfaces: SPI/I2C/I2S/UART/GPIO
SECURITY: Arm® TrustZone Security

SGeT STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

OSM module and carrier specifications are available online at: https://sget.org/standards/osm/

Note: This module is compliant with the SGET OSM 1.2 specifications.

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2. Specifications

2.1 Core System

CPU
CPU: 2x ARM Cortex-A78 @2.0 GHz | 6x Cortex A55 @2.0 GHz |
NPU: MediaTek 8th Gen. NPU
GPU: Arm Mali G57 MC2

ARM Cortex-A78 / A55 MP Core processors are high-performance and optimized for low power.

Memory
• LPDDR5-soldered down, single chip up to 16GB
• 32-bit DRAM interface

L2 Cache
64KB instruction L1 cache
64KB data cache
256KB L2 cache
Each core has it's own cache

security
•Arm® TrustZone

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2.2 Video

2.2.1 GPU

GPU Core
Mali G57 MC2

Graphics Feature Support
2x DVPP pipelines, with following support

DP
Supports DP1.4 / eDP1.3 combo interface, 4-lane up to 5.4 Gbps per lane and combo with USB3.2 port 0 / 3840 x 2160 @60 fps

eDP
Support eDP 1.4b 4-lane up to 5.4 Gbps per lane, up to 3840 x 2160 @60 fps

MIPI DSI
4-lane D-PHY, up to 2.5Gbps per lane, support up to 2560 x 1600 @60 fps

LVDS
Single link LVDS TX up to 1.05 Gbps channel speeds, support up to 1920 x 1080 @60 fps

2.2.2 Display Interfaces

DP
Maximum resolution up to 5120 x 2160 @60 fps

eDP
Maximum resolution up to 3840 x 2160 @60 fps

MIPI DSI
1x MIPI DSI 4 lane compliant to MIPI-DSI standard v1.2

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Maximum resolution 2560 x 1600 @60 fps

LVDS

1x LVDS single link up to 1920 x 1080 @60 fps

Note: LVDS/MIPI DSI pin sharing

2.3 Camera

Two 4-lane MIPI CSI2 camera input. (CSI_A / CSI_B)

2.4 Audio

I2S to carrier

2.5 Wired Ethernet

LAN

Built in MAC 10/100/1000 Ethernet Controller on SoC

Supports 10/100/1000-Mbps data transfer rates, both full-duplex and half-duplex

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2.6 Extension busses

USB
1x USB 3.1, 2x USB 2.0, 1x USB 2.0 OTG

UART
4 UART interfaces (A: TX/RX/CTS/RTS; C & D: TX/RX; 1x console: TX/RX)

SPI
3x SPI

I2S
2x I2S for connection with optional external audio codec

I2C
2 x I2C interfaces
- Support for 7-bit mode
- Software programmable clock frequency of 100 kbit/s in Standard-mode, 400 kbit/s in the Fast-mode or 1 Mbit/s in Fast-mode Plus

GPIO
22x GPIO with interrupt

2.7 System Storage

SDIO
2x SDIO (4-bit) compatible with SD3.0

UFS
64, 128, 256, 512 GB (build option)
UFS 3.1 2-Lane supports HS-G4B mode

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2.8 Power

Power Modes:	ON / OFF / SUSPEND
Power on / off behaviour same as x86	*ATX (hold off boot until PWRBTN) / AT (always boot)*
Voltage Input:	5.0V +/- 5%
Operating Temperatures	
Standard Operating Temperature:	0°C to 60°C commercial grade BOM (memory, UFS, USB hub, SOC)
Extreme Rugged Operating Temperature:	-40°C + 85°C industrial grade BOM (memory, UFS, USB hub, SOC)
Derating for two different BOMs	
Environmental	
Humidity:	5-90% RH operating, non-condensing 5-95% RH storage (and operating with conformal coating).
EMI:	EN55022 Class B inside an enclosure
Shock and Vibration:	HALT Testing, with test report that confirms Extended Operating Temp range during and after vibration. Separate Shock test report to MIL-STD-202F, Method 213B, Table 213-I, Condition A. IN ADDITION: When installed on baseboard shall operate under 18 sawtooth mechanical shocks (3 shocks in each direction) with a peak acceleration of 40g for a duration of 18 msec each and 75g for a duration of 6 msec each. Capable of supporting Random Vibration: MIL-STD-202F, Method 214A, Table 214-I, Condition D. If HALT testing shows equal or better performance, a separate vibration test report is not necessary.
MTBF:	300,000 hrs (at 40°C), 100,000 hrs (at 85°C),

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3. Block Diagram

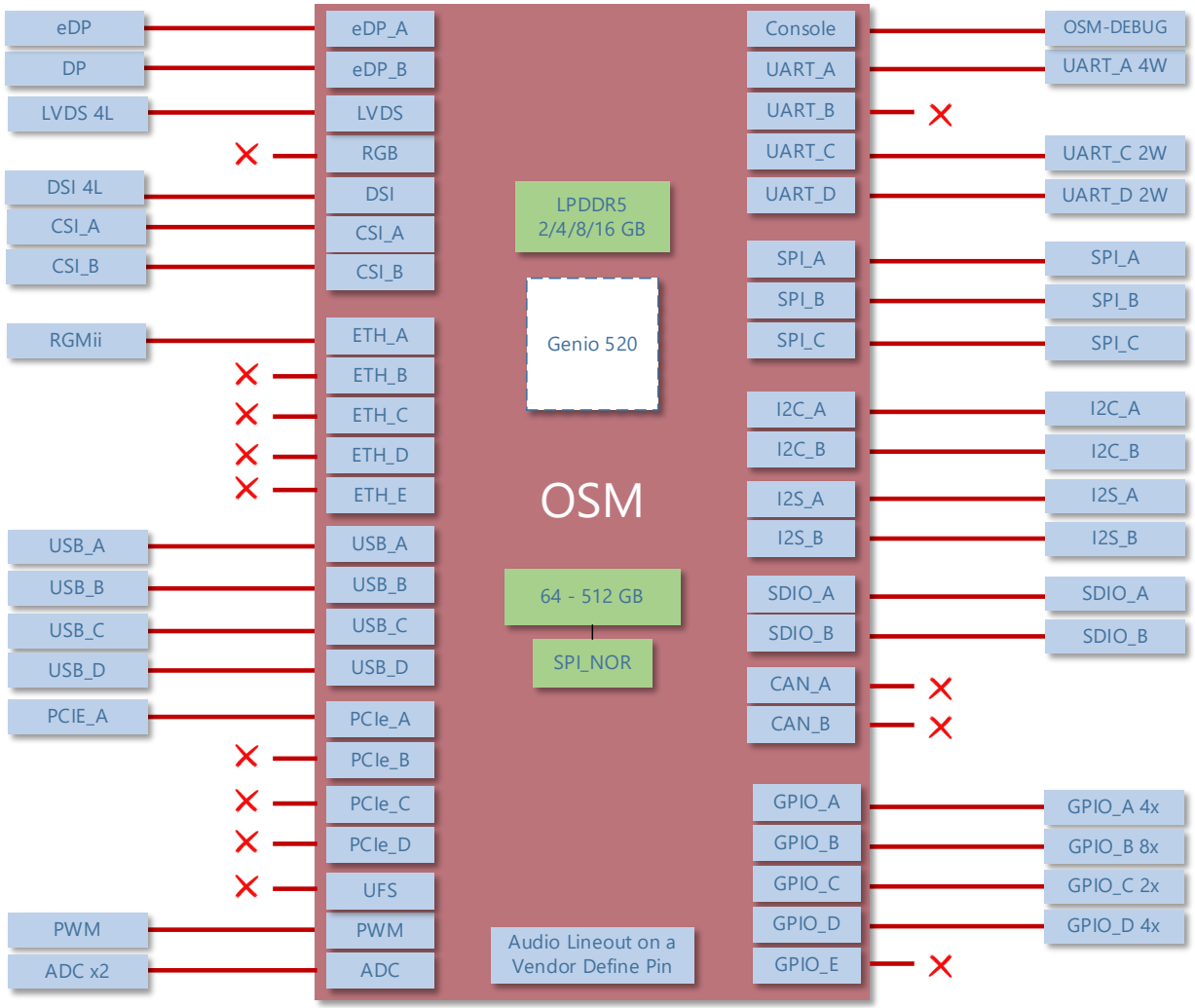


Figure 1 – Module function diagram

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4. Pinout and Signal Descriptions

4.1 Pin Summary

The tables below are a list of all signals to the LGA pads following the OSM 1.2 specifications.

- Size-0 – "Zero": 30 mm x 15 mm
- Size-S – "Small": 30 mm x 30 mm
- Size-M – "Medium": 30 mm x 45 mm
- Size-L – "Large": 45 mm x 45 mm

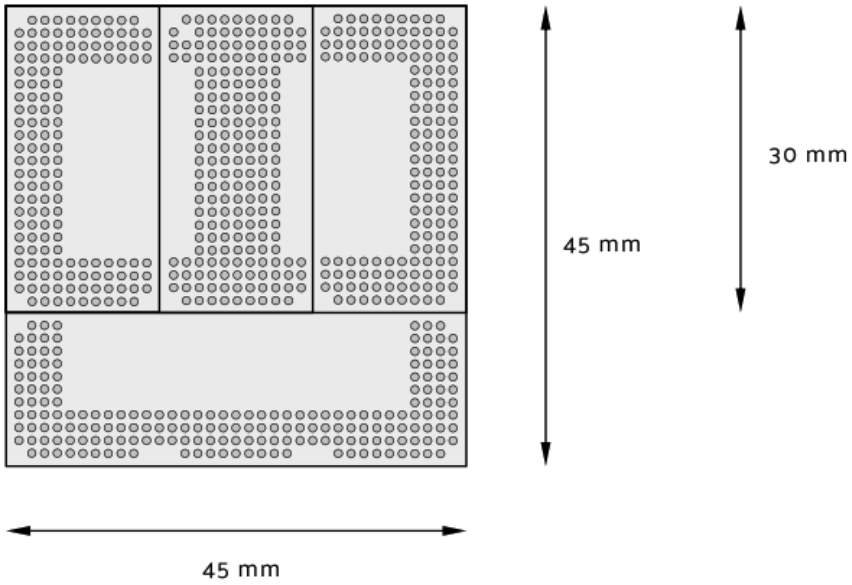


Figure 2 – Module size grid

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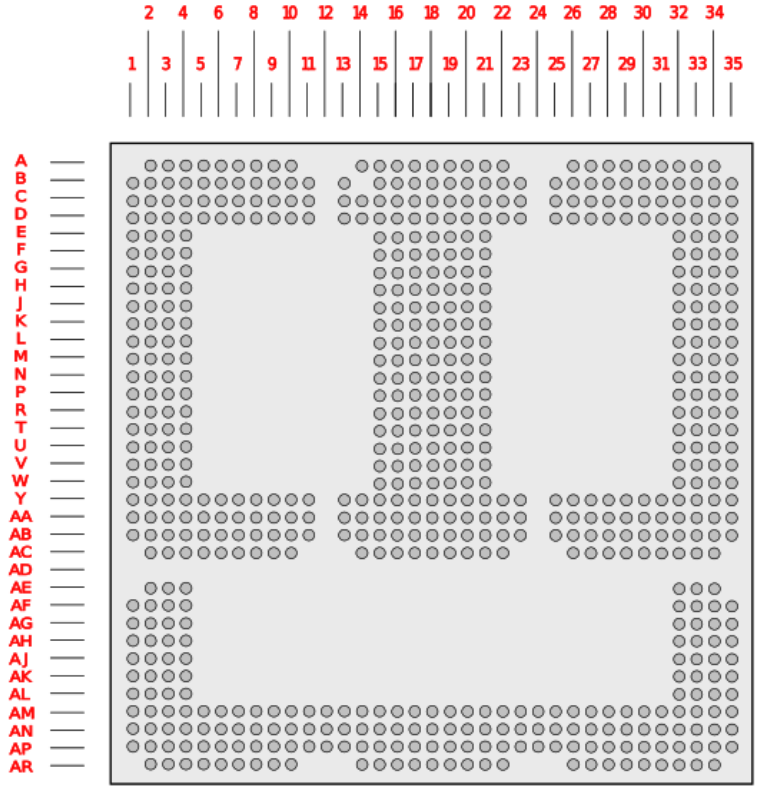


Figure 21: Contact Grid (all sizes) (view from top, through the module)

Figure 3 – Module pinout grid

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4.2 Signal Terminology Descriptions

Meaning of the terms used for signal description tables. Signals described in the specification but not supported on the OSM-MTK520 are marked with strikethrough ~~STRIKETHROUGH~~.

Term	Description
I	Input to the Module
O	Output from the Module
I/O	Bi-directional input/output
OD	Open drain
PU	PU (pull-up) resistor
PD	PD (pull-down) resistor
CMOS	Logic input or output
GBE MDI	Differential analogue signalling for gigabit media dependent interface
DP	Low voltage differential signal for DisplayPort interface
D-PHY	Low voltage differential signal for MIPI CSI-2 cameras and DSI displays
M-PHY	Low voltage differential signal for MIPI CSI-3 cameras
LVDS	Low voltage differential signal for LCD displays
PCIE	Low voltage differential signal for PCIe
SATA	Low voltage differential signal for SATA
TMDS HDMI	Transition minimized differential signal for HDMI displays
USB	DC coupled differential signalling for traditional (non-Superspeed) USB signals
USB SS	Differential signal for SuperSpeed USB signals
USB VBUS 5V	5V tolerant input for USB VBUS detection
VDD_IN	Main power source from Carrier to Module
3.3V	3.3V power domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
1.8V	1.8V power domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
3.3Vsb	3.3V standby power domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)
1.8Vsb	1.8V standby power domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)
Sleep	Module is in its lowest power state
Runtime	Module is full on. CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
Standby	Module is in standby state or higher

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4.3 Full Signal to Pad Table

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name	Description
GND	D18, E15, E21, F16, F20, J16, J20, L18, M16, M20, P18, R16, R20, V16, V20, Y18, AA14, AA17, AA19, AA22, AB15, AB21	P			GND			Module Signal and power return and GND reference
I2S_B_LRCLK	T18	O CMOS	VCC_OUT_IO		I2S_B_LRCLK	MTK MT8371	DMIC1_CLK	Reset output from CPU to reset peripherals on Carrier.
RESET_OUT#	Y14	O CMOS	VCC_OUT_IO		OSM_nRST_OUT	Logic IC		
CARRIER_STBY#	Y13				CARRIER_STBY#	Logic IC		
RESET_IN#	U17	I OD CMOS	VCC_OUT_IO	PU 10K	OSM_nRST_IN	Logic IC		Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise.
CARRIER_PWR_EN	V17	O CMOS	VCC_OUT_IO		CARRIER_PWR_EN	Logic IC		Carrier board circuits should not be powered up until the module asserts the CARRIER_PWR_EN signal.
VCC_OUT_IO	U18	P	1.8V / 3.3V		VIO18_PMU	MTK MT6365	VIO18	Can provide IO voltage level for several interfaces to connect
RTC_PWR	W17	P			VRTC_PWR	MTK MT6365	VRTC28	Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based Lithium cell or Super Cap.
BOOT_SEL0#	U19	I OD CMOS	VCC_OUT_IO	PU 10K	BOOT_SEL0#	Logic IC		
BOOT_SEL1#	R18	I OD CMOS	VCC_OUT_IO	PU 10K	BOOT_SEL1#	Logic IC		
FORCE_RECOVERY#	T17	I OD CMOS	VCC_OUT_IO	PU 10K	FORCE_RECOVERY#	MTK MT8371	KPCOL0	If low on carrier board module enters recovery mode.
JTAG_TCK(SWCLK)	N17	I CMOS	VCC_OUT_IO		JTAG_TCK	MTK MT8371	JTCK	Test Clock
JTAG_TMS(SWDIO)	N19	I CMOS			JTAG_TMS	MTK MT8371	JTMS	Test Mode Select
JTAG_TDI	P17	I CMOS			JTAG_TDI	MTK MT8371	JTDI	Test Data Input

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JTAG_TDO(SWO)	R17	O CMOS			JTAG_TDO	MTK MT8371	JTDO	Test Data Output
JTAG_nTRST	R19	I CMOS			JTAG_nTRST	MTK MT8371	JTRST	Test Reset, Active Low
UART_A_RX	A14	I CMOS	VCC_OUT_IO		UART_A_RX	MTK MT8371	UART2_RXD	Asynchronous serial data input port A
UART_A_TX	B13	O CMOS			UART_A_TX	MTK MT8371	UART2_TXD	Asynchronous serial data output port A
UART_A_RTS	C13	O CMOS			UART_A_RTS	MTK MT8371	GPIO17	Request to Send handshake line for port A
UART_A_CTS	C14	I CMOS			UART_A_CTS	MTK MT8371	GPIO16	Clear to Send handshake line for port A
UART_C_RX	A22	I CMOS	VCC_OUT_IO		UART_C_RX	MTK MT8371	UART1_RXD	Asynchronous serial data input port C
UART_C_TX	B23	O CMOS			UART_C_TX	MTK MT8371	UART1_TXD	Asynchronous serial data output port C
UART_D_RX	C22	I CMOS	VCC_OUT_IO		UART_D_RX	MTK MT8371	UART3_RXD	Asynchronous serial data input port D
UART_D_TX	C23	O CMOS			UART_D_TX	MTK MT8371	UART3_TXD	Asynchronous serial data output port D
UART_CON_RX	D22	I CMOS	VCC_OUT_IO		UART_CON_RX	MTK MT8371	UART0_RXD	Asynchronous serial data input port console
UART_CON_TX	D23	O CMOS			UART_CON_TX	MTK MT8371	UART0_TXD	Asynchronous serial data output port console
ETH_A_(R)(G)MII_COL	F15	I CMOS			GBE_COL	MTK MT8371	GBE_COL	Collision detect (half speed only) port A
ETH_A_(S)(R)(G)MII_TXD0	H15	O CMOS			ETH_A_RGMII_TXD0	MTK MT8371	GBE_TXD0	Transmit data bit 0 (transmitted first) port A
ETH_A_(S)(R)(G)MII_TXD1	G15	O CMOS			ETH_A_RGMII_TXD1	MTK MT8371	GBE_TXD1	Transmit data bit 1 port A
ETH_A_(S)(R)(G)MII_TXD2	H16	O CMOS			ETH_A_RGMII_TXD2	MTK MT8371	GBE_TXD2	Transmit data bit 2 port A
ETH_A_(S)(R)(G)MII_TXD3	G16	O CMOS			ETH_A_RGMII_TXD3	MTK MT8371	GBE_TXD3	Transmit data bit 3 port A
ETH_A_(R)(G)MII_TX_EN(_ER)	K16	O CMOS			ETH_A_RGMII_TX_EN	MTK MT8371	GBE_TXEN	Transmit enable (Error) port A
ETH_A_(R)(G)MII_TX_CLK	J15	I/O CMOS			ETH_A_RGMII_TX_CLK	MTK MT8371	GBE_TXC	Transmit clock port A
ETH_A_(S)(R)(G)MII_RXD0	K15	I CMOS			ETH_A_RGMII_RXD0	MTK MT8371	GBE_RXD0	Receive data bit 0 (received first) port A
ETH_A_(S)(R)(G)MII_RXD1	L15	I CMOS			ETH_A_RGMII_RXD1	MTK MT8371	GBE_RXD1	Receive data bit 1 port A
ETH_A_(R)(G)MII_RXD2	N15	I CMOS			ETH_A_RGMII_RXD2	MTK MT8371	GBE_RXD2	Receive data bit 2 port A
ETH_A_(R)(G)MII_RXD3	P15	I CMOS			ETH_A_RGMII_RXD3	MTK MT8371	GBE_RXD3	Receive data bit 3 port A
ETH_A_(R)(G)MII_RX_ER	L16	I CMOS			ETH_A_RGMII_RX_ER	MTK MT8371	GBE_RXER	Receive error port A
ETH_A_(R)(G)MII_RX_DV(_ER)	M15	I CMOS			ETH_A_RGMII_RX_DV	MTK MT8371	GBE_RXDV	Receive data valid port A
ETH_A_(R)(G)MII_RX_CLK	R15	I/O CMOS			ETH_A_RGMII_RX_CLK	MTK MT8371	GBE_RXC	Receive clock port A
ETH_MDIO	T15	I/O CMOS			ETH_A_MDIO	MTK MT8371	GBE_MIO	Management bus data signal for Ethernet

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ETH_MDC	T16	O CMOS			ETH_A_MDC	MTK MT8371	GBE_MDC	Management bus clock signal for Ethernet
ETH_IOPWR	M17	PO			VIO18_PMU	MTK MT6365	VIO18	ETH voltage. It is used to provide the IO Voltage Level for all Ethernet interfaces.
GPIO_A_0	D17	I/O CMOS	VCC_OUT_IO		GPIO_A_0	MTK MT8371	GPIO06	General purpose I/O Contact A0
GPIO_A_1	E17				GPIO_A_1	MTK MT8371	GPIO07	General purpose I/O Contact A1
GPIO_A_2	F17				GPIO_A_2	MTK MT8371	GPIO08	General purpose I/O Contact A2
GPIO_A_3	G17				GPIO_A_3	MTK MT8371	GPIO09	General purpose I/O Contact A3
GPIO_A_4	H17				ETH_A_RGMII_TX_ER	MTK MT8371	GBE_TXER	General purpose I/O Contact A4
GPIO_A_5	J17				GBE_INTR	MTK MT8371	GBE_INTR	General purpose I/O Contact A5
GPIO_B_0	D19				GPIO_B_0	MTK MT8371	KPROW1	General purpose I/O Contact B0
GPIO_B_1	E19				GPIO_B_1	MTK MT8371	GPIO12	General purpose I/O Contact B1
GPIO_B_2	F19				GPIO_B_2	MTK MT8371	GPIO14	General purpose I/O Contact B2
GPIO_B_3	G19				GPIO_B_3	MTK MT8371	PCM_CLK	General purpose I/O Contact B3
GPIO_B_4	H19				GPIO_B_4	MTK MT8371	PCM_SYNC	General purpose I/O Contact B4
GPIO_B_5	J19				GPIO_B_5	MTK MT8371	PCM_DO	General purpose I/O Contact B5
GPIO_B_6	K19				GPIO_B_6	MTK MT8371	PCM_DI	General purpose I/O Contact B6
GPIO_B_7	L19				GPIO_B_7	MTK MT8371	CMMCLK1	General purpose I/O Contact B7
SDIO_A_CMD	E20	I/O CMOS	1.8V / 3.3V		SDIO_A_CMD	MTK MT8371	MSDC1_CMD	SDIO A Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.
SDIO_A_CLK	F21	O CMOS			SDIO_A_CLK	MTK MT8371	MSDC1_CLK	SDIO A Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.
SDIO_A_D0	G20	I/O CMOS			SDIO_A_DAT0	MTK MT8371	MSDC1_DAT0	SDIO A Data lines. These signals operate in push-pull mode.
SDIO_A_D1	G21	I/O CMOS			SDIO_A_DAT1	MTK MT8371	MSDC1_DAT1	SDIO A Data lines. These signals operate in push-pull mode.
SDIO_A_D2	H20	I/O CMOS			SDIO_A_DAT2	MTK MT8371	MSDC1_DAT2	SDIO A Data lines. These signals operate in push-pull mode.

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SDIO_A_D3	H21	I/O CMOS			SDIO_A_DAT3	MTK MT8371	MSDC1_DAT3	SDIO A Data lines. These signals operate in push-pull mode.
SDIO_A_CD#	J21	I OD CMOS		PU 10K	SDIO_A_CD#	MTK MT8371	GPIO03	SDIO A Card Detect. This signal indicates when a SDIO/MMC card is present.
SDIO_A_PWR_EN	D21	O CMOS			SDIO_A_PWR_EN	MTK MT8371	GPIO04	SDIO A Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.
SDIO_A_IOPWR	C20	PO			VSIM1_PMU	MTK MT6365	VSIM1	SDIO A Voltage. It is used to provide the IO Voltage Level
SDIO_B_CLK	K20	O CMOS			SDIO_B_CLK	MTK MT8371	MSDC2_CLK	SDIO B Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.
SDIO_B_CMD	K21	I/O CMOS			SDIO_B_CMD	MTK MT8371	MSDC2_CMD	SDIO B Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.
SDIO_B_D0	L20	I/O CMOS			SDIO_B_DAT0	MTK MT8371	MSDC2_DAT0	SDIO B Data lines. These signals operate in push-pull mode.
SDIO_B_D1	L21	I/O CMOS			SDIO_B_DAT1	MTK MT8371	MSDC2_DAT1	SDIO B Data lines. These signals operate in push-pull mode.
SDIO_B_D2	M21	I/O CMOS			SDIO_B_DAT2	MTK MT8371	MSDC2_DAT2	SDIO B Data lines. These signals operate in push-pull mode.
SDIO_B_D3	N20	I/O CMOS			SDIO_B_DAT3	MTK MT8371	MSDC2_DAT3	SDIO B Data lines. These signals operate in push-pull mode.
SDIO_B_IOPWR	T20	PO			VIO18_PMU	MTK MT6365	VIO18	SDIO B Voltage. It is used to provide the IO Voltage Level
PWM_0	E18	O CMOS	VCC_OUT_IO		DISP_BL_PWM	MTK MT8371	DISP_PWM0	Pulse width modulation 0
PWM_1	F18	O CMOS			PWM_1	MTK MT8371	GBE_AUX_PPS0	Pulse width modulation 1
PWM_2	G18	O CMOS			PWM_2	MTK MT8371	GBE_AUX_PPS1	Pulse width modulation 2
ADC_0	M18	Analog	0V – 1.8V		ADC_0	MTK MT8371	AUXIN4	Analog Digital Converter 0
ADC_1	N18	Analog			ADC_1	MTK MT8371	AUXIN5	Analog Digital Converter 1
SPI_A_SDI_(IO0)	U15	I/O CMOS	VCC_OUT_IO		SPI_A_MISO	MTK MT8371	SPIM0_MISO	SPI A Serial Data Input
SPI_A_SDO_(IO1)	V15	I/O CMOS			SPI_A_MOSI	MTK MT8371	SPIM0_MOSI	SPI A Serial Data Output
SPI_A_CS0#	Y15	O CMOS			SPI_A_CS0#	MTK MT8371	SPIM0_CS	SPI A Master Chip Select 0

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SPI_A_SCK	U16	O CMOS			SPI_A_SCK	MTK MT8371	SPIM0_CLK	SPI A Serial Data Clock
SPI_B_SDI	Y22	I CMOS			SPI_B_MISO	MTK MT8371	SPIM1_MISO	SPI B Serial Data Input
SPI_B_SDO	Y23	O CMOS			SPI_B_MOSI	MTK MT8371	SPIM1_MOSI	SPI B Serial Data Output
SPI_B_CS0#	AA23	O CMOS			SPI_B_CS0#	MTK MT8371	SPIM1_CS	SPI B Master Chip Select 0
SPI_B_SCK	Y21	O CMOS			SPI_B_SCK	MTK MT8371	SPIM1_CLK	SPI B Serial Data Clock
I2S_A_DATA_IN	V21	I/O CMOS	VCC_OUT_IO		I2S_A_DATA_IN	MTK MT8371	I2SIN0_DI	I2S A Digital audio Input
I2S_A_DATA_OUT	W21				I2S_A_DATA_OUT	MTK MT8371	I2SOUT0_DO	I2S A Digital audio Output
I2S_B_DATA_IN	V19				I2S_B_DATA_IN	MTK MT8371	DMIC1_DAT0	I2S B Digital audio Input
I2S_B_DATA_OUT	W19				I2S_B_DATA_OUT	MTK MT8371	GPIO11	I2S B Digital audio Output
I2S_MCLK	V18				I2S_MCLK	MTK MT8371	I2SIN0_MCK	Master clock output to I2S codec(s)
I2S_A_LRCLK	W18				I2S_A_LRCLK	MTK MT8371	I2SIN0_LRCK	I2S Left & Right synchronization clock
I2S_A_BITCLK	W20				I2S_A_BITCLK	MTK MT8371	I2SIN0_BCK	I2S Digital audio clock
I2S_B_BITCLK	T19				I2S_B_BITCLK	MTK MT8371	DMIC0_DAT0	
USB_A_D_N	AB13	I/O USB	USB		USB_A_DN	MTK MT8371	USB_DM_P0	USB differential data pairs for port A
USB_A_D_P	AC14	I/O USB	USB		USB_A_DP	MTK MT8371	USB_DP_P0	USB differential data pairs for port A
USB_A_ID	AB14	I OD CMOS	VCC_OUT_IO	PU 10k	USB_A_ID	MTK MT8371	USB0_IDDIG	Input Contact to announce OTG device insertion on USB 2.0 port
USB_A_OC#	AC15	I OD CMOS	VCC_OUT_IO	PU 10k	USB_A_OC_N	MTK MT8371	KPCOL1	USB over-current for port A
USB_A_VBUS	AB16	I USB VBUS 5V	5V		USB_A_VBUS	MTK MT8371	USB0_VBUS_VALID	USB port 0 port power detection
USB_A_EN	AC16	O CMOS	VCC_OUT_IO		USB_A_EN	MTK MT8371	USB0_DRV_VBUS	Power enable for USB VBUS voltage
USB_B_D_N	AB23	I/O USB	USB		USB_B_DN	MTK MT8371	USB_DM_P1	USB differential data pairs for port B
USB_B_D_P	AC22	I/O USB	USB		USB_B_DP	MTK MT8371	USB_DP_P1	USB differential data pairs for port B
USB_B_OC#	AC21	I OD CMOS	1.8V	PU 10k	USB_B_OC_N	MTK MT8371	KPROW0	USB over-current for port B
USB_B_EN	AC20	O CMOS	1.8V		USB_B_EN	MTK MT8371	USB1_DRV_VBUS	Power enable for USB VBUS voltage
I2C_A_SCL	AA15	I/O OD CMOS	VCC_OUT_IO, Size-0 only 1.8V, >Size-0	PU 2k2	I2C_A_SCL	MTK MT8371	SCP_SCL0	I2C Port A Clock Signal
I2C_A_SDA	AA16				I2C_A_SDA	MTK MT8371	SCP_SDA0	I2C Port A Data Signal
I2C_B_SCL	AA20				I2C_B_SCL	MTK MT8371	SCP_SCL1	I2C Port B Clock Signal
I2C_B_SDA	AA21				I2C_B_SDA	MTK MT8371	SCP_SDA1	I2C Port B Data Signal

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GND	A4, A7, A10, B2, B5, B8, B9, C11, D1, D5, D8, E2, H2, H4, L2, L4, P2, P4, R1, U2, U4, V1, W3, Y2, AA1, AA4, AA7, AA8, AA10, AA11, AB3, AB6, AB9, AC4, AC7, AC10	P			GND	MTK MT8371	DVSS	Module Signal and power return and GND reference
PWR_BTN#	AA9	I OD CMOS	1.8 to 5V	PU 10K	PWR_BTN#	MTK MT6365	PWRKEY	Power-button input from Carrier board. Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module.
GPIO_C_0	D3	I/O CMOS	VCC_OUT_IO		GPIO_C_0	MTK MT8371	DMIC0_CLK	General purpose I/O Contact C0
GPIO_C_1	D4	I/O CMOS			GPIO_C_1	MTK MT8371	CMMCLK2	General purpose I/O Contact C1
DISP_VDD_EN / GPIO_C_4	F3	I/O CMOS			DISP_VDD_EN	MTK MT8371	GPIO02	General purpose I/O Contact C4
DISP_BL_EN / GPIO_C_5	F4	I/O CMOS			DISP_BL_EN	MTK MT8371	GPIO13	General purpose I/O Contact C5
DSI_DATA0_N / LVDS_A_LANE0_N	AB11	O LVDS D-PHY			DSI_DATA0_N	MTK MT8371	DSI0_D0N_T1A	DSI differential output (point to point)
DSI_DATA0_P / LVDS_A_LANE0_P	AB10	O LVDS D-PHY			DSI_DATA0_P	MTK MT8371	DSI0_D0P_T0C	DSI differential output (point to point)
DSI_DATA1_N / LVDS_A_LANE1_N	AC9	O LVDS D-PHY			DSI_DATA1_N	MTK MT8371	DSI0_D1N_T2B	DSI differential output (point to point)
DSI_DATA1_P / LVDS_A_LANE1_P	AC8	O LVDS D-PHY			DSI_DATA1_P	MTK MT8371	DSI0_D1P_T2A	DSI differential output (point to point)
DSI_DATA2_N / LVDS_A_LANE2_N	AC6	O LVDS D-PHY			DSI_DATA2_N	MTK MT8371	DSI0_D2N_T0B	DSI differential output (point to point)
DSI_DATA2_P / LVDS_A_LANE2_P	AC5	O LVDS D-PHY			DSI_DATA2_P	MTK MT8371	DSI0_D2P_T0A	DSI differential output (point to point)
DSI_DATA3_N / LVDS_A_LANE3_N	AB5	O LVDS D-PHY			DSI_DATA3_N	MTK MT8371	DSI0_D3N	DSI differential output (point to point)
DSI_DATA3_P / LVDS_A_LANE3_P	AB4	O LVDS D-PHY			DSI_DATA3_P	MTK MT8371	DSI0_D3P_T2C	DSI differential output (point to point)

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DSI_CLOCK_N / LVDS_A_CLK_N	AB8	O LVDS D-PHY			DSI_CLOCK_N	MTK MT8371	DSI0_CKN_T1C	DSI differential clock output (point to point)
DSI_CLOCK_P / LVDS_A_CLK_P	AB7	O LVDS D-PHY			DSI_CLOCK_P	MTK MT8371	DSI0_CKP_T1B	DSI differential clock output (point to point)
DSI_TE	AA3	I CMOS	VCC_OUT_IO		DSI_TE	MTK MT8371	DSI0_DSI_TE	DSI panel tearing effect signal
CSI_A_DATA0_N	C1	I LVDS D-PHY / I LVDS M-PHY			CSI_A_DATA0_N	MTK MT8371	CSI0A_L1N_T1A	CSI differential input (point to point)
CSI_A_DATA0_P	B1				CSI_A_DATA0_P	MTK MT8371	CSI0A_L1P_T0C	CSI differential input (point to point)
CSI_A_DATA1_N	A2				CSI_A_DATA1_N	MTK MT8371	CSI0B_L0N_T0B	CSI differential input (point to point)
CSI_A_DATA1_P	A3				CSI_A_DATA1_P	MTK MT8371	CSI0B_L0P_T0A	CSI differential input (point to point)
CSI_A_DATA2_N	A5				CSI_A_DATA2_N	MTK MT8371	CSI0A_L0N_T0A	CSI differential input (point to point)
CSI_A_DATA2_P	A6				CSI_A_DATA2_P	MTK MT8371	CSI0A_L0P_T0B	CSI differential input (point to point)
CSI_A_DATA3_N	B6				CSI_A_DATA3_N	MTK MT8371	CSI0B_L1N_T1A	CSI differential input (point to point)
CSI_A_DATA3_P	B7				CSI_A_DATA3_P	MTK MT8371	CSI0B_L1P_T0C	CSI differential input (point to point)
CSI_A_CLOCK_N	B3	I LVDS D-PHY			CSI_A_CLOCK_N	MTK MT8371	CSI0A_L2N_T1C	CSI differential clock input (point to point)
CSI_A_CLOCK_P	B4	I LVDS D-PHY			CSI_A_CLOCK_P	MTK MT8371	CSI0A_L2P_T1B	CSI differential clock input (point to point)
CAM_MCK	C2	O CMOS	VCC_OUT_IO		CAM_MCLK	MTK MT8371	CMMCLK0	Master clock output
I2C_A_CAM_SDA / CSI_A_TX_N	C3	I/O OD CMOS / O LVDS M-PHY	VCC_OUT_IO	PU 2k2	CAM_A_SDA	MTK MT8371	SDA7	I2C data for serial camera data support link or differential data lane
I2C_A_CAM_SCL / CSI_A_TX_P	C4	I/O OD CMOS / O LVDS M-PHY	VCC_OUT_IO	PU 2k2	CAM_A_SCL	MTK MT8371	SCL7	I2C clock for serial camera data support link or differential data lane
CAM_A_PWR / GPIO_C_6	G3	O CMOS	VCC_OUT_IO		CAM_A_PWR	MTK MT8371	CMMPDN0	Camera 0 Power Enable, active high output.
CAM_A_RST# / GPIO_C_7	G4	O CMOS	VCC_OUT_IO		CAM_A_RST#	MTK MT8371	CMMRST0	Camera 0 reset, active low output
USB_C_D_N	D11	I/O USB	USB		USB_C_DN	MTK MT8371	USB_DM_P3	USB differential data pairs for port C
USB_C_D_P	D10	I/O USB	USB		USB_C_DP	MTK MT8371	USB_DP_P3	USB differential data pairs for port C
USB_C_OC#	C8	I OD CMOS	VCC_OUT_IO	PU 10K	USB_C_OC_N	MTK MT8371	I2SOUT0_MCK	USB over-current for port C
USB_C_EN	C10	O CMOS	VCC_OUT_IO		USB_C_EN	MTK MT8371	USB3_DRV_VBUS	Power enable for USB VBUS voltage
USB_C_SSTX_N	A9	O USB SS	USB SS		USB_C_SSTX_DN	MTK MT8371	SSUSB_TXN_P1	Transmit signal differential pairs for SuperSpeed on port C
USB_C_SSTX_P	A8	O USB SS	USB SS		USB_C_SSTX_DP	MTK MT8371	SSUSB_TXP_P1	Transmit signal differential pairs for SuperSpeed on port C

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USB_C_SSRX_N	B11	I USB SS	USB SS		USB_C_SSRX_DN	MTK MT8371	SSUSB_RXN_P1	Receive signal differential pairs for SuperSpeed on port C
USB_C_SSRX_P	B10	I USB SS	USB SS		USB_C_SSRX_DP	MTK MT8371	SSUSB_RXP_P1	Receive signal differential pairs for SuperSpeed on port C
PCIe_A_HSI0_P	AB1	I LVDS PCIE			PCIe_A_HSI0_P	MTK MT8371	PCIE_RXP	Differential PCIe link A receive data pair
PCIe_A_HSI0_N	AB2	I LVDS PCIE			PCIe_A_HSI0_N	MTK MT8371	PCIE_RXN	Differential PCIe link A receive data pair
PCIe_A_HSO0_P	AC2	O LVDS PCIE			PCIe_A_HSO0_P	MTK MT8371	PCIE_TXP	Differential PCIe link A transmit data pair
PCIe_A_HSO0_N	AC3	O LVDS PCIE			PCIe_A_HSO0_N	MTK MT8371	PCIE_TXN	Differential PCIe link A transmit data pair
PCIe_CLKREQ#	W2	I OD CMOS	VCC_OUT_IO	PU 10k	PCIe_CLKREQ#	MTK MT8371	PCIE_CLKREQ	PCIe reference clock request
PCIe_A_PERST#	**V2**	O CMOS	VCC_OUT_IO		PCIe_A_PERST#	MTK MT8371	PCIE_PERESET	PCIe Port A reset output
PCIe_REFCLK_P	W1	O LVDS PCIE		PD 49.9 (MTK request)	PCIe_A_REFCLK_P	MTK MT8371	PCIE_CKP	Differential PCIe reference clock output
PCIe_REFCLK_N	Y1	O LVDS PCIE		PD 49.9 (MTK request)	PCIe_A_REFCLK_N	MTK MT8371	PCIE_CKN	Differential PCIe reference clock output
PCIe_WAKE#	T2	I OD CMOS	VCC_OUT_IO	PU 10k	PCIe_WAKE#	MTK MT8371	PCIE_WAKE	PCIe wake up interrupt to host – common to PCIe links A, B, C, D
PCIe_SMDAT	U1	I/O OD CMOS	VCC_OUT_IO	PU 2k2	PCIe_SMDAT	MTK MT8371	SDA3	System management I2C bus DATA
PCIe_SMCLK	T1	O OD CMOS	VCC_OUT_IO	PU 2k2	PCIe_SMCLK	MTK MT8371	SCL3	System management I2C bus CLK
PCIe_SM_ALERT#	R2	I OD CMOS	VCC_OUT_IO	PU 2k2	PCIE_SM_ALERT#	MTK MT8371	GPIO01	SMBus Alert# (interrupt) signal
DSI0_RST (Vendor Defined)	D6	O	1.8V		DSI_RST	MTK MT8371	DSI_LCM_RST	Defined by module manufacturer
VCC_IN_5V	Y25, Y26, Y27, Y28	P			VCC_IN_5V	Buck IC		Module power input voltage of 5V

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GND	A26, A29, A32, B27, B28, B30, B33, C25, C32, C35, D28, D34, F33, F35, G34, H32, J33, J35, K34, M35, N34, T34, W34, AA25, AA26, AA27, AA28, AA32, AB28, AB31, AB34, AC27, AC30, AC33	P			GND	MTK MT8371	DVSS	Module Signal and power return and GND reference
CSI_B_DATA0_N	L32	I LVDS D-PHY / I LVDS M-PHY			CSI_B_DATA0_N	MTK MT8371	CSI1A_L1N_T1A	CSI differential input (point to point)
CSI_B_DATA0_P	M33				CSI_B_DATA0_P	MTK MT8371	CSI1A_L1P_T0C	CSI differential input (point to point)
CSI_B_DATA1_N	N32				CSI_B_DATA1_N	MTK MT8371	CSI1B_L0N_T0B	CSI differential input (point to point)
CSI_B_DATA1_P	P32				CSI_B_DATA1_P	MTK MT8371	CSI1B_L0P_T0A	CSI differential input (point to point)
CSI_B_DATA2_N	P34				CSI_B_DATA2_N	MTK MT8371	CSI1A_L0N_T0B	CSI differential input (point to point)
CSI_B_DATA2_P	R33				CSI_B_DATA2_P	MTK MT8371	CSI1A_L0P_T0A	CSI differential input (point to point)
CSI_B_DATA3_N	T32				CSI_B_DATA3_N	MTK MT8371	CSI1B_L1N	CSI differential input (point to point)
CSI_B_DATA3_P	T33				CSI_B_DATA3_P	MTK MT8371	CSI1B_L1P_T0C	CSI differential input (point to point)
CSI_B_CLOCK_N	J32	I LVDS D-PHY			CSI_B_CLOCK_N	MTK MT8371	CSI1A_L2N_T1C	CSI differential clock input (point to point)
CSI_B_CLOCK_P	K33	I LVDS D-PHY			CSI_B_CLOCK_P	MTK MT8371	CSI1A_L2P_T1B	CSI differential clock input (point to point)
I2C_B_CAM_SDA / CSI_B_TX_N	AB26	I/O OD CMOS / O LVDS M-PHY	VCC_OUT_IO	PU 2k2	CAM_B_SDA	MTK MT8371	SDA8	I2C data for serial camera data support link or differential data lane
I2C_B_CAM_SCL / CSI_B_TX_P	AB25	I/O OD CMOS / O LVDS M-PHY	VCC_OUT_IO	PU 2k2	CAM_B_SCL	MTK MT8371	SCL8	I2C clock for serial camera data support link or differential data lane
CAM_B_PWR / GPIO_C_6	E3	O CMOS	VCC_OUT_IO		CAM_B_PWR	MTK MT8371	CMMPDN1	Camera 0 Power Enable, active high output.
CAM_B_RST# / GPIO_C_7	E4	O CMOS	VCC_OUT_IO		CAM_B_RST#	MTK MT8371	CMMRST1	Camera 0 reset, active low output

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GPIO_D_0	U32	I/O CMOS	1.8V		GPIO_D_0	MTK MT8371	SCL4	General purpose I/O Contact D0
GPIO_D_1	U33	I/O CMOS	1.8V		GPIO_D_1	MTK MT8371	SDA4	General purpose I/O Contact D1
GPIO_D_2	V32	I/O CMOS	1.8V		GPIO_D_2	MTK MT8371	SCL6	General purpose I/O Contact D2
GPIO_D_3	V33	I/O CMOS	1.8V		GPIO_D_3	MTK MT8371	SDA6	General purpose I/O Contact D3
SPI_C_SDI	C29	I CMOS	1.8V		SPI_C_MISO	MTK MT8371	SPIM2_MISO	SPI C Serial Data Input
SPI_C_SDO	D30	O CMOS	1.8V		SPI_C_MOSI	MTK MT8371	SPIM2_MOSI	SPI C Serial Data Output
SPI_C_CS0#	C30	O CMOS	1.8V		SPI_C_CS0#	MTK MT8371	SPIM2_CS	SPI C Master Chip Select 0
SPI_C_SCK	D29	O CMOS	1.8V		SPI_C_SCK	MTK MT8371	SPIM2_CLK	SPI C Serial Data Clock
USB_D_D_N	D26	I/O USB	USB		USB_D_DN	MTK MT8371	USB_DM_P2	USB differential data pairs for port D
USB_D_D_P	D25	I/O USB	USB		USB_D_DP	MTK MT8371	USB_DP_P2	USB differential data pairs for port D
USB_D_OC#	C28	I OD CMOS	VCC_OUT_IO	PU 10K	USB_D_OC_N	MTK MT8371	GPIO15	USB over-current for port D
USB_D_EN	C26	O CMOS	VCC_OUT_IO		USB_D_EN	MTK MT8371	USB2_DRV_VBUS	Power enable for USB VBUS voltage
eDP_A_LANE0_P	A30	O LVDS DP			eDP_A_LANE0_P	MTK MT8371	EDP_LN0_TXP	Primary 4-lane eDP differential pair data lines
eDP_A_LANE0_N	A31	O LVDS DP			eDP_A_LANE0_N	MTK MT8371	EDP_LN0_TXN	Primary 4-lane eDP differential pair data lines
eDP_A_LANE1_P	B31	O LVDS DP			eDP_A_LANE1_P	MTK MT8371	EDP_LN1_TXP	Primary 4-lane eDP differential pair data lines
eDP_A_LANE1_N	B32	O LVDS DP			eDP_A_LANE1_N	MTK MT8371	EDP_LN1_TXN	Primary 4-lane eDP differential pair data lines
eDP_A_LANE2_P	A33	O LVDS DP			eDP_A_LANE2_P	MTK MT8371	EDP_LN2_TXP	Primary 4-lane eDP differential pair data lines
eDP_A_LANE2_N	A34	O LVDS DP			eDP_A_LANE2_N	MTK MT8371	EDP_LN2_TXN	Primary 4-lane eDP differential pair data lines
eDP_A_LANE3_P	B34	O LVDS DP			eDP_A_LANE3_P	MTK MT8371	EDP_LN3_TXP	Primary 4-lane eDP differential pair data lines
eDP_A_LANE3_N	B35	O LVDS DP			eDP_A_LANE3_N	MTK MT8371	EDP_LN3_TXN	Primary 4-lane eDP differential pair data lines
eDP_A_AUX_P	C33	I/O LVDS DP	1.8V (HDMI)	PD 100k PU 2k2 (HDMI)	eDP_A_AUX_N	MTK MT8371	EDP_AUXN	Primary bidirectional eDP channel used for link management and device control
eDP_A_AUX_N	C34	I/O LVDS DP	1.8V (HDMI)	PD 100k PU 2k2 (HDMI)	eDP_A_AUX_P	MTK MT8371	EDP_AUXP	Primary bidirectional eDP channel used for link management and device control

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eDP_A_HPD	D33	I CMOS	VCC_OUT_IO	PD 1M	eDP_A_HPD	MTK MT8371	EDP_TX_HPD	Detection of Hot Plug / Unplug of primary eDP display and notification of the link layer.
eDP_A_BL_EN	D31	O CMOS	VCC_OUT_IO		eDP_A_BL_EN	MTK MT8371	GPIO05	Primary eDP panel backlight enable, active high
eDP_A_BL_PWM	C31	O CMOS	VCC_OUT_IO	PU 4k7 (HDMI)	eDP_A_PWM	MTK MT8371	DISP_PWM1	Primary eDP panel brightness control through pulse width modulation
eDP_B_LANE0_P	D35	O LVDS DP			DP_D0+	MTK MT8371	SSUSBDP_RXP_P2	Primary 4-lane eDP differential pair data lines
eDP_B_LANE0_N	E35	O LVDS DP			DP_D0-	MTK MT8371	SSUSBDP_RXN_P2	Primary 4-lane eDP differential pair data lines
eDP_B_LANE1_P	E34	O LVDS DP			DP_D1+	MTK MT8371	SSUSBDP_TXP_P2	Primary 4-lane eDP differential pair data lines
eDP_B_LANE1_N	F34	O LVDS DP			DP_D1-	MTK MT8371	SSUSBDP_TXN_P2	Primary 4-lane eDP differential pair data lines
eDP_B_LANE2_P	G35	O LVDS DP			DP_D2+	MTK MT8371	SSUSBDP_TXP_P1	Primary 4-lane eDP differential pair data lines
eDP_B_LANE2_N	H35	O LVDS DP			DP_D2-	MTK MT8371	SSUSBDP_TXN_P1	Primary 4-lane eDP differential pair data lines
eDP_B_LANE3_P	H34	O LVDS DP			DP_D3+	MTK MT8371	SSUSBDP_RXP_P1	Primary 4-lane eDP differential pair data lines
eDP_B_LANE3_N	J34	O LVDS DP			DP_D3-	MTK MT8371	SSUSBDP_RXN_P1	Primary 4-lane eDP differential pair data lines
eDP_B_AUX_P	G33	I/O LVDS DP		PD 100k	DP_AUX+	MTK MT8371	DP_SBU1	Secondary bidirectional eDP channel used for link management and device control
eDP_B_AUX_N	H33	I/O LVDS DP		PD 100k	DP_AUX-	MTK MT8371	DP_SBU2	Secondary bidirectional eDP channel used for link management and device control
eDP_B_HPD	G32	I CMOS	VCC_OUT_IO	PD 1M	DP_TX_HPD	MTK MT8371	DP_TX_HPD	Detection of Hot Plug / Unplug of secondary eDP display and notification of the link layer.
GND	K32, M32, R32				GND	MTK MT8371	DVSS	GND
VCC_IN_5V	AE4, AF4, AG4, AH3, AH4, AJ3, AJ4, AK4	P			VCC_IN_5V	Buck IC		Module power input voltage of 5V

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GND	AE2, AE34, AF35, AG3, AH2, AH34, AJ35, AK3, AL2, AL34, AM13, AM16, AM19, AM22, AM35, AN3, AN6, AN9, AN11, AN15, AN18, AN21, AN33, AP2, AP5, AP8, AP13, AP16, AP19, AP22, AP25, AP28, AP31, AP34, AR14, AR17, AR20, AR26, AR29, AR32	P			GND	MTK MT8371	DVSS	Module Signal and power return and GND reference
Vendor Defined	AM32	AO			AU_LOLN	MTK MT6365	AU_LOLN	Defined by module manufacturer (Audio Lineout)
Vendor Defined	AM33	AO			AU_LOLP	MTK MT6365	AU_LOLP	Defined by module manufacturer (Audio Lineout)

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4.4 Signal Description by Function

4.4.1 DSIO/LVDS

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name	Description
DSI_DATA0_N / LVDS_A_LANE0_N	AB11	O LVDS D-PHY			DSI_DATA0_N	MTK MT8371	DSI0_D0N_T1A	DSI differential output (point to point)
DSI_DATA0_P / LVDS_A_LANE0_P	AB10	O LVDS D-PHY			DSI_DATA0_P	MTK MT8371	DSI0_D0P_T0C	DSI differential output (point to point)
DSI_DATA1_N / LVDS_A_LANE1_N	AC9	O LVDS D-PHY			DSI_DATA1_N	MTK MT8371	DSI0_D1N_T2B	DSI differential output (point to point)
DSI_DATA1_P / LVDS_A_LANE1_P	AC8	O LVDS D-PHY			DSI_DATA1_P	MTK MT8371	DSI0_D1P_T2A	DSI differential output (point to point)
DSI_DATA2_N / LVDS_A_LANE2_N	AC6	O LVDS D-PHY			DSI_DATA2_N	MTK MT8371	DSI0_D2N_T0B	DSI differential output (point to point)
DSI_DATA2_P / LVDS_A_LANE2_P	AC5	O LVDS D-PHY			DSI_DATA2_P	MTK MT8371	DSI0_D2P_T0A	DSI differential output (point to point)
DSI_DATA3_N / LVDS_A_LANE3_N	AB5	O LVDS D-PHY			DSI_DATA3_N	MTK MT8371	DSI0_D3N	DSI differential output (point to point)
DSI_DATA3_P / LVDS_A_LANE3_P	AB4	O LVDS D-PHY			DSI_DATA3_P	MTK MT8371	DSI0_D3P_T2C	DSI differential output (point to point)
DSI_CLOCK_N / LVDS_A_CLK_N	AB8	O LVDS D-PHY			DSI_CLOCK_N	MTK MT8371	DSI0_CKN_T1C	DSI differential clock output (point to point)
DSI_CLOCK_P / LVDS_A_CLK_P	AB7	O LVDS D-PHY			DSI_CLOCK_P	MTK MT8371	DSI0_CKP_T1B	DSI differential clock output (point to point)
DSI_TE	AA3	I CMOS	VCC_OUT_IO		DSI_TE	MTK MT8371	DSI0_DSI_TE	DSI panel tearing effect signal
DSI0_RST (Vendor Defined)	D6	O	1.8V		DSI_RST	MTK MT8371	DSI_LCM_RST	Defined by module manufacturer

Note: LVDS/MIPI DSI pin sharing

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4.4.2 DP

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name	Description
eDP_B_LANE0_P	D35	O LVDS DP			DP_D0+	MTK MT8371	SSUSBDP_RXP_P2	Primary 4-lane eDP differential pair data lines
eDP_B_LANE0_N	E35	O LVDS DP			DP_D0-	MTK MT8371	SSUSBDP_RXN_P2	Primary 4-lane eDP differential pair data lines
eDP_B_LANE1_P	E34	O LVDS DP			DP_D1+	MTK MT8371	SSUSBDP_TXP_P2	Primary 4-lane eDP differential pair data lines
eDP_B_LANE1_N	F34	O LVDS DP			DP_D1-	MTK MT8371	SSUSBDP_TXN_P2	Primary 4-lane eDP differential pair data lines
eDP_B_LANE2_P	G35	O LVDS DP			DP_D2+	MTK MT8371	SSUSBDP_TXP_P1	Primary 4-lane eDP differential pair data lines
eDP_B_LANE2_N	H35	O LVDS DP			DP_D2-	MTK MT8371	SSUSBDP_TXN_P1	Primary 4-lane eDP differential pair data lines
eDP_B_LANE3_P	H34	O LVDS DP			DP_D3+	MTK MT8371	SSUSBDP_RXP_P1	Primary 4-lane eDP differential pair data lines
eDP_B_LANE3_N	J34	O LVDS DP			DP_D3-	MTK MT8371	SSUSBDP_RXN_P1	Primary 4-lane eDP differential pair data lines
eDP_B_AUX_P	G33	I/O LVDS DP		PD 100k	DP_AUX+	MTK MT8371	DP_SBU1	Secondary bidirectional eDP channel used for link management and device control
eDP_B_AUX_N	H33	I/O LVDS DP		PD 100k	DP_AUX-	MTK MT8371	DP_SBU2	Secondary bidirectional eDP channel used for link management and device control
eDP_B_HPD	G32	I CMOS	VCC_OUT_IO	PD 1M	DP_TX_HPD	MTK MT8371	DP_TX_HPD	Detection of Hot Plug / Unplug of secondary eDP display and notification of the link layer.

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4.4.3 eDP

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name	Description
eDP_A_LANE0_P	A30	O LVDS DP			eDP_A_LANE0_P	MTK MT8371	EDP_LN0_TXP	Primary 4-lane eDP differential pair data lines
eDP_A_LANE0_N	A31	O LVDS DP			eDP_A_LANE0_N	MTK MT8371	EDP_LN0_TXN	Primary 4-lane eDP differential pair data lines
eDP_A_LANE1_P	B31	O LVDS DP			eDP_A_LANE1_P	MTK MT8371	EDP_LN1_TXP	Primary 4-lane eDP differential pair data lines
eDP_A_LANE1_N	B32	O LVDS DP			eDP_A_LANE1_N	MTK MT8371	EDP_LN1_TXN	Primary 4-lane eDP differential pair data lines
eDP_A_LANE2_P	A33	O LVDS DP			eDP_A_LANE2_P	MTK MT8371	EDP_LN2_TXP	Primary 4-lane eDP differential pair data lines
eDP_A_LANE2_N	A34	O LVDS DP			eDP_A_LANE2_N	MTK MT8371	EDP_LN2_TXN	Primary 4-lane eDP differential pair data lines
eDP_A_LANE3_P	B34	O LVDS DP			eDP_A_LANE3_P	MTK MT8371	EDP_LN3_TXP	Primary 4-lane eDP differential pair data lines
eDP_A_LANE3_N	B35	O LVDS DP			eDP_A_LANE3_N	MTK MT8371	EDP_LN3_TXN	Primary 4-lane eDP differential pair data lines
eDP_A_AUX_P	C33	I/O LVDS DP	1.8V (HDMI)	PD 100k PU 2k2 (HDMI)	eDP_A_AUX_N	MTK MT8371	EDP_AUXN	Primary bidirectional eDP channel used for link management and device control
eDP_A_AUX_N	C34	I/O LVDS DP	1.8V (HDMI)	PD 100k PU 2k2 (HDMI)	eDP_A_AUX_P	MTK MT8371	EDP_AUXP	Primary bidirectional eDP channel used for link management and device control
eDP_A_HPD	D33	I CMOS	VCC_OUT_IO	PD 1M	eDP_A_HPD	MTK MT8371	EDP_TX_HPD	Detection of Hot Plug / Unplug of primary eDP display and notification of the link layer.
eDP_A_BL_EN	D31	O CMOS	VCC_OUT_IO		eDP_A_BL_EN	MTK MT8371	GPIO05	Primary eDP panel backlight enable, active high
eDP_A_BL_PWM	C31	O CMOS	VCC_OUT_IO	PU 4k7 (HDMI)	eDP_A_PWM	MTK MT8371	DISP_PWM1	Primary eDP panel brightness control through pulse width modulation

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4.4.4 Camera

4.4.4.1 CSI_A (4 Lanes)

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name	Description
CSI_A_DATA0_N	C1	I LVDS D-PHY / I LVDS M-PHY			CSI_A_DATA0_N	MTK MT8371	CSI0A_L1N_T1A	CSI differential input (point to point)
CSI_A_DATA0_P	B1				CSI_A_DATA0_P	MTK MT8371	CSI0A_L1P_T0C	CSI differential input (point to point)
CSI_A_DATA1_N	A2				CSI_A_DATA1_N	MTK MT8371	CSI0B_L0N_T0B	CSI differential input (point to point)
CSI_A_DATA1_P	A3				CSI_A_DATA1_P	MTK MT8371	CSI0B_L0P_T0A	CSI differential input (point to point)
CSI_A_DATA2_N	A5				CSI_A_DATA2_N	MTK MT8371	CSI0A_L0N_T0A	CSI differential input (point to point)
CSI_A_DATA2_P	A6				CSI_A_DATA2_P	MTK MT8371	CSI0A_L0P_T0B	CSI differential input (point to point)
CSI_A_DATA3_N	B6				CSI_A_DATA3_N	MTK MT8371	CSI0B_L1N_T1A	CSI differential input (point to point)
CSI_A_DATA3_P	B7				CSI_A_DATA3_P	MTK MT8371	CSI0B_L1P_T0C	CSI differential input (point to point)
CSI_A_CLOCK_N	B3	I LVDS D-PHY			CSI_A_CLOCK_N	MTK MT8371	CSI0A_L2N_T1C	CSI differential clock input (point to point)
CSI_A_CLOCK_P	B4	I LVDS D-PHY			CSI_A_CLOCK_P	MTK MT8371	CSI0A_L2P_T1B	CSI differential clock input (point to point)

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4.4.4.2 CSI_B (4 Lanes)

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name	Description
CSI_B_DATA0_N	L32	I LVDS D-PHY / I LVDS M-PHY			CSI_B_DATA0_N	MTK MT8371	CSI1A_L1N_T1A	CSI differential input (point to point)
CSI_B_DATA0_P	M33				CSI_B_DATA0_P	MTK MT8371	CSI1A_L1P_T0C	CSI differential input (point to point)
CSI_B_DATA1_N	N32				CSI_B_DATA1_N	MTK MT8371	CSI1B_L0N_T0B	CSI differential input (point to point)
CSI_B_DATA1_P	P32				CSI_B_DATA1_P	MTK MT8371	CSI1B_L0P_T0A	CSI differential input (point to point)
CSI_B_DATA2_N	P34				CSI_B_DATA2_N	MTK MT8371	CSI1A_L0N_T0B	CSI differential input (point to point)
CSI_B_DATA2_P	R33				CSI_B_DATA2_P	MTK MT8371	CSI1A_L0P_T0A	CSI differential input (point to point)
CSI_B_DATA3_N	T32				CSI_B_DATA3_N	MTK MT8371	CSI1B_L1N	CSI differential input (point to point)
CSI_B_DATA3_P	T33				CSI_B_DATA3_P	MTK MT8371	CSI1B_L1P_T0C	CSI differential input (point to point)
CSI_B_CLOCK_N	J32	I LVDS D-PHY			CSI_B_CLOCK_N	MTK MT8371	CSI1A_L2N_T1C	CSI differential clock input (point to point)
CSI_B_CLOCK_P	K33	I LVDS D-PHY			CSI_B_CLOCK_P	MTK MT8371	CSI1A_L2P_T1B	CSI differential clock input (point to point)

4.4.5 Audio Interfaces

4.4.5.1 I2S

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name	Description
I2S_B_LRCLK	T18	O CMOS	VCC_OUT_IO		I2S_B_LRCLK	MTK MT8371	DMIC1_CLK	Reset output from CPU to reset peripherals on Carrier.
I2S_A_DATA_IN	V21	I/O CMOS	VCC_OUT_IO		I2S_A_DATA_IN	MTK MT8371	I2SIN0_DI	I2S A Digital audio Input
I2S_A_DATA_OUT	W21				I2S_A_DATA_OUT	MTK MT8371	I2SOUT0_DO	I2S A Digital audio Output
I2S_B_DATA_IN	V19				I2S_B_DATA_IN	MTK MT8371	DMIC1_DAT0	I2S B Digital audio Input
I2S_B_DATA_OUT	W19				I2S_B_DATA_OUT	MTK MT8371	GPIO11	I2S B Digital audio Output
I2S_MCLK	V18				I2S_MCLK	MTK MT8371	I2SIN0_MCK	Master clock output to I2S codec(s)
I2S_A_LRCLK	W18				I2S_A_LRCLK	MTK MT8371	I2SIN0_LRCK	I2S Left & Right synchronization clock

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I2S_A_BITCLK	W20				I2S_A_BITCLK	MTK MT8371	I2SIN0_BCK	I2S Digital audio clock
I2S_B_BITCLK	T19				I2S_B_BITCLK	MTK MT8371	DMIC0_DAT0	

4.4.6 LAN Port

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name	Description
ETH_A_(R)(G)MII_COL	F15	I CMOS			GBE_COL	MTK MT8371	GBE_COL	Collision detect (half speed only) port A
ETH_A_(S)(R)(G)MII_TXD0	H15	O CMOS			ETH_A_RGMII_TXD0	MTK MT8371	GBE_TXD0	Transmit data bit 0 (transmitted first) port A
ETH_A_(S)(R)(G)MII_TXD1	G15	O CMOS			ETH_A_RGMII_TXD1	MTK MT8371	GBE_TXD1	Transmit data bit 1 port A
ETH_A_(S)(R)(G)MII_TXD2	H16	O CMOS			ETH_A_RGMII_TXD2	MTK MT8371	GBE_TXD2	Transmit data bit 2 port A
ETH_A_(S)(R)(G)MII_TXD3	G16	O CMOS			ETH_A_RGMII_TXD3	MTK MT8371	GBE_TXD3	Transmit data bit 3 port A
ETH_A_(R)(G)MII_TX_EN(_ER)	K16	O CMOS			ETH_A_RGMII_TX_EN	MTK MT8371	GBE_TXEN	Transmit enable (Error) port A
ETH_A_(R)(G)MII_TX_CLK	J15	I/O CMOS			ETH_A_RGMII_TX_CLK	MTK MT8371	GBE_TXC	Transmit clock port A
ETH_A_(S)(R)(G)MII_RXD0	K15	I CMOS			ETH_A_RGMII_RXD0	MTK MT8371	GBE_RXD0	Receive data bit 0 (received first) port A
ETH_A_(S)(R)(G)MII_RXD1	L15	I CMOS			ETH_A_RGMII_RXD1	MTK MT8371	GBE_RXD1	Receive data bit 1 port A
ETH_A_(R)(G)MII_RXD2	N15	I CMOS			ETH_A_RGMII_RXD2	MTK MT8371	GBE_RXD2	Receive data bit 2 port A
ETH_A_(R)(G)MII_RXD3	P15	I CMOS			ETH_A_RGMII_RXD3	MTK MT8371	GBE_RXD3	Receive data bit 3 port A
ETH_A_(R)(G)MII_RX_ER	L16	I CMOS			ETH_A_RGMII_RX_ER	MTK MT8371	GBE_RXER	Receive error port A
ETH_A_(R)(G)MII_RX_DV(_ER)	M15	I CMOS			ETH_A_RGMII_RX_DV	MTK MT8371	GBE_RXDV	Receive data valid port A
ETH_A_(R)(G)MII_RX_CLK	R15	I/O CMOS			ETH_A_RGMII_RX_CLK	MTK MT8371	GBE_RXC	Receive clock port A
ETH_MDIO	T15	I/O CMOS			ETH_A_MDIO	MTK MT8371	GBE_MIO	Management bus data signal for Ethernet
ETH_MDC	T16	O CMOS			ETH_A_MDC	MTK MT8371	GBE_MDC	Management bus clock signal for Ethernet
ETH_IOPWR	M17	PO			VIO18_PMU	MTK MT6365	VIO18	ETH voltage. It is used to provide the IO Voltage Level for all Ethernet interfaces.

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4.4.7 USB Ports

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name	Description
USB_A_D_N	AB13	I/O USB	USB		USB_A_DN	MTK MT8371	USB_DM_P0	USB differential data pairs for port A
USB_A_D_P	AC14	I/O USB	USB		USB_A_DP	MTK MT8371	USB_DP_P0	USB differential data pairs for port A
USB_A_ID	AB14	I OD CMOS	VCC_OUT_IO	PU 10k	USB_A_ID	MTK MT8371	USB0_IDDIG	Input Contact to announce OTG device insertion on USB 2.0 port
USB_A_OC#	AC15	I OD CMOS	VCC_OUT_IO	PU 10k	USB_A_OC_N	MTK MT8371	KPCOL1	USB over-current for port A
USB_A_VBUS	AB16	I USB VBUS 5V	5V		USB_A_VBUS	MTK MT8371	USB0_VBUS_VALID	USB port 0 port power detection
USB_A_EN	AC16	O CMOS	VCC_OUT_IO		USB_A_EN	MTK MT8371	USB0_DRV_VBUS	Power enable for USB VBUS voltage
USB_B_D_N	AB23	I/O USB	USB		USB_B_DN	MTK MT8371	USB_DM_P1	USB differential data pairs for port B
USB_B_D_P	AC22	I/O USB	USB		USB_B_DP	MTK MT8371	USB_DP_P1	USB differential data pairs for port B
USB_B_OC#	AC21	I OD CMOS	1.8V	PU 10k	USB_B_OC_N	MTK MT8371	KPROW0	USB over-current for port B
USB_B_EN	AC20	O CMOS	1.8V		USB_B_EN	MTK MT8371	USB1_DRV_VBUS	Power enable for USB VBUS voltage
USB_C_D_N	D11	I/O USB	USB		USB_C_DN	MTK MT8371	USB_DM_P3	USB differential data pairs for port C
USB_C_D_P	D10	I/O USB	USB		USB_C_DP	MTK MT8371	USB_DP_P3	USB differential data pairs for port C
USB_C_OC#	C8	I OD CMOS	VCC_OUT_IO	PU 10K	USB_C_OC_N	MTK MT8371	I2SOUT0_MCK	USB over-current for port C
USB_C_EN	C10	O CMOS	VCC_OUT_IO		USB_C_EN	MTK MT8371	USB3_DRV_VBUS	Power enable for USB VBUS voltage
USB_C_SSTX_N	A9	O USB SS	USB SS		USB_C_SSTX_DN	MTK MT8371	SSUSB_TXN_P1	Transmit signal differential pairs for SuperSpeed on port C
USB_C_SSTX_P	A8	O USB SS	USB SS		USB_C_SSTX_DP	MTK MT8371	SSUSB_TXP_P1	Transmit signal differential pairs for SuperSpeed on port C
USB_C_SSRX_N	B11	I USB SS	USB SS		USB_C_SSRX_DN	MTK MT8371	SSUSB_RXN_P1	Receive signal differential pairs for SuperSpeed on port C
USB_C_SSRX_P	B10	I USB SS	USB SS		USB_C_SSRX_DP	MTK MT8371	SSUSB_RXP_P1	Receive signal differential pairs for SuperSpeed on port C
USB_D_D_N	D26	I/O USB	USB		USB_D_DN	MTK MT8371	USB_DM_P2	USB differential data pairs for port D
USB_D_D_P	D25	I/O USB	USB		USB_D_DP	MTK MT8371	USB_DP_P2	USB differential data pairs for port D
USB_D_OC#	C28	I OD CMOS	VCC_OUT_IO	PU 10K	USB_D_OC_N	MTK MT8371	GPIO15	USB over-current for port D
USB_D_EN	C26	O CMOS	VCC_OUT_IO		USB_D_EN	MTK MT8371	USB2_DRV_VBUS	Power enable for USB VBUS voltage

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4.4.8 PCIe

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name	Description
PCIe_A_HSI0_P	AB1	I LVDS PCIE			PCIe_A_HSI0_P	MTK MT8371	PCIE_RXP	Differential PCIe link A receive data pair
PCIe_A_HSI0_N	AB2	I LVDS PCIE			PCIe_A_HSI0_N	MTK MT8371	PCIE_RXN	Differential PCIe link A receive data pair
PCIe_A_HSO0_P	AC2	O LVDS PCIE			PCIe_A_HSO0_P	MTK MT8371	PCIE_TXP	Differential PCIe link A transmit data pair
PCIe_A_HSO0_N	AC3	O LVDS PCIE			PCIe_A_HSO0_N	MTK MT8371	PCIE_TXN	Differential PCIe link A transmit data pair
PCIe_CLKREQ#	W2	I OD CMOS	VCC_OUT_IO	PU 10k	PCIe_CLKREQ#	MTK MT8371	PCIE_CLKREQ	PCIe reference clock request
PCIe_A_PERST#	**V2**	O CMOS	VCC_OUT_IO		PCIe_A_PERST#	MTK MT8371	PCIE_PERESET	PCIe Port A reset output
PCIe_REFCLK_P	W1	O LVDS PCIE		PD 49.9 (MTK request)	PCIe_A_REFCLK_P	MTK MT8371	PCIE_CKP	Differential PCIe reference clock output
PCIe_REFCLK_N	Y1	O LVDS PCIE		PD 49.9 (MTK request)	PCIe_A_REFCLK_N	MTK MT8371	PCIE_CKN	Differential PCIe reference clock output
PCIe_WAKE#	T2	I OD CMOS	VCC_OUT_IO	PU 10k	PCIe_WAKE#	MTK MT8371	PCIE_WAKE	PCIe wake up interrupt to host – common to PCIe links A, B, C, D
PCIe_SMDAT	U1	I/O OD CMOS	VCC_OUT_IO	PU 2k2	PCIe_SMDAT	MTK MT8371	SDA3	System management I2C bus DATA
PCIe_SMCLK	T1	O OD CMOS	VCC_OUT_IO	PU 2k2	PCIe_SMCLK	MTK MT8371	SCL3	System management I2C bus CLK
PCIe_SM_ALERT#	R2	I OD CMOS	VCC_OUT_IO	PU 2k2	PCIE_SM_ALERT#	MTK MT8371	GPIO01	SMBus Alert# (interrupt) signal

4.4.9 SDIO

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name	Description
SDIO_A_CMD	E20	I/O CMOS	1.8V / 3.3V		SDIO_A_CMD	MTK MT8371	MSDC1_CMD	SDIO A Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.

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SDIO_A_CLK	F21	O CMOS			SDIO_A_CLK	MTK MT8371	MSDC1_CLK	SDIO A Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.
SDIO_A_D0	G20	I/O CMOS			SDIO_A_DAT0	MTK MT8371	MSDC1_DAT0	SDIO A Data lines. These signals operate in push-pull mode.
SDIO_A_D1	G21	I/O CMOS			SDIO_A_DAT1	MTK MT8371	MSDC1_DAT1	SDIO A Data lines. These signals operate in push-pull mode.
SDIO_A_D2	H20	I/O CMOS			SDIO_A_DAT2	MTK MT8371	MSDC1_DAT2	SDIO A Data lines. These signals operate in push-pull mode.
SDIO_A_D3	H21	I/O CMOS			SDIO_A_DAT3	MTK MT8371	MSDC1_DAT3	SDIO A Data lines. These signals operate in push-pull mode.
SDIO_A_CD#	J21	I OD CMOS		PU 10K	SDIO_A_CD#	MTK MT8371	GPIO03	SDIO A Card Detect. This signal indicates when a SDIO/MMC card is present.
SDIO_A_PWR_EN	D21	O CMOS			SDIO_A_PWR_EN	MTK MT8371	GPIO04	SDIO A Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.
SDIO_A_IOPWR	C20	PO			VSIM1_PMU	MTK MT6365	VSIM1	SDIO A Voltage. It is used to provide the IO Voltage Level
SDIO_B_CLK	K20	O CMOS			SDIO_B_CLK	MTK MT8371	MSDC2_CLK	SDIO B Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.
SDIO_B_CMD	K21	I/O CMOS			SDIO_B_CMD	MTK MT8371	MSDC2_CMD	SDIO B Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.
SDIO_B_D0	L20	I/O CMOS			SDIO_B_DAT0	MTK MT8371	MSDC2_DAT0	SDIO B Data lines. These signals operate in push-pull mode.
SDIO_B_D1	L21	I/O CMOS			SDIO_B_DAT1	MTK MT8371	MSDC2_DAT1	SDIO B Data lines. These signals operate in push-pull mode.
SDIO_B_D2	M21	I/O CMOS			SDIO_B_DAT2	MTK MT8371	MSDC2_DAT2	SDIO B Data lines. These signals operate in push-pull mode.
SDIO_B_D3	N20	I/O CMOS			SDIO_B_DAT3	MTK MT8371	MSDC2_DAT3	SDIO B Data lines. These signals operate in push-pull mode.
SDIO_B_IOPWR	T20	PO			VIO18_PMU	MTK MT6365	VIO18	SDIO B Voltage. It is used to provide the IO Voltage Level

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4.4.10 SPI Interfaces

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name	Description
SPI_A_SDI_(IO0)	U15	I/O CMOS	VCC_OUT_IO		SPI_A_MISO	MTK MT8371	SPIM0_MISO	SPI A Serial Data Input
SPI_A_SDO_(IO1)	V15	I/O CMOS			SPI_A_MOSI	MTK MT8371	SPIM0_MOSI	SPI A Serial Data Output
SPI_A_CS0#	Y15	O CMOS			SPI_A_CS0#	MTK MT8371	SPIM0_CS	SPI A Master Chip Select 0
SPI_A_SCK	U16	O CMOS			SPI_A_SCK	MTK MT8371	SPIM0_CLK	SPI A Serial Data Clock
SPI_B_SDI	Y22	I CMOS			SPI_B_MISO	MTK MT8371	SPIM1_MISO	SPI B Serial Data Input
SPI_B_SDO	Y23	O CMOS			SPI_B_MOSI	MTK MT8371	SPIM1_MOSI	SPI B Serial Data Output
SPI_B_CS0#	AA23	O CMOS			SPI_B_CS0#	MTK MT8371	SPIM1_CS	SPI B Master Chip Select 0
SPI_B_SCK	Y21	O CMOS			SPI_B_SCK	MTK MT8371	SPIM1_CLK	SPI B Serial Data Clock
SPI_C_SDI	C29	I CMOS	1.8V		SPI_C_MISO	MTK MT8371	SPIM2_MISO	SPI C Serial Data Input
SPI_C_SDO	D30	O CMOS	1.8V		SPI_C_MOSI	MTK MT8371	SPIM2_MOSI	SPI C Serial Data Output
SPI_C_CS0#	C30	O CMOS	1.8V		SPI_C_CS0#	MTK MT8371	SPIM2_CS	SPI C Master Chip Select 0
SPI_C_SCK	D29	O CMOS	1.8V		SPI_C_SCK	MTK MT8371	SPIM2_CLK	SPI C Serial Data Clock

4.4.11 I2C

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name	Description
I2C_A_SCL	AA15	I/O OD CMOS	VCC_OUT_IO, Size-0 only 1.8V, >Size-0	PU 2k2	I2C_A_SCL	MTK MT8371	SCP_SCL0	I2C Port A Clock Signal
I2C_A_SDA	AA16				I2C_A_SDA	MTK MT8371	SCP_SDA0	I2C Port A Data Signal
I2C_B_SCL	AA20				I2C_B_SCL	MTK MT8371	SCP_SCL1	I2C Port B Clock Signal
I2C_B_SDA	AA21				I2C_B_SDA	MTK MT8371	SCP_SDA1	I2C Port B Data Signal
I2C_A_CAM_SDA / CSI_A_TX_N	C3	I/O OD CMOS / O LVDS M-PHY	VCC_OUT_IO	PU 2k2	CAM_A_SDA	MTK MT8371	SDA7	I2C data for serial camera data support link or differential data lane
I2C_A_CAM_SCL / CSI_A_TX_P	C4	I/O OD CMOS / O LVDS M-PHY	VCC_OUT_IO	PU 2k2	CAM_A_SCL	MTK MT8371	SCL7	I2C clock for serial camera data support link or differential data lane
PCIe_SMDAT	U1	I/O OD CMOS	VCC_OUT_IO	PU 2k2	PCIe_SMDAT	MTK MT8371	SDA3	System management I2C bus DATA

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PCIe_SMCLK	T1	O OD CMOS	VCC_OUT_IO	PU 2k2	PCIe_SMCLK	MTK MT8371	SCL3	System management I2C bus CLK
I2C_B_CAM_SDA / CSI_B_TX_N	AB26	I/O OD CMOS / O LVDS M-PHY	VCC_OUT_IO	PU 2k2	CAM_B_SDA	MTK MT8371	SDA8	I2C data for serial camera data support link or differential data lane
I2C_B_CAM_SCL / CSI_B_TX_P	AB25	I/O OD CMOS / O LVDS M-PHY	VCC_OUT_IO	PU 2k2	CAM_B_SCL	MTK MT8371	SCL8	I2C clock for serial camera data support link or differential data lane

4.4.12 GPIO

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name	Description
GPIO_A_0	D17	I/O CMOS	VCC_OUT_IO		GPIO_A_0	MTK MT8371	GPIO06	General purpose I/O Contact A0
GPIO_A_1	E17				GPIO_A_1	MTK MT8371	GPIO07	General purpose I/O Contact A1
GPIO_A_2	F17				GPIO_A_2	MTK MT8371	GPIO08	General purpose I/O Contact A2
GPIO_A_3	G17				GPIO_A_3	MTK MT8371	GPIO09	General purpose I/O Contact A3
GPIO_A_4	H17				ETH_A_RGMII_TX_ER	MTK MT8371	GBE_TXER	General purpose I/O Contact A4
GPIO_A_5	J17				GBE_INTR	MTK MT8371	GBE_INTR	General purpose I/O Contact A5
GPIO_B_0	D19				GPIO_B_0	MTK MT8371	KPROW1	General purpose I/O Contact B0
GPIO_B_1	E19				GPIO_B_1	MTK MT8371	GPIO12	General purpose I/O Contact B1
GPIO_B_2	F19				GPIO_B_2	MTK MT8371	GPIO14	General purpose I/O Contact B2
GPIO_B_3	G19				GPIO_B_3	MTK MT8371	PCM_CLK	General purpose I/O Contact B3
GPIO_B_4	H19				GPIO_B_4	MTK MT8371	PCM_SYNC	General purpose I/O Contact B4
GPIO_B_5	J19				GPIO_B_5	MTK MT8371	PCM_DO	General purpose I/O Contact B5
GPIO_B_6	K19				GPIO_B_6	MTK MT8371	PCM_DI	General purpose I/O Contact B6
GPIO_B_7	L19				GPIO_B_7	MTK MT8371	CMMCLK1	General purpose I/O Contact B7
GPIO_C_0	D3	I/O CMOS	VCC_OUT_IO		GPIO_C_0	MTK MT8371	DMIC0_CLK	General purpose I/O Contact C0
GPIO_C_1	D4	I/O CMOS			GPIO_C_1	MTK MT8371	CMMCLK2	General purpose I/O Contact C1
DISP_VDD_EN / GPIO_C_4	F3	I/O CMOS			DISP_VDD_EN	MTK MT8371	GPIO02	General purpose I/O Contact C4
DISP_BL_EN / GPIO_C_5	F4	I/O CMOS			DISP_BL_EN	MTK MT8371	GPIO13	General purpose I/O Contact C5
GPIO_D_0	U32	I/O CMOS	1.8V		GPIO_D_0	MTK MT8371	SCL4	General purpose I/O Contact D0

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GPIO_D_1	U33	I/O CMOS	1.8V		GPIO_D_1	MTK MT8371	SDA4	General purpose I/O Contact D1
GPIO_D_2	V32	I/O CMOS	1.8V		GPIO_D_2	MTK MT8371	SCL6	General purpose I/O Contact D2
GPIO_D_3	V33	I/O CMOS	1.8V		GPIO_D_3	MTK MT8371	SDA6	General purpose I/O Contact D3

4.4.13 UART

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name	Description
UART_A_RX	A14	I CMOS	VCC_OUT_IO		UART_A_RX	MTK MT8371	UART2_RXD	Asynchronous serial data input port A
UART_A_TX	B13	O CMOS			UART_A_TX	MTK MT8371	UART2_TXD	Asynchronous serial data output port A
UART_A_RTS	C13	O CMOS			UART_A_RTS	MTK MT8371	GPIO17	Request to Send handshake line for port A
UART_A_CTS	C14	I CMOS			UART_A_CTS	MTK MT8371	GPIO16	Clear to Send handshake line for port A
UART_C_RX	A22	I CMOS	VCC_OUT_IO		UART_C_RX	MTK MT8371	UART1_RXD	Asynchronous serial data input port C
UART_C_TX	B23	O CMOS			UART_C_TX	MTK MT8371	UART1_TXD	Asynchronous serial data output port C
UART_D_RX	C22	I CMOS	VCC_OUT_IO		UART_D_RX	MTK MT8371	UART3_RXD	Asynchronous serial data input port D
UART_D_TX	C23	O CMOS			UART_D_TX	MTK MT8371	UART3_TXD	Asynchronous serial data output port D
UART_CON_RX	D22	I CMOS	VCC_OUT_IO		UART_CON_RX	MTK MT8371	UART0_RXD	Asynchronous serial data input port console
UART_CON_TX	D23	O CMOS			UART_CON_TX	MTK MT8371	UART0_TXD	Asynchronous serial data output port console

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4.4.14 Power + Boot Select

Contact Name	Contact Acronym	I/O Type	I/O Level	PU/PD	Net Name of Module	Controller	Controller Pin Name	Description
GND	D18, E15, E21, F16, F20, J16, J20, L18, M16, M20, P18, R16, R20, V16, V20, Y18, AA14, AA17, AA19, AA22, AB15, AB21	P			GND			Module Signal and power return and GND reference
RESET_OUT#	Y14	O CMOS	VCC_OUT_IO		OSM_nRST_OUT	Logic IC		
CARRIER_STBY#	Y13				CARRIER_STBY#	Logic IC		
RESET_IN#	U17	I OD CMOS	VCC_OUT_IO	PU 10K	OSM_nRST_IN	Logic IC		Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise.
CARRIER_PWR_EN	V17	O CMOS	VCC_OUT_IO		CARRIER_PWR_EN	Logic IC		Carrier board circuits should not be powered up until the module asserts the CARRIER_PWR_EN signal.
VCC_OUT_IO	U18	P	1.8V / 3.3V		VIO18_PMU	MTK MT6365	VIO18	Can provide IO voltage level for several interfaces to connect
RTC_PWR	W17	P			VRTC_PWR	MTK MT6365	VRTC28	Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based Lithium cell or Super Cap.
BOOT_SEL0#	U19	I OD CMOS	VCC_OUT_IO	PU 10K	BOOT_SEL0#	Logic IC		
BOOT_SEL1#	R18	I OD CMOS	VCC_OUT_IO	PU 10K	BOOT_SEL1#	Logic IC		
FORCE_RECOVERY#	T17	I OD CMOS	VCC_OUT_IO	PU 10K	FORCE_RECOVERY#	MTK MT8371	KPCOL0	If low on carrier board module enters recovery mode.

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GND	A4, A7, A10, B2, B5, B8, B9, C11, D1, D5, D8, E2, H2, H4, L2, L4, P2, P4, R1, U2, U4, V1, W3, Y2, AA1, AA4, AA7, AA8, AA10, AA11, AB3, AB6, AB9, AC4, AC7, AC10	P			GND	MTK MT8371	DVSS	Module Signal and power return and GND reference
PWR_BTN#	AA9	I OD CMOS	1.8 to 5V	PU 10K	PWR_BTN#	MTK MT6365	PWRKEY	Power-button input from Carrier board. Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module.
VCC_IN_5V	Y25, Y26, Y27, Y28	P			VCC_IN_5V	Buck IC		Module power input voltage of 5V
GND	A26, A29, A32, B27, B28, B30, B33, C25, C32, C35, D28, D34, F33, F35, G34, H32, J33, J35, K34, M35, N34, T34, W34, AA25, AA26, AA27, AA28, AA32, AB28, AB31, AB34, AC27, AC30, AC33	P			GND	MTK MT8371	DVSS	Module Signal and power return and GND reference
GND	K32, M32, R32				GND	MTK MT8371	DVSS	GND

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VCC_IN_5V	AE4, AF4, AG4, AH3, AH4, AJ3, AJ4, AK4	P			VCC_IN_5V	Buck IC		Module power input voltage of 5V
GND	AE2, AE34, AF35, AG3, AH2, AH34, AJ35, AK3, AL2, AL34, AM13, AM16, AM19, AM22, AM35, AN3, AN6, AN9, AN11, AN15, AN18, AN21, AN33, AP2, AP5, AP8, AP13, AP16, AP19, AP22, AP25, AP28, AP31, AP34, AR14, AR17, AR20, AR26, AR29, AR32	P			GND	MTK MT8371	DVSS	Module Signal and power return and GND reference

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5. Software Support

5.1 Yocto

Yocto is the main OS supplied for this product, this is based upon the MediaTek Genio releases

MediaTek Releases > https://mediatek.gitlab.io/aiot/doc/aiot-dev-guide/master/

ADLINK Releases > https://github.com/ADLINK/meta-adlink-mtk

5.2 Canonical Ubuntu

Ubuntu will be supported in a later stage on this platform, based upon the official Canonical/MediaTek releases

https://ubuntu.com/download/mediatek-genio

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6. Mechanical

6.1 Module Dimensions

The module must be OSM-L size (45 × 45 mm).

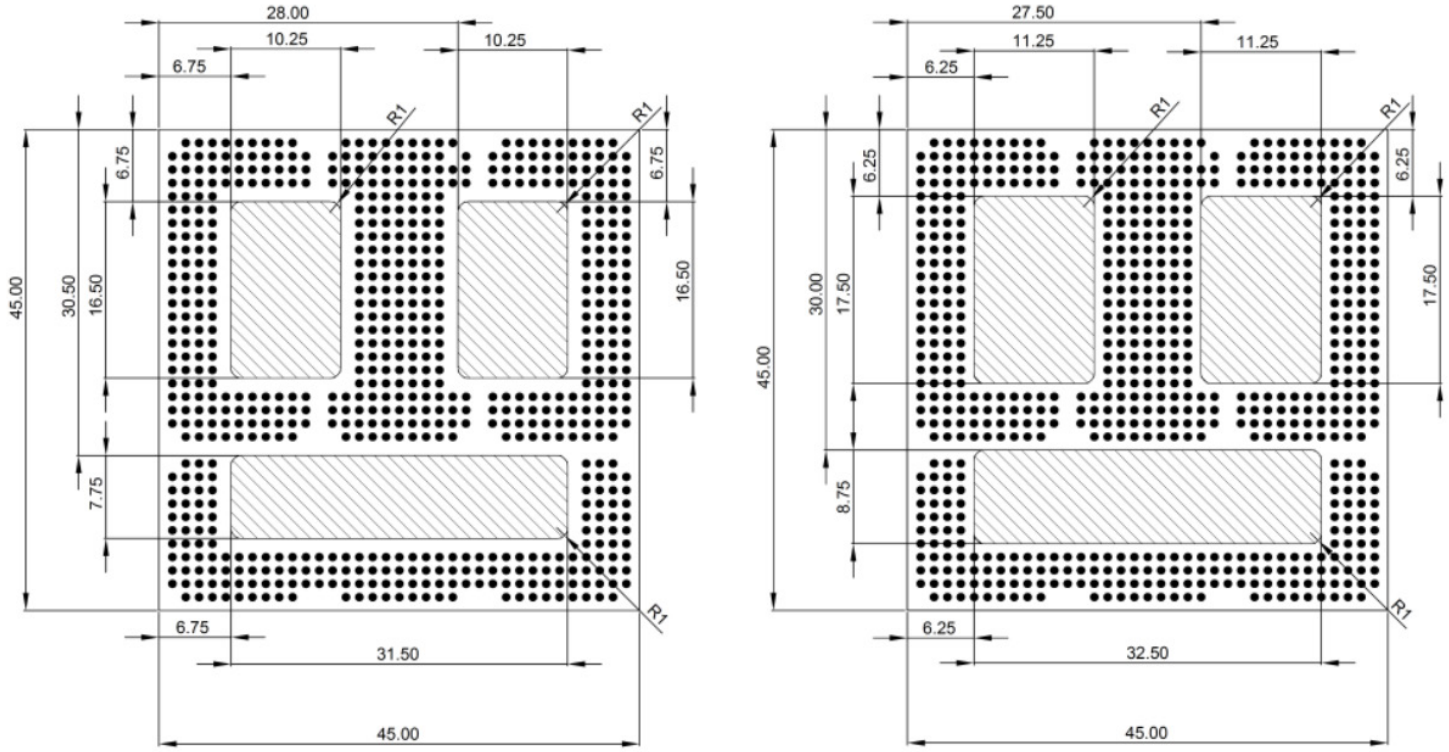


Figure 16: Placement Area (left) and Cut-Out Area (right) - Size L (view from bottom)

Figure 4 – Mechanical dimensions

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7. Thermal Solutions

7.1 Heatspreader: HTS

To be defined on the carrier, follow the carrier mounting points for off-the-shelf designs.

7.2 Heatsink: THS

To be defined on the carrier, follow the carrier mounting points for off-the-shelf designs.

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