ADLINK TECHNOLOGY INC.

PCI-6202

16-bit High-Resolution
Voltage Output Card

User's Manual

Manual Rev. 2.00

Revision Date: March 17, 2008

Part No: 50-11235-1000

Recycled Paper

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ADLINK TECHNOLOGY INC.

Web Site	http://www.adlinktech.com
Sales & Service	service@adlinktech.com
Telephone No.	+886-2-8226-5877
Fax No.	+886-2-8226-5717
Mailing Address	9F No. 166 Jian Yi Road, Chungho City, Taipei Hsien 235, Taiwan, ROC

ADLINK TECHNOLOGY AMERICA, INC.

Sales & Service	info@adlinktech.com
Toll-Free	+1-866-4-ADLINK (235465)
Fax No.	+1-949-727-2099
Mailing Address	8900 Research Drive, Irvine, CA 92618, USA

ADLINK TECHNOLOGY EUROPEAN SALES OFFICE

Sales & Service	emea@adlinktech.com
Toll-Free	+49-211-4955552
Fax No.	+49-211-4955557
Mailing Address	Nord Carree 3, 40477 Düsseldorf, Germany

ADLINK TECHNOLOGY SINGAPORE PTE LTD

Sales & Service	singapore@adlinktech.com
Telephone No.	+65-6844-2261
Fax No.	+65-6844-2263
Mailing Address	84 Genting Lane #07-02A, Cityneon Design Center, Singapore 349584

ADLINK TECHNOLOGY INDIA LIAISON OFFICE

Sales & Service	india@adlinktech.com
Telephone No.	+91-80-57605817
Fax No.	+91-80-26671806
Mailing Address	No. 1357, Ground Floor, "Anupama", Aurobindo Marg JP Nagar (Ph-1) Bangalore - 560078

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ADLINK TECHNOLOGY KOREA

Sales & Service	korea@adlinktech.com
Telephone No.	+82-2-20570565
Fax No.	+82-2-20570563
Mailing Address	#402, Dongsung B/D, 60-12, Nonhyeon-Dong Gangnam-gu, Seoul, 135-010, South Korea

ADLINK TECHNOLOGY BEIJING

Sales & Service	market@adlinkchina.com.cn
Telephone No.	+86-10-5885-8666
Fax No.	+86-10-5885-8625
Mailing Address	Room 801, Building E, Yingchuangdongli Plaza, No.1 Shangdidonglu, Haidian District, Beijing, China

ADLINK TECHNOLOGY SHANGHAI

Sales & Service	market@adlinkchina.com.cn
Telephone No.	+86-21-6495-5210
Fax No.	+86-21-5450-0414
Mailing Address	Floor 4, Bldg. 39, Caoheting Science and Technology Park, No.333 Qinjiang Road, Shanghai, China

ADLINK TECHNOLOGY SHENZHEN

Sales & Service	market@adlinkchina.com.cn
Telephone No.	+86-755-2643-4858
Fax No.	+86-755-2664-6353
Mailing Address	C Block, 2nd Floor, Building A1, Cyber-tech Zone, Gaoxin Ave. 7.S, High-tech Industrial Park S., Nanshan District, Shenzhen, Guangdong Province, China

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Using this manual

1.1 Audience and scope

This manual guides you when using ADLINK multi-function data acquisition PCI card. The card's hardware, signal connections, and calibration information are provided for faster application building. This manual is intended for computer programmers and hardware engineers with advanced knowledge of data acquisition and high-level programming.

1.2 How this manual is organized

This manual is organized as follows:

Chapter 1 Introduction: This chapter intoduces the ADLINK PCI-6202 card including its features, specifications, software support information, and package contents.

Chapter 2 Hardware Information: This chapter presents the card's layout and connector pin definition.

Chapter 3 Installation: This part describes the PCI-6202 installation, and configuration.

Chapter 4 Operation Theory: The operation theory of the PCI-6202 functions including D/A conversion, isolation DIO, and application function I/O are discussed in this chapter.

Chapter 5 Calibration: The chapter offers information on how to calibrate the PCI-6202 for accurate data acquisition and output.

Warranty Policy: This presents the ADLINK Warranty Policy terms and coverages.

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1.3 Conventions

Take note of the following conventions used throughout the manual to make sure that you perform certain tasks and instructions properly.

NOTE	Additional information, aids, and tips that help you perform particular tasks.

IMPORTANT	Critical information and instructions that you MUST perform to complete a task.

WARNING	Information that prevents physical injury, data loss, module damage, program corruption, and others when trying to complete a particular task.

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1 Introduction

The ADLINK PCI-6202 is a 4-channel, 16-bit high-resolution voltage output card with hardware timed waveform generation. It comes with four analog output channels that update simultaneously and support up to 1 MS/s update rate per channel. Delivering excellent linearity (DNL <1 LSB), the PCI-6202 is suitable for dynamic signal simulation and control applications which require high accuracy through voltage output.

The PCI-6202 also provides additional I/O control lines for system integration, including 16-CH isolated digital input and 16-CH isolated output, 8-CH TTL DI and 8-CH TTL DO, 3-CH encoder inputs, and 4-CH PWM outputs. These high-performance I/O functionalities combined with a solid voltage output linearity and high accuracy, make the PCI-6202 the best single-board solution for both equipment manufacturers and laboratory research applications.

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1.1 Features

The PCI-6202 comes with the following features:

- Supports a 32-bit 3.3 V or 5 V PCI bus
- PCI 2.3-compliant
- 4-CH single-ended analog output
- 1 MS/s with simultaneous update
- FIFO with 512 samples
- 8-CH TTL digital input and 8-CH TTL digital output
- 16-CH isolated digital input and 16-CH isolated digital output
- 2-CH 32-bit 40 MHz general purpose timer/counters
- 3-CH 4 MHz encoder input, supporting AB phase and CW/CCW
- 4-CH PWM output
- 3-CH digital application function interface with:
  - Digital input and output
  - External digital trigger in and out
  - External analog output conversion clock source
  - Encoder trigger out

1.2 Applications

The PCI-6202 is suitable for the following applications:

- Automotive testing
- Waveform generation

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1.3 Specifications

Analog Output (AO)	
Number of channels	4
D/A converter	Onboard converter
Maximum update range	1 MS/s per channel
Resolution	16-bit
Data transfers	Programmed I/O, DMA
Output range	±10 V
Settling time	3 µs (0.1% of full scale)
Slew range	20 V/µS
Rise time	0.67 V/µS (typical)
Fall time	20V/µS
Maximum DNL	±1 LSB
Output coupling	DC
Output impedance	0.01 Ω (maximum)
Output driving	±5 mA (maximum)
Stability	Any passive load, up to 1500 pF
Power-on state	0 V
Power-on glitch	6.25 mV/ms (maximum)
Offset error	After calibration: ±0.3 mV (typical)
Gain error	After calibration: ±0.06 mV (maximum)
Isolated Digital Input	
Number of channels	16
Photo isolator	PC3H410 or equivalent
Isolation voltage	2500 Vrms
Input voltage	Up to 24 VDC, non-polarity • Logic low: VIL = 0 to 3.0 V • Logic high: VIH = 3.2 V to 2.4 V
Input resistance	4.7 KΩ @ 0.12 W

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Isolated Digital Output	
Number of channels	16
Photo isolator	PC3H7 or equivalent
Isolation voltage	2500 Vrms
Output type	Photo-coupler transistors, open collector up to 24 VDC
Sink current	200 mA for each channel (maximum)
Digital I/O	
Number of channels	• 8-CH TTL digital input • 8-CH TTL digital output • 3-CH Application Function Interface (AFI)
Input voltage	• Logic low: VIL = 0.8V max; IIL = 0.2mA max • Logic high: VIH = 2.0V min; IIH = 0.2mA max
Output voltage	• Logic low: VOL = 0.5V max; IOL = 10mA max • Logic high: VOH = 2.6V min; IIH = 10mA max
Timer/Counter	
Type	2-CH 32-bit general-purpose timer/counters
Clock source	Internal or external
Maximum source frequency	• Internal: 80 MHz • External: 10 MHz
Encoder Inputs	
Number of channels	3
Maximum input frequency	4 MHz
Encoder count	19-bit data width
Photo isolator	Photo isolator
Encoder modes	• CW/CCW • X1 AB phase encoder • X2 AB phase encoder • X4 AB phase encoder
PWM Outputs	
Number of channels	4
Duty cycle	1 - 99%
Modulation frequency	20 MHz to 0.005 Hz
Isolated 5V Output	
Driving current	350 mA (maximum)

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Physical, Power, and Operating Environment	
Dimension	120 mm x 87 mm
I/O connector	2 x 68-pin SCSI-VHDCI connectors
Power Requirement (typical)	• +5 VDC: 500 mA • +12 VDC: 110 mA
Operating environment	• Ambient temperature: 0ºC to 45ºC • Relative humidity: 10% to 90%, non-condensing
Storage environment	• Ambient temperature: -20ºC to 80ºC • Relative humidity: 5% to 95% non-condensing

Specifications are subject to change without notice.

1.4 Unpacking Checklist

Before unpacking, check the shipping carton for any damage. If the shipping carton and/or contents are damaged, inform your dealer immediately. Retain the shipping carton and packing materials for inspection. Obtain authorization from your dealer before returning any product to ADLINK.

Check if the following items are included in the package.

- PCI-6202 multi-function DAQ card
- ADLINK All-in-One CD
- User's manual

If any of the items is damaged or missing, contact your dealer immediately.

CAUTION The card must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the card. Wear a grounded wrist strap when servicing.

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1.5 Software Support

ADLINK provides comprehensive software drivers and packages to suit various user approach to building a system. Aside from programming libraries, such as DLLs, for most Windows-based systems, ADLINK also provides drivers for other application environment such as LabVIEW® and MATLAB®. ADLINK also provides ActiveX component ware for measurement and SCADA/HMI, and breakthrough proprietary software applications.

All software options are included in the ADLINK All-in-One CD.

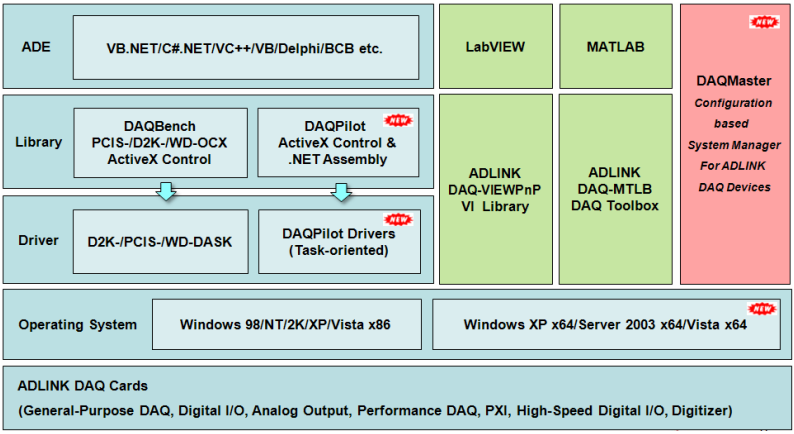


Figure 1-1: ADLINK Software Support Overview

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Driver Support for Windows

DAQPilot

DAQPilot is a driver and SDK with a graphics-driven interface for various application development environments. DAQPilot comes as ADLINK's commitment to provide full support to its comprehensive line of data acquisition products and is designed for the novice to the most experienced programmer.

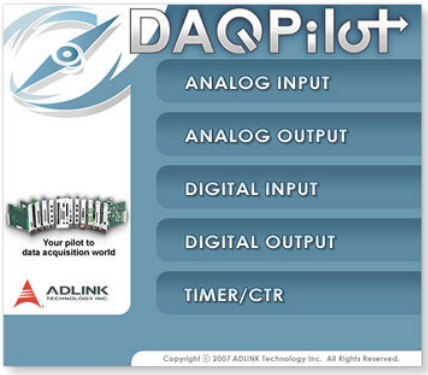


Figure 1-2: DAQPilot Main Interface

As a task-oriented DAQ driver, SDK and wizard for Windows systems, DAQPilot helps you shorten the development time while accelerating your learning curve for data acquisition programming.

You can download and install DAQPilot at
http://www.adlinktech.com/TM/DAQPilot.html

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DAQMaster

The ADLINK DAQMaster is a smart device manager that opens up access to ADLINK data acquisition and test and measurement products. DAQMaster delivers all-in-one configurations and provides you with a full support matrix to properly and conveniently configure ADLINK Test and Measurement products.

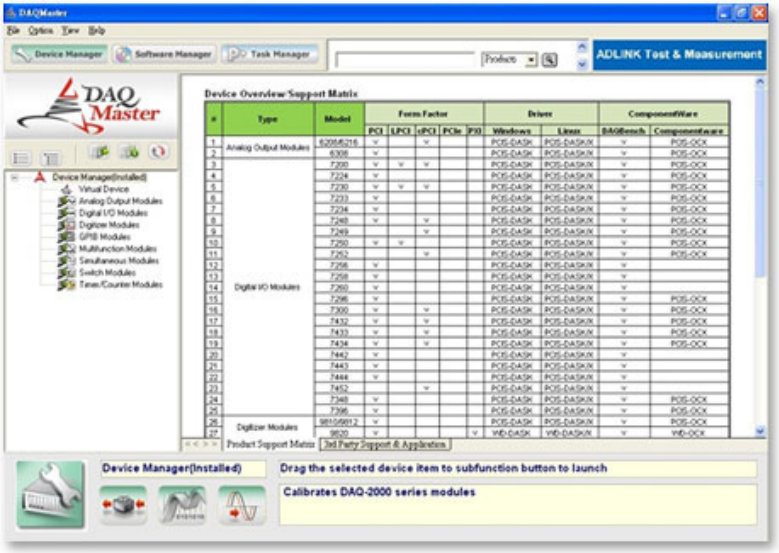


Figure 1-3: DAQMaster Device Manager

As a configuration-based device manager for ADLINK DAQ cards, DAQMaster enables you to manage ADLINK devices and interfaces, install and upgrade software applications, and manage ADLINK DAQPilot tasks.

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PCIS-DASK (Legacy Drivers and Support)

PCIS-DASK is composed of advanced 32-bit kernel drivers for customized DAQ application development. PCIS-DASK enables you to perform detailed operations and achieve superior performance and reliability from your data acquisition system. DASK kernel drivers now support the revolutionary Windows Vista® OS.

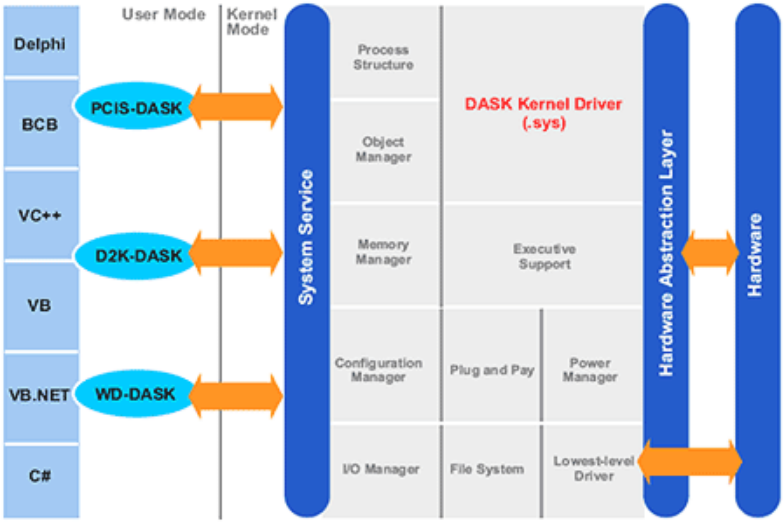


Figure 1-4: Legacy Software Support Overview

NOTE	ADLINK strongly recommends installing DAQPilot and avoid using legacy DASK drivers. For current DASK driver users or those who do not have Internet access, we offer an installation CD. Contact your ADLINK distributor for details.

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PCIS-DASK drivers prepare legacy Windows users for Windows Vista and 64-bit editions of Windows. PCIS-DASK comes with the following features:

- Supports Windows Vista 32-bit or 64-bit editions
- Supports AMD64 and Intel x86-64 architectures
- Digitally-signed for Windows Vista 64-bit edition
- Utilizes WOW64 subsystem to ensure that 32-bit applications run normally on 64-bit editions of Windows XP, Windows 2003 Server, and Windows Vista without modification

For more information about Windows Vista support, visit http://www.adlinktech.com/TM/VistaSupport.html, or view the user's guide included in the ADLINK All-in-one CD.

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2 Hardware Information

This chapter provides information on the PCI-6202 layout, connectors, and pin assignments.

2.1 Card Layout

Figure 2-1 shows the PCI-6202 board layout and dimensions.

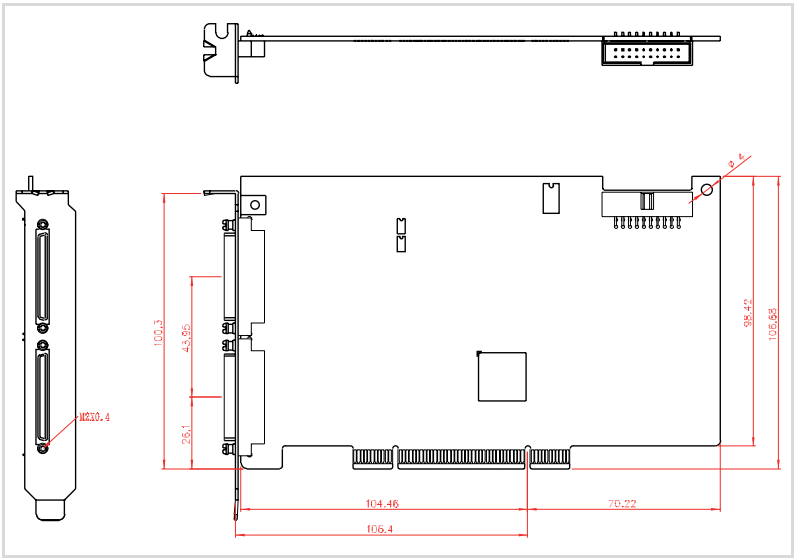


Figure 2-1: PCI-6202 Layout

2.2 Connector Pin Assignment

PCI-6202 comes with two VHDCI 68-pin SCSI-VHDCI connectors. The CN1 connector is for digital input/output, AFI, and analog output, while CN2 is for isolated DIO and encoder.

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CN1 Pin Assignment

Definition	Pin #		Definition
DO0	1	35	GPTC_OUT0
DO1	2	36	GPTC_GATE0
DO2	3	37	GPTC_UD0
DO3	4	38	GPTC_AUX0
DO4	5	39	GPTC_CLK0
DO5	6	40	GPTC_OUT1
DO6	7	41	GPTC_GATE1
DO7	8	42	GPTC_UD1
DGND	9	43	GPTC_AUX1
DGND	10	44	GPTC_CLK1
DI0	11	45	DGND
DI1	12	46	DGND
DI2	13	47	DGND
DI3	14	48	DGND
DI4	15	49	DGND
DI5	16	50	DGND
DI6	17	51	DGND
DI7	18	52	DGND
DGND	19	53	PWM_0
DGND	20	54	PWM_1
DGND	21	55	PWM_2
DGND	22	56	PWM_3
DGND	23	57	AFI0
AGND	24	58	AFI1
AGND	25	59	AFI2
AGND	26	60	AGND
AGND	27	61	AGND
AGND	28	62	AGND
AGND	29	63	AGND
AGND	30	64	AGND
AO_CH0	31	65	AGND
AO_CH1	32	66	AGND
AO_CH2	33	67	AGND
AO_CH3	34	68	AGND

Table 2-1: CN1 Pin Assignment

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CN2 Pin Assignment

Definition	Pin #		Definition
IDI_0	1	35	IDI_8
IDI_1	2	36	IDI_9
IDI_2	3	37	IDI_10
IDI_3	4	38	IDI_11
IDI_4	5	39	IDI_12
IDI_5	6	40	IDI_13
IDI_6	7	41	IDI_14
IDI_7	8	42	IDI_15
COM	9	43	COM
COM	10	44	COM
EA0+	11	45	EA1+
EA0-	12	46	EA1-
EB0+	13	47	EB1+
EB0-	14	48	EB1-
EZ0+	15	49	EZ1+
EZ0-	16	50	EZ1-
EORG0	17	51	EORG1
EA2+	18	52	EZ2+
EA2-	19	53	EZ2-
EB2+	20	54	EORG2
EB2-	21	55	Ext. +24V
Ext. GND	22	56	Ext. +24V
IGND	23	57	Ext. GND
IGND	24	58	IGND
VDD	25	59	IGND
VDD	26	60	ISO5V
IDO_0	27	61	IDO_8
IDO_1	28	62	IDO_9
IDO_2	29	63	IDO_10
IDO_3	30	64	IDO_11
IDO_4	31	65	IDO_12
IDO_5	32	66	IDO_13
IDO_6	33	67	IDO_14
IDO_7	34	68	IDO_15

Table 2-2: CN2 Pin Assignment

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Signal Descriptions

Below is the PCI-6202 I/O signal descriptions.

Signal Name	Reference	Direction	Description
AO_CH<0..3>	AGND	Output	AO channel <0..3>
AGND	—	—	Analog ground for AO
DI<0..7>	DGND	Input	Digital Input <0..7>
DO<0..7>	DGND	Output	Digital Output <0..7>
EA<0, 1, 2>	Ext. GND	Input	Encoder A Phase
EB<0, 1, 2>	Ext. GND	Input	Encoder B Phase
EZ<0, 1, 2>	Ext. GND	Input	Encoder Z Phase
ORG<0, 2>	Ext. GND	Input	Encoder Original Signal
Ext. 24V	Ext. GND	Input	Encoder voltage input pin
GPTC_CLK<0, 1>	DGND	Input	Clock source of GPTC<0, 1>
GPTC_GATE<0, 1>	DGND	Input	Gate of GPTC<0, 1>
GPTC_OUT<0, 1>	DGND	Output	Output of GPTC<0, 1>
GPTC_UD<0, 1>	DGND	Input	Up/Down of GPTC<0, 1>
IDI<0..15>	COM	Input	Isolation digital input<0..15>
IDO<0, 15>	IGND	Output	Isolation digital output<0..15>
ISO5V	IGND	Output	Isolation +5V power
NC	NC	NC	No connection

Table 2-3: I/O Signal Description

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3 Installation

3.1 Before You Proceed

The PCI-6202 card has electro-static sensitive components that can be easily damaged by static electricity. The card must be handled on a grounded anti-static mat. The operator must wear an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the card module carton for damages. Shipping and handling could cause damage to the module. Make sure that the card has no damage before installing it.

After opening the card package, get the module and place it on a grounded anti-static surface with component side up, then carefully inspect the module for any damage. Press down all socketed ICs to make sure that they are properly seated. Do this only with the module placed on a firm flat surface.

WARNING Do not apply power to the card if it is damaged.

3.2 Installing the Card

IMPORTANT Install the card driver before you install the card into your computer system. Refer to section 1.5 for driver support information.

To install the card:

1. Turn off the system/chassis and disconnect the power plug from the power source.
2. Remove the system/chassis cover.
3. Select the PCI slot that you intend to use, then remove the bracket opposite the slot, if any.
4. Align the card connectors (golden fingers) with the slot, then press the card firmly until the card is completely seated on the slot.
5. Secure the card to the chassis with a screw.

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6. Replace the system/chassis cover.
7. Connect the power plug to a power source, then turn on the system.

3.3 Configuring the Card

As a plug and play component, the card requests an interrupt number through its PCI controller. The system BIOS responds with an interrupt assignment based on the card information and on known system parameters. These system parameters are determined by the installed drivers and the hardware load detected by the system.

Configuration

The card configuration is done on a card-by-card basis for all PCI cards on your system. Because configuration is controlled by the system and the software, there is no jumper setting required for base address, DMA, and interrupt IRQ.

The configuration is subject to change with every boot of the system as new PCI cards are added or removed.

Troubleshooting

If your system fails to boot or if you experience erratic operation with your PCI card in place, this is likely caused by an interrupt conflict (such as when the BIOS Setup is incorrectly configured). Refer to the BIOS documentation that came with the system for details.

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4 Operation Theory

The operation theory of each PCI-6202 function is described in this chapter. These functions include D/A conversion, isolation DIO, application function I/O, and more. The operation theory can help you understand how to configure and program the PCI-6202.

4.1 Block Diagram

There are 4 single-ended channels of 16-bit D/A output available in the PCI-6202. Every two channels are generated by one DAC chip (TI DAC8812). The DAC controller and all timing control logics are implemented by FPGA. Combining FIFO design and synchronized update control logic, the PCI-6202 provides 4 channels simultaneous voltage output with waveform generation functionality.

For analog output, the PCI-6202 comes with a calibration circuit to provide high-accuracy voltage output with low temperature drift. The calibration data are saved in the EEPROM.

The isolated digital I/O, TTL digital I/O, encoder, and PWM output are controlled directly by the FPGA. Refer to Figure 4-1.

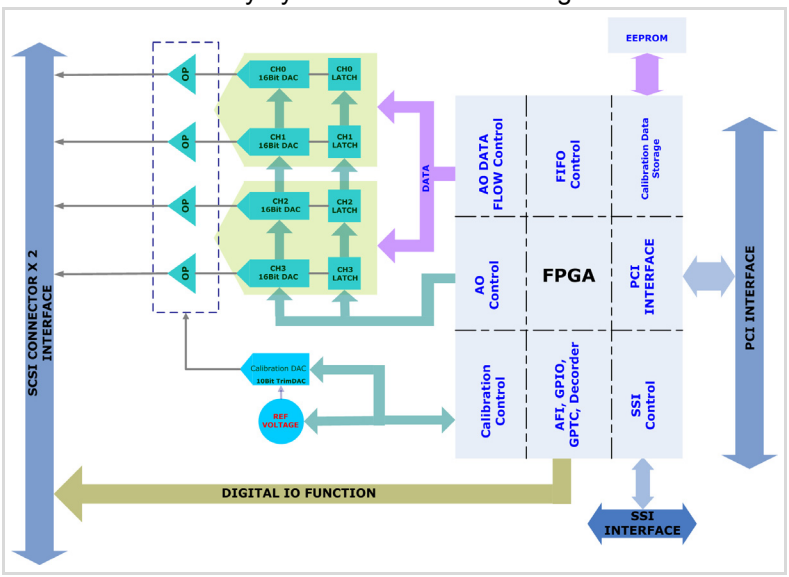


Figure 4-1: PCI-6202 Block Diagram

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4.2 D/A Conversion

The PCI-6202 supports voltage output in two ways: software polling and DMA mode. This allows control of the D/A update rate by either software or hardware timer.

Architecture

Figure 4-2 shows the PCI-6202 DAC structure. Two 16-bit D/A chips, each with two digital-to-analog converters, are available in the card. The FIFO module and timing control module are implemented in the FPGA. The FIFO module stores the D/A data that comes from DMA transfer or software polling.

The D/A data is then latched in the DAC internal register and waits for the data load command, while the timing control module handles all update time information. For example, the analog output updates data based on the update time interval parameter set by the user. The timing block counts down to this parameter. When the count down reaches zero, the timing block sends the update command to DAC to load data.

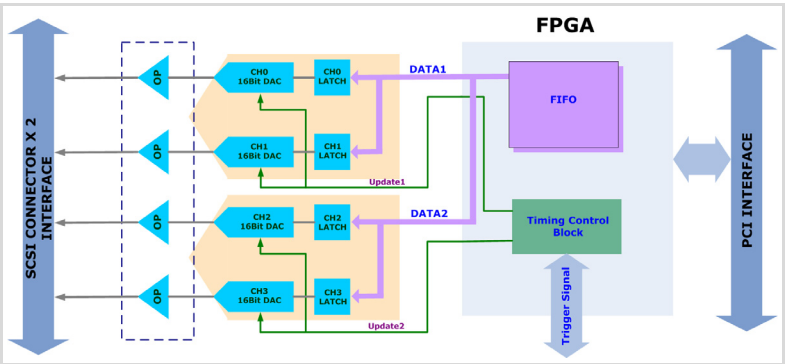


Figure 4-2: Block Diagram of D/A Conversion Function

Hardware-controlled Waveform Generation

FIFO is a hardware first-in first-out data queue that holds temporary digital codes for D/A conversion. When PCI-6202 operates in waveform generation mode, the waveform patterns are stored in FIFO with 512 samples.

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Waveform patterns larger than 512 samples are also supported using bus-mastering DMA transfer via the PCI controller. Data format in FIFO is shown in Figure 4-3.

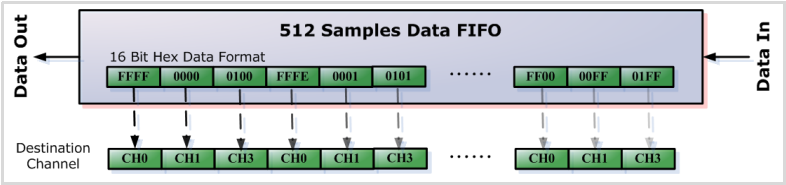


Figure 4-3: FIFO Data In/Out Structure

DMA transfers data according to channel order. Figure 4-4 shows DA channel 0 to channel 3 data, while channel 2 is disabled.

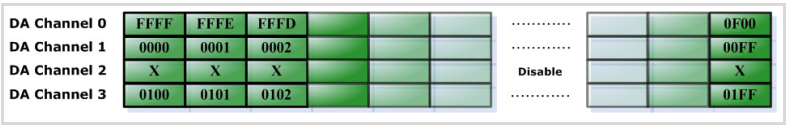


Figure 4-4: Waveform Generation for Three Channels Update

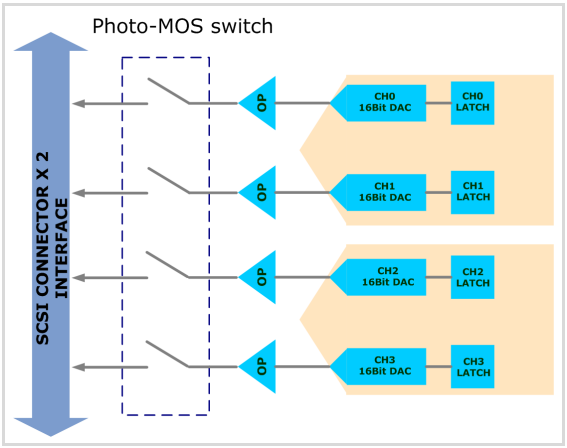
With hardware-based waveform generation, D/A conversions are updated automatically by the FPGA rather than by the application software. Compare with the conventional software-based waveform generation, the precise hardware timing control guarantees non-distorted waveform generation even when the host CPU is under heavy loading.

NOTE When using waveform generation mode, all four DACs must be configured in a single mode. However, any individual DAC can be disabled.

Output Switch

There is an onboard output switch between the DACs and DUC (device under control). Each DAC has an output switch. When DUC is ready but the controller PC is not or in start-up process, the PCI-6202 is in unknown status and the DAC output may not be stable. The DUC may malfunction or get damaged when it receives an unknown signal. In order to prevent this, the output switch isolates the DUC from the DAC signals.

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The default switch setting is OFF, but this can be programmed via the software application.

Using the Multiplying Characteristic of DACs

The PCI-6202 supports a maximum ±10V voltage output. Table 4-1 illustrates the relationship of straight binary coding between the digital codes and output voltages.

Digital Code	Analog Output
0xFFFF	20V * (65535/65536) – 10V
0xC000	5V
0x8001	20V * (32769/65536) – 10V
0x8000	0V
0x4000	-5V
0x0000	-10V

Table 4-1: Bipolar Output Codes

Software Update

This method is suitable for applications that need to generate D/A output controlled by user programs. In this mode, the D/A converter generates one output once the software command is issued. However, it would be difficult to determine the software update rate under a multitask OS such as Windows.

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Waveform Generation

This method is suitable for applications that need to generate waveforms at a precise and fixed rate. Various programmable counters will facilitate the generation of complex waveforms with great flexibility.

Waveform Generation Timing

Six counters interact with the waveform to generate different DAWR timing to form various waveforms. These are described in Table 4-2 and illustrated in Figure 4-5.

Counter Name	Width	Description	Note
UI_counter	32-bit	**Update Interval**. Defines the update interval between each data output.	Update Interval = UI_counter / Timebase*.
UC_counter	32-bit	**Update Counts**. Defines the number of data in a waveform.	When value in UC_counter is smaller than the size of waveform patterns, the waveform is generated piece-wisely.
IC_counter	32-bit	**Iteration Counts**. Defines how many times the waveform is generated.	
DLY1_counter	32-bit	Defines the delay time for waveform generation after the trigger signal.	Delay Time = (DLY1_counter / Clock Timebase)
DLY2_counter	32-bit	Defines the delay time to separate consecutive waveform generation. This is applicable only in Iterative Waveform Generation mode.	Delay Time = (DLY2_counter / Clock Timebase)
Trig_counter	32-bit	Defines the acceptable start trigger count when re-trigger function is enabled	

Table 4-2: Summary of Counters for Waveform Generation

Timebase= 80M*

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NOTE The maximum D/A update rate is 1 MHz, and the minimum setting of UI_counter is 80.

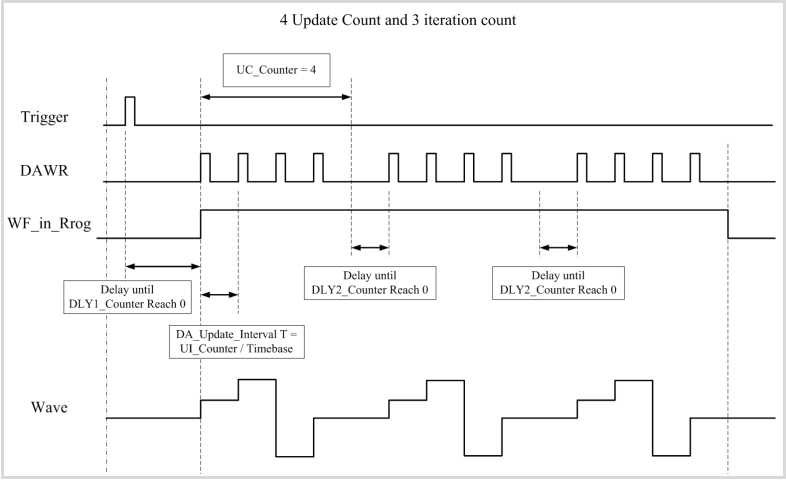


Figure 4-5: Typical D/A Timing of Waveform Generation

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Trigger Modes

Post-Trigger Generation

Use post-trigger generation when you want to generate a waveform right after a trigger signal. The number of patterns to be updated after the trigger signal is specified by UC_counter* IC_counter and is illustrated in Figure 4-6.

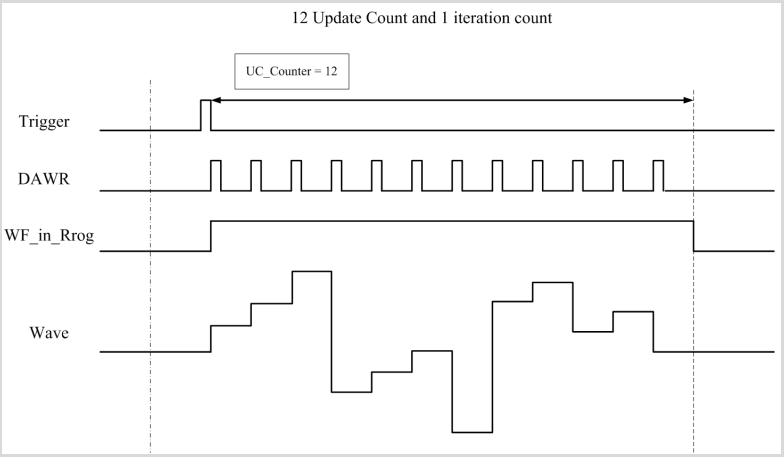


Figure 4-6: Post-Trigger Generation

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Delay-Trigger Generation

Use delay-trigger when you want to delay the waveform generation after the trigger signal. The delay time is determined by DLY1_counter, as illustrated in Figure 4-7.

The counter counts down on the rising edges of DLY1_counter clock source after the start trigger signal. When the count reaches zero, card will start to generate the waveform. The DLY1_counter clock source can be selected via software application using the internal 80 MHz timebase.

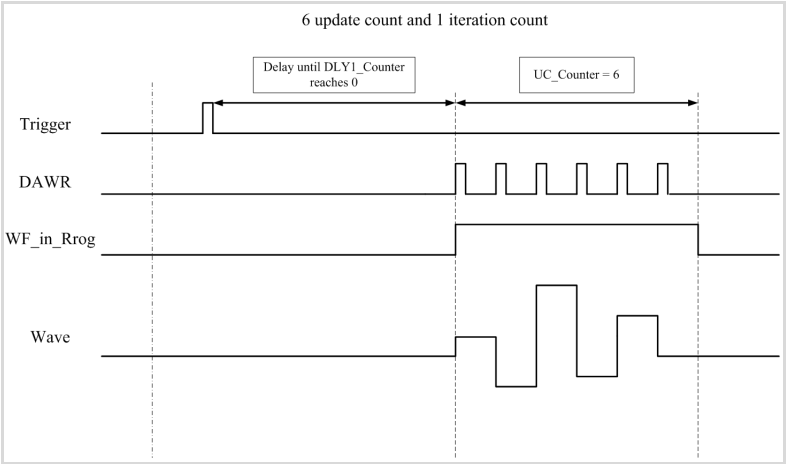


Figure 4-7: Delay-Trigger Generation

Post-Trigger or Delay-Trigger with Retrigger

Use post-trigger or delay-trigger with retrigger when you want to generate multiple waveforms with respect to multiple incoming trigger signals. You can set Trig_counter to specify the number of acceptable trigger signals. Refer to Figure 4-8.

In this example, two waveforms are generated after the first trigger signal. The board then waits for another trigger signal.

When the next trigger signal is asserted, the board generates two more waveforms.

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After two trigger signals, as specified in Trig_Counter, no more triggers signals will be accepted unless trigger reset command is executed. For more information on Iterative Waveform Generation that is used in this example, refer to the next section.

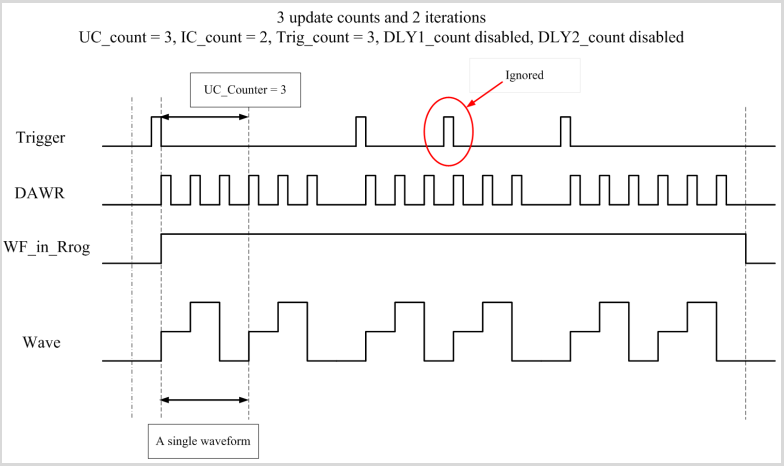


Figure 4-8: Post-Trigger with Retrigger Generation

NOTE Start Trigger signals asserted during the waveform generation process will be ignored.

Iterative Waveform Generation

You can set the IC_counter to generate iterative waveforms no matter which trigger mode is used. The IC_counter stores the iteration number. Examples are shown in Figure 4-9 and Figure 4-10. When IC_counter is enabled and set to 0, the waveform generation will not stop until IC_counter is disabled.

An onboard data FIFO is used to buffer the waveform patterns for waveform generation. If the size of a single waveform is smaller than that of the FIFO, after initially loading the data from the host computer's memory, the data in FIFO will be reused when a single waveform generation is completed and will not occupy the PCI bandwidth afterwards.

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However, if the size of a single waveform is larger than that of the FIFO, it needs to be intermittently loaded from the host computer's memory via DMA, and will occupy the PCI bandwidth.

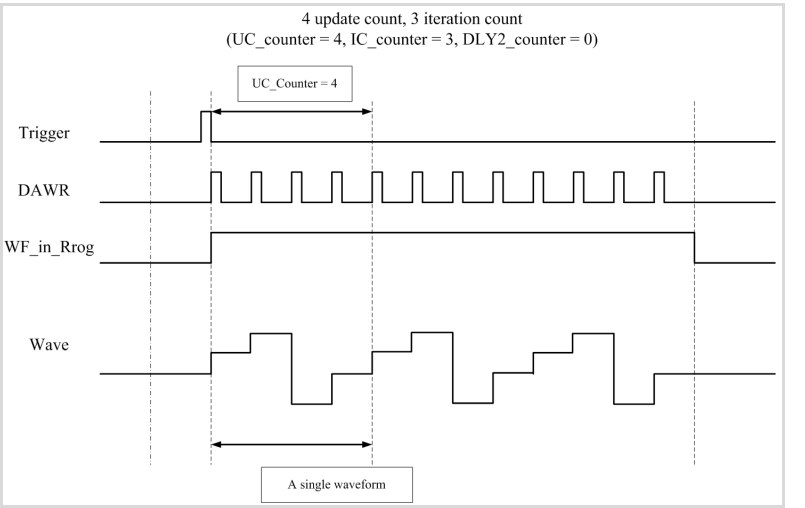


Figure 4-9: Finite Iterative Waveform Generation with Post-trigger

In conjunction with different trigger modes and counter setups, you can manipulate a single waveform to generate different and more complex waveforms.

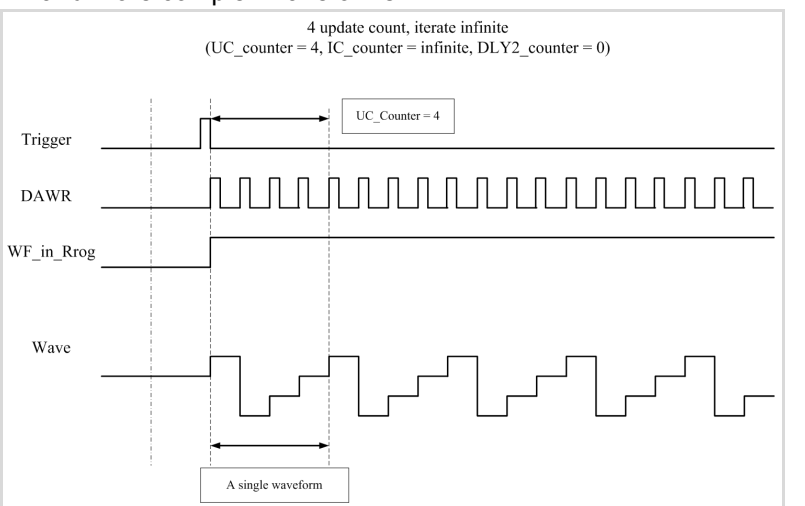


Figure 4-10: Infinite Iterative Waveform Generation with Post-trigger

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DLY2_Counter in Iterative Waveform Generation

To expand the flexibility of iterative waveform generation, DLY2_counter was implemented to separate consecutive waveform generations.

The DLY2_counter starts counting down right after a single waveform generation is completed. When it reaches zero, the next iteration of waveform generation will start as shown in Figure 4-5. If you generate the waveform piece-wisely, the next piece of waveform will be generated.

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4.3 General Purpose Digital D/O

The PCI-6202 offers comprehensive support to various digital I/O provided by an FPGA chip. These digital I/O include general purpose digital input and output, PWM, Timer/Counter, and Application Function Interface (AFI).

General Purpose DIO

PCI-6202 provides 8 channel DI and 8 channel DO. All I/O are static TTL-compliant. You can read/write these I/O line by software polling. In this way, the sample and update rate is fully controlled by software timing.

Definition	Pin #		Definition
DO0	1	35	
DO1	2	36	
DO2	3	37	
DO3	4	38	
DO4	5	39	
DO5	6	40	
DO6	7	41	
DO7	8	42	
DGND	9	43	
DGND	10	44	
DI0	11	45	DGND
DI1	12	46	DGND
DI2	13	47	DGND
DI3	14	48	DGND
DI4	15	49	DGND
DI5	16	50	DGND
DI6	17	51	DGND
DI7	18	52	DGND
DGND	19	53	PWM_0
DGND	20	54	PWM_1
DGND	21	55	PWM_2
DGND	22	56	PWM_3
DGND	23	57	AFI0
	24	58	AFI1
	25	59	AFI2
	26	60	
	...	...	
	34	68	

Table 4-3: TTL DIO Pins in CN1

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Application Function Interface (AFIx)

The application function interface can be used for special functions. The table below shows the available function for each dedicated AFI pin.

NOTE When AFIx is configured as one function, these pins may not be used for any other function.

Pin	Function	Note
AFI0	External convert signal out	Configured as a DA convert source.
	External digital trigger in	Used for one of all DA output trigger source.
	External digital trigger out	Export a digital trigger based on a software trigger.
	Encoder position trigger out	This function is combined with encoder0 input. When encoder counts up for a specific value that you have set, AFI0 will export a digital high signal.
AFI1	External convert signal out	AFI1 can be configured as a DA convert source.
	Digital trigger in	Used for one of all DA output trigger source.
	Digital trigger out	Export a digital trigger based on software trigger.
	Encoder position trigger out	This function is combined with encoder1 input. When encoder counts up for a specific value that you have set, AFI1 will export a digital high signal.
AFI2	Encoder position trigger out	This function is combined with encoder2 input. When encoder counts up for a specific value that you have set, AFI2 will export a digital high signal.

Table 4-4: AFI Functions

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PWM Output

The PCI-6202 provides four dedicated PWM outputs, each consisting of two parameters: high level and low level width. These two parameters have a 24-bit count width that can be used. The PWM base clock is 80MHz.

Figure 4-11 shows the high and low level definition of the PWM output. HV is high level width count value while LV is low level count value.

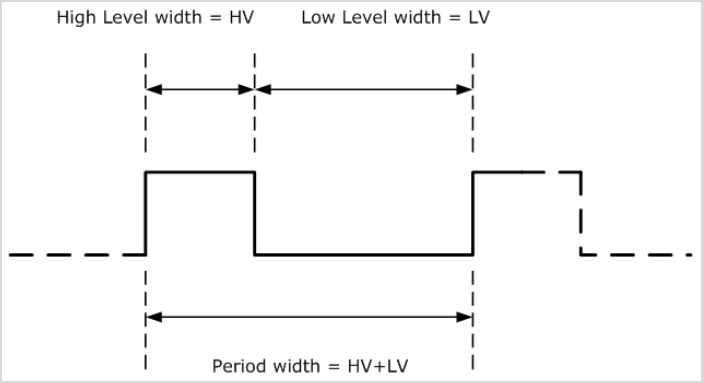


Figure 4-11: PWM Output Parameters

The period width time value is shown in this formula:

$$Period_time_value = \frac{HV + LV}{80MHz}$$

HV and LV can also set the PWM duty cycle:

$$High_level_dutycycle = \frac{HV}{HV + LV}$$

$$Low_level_dutycycle = \frac{LV}{HV + LV}$$

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General Purpose Timer/Counter

PCI-6202 comes with three general purpose timer/counter sets featuring:

- Count up/down controlled by hardware or software
- Programmable counter clock source (internal clock up to 80MHz, external clock up to 10MHz)
- Programmable gate selection (hardware or software control)
- Programmable input and output signal polarities (high active or low active)
- Initial Count can be loaded from a software application
- Current count value can be read-back by software without affecting circuit operation.

Definition	Pin #		Definition
	1	35	GPTC_OUT0
	2	36	GPTC_GATE0
	3	37	GPTC_UD0
	4	38	GPTC_AUX0
	5	39	GPTC_CLK0
	6	40	GPTC_OUT1
	7	41	GPTC_GATE1
	8	42	GPTC_UD1
DGND	9	43	GPTC_AUX1
DGND	10	44	GPTC_CLK1
	11	45	DGND
	12	46	DGND
	13	47	DGND
	14	48	DGND
	15	49	DGND
	16	50	DGND
	17	51	DGND
	18	52	DGND
DGND	19	53	
DGND	20	54	
DGND	21	55	
DGND	22	56	
DGND	23	57	
...	...	...	...
	34	68	

Table 4-5: Timer/Counter Mode Pins in CN1

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Basic Timer/Counter Functions

Each timer/counter has three inputs that can be controlled via hardware or software applications. They are clock input (GPTC_CLK), gate input (GPTC_GATE), and up/down control input (GPTC_UD). The GPTC_CLK input provides a clock source input to the timer/counter. Active edges on the GPTC_CLK input make the counter increment or decrement. The GPTC_UD input controls the counter to count up or down (high: count up; low: count down), while the GPTC_GATE input is a control signal which acts as a counter enable or a counter trigger signal under different applications. The GPTC_OUT will then generate a pulse signal based on which timer/counter mode you have set.

All input/output signals polarities can be programmed by software application. For brevity, all GPTC_CLK, GPTC_GATE, and GPTC_OUT in the following illustrations are assumed to be active high or rising-edge triggered.

General Purpose Timer/Counter modes

Ten programmable timer/counter modes are provided. All modes start operating following a software-start signal that is set by the software. The GPTC software reset initializes the status of the counter and reloads the initial value to the counter. The operation remains halted until the software-start is executed again. The operating theories under different modes are described in the following sections.

Mode1: Simple Edge Counting

In this mode, the counter counts the number of pulses on the GPTC_CLK after the software-start. Initial count can be loaded from the software application. Current count value can be read-back by software any time with no effect to the counting. GPTC_GATE is used to enable/disable counting. When GPTC_GATE is inactive, the counter halts the current count value. Figure 4-12 illustrates the operation with initial count = 5, count-down mode.

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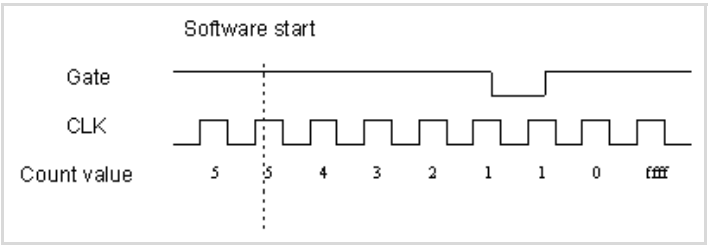


Figure 4-12: Mode 1 Operation

Mode 2: Single Period Measurement

The counter counts the period of the signal on GPTC_GATE in terms of GPTC_CLK. Initial count can be loaded from the software application. After the software-start, the counter counts the number of active edges on GPTC_CLK between two active edges of GPTC_GATE. After the completion of the period interval on GPTC_GATE, GPTC_OUT outputs high and then current count value can be read-back by the software application. Figure 4-13 illustrates the operation where initial count = 0, count-up mode.

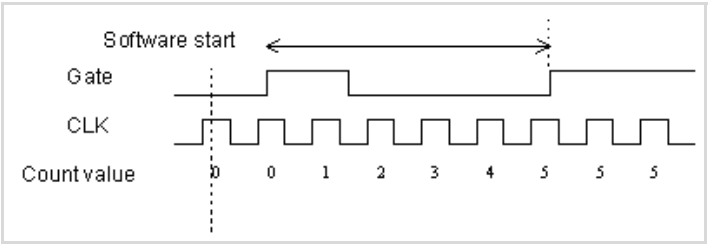


Figure 4-13: Mode 2 Operation

Mode 3: Single Pulse-width Measurement

The counter counts the pulse-width of the signal on GPTC_GATE in terms of GPTC_CLK. Initial count can be loaded from the software application.

After the software-start, the counter counts the number of active edges on GPTC_CLK when GPTC_GATE is in its active state. After the completion of the pulse-width interval on

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GPTC_GATE, GPTC_OUT outputs high and then current count value can be read-back by the software application. Figure 4-14 illustrates the operation where initial count = 0, count-up mode.

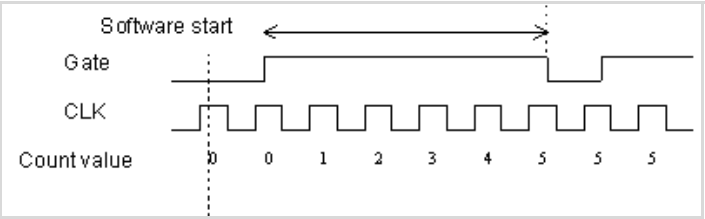


Figure 4-14: Mode 3 Operation

Mode 4: Single Gated Pulse Generation

This generates a single pulse with programmable delay and programmable pulse-width following the software-start. The two programmable parameters can be specified in terms of periods of the GPTC_CLK input by the software application. GPTC_GATE is use to enable/disable counting. When GPTC_GATE is inactive, the counter halts the current count value. Figure 4-15 illustrates the generation of a single pulse with a pulse delay of two and a pulse-width of four.

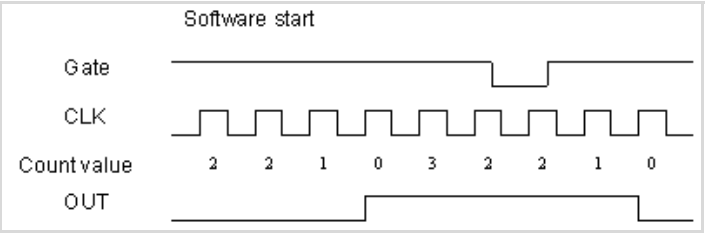


Figure 4-15: Mode 4 Operation

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Mode 5: Single Triggered Pulse Generation

This mode generates a single pulse with programmable delay and programmable pulse-width following an active GPTC_GATE edge. You may specify these programmable parameters in terms of periods of the GPTC_CLK input. When the first GPTC_GATE edge triggers the single pulse, GPTC_GATE makes no effect until the software-start is executed again. Figure 4-16 illustrates the generation of a single pulse with a pulse delay of two and a pulse-width of four.

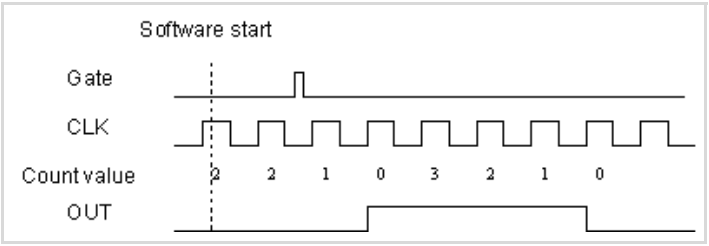


Figure 4-16: Mode 5 Operation

Mode 6: Re-triggered Single Pulse Generation

This mode is similar to Mode 5 except that the counter generates a pulse following every active edge of GPTC_GATE. After the software-start, every active GPTC_GATE edge triggers a single pulse with programmable delay and pulse-width. Any GPTC_GATE triggers that occur when the prior pulse is not completed is ignored. Figure 4-17 illustrates the generation of two pulses with a pulse delay of two and a pulse-width of four.

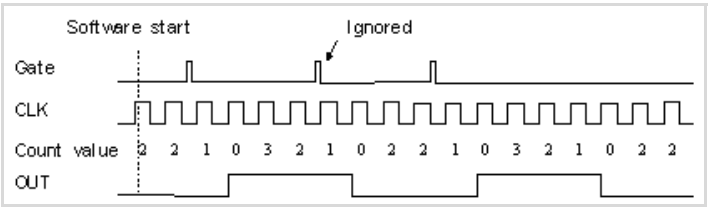


Figure 4-17: Mode 6 Operation

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Mode 7: Single Triggered Continuous Pulse Generation

This mode is similar to Mode 5 except that the counter generates continuous periodic pulses with programmable pulse interval and pulse-width following the first active edge of GPTC_GATE. When the first GPTC_GATE edge triggers the counter, GPTC_GATE makes no effect until the software-start is executed again. Figure 4-18 illustrates the generation of two pulses with a pulse delay of four and a pulse-width of three.

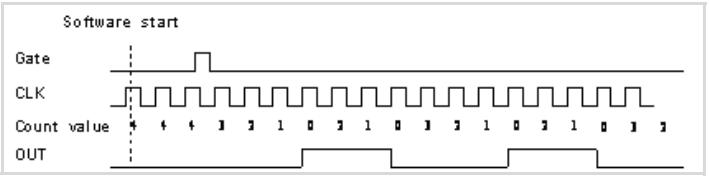


Figure 4-18: Mode 7 Operation

Mode 8: Continuous Gated Pulse Generation

This mode generates periodic pulses with programmable pulse interval and pulse-width following the software-start. GPTC_GATE is use to enable/disable counting. When GPTC_GATE is inactive, the counter halts the current count value. Figure 4-19 illustrates the generation of two pulses with a pulse delay of four and a pulse-width of three.

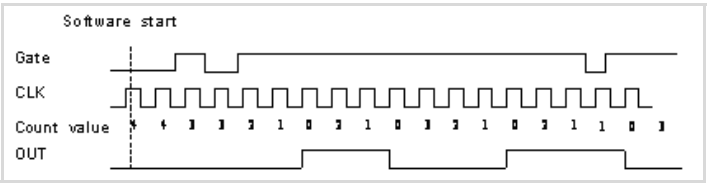


Figure 4-19: Mode 8 Operation

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Mode 9: Edge Separation Measurement

Measures the time differentiation between two different pulse signals. The first pulse signal is connected to GPTC_GATE and the second signal is connected to GPTC_AUX. It counts the clocks that pass by between the rising edge signal of two different pulses through the 40MHz internal clock or external clock. You can calculate the time period via the known clock frequency. The maximum counting width is 32-bit. Figure 4-20 illustrates how the counter value decreases in Edge Separation Measurement mode.

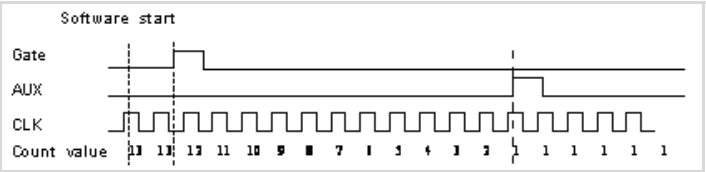


Figure 4-20: Mode 9 Operation

Mode 10: PWM Output

Aside from the 4-CH dedicated PWM outputs, the card's powerful timer/counter can also simulate a PWM (Pulse Width Modulation) output. By setting varying number of Pulse_initial_cnt and Pulse_length_cnt, you can get varying pulse frequency (Fpwm) and duty cycle (Dutypwm). Figure 4-21 illustrates the PWM output and the formula showing how to calculate the PWM frequency and duty cycle.

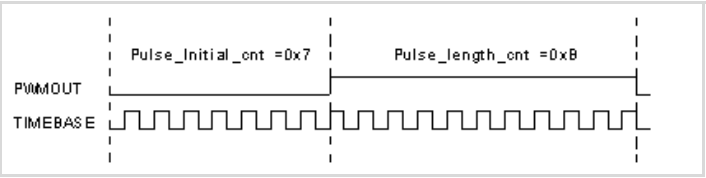


Figure 4-21: Mode 10 Operation

$$F_{PWM} = \frac{F_{Timebase}}{Pulse_initial_cnt + Pulse_length_cnt}$$

$$Duty_{PWM} = \frac{Pulse_length_cnt}{Pulse_initial_cnt + Pulse_length_cnt}$$

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4.4 Isolation Encoder

PCI-6202 features a combination of data acquisition and simple motion control with support for three encoder input sets which provide an alternative for step motor or servo motor's position feedback. The internal isolation provides easy encoder connection. The encoder sets are assigned in CN2.

Definition	Pin #		Definition
	1	35	
	2	36	
	3	37	
	4	38	
	5	39	
	6	40	
	7	41	
	8	42	
COM	9	43	COM
COM	10	44	COM
EA0+	11	45	EA1+
EA0-	12	46	EA1-
EB0+	13	47	EB1+
EB0-	14	48	EB1-
EZ0+	15	49	EZ1+
EZ0-	16	50	EZ1-
EORG0	17	51	EORG1
EA2+	18	52	EZ2+
EA2-	19	53	EZ2-
EB2+	20	54	EORG2
EB2-	21	55	Ext. 24V
Ext. GND	22	56	Ext. 24V
IGND	23	57	Ext. GND
IGND	24	58	IGND
VDD	25	59	IGND
VDD	26	60	
	27	61	
	28	62	
	29	63	
	30	64	
	31	65	
	32	66	
	33	67	
	34	68	

Table 4-6: Encoder Pins in CN2

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Encoder Isolation Input Module

Figure 4-22 illustrates the encoder isolation phase A, phase B and phase Z inputs module with 2500 Vrms protection.

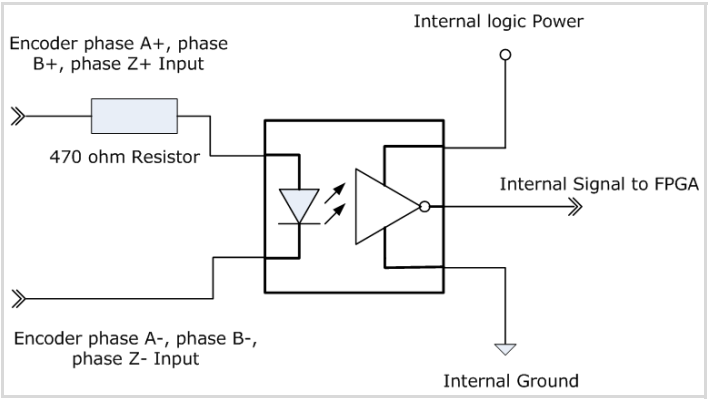


Figure 4-22: Encoder Isolation Input Module

The Encoder OGRx input is different from the encoder phase input since you need to add an external +24V power to drive the photo-couple. Figure 4-23 shows the OGRx input.

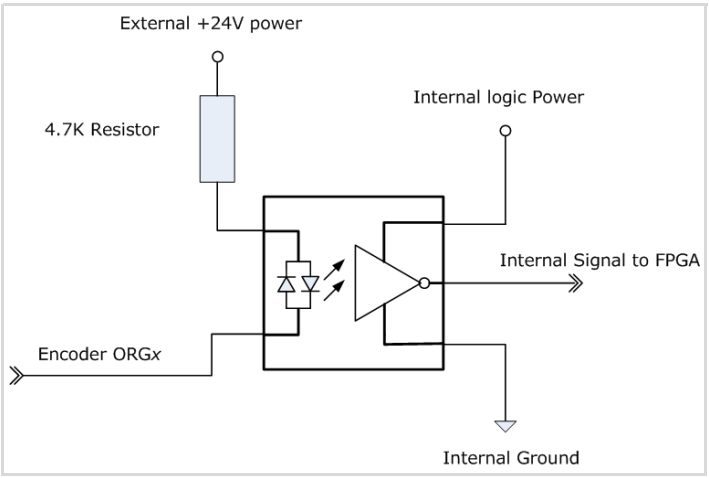


Figure 4-23: Encoder OGRx Input

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CW/CCW Encoder Mode

When GPTC is set to CW/CCW encoder mode and when the input EAx is connected to CW source signal and EBx is connected to CCW source signal, pulses from EAx will cause the counter to counter up and spin the motor clockwise. Otherwise, pulses from EBx will cause the counter to counter down and spin the motor counterclockwise. Figure 4-24 shows the increase/decrease of counter value in CW or CCW encoder mode.

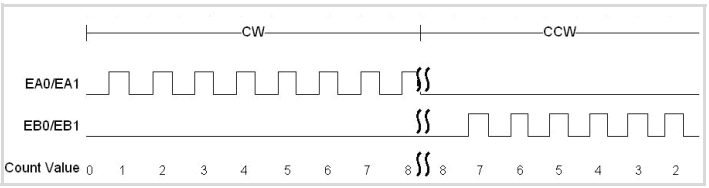


Figure 4-24: CW/CCW Encoder Timing

X1 Encoder Mode

In X1 encoder mode, if phase A (EA0/EA1) is advanced of phase B (EB0/EB1) in a quadrature cycle, the increment of counter value will be 1. Otherwise, if phase B is advanced of phase A in a quadrature cycle, the decrement of counter value will also be 1.

Figure 4-25 shows a quadrature cycle and the increment and decrement of counter value in X1 encoder mode. When phase A leads phase B, the counter value increases on the first rising edge of CLK after phase A goes high. When phase B leads phase A, the counter value decreases on the first rising edge of CLK after phase A goes low.

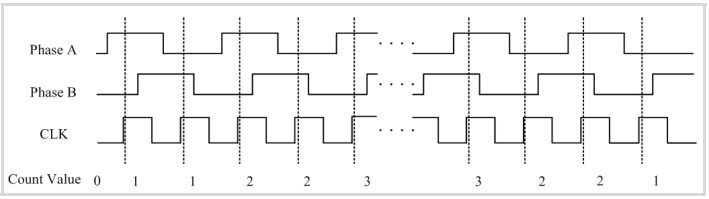


Figure 4-25: X1 Encoder Mode

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X2 Encoder Mode

This mode is similar to X1 Encoder Mode, except that the amount of counter value increases or decreases by two. Refer to Figure 4-26.

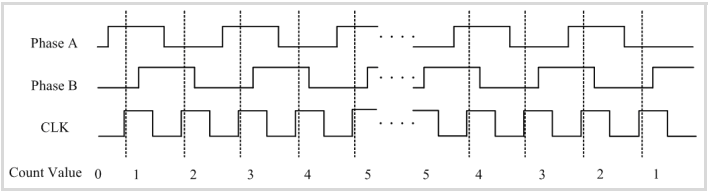


Figure 4-26: X2 Encoder Mode

X4 Encoder Mode

This mode is similar to X1 Encoder Mode, except that the amount of counter value increases or decreases by four. Refer to Figure 4-27.

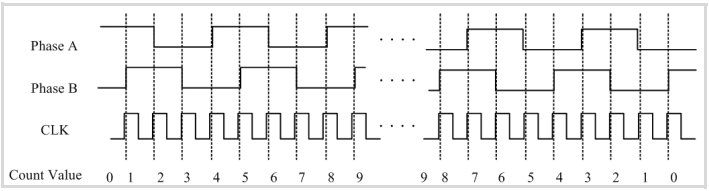


Figure 4-27: X4 Encoder Mode

Phase Z

Each encoder mode may use a third phase, phase Z, that is also frequently used for the index phase. You may decide if the counter needs to be reloaded a specified value when phase Z is at a logic high level with phase A and B at a specific logic condition.

You must ensure that the logic level of phase Z is high during at least a portion of the phase you specify for reload when you use phase Z. Otherwise, the counter does not reload.

In Figure 4-28, the reload phase is when the logic level of phase A is high, phase B is low, and phase Z is high in X1

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Encoder Mode. In addition, reloading takes higher priority than increment or decrement of counter value. The reload occurs within one maximum CLK period after the reload phase becomes true. After the counter value is reloaded, the counter continues to count as before.

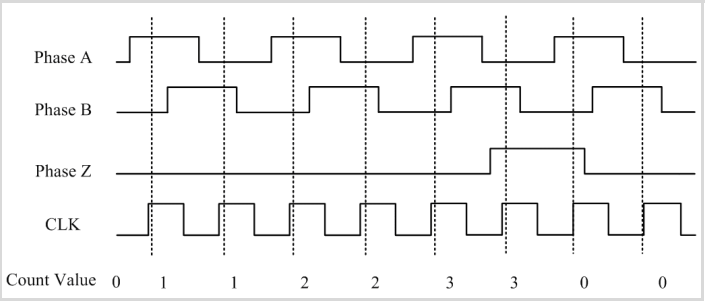


Figure 4-28: Phase Z

Original Signal (ORGx)

Original Signal (ORG0/ORG2/ORG1) is used with phase Z. With ORG enabled, a high level on phase Z and ORG causes the counter to reload with a specified value in a specified phase of the quadrature cycle. When you use ORG signal if it is at a low level and phase Z is at a high level, then counter reload is ignored.

Encoder Position Trigger

The PCI-6202 comes with a special encoder function. This function combines the encoder count function, digital output and system interrupt. When you set the pacer number and enable the encoder position trigger function, this function will start to count.

When the counting number is equal to the multiple of pacer number, the position trigger will output high in AFIx pin or generate an interrupt for software operation. The behavior may be selected by configuring this function. The output AFIx pulse width can still be configured as 200μs, 2ms, 20ms and 200ms by the software application.

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4.5 Isolated Digital Output

The isolated digital output circuit offers an open collector-type output and an isolation voltage of 2500 Vrms between the isolated output and the host power signals. Refer to Figure 4-29.

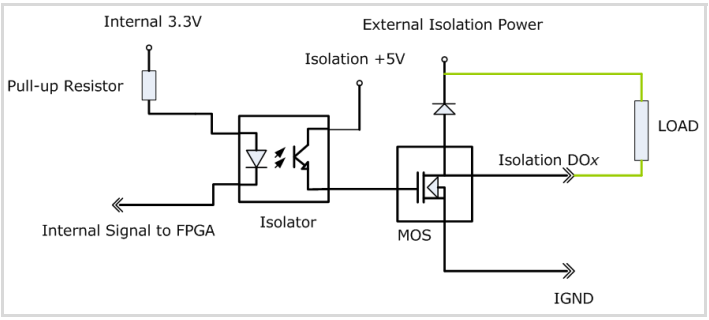


Figure 4-29: Isolated Digital Output

4.6 Isolated Digital Input

The isolated digital input circuit is equipped with a current-limit resistor and supports an input voltage of up to 24V. The isolation voltage between the isolated input and the host power signals is 2500 Vrms, as illustreated in Figure 4-30.

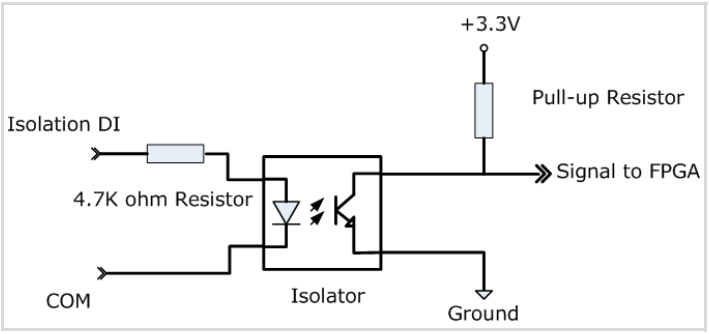


Figure 4-30: Isolated Digital Input

NOTE The 4.7 kΩ resistor constrains the maximum isolated digital input current.

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4.7 Trigger Sources

The PCI-6202 supports two trigger sources for analog input: software trigger and external digital trigger.

Software Trigger

This trigger mode does not need any external trigger source. The trigger asserts right after you execute the specified function calls to begin data acquisition.

External Digital Trigger

An external digital trigger occurs when a rising edge or a falling edge is detected on the digital signal connected to the PCI-6202's function I/O. You can set any DI line as external trigger pin. You may also easily program the trigger polarity via the ADLINK software drivers. Take note that the signal level of the external digital trigger signals should be TTL-compatible with a minimum 25 ns pulse.

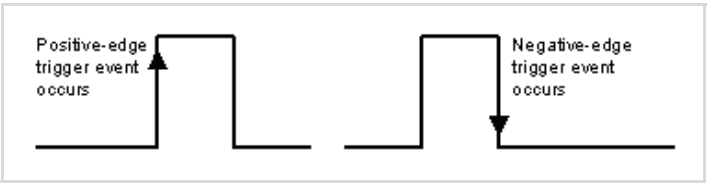


Figure 4-31: External Digital Trigger

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5 Calibration

Before shipment, the PCI-6202 is factory calibrated with Agilent 34410. The calibration is done by writing the associated calibration constants of TrimDACs firmware to the onboard EEPROM. TrimDACs firmware is the algorithm in the FPGA. Loading calibration constants is the process of loading the values of TrimDACs firmware stored in the onboard EEPROM.

NOTE A one year re-calibration interval is recommended. Contact your distributor or ADLINK to have your card re-calibrated.

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   - For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ADLINK is not responsible for any loss of data.
   - Please ensure the use of properly licensed software with our systems. ADLINK does not condone the use of pirated software and will not service systems using such software. ADLINK will not be held legally responsible for products shipped with unlicensed software installed by the user.
   - For general repairs, please do not include peripheral accessories. If peripherals need to be included, be certain to specify which items you sent on the RMA Request & Confirmation Form. ADLINK is not responsible for items not listed on the RMA Request & Confirmation Form.

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   - Damage caused by carelessness on the user's part during product transportation.
   - Damage caused by fire, earthquakes, floods, lightening, pollution, other acts of God, and/or incorrect usage of voltage transformers.
   - Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).
   - Damage caused by leakage of battery fluid during or after change of batteries by customer/user.
   - Damage from improper repair by unauthorized ADLINK technicians.
   - Products with altered and/or damaged serial numbers are not entitled to our service.
   - This warranty is not transferable or extendible.
   - Other categories not protected under our warranty.
4. Customers are responsible for shipping costs to transport damaged products to our company or sales office.
5. To ensure the speed and quality of product repair, please download an RMA application form from our company website: http://rma.adlinktech.com/policy. Damaged products with attached RMA forms receive priority.

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