NuDAQ®
PCI-7256
Latching Relay Actuator & Isolated D/I Cards
User's Guide



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Questions	
Product Model	
Environment to Use	OS_____ Computer Brand_____ M/B: CPU: Chipset: BIOS: Video Card: Network Interface Card: Other:
Challenge Description	
Suggestions to ADLINK	

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How to Use This Guide

This manual is for helping users to manipulate the PCI-7256. It is divided into 5 chapters.

- **Chapter 1, Introduction**, gives an overview of the product features, applications, and specifications.
- **Chapter 2, Installation**, describes how to install the PCI-7256. The layout of PCI-7256 is shown, and jumper setting for digital input filter, external LED connection and Board ID switch are specified. The connectors' pin assignments are also described.
- **Chapter3, Register Format**, describes the details of register format and structure of the PCI-7256. This information is very important for the programmers who want to control the hardware by low level programming.
- **Chapter 4, Operation Theorem**, describes how to operate the PCI-7256. The latching relay, isolated digital input and change-of-state functions are introduced. Some programming concepts are also described.
- **Chapter 5, C/C++ libraries**, describes the software utility and the library of PCI-7256, and also describes how to meet your requirements and help you to program your own software application.
- **Appendix A, relay Contact Protection Circuits,** provides the information about relay contact protection circuits.

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1

Introduction

The PCI-7256 Latching Relay Actuator and Isolated D/I card is a basic Digital I/O card for PCI bus computer in industrial applications.

This PCI-7256 provide 16 latching relay actuators and 16 opto-isolated digital inputs. All relays are Form C type. They are very suitable for ON/OFF control devices.

All of the digital input channels are identical non-polarity opto-isolated, each of them can be switchable by using RC filter or non-RC filter. All channels are isolated and suitable for collecting digital inputs in noisy environments. The function of “Change-of-State” (COS) interrupt is provided. It means when any of these digital inputs changes its state, an interrupt will be generated for user to handle this external event.

Using latching relays, the PCI-7256 has the advantage of power saving. The status of each latching relay output is reflected by a LED. When the latching relay is in SET condition, its corresponding in-board LED will turn ON, otherwise it is OFF.

Another useful feature is Board ID. It’s convenient for user to identify a specified card by setting up a switch when user have two or more PCI-7256 cards in one system.

The I/O signals are via a 68-pin SCSI connector.

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1.1 Features

The PCI-7256 Latching Relay Actuator and D/I Card provides the following advanced features:

- 32-bit PCI-Bus, Plug and Play
- 16 latching relay actuator outputs, the output status will remain when power-off
- 16 opto-isolated digital inputs for PCI-7256
- LED indicators to show the status of relays and can be read back
- Jumper selectable AC-filtered/non-AC-filtered input signals
- On-board relay driving circuits
- Change-of-State (COS) detection for digital input channels
- Digital input channel 0 & 1 interrupt
- Dry contact input available
- Board ID

1.2 Applications

- Industrial ON/OFF control
- External high power relay driving, Signal switching
- Laboratory automation
- Industrial automation
- Switch contact status sensing, limit switch monitoring,
- Cooperating with A/D and D/A cards to implement a data acquisition & control system

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1.3 Specifications

- **Digital input**

Input channels	16
Photo-coupler	PC-3H4
Input current	10 mA rated 50 mA max. for isolated input
Input Voltage	Up-to 24 V_{DC} or 24V_{AC} Logic Low: 0~2V Logic High 5~24V
Input impedance	4.7 KΩ
Input mode	Isolation AC-filter/ Non-AC-filter
Isolated voltage	2,500 Vrms channel-to-system

- **Relay Output**

Output channels	16
Relay type	16 DPDT (Form C)
Contact rating	125V_{AC} , 0.5 A 30V_{DC}, 1A
Breakdown voltage	1000 V_{rms}
Release time	3 msec
Operate time	3 msec
Contact resistance	60mΩ
Insulation resistance	1000M Ω min. (at 500 V_{DC})
Life expectancy (min. operations)	> 2 X 10^5 times at 1A 30V_{DC} > 10^5 times at 0.5A 125V_{AC}
Vibration Resistance	176.4m/s^2(18G), 10 to 55Hz at double amplitude of 3mm
LED indicators	Monitor SET/RESET status of each relay; external LED connectors could be applied
Power supply of Relay	+ 5V from the PCI-Bus

- **Isolated +5V Power Supply**

Output Voltage	+5V
Output Current	170mA max. (@ 40°C)

- **General Specifications**

Dimension	174 mm x 106 mm, standard PCI half size
Bus	32-bit PCI bus
Operating temperature	0 ~ 60 °C
Storage temperature	-20 °C ~ 80 °C

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Humidity	5 to 95% non-condensing

- **Power Consumption**

PCI-7256	+5V @ 340 mA (No relays energized) 980mA maximum when all relays are active simultaneously

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1.4 Software Support

ADLINK provides versatile software drivers and packages for users' different approach to built-up a system. We not only provide programming library such as DLL for many Windows systems, but also provide drivers for many software packages such as LabVIEW®, VEE™, InTouch™, InControl™, ISaGRAF™, and so on.

All the software options are included in the ADLINK CD. The non-free software drivers are protected with serial licensed code. Without the software serial number, you can still install them and run the demo version for two hours for demonstration purpose. Please contact ADLINK or the dealer to purchase the software license serial code.

1.4.1 Programming Library

For customers who are writing their own programs, we provide function libraries for many different operating systems, including:

- DOS Library: Borland C/C++ and, the functions descriptions are included in this user's guide.
- PCIS-DASK: Include device drivers and DLL for Windows 98, Windows NT and Windows 2000. DLL is binary compatible across Windows 98, Windows NT and Windows 2000. That means all applications developed with PCIS-DASK are compatible across Windows 98, Windows NT and Windows 2000. The developing environment can be VB, VC++, Delphi, BC5, or any Windows programming language that allows calls to a DLL. The user's guide and function reference manual of PCIS-DASK are in the CD. Please refer the PDF manual files under \Manual_PDF\Software\PCIS-DASK.

The above software drivers are shipped with the board. Please refer to the "Software Installation Guide" to install these drivers.

1.4.2 PCIS-LVIEW: LabVIEW® Driver

PCIS-LVIEW contains the VIs, which are used to interface with NI's LabVIEW® software package. The PCIS-LVIEW supports Windows 95/98/NT/2000. The LabVIEW® drivers are free and shipped with the board. You can install and use them without license. For detail information about PCIS-LVIEW, please refer to the user's guide in the CD.

(\Manual_PDF\Software\PCIS-LVIEW)

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1.4.3 PCIS-VEE: VEE Driver

The PCIS-VEE includes the user objects, which are used to interface with VEE software package. PCIS-VEE supports Windows 95/98/NT/2000. The VEE drivers are free and shipped with the board. You can install and use them without license. For detail information about PCIS-VEE, please refer to the user's guide in the CD.

(\Manual_PDF\Software\PCIS-VEE)

1.4.4 PCIS-OCX: ActiveX Controls

We suggest the customers who are familiar with ActiveX controls and VB/VC++ programming use PCIS-OCX ActiveX control components library for developing applications. PCIS-OCX is designed for Windows 98/NT/2000. For more detailed information about PCIS-OCX, please refer to the user's guide in the CD.

(\Manual_PDF\Software\PCIS-OCX\PCIS-OCX.PDF)

The above software drivers are shipped with the board. Please refer to the "***Software Installation Guide***" in the package to install these drivers.

Also ADLINK supplies an ActiveX control software *DAQBench*. DAQBench is a collection of ActiveX controls for measurement or automation applications. With DAQBench, you can easily develop custom user interfaces to display your data, analyze data you acquired or received from some other sources, and integrate with popular applications or data sources. For more detailed information about DAQBench, please refer to the user's guide in the CD.

(\Manual_PDF\Software\DAQBench\DAQBenchManual.PDF)

You can also get a free 4-hour evaluation version of DAQBench from the CD.

DAQBench is charged software. Please contact ADLINK dealer or ADLINK to purchase the software license.

1.4.5 PCIS-DDE: DDE Server and InTouch™

DDE stands for Dynamic Data Exchange specifications. The PCIS-DDE includes the PCI cards' DDE server. The PCIS-DDE server is free and included in the ADLINK CD. The DDE server can be used conjunction with any DDE client under Windows 98/NT/2000.

1.4.6 PCIS-ISG: ISaGRAF™ driver

The ISaGRAF WorkBench is an IEC1131-3 SoftPLC control program development environment. The PCIS-ISG includes ADLINK products' target

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drivers for ISaGRAF under Windows NT environment. The PCIS-ISG is included in the ADLINK CD. It needs license. Please contact ADLINK or dealer to purchase the license.

1.4.7 PCIS-ICL: InControl™ Driver

PCIS-ICL is the InControl driver which support the Windows NT. The PCIS-ICL is included in the ADLINK CD. It needs license. Please contact ADLINK or dealer to purchase the license.

1.4.8 PCIS-OPC: OPC Server

PCIS-OPC is an OPC server, which can link with the OPC clients. There are many software packages on the market can provide the OPC clients now. The PCIS-OPC supports the Windows 98, NT, and 2000. Please contact ADLINK or dealer to purchase the license.

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2

Installation

This chapter describes how to install the PCI-7256. The contents in the package and unpacking information that you should be careful are described.

2.1 What you have

In addition to the User's Manual, the package includes the following items:

- PCI-7256 latching relay and digital input cards
- ADLINK Software CD
- Software Installation Guide

If any of these items is missing or damaged, contact ADLINK or the dealer from whom you purchased the product. Save the shipping materials and carton in case you want to ship or store the product in the future.

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2.2 Unpacking

Your PCI-7256 card contains sensitive electronic components that can be easily damaged by static electricity.

The card should be operated on a grounded anti-static mat. The operator should be wearing an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the card module carton for obvious damage. Shipping and handling may cause damage to your module. Be sure there are no shipping and handling damages on the module before processing.

After opening the card module carton, extract the system module and place it only on a grounded antistatic surface with component side up.

Again inspect the module for damage. Press down on all the socketed IC's to make sure that they are properly seated. Do this only with the module place on a firm flat surface.

Note : DO NOT APPLY POWER TO THE CARD IF IT HAS BEEN DAMAGED.

You are now ready to install your PCI-7256.

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2.3 PCB Layout

The location of connector, switch and jumpers are shown in the figure2.1. They are described in the following sections.

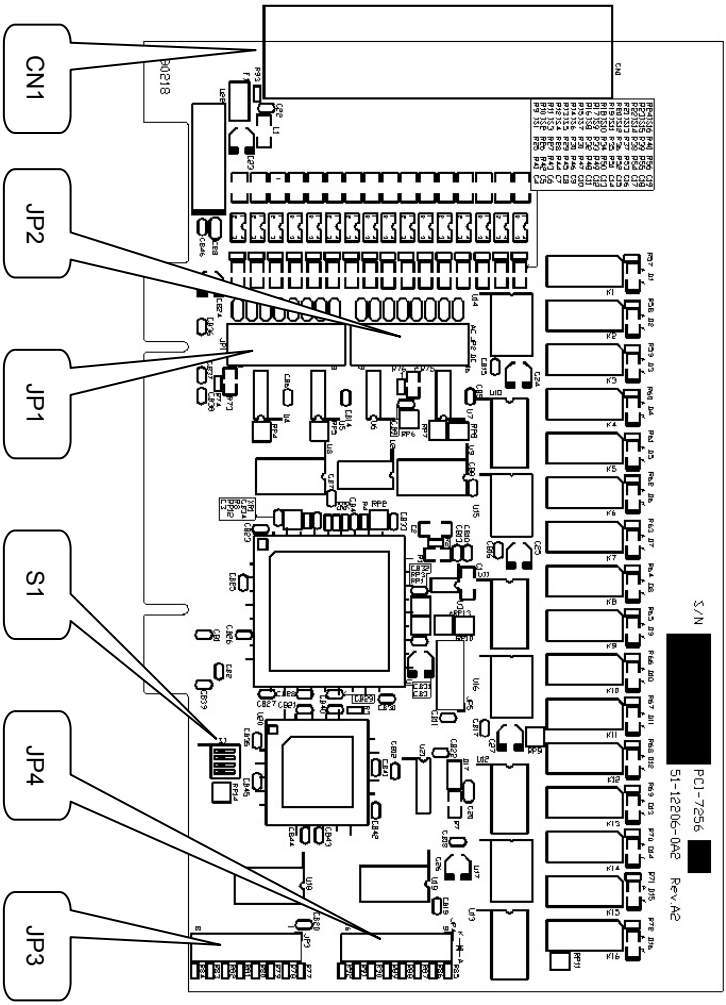


Figure 2.1 PCI-7256 PCB Layout

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2.4 Jumper Setting

The PCI-7256 is a 'plug and play' add-on card for PCI bus. It is not necessary for user to setup its base address and IRQ level to fit the hardware of your computer system. However, to fit user's versatile operation, there are still a few jumpers to set for the digital input.

The jumpers on PCI-7256 card are used to configure the digital input channels as *AC-Filtered* or *Non-AC-Filtered* inputs. Each digital input channel and their corresponding jumpers are shown in the following Table2.1.

JUMPER	INPUT SIGNAL
JP1	DI0 ~ DI7
JP2	DI8 ~ DI15

Table 2.1 The jumpers and DI channels

The default setting of the input signal selection is **Non-AC-Filtered** (DC signal input), which is shown as below :

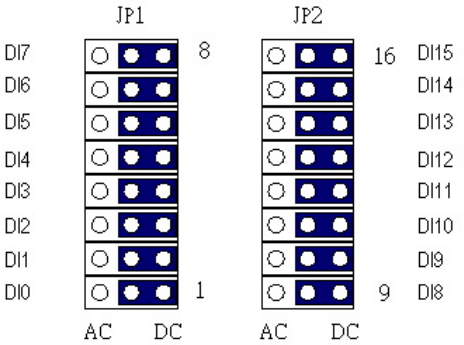


Figure 2.2 Default Input Signal Jumper Setting

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2.4 External LED connection

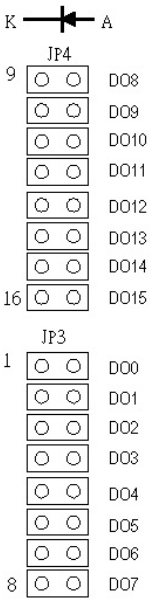


Figure 2.3 External LED connectors for relay status indication

The PCI-7256 card has 16 LEDs on board to indicate the operation status of the 16 relays. In addition, PCI-7256 also has 16 external LED connectors for users' applications. Utilizing external LEDs connecting with the JP3 and JP4, users can have their relays status shown on chassis ,panel or other apparatus. Only LED which have fordward voltage (V_f) lower than 3V can work normally. Each external LED connector has a current limiting resistor (330Ω) connecting with +5V power, so it's not necessary for user to add a resistor to limit the current flow through LED.

The direction of the external LED's connection is shown in Figure 2.3. Before connect user's LEDs on these connectors, make sure the LED is in the right direction.

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2.5 Board ID

When users plug two or more data acquisition cards in one system, it takes a lot of efforts to identify one specific card. For easier identification, PCI-7256 provides a Board ID function. According to a DIP switch configuration located in S1, users can assign a board ID to a specific card directly and access the card correctly through software programming. For more details about Board ID in programming, please refer to chapter 5.

Table 2.2 shows all of the switch setting conditions.

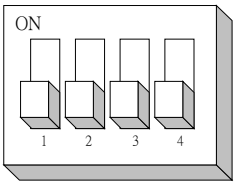


Figure 2.4 Board ID setting

Board ID	Switch No.			
	1	2	3	4
0	1	1	1	1
1	0	1	1	1
2	1	0	1	1
3	0	0	1	1
4	1	1	0	1
5	0	1	0	1
6	1	0	0	1
7	0	0	0	1
8	1	1	1	0
9	0	1	1	0
10	1	0	1	0
11	0	0	1	0
12	1	1	0	0
13	0	1	0	0
14	1	0	0	0
15	0	0	0	0

Note: 1=on, 0=off

Table 2.2 Board ID Setting Conditions

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2.6 Connector Pin Assignments

The PCI-7256 card is equipped with a 68-pin SCSI connector (CN1). The pin assignment of the SCSI connector is described by Figure 2.5.

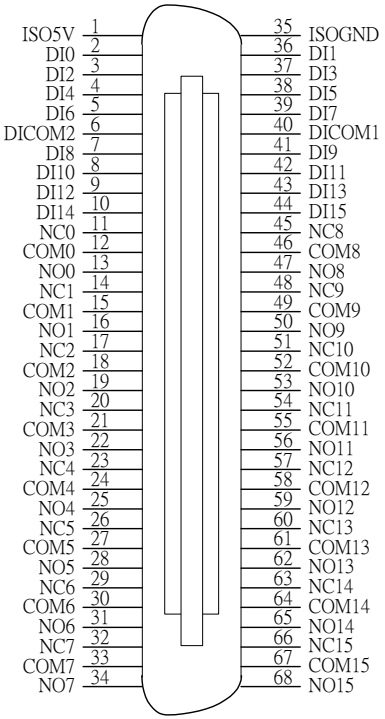


Figure 2.5 Pin Assignment of PCI-7256 CN1

Legend :

DI x	**:**	**Digital input channel x, x= 0~15**
DICOM x	**:**	**DI common ground group x, x=1 for DI channel 0~7, x=2 for DI channel 8~15**
ISO5V	**:**	**Isolated 5V power output**
ISOGND	**:**	**Isolated ground for +5V power output**
NO x	**:**	**Normal Open pin of relay x, x=0~15**
COM x	**:**	**Common pin of relay x, x=0~15**
NC x	**:**	**Normal Close pin of relay x, x=0~15**

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2.7 Termination Board Connection

The PCI-7256 is equipped with a SCSI 68-pin connector. The available termination board is DIN-68S/1S. The DIN-68S/1S is a general purpose 68 pin screw terminal with DIN socket. It is also equipped with a SCSI-68 pin cable that makes users install PCI-7256 more easily.

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3

Register Format

The detailed descriptions of the register format are specified in this chapter. This information is quite useful for the programmers who want to handle the card by low-level programming. However, we suggest user understand more about the PCI interface before starting low-level programming.

3.1 I/O Address Map

The 7256 registers are all 16-bit wide. Users can access these registers only by 16 bits I/O instructions. The control of the relays and status of the isolation input is by means of accessing registers. The following table shows the register map, including descriptions and their offset addresses relative to the base address.

Table 3.1 The register map of PCI-7256

Offset	Write	Read
0x00h	Relay Output CH. 0~7	--
0x02h	Relay Output CH. 8~15	Relay Output Read back CH.0~15
0x04h	---	Isolated Input CH. 0~15
0x06h	COS Setup Register	COS Latch Register
0x08h	Interrupt Control Register	Interrupt Status Register

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3.2 Relay Output Control Register

There are 16 latching relays on each PCI-7256 board. Each latching relay is controlled by two bits of the control register. The setting (0,1) means the latching relay is in RESET condition. Under the RESET condition, the normal open(NO) signal line is 'open' from the common(COM) line and the normal close(NC) signal line is connected with the common line. The setting (1,0) means the normal open signal line is now closed, while the NC signal is open. **For safety operation, do not fill the register with (1,1) or it will cause an uncertain output status of the relay.**

For more information about the latching relay and software function library, please refer to section 4.1 and 5.3, respectively.

Address: BASE + 0x00

Attribute: Write

7	6	5	4	3	2	1	0
DO3_S	DO3_R	DO2_S	DO2_R	DO1_S	DO1_R	DO0_S	DO0_R
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DO7_S	DO7_R	DO6_S	DO6_R	DO5_S	DO5_R	DO4_S	DO4_R

Address:BASE + 0x02

Attribute: Write

7	6	5	4	3	2	1	0
DO11_S	DO11_R	DO10_S	DO10_R	DO9_S	DO9_R	DO8_S	DO8_R
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DO15_S	DO15_R	DO14_S	DO14_R	DO13_S	DO13_R	DO12_S	DO12_R

DOx_R: Reset bit of relay output channel x, x=0~15

DOx_S: Set bit of relay output channel x, x=0~15

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3.3 Relay Output Read Back Register

The status of the latching relay can be readback from the readback register. If the relay is in RESET condition, the corresponding bit value is '0'. If the relay is in SET condition, the bit value is '1'

.

Address: BASE + 0x02

Attribute: Read

7	6	5	4	3	2	1	0
RBK7	RBK6	RBK5	RBK4	RBK3	RBK2	RBK1	RBK0
15	14	13	12	11	10	9	8
RBK15	RBK14	RBK13	RBK12	RBK11	RBK10	RBK9	RBK8

RBKx: Read back data of relay x, x=0~15

1: relay is in SET status

0: relay is in RESET status

3.4 Isolated Digital Input Register

There are 16 isolated input channels on PCI-7256 card. The status of the 16 channels can be read from the isolated input register. Each bit corresponds to each channel. The bit value "1" means the input logic is high and "0" menas the input logic is low.

Address: BASE + 0x04

Attribute: Read

7	6	5	4	3	2	1	0
DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
15	14	13	12	11	10	9	8
DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8

DIx: isolated digiatal input channel x, x=0~15

1: input voltage is in high level

0: input voltage is in low level

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3.5 COS Setup Register

The PCI-7256 provides a Change-of-State(COS) interrupt function on any one of digital input channel. This function allows users to monitor the status of input channels. By enabling the COS Setup registers, it will generate an interrupt when the corresponding channnel changes its state, whether a rising edge signal or a falling edge signal. For more detailed information, please refer to section 4.4.

Address: BASE + 0x06

Attribute: Write

7	6	5	4	3	2	1	0
COS SET7	COS SET6	COS SET5	COS SET4	COS SET3	COS SET2	COS SET1	COS SET0
15	14	13	12	11	10	9	8
COS SET15	COS SET14	COS SET13	COS SET12	COS SET11	COS SET10	COS SET9	COS SET8

COS SETx: change-of-state setup of DI channel x, x=0 ~15

1: enable the COS interrupt

0: disable the COS interrupt

3.6 COS Latch Register

When COS occurs, the COS Latch register will also latch the DI data. Once the user clear the interrupt request, the COS Latch register will be cleared automatically. The COS function releases the CPU from the burden of polling all of the input channels, and enables the computer to handle higher I/O performance.

Address: BASE + 0x06

Attribute: Read

7	6	5	4	3	2	1	0
CL7	CL6	CL5	CL4	CL3	CL2	CL1	CL0
15	14	13	12	11	10	9	8
CL15	CL14	CL13	CL12	CL11	CL10	CL9	CL8

CL x: COS latch register of DI channel x, x = 0 ~ 15

1: digital input voltage is in high level

0: digital input voltage is in low level

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3.7 Interrupt Control Register

There are two different interrupt modes in PCI-7256. In the first mode, users enable the COS interrupt function to monitor the enabled input channel's status whenever the status changes from 0 to 1 or 1 to 0. In the second mode, users can select digital input channel 0, channel 1 or both channels as the interrupt sources. In this mode, interrupt only assertes when the DI status changes from 0 to 1, i.e., rising edge. **Because the two different modes share the same interrupt signal in hardware, users are not allowed to enable these two modes at the same time.**

After processing the interrupt request event, users have to clear the interrupt request in order to handle another interrupt request. To clear the interrupt request, write 1 to the corresponding bit.

Address: BASE + 0x08

Attribute: Write

7	6	5	4	3	2	1	0
---	---	---	---	---	CH1 CLR	CH0 CLR	COS CLR
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
---	---	---	---	---	CH1 Int_EN	CH0 Int_EN	COS Int_EN

COS CLR (bit 0): write 1 to clear the COS interrupt.
1 : clear the COS interrupt
0 : no effect

CH0 CLR (bit 1): write 1 to clear DI channel 0 interrupt.
1 : clear DI channel 0 interrupt
0 : no effect

CH1 CLR (bit 2): write 1 to clear DI channel 1 interrupt.
1 : clear DI channel 1 interrupt
0 : no effect

COS Int_EN (bit 8): Write/Read
Change-of-State interrupt enable control
1 : enable
0 : disable

CH0 Int_EN (bit 9): Write/Read
DI channel 0 interrupt enable control
1 : enable
0 : disable

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CH1 Int_EN (bit 10): Write/Read

DI channel 1 interrupt enable control

1 : enable

0 : disable

The following table shows all possible combinations of interrupt source.

Table 3.2 Interrupt source set up

Interurpt type	Bit 10	Bit 9	Bit 8	IRQ source	IRQ trigger condition
Disable	0	0	0	Interrupt disable	--
Mode 1	0	0	1	COS interrupt	Change of state in the enabled channel
Mode 2	0	1	0	Ch.0 interrupt enable	Rising edge of DI channel 0
Mode 2	1	0	0	Ch.1 interrupt enable	Rising edge of DI channel 1
Mode 2	1	1	0	Ch.0 & 1 interrupt enable	Rising edge of DI channel 0 or 1
Forbidden	0	1	1	Not allowed (disable)	---
	1	0			
	1	1			

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3.8 Interrupt Status Register

When interrupt occurs, this register provides information for users to recognize the interrupt status and the interrupt setup condition.

Address: BASE + 0x08

Attribute: Read

7	6	5	4	3	2	1	0
---	---	---	---	---	CH1 Int. Status	CH0 Int. Status	COS Int. Status
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
---	---	---	---	---	CH1 Int_EN	CH0 Int_EN	COS Int_EN

COS Int. Status (bit 0): COS interrupt Status register

0: COS interrupt de-asserts

1: COS interrupt asserts

CH0 Int. Status (bit 1): Digital input channel 0 interrupt status

0: Ch0 interrupt de-asserts

1: Ch0 interrupt asserts

CH1 Int. Status (bit 2): Digital input channel 1 interrupt status

0: Ch1 interrupt de-asserts

1: Ch1 interrupt asserts

3.9 Handling PCI Controller Registers

The PCI bus controller adopted in PCI-7256 is PCI-9030 which is provided by PLX technology Inc. When users attempt to handle **low-level programming**, some registers in PCI-9030 should be noticed. The interrupt control register(INTCSR; 0x4Ch) of PCI-9030 takes charge of all interrupt information from local bus to PCI bus. When users want to develop their own interrupt function driver, both interrupt registers in PCI-9030 and in PCI-7256 have to work together. For more detailed information about the interrupt control register in PCI-9030, please refer to the PCI-9030 databook.

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In PCI-7256 software funciton library, we provide simple and easy-to-use functions to handle the procedure of interrupt. Using these functions, users don't need to care about the interrupt register in PCI controller. We suggest users use these functions instead of developing interrupt functions by themselves. For more information about PCI-7256 funciton library, please refer to Chapter 5.

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4

Operation Theorem

4.1 Latching Relay Output

One of the innovative features on PCI-7256 is the 16-channel latching relay output. The PCI-7256 contains only one type of latching relay : 2 coil Form C. Figure 4.1 shows the latching relay contact arrangement under RESET condition.

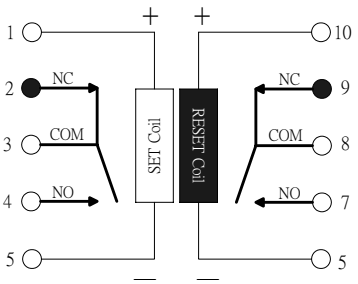


Figure 4.1 2 coil latching relay(RESET condition)

Each latching relay on PCI-7256 has two coils which serve as one SET coil and one RESET coil. To control the two-coil latching relay, we need two control bits: one for the SET coil, and one for the RESET coil. What we have to do is to energize the SET coil and deenergize the RESET coil when switching RESET condition to SET condition. After the contact switches to the opposite position at a steady state, we can cut out the current on the SET coil and the contact will not change any more. Thus the latching relay can achieve the advantage of power saving. Under the scheme of controlling latching relay, we define the SET condition control bits as (1,0) and the

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RESET condition control bits as (0,1). For more details about the latching relay control register, refer to section 3.3.

PCI-7256 also provides a software function for user to control the latching relays. Using this function, relay control is as simple as the general relay. Instead of writing 32-bit data to the relay output register, user only needs to prepare 16-bit data and each bit represents a relay's status. Value '1' represents SET condition and value '0' represents RESET condition. For more details about the relay output function library, refer to section 5.3.

The relay output contacts are rated for a maximum of 0.5A at $125V_{AC}$ (resistive), or 1A $30V_{DC}$. You should reduce these ratings for inductive loads. For more detailed information of relay contact, please refer to Appendix A.

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4.2 Isolated Digital Input

The PCI-7256 contains 16 opto-isolated digital input channels. The circuit diagram of the isolated input channel is shown below.

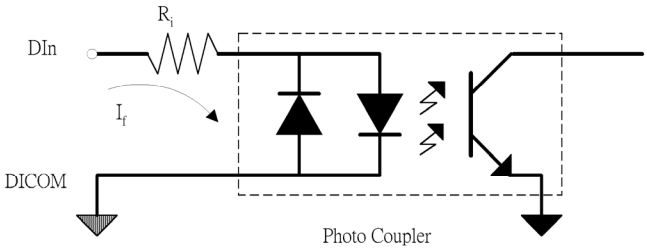


Figure 4.2 Photo Coupler

The digital input is first routed through a photo-coupler (PC3H4), so that the connection are not polarity sensitive whether useing positive or negative voltage.

In addition, a first order-filter with time constant about 1.5ms is provided to filter high frequency noise. The normal input voltage range for high state is 5 to 24V.

The PCI-7256 provides an isolated +5V power for dry contact input. When the external circuit has no voltage source(e.g. a switch), users can use the on board +5V to respond the change of external circuit. The maximum output current of the on board isolated power is 170mA (@40℃). Please pay attention to the current consumption of the external circuit not exceeding the limit. The dry contact architecture is shown in Figure 4.3.

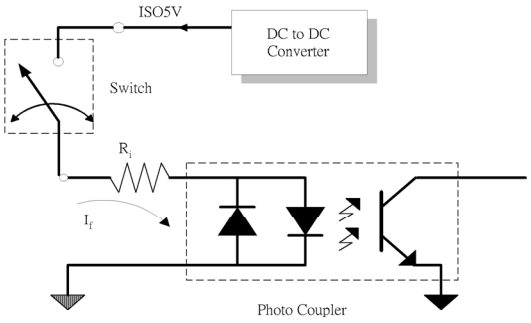


Figure 4.3 Dry contact

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4.3 Interrupt Architecture

PCI-7256 has a powerful dual interrupt routing scheme including change-of-state detection and interrupt sources on digital input channel 0 and channel 1. Using these interrupts well can make you handle more complicated information from outside enviroment and release your computer from a heavy burden in dealing with digital input data. Note that the dual interrupts do not mean the card occupies two IRQ levels.

There are two interrupt modes in PCI-7256, but you can only choose one of them at one time. Table3.2 shows all of the combinations of interrupt modes.

4.4 Change of State(COS) Interrupt

What is COS?

The COS (Change of State) means either the input state(logic level) changes from low to high, or from high to low. The COS detection circuit will detect the edge of level change. In the PCI-7256 card, the COS detection circuit is applied to all the input channels. When any channel changes its logic level, the COS detection circuit generates an interrupt request to PCI controller.

COS Detection

The following timing is an example of COS operation. All of the enabled DI channels' signal level change will be detected to generate the interrupt request.

While the interrupt request generates, the corresponding DI data will also be latched into the COS latch register. In our COS architecture, the DI data are sampled by a 8.25MHz clock. It means the pulse width of the digital input have to last longer than 122 ns, or the COS latch register won't latch the correct input data. The COS latch register will be erased after clearing the interrupt request.

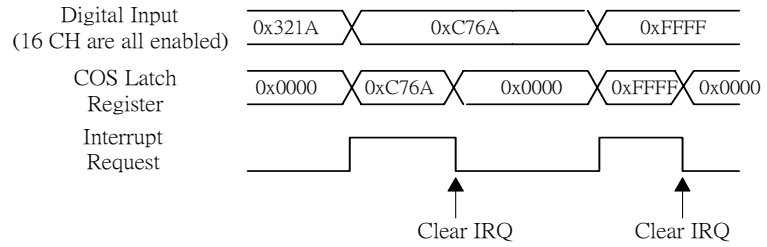


Figure4.4 Timing of COS

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5

C/C++ DOS Libraries

5.1 Programming Guide

5.1.1 Naming Convention

The functions of the NuDAQ PCI cards or NuIPC CompactPCI cards' software driver are using full-names to represent the functions' real meaning. The naming conventions are:

_{hardware_model}_{action_name}. **e.g. `_7256_Initial().`**

All functions in the PCI-7256 drivers are with 7256 as {hardware_model}.

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5.1.2 Data Types

We have defined some data types in Pci_7256.h. These data types are used by NuDAQ Cards' library. We suggest you use these data types in your application programs. The following table shows the data type names and their range.

Type Name	Description	Range
U8	8-bit ASCII character	0 to 255
I16	16-bit signed integer	-32768 to 32767
U16	16-bit unsigned integer	0 to 65535
I32	32-bit signed integer	-2147483648 to 2147483647
U32	32-bit single-precision floating-point	0 to 4294967295
F32	32-bit single-precision floating-point	-3.402823E38 to 3.402823E38
F64	64-bit double-precision floating-point	-1.797683134862315E308 to 1.797683134862315E309
Boolean	Boolean logic value	TRUE, FALSE

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5.2 _7256 Initial

@ *Description*

The PCI-7256 cards are initialized according to the card number. Because the PCI-7256 is PCI bus architecture and meets the plug and play design, the ***IRQ*** and ***base_address*** (pass-through address) are assigned by system BIOS directly. Every PCI-7256 card has to be initialized by this function before using other functions.

@ *Syntax*

U16 _7256_Initial (U16 *existCards, PCI_INFO *pciInfo)

@ *Argument*

existCards : The number of installed PCI-7256 cards. The returned value shows how many PCI-7256 cards are installed in your system.

pciInfo: It is a structure to memorize the PCI bus plug and play initiallization information which is decided by p&p BIOS. The PCI_INFO structure is defined in ACL_PCI.H. The base I/O address and the interrupt channel number is stored in pciinfo which is for reference.

@ *Return Code*

ERR_NoError, ERR_PCIBiosNotExist, ERR_BoardNoInit, ERR_InvalidBoardNumber

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5.3 _7256_DO

@ Description

This function is used to write data to digital output port which can energize the Latching relay SET/RESET coils. You can control all 16 RELAYs through _7256_DO by using this function. Althought the register map of latching relays is 32 bit width, we use 16-bit access to control the latching relay through this function. Bit '1' represent the SET condition (1,0), and Bit '0' represent the RESET condition (0,1).

@ Syntax

```
U16 _7256_DO (U16 boardID, U16 doData)
```

@ Argument

boardID :Board ID to the specific borad.
doData :value which will be written to digital output port.

@ Return Code

ERR_NoError, ERR_BoardNoInit

5.4 _7256_DO_Read_Back

@ Description

This function is used to read data back from digital output port control by 7256_DO function. There are 16-bit digital outputs on the PCI-7256. You can get back all RELAYs status (SET or RESET) by using this function.

@ Syntax

```
U16 _7256_DO_Read_Back (U16 boardID, U16 *doReadBackData)
```

@ Argument

boardID : Board ID to the specific borad.
diReadBackData : value read back from digital output port. '0' represents the latching relay is under RESET condition and '1' represents the latching relay is under SET condition.

@ Return Code

ERR_NoError, ERR_BoardNoInit

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5.5 _7256_DI

@ Description

This function is used to read data from digital input port. There are 16-bit digital inputs on the PCI-7256. You can get all 16 input data by using this function.

@ Syntax

```
U16 _7256_DI (U16 boardID, U16 *diData)
```

@ Argument

boardID : Board ID to the specific borad.
diData :return 16-bit value from digital input port.

@ Return Code

ERR_NoError, ERR_BoardNoInit

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5.6 _7256_COS_Channel

@ Description

This function is used to enable the COS channel.

@ Syntax

```
U16  _7256_COS_Channel (U16 boardID, U16 COS_Enable_Data)
```

@ Argument

boardID : Board ID to the specific borad.
COS_Enable_Data : COS channel enable. '1' enable the corresponding channel and '0' disable the corresponding channel.

@ Return Code

ERR_NoError, ERR_BoardNoInit

5.7 _7256_COS_Latch

@ Description

This function is used to latch digital input data after COS interrupt occurs.

@ Syntax

```
U16  _7256_COS_Latch (U16 boardID, U16 *COS_Latch_Data)
```

@ Argument

boardID :Board ID to the specific borad.
COS_Latch_Data :Digital input data when COS occurs. This register will be erased when clearing IRQ.

@ Return Code

ERR_NoError, ERR_BoardNoInit

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5.8 _7256_INT_Control

@ *Description*

This function is used to control the interrupt source of PCI-7256. For more details about interrupt sources, refer to section 3.7

@ *Syntax*

```
U16  _7256_INT_Control (U16 boardID, U16 COS_Enable, U16
CH0_Enable, U16 CH1_Enable)
```

@ *Argument*

boardID : Board ID to the specific borad.
COS_Enable: COS interrupt function enable/disable.
CH0_Enable: Digital input channel 0 interrupt enable/disable.
CH1_Enable: Digital input channel 1 interrupt enable/disable.
The possible combinations of interrupt source are shown in the following table.

CH1_Enable	CH0_Enable	COS_Enable	IRQ source	IRQ trigger condition
0	0	0	Interrupt disable	--
0	0	1	COS interrupt	Change of state in the enabled channel
0	1	0	Ch.0 interrupt enable	Rising edge of DI channel 0
1	0	0	Ch.1 interrupt enable	Rising edge of DI channel 1
1	1	0	Ch.0 & 1 interrupt enable	Rising edge of DI channel 0 & 1
0	1	1	Not allowed (disable)	---
1	0			
1	1			

@ *Return Code*

ERR_NoError, ERR_BoardNoInit, ERR_INTNotSet

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5.9 _7256_CLR_IRQ

@ Description

This function is used to clear the interrupt request of PCI-7256.

@ Syntax

```
U16  _7256_CLR_IRQ (U16 boardID, U16 COS_CLR, U16
CH0_CLR, U16 CH1_CLR)
```

@ Argument

boardID: Board ID to the specific borad.
COS_CLR: Write '1' to clear COS interrupt request and write '0' without any effect.
CH0_CLR: Write '1' to clear digital input channel 0 and write '0' without any effect.
CH1_CLR: Write '1' to clear digital input channel 1 and write '0' without any effect.

@ Return Code

ERR_NoError, ERR_BoardNoInit

5.10 _7256_GET_IRQ_Status

@ Description

This function is used to get the interrupt status of PCI-7256.

@ Syntax

```
U16  _7256_GET_IRQ_Status (U16 boardID, U16 *COS_Status,
U16 *CH0_Status, U16 *CH1_Status)
```

@ Argument

boardID: Board ID to the specific borad.
COS_Status: COS interrupt status. '1' represents interrupt asserts. '0' represents interrupt de-asserts.
CH0_Status: Digital input channel 0 interrupt status. '1' represents interrupt asserts. '0' represents interrupt de-asserts.
CH1_Status: Digital input channel 1 interrupt status. '1' represents interrupt asserts. '0' represents interrupt de-asserts.

@ Return Code

ERR_NoError, ERR_BoardNoInit

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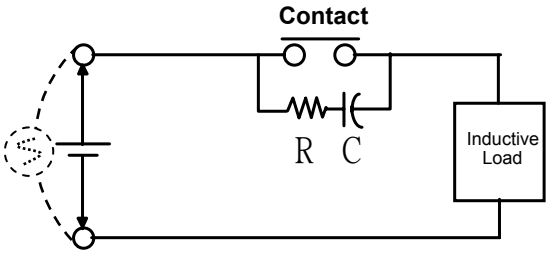
Appendix A. Relay Contact Protection Circuits

The contacts are the most important elements of relay constructions, Contact performance is conspicuously influenced by contact material, voltage and current values applied to the contacts.

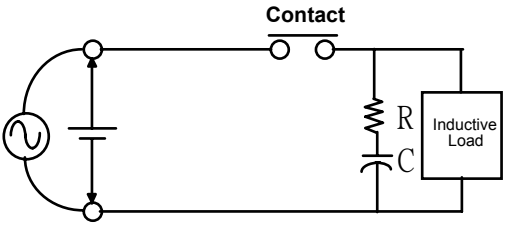
Another important issue is contact protection, a right contact protection circuit can suppress the counter EMF to a low level. However, note that incorrect use will result in an adverse effect. Typical contact protection circuits are given below :

1. RC Circuit

This circuit is suitable for DC application. If the load is a timer, leakage current flows through the RC circuit causing faulting operation.



The below circuit is suitable for both AC and DC applications. If the load is a relay or solenoid, the release time lengthens. It's effective when connected to both contacts if the power supply voltage is 24V or 48V and the voltage cross the load is 100 to 200V.



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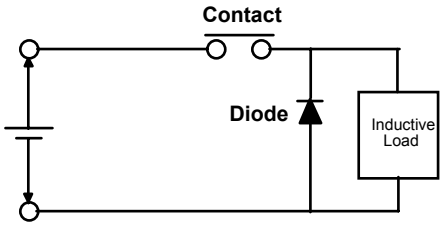
Device Selection:

As a guide in selecting R and C,
R : 0.5 to 1 Ω per 1V contact voltage
C : 0.5 to 1 μF per 1A contact current

Values vary depending on the properties of the capacity C acts to suppress the discharge the moment the contacts open. Resistor R acts to limit the current when the power is turned on the next time. Test to confirm. Use a capacitor with a breakdown voltage of 200 to 300V. Use AC type capacitors (non-polarized) for AC circuits.

2. Diode Circuit

This circuit is suitable for DC application. The diode connected in parallel causes the energy stored in the coil to flow to the coil in the form of current and dissipates it as joule heat at the resistance component of the inductive load. This circuit further delays the release time compared to the RC circuit.

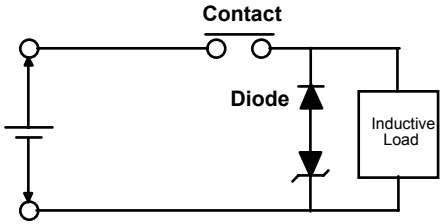


Device Selection:

Use a diode with a reverse breakdown voltage at least 10 times the circuit voltage and a forward current at least as large as the load current. In electronic circuits where the circuit voltages reverse breakdown voltage of above 2 to 3 times the power supply voltage.

3. Diode & Zener diode Circuit

This circuit is also suitable for DC application. Effective when the release time i the diode circuit is too long.



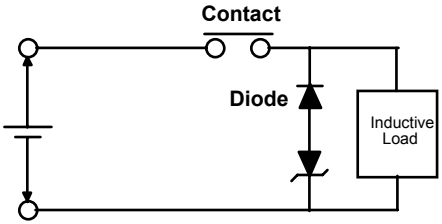
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Device Selection:

Use a zener diode with a zener voltage about the same as the power supply voltage.

4. Varistor Circuit

This circuit is also suitable for both AC & DC applications. Using the stable voltage characteristics of the varistor, this circuit prevents excessively high voltages from being applied across the contacts. This circuit also slightly delays the release time. Effective when connected to both contacts of the power supply voltage is 24 or 48V and the voltage across the load is 100 to 200 V.



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