ADLINK TECHNOLOGY INC.

NuDAQ® PCI-9222
NuDAQ® PCI-9223

16-bit High-Performance DAQ Card with
Programmable Function I/O

User's Manual

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Using this manual

1.1 Audience and scope

This manual guides you when using ADLINK high-performance data acquisition PCI card. The card's hardware, signal connections, and calibration information are provided for faster application building. This manual is intended for computer programmers and hardware engineers with advanced knowledge of data acquisition and high-level programming.

1.2 How this manual is organized

This manual is organized as follows:

Chapter 1 Introduction: This chapter introduces the ADLINK NuDAQ PCI-9222 and NuDAQ PCI-9223 cards including their features, specifications, software support information, and package contents.

Chapter 2 Hardware Information: This chapter presents the card's layout, connector pin assignment, signal descriptions, and analog input signal connection.

Chapter 3 Installation: This part describes the PCI-9222/PCI-9223 installation and configuration.

Chapter 4 Operation Theory: The operation theory of the PCI-9222/PCI-9223 card functions are discussed in this chapter. These include A/D conversion, D/A conversion, programmable function I/O, application function I/O, digital waveform acquisition, isolation encoder, and trigger sources.

Chapter 5 Calibration: The chapter offers information on how to calibrate the PCI-9222/PCI-9223 for accurate data acquisition and measurement.

Warranty Policy: This presents the ADLINK Warranty Policy terms and coverages.

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1.3 Conventions

Take note of the following conventions used throughout the manual to make sure that you perform certain tasks and instructions properly.

NOTE	Additional information, aids, and tips that help you perform particular tasks.

IMPORTANT	Critical information and instructions that you MUST perform to complete a task.

WARNING	Information that prevents physical injury, data loss, module damage, program corruption, and others when trying to complete a particular task.

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1 Introduction

The NuDAQ PCI-9222 (16-CH, 250 kS/s) and NuDAQ PCI-9223 (32-CH, 500 kS/s) are 16-bit high-performance DAQ cards with eight different input ranges. These cards also features a 2-CH, 16-bit analog output capable of up to 1 MS/s update rate, a 2-CH encoder input, and a programmable function I/O. The software-programmable function I/O supports a variety of applications including TTL digital I/O, high-speed DIO, general-purpose timer/counter, and PWM output.

These cards' analog input, analog output, and function I/O are capable of functioning simultaneously at full speed. If you need additional channels, you can synchronize these cards using the onboard SSI (System Synchronization Interface) bus. Suitable for mixed-signal tests, laboratory research, and factory automation, the PCI-9222 and PCI-9223 provide the best single-board solution with optimum integration capability of multiple tasks at an affordable price.

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1.1 Features

The PCI-9222/PCI-9223 comes with the following features:

- Supports a 32-bit 3.3 V or 5 V PCI bus
- PCI 2.3-compliant
- Up to 32-CH single-ended or 16-CH differential analog input
- Up to 500 kS/s sampling rate
- Programmable analog input gains of 1, 2, 4, 5, 8, 10, 20, 40
- 2-CH, 16-bit simultaneous analog output supports update rate of up to 1 MS/s
- Programmable function I/O supports the following modes:
  - 16-CH TTL DI and 16-CH TTL DO
  - 2 MHz 32-CH high-speed DIO
  - 4-CH 32-bit 80 MHz general-purpose timer/counter
  - 4-CH PWM outputs
- 2-CH 4 MHz dedicated encoder inputs, supporting AB phase, and CW/CCW
- Four DMA channels for A/D, D/A, and high-speed DIO
- External digital trigger for A/D, D/A, and high-speed DIO
- Multiple card synchronization through SSI (System Synchronization Interface)
- Auto-calibration feature

1.2 Applications

The PCI-9222 and PCI-9223 are ideal for these applications:

- Automotive testing
- Cable testing
- Transient signal measurement
- Waveform generation
- ATE
- Laboratory automation
- Biotech measurement
- Motor control feedback

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1.3 Specifications

Analog Input (AI)		
Hardware	**PCI-9222**	**PCI-9223**
Number of channels (programmable)	16	32
A/D converter	AD7685 or equivalent	AD7686 or equivalent
Maximum sampling rate Single-channel: Scanning:	 250 K samples/s 100 K samples/s	 500 K samples/s 200 K samples/s
Resolution	16-bit	
Input coupling	DC	
Programmable input range	±10 V, ±5 V, ±2.5 V, ±2 V, ±1.25 V, ±1 V, ±500 mV, ±250 mV	
Operational common mode voltage range	±8 V	
Overvoltage protection Power on: Power off:	 Continuous ±30 V Continuous ±30 V	 Continuous ±30 V Continuous ±30 V
FIFO buffer size	1K samples	
Data transfers	Programmed I/O Bus-mastering DMA with scatter/gather	
Channel Gain Queue configuration size	32 words	
Input impedance	1000G/150pF	
Trigger mode	Post-trigger with retrigger, Gated trigger	
Time-base source	Internal, 80 Mhz	
Electrical		
Function	23°C (±5°C)	
Offset error	±0.5 mV	
Gain error	±2 mV	
–3dB small signal bandwidth[1]	1.5 Mhz	
System noise[2]	0.5 mVrms	
1% THD large signal bandwidth		
CMRR[3]	93.5 dB	

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Spurious-free dynamic range (SFDR)	95 dB	88 dB
Signal-to-noise and distortion ratio (SINAD)	86 dB	84 dB
Total harmonic distortion (THD)	–94 dB	–90 dB
Signal-to-noise ration (SNR)	87 dB	86 dB
Effective number of bits (ENOB)	13.9	13.5
Settling time to full-scale step Multiple channels Multiple ranges	2 µs to 0.1% error 4 µs to 0.01% error	
Analog Output (AO)		
Hardware		
Function	23°C (±5°C)	
Number of channels	2	
D/A converter	DAC8812 or equivalent	
Maximum update range	1M sample/s (static)	
Resolution	16-bit	
FIFO size	512 samples, 2-CH sharing	
Data transfers	Programmed I/O, DMA	
Output range	±10 V	
Output coupling	DC	
Output impedance	0.010 (maximum)	
Protection	None	
Stability	Any passive load, up to 1500pF	
Power-on state	Around 0 V, steady-state	
Electrical		
Offset error Before calibration: After calibration:	 ±35 mV typical ±1 mV typical	
Gain error Before calibration: After calibration:	 ±1% of output max 0.001% of output max	
Slew rate	20 V/µs	
Rise time	0.67 µs	

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Fall time	0.7 µs
Settling time to 1% output error	3 µs
DNL	0.7 LSB
INL	1 LSB
Output driving	±5 mA (maximum)
Function I/O	
Number of channels	• 16-CH programmable function DI • 16-CH programmable function DO
Compatibility	TTL (single-ended) (supports 3.3 V and 5 V DI; 3.3 V DO)
Input voltage	• Logic low: VIL=0.8 V max; IIL=0.2 mA max • Logic high: VIH=2.0 V min; IIH=0.2 mA max
Output voltage	• Logic low: VOL=0.5 V max; IOL=10 mA max • Logic high: VOH=2.6 V min; IIH=10 mA max
Supported modes[4]	• 16-CH TTL DI and16-CH TTL DO • 4-CH 32-bit general-purpose timer/counters Clock source: Internal or External Max. source frequency: Internal 80 MHz External 10 MHz • 4-CH PWM outputs Duty cycle[5]:1-99% Modulation frequency: 20 MHz to 0.005 Hz • External digital trigger in and out • External analog input convert source • External analog output convert source • Digital waveform acquisition and generation
DI acquisition FIFO size	512 samples
DO acquisition FIFO size	512 samples
Data transfers	Programmed I/O, DMA

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Encoder Input (EI)	
Number of channels	2
Max. Input frequency	4 MHz
Encoder count	(2^{31}-1) bits
Photo isolator	NEC PS9115 or equivalent
Encoder modes	• CW/CCW • X1 AB phase encoder • X2 AB phase encoder • X4 AB phase encoder
Physical, Power, and Operating Environment	
Interface	PCI 2.3-compliant
Dimension	120 mm x 87 mm
I/O connector	2 x 68-pin female VHDCI connectors
Power requirement (typical)	• +5 VDC: 1.2A • +12 VDC: 760 mA • -12 VDC: 50 mA
Operating environment	• Ambient temperature: 0ºC to 45ºC • Relative humidity: 10% to 90%, non-condensing
Storage environment	• Ambient temperature: -20ºC to 80ºC • Relative humidity: 5% to 95%, non-condensing

Specifications are subject to change without notice.

1. -3dB small signal bandwidth: (Typical, 25ºC)

Input range	Bandwidth(-3dB)
±10 V	1500 kHz
±5 V	1400 kHz
±2.5 V	1400 kHz
±2 V	1400 kHz
±1.25 V	1400 kHz
±1 V	1400 kHz
±500 mV	1350 kHz
±250 mV	1250 kHz

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2. System Noise (LSBrms, including Quantization, Typical, 25ºC)

Input Range	System Noise
±10 V	0.78 LSBrms
±5 V	0.80 LSBrms
±2.5 V	0.98 LSBrms
±2 V	0.96 LSBrms
±1.25 V	0.77 LSBrms
±1 V	0.81 LSBrms
±500 mV	0.99 LSBrms
±250 mV	0.96 LSBrms

3. CMRR (DC to 60 Hz, Typical)

Input Range	System Noise
±10 V	93.5 dB
±5 V	96.3 dB
±2.5 V	103 dB
±2 V	104.2 dB
±1.25 V	106 dB
±1 V	106.2 dB
±0.5 V	110 dB
±0.25 V	118 dB

4. Only one of the following modes can be selected. These modes can not work at the same time. Refer to section 4.3 and 4.4.
5. Refer to Chapter 4.

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1.4 Unpacking Checklist

Before unpacking, check the shipping carton for any damage. If the shipping carton and/or contents are damaged, inform your dealer immediately. Retain the shipping carton and packing materials for inspection. Obtain authorization from your dealer before returning any product to ADLINK.

Check if the following items are included in the package.

- PCI-9222 or PCI-9223 multi-function DAQ card
- ADLINK All-in-One CD
- User's manual

If any of the items is damaged or missing, contact your dealer immediately.

CAUTION The card must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the card. Wear a grounded wrist strap when servicing.Software Support

1.5 Software Support

ADLINK provides comprehensive software drivers and packages to suit various user approach to building a system. Aside from programming libraries, such as DLLs, for most Windows-based systems, ADLINK also provides drivers for other application environment such as LabVIEW® and MATLAB®. ADLINK also provides ActiveX component ware for measurement and SCADA/HMI, and breakthrough proprietary software applications.

All software options are included in the ADLINK All-in-One CD.

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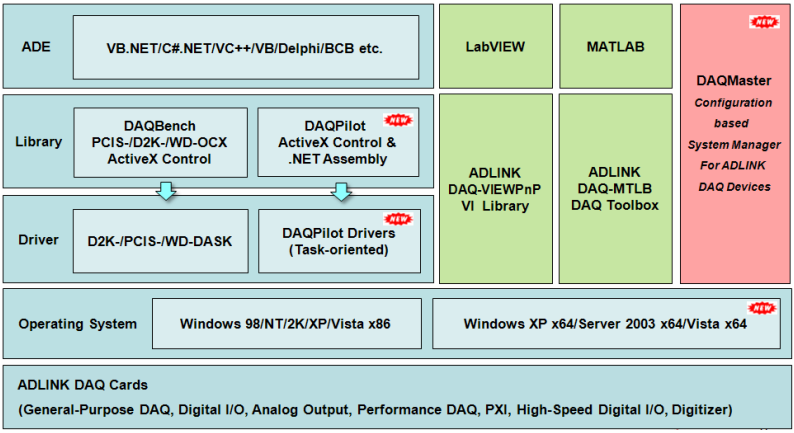


Figure 1-1: ADLINK Software Support Overview

Driver Support for Windows

DAQPilot

DAQPilot is a driver and SDK with a graphics-driven interface for various application development environments. DAQPilot comes as ADLINK's commitment to provide full support to its comprehensive line of data acquisition products and is designed for the novice to the most experienced programmer.

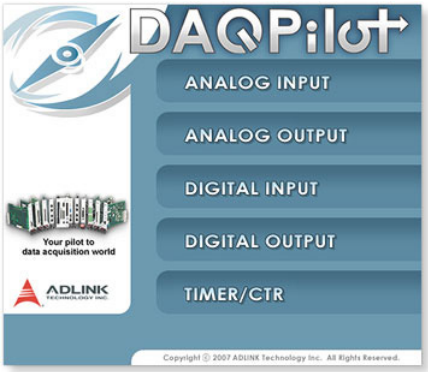


Figure 1-2: DAQPilot Main Interface

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As a task-oriented DAQ driver, SDK and wizard for Windows systems, DAQPilot helps you shorten the development time while accelerating your learning curve for data acquisition programming.

You can download and install DAQPilot at
http://www.adlinktech.com/TM/DAQPilot.html

DAQMaster

The ADLINK DAQMaster is a smart device manager that opens up access to ADLINK data acquisition and test and measurement products. DAQMaster delivers all-in-one configurations and provides you with a full support matrix to properly and conveniently configure ADLINK Test and Measurement products.

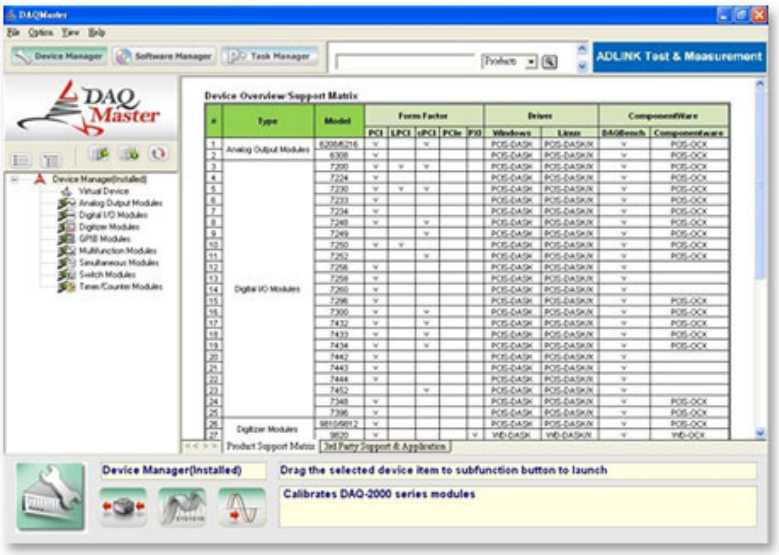


Figure 1-3: DAQMaster Device Manager

As a configuration-based device manager for ADLINK DAQ cards, DAQMaster enables you to manage ADLINK devices and interfaces, install and upgrade software applications, and manage ADLINK DAQPilot tasks.

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PCIS-DASK (Legacy Drivers and Support)

PCIS-DASK is composed of advanced 32-bit kernel drivers for customized DAQ application development. PCIS-DASK enables you to perform detailed operations and achieve superior performance and reliability from your data acquisition system. DASK kernel drivers now support the revolutionary Windows Vista® OS.

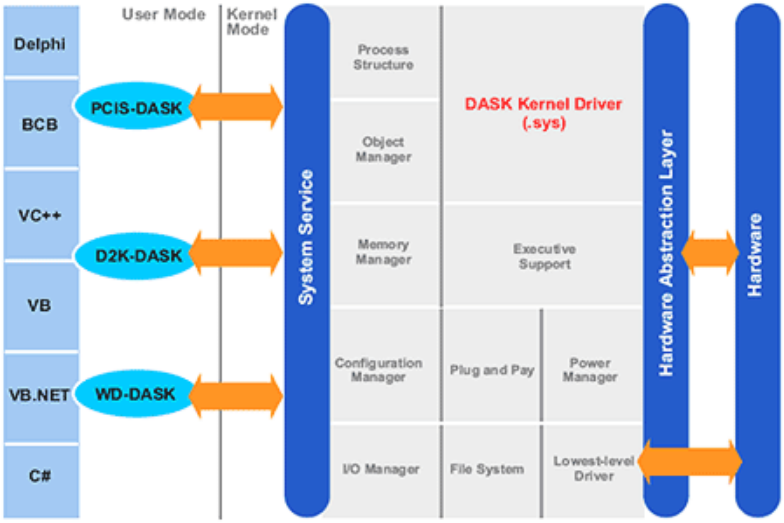


Figure 1-4: Legacy Software Support Overview

NOTE ADLINK strongly recommends installing DAQPilot and avoid using legacy DASK drivers. For current DASK driver users or those who do not have Internet access, we offer an installation CD. Contact your ADLINK distributor for details.

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PCIS-DASK drivers prepare legacy Windows users for Windows Vista and 64-bit editions of Windows. PCIS-DASK comes with the following features:

- Supports Windows Vista 32-bit or 64-bit editions
- Supports AMD64 and Intel x86-64 architectures
- Digitally-signed for Windows Vista 64-bit edition
- Utilizes WOW64 subsystem to ensure that 32-bit applications run normally on 64-bit editions of Windows XP, Windows 2003 Server, and Windows Vista without modification

For more information about Windows Vista support, visit http://www.adlinktech.com/TM/VistaSupport.html, or view the user's guide included in the ADLINK All-in-one CD.

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2 Hardware Information

This chapter provides information on the PCI-9222/PCI-9223 layout, connectors, and pin assignments.

2.1 Card Layout

Figure 2-1 shows the PCI-9222/PCI-9223 board layout and dimensions.

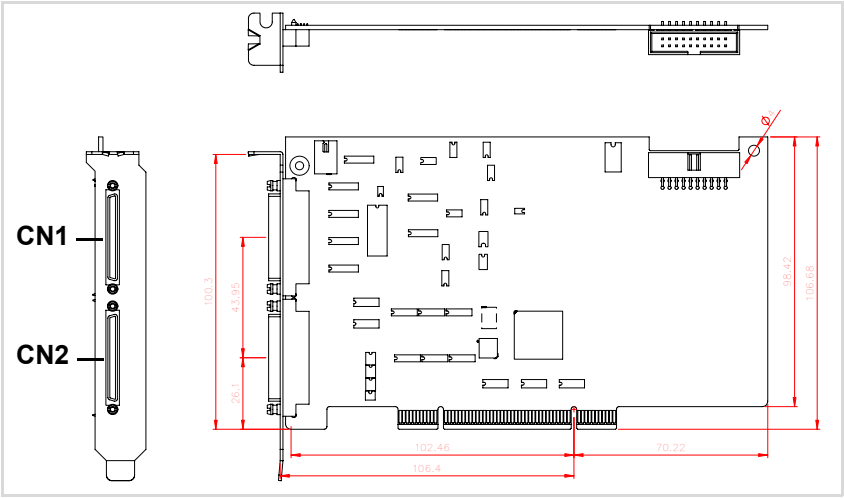


Figure 2-1: PCI-9222/PCI-9223 Layout

2.2 Connector Pin Assignment

The PCI-9222/PCI-9223 card is equipped with two VHDCI 68-pin connectors. CN1 is for analog input/output, while CN2 is for digital input/output and encoder functions. These cards also come with an SSI (System Synchronous Interface) connector. Attached a 20-pin ribbon connector (male) to the SSI when synchronizing the PCI-9222/PCI-9223 card with other cards.

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CN1 Pin Assignment

Definition	Pin #		Definition
AI0(AIH0)	34	68	AI8(AIL0)
AI1(AIH1)	33	67	AI9(AIL1)
AI2(AIH2)	32	66	AI10(AIL2)
AI3(AIH3)	31	65	AI11(AIL3)
AI4(AIH4)	30	64	AI12(AIL4)
AI5(AIH5)	29	63	AI13(AIL5)
AI6(AIH6)	28	62	AI14(AIL6)
AI7(AIH7)	27	61	AI15(AIL7)
AGND	26	60	AISENSE
NC	25	59	NC
NC	24	58	NC
NC	23	57	NC
NC	22	56	NC
NC	21	55	NC
NC	20	54	NC
NC	19	53	NC
NC	18	52	NC
AGND	17	51	AGND
AO0	16	50	AGND
AO1	15	49	AGND
NC	14	48	NC
NC	13	47	NC
NC	12	46	NC
NC	11	45	NC
NC	10	44	NC
NC	9	43	NC
NC	8	42	NC
NC	7	41	NC
NC	6	40	NC
NC	5	39	NC
NC	4	38	NC
NC	3	37	NC
NC	2	36	NC
NC	1	35	NC

Table 2-1: CN1 Pin Assignment for PCI-9222

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Definition	Pin #		Definition
AI0(AIH0)	34	68	AI16(AIL0)
AI1(AIH1)	33	67	AI17(AIL1)
AI2(AIH2)	32	66	AI18(AIL2)
AI3(AIH3)	31	65	AI19(AIL3)
AI4(AIH4)	30	64	AI20(AIL4)
AI5(AIH5)	29	63	AI21(AIL5)
AI6(AIH6)	28	62	AI22(AIL6)
AI7(AIH7)	27	61	AI23(AIL7)
AGND	26	60	AISENSE
AI8(AIH8)	25	59	AI24(AIL8)
AI9(AIH9)	24	58	AI25(AIL9)
AI10(AIH10)	23	57	AI26(AIL10)
AI11(AIH11)	22	56	AI27(AIL11)
AI12(AIH12)	21	55	AI28(AIL12)
AI13(AIH13)	20	54	AI29(AIL13)
AI14(AIH14)	19	53	AI30(AIL14)
AI15(AIH15)	18	52	AI31(AIL15)
AGND	17	51	AGND
AO0	16	50	AGND
AO1	15	49	AGND
NC	14	48	NC
NC	13	47	NC
NC	12	46	NC
NC	11	45	NC
NC	10	44	NC
NC	9	43	NC
NC	8	42	NC
NC	7	41	NC
NC	6	40	NC
NC	5	39	NC
NC	4	38	NC
NC	3	37	NC
NC	2	36	NC
NC	1	35	NC

Table 2-2: CN1 Pin Assignment for PCI-9223

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CN2 Pin Assignment

Definition	Pin #		Definition
GPI0/GPTC_CLK0	34	68	GPI8/GPTC_CLK2
GPI1/GPTC_UD0	33	67	GPI9/GPTC_UD2
GPI2/GPTC_GATE0	32	66	GPI10/GPTC_GATE2
GPI3/GPTC_AUX0	31	65	GPI11/GPTC_AUX2
GPI4/GPTC_CLK1	30	64	GPI12/GPTC_CLK3
GPI5/GPTC_UD1	29	63	GPI13/GPTC_UD3
GPI6/GPTC_GATE1	28	62	GPI14/GPTC_GATE3
GPI7/GPTC_AUX1	27	61	GPI15/GPTC_AUX3
DGND	26	60	DGND
GPO0/GPTC_OUT0	25	59	GPO8
GPO1/GPTC_OUT1	24	58	GPO9
GPO2/GPTC_OUT2	23	57	GPO10
GPO3/GPTC_OUT3	22	56	GPO11
GPO4	21	55	GPO12
GPO5	20	54	GPO13
GPO6	19	53	GPO14
GPO7	18	52	GPO15
DGND	17	51	DGND
DGND	16	50	DGND
DGND	15	49	DGND
+5Vout	14	48	DGND
NC	13	47	NC
NC	12	46	NC
NC	11	45	NC
NC	10	44	NC
E24V	9	43	NC
EGND	8	42	NC
IEA0+	7	41	IEA1+
IEA0-	6	40	IEA1-
IEB0+	5	39	IEB1+
IEB0-	4	38	IEB1-
IEZ0+	3	37	IEZ1+
IEZ0-	2	36	IEZ1-
IORG0	1	35	IORG1

Table 2-3: CN2 Pin Assignment for PCI-9222/PCI-9223

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CN1/CN2 Signal Descriptions

Below are the signal descriptions for the CN1/CN2 connectors:

Signal Name	Reference	Direction	Description
AIGND	—	—	Analog input ground. All three ground references (AIGND, AOGND, and DGND) are connected onboard.
AI<0..15> (16-CH)	AIGND	Input	**PCI-9222** Analog Input Channels 0~15. Each channel pair, AI<i, i+8> (I=0..7), can be configured as either two single-ended inputs or one differential input pair (marked as AIH<0..7> and AIL<0..7>).
AI<0..31> (32-CH)	AIGND	Input	**PCI-9223** Analog Input Channels 0~31. Each channel pair, AI<i, i+16> (I=0..15) can be configured as either two single-ended inputs or one differential input pair (marked as AIH<0..15> and AIL<0..15>).
AISENSE	AIGND	Input	Analog Input Sense. This pin serves as reference for any channels AI<0..63> in NRSE input configuration.
AO<0, 1>	AOGND	Output	Analog output channel <0, 1>
AOGND	-	-	Analog output ground
GPI<0..15>	DGND	Input	Function input <0..15>. See section 4.3.
GPO<0..15>	DGND	Output	Function output <0..15>. See section 4.3.
EA<0, 1>	Encoder Ground	Input	Encoder A Phase
EB<0, 1>	Encoder Ground	Input	Encoder B Phase

Table 2-4: CN1/CN2 Signal Description

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Signal Name	Reference	Direction	Description
EZ<0, 1>	Encoder Ground	Input	Encoder Z Phase
ORG<0, 1>	Encoder Ground	Input	Encoder Original Signal
Encoder +24V	Encoder Ground	Input	Encoder voltage input pin
GPTC_CLK<0, 3>	DGND	Input	GPTC<0, 3> clock source
GPTC_GATE<0, 3>	DGND	Input	GPTC<0, 3> gate
GPTC_OUT<0, 3>	DGND	Output	GPTC<0, 3> output
GPTC_UD<0, 3>	DGND	Input	GPTC<0, 3> up/down
NC	NC	NC	No connection

Table 2-4: CN1/CN2 Signal Description

SSI Connector Pin Assignment

Definition	Pin#		Definition
RESERVED	**1**	**2**	DGND
SSI_ADCONV	**3**	**4**	DGND
SSI_DAWR	**5**	**6**	DGND
RESERVED	**7**	**8**	DGND
RESERVED	**9**	**10**	DGND
SSI_AD_TRIG	**11**	**12**	DGND
SSI_DA_TRIG	**13**	**14**	DGND
RESERVED	**15**	**16**	DGND
RESERVED	**17**	**18**	DGND
RESERVED	**19**	**20**	DGND

Table 2-5: SSI Connector Pin Assignment

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SSI Connector Signal Description

Signal Name	Setting	Direction	Description
SSI_ADCONV	Master	Output	Sends out the ADCONV
	Slave	Input	Accepts the SSI_ADCONV to replace the internal ADCONV signal
SSI_AD_TRIG	Master	Output	Sends the internal AD_TRIG out
	Slave	Input	Accepts the SSI_AD_TRIG as the digital trigger signal
SSI_DAWR	Master	Output	Sends the DAWR out
	Slave	Input	Accepts the SSI_DAWR to replace the internal DAWR signal
SSI_DA_TRIG	Master	Output	Sends the DA_TRIG out
	Slave	Input	Accepts the SSI_DA_TRIG as the digital trigger signal

Table 2-6: SSI Connector Signal Description

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2.3 Analog Input Signal Connection

The PCI-9222 provides up to 16 single-ended or 8 differential analog input channels, while the PCI-9223 offers up to 32 single-ended or 16 differential analog input channels. You can fill the Channel Gain Queue to get the desired input signal type combination. The analog signal can be converted to digital value by the A/D converter. To avoid ground loops and obtain a more accurate measurement from the A/D conversion, it is important to understand the type of signal source and how to choose the analog input modes: Referenced Single-Ended (RSE), Non-Referenced Single-Ended (NRSE), and Differential Input (DIFF).

Types of Signal Sources

Floating Signal Sources

A floating signal source means it is not connected in any way to the building's ground system. A device with an isolated output is a floating signal source. This includes optical isolator outputs, transformer outputs, and thermocouples.

Ground-Referenced Signal Sources

A ground-referenced signal means it is connected in some way to the building's ground system. That is, the signal source is already connected to a common ground point with respect to the PCI-9222/PCI-9223, assuming that the computer is plugged into the same power system. Non-isolated outputs of instruments and devices that plug into the building's power systems are ground-referenced signal sources.

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Input Configurations

Single-ended Connections

A single-ended connection is used when the analog input signal is referenced to a ground that can be shared with other analog input signals. There are two types of single-ended connections: RSE and NRSE configuration. In RSE configuration, the PCI-9222/PCI-9223 card provides the grounding point for external analog input signals and is suitable for floating signal sources. In NRSE configuration, the card does not provide the grounding point. The external analog input signal provides its own reference grounding point and is suitable for ground-referenced signals.

Referenced Single-ended (RSE) Mode

In referenced single-ended mode, all the input signals are connected to the ground provided by the PCI-9222/PCI-9223. This mode is suitable for connections with floating signal sources. Figure 2-2 shows an illustration of this mode. Take note that when two or more floating sources are connected, these sources will be referenced to the same common ground.

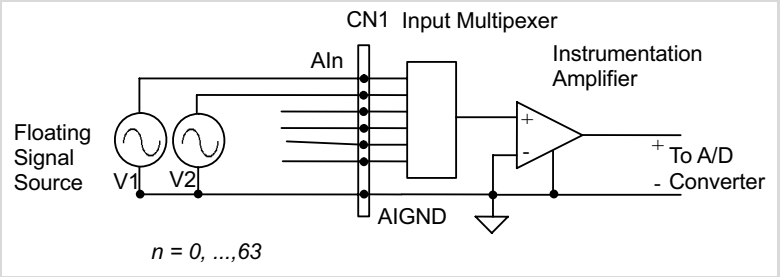


Figure 2-2: Floating Source and RSE Input Connections

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Non-Referenced Single-Ended (NRSE) Mode

To measure ground-referenced signal sources, which are connected to the same ground point, you can connect the signals in NRSE mode. Figure 2-3 illustrates the connection. The signal's local ground reference is connected to the negative input of the instrumentation amplifier (AISENSE pin on CN1 connector), and the common-mode ground potential between signal ground and the onboard ground will be rejected by the instrumentation amplifier.

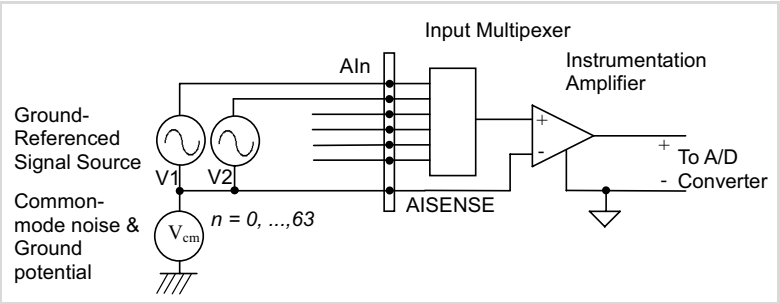


Figure 2-3: Ground-referenced Sources and NRSE Input Connections

Differential input mode

The differential input mode provides two inputs that respond to signal voltage difference between them. If the signal source is ground-referenced, the differential mode can be used for the common-mode noise rejection. Figure 2-4 shows the connection of ground-referenced signal sources under differential input mode.

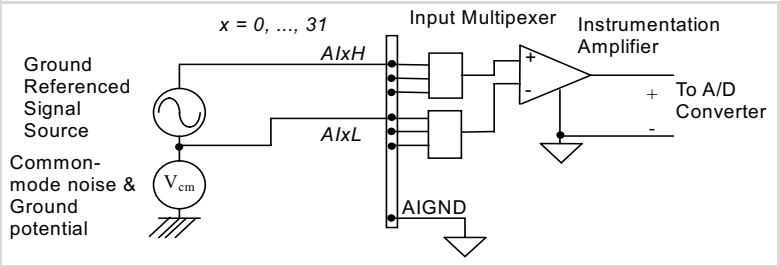


Figure 2-4: Ground-referenced Source and Differential Input

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Figure 2-5 shows how to connect a floating signal source to the PCI-9222/PCI-9223 card in differential input mode. For floating signal sources, you need to add a resistor at each channel to provide a bias return path. The resistor value should be about 100 times the equivalent source impedance. If the source impedance is less than 100 ohms, you can simply connect the negative side of the signal to AIGND as well as the negative input of the instrumentation amplifier without any resistors. In differential input mode, less noise couples into the signal connections than in single-ended mode.

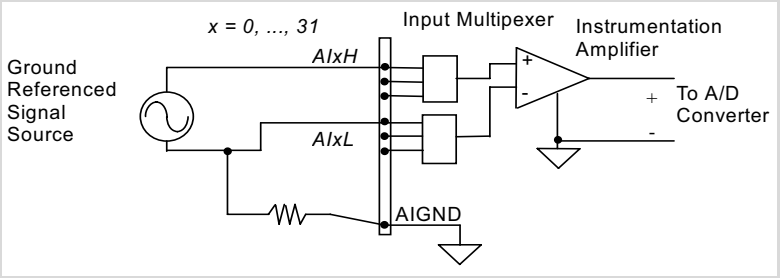


Figure 2-5: Floating Source and Differential Input

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3 Installation

3.1 Before You Proceed

The PCI-9222/PCI-9223 card has electro-static sensitive components that can be easily damaged by static electricity. The card must be handled on a grounded anti-static mat. The operator must wear an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the card module carton for damages. Shipping and handling could cause damage to the module. Make sure that the card has no damage before installing it.

After opening the card package, get the module and place it on a grounded anti-static surface with component side up, then carefully inspect the module for any damage. Press down all socketed ICs to make sure that they are properly seated. Do this only with the module placed on a firm flat surface.

WARNING Do not apply power to the card if it is damaged.

3.2 Installing the Card

IMPORTANT Install the card driver before you install the card into your computer system. Refer to section 1.5 for driver support information.

To install the card:

1. Turn off the system/chassis and disconnect the power plug from the power source.
2. Remove the system/chassis cover.
3. Select the PCI slot that you intend to use, then remove the bracket opposite the slot, if any.
4. Align the card connectors (golden fingers) with the slot, then press the card firmly until the card is completely seated on the slot.
5. Secure the card to the chassis with a screw.

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6. Replace the system/chassis cover.
7. Connect the power plug to a power source, then turn on the system.

3.3 Configuring the Card

As a plug and play component, the card requests an interrupt number through its PCI controller. The system BIOS responds with an interrupt assignment based on the card information and on known system parameters. These system parameters are determined by the installed drivers and the hardware load detected by the system.

Configuration

The card configuration is done on a card-by-card basis for all PCI cards on your system. Because configuration is controlled by the system and the software, there is no jumper setting required for base address, DMA, and interrupt IRQ.

The configuration is subject to change with every boot of the system as new PCI cards are added or removed.

Troubleshooting

If your system fails to boot or if you experience erratic operation with your PCI card in place, this is likely caused by an interrupt conflict (such as when the BIOS Setup is incorrectly configured). Refer to the BIOS documentation that came with the system for details.

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4 Operation Theory

The operation theory of each function in the PCI-9222/PCI-9223 card is described in this chapter. These functions include A/D conversion, D/A conversion, encoder, programmable function I/O, and more. The operation theory can help you understand how to configure and program the PCI-9222/PCI-9223 card.

4.1 Block Diagram

There are 32/16 single-ended channels of 16-bit A/D input and 2 single-ended channels of 16-bit D/A output available in the PCI-9222/PCI-9223 card. By switching the multiple front-end multiplexers, all A/D input channels are connected to one ADC (ADI AD7685/7686 or equivalent). As for the D/A function, 2 analog output channels are generated by one DAC chip (TI DAC8812). The ADC/DAC controller and all timing control logics are implemented by the FPGA.

The PCI-9222/PCI-9223 has calibration circuits to provide high-performance and low-temperature drift DC signal source. The calibration data are saved in the EEPROM. Combining FIFO control logic and simultaneous update characteristic, the PCI-9222/PCI-9223 offers a 2-channel simultaneous basic waveform generation. The general purpose function digital IO and encoders are controlled directly by the FPGA. Refer to Figure 4-1.

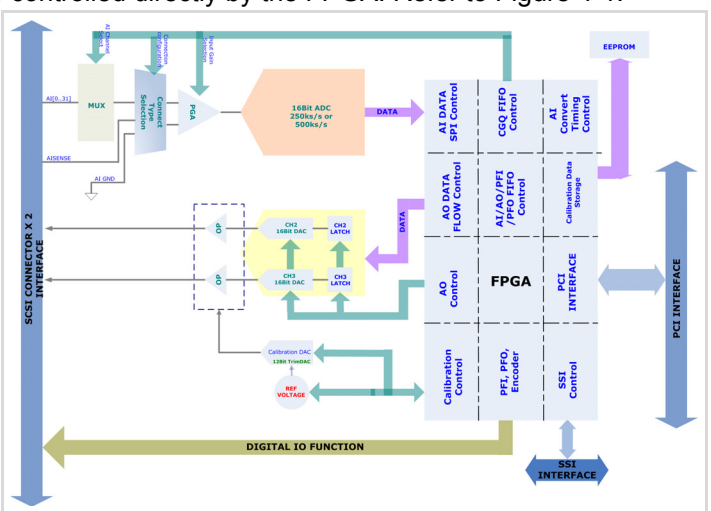


Figure 4-1: PCI-9222/PCI-9223 Block Diagram

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4.2 A/D Conversion

When using an A/D converter, you must know about the properties of the signal to be measured and decide which channel to use and how to connect the signals to the card. Refer to section 2.3. In addition, you should define and control the A/D signal configurations, including channels, gains, and signal types.

The A/D acquisition is initiated by a trigger source and you must decide how to trigger the A/D conversion. The data acquisition will start once a trigger condition is matched.

After the end of an A/D conversion, the A/D data is buffered in a data FIFO. The A/D data can now be transferred into the system's memory for further processing.

Software Polling and Scan Acquisition modes are discussed below as well as timing, trigger modes, trigger sources, and transfer methods.

PCI-9222/PCI-9223 AI Circuitry

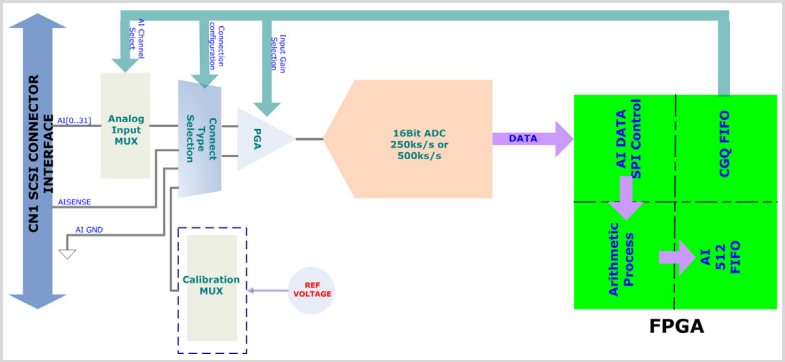


Figure 4-2: PCI-9222/PCI-9223 AI Circuitry

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AI Data Format

The data format of the acquired 16-bit A/D data is 2's complement coding. Table 4-1 shows the valid input ranges and the ideal transfer characteristics.

Description	Bipolar Analog Input Range				Digital code
Full-scale Range	±10V	±5V	±2.5V	±2V	
Least significant bit	305.2uV	152.6uV	76.3uV	61.03uV	
FSR-1LSB	9.999695V	4.999847V	2.499924V	1.999938V	7FFF
Midscale +1LSB	305.2uV	152.6uV	76.3uV	61.03uV	0001
Midscale	0V	0V	0V	0V	0000
Midscale -1LSB	-305.2uV	-152.6uV	-76.3uV	-61.03uV	FFFF
-FSR	-10V	-5V	-2.5V	-2V	8000

Table 4-1: Bipolar Analog Input Range and Output Digital Code

Description	Bipolar Analog Input Range				Digital code
Full-scale Range	±1.25V	±1V	±0.5V	±0.25V	
Least significant bit	38.14uV	30.51uV	15.25uV	7.62uV	
FSR-1LSB	1.249961V	0.999969V	0.499984V	0.249992V	7FFF
Midscale +1LSB	38.14uV	30.51uV	15.25uV	7.62uV	0001
Midscale	0V	0V	0V	0V	0000
Midscale -1LSB	-38.14uV	-30.51uV	-15.25uV	-7.62uV	FFFF
-FSR	-1.25V	-1V	-0.5V	-0.25V	8000

Table 4-2: Bipolar Analog Input Range and Output Digital Code

Software Conversion with Polling Data Transfer Acquisition Mode (Software Polling)

Considered the most convenient way to acquire a single A/D data, the A/D converter starts one conversion whenever the dedicated software command is executed. The software then polls the conversion status and reads back the A/D data when it is available.

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This method is suitable for applications that need to process A/D data in real time. In this mode, the timing of the A/D conversion is fully controlled by the software. The A/D conversion rate is decided by the software timer and may not be totally precise.

In Software Polling, the channel, gain, and input configuration (RSE, NRSE, or DIFF) may be specified for each single-point measurement. For example:

Ch2 with ± 5V input range and single-ended NRSE connection

Continuous Acquisition (Scanning) Mode

Continuous A/D Conversion Clock Source

When the onboard ADC receives a conversion clock signal, it will trigger an A/D conversion. The conversion clock of PCI-9222/PCI-9223 may come from three different clock sources: internal hardware timer, general purpose input channel (GPI 0 ~ GPI 7), or SSI (system synchronization interface). Refer to Figure 4-3.

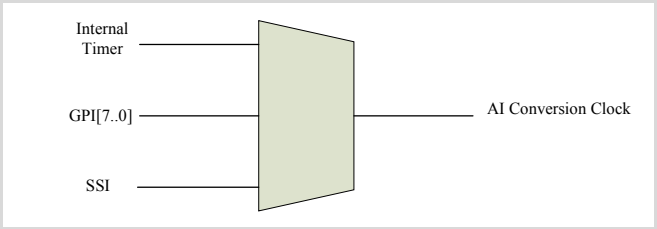


Figure 4-3: Continuous A/D Conversion Clock Source Block Diagram

You can choose conversion clock source by setting AI source configuration. But if users want to get the precision acquisition, the internal hardware timer is recommended.

Continuous Scanning with Internal Hardware Timer

It is recommended that you use this mode if your applications need a fixed and precise A/D sampling rate. You can accurately program the period between conversions of individual channels. There are at least four counters that have to be specified:

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- SI_counter (32-bit)
  Specify the Scan Interval = SI_counter / Timebase
- SI2_counter (24-bit)
  Specify the Data Sampling Interval = SI2_counter/Timebase
- PSC_counter (31-bit)
  Specify the Post Scan Counts after a trigger event
- NumChan_counter (8-bit)
  Specify the number of samples per scan

The acquisition timing and the meaning of the four counters are illustrated in Figure 4-4.

Timebase Clock Source

In scan acquisition mode, all A/D conversions start on the output of counters which use Timebase as the clock source. Through the software, you can specify the Timebase as the internal clock source (onboard 80 MHz).

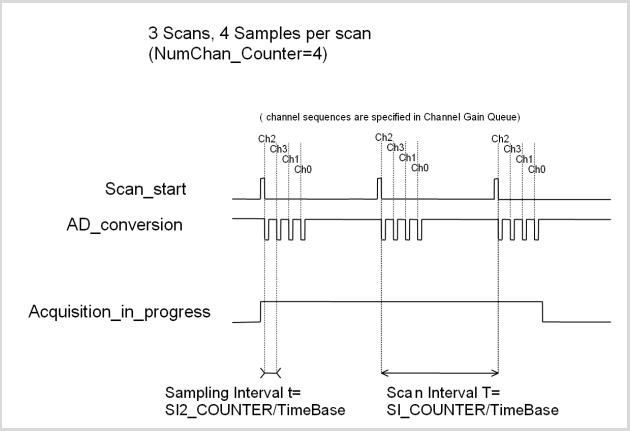


Figure 4-4: Scan Timing

Two trigger sources are available to start the scan acquisition. Refer to section 4.6 for details. For data transfer mode, refer to the Bus-mastering DMA Data Transfer section.

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NOTES

- The maximum A/D sampling rate is 250 kHz for PCI-9222 and 500 kHz for PCI-9223. The minimum setting for the SI2_counter when using the internal Timebase is 320 (PCI-9222) and 160 (PCI-9223).
- The SI_counter is 32-bit while the SI2_counter is 24-bit. The maximum scan interval using the internal Timebase = 2^{32}/80 Ms = 53.687s, and the maximum sampling interval between two channels using the internal Timebase = 2^{24}/40 Ms = 0.419s.
- The scan interval must not be smaller than the product of the data sampling interval and the NumChan_counter value. The relationship can be represented as: SI_counter>=SI2_counter * NumChan_counter.

Specifying Channels, Gains, and Input Configurations in the Channel Gain Queue

The channel, gain, and input configurations can be specified in the **Channel Gain Queue** under the scan acquisition mode. Note that in scan acquisition mode the number of entries in the Channel Gain Queue is normally equivalent to the value of NumChan_counter (the number of samples per scan).

Example:

Set

- SI2_counter = 160
- SI_counter = 640
- PSC_counter = 3
- NumChan_counter = 4
- Timebase = Internal clock source
- Channel entries in the Channel Gain Queue: ch1, ch2, ch0, ch2

Then:

- Acquisition sequence of channels: 1, 2, 0, 2, 1, 2, 0, 2, 1, 2, 0, 2
- Sampling Interval = 160/80M s = 2 us
- Scan Interval = 640/80M s = 8 us
- Equivalent sampling rate of ch0, ch1: 125 kHz
- Equivalent sampling rate of ch2: 250 kHz

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Trigger Modes

The PCI-9222/PCI-9223 supports two trigger sources: internal software and external digital trigger. You must select one as the trigger event source. A trigger event occurs when the specified condition is detected on the selected trigger source. For example, a rising edge on the external digital trigger input.

These cards support post-trigger (with retrigger) via software or an external digital trigger source to initiate various scan data acquisition timing when a trigger event occurs.

Post-Trigger Acquisition (no retrigger)

Use post-trigger acquisition in applications where you want to collect data after a trigger event. The number of scans after the trigger is specified in the PSC_counter as illustrated in Figure 4-5. The total acquired data length = NumChan_counter *PSC_counter.

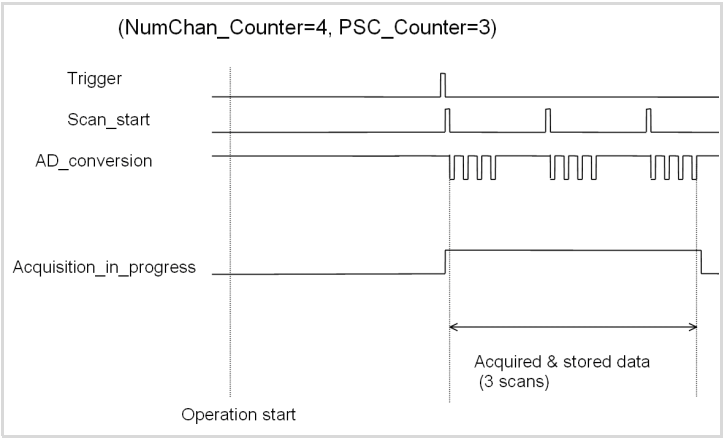


Figure 4-5: Post Trigger without Retrigger

Post-Trigger Acquisition (with retrigger)

Use post-trigger acquisition with retrigger function in applications where you want to collect data after several trigger events. The number of scans after each trigger is specified in PSC_counter and are programmable.

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Use Retrig_no to specify the re-trigger numbers. In Figure 4-6, two scans of data are acquired after the first trigger signal, then the card waits for the retrigger signal (retrigger signals which occur before the scans are completed will be ignored). When the retrigger signal occurs, two more scans are performed. The process repeats until the specified amount of retrigger signals are detected.

The total acquired data length = NumChan_counter *PSC_counter * Re-trig_no. For infinite retrigger, the retrig_no is set to 0.

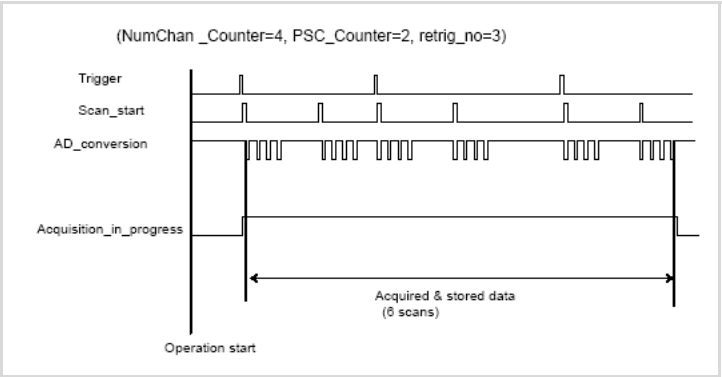


Figure 4-6: Post Trigger with Retrigger

Gated Trigger

Use the gated-trigger acquisition function in applications where you want to collect data when trigger events are set to level high/low, and hold acquisition when trigger events are set to the opposite level.

The number of scans after each trigger is specified in the PSC_counter. In Figure 4-7, after the operation starts, the first scan of data is immediately acquired when the trigger signal is disasserted and paused at the second scan when the trigger signal is asserted.

The four remaining scans are not performed until the trigger signal is disasserted again. The process repeats until the specified amount of retrigger signals are detected.

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The total acquired data length = NumChan_counter *PSC_counter.

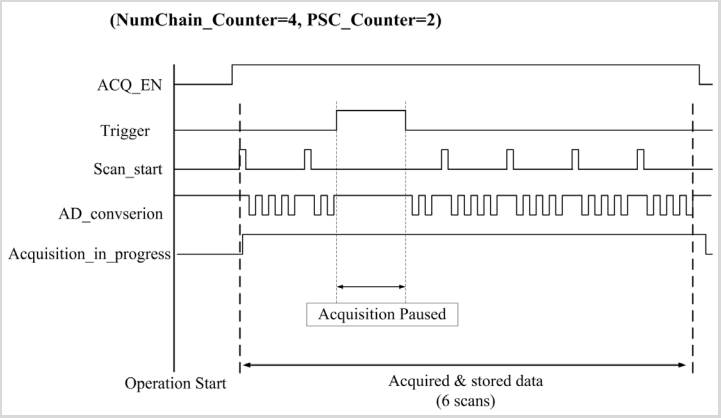


Figure 4-7: Gated Trigger with Finite Scan Acquisition

Bus-mastering DMA Data Transfer

In programmable scan acquisition mode, the PCI-9222/PCI-9223 supports bus-mastering DMA data transfer. PCI bus-mastering DMA is necessary for high speed DAQ in order to utilize the maximum PCI bandwidth. The bus-mastering controller controls the PCI bus when it becomes the master. Bus mastering reduces the size of the onboard memory and reduces CPU loading since data is directly transferred to the system memory with no host CPU intervention.

Bus-mastering DMA provides the fastest data transfer rate on PCI-bus. Once the analog input operation starts, control returns to your program. The hardware temporarily stores the acquired data in the onboard AD Data FIFO, then transfers the data to a user-defined DMA buffer memory in the computer. Note that even when the acquired data length is less than the Data FIFO, the AD data is not kept in the Data FIFO but rather directly transferred to the host memory by the bus-mastering DMA.

The DMA transfer mode is a very complex to program. It is recommended that you use a high-level program library provided by the ADLINK driver to configure this card. By using a high-level programming library for high speed DMA data acquisition, you

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simply need to assign the sampling period and the number of conversion through their specified counters. After the AD trigger condition is matched, the data will be transferred to the system memory by the bus-mastering DMA.

The PCI controller also supports the scatter/gather bus mastering DMA function that enables transfer of large amounts of data by linking all the memory blocks into a continuous linked list.

In a multi-user or multitasking OS, like Windows, Linux, etc, it is difficult to allocate a large continuous memory block to do the DMA transfer. Therefore, the PCI controller provides the function of scatter-gather or chaining mode DMA to link the non-continuous memory blocks into a linked list, allowing transfers of very large amounts of data without being limited by the fragment of small size memory. You may configure the linked list for the input DMA channel or the output DMA channel. Figure 4-8 shows a linked list that is constructed by three DMA descriptors. Each descriptor contains a PCI address, a PCI dual-address, a transfer size, and the pointer to the next descriptor. PCI address and PCI dual-address support 64-bit addresses which can be mapped into more than 4 GB of the address space. You can allocate many small size memory blocks and chain their associative DMA descriptors altogether by their application programs. The software driver provides simple settings of the scatter-gather function, and some sample programs are also provided in the ADLINK All-in-one CD.

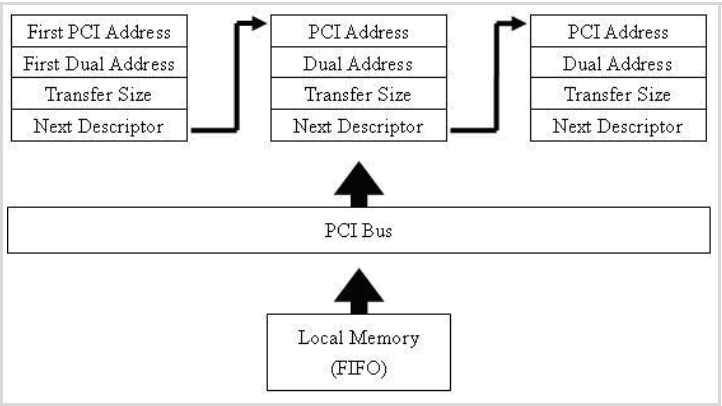


Figure 4-8: Scatter-gather DMA for Data Transfer

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In non-chaining mode, the maximum DMA data transfer size is 2M double words (8 MB). However, by using chaining mode-scatter/gather, there is no limitation for the DMA data transfer size. You may also link the descriptor nodes circularly to achieve a multi-buffered mode DMA.

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4.3 D/A Conversion

For complex applications, the PCI-9222/PCI-9223 offers software polling to update the output, and DMA data transfer to generate waveform. This means that the D/A update rate is not only controlled by software timing, but can also be set by a precision hardware timer that you specified. The following sections discuss the PCI-9222/PCI-9223 D/A architecture and control methods.

Bipolar Output Modes

The PCI-9222/PCI-9223 supports a maximum ±10 V voltage output. Table 4-3 illustrates the relationship of straight binary coding between the digital codes and output voltages.

Digital Code	Analog Output
0xFFFF	20V * (65535/65536) – 10V
0xC000	5V
0x8001	20V * (32769/65536) – 10V
0x8000	0V
0x4000	-5V
0x0000	-10V

Table 4-3: Bipolar Output Codes

Software Update

This method is suitable for applications that need to generate D/A output controlled by user programs. In this mode, the D/A converter generates one output once the software command is issued. However, it is difficult to determine the software update rate under a multitask OS such as Windows.

Waveform Generation

Waveform Generation Data Structure

FIFO is a hardware first-in first-out data queue that holds temporary digital codes for D/A conversion. When PCI-9222/PCI-9223 operates in waveform generation mode, the waveform patterns are stored in FIFO with 512 samples.

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Waveform patterns larger than 512 samples are also supported using bus-mastering DMA transfer via the PCI controller. Data format in FIFO is shown in Figure 4-9.

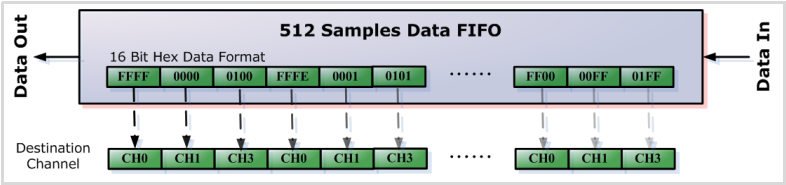


Figure 4-9: FIFO Data In/Out Structure

DMA transfers data according to channel order. Figure 4-10 shows DA channel 0 to channel 3 data, while channel 2 is disabled.

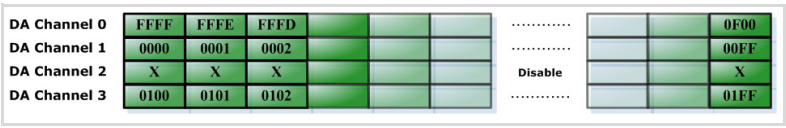


Figure 4-10: Waveform Generation for Three Channels Update

With hardware-based waveform generation, D/A conversions are updated automatically by the FPGA rather than by the application software. Compare with the conventional software-based waveform generation, the precise hardware timing control guarantees non-distorted waveform generation even when the host CPU is under heavy loading.

NOTE When using waveform generation mode, both DACs must be configured in a single mode. However, any individual DAC can be disabled.

Waveform Generation Clock Source

When the onboard DAC receives a conversion clock signal, it will trigger a D/A update. The update clock of PCI-9222/PCI-9223 may come from three different clock sources: internal hardware timer, general purpose input channel (GPI 0 ~ GPI 7), or SSI (system synchronization interface).

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You can choose the update clock source by setting the AO source configuration. Refer to Figure 4-11. It is recommended that you use the internal hardware to get a more precise update rate.

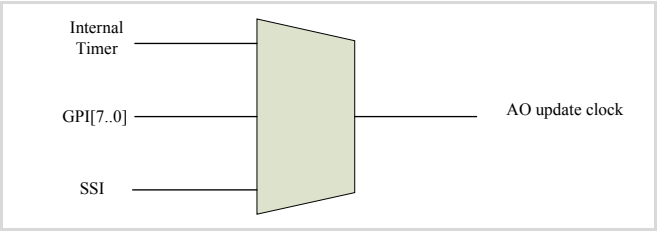


Figure 4-11: Waveform Generation Clock Source Selection

Waveform Generation with Internal Hardware Timer

Six counters interact with the waveform to generate different DAWR timing to form various waveforms. These are described in Table 4-4 and illustrated in Figure 4-12.

Counter Name	Width	Description	Note
UI_counter	32-bit	**Update Interval**. Defines the update interval between each data output.	Update Interval = UI_counter / Timebase*.
UC_counter	32-bit	**Update Counts**. Defines the number of data in a waveform.	When value in UC_counter is smaller than the size of waveform patterns, the waveform is generated piece-wisely.
IC_counter	32-bit	**Iteration Counts**. Defines how many times the waveform is generated.	
DLY1_counter	32-bit	Defines the delay time for waveform generation after the trigger signal.	Delay Time = (DLY1_counter / Clock Timebase)

Table 4-4: Summary of Counters for Waveform Generation

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DLY2_counter	32-bit	Defines the delay time to separate consecutive waveform generation. This is applicable only in Iterative Waveform Generation mode.	Delay Time = (DLY2_counter / Clock Timebase)
Trig_counter	32-bit	Defines the acceptable start trigger count when re-trigger function is enabled	

Table 4-4: Summary of Counters for Waveform Generation

Timebase= 80M*

NOTE The maximum D/A update rate is 1 MHz, and the minimum UI_counter setting is 80.

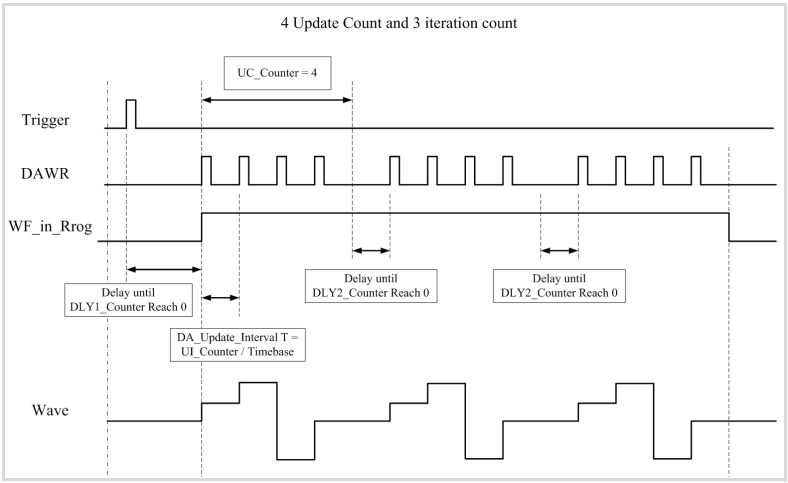


Figure 4-12: Typical D/A Timing of Waveform Generation

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Trigger Modes

Post-Trigger Generation

Use post-trigger generation when you want to generate a waveform right after a trigger signal. The number of patterns to be updated after the trigger signal is specified by UC_counter* IC_counter and is illustrated in Figure 4-13.

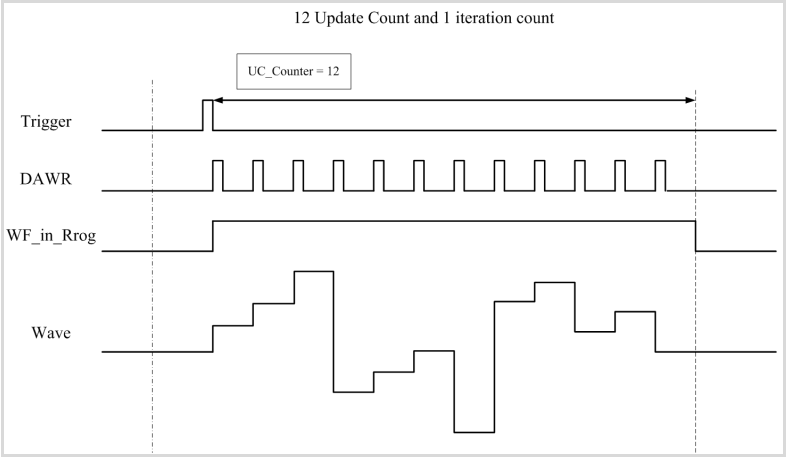


Figure 4-13: Post-Trigger Generation

Delay-Trigger Generation

Use delay-trigger when you want to delay the waveform generation after the trigger signal. The delay time is determined by DLY1_counter, as illustrated in Figure 4-14.

The counter counts down on the rising edges of DLY1_counter clock source after the start trigger signal. When the count reaches zero, card will start to generate the waveform. The DLY1_counter clock source can be selected via software application using the internal 80 MHz timebase.

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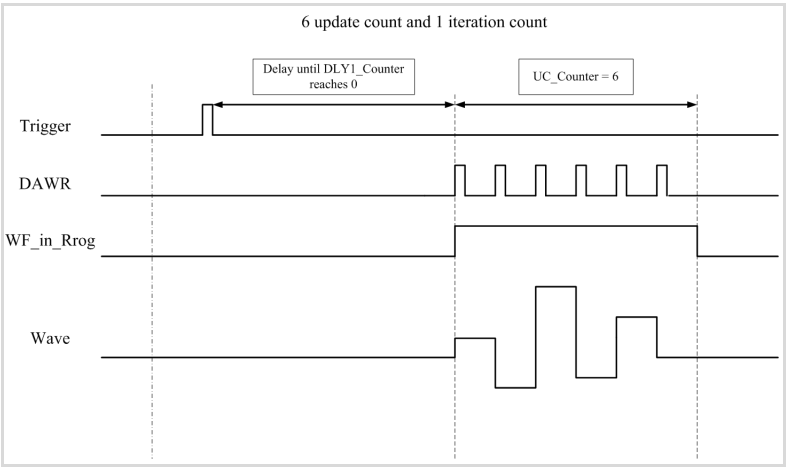


Figure 4-14: Delay-Trigger Generation

Post-Trigger or Delay-Trigger with Retrigger

Use post-trigger or delay-trigger with retrigger when you want to generate multiple waveforms with respect to multiple incoming trigger signals. You can set Trig_counter to specify the number of acceptable trigger signals. Refer to Figure 4-15.

In this example, two waveforms are generated after the first trigger signal. The card then waits for another trigger signal.When the next trigger signal is asserted, the card generates two more waveforms.

After two trigger signals, as specified in Trig_Counter, no more triggers signals will be accepted unless trigger reset command is executed. For more information on Iterative Waveform Generation that is used in this example, refer to the next section.

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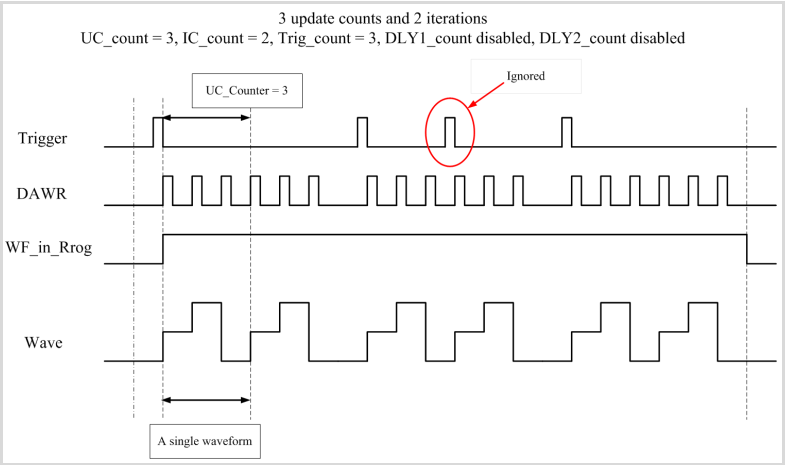


Figure 4-15: Post-Trigger with Retrigger Generation

NOTE Start Trigger signals asserted during the waveform generation process will be ignored.

Iterative Waveform Generation

You can set the IC_counter to generate iterative waveforms regardless of the trigger mode used. The IC_counter stores the iteration number. Examples are shown in Figure 4-16 and Figure 4-17.

NOTE When IC_counter is disabled, the waveform generation will not stop until a stop trigger is asserted.

An onboard data FIFO is used to buffer the waveform patterns for waveform generation. If the size of a single waveform is smaller than that of the FIFO, after initially loading the data from the host computer's memory, the data in FIFO will be reused when a single waveform generation is completed and will not occupy the PCI bandwidth afterwards.

However, if the size of a single waveform is larger than that of the FIFO, it needs to be intermittently loaded from the host computer's memory via DMA, and will occupy the PCI bandwidth.

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If the value specified in UC_counter is smaller than the sample size of the waveform patterns, the waveform will be generated piece-wisely. For example, if you defined a 16-sample sine wave and set the UC_counter to 2, the generated waveform will be a 1/8-cycle sine wave for every waveform period, and a complete sine wave will be generated for every 8-iterations. If you specified a UC_counter value that is larger than the sample size of the waveform LUT (for example, 32), the generated waveform will be a 2-cycle sine wave for every waveform period.

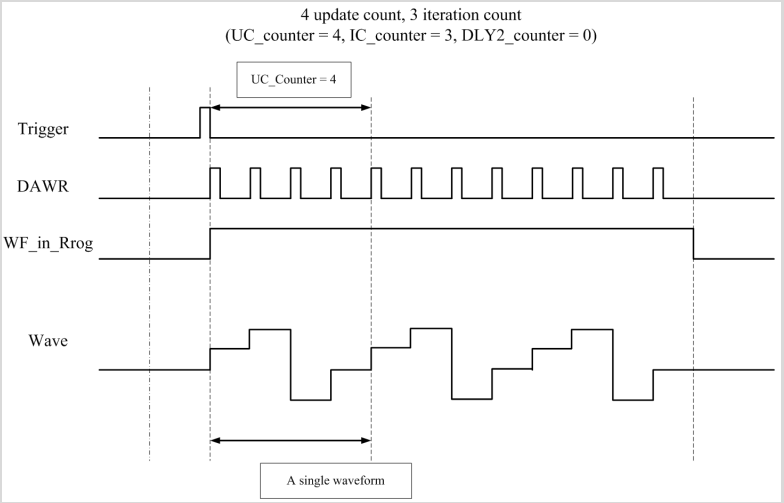


Figure 4-16: Finite Iterative Waveform Generation with Post-trigger

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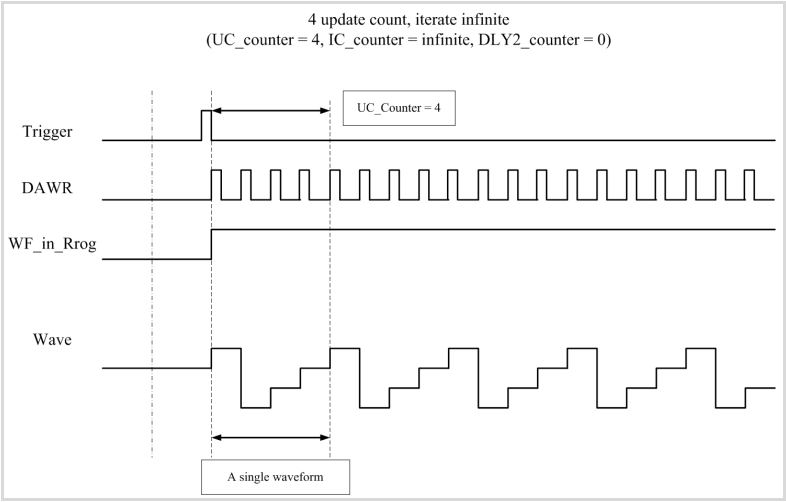


Figure 4-17: Infinite Iterative Waveform Generation with Post-trigger

In conjunction with different trigger modes and counter setups, you can manipulate a single waveform to generate different and more complex waveforms.

DLY2_Counter in Iterative Waveform Generation

To expand the flexibility of iterative waveform generation, DLY2_counter was implemented to separate consecutive waveform generations.

The DLY2_counter starts counting down right after a single waveform generation is completed. When it reaches zero, the next iteration of waveform generation will start as shown in Figure 4-12. If you generate the waveform piece-wisely, the next piece of waveform will be generated. The DLY2_counter clock source can be software selected from internal 80 MHz Timebase.

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4.4 Programmable Function I/O

The PCI-9222/PCI-9223 supports a powerful programmable function I/O provided by an FPGA chip. These function I/O can be configured as TTL DI/DO or 32-bit timer/counters. In addition, the timer/counter supports a variety of modes, including general purpose timer/counter, PWM output, or encoder input for simple motion control. These signals are single-ended and 5V TTL-compliant.

TTL DI/DO

Programmable function I/O can be used as static TTL-compliant 8-CH digital input and 4-CH digital output. You can read/write these I/O lines by software polling. Its sample and update rate is fully controlled by software timing.

Definition	Pin #		Definition
GPI0	**34**	**68**	GPI8
GPI1	**33**	**67**	GPI9
GPI2	**32**	**66**	GPI10
GPI3	**31**	**65**	GPI11
GPI4	**30**	**64**	GPI12
GPI5	**29**	**63**	GPI13
GPI6	**28**	**62**	GPI14
GPI7	**27**	**61**	GPI15
DGND	**26**	**60**	DGND
GPO0	**25**	**59**	GPO8
GPO1	**24**	**58**	GPO9
GPO2	**23**	**57**	GPO10
GPO3	**22**	**56**	GPO11
GPO4	**21**	**55**	GPO12
GPO5	**20**	**54**	GPO13
GPO6	**19**	**53**	GPO14
GPO7	**18**	**52**	GPO15
	...	**...**	
	1	**35**	

Table 4-5: TTL DIO Pins in CN1

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General Purpose Timer/Counter

The PCI-9222/PCI-9223 comes with three general purpose timer/counter sets featuring:

- Count up/down controlled by hardware or software
- Programmable counter clock source (internal clock up to 80 MHz, external clock up to 10 MHz)
- Programmable gate selection (hardware or software control)
- Programmable input and output signal polarities (high active or low active)
- Initial Count can be loaded from a software application
- Current count value can be read-back by software without affecting circuit operation.

Definition	Pin #		Definition
GPTC_CLK0	34	68	GPTC_CLK2
GPTC_UD0	33	67	GPTC_UD2
GPTC_GATE0	32	66	GPTC_GATE2
GPTC_AUX0	31	65	GPTC_AUX2
GPTC_CLK1	30	64	GPTC_CLK3
GPTC_UD1	29	63	GPTC_UD3
GPTC_GATE1	28	62	GPTC_GATE3
GPTC_AUX1	27	61	GPTC_AUX3
DGND	26	60	DGND
GPTC_OUT0	25	59	
GPTC_OUT1	24	58	
GPTC_OUT2	23	57	
GPTC_OUT3	22	56	
	...	...	
	1	35	

Table 4-6: Timer/Counter Mode Pins in CN1

Basic Timer/Counter Functions

Each timer/counter has three inputs that can be controlled via hardware or software applications. They are clock input (GPTC_CLK), gate input (GPTC_GATE), and up/down control input (GPTC_UD). The GPTC_CLK input provides a clock source input to the timer/counter. Active edges on the GPTC_CLK input make the counter increment or decrement. The GPTC_UD input

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controls the counter to count up or down (high: count up; low: count down), while the GPTC_GATE input is a control signal which acts as a counter enable or a counter trigger signal under different applications. The GPTC_OUT will then generate a pulse signal based on which timer/counter mode you have set.

All input/output signals polarities can be programmed by software application. For brevity, all GPTC_CLK, GPTC_GATE, and GPTC_OUT in the following illustrations are assumed to be active high or rising-edge triggered.

General Purpose Timer/Counter Modes

Ten programmable timer/counter modes are provided. All modes start operating following a software-start signal that is set by the software. The GPTC software reset initializes the status of the counter and reloads the initial value to the counter. The operation remains halted until the software-start is executed again. The operating theories under different modes are described in the following sections.

Mode1: Simple Gated-Event Counting

In this mode, the counter counts the number of pulses on the GPTC_CLK after the software-start. Initial count can be loaded from the software application. Current count value can be read-back by software any time with no effect to the counting. GPTC_GATE is used to enable/disable counting. When GPTC_GATE is inactive, the counter halts the current count value. Figure 4-18 illustrates the operation with initial count = 5, count-down mode.

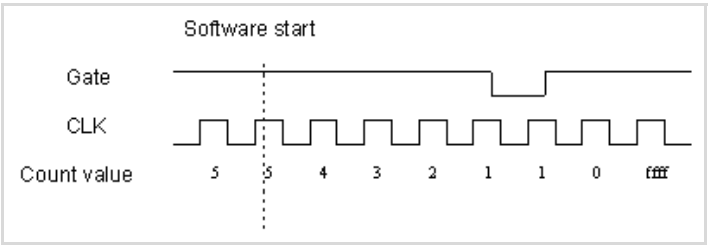


Figure 4-18: Mode 1 Operation

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Mode 2: Single Period Measurement

The counter counts the period of the signal on GPTC_GATE in terms of GPTC_CLK. Initial count can be loaded from the software application. After the software-start, the counter counts the number of active edges on GPTC_CLK between two active edges of GPTC_GATE. After the completion of the period interval on GPTC_GATE, GPTC_OUT outputs high and then current count value can be read-back by the software application. Figure 4-19 illustrates the operation where initial count = 0, count-up mode.

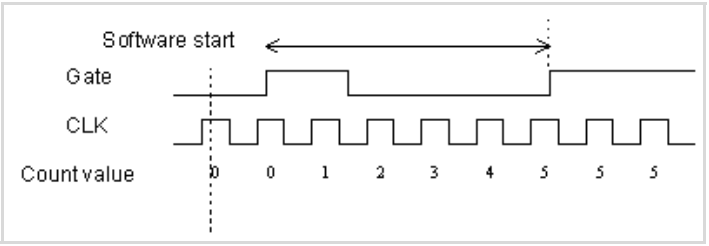


Figure 4-19: Mode 2 Operation

Mode 3: Single Pulse-width Measurement

The counter counts the pulse-width of the signal on GPTC_GATE in terms of GPTC_CLK. Initial count can be loaded from the software application.

After the software-start, the counter counts the number of active edges on GPTC_CLK when GPTC_GATE is in its active state.

After the completion of the pulse-width interval on GPTC_GATE, GPTC_OUT outputs high and then current count value can be read-back by the software application. Figure 4-20 illustrates the operation where initial count = 0, count-up mode.

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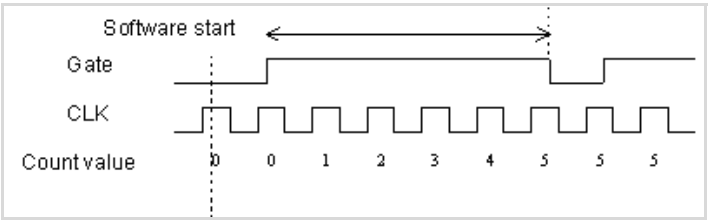


Figure 4-20: Mode 3 Operation

Mode 4: Single Gated Pulse Generation

This generates a single pulse with programmable delay and programmable pulse-width following the software-start. The two programmable parameters can be specified in terms of periods of the GPTC_CLK input by the software application. GPTC_GATE is use to enable/disable counting. When GPTC_GATE is inactive, the counter halts the current count value. Figure 4-21 illustrates the generation of a single pulse with a pulse delay of two and a pulse-width of four.

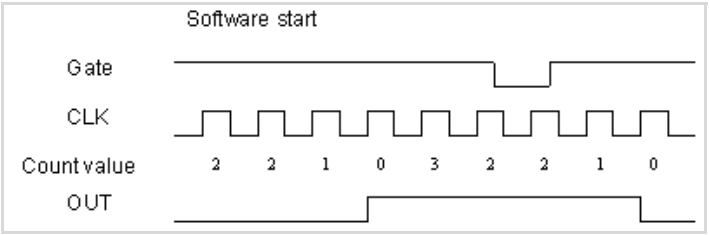


Figure 4-21: Mode 4 Operation

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Mode 5: Single Triggered Pulse Generation

This mode generates a single pulse with programmable delay and programmable pulse-width following an active GPTC_GATE edge. You may specify these programmable parameters in terms of periods of the GPTC_CLK input. When the first GPTC_GATE edge triggers the single pulse, GPTC_GATE makes no effect until the software-start is executed again. Figure 4-22 illustrates the generation of a single pulse with a pulse delay of two and a pulse-width of four.

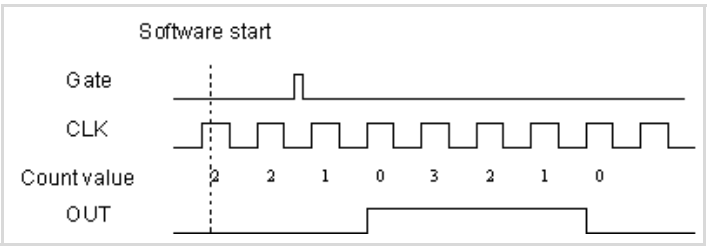


Figure 4-22: Mode 5 Operation

Mode 6: Re-triggered Single Pulse Generation

This mode is similar to Mode 5 except that the counter generates a pulse following every active edge of GPTC_GATE. After the software-start, every active GPTC_GATE edge triggers a single pulse with programmable delay and pulse-width. Any GPTC_GATE triggers that occur when the prior pulse is not completed is ignored. Figure 4-23 illustrates the generation of two pulses with a pulse delay of two and a pulse-width of four.

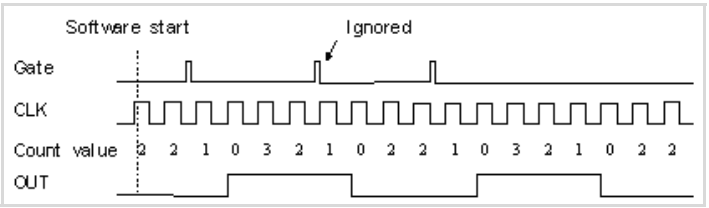


Figure 4-23: Mode 6 Operation

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Mode 7: Single Triggered Continuous Pulse Generation

This mode is similar to Mode 5 except that the counter generates continuous periodic pulses with programmable pulse interval and pulse-width following the first active edge of GPTC_GATE. When the first GPTC_GATE edge triggers the counter, GPTC_GATE makes no effect until the software-start is executed again. Figure 4-24 illustrates the generation of two pulses with a pulse delay of four and a pulse-width of three.

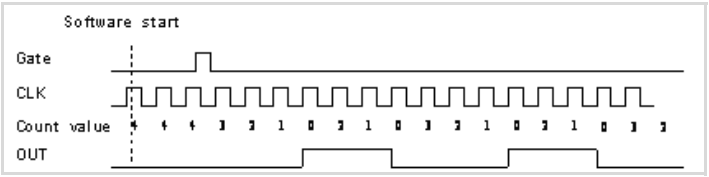


Figure 4-24: Mode 7 Operation

Mode 8: Continuous Gated Pulse Generation

This mode generates periodic pulses with programmable pulse interval and pulse-width following the software-start. GPTC_GATE is use to enable/disable counting. When GPTC_GATE is inactive, the counter halts the current count value. Figure 4-25 illustrates the generation of two pulses with a pulse delay of four and a pulse-width of three.

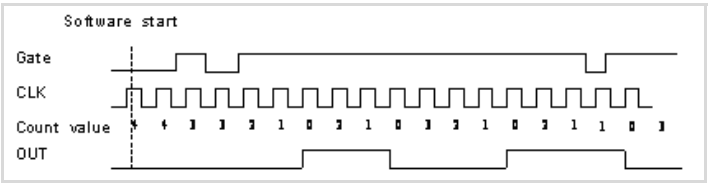


Figure 4-25: Mode 8 Operation

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Mode 9: Edge Separation Measurement

Measures the time differentiation between two different pulse signals. The first pulse signal is connected to GPTC_GATE and the second signal is connected to GPTC_AUX. It counts the clocks that pass by between the rising edge signal of two different pulses through the 40MHz internal clock or external clock. You can calculate the time period via the known clock frequency. The maximum counting width is 32-bit. Figure 4-26 illustrates how the counter value decreases in Edge Separation Measurement mode.

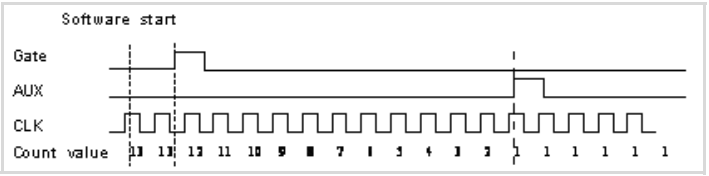


Figure 4-26: Mode 9 Operation

Mode 10: PWM Output

These cards' powerful timer/counter can also simulate a PWM (Pulse Width Modulation) output. By setting varying number of Pulse_initial_cnt and Pulse_length_cnt, you can get varying pulse frequency (Fpwm) and duty cycle (Dutypwm). Figure 4-27 illustrates the PWM output and the formula showing how to calculate the PWM frequency and duty cycle.

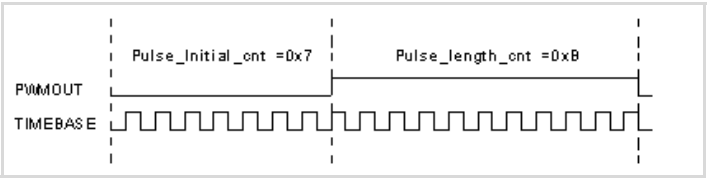


Figure 4-27: Mode 10 Operation

$$F_{PWM} = \frac{F_{Timebase}}{Pulse_initial_cnt + Pulse_length_cnt}$$

$$Duty_{PWM} = \frac{Pulse_length_cnt}{Pulse_initial_cnt + Pulse_length_cnt}$$

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Digital Waveform Acquisition and Generation

The PCI-9222/PCI-9223 GPI and GPO support digital waveform generation and digital waveform acquisition. You can sample GPI or update GPO based on the precision hardware timer.

Digital Waveform Acquisition

The digital data on GPI channels can be acquired by using the digital waveform acquisition mode. This function is similar with AI scan acquisition mode.

With periodic sampling clock, you can acquire data based on the precision hardware time interval. The PCI-9222/PCI-9223 comes with a dedicated FIFO that stores the sampled digital data and transfers it to the system memory via DMA.

The GPI is a 16-bit data and the sample clock source can be configured from an internal timer pacer, internal analog conversion clock, or external clock. When using an internal timer pacer as clock source, the GPI supports data transfer rates of up to 2MHz. The internal analog conversion clock source can come from AI conversion clock or AO update clock. The external signal clock source can be set from any of the GPI [0..7] pins. When the sample clock is from the GPI, the actual GPI data width is only 15-bit since the external sample clock signal occupies one bit. Figure 4-28 illustrates the GPI sample clock routing.

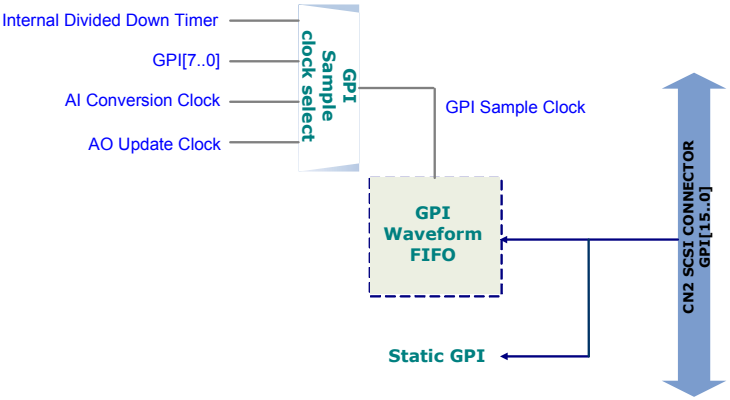


Figure 4-28: Digital Waveform Acquisition Operation

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Digital Waveform Generation

The digital output on GPO [15..0] channels can be updated by using digital waveform generation mode. This works similar to AO waveform generation. With periodic update clock, you can generate a sequence of digital output patterns based on precision hardware time interval. The PCI-9222 and PCI-9223 come with a dedicated FIFO that stores these waveform patterns. The update patterns are transferred from the system memory to the FIFO via DMA after the digital waveform generation starts.

The GPO update clock source can be configured from the onboard timer pacer, internal analog conversion clock, or external clock. When using the internal timer pacer as update clock source, the GPO supports data update rates of up to 2MHz.

The internal analog conversion clock source can come from AI conversion clock or AO update clock, while the external signal clock source can be set from any of the GPI [0..7] pins. When the update clock is from the GPI and the GPI funtions at the same time, the actual GPI data width is only 15-bit. Figure 4-29 illustrates the routing of GPO update clock.

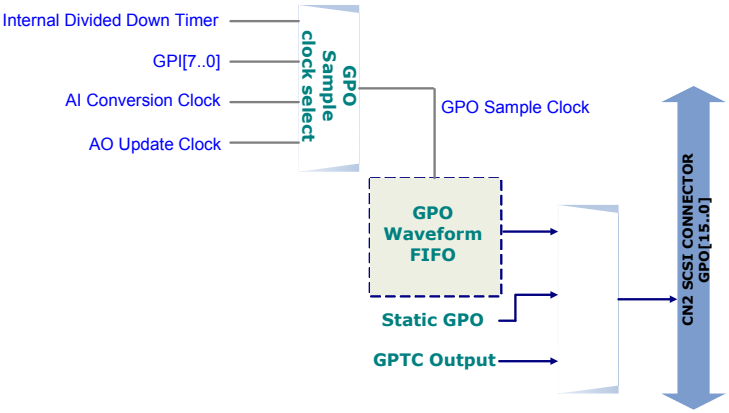


Figure 4-29: Digital Waveform Generation Operation

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4.5 Isolation Encoder

The PCI-9222/PCI-9223 features a combination of data acquisition and simple motion control with support for two channel encoder input sets which provide an alternative for step motor or servo motor's position feedback. The encoder sets are assigned in CN2.

Definition	Pin #		Definition
	34	68	
	...	...	
E24V	9	43	NC
EGND	8	42	NC
IEA0+	7	41	IEA1+
IEA0-	6	40	IEA1-
IEB0+	5	39	IEB1+
IEB0-	4	38	IEB1-
IEZ0+	3	37	IEZ1+
IEZ0-	2	36	IEZ1-
IORG0	1	35	IORG1

Table 4-7: Encoder Pins in CN2

Encoder Isolation Input Module

Figure 4-30 illustrates the encoder isolation phase A, phase B and phase Z inputs module with 2500 Vrms protection.

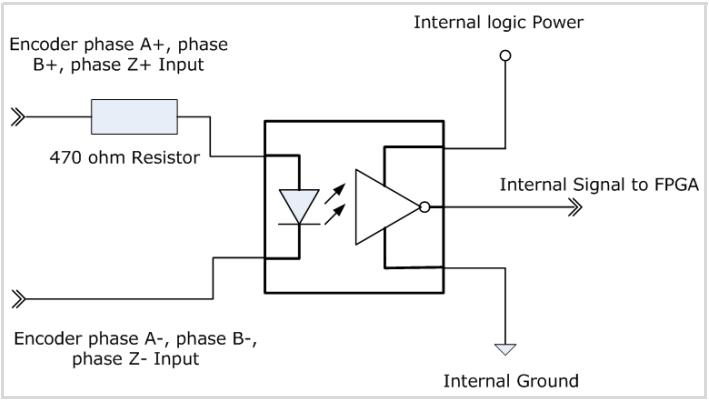


Figure 4-30: Encoder Isolation Input Module

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The Encoder OGRx input is different from the encoder phase input since you need to add an external +24V power to drive the photo-couple. Figure 4-31 shows the OGRx input.

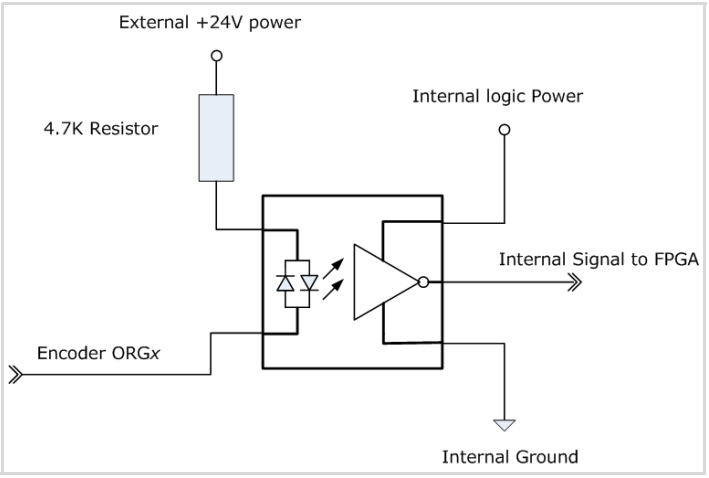


Figure 4-31: Encoder OGRx Input

CW/CCW Encoder Mode

When GPTC is set to CW/CCW encoder mode and when the input EAx is connected to CW source signal and EBx is connected to CCW source signal, pulses from EAx will cause the counter to counter up and spin the motor clockwise. Otherwise, pulses from EBx will cause the counter to counter down and spin the motor counterclockwise. Figure 4-32 shows the increase/decrease of counter value in CW or CCW encoder mode.

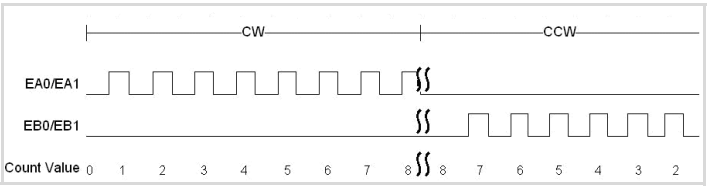


Figure 4-32: CW/CCW Encoder Timing

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X1 Encoder Mode

In X1 encoder mode, if phase A (EA0/EA1) is advanced of phase B (EB0/EB1) in a quadrature cycle, the increment of counter value will be 1. Otherwise, if phase B is advanced of phase A in a quadrature cycle, the decrement of counter value will also be 1.

Figure 4-33 shows a quadrature cycle and the increment and decrement of counter value in X1 encoder mode. When phase A leads phase B, the counter value increases on the first rising edge of CLK after phase A goes high. When phase B leads phase A, the counter value decreases on the first rising edge of CLK after phase A goes low.

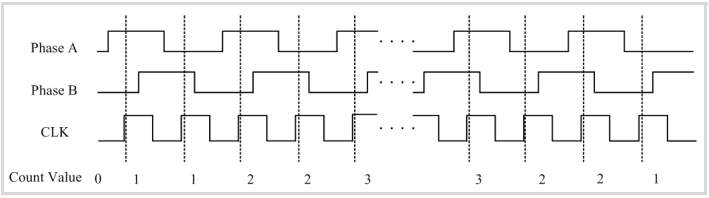


Figure 4-33: X1 Encoder Mode

X2 Encoder Mode

This mode is similar to X1 Encoder Mode, except that the amount of counter value increases or decreases by two. Refer to Figure 4-34.

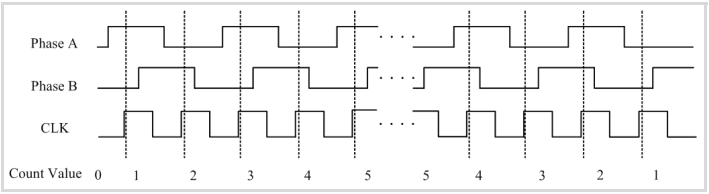


Figure 4-34: X2 Encoder Mode

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X4 Encoder Mode

This mode is similar to X1 Encoder Mode, except that the amount of counter value increases or decreases by four. Refer to Figure 4-35.

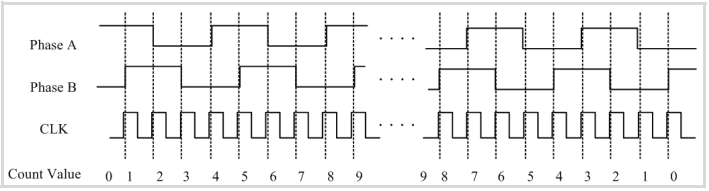


Figure 4-35: X4 Encoder Mode

Phase Z

Each encoder mode may use a third phase, phase Z, that is also frequently used for the index phase. You may decide if the counter needs to be reloaded a specified value when phase Z is at a logic high level with phase A and B at a specific logic condition.

You must ensure that the logic level of phase Z is high during at least a portion of the phase you specify for reload when you use phase Z. Otherwise, the counter does not reload.

In Figure 4-36, the reload phase is when the logic level of phase A is high, phase B is low, and phase Z is high in X1 Encoder Mode. In addition, reloading takes higher priority than increment or decrement of counter value. The reload occurs within one maximum CLK period after the reload phase becomes true. After the counter value is reloaded, the counter continues to count as before.

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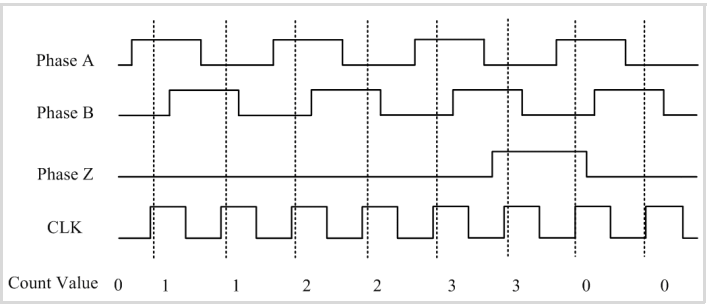


Figure 4-36: Phase Z

Original Signal (ORGx)

Original Signal (ORG0/ORG2/ORG1) is used with phase Z. With ORG enabled, a high level on phase Z and ORG causes the counter to reload with a specified value in a specified phase of the quadrature cycle. When you use ORG signal if it is at a low level and phase Z is at a high level, then counter reload is ignored.

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4.6 Trigger Sources

The PCI-9222/PCI-9223 supports two trigger sources for analog input, analog output, and digital waveform acquisition/generation: software trigger and external digital trigger.

Software Trigger

This trigger mode does not need any external trigger source. The trigger asserts right after you execute the specified function calls to begin data acquisition.

External Digital Trigger

An external digital trigger occurs when a rising edge or a falling edge is detected on the digital signal connected to the PCI-9222/PCI-9223 function I/O. You can set any DI line as external trigger pin. You may also easily program the trigger polarity via the ADLINK software drivers. Take note that the signal level of the external digital trigger signals should be TTL-compatible with a minimum 25 ns pulse.

NOTE Digital waveform acquisition/generation only supports rising-edge trigger. You can not set the polarity using the software driver.

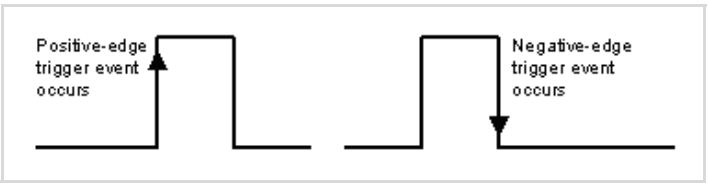


Figure 4-37: External Digital Trigger

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5 Calibration

This chapter introduces the card calibration process to minimize AD measurement errors and DA output errors.

5.1 Loading Calibration Constants

The PCI-9222/PCI-9223 is factory-calibrated before shipment. The associated calibration constants of the TrimDACs firmware are written to the onboard EEPROM. TrimDACs firmware is the algorithm in the FPGA. Loading calibration constants is the process of loading the values of TrimDACs firmware stored in the onboard EEPROM. ADKLINK provides a software utility that automatically reads the calibration constants, if necessary.

There is a dedicated space for storing calibration constants in the EEPROM. In addition to the default bank of factory calibration constants, there is one user-utilization bank. This bank allows you to load the TrimDACs firmware values either from the original factory calibration or from a subsequently-performed calibration.

Because of the fact that measurements and outputs errors may vary depending on time and temperature, it is recommended that you calibrate the card when it is integrated in your computing environment. The auto-calibration function is presented in the following sections.

5.2 Auto-calibration

Through the PCI-9222/PCI-9223 auto-calibration feature, the calibration software measures and corrects almost all calibration errors without any external signal connections, reference voltage, or measurement devices.

The PCI-9222/PCI-9223 comes with an onboard calibration reference to ensure the accuracy of auto-calibration. The reference voltage is measured in the production line through a digital potentiometer and compensated in the software. The calibration constant is memorized after this measurement. We do not recommended adjustment of the onboard calibration reference except when an ultra-precision calibrator is available.

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5.3 Saving Calibration Constants

Factory-calibrated constants are permanently stored in a bank of the onboard EEPROM and may not be modified. When you re-calibrate the device, the software stores the new constants in a user-configurable section of the EEPROM. To return a device to its initial factory calibration settings, the software can copy the factory calibrated constants to the user-configurable section of the EEPROM. When auto-calibration is completed, you can save the new calibration constants to the user-configurable banks in the EEPROM. The date and the temperature when you ran auto-calibration is saved with the calibration constants. You can store three sets of calibration constants according to three different environments and re-load the calibration constants later.

NOTES

- Warm the card up for at least 15 minutes before initiating auto-calibration.
- Remove the cable before auto-calibrating the card since the DA outputs are changed during the process.

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Warranty Policy

Thank you for choosing ADLINK. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. Before using ADLINK's products please read the user manual and follow the instructions exactly. When sending in damaged products for repair, please attach an RMA application form which can be downloaded from: http://rma.adlinktech.com/policy/.
2. All ADLINK products come with a limited two-year warranty, one year for products bought in China:
   - The warranty period starts on the day the product is shipped from ADLINK's factory.
   - Peripherals and third-party products not manufactured by ADLINK will be covered by the original manufacturers' warranty.
   - For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ADLINK is not responsible for any loss of data.
   - Please ensure the use of properly licensed software with our systems. ADLINK does not condone the use of pirated software and will not service systems using such software. ADLINK will not be held legally responsible for products shipped with unlicensed software installed by the user.
   - For general repairs, please do not include peripheral accessories. If peripherals need to be included, be certain to specify which items you sent on the RMA Request & Confirmation Form. ADLINK is not responsible for items not listed on the RMA Request & Confirmation Form.

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3. Our repair service is not covered by ADLINK's guarantee in the following situations:
   - Damage caused by not following instructions in the User's Manual.
   - Damage caused by carelessness on the user's part during product transportation.
   - Damage caused by fire, earthquakes, floods, lightening, pollution, other acts of God, and/or incorrect usage of voltage transformers.
   - Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).
   - Damage caused by leakage of battery fluid during or after change of batteries by customer/user.
   - Damage from improper repair by unauthorized ADLINK technicians.
   - Products with altered and/or damaged serial numbers are not entitled to our service.
   - This warranty is not transferable or extendible.
   - Other categories not protected under our warranty.
4. Customers are responsible for shipping costs to transport damaged products to our company or sales office.
5. To ensure the speed and quality of product repair, please download an RMA application form from our company website: http://rma.adlinktech.com/policy. Damaged products with attached RMA forms receive priority.

If you have any further questions, please email our FAE staff: service@adlinktech.com.

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