NuDAQ®

PCI-9820

2-CH, 130MS/s, 14-Bit, Simultaneous-Sampling Digitizer

User's Guide



Recycle Paper

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Manual Rev. 1.00 Sep 19, 2003

Part No: 50-11133-100

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How to Use This Guide

This manual is designed to help users understand the PCI-9820. It is divided into four chapters:

Chapter 1 **Introduction**

Gives an overview of the product features, applications, and specifications.

Chapter 2 **Installation**

Describes how to install the PCI-9820.

Chapter 3 **Signal Connections**

Describes connector pin assignments.

Chapter 4 **Operation Theory**

Describes how to operate the PCI- 9820, including signal sources, TIMEBASE sources, trigger sources, trigger modes, data transfers, synchronizing multiple cards, and auto-calibration.

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1

Introduction

The ADLINK PCI-9820 is a 65MS/s, high-resolution PCI digitizer with deep SODIMM SDRAM memory that features flexible input configurations, including programmable input ranges and user-selectable input impedance. With the deep on-board acquisition memory, the PCI-9820 is not limited by the PCI's 132MB/s bandwidth, and can record the waveform for extended periods of time. The PCI-9820 is ideal for high-speed waveform capturing (such as radar and ultrasound), software radio, and other signal digitizing applications needing large amounts of memory for data storage.

Analog Input

The PCI-9820 device features two analog input channels. The small signal bandwidth of each channel exceeds 30MHz, which satisfies the Nyquist sampling theory. The input ranges are programmable as either ±5V or ±1V. The 14-bit A/D resolution makes the PCI-9820 ideal both for time-domain and frequency-domain applications.

Acquisition System

The ADLINK PCI-9820 device uses a pair of 65MS/s, 14-bit pipeline ADCs to digitize the input signals. The device provides an internal 60MHz timebase for data acquisition. The maximum real-time sampling rate is 60MS/s with internal timebase and up to 65MS/s with external timebase. By using the "ping pong" mode, the sampling rate is up to 120MS/s with internal timebase or 130MS/s with external timebase.

Acquisition Memory

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The PCI-9820 device supports SODIMM SDRAM ranging from 64MB to 512MB. The digitized data is stored in the on-board SDRAM before being transferred to host memory. The PCI-9820 uses scatter-gather bus mastering DMA to move data to the host memory. If the data throughput from the PCI-9820 is less than the available PCI bandwidth, the PCI-9820 also features on-board 3k-sample FIFO to achieve real-time transfer bypassing the SDRAM, directly to the host memory.

Triggering

The PCI-9820 features flexible triggering functions, such as analog and digital triggering. The analog trigger features programmable trigger thresholds on rising or falling edges of both input channels. The 5V/TTL digital trigger comes from SSI interface or the external SMB connector for synchronizing multiple devices.

Post-trigger, pre-trigger, delay-trigger and middle-trigger modes are available to acquire data around the trigger event. The PCI-9820 also features repeated trigger acquisition to acquire data in multiple segments coming with successive trigger events at extremely short rearming intervals.

Multiple-Instrument Synchronization

On the PCI-9820, a synchronization bus (system synchronization interface, SSI) routes timing and trigger signals between one or more PCI-9820 devices. The SSI synchronizes between different acquisition hardware by a common trigger signal or a single sample clock for the acquisition of multiple devices.

Calibration

The auto-calibration function of the PCI-9820 is performed with trim DACs to calibrate the offset and gain errors of the analog input channels. Once the calibration process is done, the calibration constant will be stored in EEPROM. These values are loaded and used as needed by the board. Because all the calibration is conducted automatically by software commands, users do not have to adjust trimpots to calibrate the boards.

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1.1 Features

- Supports 32-bit 3.3V or 5V PCI bus
- 14-bit A/D resolution
- Up to 60MS/s sampling rate per channel with internal timebase
- Up to 65MS/s sampling rate per channel with external timebase
- Up to 130MS/s sampling rate using “ping pong” mode for single-channel acquisition
- 2-CH simultaneous-sampled single-ended analog inputs
- Programmable input ranges of ±1V and ±5V
- User-selectable input impedance of 50Ω or high input impedance
- >30MHz -3dB bandwidth
- Up to 512MB on-board SODIMM SDRAM
- Scatter-gather DMA data transfers
- Analog and digital triggering
- Fully auto calibration
- Multiple cards synchronization
- Compact, half-size PCB

1.2 Applications

- Communication system analysis
- Software radio
- Automotive Testing
- RF signal analysis
- Transient signal capture
- ATE
- Laboratory automation
- Biotech measurement

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1.3 Specifications

♦ Analog Input

- **Number of channels:** 2 simultaneous-sampled single-ended
- **Resolution:** 14 bits
- **Max sampling rate:**

  60MS/s per channel with internal timebase

  65MS/s per channel with external timebase

  120MS/s using “ping pong” mode on CH0 with internal timebase

  130MS/s using “ping pong” mode on CH0 with external timebase
- **On-board memory size:**

  SODIMM SDRAM:

  64MB standard, up to 512MB

  FIFO buffer:

  3056 samples
- **Bandwidth (-3 dB):** 30MHz minimum
- **Input signal ranges:**

  ±5V, ±1V (software programmable)
- **Input coupling:** DC
- **Overvoltage protection:**

Range	Overvoltage protection
±5V	±10V
±1V	±5V

- **Input impedance:**

  50Ω (default), 1.5MΩ (soldering selectable)
- **System Noise:** (typical)

Range	Noise(LSBrms)
±5V	1.25

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±1V	1.75

- **Crosstalk:** < -80dB, DC to 1MHz
- **Total Harmonic Distortion (THD)*:** -75dB
- **Signal-to-noise ratio (SNR)*:**

Range	SNR (dB)
±5V	66
±1V	62

- **Spurious-free dynamic range (SFDR)*:** 75dB

*Measured using 200kHz sine wave input with amplitude of 95% of full scale at 60MS/s

♦ Timebase System

- **Sources:** Internal 60MHz, external sine wave, SSI TIMEBASE
- **External sine wave source:**

  Connector: SMB

  Impedance: 50Ω

  Coupling: AC

  Input amplitude: $1V_{pp}$ to $2V_{pp}$

  Overvoltage protection: $2.5V_{pp}$

  Frequency range:

  Ping-pong mode: 25MHz - 65MHz

  Others: 500kHz - 65MHz

♦ Triggering

- **Sources:** software, analog, digital, SSI
- **Modes:** pre-trigger, middle-trigger, post-trigger, delay-trigger
- **Repeated trigger rearming interval:** 2 cycles of timebase
- **Pre-trigger depth:** 64MB to 512MB, depending on memory size
- **Post-trigger depth:** 64MB to 512MB, depending on memory size

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- **Analog triggering**

  Sources: CH0 and CH1

  Slope: rising/falling

  Coupling: DC

  Trigger sensitivity: 256 steps in full-scale voltage range

  Hysteresis: 1.5% of the full range

  Offset error: 1.25% of the full range

- **Digital triggering**

  Connectors: SMB

  Slope: rising/falling

  Compatibility: 5V/TTL

  Minimum pulse width: 20ns

♦ Calibration

- **Recommended warm-up time:** 15 minutes
- **On-board calibration reference:**

  Level: 5.000V

  Temperature coefficient: ±2ppm/°C

  Long-term stability: 6ppm/1000Hr

♦ General Specifications

- **Dimensions:** (not including connectors)

  175mm by 107mm

- **I/O connector:**

  BNC x 2 for analog inputs

  SMB x 2 for external timebase and external digital trigger

- **PCI signaling environment:**

  Universal board, supports a 32-bit 3.3V or 5V PCI bus

- **Operating environment:**

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Ambient temperature: 0 to 50°C

Relative humidity: 10% to 90% non-condensing

- **Storage environment :**

  Ambient temperature: -20 to 80°C

  Relative humidity: 10% to 90% non-condensing

- **Power requirement:** (typical)

Power Rail	Current (mA)
5V	895
12V	295
3.3V	310 (with 128MB onboard SDRAM memory) 430 (with 512MB onboard SDRAM memory)

1.4 Software Support

ADLINK provides versatile software drivers and packages for users' differing approaches to building up a system. ADLINK not only provides programming libraries such as DLLs for most Windows based systems, but also drivers for other software packages such as LabVIEW®.

All software options are included in the ADLINK CD. Non-free software drivers are protected with licensing codes. Without the software code, you can install and run the demo version for two hours for trial/demonstration purposes. Please contact ADLINK dealers to purchase the formal license.

1.4.1 Programming Library

For customers who are writing their own programs, we provide function libraries for many different operating systems, including:

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- **WD-DASK:** Includes device drivers and DLLs for **Windows 98**, **Windows NT**, and **Windows 2000**. DLL is a binary compatible across Windows 98, Windows NT, and Windows 2000. All applications developed with WD-DASK are compatible across Windows 98, Windows NT, and Windows 2000. The developing environment can be VB, VC++, Delphi, BC5, or any Windows programming language that allows calls to a DLL. The user's guide and function reference manual of WD-DASK are in the CD (`\Manual_PDF\Software\WD-DASK`).

- **WD-DASK/X:** Includes device drivers and shared libraries for Linux. The developing environment can be Gnu C/C++ or any programming language that allows linking to a shared library. The user's guide and function reference manual of WD-DASK/X are in the CD (`\Manual_PDF\Software\WD-DASK-X`).

1.4.2 WD-LVIEW: LabVIEW® Driver

WD-LVIEW contains the VIs, which are used to interface with National Instrument's LabVIEW® software package. The WD-LVIEW supports Windows 98/NT/2000. The LabVIEW® driver is shipped free with the card. Users can install and use them without a license. For detailed information about WD-LVIEW, please refer to the user's guide in the CD (`\Manual_PDF\Software\WD-LVIEW`)

1.4.3 WD-OCX: ActiveX Controls

We suggest customers who are familiar with ActiveX controls and VB/VC++ programming use WD-OCX ActiveX control component libraries for developing applications. WD-OCX is designed for Windows 98/NT/2000. For more detailed information about WD-OCX, please refer to the user's guide in the CD (`\Manual_PDF\Software\WD-OCX\WD-OCX.PDF`)

The above software drivers are shipped with the card. Please refer to the "***Software Installation Guide***" in the package to install the drivers.

In addition, ADLINK supplies ActiveX control software *DAQBench*. *DAQBench* is a collection of ActiveX controls for measurement or automation applications. With *DAQBench*, users can easily develop custom interfaces to display data, analyze acquired data or data received from other sources, or integrate with popular applications or other data sources. For more detailed information about *DAQBench*, please refer to the user's guide in the CD (`\Manual_PDF\Software\DAQBench\DAQBenchManual.PDF`)

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Users can also get a free 4-hour evaluation version of *DAQBench* from the CD. Please contact ADLINK or an ADLINK dealer to purchase the software license.

1.5 Block Diagram

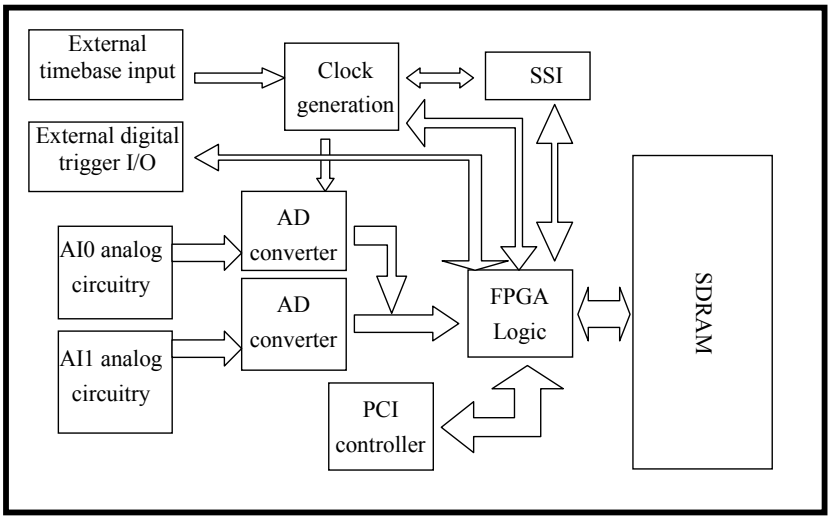


Figure 1.1: PCI-9820 block diagram

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2

Installation

This chapter describes how to install the PCI-9820. The contents of the package and unpacking information are also outlined.

The PCI-9820 performs an automatic configuration of the IRQ and port address. Users can use the software utility, `PCI_SCAN`, to read the system configuration.

2.1 Contents of Package

In addition to this *User's Guide*, the package should include the following items:

- PCI-9820 Digitizer
- ADLINK All-in-one Compact Disc
- Software Installation Guide

If any of these items are missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in to ship or store the product in the future.

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2.2 Unpacking

Your PCI-9820 card contains electro-static sensitive components that can be easily be damaged by static electricity.

Therefore, the card should be handled on a grounded anti-static mat. The operator should be wearing an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the card module carton for obvious damage. Shipping and handling may cause damage to the module. Be sure there is no shipping and handling damage on the module carton before continuing.

After opening the card module carton, extract the system module and place it only on a grounded anti-static surface with component side up.

Again, inspect the module for damage. Press down on all the socketed IC's to make sure that they are properly seated. Do this only with the module place on a firm flat surface.

You are now ready to install your PCI-9820.

Note: DO NOT APPLY POWER TO THE CARD IF IT HAS BEEN DAMAGED.

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2.3 PCI Configuration

1. Plug and Play:

As a Plug and Play component, the card requests an interrupt number via its PCI controller. The system BIOS responds with an interrupt assignment based on the card information and on known system parameters. These system parameters are determined by the installed drivers and the hardware load seen by the system.

2. Configuration:

The board configuration is done on a board-by-board basis for all PCI boards on your system. Because configuration is controlled by the system and software, there is no jumper setting required for base-address, DMA, and interrupt IRQ.

The configuration is subject to change with every boot of the system as new boards are added or removed.

3. Trouble shooting:

If your system doesn't boot or if you experience erratic operation with your PCI board in place, it's likely caused by an interrupt conflict (perhaps the BIOS Setup is incorrectly configured). In general, the solution, once you determine it is not a simple oversight, is to consult the BIOS documentation that comes with your system.

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3

Signal Connections

This chapter describes the connectors of the PCI-9820, and the signal connections between the PCI-9820 and external devices.

3.1 Connectors

Fig. 3.1 shows the location of connectors on the PCI-9820. The connector types and functions are described as follows.

CLK IN: The SMB connector is a 50Ω, AC-coupled external reference timebase input.

TRG IO: The SMB connector is for external digital trigger input or output.

CH0: The BNC connector is for attaching the analog input signal to measure on channel 0.

CH1: The BNC connector is for attaching the analog input signal to measure on channel1.

SO-DIMM: The SO-DIMM connector is for plugging the 144-pin SDRAM SODIMM.

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SSI: The SSI connector is the System Synchronization Interface for synchronizing multiple cards. The pin assignment is described as follows:

Signal Name	Direction	Description	Location
SSI_TIMEBASE	Input/Output	60MHz timebase signal through SSI	pin 1
SSI_TRIG1	Input/Output	Trigger signal through SSI	pin 11
SSI_TRIG2	Input/Output	Clocked trigger signal through SSI	pin 9
SSI_START_OP	Input/Output	Acquisition start signal in pre-trigger or middle-trigger mode	pin 7
GND	--	Ground	pins 2, 4, 6, 8, 10, 12, 14, 16, 18, 20
NC	--	No Connection	pins 3, 13
Reserved	Input/Output	Reserved for future use	pins 5, 15, 17, 19

Table 3.1: Signal Locations

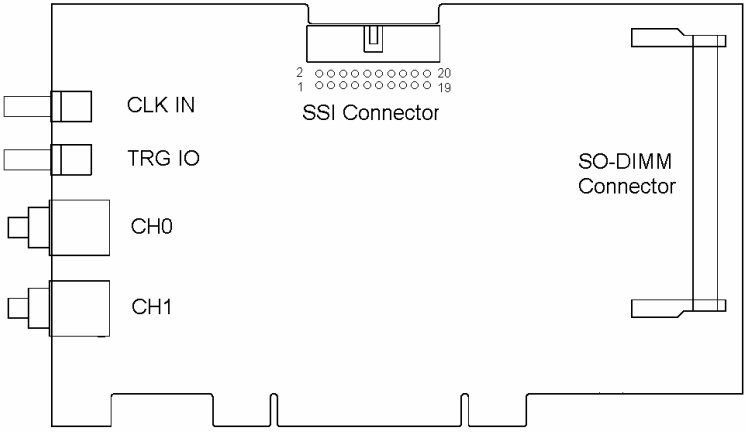


Figure 3.1: Location of connectors

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3.2 Analog Input Impedance Setting

3.2.1 Analog Input Impedance Setting

The CH0 and CH1 input impedance can be selected to 50Ω or 1.5MΩ by soldering gap switches J6 and J7 on the backside of the PCI-9820. The location of J6, J7 and the corresponded input impedance setting are shown in Fig. 3.2 and Table 3.2. The default setting is 50Ω input impedance.

J6	CH0 Input Impedance
Open	High (1.5MΩ)
Close (Default)	Low (50Ω)

J7	CH1 Input Impedance
Open	High (1.5MΩ)
Close (Default)	Low (50Ω)

Table 3.2: Location of solder switches

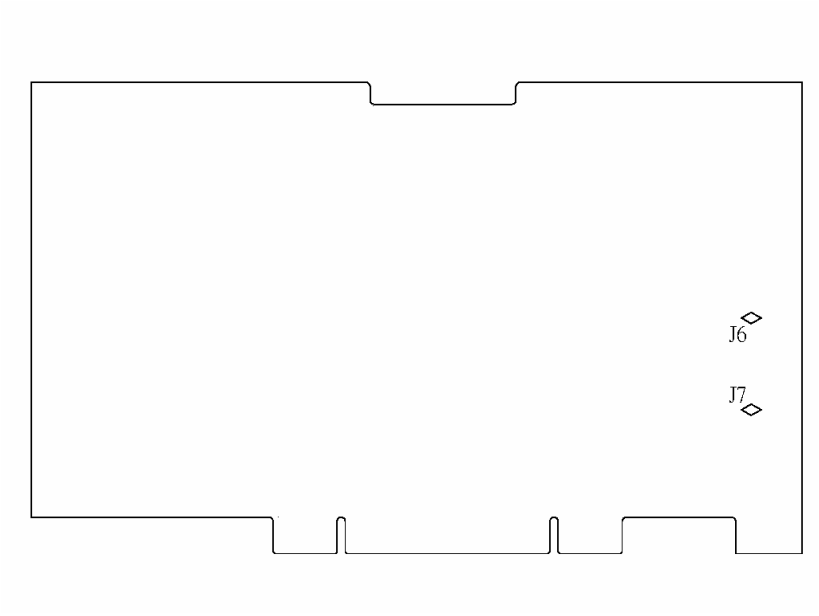


Figure 3.2: Location of solder switches

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NOTE:

If the high input impedance 1.5MΩ is selected, the output impedance of the signal sources should be kept low to avoid of the offset voltage caused by the input bias current, which is 2 μA min. and 25 μA max.

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4

Operation Theory

The operation theory of the PCI-9820 is described in this chapter, including the control and setting of signal sources, timebase sources, trigger sources, trigger modes, data transfers, synchronizing multiple cards, and auto-calibration.

4.1 Analog Input Signal Source Control

Number of Channels

The PCI-9820 provides two simultaneously sampled analog input channels in SE (single ended) connection. Each channel can be enabled individually.

Signal Range and Input impedance

The available signal input ranges are ±5V or ±1V, which can be set by software. All signals are DC-coupled. The input impedance for high-speed applications should also be considered. The selectable input impedance values are 50Ω and 1.5MΩ. Please refer to section 3.2 for the details.

4.2 A/D Sampling rate and TIMEBASE Sources Control

The PCI-9820 supports three timebase sources for analog input conversion:

- Internal 60MHz
- External sine wave
- SSI timebase

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Once choosing the timebase source, users can set a 24-bit counter to divide the timebase to get the needed sampling rate. The following formula determines the ADC sampling frequency:

Sampling Rate = Timebase Frequency / ADC Clock Divisor

where the ADC Clock Divisor = 1,2,3,4,5… 2^{24}-1(maximum)

For more information about SSI timebase, please refer to section 4.5

4.2.1 External sine wave clock source

Users can supply the timebase from external SMB connector **CLK IN**, which should be a sine wave signal. This signal is AC coupled with 50Ω input impedance and the valid input level is from 1 to 2 volts peak-to -peak. Note that the external clock must be continuous for correct ADC operation because of the pipeline architecture of the ADC.

4.2.2 130MS/s Sampling using Ping-Pong Mode

The PCI-9820 uses two A/D converters, each running at 60MS/s, to provide a dual-channel simultaneous real-time sampling rate of 60MS/s. (65MS/s with external timebase)

For the single-channel acquisition, the two ADCs can be clocked in a "ping-pong" mode to achieve up to 120MS/s sampling (130MS/s with external timebase). Note that only CH0 can be applied to ping-pong mode operation.

The onboard auto-calibration circuitry allows the two channels to be matched in order to reduce the image signal.

4.3 Trigger Modes

The PCI-9820 provides 4 trigger sources (internal software trigger, external analog trigger, external digital trigger, and SSI trigger signals). Users must select one of them as the source of the trigger event. A trigger event occurs when the specified condition is detected on the selected trigger source (For example, a rising edge on the external digital trigger input). Please refer to section 4.4 for more information about trigger sources.

There are 4 trigger modes (pre-trigger, post-trigger, middle-trigger, and delay-trigger) working with the 4 trigger sources to initiate different data acquisition timing when a trigger event occurs. They are described as follows.

4.3.1 Post-trigger Acquisition

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Use post-trigger acquisition when you want to collect data after the trigger event, as illustrated in Fig 4.1.

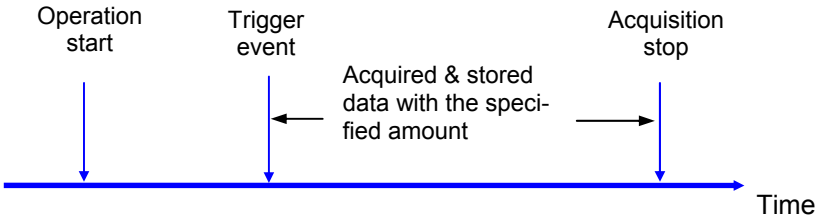


Figure 4.1 Post trigger

4.3.2 Pre-trigger Acquisition

Use pre-trigger acquisition to collect data before the trigger event. The acquisition starts once specified function calls are executed to begin the pre-trigger operation, and it stops when the trigger event occurs.

If the trigger event occurs after the specified amount of data has been acquired, the system only stores the data before the trigger event with the specified amount, as illustrated in Fig 4.2.

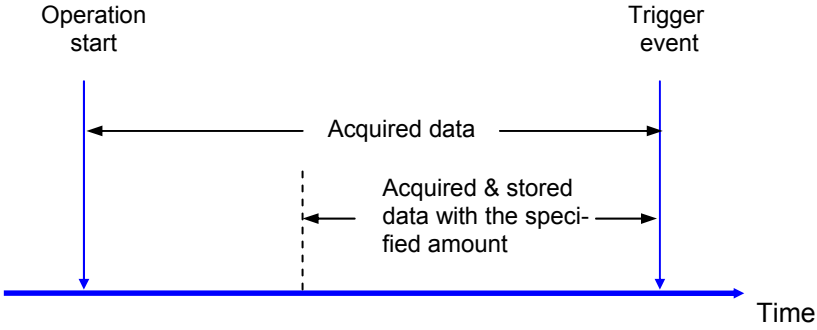


Figure 4.2 Pre trigger (the trigger event occurs after the specified amount of data has been acquired)

However, if the trigger event occurs before the specified amount of data has been acquired, the system can either stop the acquisition immediately (which implies the stored data will be less then the amount you specified) or ignore the trigger signal until the specified amount of data has been acquired (which assures the user can get the specified amount of data). These can be set by software and are illustrated in Fig 4.3 and Fig 4.4.

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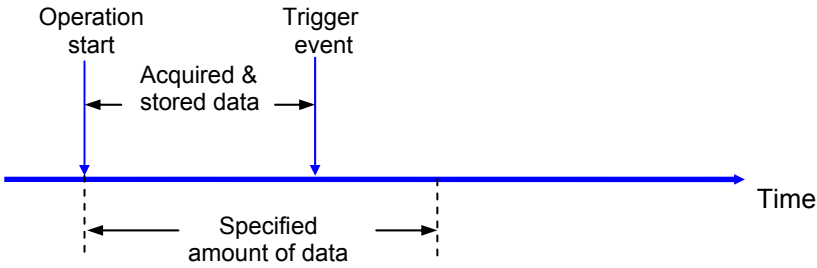


Figure 4.3 Pre trigger (The trigger signal is accepted anytime after the operation starts)

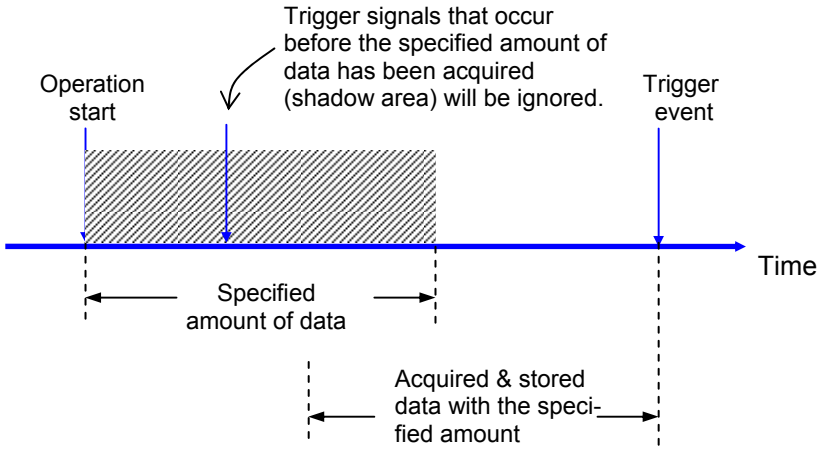


Figure 4.4 Pre trigger (The trigger signal will be ignored until the specified amount of data is acquired)

4.3.3 Middle-trigger Acquisition

Use middle-trigger acquisition when you want to collect data before and after the trigger event. The amount of stored data before and after the trigger can be set individually (M and N), as illustrated in Fig 4.5.

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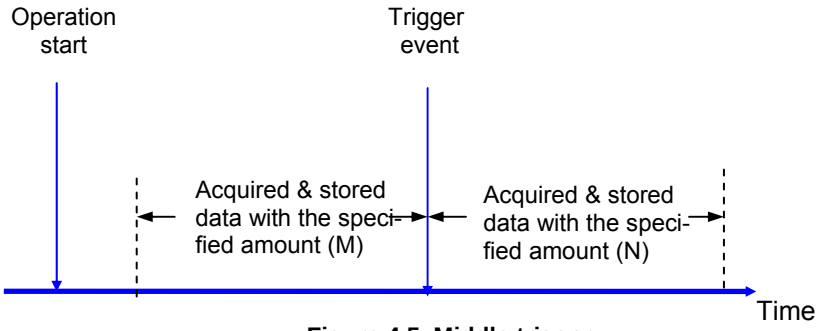


Figure 4.5 Middle trigger

Like pre-trigger mode, the stored data may be less than the amount specified if the trigger event occurs before the specified amount of data (M) has been acquired. Users can also set by program to ignore trigger signals until the specified amount of data (M) has been acquired.

4.3.4 Delay-trigger Acquisition

Use delay trigger acquisition to delay the data collection after the trigger event, as illustrated in Fig 4.6. The delay time is specified by a 32-bit counter value so that the maximum delay time is the period of timebase * (2^{32} –1), while the minimum delay time is the period of timebase.

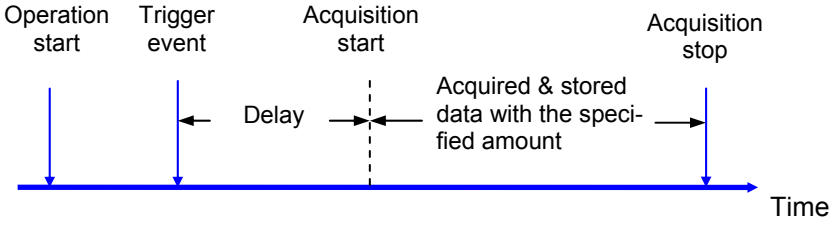


Figure 4.6 Delay trigger

4.3.5 Post-trigger of Delay-trigger Acquisition with Re-trigger

Use post-trigger or delay-trigger acquisition with re-trigger function to collect data after several trigger events, as illustrated in Fig 4.7. Users can program the number of triggers then the PCI-9820 will acquire an additional record each time a trigger is accepted until all the requested records have been

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stored in memory. After the initial setup, the process does not require software intervention.

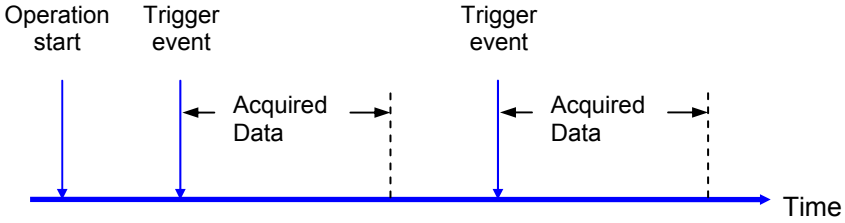


Figure 4.7 Post-trigger with re-trigger

4.4 Trigger Sources

In addition to the internal software trigger, the PCI-9820 also supports external analog, digital triggers and SSI triggers. Users can configure the trigger source by software. For SSI trigger operation, please refer to section 4.7.

4.4.1 Software-Trigger

This trigger mode does not need any external trigger source. The trigger asserts right after executing specified function calls to begin the operation.

4.4.2 External Analog Trigger

Users can choose either CH0 or CH1 as the trigger signal while using external analog trigger source. The trigger level can be set by software with 8-bit resolution. Please refer to table 4.1 for the ideal transfer characteristic.

Trigger Level digital setting	Trigger voltage (±5V range)	Trigger voltage (±1V range)
0xFF	4.96V	0.992V
0xFE	4.92V	0.984V
---	---	---
0x81	0.04V	0.008V
0x80	0	0
0x7F	-0.04V	-0.008V
---	---	---

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0x01	-4.96V	-0.992V

Table 4.1 Analog trigger ideal transfer characteristic

The trigger conditions for analog triggers are illustrated in Fig4.8 and described as follows:

- **Positive-slope trigger** - The trigger event occurs when the trigger signal (analog input signal) changes from a voltage that is lower than the specified trigger level to a voltage that is higher than the specified trigger level.
- **Negative-slope trigger** - The trigger event occurs when the trigger signal (analog input signal) changes from a voltage that is higher then the specified trigger level to a voltage that is lower than the specified trigger level.

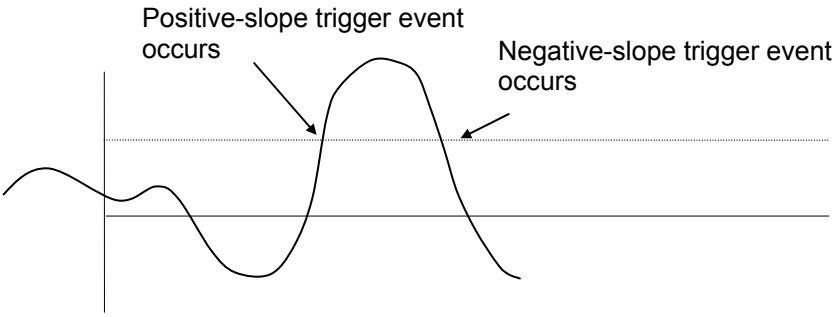


Figure 4.8 Analog trigger conditions

4.4.3 External Digital Trigger

An external digital trigger occurs when a TTL rising edge or a falling edge is detected at the SMB connector **TRG IO** on the front panel, as illustrated in Fig 4.9. The trigger polarity can be selected by software. Note that the signal level of the external digital trigger signal should be TTL-compatible, and the minimum pulse width is 20ns.

The **TRG IO** on the front panel can also be programmed to output the trigger signal when the trigger source is from software, analog trigger, or SSI trigger. The timing characteristic is in Fig 4.10.

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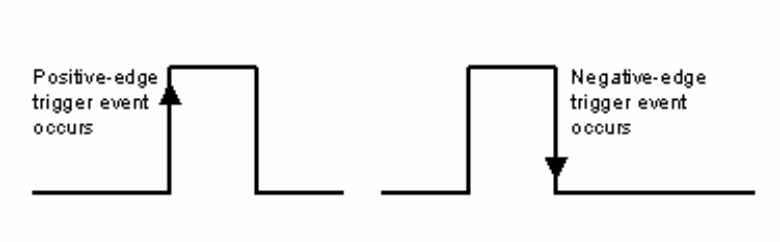


Figure 4.9 External digital trigger input

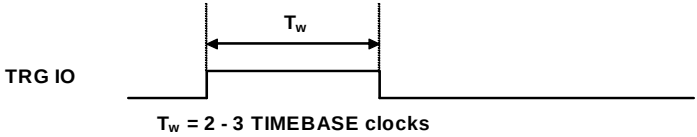


Figure 4.10 TRG IO output signal timing

4.5 Data Transfers

Since the maximum data throughput on the PCI-9820 (60MS/s * 2 channels * 2 Bytes/channel = 240MB/s) is much higher than the 32bit/33MHz PCI-bus bandwidth, samples are acquired into the onboard SDRAM memory before being transferred to the host computer. Since the number of stored samples per acquisition is limited by the amount of on-board memory, the PCI-9820 supports different sizes of SODIMM SDRAM ranging from 64MB to 512MB in order to meet application requirements.

Once all the data has been stored in the on-board memory, the data will be transferred to the host computer's memory through bus-mastering DMA.

In a multi-user or multi-tasking OS, like Microsoft Windows, Linux, and so on, it is difficult to allocate a large continuous memory block to do the DMA transfer. Therefore, the PCI-9820 provides the function of scatter /gather DMA to link the non-continuous memory blocks into a linked list so that users can transfer very large amounts of data without being limited by the fragment of small size memory, as illustrated in Fig 4.11.

If the data throughput from the PCI-9820 is less than the available PCI bandwidth (For example: 20MS/s * 2 channels * 2 Bytes/channel = 80MB/s),

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the PCI-9820 also features on-board 3k-sample FIFO to achieve real-time transfer bypassing the SDRAM, directly to host memory.

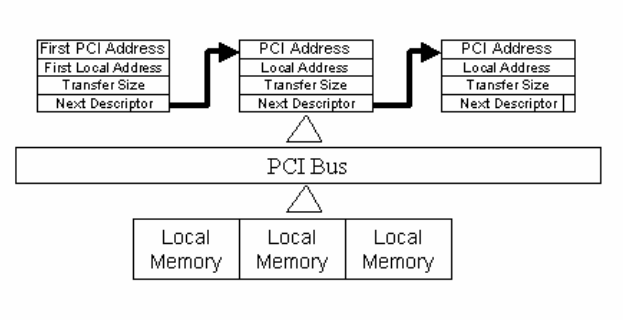


Figure 4.11 Scatter/gather DMA for data transfer

4.6 AI Data Format

Table 4.2 illustrates the ideal transfer characteristics of various input ranges of the PCI-9820. Bit13-0 is the acquired 14-bit A/D data with binary coding format while bit14 is the out-of-range indicator (logic "1" means out-of-range).

Description	Analog Input Voltage		Digital code
Full-scale Range	±5V	±1V	
Least significant bit	0.61mV	0.122mV	
> = FSR	>= 5V	>= 1V	7FFF
FSR-1LSB	4.99939V	0.999878V	3FFF
Midscale +1LSB	0.61mV	0.122mV	2001
Midscale	0V	0V	2000
Midscale –1LSB	-0.61mV	-0.122mV	1FFF
-FSR	-5V	-1V	0000
< -FSR	< -5V	< -1V	4000

Table 4.2 Analog input voltage and the output digital code (Note that bit14 is the out-of-range indicator)

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4.7 Synchronizing Multiple Devices

SSI (System Synchronization Interface, please refer to 3.1 for its location) provides the timing synchronization between multiple cards. Users can connect a special ribbon cable (ACL-SSI) to all the cards in a daisy-chain configuration.

The bi-directional SSI I/Os provide a flexible connection between cards, which allows one SSI master PCI-9820 to output the SSI signals to up to three slaves PCI-9820s to receive the signals. Table 4.3 lists the summary of SSI timing signals and the functionalities.

SSI timing signal	Functionality
SSI_TIMEBASE	Input/Output 60MHz timebase signal through SSI
SSI_TRIG1	Input/Output the trigger signal through SSI
SSI_TRIG2	Input/Output the clocked trigger signal through SSI
SSI_START_OP	Input/Output the acquisition start signal in pre-trigger or middle-trigger mode

Table 4.3 Summary of SSI timing signals and the corresponding functionalities

4.7.1 SSI_TIMEBASE

As an output, the SSI_TIMEBASE signal outputs the onboard 60MHz LVTTL timebase through SSI connector. Note that a timebase generated from external sine wave SMB connector input cannot be routed to SSI_TIMEBASE.

As an input, the PCI-9820 accepts the SSI_TIMEBASE signal to be the source of timebase.

4.7.2 SSI_TRIG1

As an output, the SSI_TRIG1 signal reflects the trigger event signal in an acquisition sequence. Please refer to Fig 4.1 - Fig 4.7 for the relationship between the trigger event and the acquisition sequence. Users can use the function SSI_SourceConn() to output the SSI_TRIG1 signal.

As an input, the PCI-9820 accepts the SSI_TRIG1 signal to be the trigger event source. The signal is configured in the rising edge-detection mode. When selecting the trigger sources of the PCI-9820, Users can select **TRSRC_SSI_1** to set SSI_TRIG1 as the source of trigger event.

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Fig 4.12 and Fig 4.13 show the input and output timing requirements.

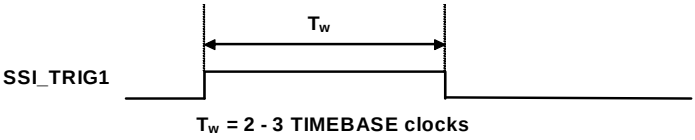


Figure 4.12 SSI_TRIG1 output signal timing

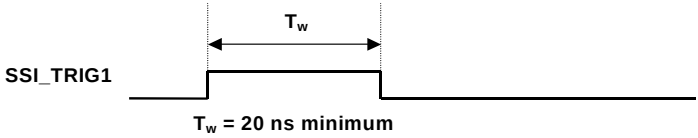


Figure 4.13 SSI_TRIG1 input signal timing

4.7.3 SSI_TRIG2 and SSI_START_OP

As an output, the SSI_TRIG2 signal is a clocked SSI_TRIG1 signal by TIMEBASE, as illustrated in Fig 4.14.

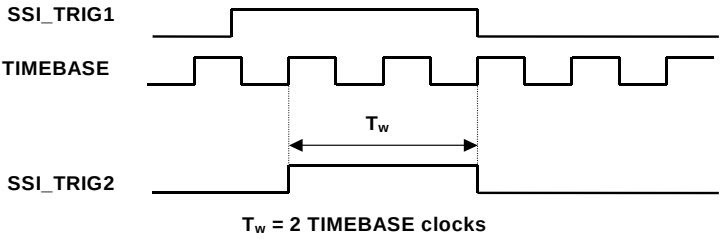


Figure 4.14 SSI_TRIG2 output signal timing

As an input, the PCI-9820 accepts the SSI_TRIG2 signal to be the source of a one-clock delayed trigger event. The controller on the PCI-9820 will then compensate the one-clock delay if using SSI_TRIG2 as the source of trigger event. The signal is configured in the rising edge-detection mode.

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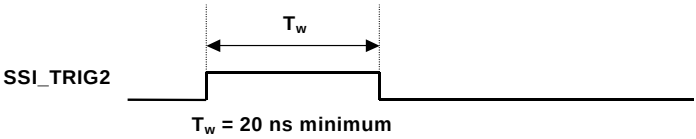


Figure 4.15 SSI_TRIG2 input signal timing

As an output, the SSI_START_OP signal reflects the operation start signal in a pre-trigger or middle-trigger acquisition sequence. Please refer to Fig 4.2 - Fig 4.5 for the relationship between the operation start signal and the acquisition sequence.

As an input, the PCI-9820 accepts the SSI_START_OP signal to be the operation start signal in a pre-trigger or middle-trigger acquisition sequence. The signal is configured in the rising edge-detection mode. Fig 4.16 and Fig 4.17 show the SSI_START_OP signal input and output timing requirements.

For enabling output operations, users can use the function SSI_SourceConn() to output the SSI_TRIG2 and SSI_START_OP signals.

For the input operations, users can select **TRSRC_SSI_2** to set SSI_TRIG2 and SSI_START_OP as the source of the trigger event and operation start signal.

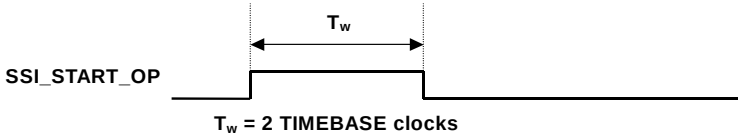


Figure 4.16 SSI_START_OP output signal timing

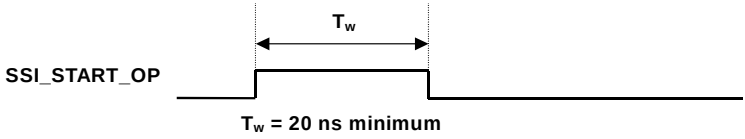


Figure 4.17 SSI_START_OP input signal timnig

4.7.4 Comparing the different trigger sources from SSI

When selecting **TRSRC_SSI_1** as the trigger source input, the signal SSI_TRIG1 reflects the trigger event signal in an acquisition sequence. However, when synchronizing multiple PCI-9820 devices, each PCI-9820

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may recognize the trigger signal with one-clock time difference because the signal is not related to the timebase.

There is another phenomenon if using **TRSRC_SSI_2** in pre-trigger and middle-trigger mode. The operation start signal is generated by a software command so multiple PCI-9820 devices don't start the data acquisition simultaneously, which may result in the fact that the amount of stored samples are different if the trigger event occurs before the specified amount of data has been acquired.

When selecting **TRSRC_SSI_2** as the trigger source input, SSI_TRIG2 and SSI_START_OP can achieve a better synchronization between multiple PCI-9820 devices. A clocked SSI_TRIG2 can guarantee all PCI-9820 devices recognize the trigger event at the same clock edge if they use the same timebase. In pre-trigger and middle-trigger mode, SSI_START_OP guarantees all the PCI-9820 devices start the data acquisition at the same time.

4.8 Auto-calibration

By using the auto-calibration feature of the PCI-9820, the calibration software can measure and correct offset and gain errors without any external signal connections, reference voltages, or measurement devices.

After the auto-calibration procedure finishes, the calibration constants can be saved into the EEPROM. In addition to the default bank of factory calibration constants, there are three extra user-modifiable banks in the EERPOM for users to store three sets of calibration constants according to different environments and re-load the calibration constants when necessary.

Because of the fact that errors in measurements will vary with time and temperature, it is recommended that users re-calibrate the PCI-9820 when the card is installed in a new environment.

Note: Before auto-calibration procedure starts, please warm up the card for at least 15 minutes.

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   d. Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals.
   e. Damage caused by leakage of battery fluid.
   f. Damage from improper repair by unauthorized technicians.
   g. Products with altered and/or damaged serial numbers.
   h. Other categories not protected under our guarantees.
5. Customers are responsible for shipping costs to transport damaged products to our company or sales office.
6. To ensure the speed and quality of product repair, please download a RMA application form from our company website: www.adlinktech.com. Damaged products with attached RMA forms receive priority.

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