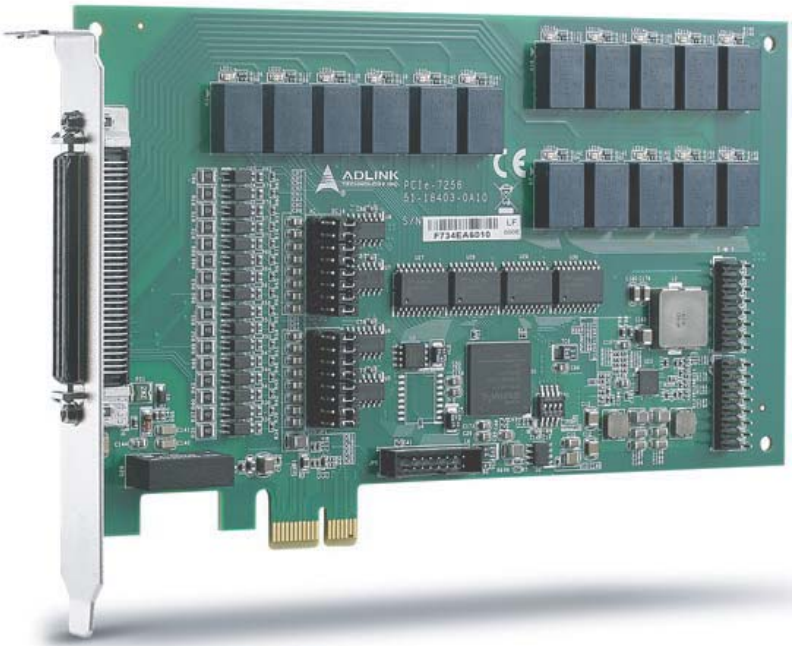
PCIe-7256

16CH Latching Relay Output/16CH Isolated DI Card



Manual Rev.: 2.00

Revision Date: Jan. 7, 2016

Part No: 50-11043-1000

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Revision History

Revision	Release Date	Description of Change(s)
2.00	Jan.7, 2016	Initial release

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Preface

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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.


NOTE:

Additional information, aids, and tips that help users perform tasks.


CAUTION:

Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.


WARNING:

Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

ADLINK'S PCIe-7256 is a basic Digital I/O card for PCIe bus computer in industrial applications. The PCIe-7256 provides 16 latching relay actuators and 16 opto-isolated digital inputs, and all relays are Form C, suitable for ON/OFF control devices.

All digital input channels are identical non-polar and opto-isolated, and each is switchable using RC or non-RC filter. All channels are isolated and suitable for collecting digital inputs in noisy environments. COS (Change-of-State) interrupt is supported, whereby when any digital input changes state, an interrupt is generated to allow management of the external event.

Latching relays conserve power, and the status of each latching relay output is indicated by LED, such that when the latching relay is SET, its corresponding onboard LED is lit. Also enabled is Board ID setting, providing identification of a specified card when two or more PCIe-7256 cards are deployed in a single system, and all I/O signals are transmitted via 68-pin SCSI connector.

1.1 Features

- PCI Express x1, Plug and Play
- 16 latching relay actuator outputs, with output status retained after power-off
- 16 opto-isolated digital inputs
- LED indicators show relay status
- Jumper-selectable AC-filtered/non-AC-filtered input signals
- Onboard relay driving circuits
- COS (Change-of-State) detection for digital input channels
- Digital input channel 0 & 1 interrupt
- Dry contact input available
- Board ID setting

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1.2 Applications

- Industrial ON/OFF control
- External high power relay driving, signal switching
- Laboratory automation
- Industrial automation
- Switch contact status detection and limit switch monitoring & control systems

1.3 Specifications

1.3.1 Digital Input

Input channels	16
Photocoupler	PC-3H4
Input current	▶ 10 mA rated ▶ 50 mA max. for isolated input
Input voltage	▶ Up to 24V DC or 24V AC ▶ Logic Low: 0 to 2V ▶ Logic High 5 to 24V
Input impedance	4.7 kΩ
Input mode	Isolation AC filter/Non-AC filter
Isolated voltage	2,500 Vrms channel-to-system

1.3.2 Relay Output

Output channels	16
Relay type	16 DPDT (Form C)
Contact rating	125V AC/0.5A, 30V DC/1A
Breakdown voltage	1000 Vrms
Release time	3 msec
Operate time	3 msec
Contact resistance	60mΩ
Insulation resistance	1000MΩ min. (at 500V DC)

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Life expectancy (min. operations)	▶ 2x 10^5 times at 30V DC/1A ▶ 10^5 times at 125V AC/0.5A
Vibration resistance	176.4m/s^2 (18G), 10 to 55Hz at double amplitude of 3mm
LED indicators	Monitor SET/RESET status of each relay; external LED connectors applicable
Relay power supply	+ 5V from onboard power source

1.3.3 Isolated +5V Power Supply

Output Voltage	+5V
Output Current	170mA max. (@ 40°C)

1.3.4 Physical & Bus

Dimensions	175 mm x 107 mm, standard PCIe half size
Bus	1x PCI Express
Operating temperature	0 to 60 °C
Storage temperature	-20 °C to 80 °C
Humidity	5 to 95% non-condensing
Power consumption	▶ +12V@141mA(typical) 500mA (Max.) ▶ +3.3V@36.6mA(typical) 45mA (Max.) (when all relays are activated simultaneously)

1.4 Software Support

ADLINK provides comprehensive software solutions for all system building requirements. In addition to programming libraries such as DLLs for most Windows-based systems, ADLINK also provides drivers for other application environments such as LabVIEW®.

Be sure to install the driver & utility before using the PCIe-7256.

PCIS-DASK

PCIS-DASK consists of advanced 32/64-bit kernel drivers and SDK for customized DAQ application development, enabling

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detailed operations and superior performance and reliability from data acquisition systems.

PCIS-DASK kernel drivers now support Windows 7/8.1 OS.

1.5 PCB Layout

NOTE: All dimensions shown are in mm

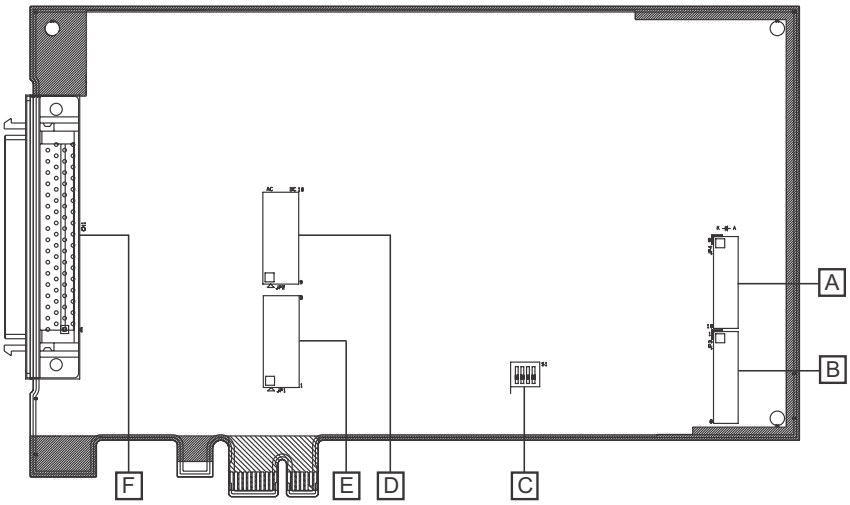


Figure 1-1: PCIe-7256 Board Layout

	Name	Description
A	JP4	External LED connector setting
B	JP3	External LED connector setting
C	S1	Board ID setting
D	JP2	AC & Non-AC filter setting
E	JP1	AC & Non-AC filter setting
F	CN1	68-pin SCSI connector

Table 1-1: PCIe-7256 Board Layout Legend

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1.6 Connectors

The PCIe-7256 is equipped with a 68-pin SCSI connector (CN1).

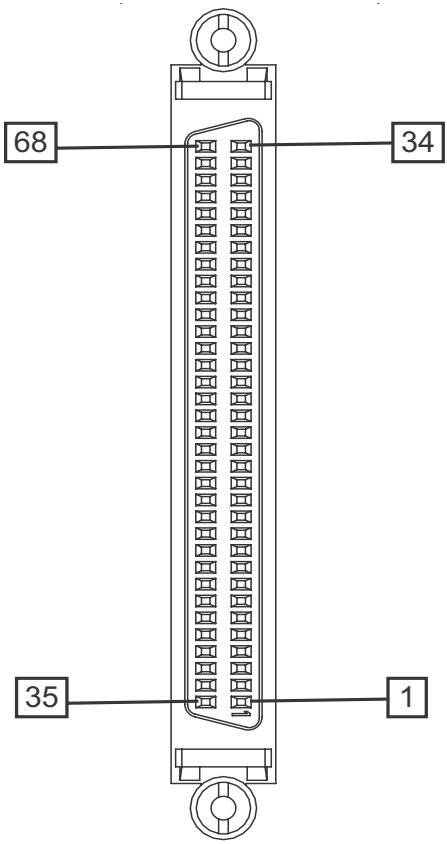


Figure 1-2: PCIe-7256 CN1 Connector

ID	Pin	Pin	ID
NO15	68	34	NO7
COM15	67	33	COM7
NC15	66	32	NC7

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ID	Pin	Pin	ID
NO14	65	31	NO6
COM14	64	30	COM6
NC14	63	29	NC6
NO13	62	28	NO5
COM13	61	27	COM5
NC13	60	26	NC5
NO12	59	25	NO4
COM12	58	24	COM4
NC12	57	23	NC4
NO11	56	22	NO3
COM11	55	21	COM3
NC11	54	20	NC3
NO10	53	19	NO2
COM10	52	18	COM2
NC10	51	17	NC2
NO9	50	16	NO1
COM9	49	15	COM1
NC9	48	14	NC1
NO8	47	13	NO0
COM8	46	12	COM0
NC8	45	11	NC0
DI15	44	10	DI14
DI13	43	9	DI12
DI11	42	8	DI10
DI9	41	7	DI8
DICOM1	40	6	DICOM2
DI7	39	5	DI6
DI5	38	4	DI4
DI3	37	3	DI2
DI1	36	2	DI0
ISOGND	35	1	ISO5V

Table 1-2: PCIe-7256 CN1 Pin Assignment

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1.7 External LED Connection

16 onboard LEDs indicate the operating status of the 16 relays. In addition, 16 external LED connectors are available for users applications. Utilizing external LEDs connecting with JP3 and JP4, relay status can be displayed on chassis, panel, or other apparatus. Only LEDs with forward voltage (Vf) lower than 2V can function. Each external LED connector has a current limiting resistor (330Ω) connecting with +3.3 V power, eliminating the need for addition of a resistor to limit current flow through the LED.

Before connecting external LEDs, ensure the LED is in the right direction, as shown.

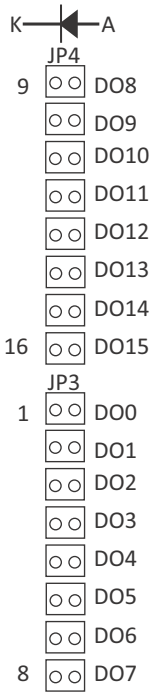


Figure 1-3: External LED Connectors

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2 Getting Started

2.1 Unpacking Checklist

Before unpacking, check the shipping carton for any damage. If the shipping carton and/or contents are damaged, inform your dealer immediately. Retain the shipping carton and packing materials for inspection. Obtain authorization from your dealer before returning any product to ADLINK. Ensure that the following items are included in the package.

- PCIe-7256 high-speed DI/O card
- Quick Start Guide

If any of the items is damaged or missing, contact your dealer immediately.



The card must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the card. Wear a grounded wrist strap when servicing.

2.2 Installing the Card

Install the card driver before you install the card into your computer system. See “Software Support” on page 3. for driver support information.

To install the card:

1. Turn off the system/chassis and disconnect the power plug from the power source.
2. Remove the system/chassis cover.
3. Select the PCIE Express slot that you intend to use, then remove the bracket opposite the slot, if any.
4. Align the card connectors (golden fingers) with the slot, then press the card firmly until the card is completely seated on the slot.
5. Secure the card to the chassis with a screw.

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6. Replace the system/chassis cover.
7. Connect the power plug to a power source, then turn on the system.

Configuration

All PCI/PCIE Express cards on your system are configured individually. Because configuration is controlled by the system and the software, no jumper setting is required for base address, DMA, and interrupt IRQ. Configuration is subject to change with every boot of the system as new PCI/PCIE Express® cards are added or removed.

Troubleshooting

If your system fails to boot or if you experience erratic operation with your PCI/PCIE Express card in place, an interrupt conflict may have been generated (such as when the BIOS Setup is incorrectly configured). Refer to the system's BIOS documentation for details.

2.3 Setting Jumpers

The PCIe-7256's plug and play eliminates the need to set up base address and IRQ level to allow operation in the host system. However, for more versatile operation, some jumpers can be set for digital input. Jumpers on the PCIe-7256 configure digital input channels for AC-filtered or non-AC-filtered input, as shown.

Jumper	Input Signal
JP1	DI0 to DI7
JP2	DI8 to DI15

Default setting of input signal selection is non-AC-Filtered (DC signal input), as shown.

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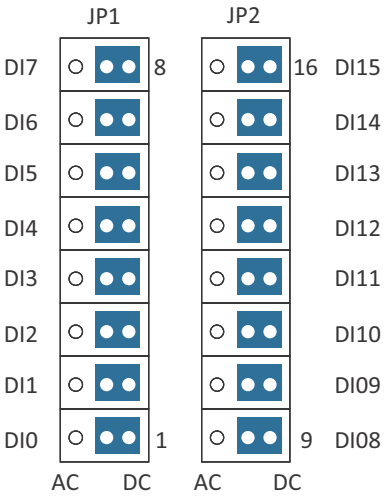
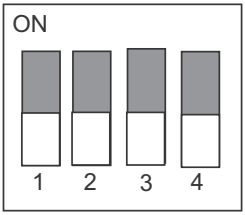


Figure 2-1: Default Input Signal Jumper Settings

2.4 Setting Board ID

When more than one data acquisition card is installed in the system, identification of specific cards can be a problem. The PCIe-7256 provides Board ID function, in which, according to settings of a DIP switch located in S1, ID is directly assigned to specific cards, providing error-free access to the card. Switch setting conditions are as shown, wherein 1= ON and 0 = OFF.



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Board ID	Switch			
	1	2	3	4
0	1	1	1	1
1	0	1	1	1
2	1	0	1	1
3	0	0	1	1
4	1	1	0	1
5	0	1	0	1
6	1	0	0	1
7	0	0	0	1
8	1	1	1	0
9	0	1	1	0
10	1	0	1	0
11	0	0	1	0
12	1	1	0	0
13	0	1	0	0
14	1	0	0	0
15	0	0	0	0

Table 2-1: Board ID Setting Conditions

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3 Register Format

The following detailed register format descriptions are helpful for low-level programming, although it is recommended that users first fully understand the PCIe interface.

3.1 I/O Address Map

PCIe-7256 registers are all 16 bits wide, accessible only via 16-bit I/O instruction. Relays and status of isolation input is controlled by register access. The register map, including descriptions and offset addresses relative to the base address, is as follows.

Offset	Write	Read
0x00h	Relay output CH 0 to 7	--
0x02h	Relay output CH 8 to 15	Relay output read back CH 0 to 15
0x04h	---	Isolated input CH. 0 to 15
0x06h	COS setup register	COS latch register
0x08h	Interrupt control register	Interrupt status register

Table 3-1: PCIe-7256 Register Map

3.2 Relay Output Control Register

The 16 latching relays are each controlled by two bits of the control register. Setting (0,1) indicates the latching relay is in RESET, under which normal open (NO) signal line is ‘open’ from the common (COM) line, and the normal close (NC) signal line is connected with the common line. Setting (1,0) indicates the normal open signal line is now closed, while the NC signal is open.

Note that filling the register with (1,1) can cause uncertain output status of the relay.

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Address: BASE + 0x00

Attribute: Write

7	6	5	4	3	2	1	0
DO3_S	DO3_R	DO2_S	DO2_R	DO1_S	DO1_R	DO0_S	DO0_R
15	14	13	12	11	10	9	8
DO7_S	DO7_R	DO6_S	DO6_R	DO5_S	DO5_R	DO4_S	DO4_R

Address: BASE + 0x02

Attribute: Write

7	6	5	4	3	2	1	0
DO11_S	DO11_R	DO10_S	DO10_R	DO9_S	DO9_R	DO8_S	DO8_R
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DO15_S	DO15_R	DO14_S	DO14_R	DO13_S	DO13_R	DO12_S	DO12_R

DOx_R: Reset bit of relay output channel x, x=0~15

DOx_S: Set bit of relay output channel x, x=0~15

3.3 Relay Output Read Back Register

The status of the latching relay can be read back from the read-back register. If the relay is in RESET, the corresponding bit value is 0. If the relay is in SET, the corresponding bit value is 1.

Address: BASE + 0x02

Attribute: Read

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8

DIx: isolated digital input channel x, x=0~15

1: input voltage high

0: input voltage is low

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3.4 Isolated Digital Input Register

Status of the 16 isolated input channels can be read from the isolated input register. Each bit corresponds to each channel, with bit value of 1 indicating input logic is high and 0 low.

Address: BASE + 0x04

Attribute: Read

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8

DIx: isolated digital input channel x, x=0~15

1: input voltage is high

0: input voltage is low

3.5 COS Setup Register

The PCIe-7256 provides COS (Change-of-State) interrupt function on any one digital input channel, enabling monitoring of input channel status. Enabling the COS Setup registers generates an interrupt when the corresponding channel changes state, whether rising edge signal or falling edge signal.

Address: BASE + 0x06

Attribute: Write

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COS	COS	COS	COS	COS	COS	COS	COS
SET7	SET6	SET5	SET4	SET3	SET2	SET1	SET0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COS	COS	COS	COS	COS	COS	COS	COS
SET15	SET14	SET13	SET12	SET11	SET10	SET9	SET8

COS SETx: change-of-state setup of DI channel x, x=0 ~15

1: enables COS interrupt

0: disables COS interrupt

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3.6 COS Latch Register

When COS occurs, the COS Latch Register also latches DI data, until the interrupt request is cleared, at which point the COS Latch register is automatically cleared. The COS function frees the CPU from the task of polling all input channels, increasing I/O performance.

Address: BASE + 0x06

Attribute: Read

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CL7	CL6	CL5	CL4	CL3	CL2	CL1	CL0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CL15	CL14	CL13	CL12	CL11	CL10	CL9	CL8

CL x: COS latch register of DI channel x, x = 0 ~ 15

1: digital input voltage is in high level

0: digital input voltage is in low level

3.7 Interrupt Control Register

In a first interrupt mode, COS interrupt function is enabled to monitor the enabled input channel's status whenever the status changes from 0 to 1 or 1 to 0. In a second mode, digital input channel 0, channel 1, or both can be selected as interrupt sources. In this mode, interrupt only asserts when DI status changes from 0 to 1, that is, the rising edge. Because the two modes share the same interrupt signal in the hardware, both cannot be enabled at the same time. After processing the interrupt request event, the interrupt request must be cleared to handle another interrupt request. To clear the interrupt request, write 1 to the corresponding bit.

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Address: BASE + 0x08

Attribute: Write

7	6	5	4	3	2	1	0
---	---	---	---	---	CH1 CLR	CH0 CLR	COS CLR
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
---	---	---	---	---	CH1 Int_EN	CH0 Int_EN	COS Int_EN

COS CLR (bit 0): write 1 to clear the COS interrupt.

1 : clear the COS interrupt

0 : no effect

CH0 CLR (bit 1): write 1 to clear DI channel 0 interrupt.

1 : clear DI channel 0 interrupt

0 : no effect

CH1 CLR (bit 2): write 1 to clear DI channel 1 interrupt.

1 : clear DI channel 1 interrupt

0 : no effect

COS Int_EN (bit 8): Write/Read

Change-of-State interrupt enable control

1 : enable

0 : disable

CH0 Int_EN (bit 9): Write/Read

DI channel 0 interrupt enable control

1 : enable

0 : disable

CH1 Int_EN (bit 10): Write/Read

DI channel 1 interrupt enable control

1 : enable

0 : disable

All possible combinations of interrupt source are shown as follows.

Interrupt	Bit 10	Bit 9	Bit 8	IRQ Source	IRQ Trigger Condition
Disable	0	0	0	Interrupt disable	--
Mode 1	0	0	1	COS interrupt	Change of state in enabled channel
Mode 2	0	1	0	Ch.0 interrupt enable	Rising edge of DI channel 0
Mode 2	1	0	0	Ch.1 interrupt enable	Rising edge of DI channel 1
Mode 2	1	1	0	Ch.0 & 1 interrupt enable	Rising edge of DI channel 0 or 1
Forbidden	0	1	1	Not allowed (disable)	---
	1	0			
	1	1			

3.8 Interrupt Status Register

When interrupt occurs, provides information to determine interrupt status and interrupt setup condition.

Address: BASE + 0x08

Attribute: Read

7	6	5	4	3	2	1	0
---	---	---	---	---	CH1 Int. Status	CH0 Int. Status	COS Int. Status

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15	14	13	12	11	10	9	8
---	---	---	---	---	CH1 Int_EN	CH0 Int_EN	COS Int_EN

COS Int. Status (bit 0): COS interrupt Status register

0: COS interrupt de-asserts

1: COS interrupt asserts

CH0 Int. Status (bit 1): Digital input channel 0 interrupt status

0: Ch0 interrupt de-asserts

1: Ch0 interrupt asserts

CH1 Int. Status (bit 2): Digital input channel 1 interrupt status

0: Ch1 interrupt de-asserts

1: Ch1 interrupt asserts

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Appendix A C/C++ DOS Function Library

A.1 Data Types

The following data types in the PCIe function library can be used in application programs. The following shows data type names and ranges.

Type	Description	Range
U8	8-bit ASCII character	0 to 255
I16	16-bit signed integer	-32768 to 32767
U16	16-bit unsigned integer	0 to 65535
I32	32-bit signed integer	-2147483648 to 2147483647
U32	32-bit single-precision floating-point	0 to 4294967295
F32	32-bit single-precision floating-point	-3.402823E38 to 3.402823E38
F64	64-bit double-precision floating-point	-.797683134862315E308 to 1.797683134862315E309
Boolean	Boolean logic value	TRUE, FALSE

A.2 List of Functions

Function
_7256_COS_Channel
_7256_CLR_IRQ
_7256_COS_Latch
_7256_DI
_7256_DO
_7256_DO_Read_Back
_7256_GET_IRQ_Status
_7256_Initial
_7256_INT_Control

_7256_COS_Channel

Enables the COS channel.

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Syntax

```
U16 _7256_COS_Channel (U16 boardID, U16
COS_Enable_Data)
```

Argument

boardID : Board ID to the specific board.

COS_Enable_Data : COS channel enable. 1 enables and 0 disables the corresponding channel.

Return Code

```
ERR_NoError
ERR_BoardNoInit
```

_7256_CLR_IRQ

Clears interrupt request.

Syntax

```
U16 _7256_CLR_IRQ (U16 boardID, U16 COS_CLR,
U16 CH0_CLR, U16 CH1_CLR)
```

Argument

boardID : Board ID to the specific board.

COS_CLR: Write 1 to clear COS interrupt request and 0 with no effect.

CH0_CLR: Write 1 to clear digital input channel 0 and 0 with no effect.

CH1_CLR: Write 1 to clear digital input channel 1 and 0 without any effect.

Return Code

```
ERR_NoError
ERR_BoardNoInit
```

_7256_COS_Latch

Latches digital input data after COS interrupt.

Syntax

```
U16 _7256_COS_Latch (U16 boardID, U16
*COS_Latch_Data)
```

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Argument

boardID : Board ID to the specific board.

COS_Latch_Data :Inputs digital input data when COS occurs, is erased when IRQ is cleared.

Return Code

```
ERR_NoError
ERR_BoardNoInit
```

_7256_DI

Reads data from all 16-bit digital inputs.

Syntax

```
U16 _7256_DI (U16 boardID, U16 *diData)
```

Argument

boardID : Board ID to the specific board.

diData :Returns 16-bit value from digital input port.

Return Code

```
ERR_NoError
ERR_BoardNoInit
```

_7256_DO

Writes data to the digital output port, energizing the Latching relay SET/RESET coils. All 16 relays can be controlled with this function.

Although the latching relay register map is 32-bit, the function allows latching relay control via 16-bit access, with 1 representing SET condition (1,0), and bit 0 the RESET condition (0,1).

Syntax

```
U16 _7256_DO (U16 boardID, U16 doData)
```

Argument

boardID : Board ID to the specific board.

diData :Returns 16-bit value from digital input port.

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Return Code

```
ERR_NoError
ERR_BoardNoInit
```

_7256_DO_Read_Back

Reads data back from digital output port control for all relay SET or RESET status.

Syntax

```
U16 _7256_DO_Read_Back (U16 boardID, U16 *doReadBackData)
```

Argument

boardID : Board ID to the specific board.

diReadBackData : value read back from digital output ports, with 0 indicating RESET condition and 1 SET.

Return Code

```
ERR_NoError
ERR_BoardNoInit
```

_7256_GET_IRQ_Status

Acquires current interrupt status.

Syntax

```
U16 _7256_GET_IRQ_Status (U16 boardID, U16 *COS_Status, U16 *CH0_Status, U16 *CH1_Status)
```

Argument

boardID : Board ID to the specific board.

COS_Status: COS interrupt status, where 1 indicates interrupt assertion, and 0 interrupt de-assertion

CH0_Status: Digital input channel 0 interrupt status, where 1 indicates interrupt assertion, and 0 interrupt de-assertion

CH1_Status: Digital input channel 1 interrupt status, where 1 indicates interrupt assertion, and 0 interrupt de-assertion.

Return Code

```
ERR_NoError
```

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```
ERR_BoardNoInit
```

_7256_Initial

Since IRQ and base_address (pass-through address) are assigned by system BIOS directly, each card must be initialized by this function before using other functions.

Syntax

```
U16 _7256_Initial (U16 *existCards, PCI_INFO *pciInfo)
```

Argument

existCards : The returned value indicates the number of PCI-7256 cards installed on the system.

pciInfo: A structure to detect PCI bus plug and play initialization information as defined by p&p BIOS. PCI_INFO structure is defined in ACL_PCI.H, and base I/O address and interrupt channel number are stored in pciinfo for reference.

Return Code

```
ERR_NoError
ERR_PCIBiosNotExist
ERR_BoardNoInit
ERR_InvalidBoardNumber
```

_7256_INT_Control

Controls interrupt source. For more details , see Section 3.7 Interrupt Control Register.

Syntax

```
U16 _7256_INT_Control (U16 boardID, U16 COS_Enable, U16 CH0_Enable, U16 CH1_Enable)
```

Argument

boardID : Board ID to the specific board.

COS_Enable: Enables/disables COS interrupt.

CH0_Enable: Enables/disables digital input channel 0 interrupt

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CH1_Enable: Enables/disables digital input channel 1 interrupt.

Possible interrupt source combinations are as shown.

CH1_Enable	CH0_Enable	COS_Enable	IRQ Source	IRQ Trigger Condition
0	0	0	Interrupt disable	--
0	0	1	COS interrupt	Change of state in the enabled channel
0	1	0	Ch.0 interrupt enable	Rising edge of DI channel 0
1	0	0	Ch.1 interrupt enable	Rising edge of DI channel 1
1	1	0	Ch.0 & 1 interrupt enable	Rising edge of DI channel 0 & 1
0	1	1	Not allowed (disable)	---
1	0			
1	1			

Return Code

```
ERR_NoError
ERR_BoardNoInit
ERR_INTNotSet
```

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Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

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- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

A Lithium-type battery may be provided for uninterrupted, backup or emergency power.



Risk of explosion if battery is replaced with one of an incorrect type. Dispose of used batteries appropriately.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

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